INSTRUMENT DESCRIPTION

The ATC321 is the replacement for the ATC311, and it is very similar to the ATC311 in most respects. The differences include:

- Upgrade to DM3 system with cable card slot.
- Audio & I/O modules have been combined into a single board.
- Single horizontal scan rate: 2.14H.
- No sub-woofer.
- DVI input changed to HDMI type.
- Elimination of Gemstar EPG & web browser.

CHASSIS DESCRIPTION

ATC321 Power Supply System

The ATC321 has two distinct power supplies.

1. The ACIN supply used to provide power for the DM3 module and the A/V-I/O module.
2. Deflection Power Supply which provides power for all the deflection and comvergence amp circuitry.

The ACIN Digital supply powers the DM3 module and provides standby power for the chassis.

AC-IN Power Supply

Functional Description

The ACIN /Digital power supply used for the ATC321 is a flyback-type, current-mode controlled, zero voltage switching (ZVS) topology utilizing a discrete control circuit and cold-side regulation. The circuit is functionally similar to those used for DVD, MMDS2, and other digital box applications.

A three-terminal error amplifier IC senses the 12 volt supply and provides feedback to the control circuit through an optoisolator. A power-fail signal is provided to the DM3 module to provide advance warning of an imminent supply voltage dropout.

Circuit Operation

The principle of this power supply is a flyback type zero voltage switching (ZVS) converter operating in the discontinuous mode.

A start-up resistor , RP604, provides the initial gate bias voltage for the MOSFET, TP601, which begins to conduct. A positive feed back winding (8-7) on the transformer LP601 begins to increase the gate voltage and causes TP601 to eventually saturate and begin the first cycle of operation. As the current in TP601 increases, the voltage drop across the current sense resistor, RP601 increases until a threshold level is reached. At this point the transistor TP602 turns on and the gate drive of the MOSFET is removed. The current flowing in TP601 drops quickly to zero and the energy stored in the primary inductance of the transformer is transferred to the resonating capacitor, CP609, causing the voltage across the capacitor to rise.

The rising voltage appears across the secondary windings (15-16) and causes a rectifier diode, DP612, to conduct when the voltage exceeds the voltage across the filter capacitor , CP624.

When DP612 conducts, the energy stored in the primary inductance of the transformer is delivered to the output capacitor and the load. When DP612 stops conducting, the energy remaining in CP09 resonates with the transformer primary inductance, driving the drain voltage of TP601 towards zero. When the drive voltage tries to go below zero the internal drain to source diode clamps the voltage near ground. The voltage of the drive winding again goes positive causing TP601 to turn on and begins the next cycle.

Regulation of the supply is accomplished by monitoring the 12VA voltage output. AC line isolation is provided by the optoisolator IP601. As the output voltage increases, the amount of current flowing in error amplifier IP602 increases. This causes an increase in the current through the optoisolator IP601. This causes the voltage at the base of TP602 to increase which adjusts the point at which the transistor turns on by varying the bias voltage at the base. The increasing voltage reduces the current trip threshold and the current in the MOSFET is decreased. This lowers the energy stored during each cycle and maintains a regulated output voltage.

Additional Design Features

- Switched Run Supplies 12VR & 5VR :
  The RUN_ENABLE voltage from the DM3 turns on the 12VR and 5VR supplies
- Power Fail Signal:
  The unregulated negative supply for the –5V follows the raw B+. TP101 and TP102 are normally on and TP103 is normally off. Thus the collector of TP103 is high. When raw B+ goes below a threshold, TP102 turns off and the collector of TP102 goes high. This turns on TP103 and thus the collector of TP103 goes low and issues a POWER_FAIL signal.

Deflection - Scan Power Supply

Overview

The main run power supply used for the ATC321 is a flyback-type, current-mode controlled that utilizes a discrete control circuit and cold-side regulation. A three-terminal error amplifier IC senses the scan supply and provides feedback to the control circuit through an optoisolator.

Control lines to the scan supply come from the Deflection_DAC, U14850, and include SMT_ON_OFF, REGB+_SW and B+_ALIGN. The DAC is controlled through the I^2C data bus from the DM3 module. SMT_ON_OFF is used to turn the scan supply On/Off and the B+ voltage level is controlled by the REGB+_SW and B+_ALIGN control lines.

Different taps on the SMT transformer are used to provide +31 Volts, +15 Volts, +20 Volts and a –20 Volt supply in addition to the scan supply. The tap supplies are further used to derive +24 Volts, +12 Volts and a +45 Volts.

A regulated +9 Volt run supply is generated by taking power from the +12 Volt standby supply and two regulated 12 Volt supplies are generated with discrete regulators on the +24 Volt and +12 Volt supplies.

The high voltage is monitored in case the voltage becomes excessive which could cause X-rays. In this case an X-ray protection circuit will shut the main supply down using the XRP_LATCH control line.

A line from the control DAC, B+_Align, is used to adjust the scan B+ voltage so that the raster width can be controlled.

The SMT_ON_OFF line from the control DAC is used to turn the Scan Power Supply On/Off. A separate TA1316_ON_OFF line is also used to turn the +9VR supply On/Off since the timing is different for the +9VR supply versus the Scan Power Supply

Operation

Raw_B+ voltage is supplied from the AC-IN board through connector J14101 whenever AC power is supplied to the instrument.

The supply is turned On/Off with control circuitry lines to the optoisolator U14150. When the set is in standby or in XRP Latch no current flows through Q14150 or the LED of U14150. The base of Q14151 is pulled to RAW_B+ through R14152 making the base forward biased. Q14151 pulls the base of Q14102 low forward biasing the transistor and causing current to flow. This pulls the Gate of MOSFET Q14101 low turning the scan supply off.

To turn on the scan supply the SMT_ON_OFF line goes high at the base of Q14150 causing current to flow through it and the LED in U14150. This in turn reverse biases the base of Q14151 turning the transistor off. This causes the base of Q14102 to rise turning it off . This causes the gate voltage of Q14101 to rise which turns on the MOSFET . When Q14101 begins to conduct the field on the primary of T14101 collapses inducing current into the secondary windings of T14101. As current increases in Q14101 the voltage across the current sense resistor R14109 increases until the base of Q14103 is forward biased. Once turned on Q14103 pulls down the base of Q14102 which turns the transistor on. This removes the bias voltage on the gate of Q14101 turning it off.

Current flowing through Q14102 and R14113 latches Q14103 off. Q14103 remains latched until the voltage across R14113 falls to a point where Q14103 turns off. R14113 is also connected to the output of the optoisolator, U14101, used to regulate the scan supply. If the voltage on the optoisolator side of R14113 is varied then the bias point on the base of Q14103 is raised or lowered. Varying the bias point on Q14103 will vary the on time of Q14101 varying the current transferred to the secondary of T14101. The secondary REG_B+_FBA supply is monitored by U14103 which increases or decreases the current flowing through the optoisolator U14101 based on the REG_B+_FBA loading. This provides the isolated feedback path with which to regulate the scan supply.

The fine adjustment of the scan B+ voltage is accomplished by varying the DAC voltage applied to B+_ALIGN line to Q14108 which in turn controls the feedback reference voltage. This base voltage is adjusted in the factory and stored in memory for proper scan width.

The +9Vr supply is controlled by the control line TA1316_ON_OFF. This control line comes directly from the DM3 module via J14801. When the control is taken high the base of Q14111 is forward biased and lowers the base voltage of Q14110 which turns on. With Q14110 on the +12Vs is supplied to the 9 volt regulator U14104 which produces +9Vr for the Deflection Processor, U14802, and associated circuitry.

Deflection

The ATC311 deflection system consists of two levels, Low Level Horizontal and Vertical Processing and the Yoke Drive Output circuitry.

The low level deflection processing is performed using a chip set on both the Back End Processor (BEP) module and the deflection module which are mated and aligned in the factory.

The BEP is populated with Backend Processor (BEP) IC, IV901, and the switching IC, IV902. The horizontal PLL and H/V countdown circuits are contained in IV901, while IV902 is used to select the source of the deflection timing signals.

The vertical ramp generator, the East West parabola generator, and the dynamic focus waveform generators are contained in U14802 on the deflection board. The deflection board also contains a 4k EEPROM, U14803, so that alignment data can be stored locally. There is also an octal DAC, U14850, which is used to minimize the number of hardware connections between the deflection board and the DM3.

The deflection pcb also contains the main run supplies mention previously, the horizontal drive circuit, the horizontal output transistor (HOT), IHVT and vertical yoke drive circuit.

Backend Processor Operation

IV901, located on the BEP module, is a component signal and sync processor for use in multiple frequency applications. The main source of power for this IC is +9Vr. The +9Vr supply is switchable via the TA1316_ON_OFF control line from the DM3 to allow switching off the BEP module during Standby mode. An I^2C bus interface is used for adjustment and alignments. Input signals to the deflection system have a horizontal frequency of either 2H or 2.14H and can be from either the

Deflection - continued

DM3 or an external source from the A/V-I/O module.

The DM3 deflection signal lines to the BEP are labeled DEINT_H and DEINT_V and are connected to IV902 at pins 14 &15. The external signals coming from the A/V-I/O board are labeled HD_H_SYNC and HD_V_ SYNC and are connected directly to IV901 at pins 13 & 12 respectively. These signals are selected by the system control code depending on which input is used as the source.

The matrix switch, IV902, is used to switch timing signals depending on the mode of operation. When the video is from the DM3, the switch routes DEINT_H and DEINT_V drive on pins 14 & 15 of IV902 to pins 15 & 16 of IV901. When the sources are 2H or 2.14H external component signals, the switch (pins 2 & 12) is used to route the VP_OUT timing signal from IV901through IV902 to the DM3 along with the FBP signal from the IHVT on the deflection board. These timing signals are sent to the DM3 to synchronize the OSD system to the external video signal.

The output of the HPLL is the H_OUT signal, which is used to drive the horizontal driver circuit on the deflection board. The duty cycle of the H_OUT waveform can be adjusted by I^2C bus.

A vertical timing pulse is supplied from IV901 to synchronize the various vertical rate timing generators in U14802 deflection processor. This pulse is generated by the vertical countdown circuit. Vertical frequency characteristics are controlled by I^2C bus.

Horizontal and vertical blanking signals are also generated in IV901. An external input is available for use with an analog blanking signal generated by IV901.

U14802 - Deflection Processor Operation

U14802 is the deflection processor IC, which incorporates EW pin correction, vertical ramp generation and distortion correction, and dynamic focus correction, circuits. The various IC functions are adjustable via the I^2C bus. The same +9 volt regulator used by IV901 also supplies this IC.

U14802 requires two timing inputs to synchronize to system vertical and horizontal timing. A vertical rate timing pulse is received from IV901 as mentioned before. A FBP pulse from the horizontal output circuit is used to supply Horizontal timing. The vertical input pulse leading edge is used to generate an internal vertical pulse using the TC filter at pin 22. This pulse is used to generate a vertical rate ramp by utilizing the Vramp filter at pin 23. This common ramp is used to generate all of the vertical rate waveforms generated by the vertical, EW, and DF circuits. For the ATC321 application, the FBP input is only used to drive the HDF section of the IC.

U14802 has an EHT input which allows beam current information to be supplied to both the vertical and EW pin correction circuits. This input can be used to compensate for raster size change due to less than ideal high voltage regulation. The IC has separate I^2C bus adjustments of the gain of the compensation circuits for vertical and EW so that the performance can be independently optimized.

Horizontal Deflection

The horizontal output circuit generates the high current ramp waveform used to drive the horizontal yokes. It also drives the flyback transformer, which in turn produces the supplies necessary for picture tube operation. The supplies include the High Voltage, the focus supply, the screen supply, cathode B+, and the heater voltage.

The horizontal yoke current is provided by a circuit consisting of a switch (HOT and damper diode combination), the primary inductance of the IHVT, a retrace capacitor, the trace capacitor (S-Shaping capacitor), and the horizontal yoke coils.

The voltage supplies provided by the horizontal deflection system are derived from secondary and tertiary windings on the IHVT. These supplies are provided for the video amplifier, the CRT, and the horizontal driver.

The low level signal processing circuits for the horizontal deflection system are contained in IV901 and include the horizontal sync processor.

X-Ray Protection Circuit

High Voltage shutdown is accomplished by sensing a secondary IHVT pulse, rectifying it, and if the sensed signal exceeds safe limits, driving the SMT_ON_OFF line low. Reporting to the microcomputer is accomplished by reading the “X-Ray Protection bit” of the U14802 IC. The microcomputer will then turn off the power supplies, turn the power supplies back on, and attempt to restart the instrument.

The X-Ray Protection (XRP) latch is an open-collector output that removes the Regulated B+ Power Supply by pulling the control line XRP_LATCH low if a fault is detected. Also an X-Ray Fault is reported to the Control System over the I^2C bus when IC, U14802, reports a “Power Supply Disturbance” on pin 17. The first occurrence of the XRP is interpreted as a fault condition, and the DM3 will attempt to restart the Main Power Supply after a reboot procedure by toggling the Main Power On control. The x-ray protection circuit is aligned to set the latch before the anode voltage can rise to a level where it can induce CRT radiation exceeding acceptable limits. This circuit produces a DC voltage that is proportional to the CRT anode voltage. This voltage is compared to a discrete voltage reference.

E-W Pincushion Correction

East- West pincushion correction and width adjustment are driven by a linear pincushion driver. The parabola used to develop the correction waveform is generated in IC, U14802. U14802 provides bus control of the horizontal width and pin amplitude as well as horizontal trap correction and corner correction. In addition, a voltage developed across the high voltage return resistor is summed at the pin driver to compensate for the decrease in width that occurs as the high voltage increases with decreasing beam current.

Vertical Deflection

The vertical deflection processing is done in two parts. First, IC IV901 includes the sync separator and countdown circuit, that provides the negative going vertical rate pulse, VP_OUT to IC, U14802. This pulse is also used to synchronize the digital convergence. Second, IV901 also develops the vertical blanking signal, which starts with the vertical pulse and ends at a programmable line count. An additional programmable blanking signal is provided for use in the compressed vertical deflection mode that starts before the vertical sync pulse.

IC U14802 receives the VP_OUT pulse at its pin 21 and develops the vertical deflection ramp, at pin 6, V_FB . The IC also provides a dc reference at pin 5, VD_REF, which tracks at twice the ramp center value. These two signals after a source resistor and restive divider respectively become V_RAMP and V_REF respectively, and are coupled differentially to the vertical output IC, U14501, which drives the yoke. Vertical kill is achieved by I^2C bus control of U14802.

U14802 develops the vertical ramp using a ramp capacitor at pin 23, VRAMP_FILTER. If this capacitor has significant changes in series resistance during aging, the ramp amplitude and DC value can be adversely affected. A timer involving the components at T filter, pin 22, sets the reference ramp clamp time. If this time constant were too long, it could cause flat scan at the top of the picture.

Digital Convergence

Overview

The Digital Convergence Integrated Circuit (DCIC) and amplifier system generates 6 convergence yoke drive currents that correct the geometry of the 3 colored pictures from the projection tubes such that they are rectilinear and convergent on the PTV screen. For horizontal and vertical directions in each of the three colors, values for a matrix of 13 vertical points by 16 horizontal points (1248 total) are stored in non-volatile digital memory. This information is converted by digital to analog converters into 6 analog signals that are power amplified to supply the drive for the convergence yokes. In the vertical direction the signals for scan lines that are between the lines with adjustment points are calculated by the DCIC using smoothed interpolation. In the horizontal direction the DCIC output is digital steps that are smoothed internally by digital filtering and externally by analog low pass filtering. The data values for both convergence and focus are adjustable via I^2C bus commands. Each data point can be individually changed (dynamic adjustment) or the entire raster of a color may be moved (static adjustment). The effects of the Earth’s magnetic field change with the placement of the TV can cause picture distortion and misconvergence. These distortions are automatically corrected using a micro processor and data from optical sensors located around the edge of the screen. The customer can then optimize the red and blue center convergence to green. A video test pattern is generated by digital convergence to aid in the customer and service adjustments. Convergence adjustment is required for the initial factory setup, when a major component is replaced or when the receiver is moved to a different magnetic field. In the factory a vision system and external computer are used to initially determine the convergence data values. In field service a PC can be used with Chipper Check Software to speed the alignment process.

Automatic Alignment

A menu item starts the autoconvergence function. If a sensor fails to work, auto alignment will be aborted. Light sensors are placed around the edges of the picture. These sensors sense lighted target edges in each of the three colors. Convergence parameters are then changed by the micro computer to adjust the picture size, shape and position to compensate for picture movement due to magnetic fields, electrical drift or mechanical drift. This system should locate the target edges of all 3 colors within +/- 1mm of the sensor center.

At the start of auto alignment, the screen will blank and color blocks will appear on screen in the screen section for each of the eight (8) sensors in sequence. Brightness is calibrated for each color and sensor display then the values are stored in memory. Next a block shaped pattern will be displayed in the area for each sensor at each color. These lighted areas will be moved by the static convergence adjustment in a preset search pattern until an edge location is detected. An edge is calculated by detecting the edge position from opposite directions on the edge and averaging the two detected locations

A memory record is kept of the required horizontal or vertical movement at each sensor. In the factory, after convergence alignment, a similar process is used to locate the sensors and record their positions. The values of the current sensor locations can then be used to calculate the difference between the current values and the factory recorded values. The picture can then be repositioned and resized to restore proper geometry and convergence. Since there is no center sensor, the average of the screen edge sensor locations is used to shift the center. A small center convergence error may be introduced by this process. To optimize the center convergence, the customer can fine adjust the match of red and blue to green at the picture center using the convergence menu. To correct the errors introduced by moving the red or blue centering, the micro processor will then recalculate the convergence grid for the entire picture using the new center values.

Operation

The ATC321 convergence system has essentially the same operation and circuitry as the ATC311.

Convergence Operation -continued

Power Amplifier

The power amplifier is similar to the MMC102 circuit. A dual transistor is used at the amplifier input to improve temperature drift performance. The power transistors are the same as used in PTK195 instruments. The amplifier requires only +/-20V supplies so low voltage drive transistors can be used. Signal mute switching is incorporated into the amplifier eliminating it from the generator circuit.

The convergence amplifier compares the voltage applied to the input to the voltage across the sense resistors and supplies whatever yoke current is required to make these voltages equal. At TV turn on the amplifiers are muted because the input signals will be inappropriate until after the convergence IC is programmed from the EEPROM stored values. The two current source transistors can be turned off with the AMPMUTE control signal.

The circuit uses multiple sense resistors to increase their resistance accuracy and reduce thermal drift. Ferrite beads are used to stop high frequency oscillations of the power transistors. A bias transistor is used in the vertical amplifiers to reduce the transients due to cross over of the power amplifier when the input signal switches polarity. The horizontal amplifiers do not use the bias transistor or emitter resistors. The vertical power stage emitter resistors prevent shoot through currents. The crossover picture distortion is not visible for horizontal direction convergence corrections.

Opto-sensor Detector

The detector sensitivity circuits used in previous product have been replaced with color detecting switches. These lower detector sensitivity for red and blue. This eliminates sensitivity setup time from the auto converge sequence. The AC coupling has been simplified and a one shot pulse circuit has been added to eliminate short light detection pulses that might be ignored.

Convergence Power and Disconnect Switch

In previous products the convergence has had its own separate power supply that turned off if a fault existed. For the ATC311, convergence power comes from the chassis run supply. If the run supply is turned off, trouble shooting is very difficult. Convergence fault protection comes from two transistor switches that open and latch when the normal power supply current is exceeded in either the +20V or –20V convergence supply.

Over current is detected by comparing the voltage drop across a current sensing resistor against a fraction of a 20V supply. A differential transistor circuit is used to compensate for temperature. The latch is a NPN/PNP feedback pair. Once the latch is on, chassis power must be turned off to reset it. The +20V switched output controls the –20V switch so that +20V comes on first and turns off last. A filter circuit is used in the over current detectors so that a fault must exist for several milliseconds to trigger the latch. This allows high currents at start up to charge the filter capacitors in the convergence circuits. Very high currents that might damage the switch transistors are prevented by drive limiting zener diodes that limit drive voltage to the switch transistors.

Video - Chroma Processing

Overview

The video processing in the ATC321 is broken into several sections: chroma processing, deinterlacing processing, luminance processing, color difference processing, external YPrPb processing, OSD RGB processing and RGB output processing. The chroma decoding is performed on the A/V IO by the chroma decoder, IC101. Deinterlacing is also discussed elsewhere.

Luminance Processing

Except for the deinterlacing, the luminance processing is done in the back end processor, IV901. IV901 has two component video input ports, but only the Y1 and PrPb1 inputs are used. Luminance from the DM3 is applied to the Y1 input through a clamping capacitor. The luminance signal undergoes the following processing:

- Black Stretch
- Black Level Correction
- Dynamic Gamma Processing
- Controlled DC Restoration
- Sharpness Control
- Edge Replacement
- High Frequency White Peak Limiting
- Sub Contrast
- UniColor (Ganged Contrast and Color Level)
- Clamping
- White Peak Limiting
- Output Gamma Processing
- Half Tone Processing

Beam limiting is done in the clamping and UniColor stage. After half tone processing, the luminance is applied to the RGB matrix in IV901. Because the peaking filtering is in the IC, it is possible to generate a first derivative signal that can be used for SVM. Because of the length of cable from IV901 to the CRT board, the SVM signal is coupled via an NPN-PNP emitter follower circuit. The two transistors are used to maintain temperature stability of the DC operating point.

Color Difference Processing

As stated above, the chroma decoding is done on the A/V IO in IC101. The output of IC101 is YPrPb and is applied through IT701 to one of the YPrPb inputs to the GPIP IC on the DM3. The output of the GPIP IC is a digital CCIR 656 stream and is fed to the MPEG decoder on the DM3. The DM3 then provides 2.14 H luminance and color difference signals to the Backend Processor. The signals are Pr and Pb: the signal amplitudes are 0.7V peak to peak on a 100% color bar signal.

External 2.xx H YPrPb color difference signals are fed into a High Definition A/D converter, IT501, which provides a digital stream to the MPEG decoder on the DM3. The digital signal is then processed in the MPEG decoder and output to the Back End Processor as above.

The Pr and Pb signals are capacitively coupled to the Cr/Pr and Cb/Pb 1 inputs. The color difference inputs are clamped during the horizontal blanking interval. From the Cx/Px 1 input the signals are routed through switches that are ganged to the luminance switch. From the switch the signals go into a switchable matrix that converts the input signals to YUV format. The matrix will convert signals matrixed according to either SMPTE 170M or SMPTE 274M (NTSC/SDTV or HDTV) to standard color difference levels. This allows the system to process the color difference signals properly regardless of standard. In the ATC321, the switch will be set for SMPTE 274M at all times.

Following the matrix conversion, the YUV signals are converted to YIQ for use in the Auto Flesh circuit. Auto Flesh operates by reducing the level of Q signal associated with colors in the +I portion of the color difference space. Auto Flesh can be disabled, and it is bus controlled. After the Auto Flesh stage, the I and Q signals are converted back to U and V.

After the I/Q to U/V conversion the signals undergo the following processing:

- Tint Control
- Color Edge Correction
- Color Control
- UniColor (Ganged Contrast and Color Level)
- R-Y Rematrix (Bus Programmable)
- G-Y Matrix (Bus Programmable)
- R-Y Color Gamma
- Half Tone
- Blue Enhancement
- Clamping

After clamping the R-Y, G-Y and B-Y signals are applied to the RGB Matrix in IV901 with the luminance to generate RGB signals. Beam limiting is done in the UniColor stage, just as it is for luminance. This means that the RGB signals are controlled by beam limiting, but by means of controlling the luminance and color difference separately.

OSD RGB Processing

Unlike the ATC311, the OSD for external 2.xx YPrPb will be overlaid on the video because of the processing being done in the MPEG decoder. Therefore, the slave mode of operation that was used in the ATC311 is not used. There will be no usage of the RGB OSD inputs in IV901.

RGB Output Processing

The RGB signals from the Video RGB matrix in IV901 are applied to variable gain stages, two of which are controlled by the bus. Which two of the three are controlled is selectable by the bus. The control circuitry in the ATC321 will control the gains of the Red and Blue channels, leaving the Green channel at fixed gain. The gains of the amplifiers are adjusted to achieve the desired display color temperature. The values of the Red and Blue amplifier gain will be modified to change color temperature from Normal to Warm or Cool. To set the color temperature for Warm, the Red gain will be increased and the Blue gain will be reduced. To set the color temperature for Cool, the Red gain will be reduced and the Blue gain will be increased.

After the RGB signals are gain controlled, they are applied to a set of clamps. These clamps are used to set the output DC levels of the RGB signals. The clamps are controlled in two ways. It is possible to set the clamp level, and thus the DC level, via the bus. This mode will be used at initial turn on to ensure that the AKB system does not drive the cathode-grid diode to forward bias. The normal mode of operation in the ATC321 will be with AKB on. A series of time-multiplexed pulses is applied to the video at the end of vertical retrace. These pulses generate beam currents in the three CRT guns that are fed back to the TA1316AN. The currents are converted to voltages, clamped and compared to internal reference voltages. The AKB system adjusts the DC levels of the outputs until the voltage generated from the beam currents match the internal references. The references are adjustable via the bus, and can be used to adjust low light color temperature. The reference values will be changed when the color warmth is changed from normal to cool or warm. The AKB system maintains the black level of the signal at the cathodes due to the feedback. IV901 has an internal clamp to remove CRT leakage currents during measurement; however, the range is not sufficient to remove the offset currents from the Kine Driver IC's, U25101/301/501, in the worst case from the current being generated by the CRT. Therefore the clamping scheme will be the same as in the ATC311CR.

After the RGB output clamps, the video signals have horizontal and vertical blanking applied to them. The blanked signal is applied to output buffers and is output on the RGB pins of the IC.

Because of the length of cable from the Back End Processor to the CRT board, an NPN transistor buffers the output of IV901. To maintain temperature stability of the DC operating point, an additional PNP emitter follower is used. The blanking of the RGB signals is limited in its negative excursion. This is done to keep the Kine Driver IC's out of deep cutoff so that they come from horizontal blanking without excess time delay. A divider on the emitter of the NPN emitter follower adjusts the minimum blanking level.

Video-Chroma Circuit Functional Description

For detailed video-chroma circuit description, refer to the ATC32x training manual included in this ESI publication.

Audio Processing

Features

Components of the ATC32x audio system are located on the AV I/O module and the DM3 assembly. All ATC32x-series models utilize the same basic audio system. The main difference is the number of I/O jacks provided. The audio jacks are arranged two-high so that the top row can be left off for slim instruments.

Jacks always present (bottom row):

- Variable Out L and R (“HiFi”).
- Center Speaker Input
- Subwoofer line-level out.
- Record Out (L, R, and Video).
- Composite 1 Input (L and R)
- Component 1 Input (L and R)

Optional jacks (top row):

- Center line-level output.
- Rear-channel line level outputs
- Composite 2 Input (L and R)
- Component 2 Input (L and R)

Overview

The ATC321 audio system hardware resides on two assemblies. The A/V-I/O module contains the IT501 A/V switch and all the baseband I/O jacks, op-amp-based buffers and level-shifters to interface with the DM3 and jacks, a post-volume control, the audio power amplifier, and the speaker switching. The DM3 module contains (from an audio perspective) the tuners, Nextstream link IC, MPEG decoder, and mixed-signal audio processing IC, IS101. These receive the RF inputs and decode the audio formats (BTSC and ATSC).

IS101 performs most of the baseband audio processing – stereo/SAP (BTSC) decoding, graphic equalizer, subwoofer support, and SRS feature processing. The A/V-I/O module performs the baseband input switching, volume control, center and rear-channel synthesis, and power amplification and speaker switching. On the DM3 module, the tuner and IF demodulate NTSC and HDTV channels. In NTSC mode a 4.5MHz sound subcarrier is provided to IS101. IS101 demodulates stereo and SAP. In HDTV mode, a digital bitstream is recovered. The digital system (MPEG decoder) decodes Dolby Digital and provides a Dolby Virtual Surround 2-channel (Lt and Rt) mixdown in I2S form to IS101. IS101 also provides an asynchronous I2S interface for customer use. IS101 receives analog audio from the AV I/O module via a SCART input, and provides two analog audio ouputs to the A/V-I/O module via the SCART outputs.

The AV switch, IT501 on the A/V-I/O module selects the desired baseband (Aux) input. The switch output is routed to the DM3 module where it is applied to the SCART4 input of IS101. In baseband–input mode IS101 selects the SCART input and digitizes it and sends the I2S stream to the MPEG decoder where lip-sync delay is performed if needed. The stream is returned to IS101 for processing (graphic equalizer, Sound Logic, SRS). The audio is converted back to analog and leaves via the SCART outputs at line level, being routed to the A/V-I/O module for final processing.

As indicated above, IS101 has access to the NTSC (via internal decoding) and HDTV (via I2S from the MPEG decoder) audio signals. When one of these is selected (instead of baseband inputs), the needed processing is performed and the signal is converted back to analog and leaves via the SCART outputs. The analog audio is received onto the A/V-I/O module via differential-input amplifiers to eliminate ground loops. The signal from SCART2 is the Record output at fixed level; the diff-amp also drives the record jacks. The signal from SCART1 is the main output and is sent to several processing blocks.

IS101 performs volume control so that the main signal on SCART1 can be sent to the following blocks (power amp, etc). The volume-controlled signal, from either the SCART1 diff-amp directly or the volume control, is routed to the several blocks - the headphone driver IC, a buffer-amp to drive the variable-output jacks (HiFi jacks), the main power amplifier, and op-amp-based sum and difference blocks that generate the center and rear line-level outputs. The output of the headphone driver IC, IA851, is routed via connector and cable to the FAV module where the headphone jack is located. A switch on the headphone jack provides a logic level that the headphone has been plugged in. A port on IT501 conveys this information to the system controller so that the speakers are shut off (by muting the power amplifier).

A class-D stereo power amplifier IC, IA901, is utilized as the main audio power amp. The majority of models will be rated for 15+15 watts and the supply voltage has been chosen to deliver that power to the rated 8-ohm load. IA901 has a control pin that puts it in standby mode when the set is off or when the speakers are turned off in the menu. This pin is controlled by a port on the IT501 switch IC. The power amplifier receives its main supply from the AC In module. Nominal voltage is plus and minus 19 volts. Although the power amplifier operates in split mode with direct output coupling, a DC Detector function is not required because there are no external speaker jacks.

Two speaker-output arrangements are supported. The power amp outputs can be routed directly to the internal speaker connectors, or switching for an external center-channel speaker-level input can be inserted. External speaker jacks (outputs) and the “matrix” surround feature are not supported. The switching for the external center channel input is relay-based instead of the mechanical switch used previously. As before, the set’s speakers will be placed in series and isolated from the internal circuitry in this mode. This feature is selected by menu and a port on IT501 controls the relays. Since the A/V-I/O module will be built in different versions with and without this hardware, a bit in the video EEPROM can be set to cue the control system to provide the correct menu.

“Center” and “rear” line-level outputs are created by an op-amp-based summer and differencer. The levels of these outputs track the main the volume (since they are dirived from the main signal).

The chassis control system convolves the user inputs and sends control data to the various components to achieve the needed mode.

The DM3 is controlled to select the following functions:

- Tuning and type of input channel decoded
- Type of decoding (Dolby Digital and options, BTSC, etc)
- Application of delay
- Baseband or off-air
- Application of Automatic Volume Leveler (Sound Logic)
- SRS processing
- Graphic Equalizer
- Volume Control (if needed)

The A/V-I/O Module is controlled to select the following functions:

- Volume control
- Headphone plug-in detection
- Main power amplifier mode (standby/play)

Audio Circuit Functional Description

For detailed audio circuit description, refer to the ATC32x training manual included in this ESI publication.