CIRCUIT OVERVIEW

Caution: Hot Chassis

In all versions of this chassis, the AC input, Horizontal Output and B+ Regulator circuits are considered "HOT" and should be serviced using an isolation transformer.

AC Input

The 150V raw B+ is derived from the AC line through a bridge rectifier consisting of CR4001, CR4002, CR4003 and CR4004. Initial Regulator start up voltage is derived from the raw B+ source via resistor R4003. After the regulator is up and running this voltage is replaced by a run voltage derived via CR4101 and R4149.

Both Raw B+ and Regulated B+ are present any time AC line voltage is applied to the instrument. The degaussing operation is activated by the system control micro via R3124, Q4202, Q4201, and relay K4201.

+5 Volt Standby Supply

Standby supply voltage for the System Control Micro, U3101, is supplied by the +15VB supply from the regulated power supply, via the +5V Standby Regulator Transistor, (Q4601).

Start Up

The regulator circuit is activated any time AC power is applied to the instrument, therefore start up only involves activation of the supply voltage to pin 26 of the CTV IC U1001.

When the power button is pressed, the system control micro will output a high from pin 38 (U3101). This high is applied to the base of Q4306 turning it ON. When Q4306 is turned on Q4304 will be turned ON. When Q4304 is turned on, a low is placed on the base of Q4301 turning Q4301 OFF. When Q4301 is turned off, a high is placed on the base of Q4305 turning ON Q4305, thus providing the supply voltage for pin 26 of the CTV IC U1001.

Run Supply Voltages

The +12V (Q4702) and +9V run (Q4704) supplies are activated by the +26V derived supply from the secondary of the IHVT (T4401). The +5V run supply (Q4703) is activated by the +12V run supply. The run supply sources have additional circuit components to maintain regulation.

Regulated B+

Regulated B+ control is of the pulse width modulated (PWM) type. The main power source for the regulator circuit is the +150V raw B+. Initial start up voltage is supplied to pin 16 of the regulator IC (U4101) through dropping resistor R4003. When the regulator circuit is up and running the operating supply for U4101 is provided by a pulse from a winding on transformer T4102. This pulse is rectified by CR4101 and applied to pin 16 of U4101 through resistor R4149. The +150V raw B+ supplies power for the output transistor Q4101.

Slow startup is provided by capacitor C4105 at pin 9 of the IC (U4101). The shut down latch is controlled by capacitor C4104 at pin 8 of the IC. The internal oscillator frequency is controlled by resistor R4105 at pin 11 and capacitor C4107 at pin 10 of the IC. Standby operation of the regulator is controlled by the same pulse from transformer T4101 which provides the run supply for the IC. This pulse is rectified by CR4106 and applied to pin 6 of the IC through R4117, R4102 and standby adjust control R4113. It is aided in its efforts by a feedback voltage from pin 7 of the IC via resistor R4103 and capacitor C4106.

The PWM drive pulse is output at pin 14 of the IC and applied to the base of output transistor Q4101. The ON and OFF operation of the output transistor is used to transfer energy from the primary windings to the secondary windings. This transferred energy provides pulses in the secondary windings which are rectified to produce several operating voltage supplies for the instrument.

Regulation is accomplished, when the instrument is in the operational mode, by sensing the +143.5V regulated B+ source and a horizontal pulse from the IHVT (T4401) pin 7. The regulated B+ is dropped down to a usable value by resistors R4114, R4148, R4116 and R4115 and applied to the base of Q4105. The collector of Q4105 feeds the emitter of Q4106. A horizontal pulse is applied to the base of Q4106 through R4144, JW306, R4143, C4138 and R4142. The output of Q4106 is then applied through Q4107, T4101, voltage divider R4137 and R4135 to pin 2 of the regulator IC (U4101) where it is used to control the duty cycle of the pulse width modulator internal to the IC.

Transistor Q4109 is used to assure that no pulses get through Q4106 when the instrument is in the OFF mode. Q4110 senses the high voltage return line. In the event that an excessive amount of beam current is drawn through the high-voltage circuit, Q4110 will conduct turning on Q4108 thus reducing the reference voltage supplied to error amp transistor Q4105.

If a fault should occur causing an overcurrent situation in the output stage, it will be detected through the overcurrent sensing circuit (R4109, R4108 and C4109) located in the emitter circuit of Q4101 and connected to pin 3 of U4101.

Horizontal Deflection

Composite video is fed to pins 40 and 43 of the CTV IC U1001 where, internally, it is applied to a sync separator stage. Horizontal sync is output from the sync separator and applied to a horizontal AFC stage. A flyback pulse from pin 7 of T4401 and controlled by horizontal phase control R4306 is capacitively coupled (C4313) to pin 21 of U1001 where, internally, it is also applied to the horizontal AFC stage. A horizontal AFC pulse from pin 4 of T4401 is input to U1001 at pin 24 and combined with the output of the horizontal AFC stage. The resultant signal is then used to control the 32xH VCO oscillator stage. An external crystal sets the operating frequency of the 32xH oscillator and is connected to pin 25 of U1001. The output of the 32xH VCO is applied through a horizontal countdown stage to a horizontal output stage and a drive pulse is output at pin 23 of U1001.

CIRCUIT OVERVIEW (Continued)

Horizontal Deflection (Continued)

The horizontal drive pulse is then applied to horizontal driver transistor Q4302. Output from the driver transistor is then transformer coupled to the horizontal output device Q4401. The output of Q4401 is then used to drive the IHVT (T4401) primary, as well as the horizontal deflection yoke winding.

X-Radiation Protection

The filament pulse from pin 5 of the IHVT (T4401) is rectified by CR4901 and applied to the cathode of zener diode CR4902 through a precision voltage divider consisting of R4903 and R4904. If this voltage exceeds 10 volts, the zener conducts and a DC voltage is applied to pin 22 of the CTV IC (U1001). This activates the x-ray protection circuit (internal to U1001), which in turn inhibits the horizontal drive signal at pin 23, causing the secondary supplies to drop. The +26V secondary supply is used to turn ON the +12V and +9V run supply transistors. Therefore, when the secondary supplies drop, the +12V and +9V run supplies also drop.

The system control micro, (U3101 pin 2) detects x-ray shutdown by monitoring the +9V run supply. When the instrument shuts down, the DC voltage at U1001 pin 22 drops to zero and the x-ray protection circuit (internal to U1001) resets. After approximately 2 seconds, the system control micro responds by turning the instrument back ON, trying to restart horizontal deflection. If the fault is still present, the x-ray protection circuit will cause the system to shut down again. This cycle will repeat until either the fault is removed or the instrument is turned OFF.

Vertical Deflection

The vertical deflection system in this chassis is a switched vertical type, similar in operation to a switched power supply. The vertical reset pulse, generated by the CTV (U1001) and output at pin 29, is applied to the base of ramp reset transistor Q4505. The ramp capacitors C4519 and C4518 are charged through resistor R4507 from a nominal +31V source developed by a 90V p-p horizontal pulse generated in the secondary windings of the IHVT (T4401 pin 7). This pulse is applied to a voltage divider consisting of R4539, R4514 and height control R4522. It is then rectified by CR4502 to develop the nominal +31V source to charge ramp capacitor C4519. Vertical height is determined by varying the 31V source voltage between 39.7V for maximum height and 22.6V for minimum height.

When the positive portion of the reset pulse (from pin 29 of U1001) is present, Q4505 turns ON, discharging ramp capacitors C4519 and C4518. At the same time Q4505 turns on, Ramp Generator transistor Q4506 (a darlington type transistor) turns ON limiting the p-p voltage of the pulse present at the emitter of Q4506 to approximately 1 volt.

When the reset pulse (applied to the base of Q4505) goes negative, Q4505 will turn OFF allowing ramp capacitors C4519 and C4518 to recharge. However, C4519 will recharge at a different rate (due to resistors R4521 and R4525 being in the circuit) and form the proper waveshape of the ramp pulse. The vertical kill transistor (Q4202) is activated at instrument turn-on time to kill vertical deflection and allow for degaussing action to take place. When Q4202 is turned on, Q4201 is turned ON. This activates the degaussing relay allowing the degaussing action to take place. Also, when Q4202 is turned ON, the ramp reset switch transistor (Q4505) is driven into saturation thus defeating vertical deflection.

The ramp pulse is fed through R4509 where it is combined with the current sense resistor (R4505 via R4510) pulse, which is of the opposite polarity, and the DC feedback voltage from the vertical yoke windings. The sum of these signals is then applied to pin 3 of the voltage-to-phase converter IC (U4501). Capacitor C4520 is the "S" shaping capacitor and is used to achieve linearity at the top and bottom of vertical scan. The horizontal reference ramp pulse (applied to pin 2) of the voltage-to-phase converter IC is developed from the 90V p-p horizontal pulse generated in the secondary of the IHVT (T4401 pin 7) and rectified by diode CR4501. Q4507 is turned ON during channel change to draw additional current from C4522 thereby reducing the gated ON time of the SCR, this prevents height bounce during channel change. A positive gating pulse is output from pin 1 of the error amp IC (U4501). It is modulated at a horizontal rate and used to gate SCR501 ON and OFF.

A dedicated winding on the IHVT (T4401 pins 2 and 3) provides a 160V p-p pulse during horizontal retrace. The current path is through CR4504, the inductor winding on T4301, the dedicated winding on the IHVT, the vertical yoke windings, AC coupling capacitor C4503, current sense resistor R4505, and the chassis ground circuit. During the vertical trace interval this horizontal retrace pulse is rectified by CR4504. This action places a charge on capacitor C4511 and builds up current in the vertical yoke windings. The SCR is being gated ON for short periods of time to limit the amount of peak current being built up in the vertical yoke windings. As vertical trace is pulled to the center of scan, the SCR is allowed to remain ON for longer periods of time further limiting the positive current in the yoke. When vertical trace reaches the center of scan the gated ON time of the SCR nearly equals the OFF time reflecting nearly equal amounts of positive and negative current (effectively zero current) in the vertical yoke windings. At this time, the gated ON time of the SCR is gradually increased to reflect a negative current flow through the vertical yoke windings. This pulls vertical trace from the center of scan toward the bottom of scan.

Vertical retrace is accomplished by turning the SCR OFF for a relatively long period of time. This allows the peak current in the vertical yoke windings to build up at a fast rate. Then the vertical trace is resumed.

System Control

The micro controller (U3101) controls all functions of the instrument. It interprets commands from the front control panel keyboard (as well as the remote control hand unit) and sends appropriate commands to various circuits of the chassis. Functions performed within the micro controller are: D/A control, OSD generation, IR signal processing, sync presence detection, and AFT A/D conversion. Timing of communications is controlled by a 4MHz clock internal to the micro.

CIRCUIT OVERVIEW (Continued)

System Control (Continued)

The micro is responsible for channel tuning, band switching, on screen display generation, and quasi-digital control over video and audio setup parameters (brightness, contrast, color, tint and volume). Video and audio parameters are controlled by varying the digital outputs of the micro, which are then filtered to provide DC control voltages for the video and audio circuits.

Micro Reset

The Micro Reset circuit controls pin 1 of the micro. It consists of resistors R3114, R3115 and zener diode CR3101 with the +15V regulated source as the input signal. The +5V standby source is derived from the +15V regulated source. The value of CR3101 (5.6V) allows the +5V standby source to be established before pin 1 of the micro becomes high. Likewise, during AC dropout, pin 1 will go low before the +5V standby source begins to drop. The purpose of R3116 and CR3102, connected between the reset circuit and the 4MHz oscillator, is to stop the oscillator when the reset line voltage drops. This is to conserve the charge on C4612. The discharge time of C4612 is the memory retention time which is specified as a minimum of 10 seconds. Typically, the memory retention time is a few minutes.

Keyboard Interface

The keyboard sense lines KS0 through KS3 should be high when no keys are pressed. Approximately once every millisecond, the micro reads the KS inputs. If one of the keyboard switches is pressed (closed), the circuit is completed and the corresponding KS line will go low. This tells the micro which of the 4 rows, of the 4 X 2 keyboard matrix, the pressed key is in. The micro will then scan the two KD lines, pulsing one low at a time, to determine which of the two columns the pressed key is in.

On-Screen Display

The OSD function is generated within the micro. This system offers multicolored OSD with its R, G, B outputs. Blanking is performed by the active low signal output at pin 21. The OSD horizontal position is phase-locked with the H-SYNC signal input at pin 23. The OSD vertical position is determined by the V-SYNC input signal at pin 24. The components external to the micro at pins 25 and 26 set up the characteristics of the OSD PLL. The voltages at pins 25 and 26 should be around 2V DC.

Tuning System

The tuning system used in this chassis is similar to the FS4 tuning system used in previous chassis. However, the phase-lock-loop (PLL) portion of the system is now an integral part of the tuner SIP. Tuner band switching and tuning frequency commands are sent to the tuner SIP via the micro's clock and data lines and the tuner responds accordingly. The AFT signal is input to the micro's internal A/D convertor (the AFT signal has a negative slope). Tuning sync is also input to the micro and periodically sampled using a special sync presence detection algorithm. The output of the sync separator is coupled with the KD3 line input at pin 12 of the micro in a time-sharing fashion.

The first step in the tuning of Air Channels begins at nominal +156kHz. If an AFT voltage of less than 2V is measured, nominal -156kHz is synthesized. If the AFT voltage is now greater than 3V, an AFT crossover has been detected and the nominal frequency is synthesized.

During the second step, if the less than 2V and greater than 3V criteria is not met, the system will synthesize nominal +3.0MHz. At this time the system will begin decrementing in 0.5MHz steps until an AFT crossover is detected. Once detected, the system checks for valid sync. After seeing valid sync, the AFT signal is successively sampled to fine tune the channel. If an AFT crossover is never detected, the system will default to synthesizing the nominal frequency.

Tuning in the cable mode is similar to air channel tuning with the following exceptions. As in air channel tuning, the first step is to synthesize nominal +156kHz. If the AFT voltage is less than 2V, the nominal -156kHz is synthesized. If the AFT voltage is now greater than 3V, a sync check is done. If sync is present, the nominal frequency is synthesized.

If an AFT crossover was not detected or sync was not valid, the system will proceed to step two in the tuning process. At this time the system will synthesize HRC +156kHz, looking for the HRC frequency of -1.25MHz. Again, the AFT voltage is checked. If it is less 3V, HRC -156kHz is synthesized. If the AFT voltage is now greater 3V, a crossover is detected and the sync is checked. If sync is valid, the nominal HRC frequency is synthesized. If an AFT crossover was not detected during step two, or sync was not valid, then the system will proceed to step 3 and synthesize +3.0MHz. The system will begin decrementing in -.5MHz steps until an AFT crossover is detected. Once found, fine tuning is performed similar to air tuning.

AFT is checked, at each of the 0.5MHz steps, whether sync is detected or not. If an AFT crossover was detected but no sync, that step will be remembered. Then, at the end of search, the step where the AFT crossover was detected will be synthesized. This gives the system the capability to tune both offset music channels and offset scrambled channels which normally do not have valid video with the carrier. This algorithm allows a +2.3 to -1.9MHz offset signal without valid video to be tuned.

Autoprogramming

Autoprogramming is a feature which automatically programs the scan list by progressively searching for channels at the antenna input. Autoprogramming starts by determining whether the TV is connected to a cable system or an "off-air" antenna. This eliminates the need for a manual cable/air switch.

Note: Because the system is looking for valid sync, weak off-air signals may not be programmed. These channels can, however, be manually programmed by selecting the Channel Memory feature in the Setup menu.

CIRCUIT OVERVIEW (Continued)

Video Controls

The micro has dedicated D/A convertors used to control the video parameter adjustments (brightness, contrast, color, tint and sharpness). The D/A method is pulse-width-modulated (PWM) with a repeating period of 512 uSec. The duty cycle can vary between 0% and 98.4% in 63 steps. Some versions of this chassis may incorporate analog stereo and mono systems, in that event the volume will also be controlled by a dedicated D/A convertor.

Non-Volatile Memory (EEPROM)

The EEPROM (U3200) will be incorporated in all instrument models (chassis versions) requiring the channel labeling feature. These instruments will have nonvolatile scan lists but may or may not have RF Switching. The absence of the EEPROM will signify to the control micro that autoprogramming shall be performed after each cold start.

IF Signal Processing

The IF signal from the tuner is amplified by Q2301, processed by the Saw filter (SF2301), then applied to pins 9 and 10 of the CTV IC (U1001). Signal processing internal to U1001 generates baseband video, AFT and AGC signals at pins 45, 50 and 2 respectively. The AFT signal is sent to the control micro where it is used to control fine tuning of the incoming RF signal. Similarly, the AGC signal is returned to the tuner to control the gain of the incoming RF signal.

Wideband Audio Processing

The detected video output signal at pin 45 of the CTV IC (U1001) is amplified by Q2302 and passed through a 4.5MHz bandpass filter (CF1201) and reapplied to U1001 at pin 51. Internal to the CTV IC, the signal is limited, detected and output at pin 52. It is then buffered by Q1201 and applied to level control R1204. The signal is then capacitively coupled (C1203) to either the digital stereo processing circuit or the analog audio processing circuit.

Luminance Processing

The composite video signal, output at pin 45 of the CTV IC (U1001), is passed through two emitter followers (Q2302 and Q2701) and a 4.5MHz trap. It is then sent to the video input switching circuit. From the switching circuit it is applied to pin 1 of the comb filter IC, U2601. The signal is buffered and output at pin 2, of the IC and applied to the glass delay line, DL2601. It is then applied to the notch depth control (R2630) and capacitively coupled back into the comb filter IC at pin 5.

The signal is then combed and separate luminance and chroma signals output at pins 7 and 8 respectively. The luminance signal is then applied to pins 43 and 40 of the CTV IC. The reason for two video inputs to the CTV IC is that, typically, video processed by the instrument is approximately 1.6V to 1.9V p-p while external input video is nominally less than 1V p-p. The processing circuits internal to the CTV IC compensate for this, assuring that the luminance signal output at pin 38 of the CTV IC remains at a normal 3.0V p-p level.

The luminance signal output at pin 38 of the CTV IC (U1001) is then applied to the luminance delay line. It is then passed through the contrast preset control, R2730, and the equalizer stage, Q2702. The low frequency luminance is then input to the CTV IC at pin 35 and the high frequency luminance is input at pin 34. The sharpness control is also applied to pin 34 analog with the high frequency luminance. Internal to the CTV IC the luminance signal is processed and output at pin 16 as a nominal 2.4V black-to-white-Y signal.

Chroma Processing

The chroma signal output from the comb filter IC (U2601) is applied to pin 31 of the CTV IC (U1001). The contrast control voltage is applied to the chroma signal as it emerges from the comb filter. This controls the color intensity as the contrast is raised and lowered, thus providing the ColorTrak feature. Internal to the CTV IC, the chroma signal is amplified and passed through a bandpass filter. There are two bandpass filters, one for the TV generated chroma signal and one for the external chroma input from a S-VHS signal. The output of the two bandpass filters are applied to a switch which is controlled by the DC voltage level on pin 31. During the TV mode there will be approximately 100mV of burst and 4V of DC present at pin 31. During the external mode there will be approximately 200mV of burst and 1V to 2V of DC present at pin 31.

After passing through the switch, the chroma is applied to another stage of amplification where it is burst keyed. At this point, a feedback signal is used for ACC.

The chroma signal is then applied to the second chroma amplifier and the color killer. If no burst is present, the killer will be activated pulling the color control line low, turning color off. If burst is present the signal is phase detected and shifted to generate the R-Y and B-Y signals. These two signals are applied to a demodulator stage where the G-Y signal is generated and the R-Y, B-Y and G-Y signals are output from the CTV IC at pins 15, 18 and 17 respectively. The frequency of the VCO is determined by the external 3.58MHz crystal at pin13 of the CTV IC and controlled by oscillator adjust control R2802 at pin 11.

Kine Driver

Each of the three kine drivers consists of a cascode pair. The upper device of the cascode pair, or driver transistor, is a high-voltage device connected in a common base configuration. The lower device of the cascode pair, or pre-driver transistor, is a small signal transistor connected in a common emitter configuration. Each of the color difference inputs to the kine driver is connected to the base of one of the lower devices of the cascode pair. The luminance signal is added to the emitter of each of the lower devices by means of an emitter follower buffer.

The kine driver circuit is an interface between the video processing circuits and the picture tube. The purpose of the circuit is to receive a video signal from the CTV IC (U1001), amplify it, and present it to its respective cathode of the picture tube, as a color signal. The video signal received by the kine driver is in the form of a color difference signal (example; R-Y) and the luminance signal (-Y). The color

CIRCUIT OVERVIEW (Continued)

Kine Driver (Continued)

difference is presented to the lower device of the cascode pair and is a non inverted signal. The luminance signal is presented to the base of the luma buffer and is an inverted signal. The kine driver inverts the color difference signal and sums it with the luminance signal. The sum is amplified by the kine driver and the resultant signal is presented to its respective cathode of the picture tube.

Digital Stereo Audio

The digital stereo audio processor (U1600) operates as a slave to the system micro. It will respond only to commands from the system control micro (U3101). These commands are passed to the processor through the enable, data and clock lines connecting the two IC's. Wideband audio is developed by the CTV IC (U1001) and applied to the digital stereo processor, through voltage a divider R1605, R1606 and capacitor C1609, to pin 13 of the processor (U1600).

The signal level, input at pin 13, should be approximately 400mV at full deviation. Internal to the IC, the signal is applied to an A/D converter. The signal is then digitally processed by the IC and applied to separate D/A converters. One D/A converter provides Hi-Fi output at pins 20 and 21. The other converter provides low-level selected line output at pins 23 and 24.

Power for U1600 is provided by the +5V run source. It is applied to pin 19 of the IC for the analog processing circuits and to pin 7 for the digital processing circuits. An external crystal, Y1601, is used to set the operating frequency of the digital processing circuits. VCXO filtering is accomplished by external components R1609, R1623 and C1613 at pin 16. Analog bias (2.5V) is generated internal to the IC and output at pin 14. It is used to bias the wideband audio input circuit as well as the auxiliary audio input circuits.

Power Amplifier 1W/5W

The Hi-Fi output (pins 20 and 21) of the digital stereo processor is capacitively coupled to the power output IC (U1900) at pins 5 and 1. The left and right audio is amplified and output at pins 8 and 10 respectively and capacitively coupled to the speakers. U1900 is powered by the +26V supply, derived in the secondary of the IHVT.

S-PIP (Defeatured Pix-in-Pix)

The S-PIP (defeatured) module allows for small pix insertion into the large pix with the capability of progressive movement to each of the four corners. It also provides for freezing action of the small pix. These are the only features provided by the defeatured pix-in-pix module.

The PIP IC has two built in switches. One determines the source of the big pix and the other determines the source of the small pix. The big pix signal is routed out of the processor IC and applied to the comb filter circuit for processing. The small pix information is routed into the PIP processing portion of the IC and output as separate luminance and chroma signals. These signals are then passed through separate op-amp stages and applied to the fast switch. The big pix luminance and chroma information, from the comb filter, is routed back into the module and also applied to the fast switch. The small pix information is combined with the big pix information and output from the module for processing by the TV luma/chroma processing circuits. It is also applied to a summing stage, on the module, and output from the module as pix-in-pix selected video.

SVM (Scan Velocity Modulation)

Scan Velocity Modulation is used in some 27 inch and all 31 and 35 inch versions of this chassis series. Its function is to concentrate the beam current into a smaller area so as to hit only two phospher dots at a time rather than approximately six. The system is most effective in the video frequency range around 2MHz.

SVM coils are placed on the neck of the picture tube. The SVM circuit then develops a magnetic field perpendicular to the beam, thus causing the beam to be concentrated into a smaller area during the deflection process.

A portion of the luminance signal is provided to the SVM circuit by Q2708. The signal is passed through a delay matching network and applied to the emitter of a common base amplifier (Q6200). It is then passed through a emitter follower (Q6201) and capacitively coupled to a differential amplifier (Q6202 and Q6203). Q6204 is the current source for the differential amp stage. The differential amplifier provides paring (clipping) of the SVM correction signal above 50 IRE. This is to stabilize the amount of correction on high transitions. The signal is then passed through differential buffer Q6205 and applied to a push-pull driver stage (Q6206 and Q6207). Coring (noise suppression) takes place at this point. The signal is then capacitively coupled to the output stage (Q6208 and Q6209). The output stage drives the SVM coil.

Over-current limiting is provided by Q6210 which senses the current through the output stage. OSD (on screen display) blanking interface is provided by Q6211 and Q6212. This curcuit causes a quick shut-off of the SVM circuit and capacitor C6227 provides a slow recovery of SVM circuit operation. This is done to prevent crosstalk and tearing in the picture information during the OSD function.