Table of Contents

ITC222
CIRCUIT OVERVIEW

The ITC222 (International Television Chassis) is designed to address many of the service and performance concerns found in the first Generation ATC (Americas Television Chassis) instruments. It uses integration to reduce the number of circuit boards and cables used in the chassis to improve the serviceability. Picture performance has also been improved and is optimized for HDTV signals. The results are a projection television that generates an HDTV quality picture in a service friendly package.

Integration is the main reason for the reduction of circuit boards in the ITC222 chassis. The ITC222 uses eight circuit boards while the first generation ATC221 chassis used eleven. Most of the integration is done on the Small Signal Board (SSB). The ATC221 also used a SSB, but separate boards to process component video, convergence signals, and the subwoofer driver circuits. The SSB board of the ITC222 includes all of these circuits. Even with the additional circuits on it, the ITC222's SSB has 15 fewer IC's and 450 fewer components than the SSB board of the ATC221 chassis.

Fewer circuit boards are just one reason there are less cables in the ITC222 chassis. Positioning the connectors at the edge of board and serially connecting boards were two of the other techniques used to reduce cable count. Placing connectors at the edge of circuit boards allows designers to use the circuit board traces to reduce cable count. Instead of separate connectors for system control and voltage sources, a single connector can be used to pass both to the next circuit board. Placing the connectors at the edge of the board simplifies the routing of the copper traces to get the sources and signals to the connectors. Serially connecting circuit boards passes signals used by a group of boards through one board to the next board. Instead of individual cables passing from each circuit board back to the source, a single cable moves the signal to the first board, then another cable passes the signals from the first board to the second board. This continues until all the boards are connected. These techniques reduced the cable count of the ITC222 to thirty while the ATC221 required fifty cables.

Picture performance improvements are a result of using new IC's to improve circuit integration. The IC's that allowed multiple circuits to be moved to the SSB, have the benefit of better signal characteristics over the IC's used in the ATC221 chassis. The performance improvements in the new IC's include wider video bandwidth (30 MHz), better 1H to 2H up conversion, and improved color resolution (ITC222 uses 4:2:2 while ATC221 uses 4:1:1). The results of these enhancements are a sharp, stable, picture with less artifacts than the previous ATC221 chassis.

Fewer cables and circuit boards combine to improve the serviceability of this chassis. Enhanced picture performance helps it to display a sharp, stable picture with both NTCS and ATCS signals. This is a projection television that generates an HDTV quality picture in a service friendly package.

Abbrevations & Acronyms

480_on	Switching signal for 480P & up-converted 480i mode
ABL	Average Beam Current Limiting
ACQ	Acquisition power mode
ADB	Adaptor Board, PTV
APR_ON	uP signal to switch between 6V & USYS regulation
AQR_ON	Signal from uP to switch from 6V regulation to USYS regulation
BCL	Beam Current Limiter
Breathing	
BSVM	Beam Scan Velocity Modulation
CAB	Convergence Amplifier Board
CBA	Circuit Board Assembly
CCC	Continuous Cathode Calibration
CSB	Convergence Signal Board
CTI	Color Transient Improvement
CVBS	Composite Video Baseband Signal
DCR (R,G,B)	Dark Current Signal (cathode cutoff)
DCU	Digital Convergence Unit
DEGAUSS	Signal from uP to turn degaussing circuit on & off
DFB	Dynamic Focus Board
DP	Deflection Part
DRI	Digital Ready Interface
DST	Diode Split Transformer (IHVT)
DVI	Digital Visual Interface
ECO_ Standby	Signal from uP to switch stdby power supply modes
EFC	Earth Field Correction
EW	East West
H_DRIVE	Horizontal Drive Signal
HIP	Hi-Level Input Processor
HOP	Hi-Level Output Processor
IHVT	Integrated High Voltage Transformer
INF_POW_FAIL	signal from standby SMPS indicating loss of mains (120VAC)
LTI	Luminance Transient Improvement
MID	Mains Input Doubler (doubles Raw B+)
NVM	Non Volatile Memory or EEPROM
PA/SW	Power Amp Sub Woofer
PE	Protective Earth
PO	Power On signal from uP to start main SMPS
PP	Power Supply Part
PS_ON	signal derived from PO to start main SMPS, also controlled by safety circuits of the main SMPS
PS-ADB	PTV Power Supply/Adaptor Board (same as ADB)
PSB	Power and Scan Board
PSI	Picture Signal Improvement
PWM	Pulse Width Modulation
RP	Rear Projection

ITC222
CIRCUIT OVERVIEW

Abbrevations & Acronyms

SAFETY	signal generated by safety circuit located on SPP CBA
SMPS	Switched Mode Power Supply
SMT	Switched Mode Transformer
SPP	Signal Power Part
SSB	Small Signal Board
SSC	Super Sandcastle Signal
TFT	True Flat Tube
UP	Micro-Processor
USYS	System voltage for the horz deflection or Reg B+
XRP	X-Ray Protect

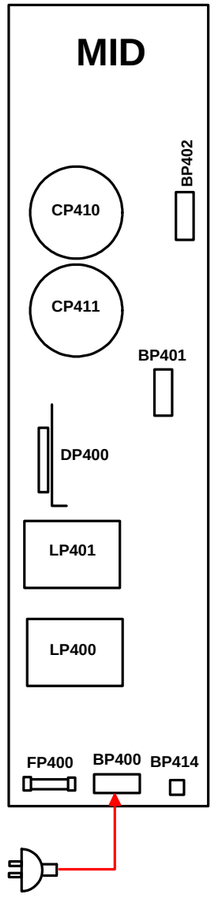
ITC222 MID Overview

The Mains Input Doubler (MID) circuit board assembly (CBA) used in the ITC222 performs the function of producing +300Vdc (raw B+) for Stand-by, Run, and Convergence power supplies. The MID accomplishes this by rectifying the 120VAC to 150Vdc and then doubling the dc to +300V.

The AC voltage is applied to the MID via connector BP400 through FP400 (fuse). This AC voltage is "smoothed" by LP400 / 401 and is used for degaussing on the direct view sets via connector BP401.

The "smoothed" AC voltage is also fed to bridge rectifier DP400. The rectified AC voltage from DP400 is filtered by CP410. CP411 along with other components are used to double the DC voltage to approximately +300Vdc.

Connector BP402 is used to connect the 300Vdc to the main switch mode power supply CBA to be used as raw B+ for Stand-by, Run, and Convergence power supplies. This voltage is critical to set operation so connector BP402 should have +300Vdc present when ever AC power is applied to the set. With out this voltage the stand-by switch mode power supply cannot function and thus system control will not function.



Mains Input Doubler CBA

ITC222 PSD Overview

The PSD or Power supply Deflection CBA is home to two main circuits, Power Supply (Run and Stand-by) and Deflection. Its purpose in life is to supply the required voltages for all circuits in the ITC222. It also provides the horizontal and vertical deflection for the CRT(s).

The stand-by power supply starts when the +300Vdc is present from the MID at connector BP010. IP020 provides the switching necessary to drive LP020 producing the secondary stand-by voltages +7V, +5V, and +3.3V. These voltages are sent to the small signal board (SSB) via connector BP005.

With the stand-by voltages preset at the SSB, System control comes on line and awaits user input. Once the user pushes the power switch, System control sends a power on command to the run supply start circuit.

Start up of the run supply occurs when the Power on command from system control on the SSB is present at BP005. This signal is low to turn on the run supply and high to turn it off. The voltages developed by the run supply are:

- v ±UA (Audio output supply voltages)
- v +USYS (Reg B+)
- v +33 Tuner
- v +20
- v +10
- v +6V

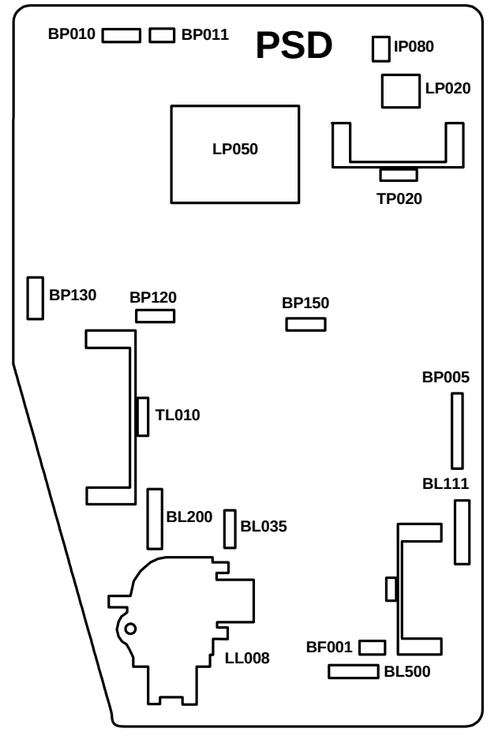
The SSB and other sections of the PSD CBA use these voltages.

NOTE: +USYS and ±UA voltages are determined by model.

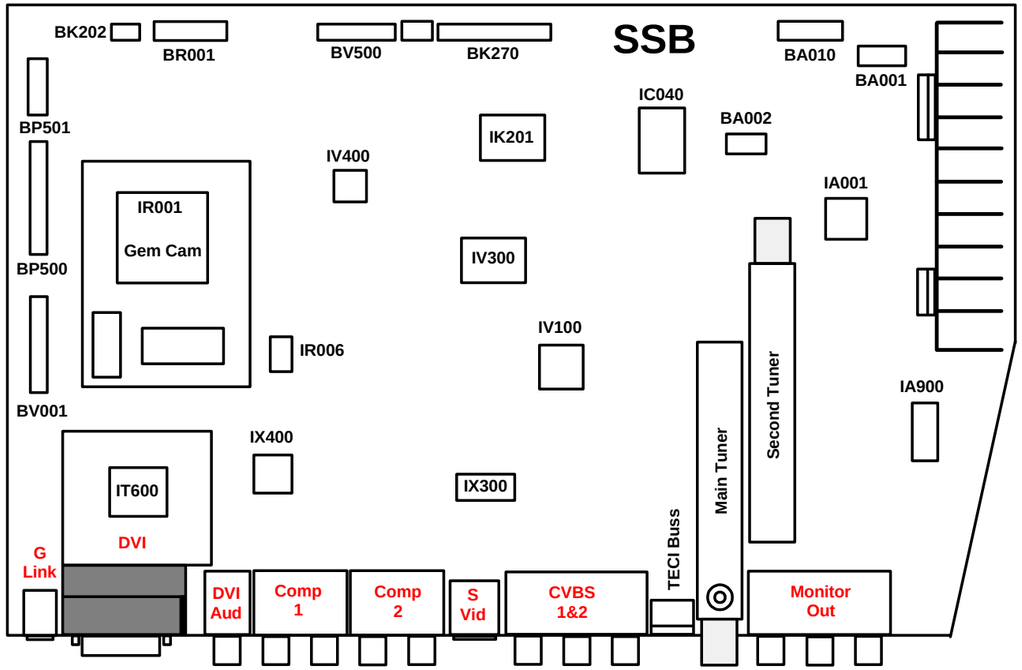
TP020 provides the switching current necessary to drive LP050 producing the run voltages. Once the run voltages reach regulation, system control sends the clock and data command to the deflection processor to start horizontal and vertical.

The deflection processor, on the SSB, generates the horizontal and vertical drive signals that are sent to the horizontal and vertical circuits on the PSD CBA via connector BP005. The vertical signals (+, -) drive the vertical output IF001. The horizontal drive signal drives LL001 and TL010 horizontal out transistor (HOT). TL010 in turn drives LL008 IHVT producing the scan-derived voltages.

The scan-derived voltages from IHVT LL008 are used for CRT drive, Vertical, and XRP protection.



Power Supply Deflection CBA



Small Signal Board CBA

ITC222 SSB Overview

The Small Signal Board (SSB) is the heart of the ITC222. All processing and control functions are performed by the SSB. These processing and control circuits are:

- Audio and Video processing
- Audio and Video switching
- Deflection processing
- System Control (Gem Cam)
- Convergence processing and control
- NTSC Tuner(s)
- Audio Output

These circuits all have one circuit in common, the Gem Cam. This section will focus on the Gem Cam section of the SSB and it's function for start-up, turn-off and shutdown of the set.

The Gem Cam or system control (IR001) communicates to the other circuits via I²C clock and data. IR001 has four (4) buses for communication. This allows the IR001 to communicate with other ICs in the various circuits.

IR001 operates on +5V, +3.3V, and +1.8V derived from the PSD CBA (Stand-by Voltage) via connector BP500.

Once the stand-by voltages are up and stable, IR001 awaits user input.

When the power button is pushed, the signal is sent to the SSB from the front panel assembly via connector BR001. IR001 processes the signal and performs the power on function. The sequence starts with a power on command being sent to the SSB turning on the run supply. After the run supply is operational, IR001 communicates with the deflection processor telling it to produce horizontal and vertical drive.

With horizontal and vertical up and operational, IR001 now communicates with the other IC's on the SSB bringing all systems on line. On the PTV, convergence is brought up after horizontal but before the other systems.

Turn off is the reversal with Audio and Video being muted until the other systems are off.

Because the SSB is the heart of the ITC222, special consideration needs to be used when troubleshooting it. With all processing taking place on the SSB one needs to consider the type of problem and the likely hood of the problem being associated with the SSB before replacing it.

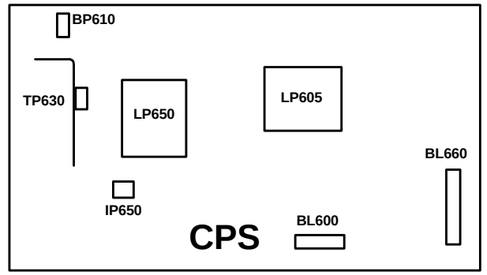
ITC222 Conv PS Overview

The Convergence Power Supply CBA is home to a switch mode power supply. This supply produces the ±53 and ±15 volts that are used by the Convergence Amplifier CBA. These voltages are present after the set is operational.

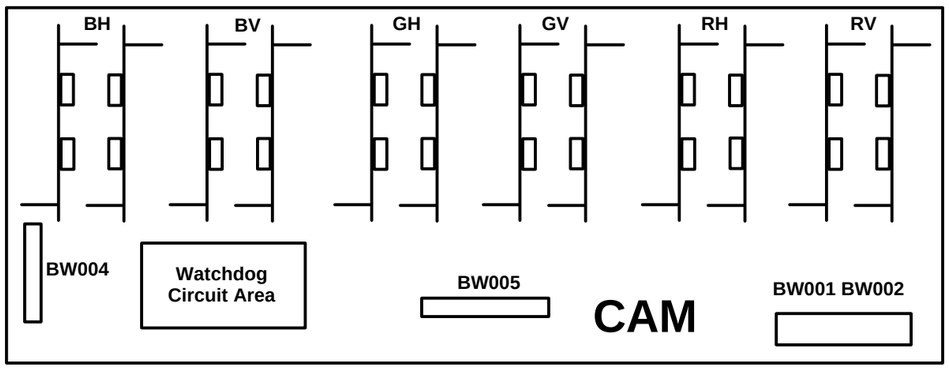
Turn on of the Convergence Power Supply (CPS) comes through the Convergence Amplifier (CA) CBA (Watchdog circuit) via connectors BW005 (CA) and BP660 (CPS). A high from the SSB tells the Watchdog circuit to supply +10V to the Convergence Power Supply. The +10V from BP660 allows TP620 to switch, driving transformer LP650. The voltages developed by LP650 are ±53 and ±15. These voltages are sent to the convergence amplifier CBA via connector BP660 and are monitored by the Watchdog circuit.

NOTE: The watchdog circuit on the convergence amplifier CBA turns on and off the convergence power supply. Any problem with the output voltage will result in the convergence power supply being turned off.

The Convergence Power Supply is a simple switch mode power supply that is turned on by the Convergence Amplifier CBA Watchdog circuit. It produces the voltages required by the Convergence Amplifier CBA.



Convergence Power Supply CBA



Convergence Amplifier CBA

ITC222 Conv Amplifier Overview

The Convergence Amplifier CBA is home to the convergence amplifiers and Watchdog shutdown circuit. The convergence amplifiers are used to drive the convergence yokes. The Watchdog circuit monitors the input voltage for any changes to protect the convergence amplifiers. There are two groups of transistor amplifiers for each color red, green and blue. These groups are Horizontal and Vertical.

Signals from the SSB, via BW005, are amplified by output transistors and supplied to the convergence yokes by connectors BW001 and BW002. These amplifiers can be viewed as audio amplifiers driving a speaker (yoke).

Power for the output transistors comes from the Convergence Power Supply CBA via connector BW004. The voltages required by the convergence amplifiers are ±53V and ±15V. A Watchdog circuit, to shutdown the convergence power supply, monitors these voltages. If excessive current is drawn in the amplifier, the Watchdog circuit shuts down the power supply. The Watchdog circuit also turns on the convergence power supply via signal from the SSB through connector BW005.

All in all the Convergence Amplifier CBA provides the amplification of convergence signals to drive the convergence yokes, turns on the convergence power supply and monitors the voltages for excessive current draw.

ITC222
CIRCUIT OVERVIEW

ITC222 Startup Sequence Overview

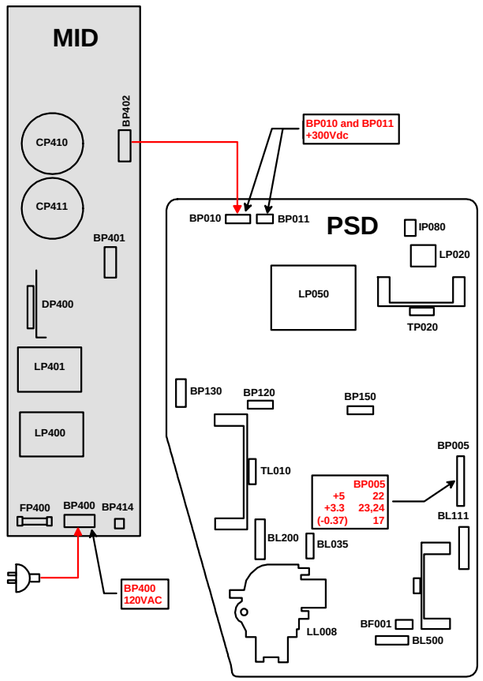
The ITC222 startup sequence is not all that different from any other chassis produced by Thomson it just takes 10-15 seconds before picture is displayed. It starts with the standby supply coming up when AC power is applied. Standby Power Supplies supply the voltage for System Control. Once the standby supplies are up, System Control is active and awaits user input. After the user pushes the power switch, System Control brings up the run supplies and deflection. After the run and deflection supplies are up, video and audio processing starts. The CRT(s) is the last to come up producing the picture along with audio. What is different about the ITC222 is its modular design. This section will focus on each modules place in the start up sequence and the requirements of each to be part of the over all system.

To start with the Mains Input Doubler (MID) CBA gets AC power supplied through connector BP400. As you may recall the MID rectifies the AC to DC and doubles the +150Vdc to about +300Vdc. This +300Vdc is sent to the Power Supply Deflection (PSD) CBA for standby power supply operation and to Convergence Power Supply CBA in the PTV.

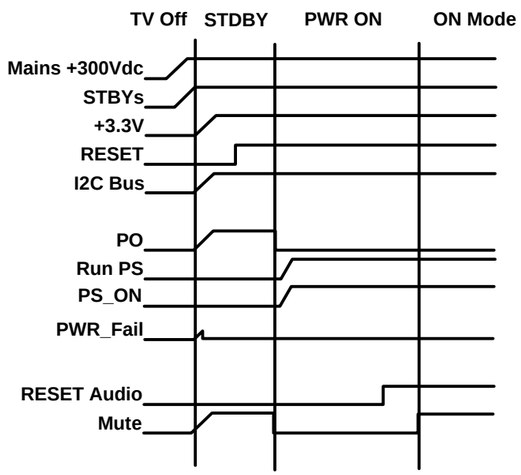
The Power Supply Deflection CBA receives the +300Vdc at connector BP010. This voltage is used by IP020 and LP020 to produce the standby voltages +7Vdc, +5Vdc, (–0.37Vdc), and +3.3Vdc. System Control uses these voltages for operation, reset, power fail detection and memory. Connector BP005 needs to have voltage on pins 17 (-.37Vdc), 22 (5V), 23 and 24 (3.3V) to be considered operational in the standby mode.

The (–0.37Vdc), found on pin 17 is used by system control for INF_POW_FAIL (power fail) shutdown. This signal is buffered on the SSB before being sent to System Control. After System Control resets, it checks the INF_POW_FAIL (power fail) signal. If all is ok System Control awaits user input. If pin 17 is 0Vdc, System Control will “batten down the hatches” and shutdown. This will appear as a dead set because System Control will not finish the startup sequence.

Once the power switch is pushed, things start to happen all at once. System Control processes the power on command and starts the run supply. The startup of the run supply comes from a PO signal that System Control sends to the PSD CBA via connector BP500 pin 18. Once the run supplies are up and regulated, System control communicates with the deflection processor. The deflection processor sends horizontal and vertical drive signals to the PSD via connector BV001.



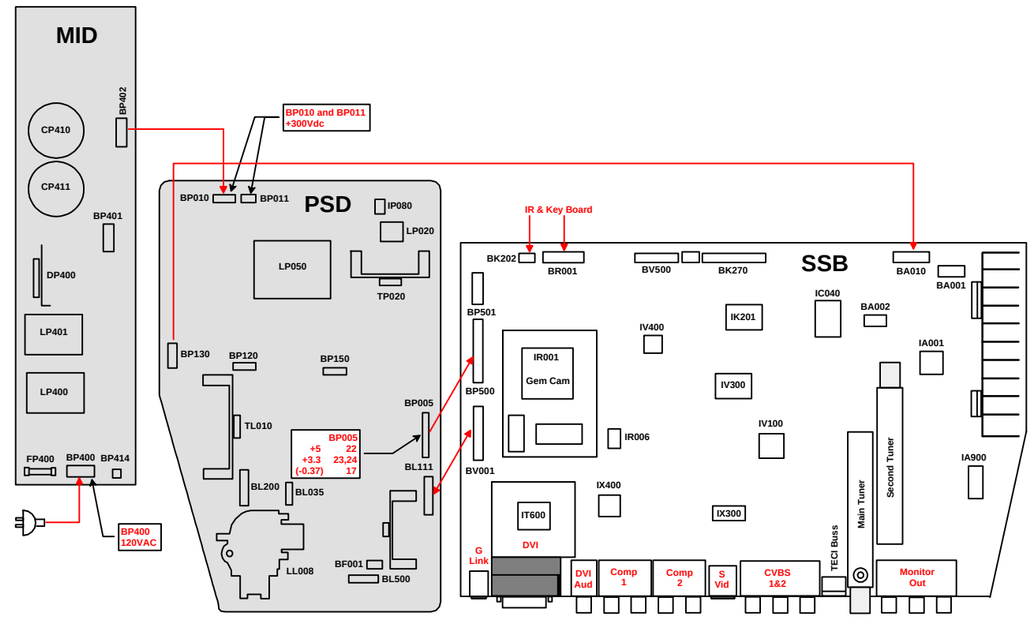
MID and PSD Startup



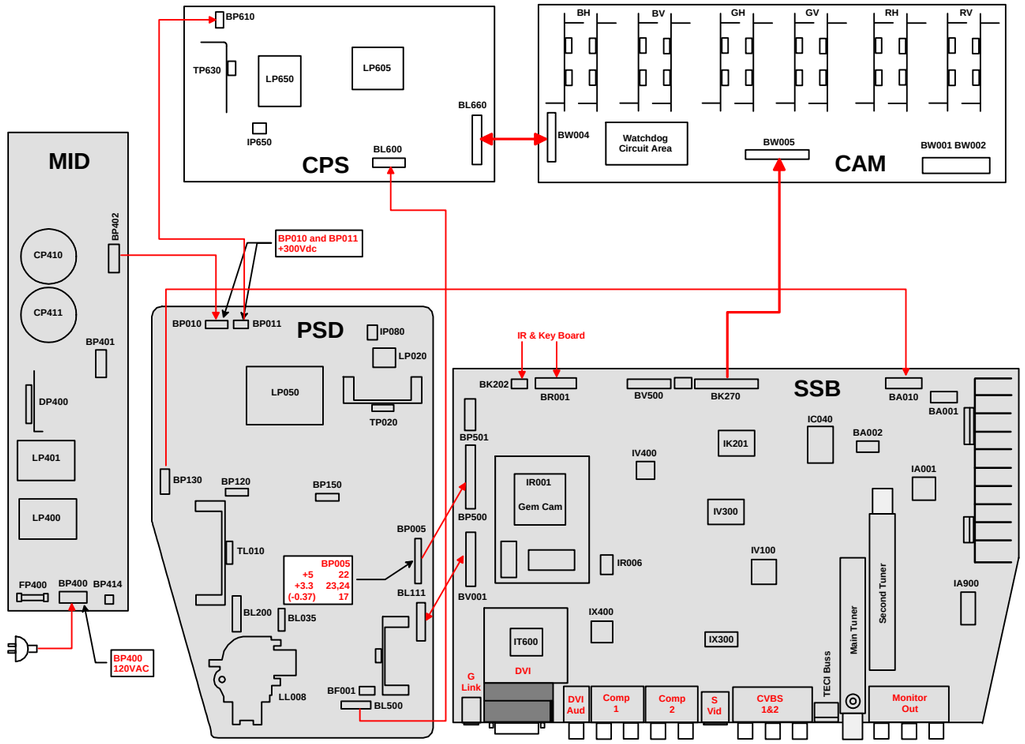
Power On Sequence

System control monitors deflection for proper operation via feedback signals on pins 10 and 15 of BV001. If there is a problem with deflection, System Control will stop the process and shutdown. If all systems are ok, System Control will start convergence (PTV) and audio / video processing via I2C bus communication.

Also monitored is the +20V. This voltage is used to make sure the PSD, SSB, and CRT circuit boards are connected. It is looped through connectors on PSD, SSB, and CRT(s) circuit boards. If this loop is opened (connector disconnected), System Control will shut down the set.



MID, PSD, and SSB Startup



MID, PSD, SSB, and Convergence Startup

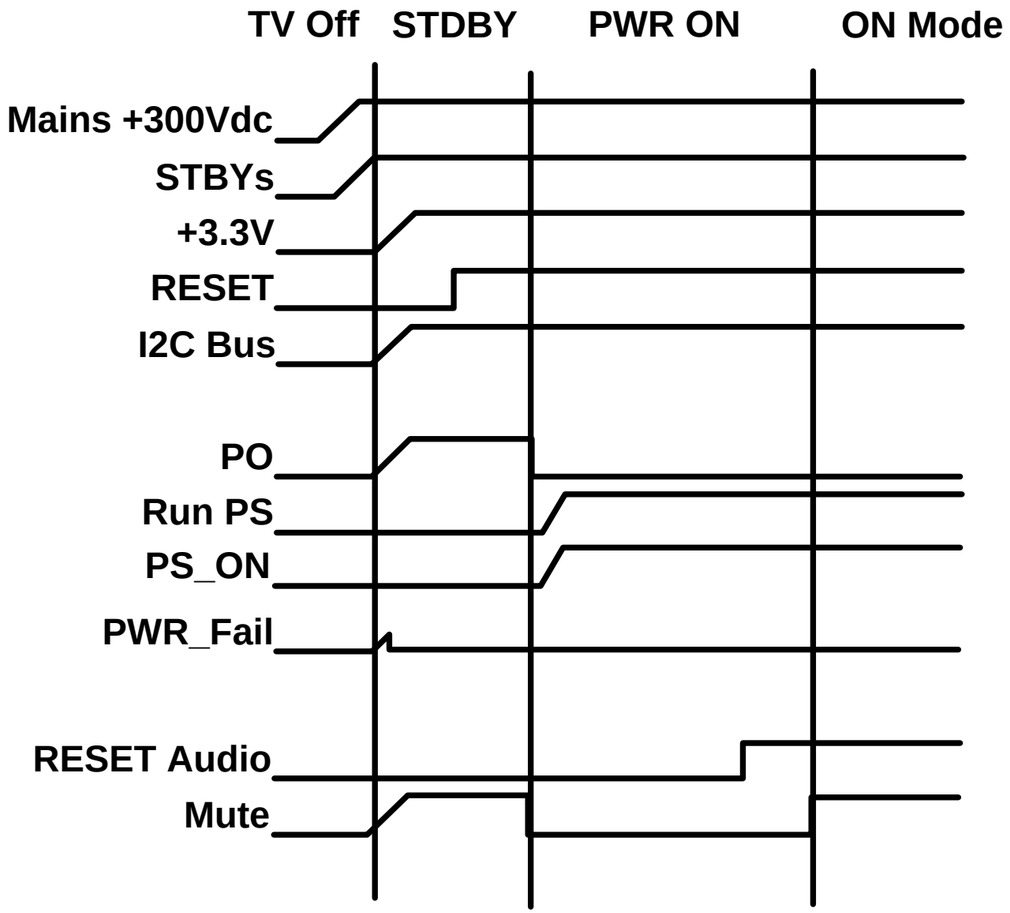
Turn on of the Convergence Processor is by I2C bus commands from System Control. The Convergence Processor starts the Convergence Power Supply with a PS_ON command. This signal is routed to the Convergence Power Supply via the Convergence Amplifier through connectors BK270, BW005, BW004 and BL660. The PS_ON signal is +9.6Vdc found on pin 4 of connector BP660.

Once the Convergence Power Supply comes up, a Watchdog circuit on the Convergence Amplifier CBA monitors the voltages for proper operation. Any problem detected will shutdown the convergence power supply.

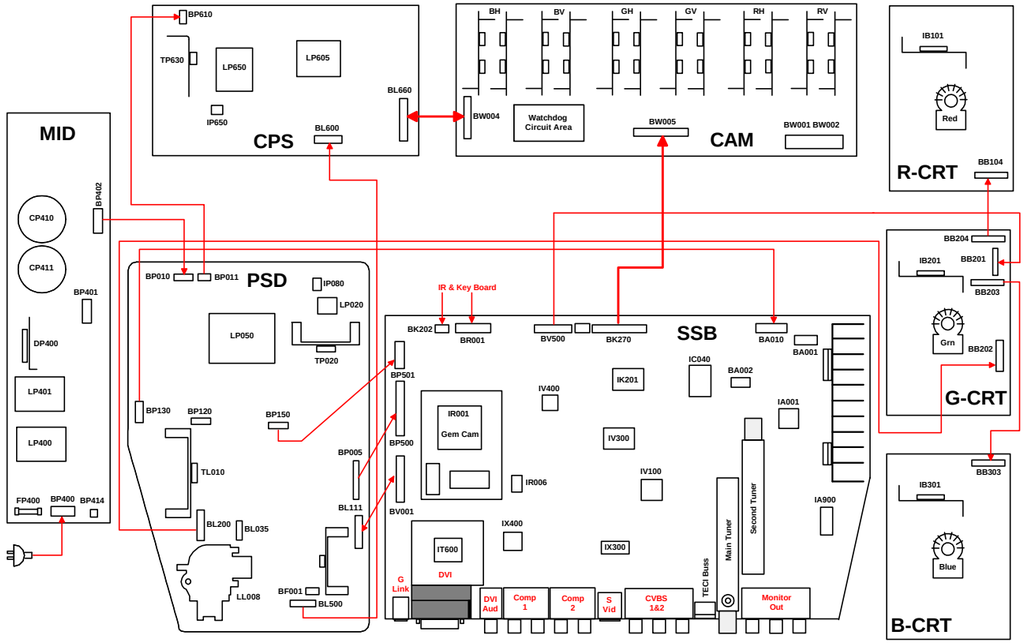
The Watchdog shutdown circuit controls the Convergence Power supply only. There are no signals sent back to the SSB to shutdown the set. In other words the ITC222 will operate with out the convergence power supply or convergence amplifier being connected.

All the checks for proper operation in each section cause a significant delay in startup of the ITC222. Only after all systems are brought on line and checked will System Control communicate to Video and Audio processing to produce sound and picture. Typically, the ITC222 from power on request to picture being displayed is about 10-15 sec.

ITC222
CIRCUIT OVERVIEW



Power On Sequence



ITC222 Chassis

ITC222 Shutdowns

The ITC222 uses several circuits to prevent damage to components by shutting down the set. These circuits are found in the power supply, deflection, system control, CRT, and convergence circuits. These shutdowns can be classified into two categories, Non-Fatal Shutdowns and Fatal Shutdowns.

The Non-Fatal Shutdowns are communication errors between System Control and the other ICs and may or may not completely shutdown the set. Non-Fatal Shutdowns will almost always throw an error code. This error code is stored by System Control and retrieved by the use of Chipper Check or accessing the service menu. Fatal Shutdowns on the other hand may not throw an error code but will always shutdown the set. Fatal Shutdowns are ones were component failure has occurred or were other damage may result if the set remains in operation. In this section we will look at the different shutdowns by classification as an informative basis.

Non-Fatal Shutdowns

Non-Fatal shutdowns are communication problems associated with the System Control. All the Non-Fatal shutdowns are found on the SSB and are associated with each processor, switch, and or tuner on the SSB using I2C communication. During Non-Fatal shutdown, an error code is sent to System Control and stored. Because of I2C communication, there are no test points to check for the Non-Fatal Shutdown. Chipper Check or the Service Menu, if the set is operational, are the only way to determine a Non-Fatal shutdown. This will be indicated by the error code displayed in Chipper Check or the Service Menu. Remember there are no Non-Fatal shutdowns out side of the SSB.

Fatal Shutdowns (Safety Protection)

Fatal shutdowns can be found on all major CBAs in the ITC222. Because of that, we will be looking at the shutdowns found on each CBA. Some of the Fatal shutdowns have ties back to the SSB (System Control) and some do not. Those that have ties back to System Control will store error codes. These error codes are retrieved using Chipper Check only.

MID Safety Protection

The MID only has one safety protection device, FP400. FP400 is the main fuse for the set. Its purpose in life is to prevent

over current fires. If FP400 is open, the CPS and PSD are prime suspects.

PSD Safety Protection

The PSD safety protection is divided into two sections, Power supply and Deflection. The Power supply protection is designed to shutdown the power supply for over current and over voltage. The Deflection shutdown is designed to disable horizontal drive and turn off the run supply. The Deflection shutdown will also communicate with System Control and store error codes.

The Power supply protection has several components on both the primary and secondary side of the switch mode transformer (SMT). These circuits protect the power supply from over current, over voltage, and under voltage. There is also Beam-Current control, Uvideo control, and Audio safety.

The Beam-Current control is used to shutdown the power supply during excessive beam current. This type of shutdown will not produce an error code. It is only active during run mode.

Uvideo control shuts down the run power supply if the CRTs (PTV only) draw excessive current. This signal monitors the cathode voltage for excessive current. The detection circuit is found on the Green CRT drive CBA with monitor circuits on the Red and Blue CRT CBAs. Disconnecting BV500 (SSB CBA) and BL200 (PSD CBA) will disable the Uvideo control.

Audio Safety circuit detects excessive current draw from the audio output and shuts down the run supply. Disconnecting BA010 (SSB CBA) removes power to the audio outputs and possible excessive current draw.

SSB Safety Protection

The safety protection circuits on the SSB deal with the horizontal processor (IV400). There are three inputs; BEAM_PROT, EHT_INFO, and EW_PROT that IV400 monitors at one input (pin 4 EHT In). This input is more commonly known as XRP detect. The three inputs are sent to a comparator circuit that is tied to IV400 pin 4. All three inputs send the same error code, XRP. These signals come from the PSD via BV001 connector.

CPS Safety Protection

The Convergence Power Supply (CPS) safety protection is contained on the Convergence Amplifier CBA. This circuit is called the Watchdog circuit. It provides protection from improper voltage and over current. It also starts the CPS. There are no error codes stored for this safety protection. The only symptom will be no convergence correction. If the convergence power supply is not coming up, disconnect BW001 and 002 on the CAM CBA. This will remove the load from the convergence amplifiers and may unload the CPS.

CRT Safety Protection

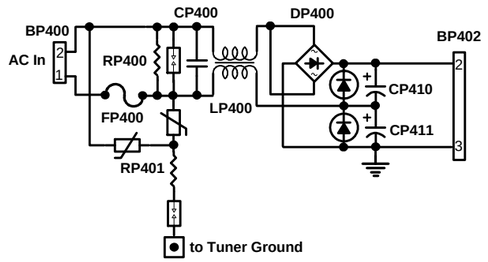
The CRT CBAs are protected by a loop through signal that when broken will cause the set to cycle three times. This prevents the cables (BB204, BB201, and BB203) from being disconnected.

As mentioned earlier in PSD Safety Protection, the Green CRT CBA has an Uvideo short circuit protection. This protection is monitored by each of the other CRT CBAs.

Another safety protection is “Spot Killer” circuit. This circuit protects the CRTs from being burnt during turn off of the set.

Mains Input Doubler

The Mains filter is located on the Mains Input Doubler board and consist of CP400 and LP400. The purpose of this circuit is to minimize interference transmission from the power supply to the Mains and visa versa. Resistor RP400 is necessary to ensure that CP400 is quickly discharged after the instrument has been disconnected from AC. To protect the Mains input, varistor RP401 will absorb any high peak voltages. The AC is rectified by DP400. The doubled rectified main voltage is the result of CP410 and CP411. Both capacitors are connected in series, with CP410 being charged by the positive cycle, CP411 the negative cycle.



MID Block Diagram

STANDBY POWER SUPPLY

Start Up

ECO Mode

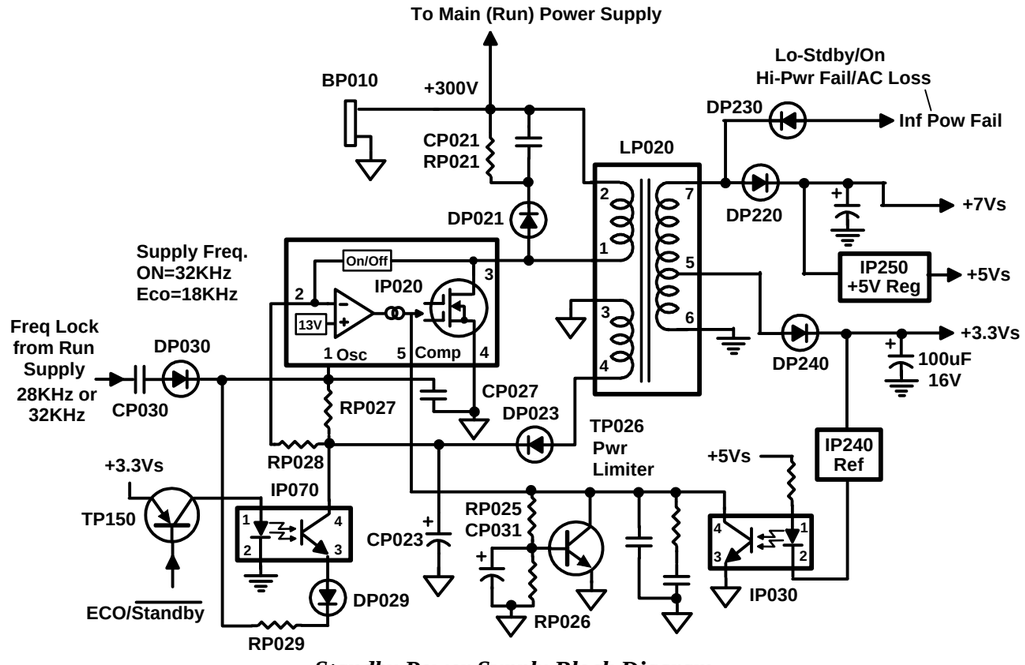
When AC is connected, the standby power supply starts in “ECO” mode. The chassis’s microprocessor determines if it stays in “ECO” or goes to “STANDBY” and advances to “RUN”. This depends on the previous state of the set at AC interruption or disconnection. The set will always come back to the last status before AC interruption.

When the AC is first connected, the integrated high voltage current source of IP020 provides a bias current from pin 3 during the start-up phase. As soon as the voltage on pin 2 reaches the threshold VDDON of IP020, the device turns into active mode and begins switching. The start up current generator is switched off, and the re-supply provides the needed current on the VDD pin 2 through the winding between pin 3 and 4 of LP020. The oscillator at pin 1 starts working after VDDON at pin 2 is reached. It takes approx. 0.6s for the standby power supply to switch on after AC has been connected.

The oscillating frequency at pin 1 of IP020 is determined by the values of RP027 and CP027. The typical value of the oscillator frequency is approximately 28kHz in standby (mode prior to run) and 17kHz in “ECO” mode. The first time that AC is connected, the ECO_STANDBY IR001 pin 110 is high and TP150 is switched off. No current can flow from the opto coupler IP070 and the resistor RP029 to pin 1 of IP020.

STANDBY Mode

To switch from “ECO” to “STANDBY” (mode prior to run), the ECO_STANDBY line will be switched low turning on TP150 via 5V_STBY, resistor RP153 and RP152. This results in switching on TP150 and now current can flow from CP023 via the opto-coupler IP070 and RP029 to pin 1 of IP020. This additional current results in a frequency shift and the standby SMPS is then running at approximately 28kHz.



Standby Power Supply Block Diagram

The standby SMPS is synchronized to the main SMPS by differentiation of the auxiliary voltage at pin 5 of the SMT LP050 via CP030 and RP030. Only during the positive peak voltage does current flow via the diode DP030 and the current limitation resistor RP032 to the oscillator input of IP020. To provide the desired transfer function of the regulation loop, a compensation network CP026, RP024 and CP024 is connected to the COMP pin 5 of IP020 which is the output of the error amplifier and acts as soft start. In addition, the transistor TP026 limits the output power. If the threshold of TP026 is reached, TP026 is switched on and the voltage on pin 5 of IP020 is below 0.5V causing shutdown of the power MOSFET of IP020. The capacitor CP031, in conjunction with resistors RP025 and RP026, define the time for TP026 to be active.

IP020 -One Complete Cycle in On Mode

Switch On Phase

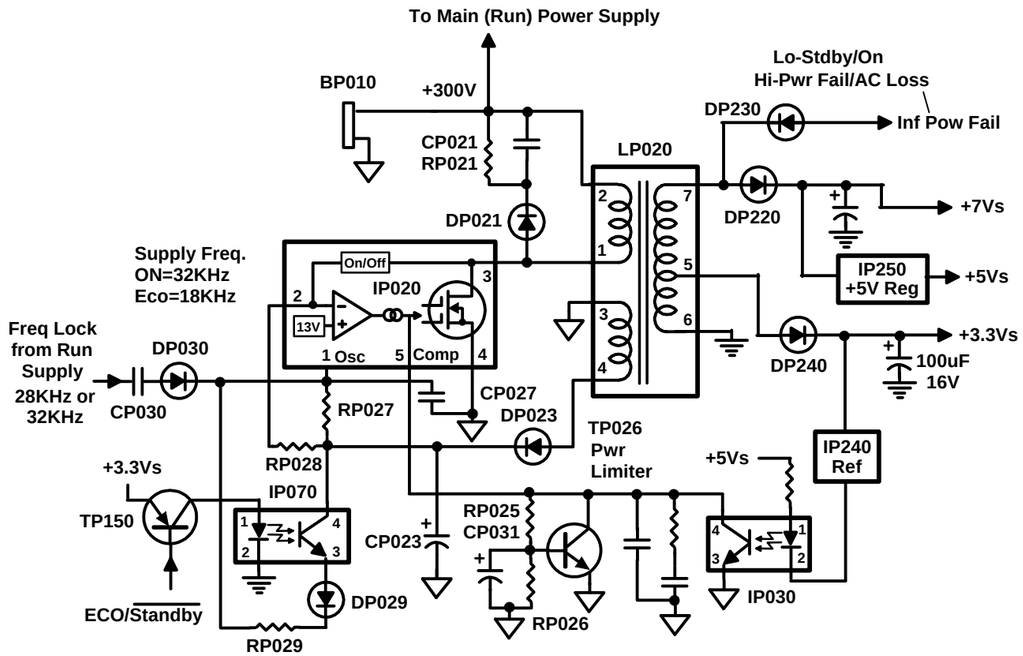
When the internal driving circuit switches the power transistor of IP020 on, the voltage across the transistor is almost zero. This switches a large voltage across the capacitor CP021 of the snubber network and results in short thus charging current through the capacitor CP022 and CP021 and also through the drain of IP020. This explains the large drain current peak at the start of the conducting phase and is a source of power loss in the power transistor of IP020. The snubber network is described more in detail later on.

Conduction Phase

With IP020 now conducting, the drain current through the primary winding of LP020, and hence through the IC’s drain, rises linearly with time.

Switch OFF Phase

When the power transistor of IP020 switches off the current through the drain is abruptly stopped. At this time, there is a large current flowing through the primary winding of LP020. This causes the voltage across the primary winding and the IC to rise rapidly. In addition, the power transistor’s gate source voltage must be zero during switch off so that it can sustain a



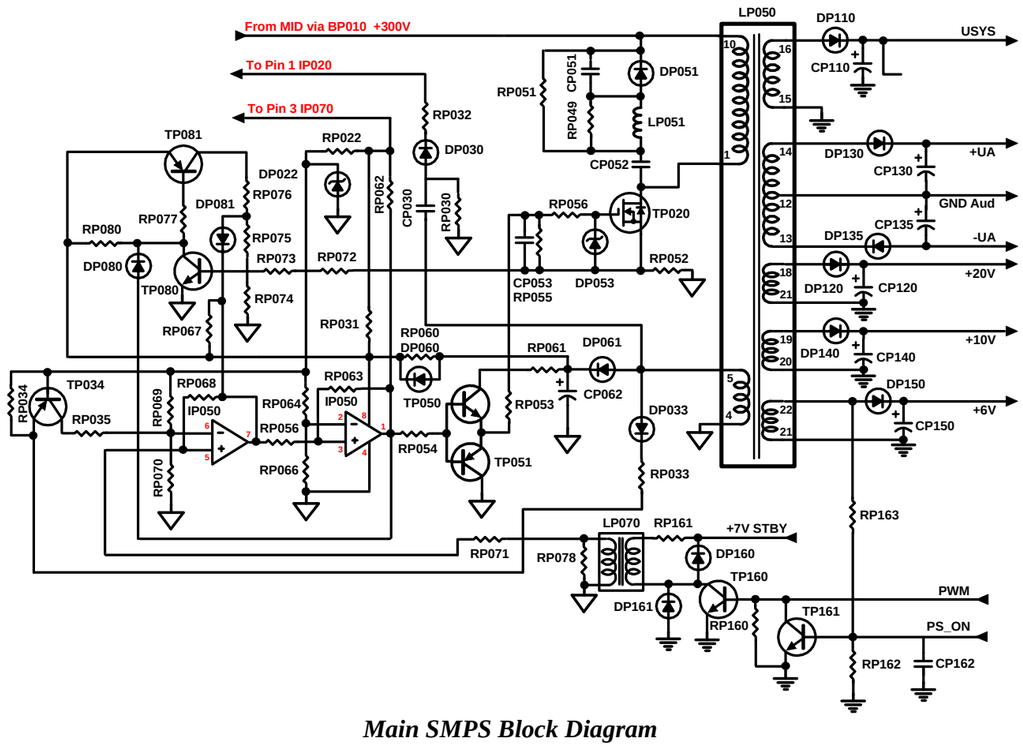
Standby Power Supply Block Diagram

high drain source voltage during this time. This is done internally in the IC IP020.

OFF Phase
The Off time must be separated into two parts: the energy transfer phase and the dead time.

Energy Transfer Phase
Immediately after the power transistor of IP020 switches off, the energy transfer to the secondary starts. The output voltages of LP020 become positive, the secondary diodes conduct and the magnetic energy that is stored in LP020 is transmitted to the secondary capacitors CP220 and CP240 along with linear falling current of DP220 and DP240.

DEAD Time
After the energy transfer is complete, there is a dead time that lasts until the next conduction pulse occurs. During this time, IP020 and the secondary diodes are off and there is no current in LP020. The voltages are oscillating within the winding inductance, the winding capacitance and snubber capacitance.



Main SMPS Block Diagram

Start Up of the Main-SMPS
Oscillator
During “ECO” or “STANDBY”, the resistor RP177 charges CP171. When the upper threshold of the voltage comparator is reached, pin 1 of IP170 is switched to high and a current can flow via 5V_STBY to resistor RP170 into the base of TP170. The upper threshold of IP170 is determined by resistor RP173 and RP174. If the transistor TP170 is switched on, the capacitor CP171 will be discharged by DP171 and RP176.

The parallel resistance of RP174 and RP175 determines the lower threshold of IP170. By reaching this lower threshold, pin 1 of IP170 will be switched to low, transistor TP170 is switched off and capacitor CP171 will be charged. The oscillating frequency of the saw-tooth during “ECO” or “STANDBY” mode is approximately 2.5kHz.

PWM Circuit
The PWM circuit is active during “ECO” or “STANDBY” mode. The PWM pulse at pin 7 of IP170 is present but at a lower amplitude. The transistor TP161 is switched on in “ECO” and “STANDBY” keeping the main SMPS off.

The saw-tooth on pin 6 of IP170 is generated by the oscillator, then compared with a DC voltage on pin 5. During “ECO” or “STANDBY” mode the frequency of the PWM pulse is 2.5kHz and shifted to 18kHz via the resistor RP225 during start up. An additional shift takes place when TP221 turns off because of the additional current that can flow from the 5V_STBY through the resistor RP222 and the diode DP222. This results in a decreased charge time of CP171. The frequency of approximately 28kHz will be synchronized to the horizontal

deflection frequency (31.5KHz) via H_DRIVE after horizontal comes up. More details about the reason for frequency shift during start up can be found in the **Primary Control Circuit** section.

STANDBY to ACQUISITION Mode
When the SMPS is in "ACQUISITION" mode, the deflection stage is not running and all secondary voltages are available to power up the signal board. Because the main SMPS is always going through "ACQUISTION" mode during start up this mode needs to be explained. This section describes this special mode.

If the standby power supply is running and the microprocessor (µP) has switched on the PO signal, the main SMPS starts up. If the PO signal is high, the base of TP210 is also high and no base current can flow, therefore TP210 is switched off along with TP161. The PWM pulses from pin 7 of IP170 are now available to drive the base of TP160.

After a few pulses, the primary control circuit with IP050, TP050, TP051, TP080, and TP081 is now supplied by the winding between pins 4 and 5 of LP050. The rectifying components are CP061 and DP061. The resistor RP060 decouples the smoothing capacitor CP062 from the signal stage during the switch from ECO to STANDBY mode. The diode DP060 ensures that the VCC of IP050 and current limitation circuit of TP080 and TP081 is only 0.7V below the voltage of CP062.

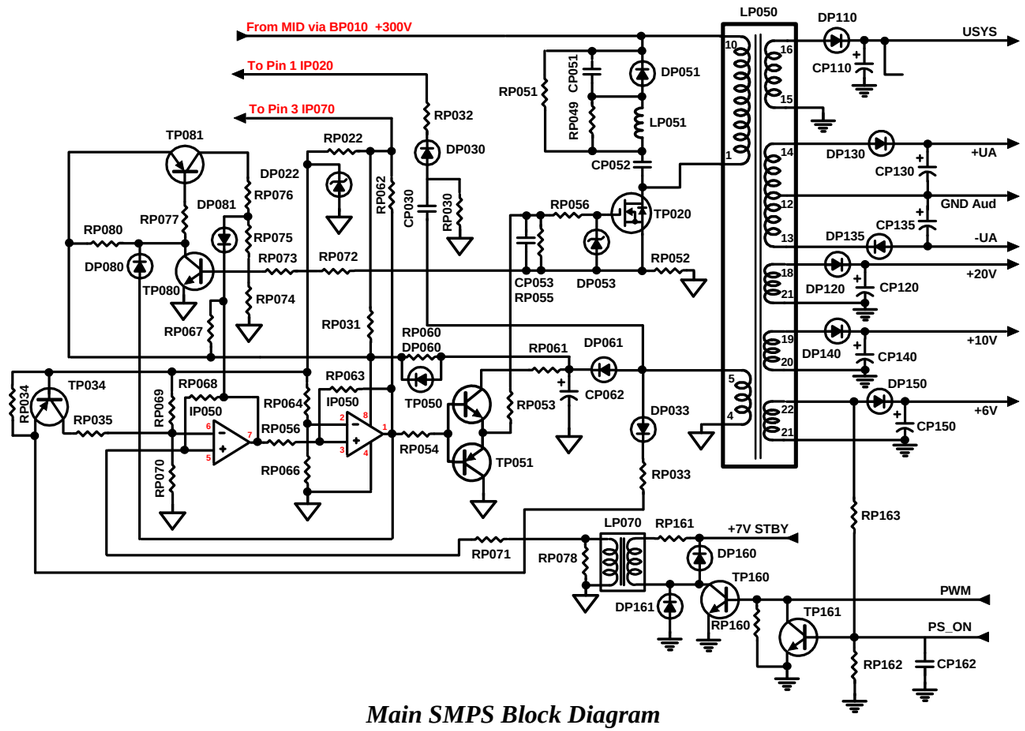
ACQUISITION Mode
The AQR_ON signal is high during "ACQUISITION" mode turning on TP221. With TP221 switched on, base current of TP180 can flow via the resistor RP187 and the diode DP180 to ground. Thus the transistor TP180 is also switched on during "ACQUISITION" mode and the PWM circuit monitors the 6Vr. This provides the secondary regulation pulses in the form of Pulse Width Modulation (PWM). The resistor RP188 and the parallel resistance of PP180, RP184 and RP183 attenuate the 6Vr to provide a DC voltage proportional to the 6Vr. The divided 6Vr, which is given to the base of the transistor TP179, is compared with the reference voltage on the emitter. The reference voltage is based on the 5Vs_STBY but increased by a voltage drop of DP170 that gives a temperature compensation of the voltage comparator TP179. The generated voltage from TP179 is used as one control input (pin 5) by IP170. The capacitor CP182 ensures a stable regulation loop over the used frequency range with a limitation of the bandwidth. The oscillator generates the saw-tooth for the PWM. The values of RP179 and the parallel impedance of RP181 with RP182 in series of DP179 define the maximum t ON time. The comparator of IP170 compares the saw-tooth at pin 6 with the 6Vr proportional DC voltage at pin 5 and the difference between the two voltages controls the t ON time of the PWM signal.

The resistor RP164 provides a pull up for the open collector output of IP170. This PWM signal is applied to the base of TP160. If the PWM signal is high, current can flow from 7Vs_STBY through the winding on pins 3 and 4 of LP070. The resistor RP161 limits the collector current of TP160. LP070 works as a voltage transformer providing a positive signal to pin 5 of IP050. If TP160 is switched off by a low PWM signal, the collector voltage will be clamped by diode DP160 to the 7Vs_STBY. The resistor RP078 is acting as a dampening resistor and will eliminate oscillating. The diode DP161 ensures that no negative voltage "spikes" on the collector of TP160 can generate a signal at pin 5 of IP050.

Primary Control Circuit
The primary control circuit with IP050, TP050 and TP051 is used as buffer and driving stage of TP020. The PWM pulses that will be transferred by LP070 are compared on pin 5 of IP050 with the threshold determined by the resistors RP069 and RP070 at pin 6. The result is a regenerated pulse to drive the second comparator of IP050. Because the outputs of IP050 are open collector the resistors RP067 and RP062 are needed as pull up resistors. The output (pin 7) of the first comparator will be compared with the threshold on pin 2. This ensures, during power up and down, that only pulses at pin 1 can drive the push pull circuit of TP050 and TP051. This protects the transistor TP020 against high losses and improves reliability. The resistor RP054 limits the base current of transistor TP051 if pin 1 of IP050 is switched to ground. Two comparators in series are necessary because the first one is acting as pulse former, with TP034 acting as demagnetization control. The second one is a driving circuit with the transistors TP050 and TP051.

The most critical period of operation for a SMPS, especially for the power transistor TP020, is the starting phase. All capacitors on the secondary side are discharged before switching on and present a short circuit to the SMPS for the first few cycles. The power supply has to be protected during this switch on phase.

For the first cycles, the current limitation becomes active during start up of the main SMPS. The current through diode DP110 is very high and because of the low start up frequency (approximately 2.5kHz), the current will be zero before next switch on of the

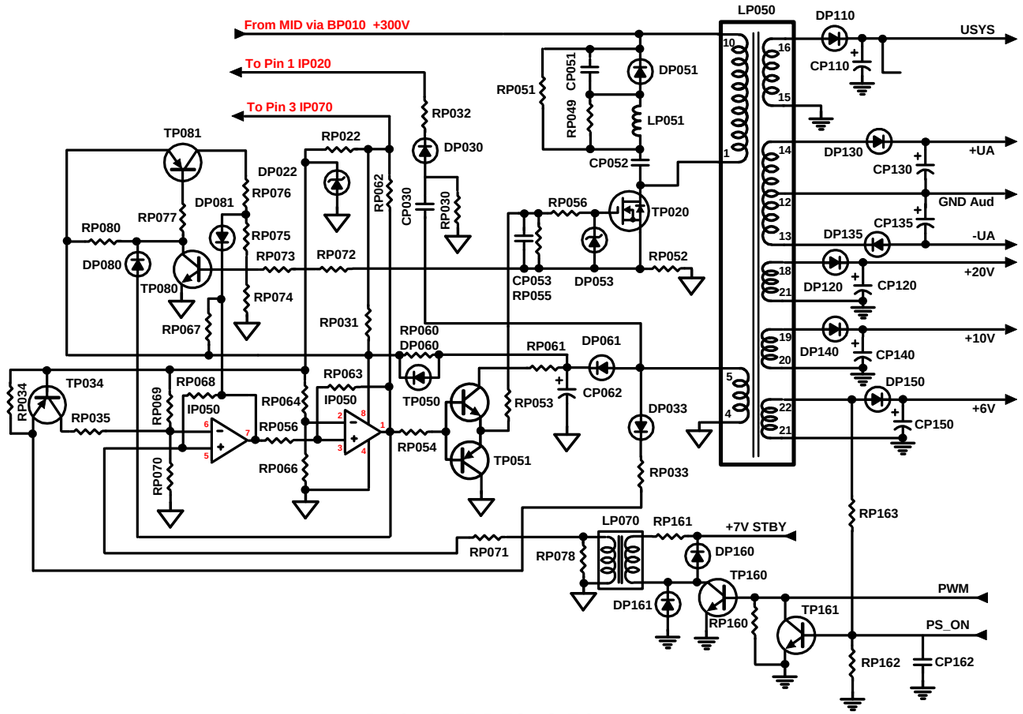


Main SMPS Block Diagram

transistor TP020. This is important because the current of DP110 is not at zero, which means there is still energy inside the SMT. If the transistor TP020 is switched on, it will result in high peak reverse voltage of DP110.

ACQUISITION to ON Mode
After the main SMPS is in "ACQUISITION" mode it depends on the µP(microprocessor) to switch on the horizontal deflection stage. When the horizontal deflection is running, the oscillator with IP170 and transistor TP170 is synchronized by the H_DRIVE signal. The H_DRIVE signal is started approx. 600ms after PO command becomes high.

The transistor TP221 ensures that during "ACQUISITION" mode only the 6Vs regulation is active. This means if AQR_ON is high, the transistor



Main SMPS Block Diagram

TP221 is switched on because a current can flow from the 5Vs_STBY via the resistor RP223 and RP221 in the base of TP221. The resistor RP224, in conjunction with capacitor CP221, is for filtering of horizontal disturbances on the AQR_ON signal.
The time when AQR_ON is switched to low is approx. 100ms after H_DRIVE was started. This ensures that the switch from "ACQUISITION" mode regulation to "ON" mode regulation will be done when the horizontal deflection start up is nearly finished.

ON Mode with Secondary Regulation
The PWM circuit monitors the +USYSr voltage and provides the secondary regulation pulses in the form of Pulse Width Modulation (PWM). The resistors RP900, RP185, RP183, PP180, and RP184 attenuate the +USYSr to provide a DC voltage proportional to the +USYSr. The resistor RP900's value is dependent on the required system voltage for the picture tube. A fine adjustment of the system voltage can be done by variation of the resistor PP180.

The divided +USYSr that is given to the base of the transistor TP179 is compared with the referencevoltage on the emitter. The reference voltage is based on the 5Vs_STBY but increased by a voltage drop of DP170 that provides temperature compensation of the voltage comparator TP179. The generated voltage from TP179 is used as one control input (pin 5) by IP170. The capacitor CP182 ensures a stable regulation loop over the used frequency range with a limitation of the bandwidth. The oscillator that is built with IP170 in conjunction with transistor TP170 generates the saw-tooth for the PWM.

During ON mode ,the lower threshold of the oscillator described in the Oscillator section will be introduced through the negative voltage produced by the differentiation of the H_DRIVE pulse. The differentiation will be done by resistor RP220 and capacitor CP175. This allows the oscillator to synchronize with the horizontal deflection frequency.

The maximum T-ON time is defined by the values of RP181 and RP179 that is approx. 40% of the horizontal frequency. The comparator of IP170 compares the saw-tooth at pin 6 with the +USYSr proportional DC voltage at pin 5 and the difference between the two voltages controls the T-ON time of the output signal PWM.

The resistor RP164 provides a pull up for the open collector output of IP170. This PWM signal is applied to the base of TP160. If the PWM signal is high, current can flow from 7Vs_STBY through the winding on pins 3 and 4 of LP070. The resistor RP161 limits the collector current of TP160. LP070 works as a voltage transformer providing a positive signal to pin 5 of IP050. If TP160 is switched off by a low PWM signal, the collector voltage will be clamped by diode DP160 to the 7Vs_STBY. The resistor RP078 is acting as dampening resistor and will eliminate oscillating. The diode DP161 ensures that no negative voltage "spikes" on the collector of TP160 can generate a signal at pin 5 of IP050.

TP020 - One Complete Cycle in On Mode

Switch On Phase
The rising edge of the pulse from pin 1 of IP050 switches the transistor TP020 on, thus the voltage across the transistor is almost zero. This switches a large voltage across the capacitor CP052 of the primary snubber network. The capacitor CP020 will also be discharged during switch on. This results in a short charging current through the capacitor CP052 and discharging current of CP020 and thus through the drain of TP020. The resistor RP051 limits the size of this current peak.

Conduction Phase
With TP020 now conducting, the current through the primary winding of LP050, through the transistor's drain, and rises linearly with time. For gate drive, this conduction phase must be separated into two parts: the T- ON time of IP050 in conjunction with TP050, TP051, and the storage time of TP020.

T-ON Time of IP050, TP050
During this period, the output from pin 1 of IP050 is high and current flows from the auxiliary voltage via resistor RP061, the transistor TP050, and resistor RP053 into the gate of TP020. The auxiliary voltage winding is between pins 4 and 5 of LP050 using rectifying components CP062 and DP061. This voltage is approximately 14V and supplies the primary control circuit IP050, transistors TP050, TP051, TP080 and TP081 during "ACQUISITION" or "ON" mode. The resistors RP061 and RP053 define the value of the positive gate current. The resistor RP055 gives the gate of TP020 low impedance and eliminates the risk of unwanted switching on. The diode DP053 ensures that the gate source voltage of TP020 is limited and a high energy or burst pulse from the AC can't destroy the transistor.

Storage Time of TP020
The storage time of TP20 is the duration required to cut off the drain- source channel of the power transistor. At the beginning of this period, the gate current is reversed in direction by pin 1 going low and the current flows from the gate via the transistor TP051 to ground. Resistor RP053 limits the negative gate current. The storage time of the power transistor TP020 is very small.

Switch OFF Phase
When the power transistor TP020 switches off, the current through the drain is abruptly cut off. At this time, there is a large current flowing through the primary winding of LP050. This causes the voltage across the primary of LP050 and the transistor TP020, to rise rapidly. The snubber network limits the increase time of this voltage. In addition, the power transistor's gate-source voltage must be zero during switch off so that it can sustain a high drain

source voltage.

OFF Phase
During the off phase, the power transistors gate is held to zero. In a synchronized SMPS, the off time must be separated into two parts: the energy transfer phase and the dead time.

Energy Transfer Phase
Immediately after the power transistor TP020 switches off, the energy transfer to the secondary starts. The output voltages of LP050 become positive, the secondary diodes conduct and the magnetic energy that is stored in the SMT LP050 is transmitted to the secondary capacitors with linear falling current of all secondary diodes.

During this energy transfer phase, the voltage on TP020's drain is the sum of the rectified mains voltage across CP010 and the secondary system voltage multiplied by the primary secondary turns ratio of the transformer.

Dead Time
After the energy transfer is complete, there is a dead time that lasts until the next conduction pulse occurs. During this time, the transistor TP020 and the secondary diodes are off and there is no current in LP050. The voltages are oscillating with the winding inductance, the winding capacitance and snubber capacitance.

Primary Side Snubber Network
The primary snubber network consists of CP052, DP051 and RP051. When the transistor switches off, CP052 is charged through DP051 by the current from the primary inductance (this current flows into CP010 thus returning some energy to the system). This reduces the cascading effect on the transistor and now energy is stored in CP052. The next time the transistor switches on, CP052 is discharged through RP051. Thus the energy stored in CP052 is transferred to RP051 and dissipated as heat. For this reason, RP051 has to be a large 10W resistor. The coil LP051 with dampening resistor RP049 in parallel limits the current flowing into the diode DP051 and thus reducing noise in the picture.

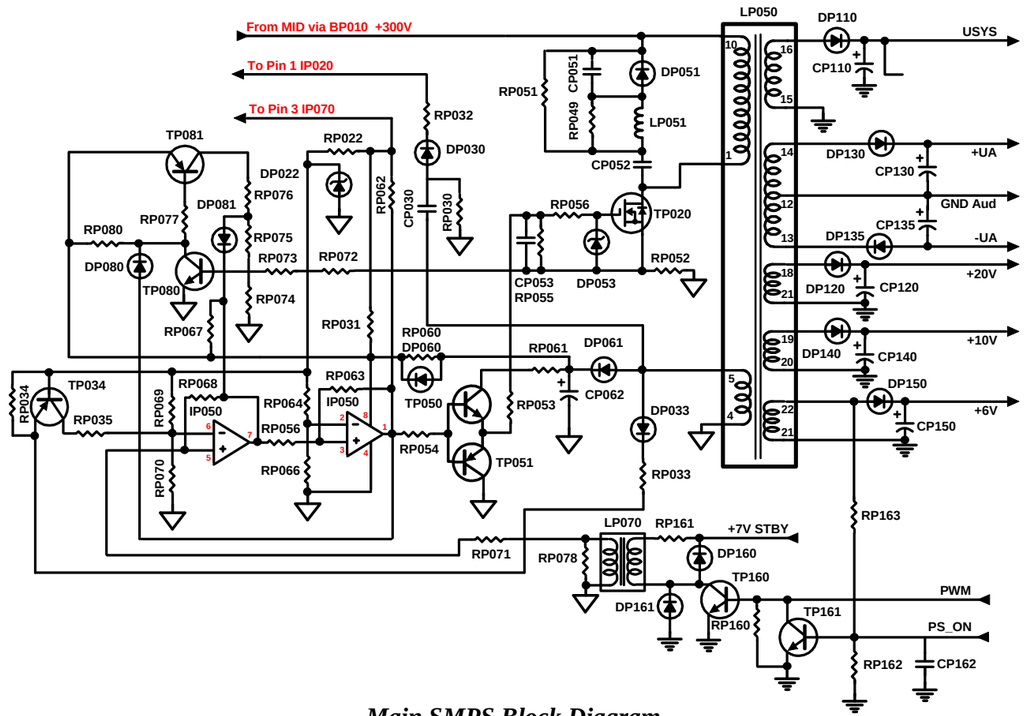
The additional snubber capacitor CP020 that is parallel to the transistor's drain and source has the additional effect of limiting the current on the transistor TP020. This helps to reduce noise generated by switching of TP020. The capacitor CP019 works in the same direction as the capacitor CP220. The difference being capacitor CP119 is connected via ferrite bead between drain of TP020 and ground. This provides a better result for EMI and the ferrite bead LP004 avoid oscillating from the falling edge of TP020's drain current.

Secondary Side Snubber Network
The snubber network on the secondary side consists of CP112, DP111, DP112, DP113, LP112 and RP112. When the transistor TP020 is on, the capacitor CP112 is charged through the diode DP113 to the negative forward voltage of the system voltage winding. The inductance LP112 limits the slope of the charging current and thus provides a slow charging of the capacitor CP112 when the transistor TP020 switches on. When the transistor TP020 is switched off, the voltage across the system voltage winding rises rapidly including the voltage on the anode of the diode DP112. When the voltage on the anode of the diode DP112 reaches the level of the 10Vr, the diode DP112 starts to conduct. When the diode DP112 starts to conduct, the capacitor CP112 discharges and reduces the flux of the secondary (and hence the primary due to coupling) winding.

The resistor RP112 is necessary to dampen oscillations between the inductor LP112 and the capacitor CP112. An additional filter with the coil LP114 in conjunction with capacitor CP114 is needed for picture disturbance improvement. The ferrite bead LP113 and the capacitor CP113 helps to reduce picture pollution generated by switching of the diodes DP112 and DP113. Energy that is stored in LP112 is also given back via the diode DP111 to the 10Vr. Unlike the primary snubber network, the secondary snubber network returns the energy stored in the capacitor CP112 to the system. In this case, the 6V capacitor CP150.

Demagnetization Control
The demagnetization control circuit prevents the power transistor TP020 from switching on while the SMT LP050 is still magnetized. Without this magnetization control, the transistor TP020 could switch on while LP050 is still magnetized. When this happens, the switch on current through TP020 will be too high reducing the reliability of the transistor TP020.
Another problem is the diode DP110 will be damaged if the transistor TP020 is switched on and LP050 is still magnetized because this will result in a high peak reverse voltage of DP110.

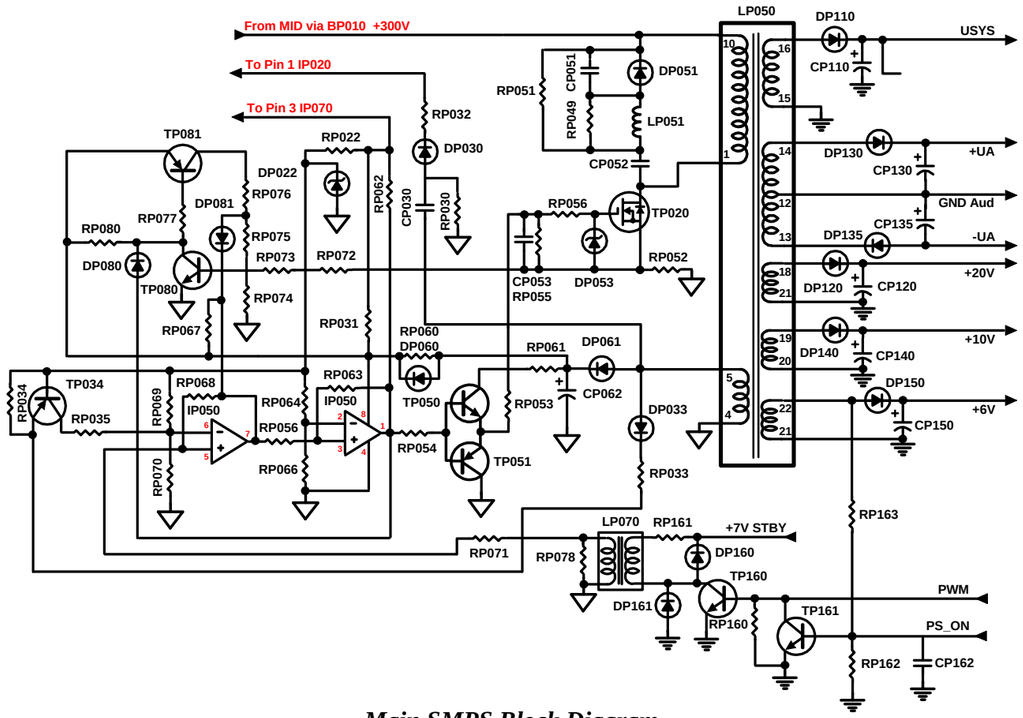
Secondary side
The circuit with RP162, RP163 and TP161 prevents the power transistor TP020 from switching on while LP050 is still magnetized. When LP050 is still magnetized, the secondary diodes are still conducting and



Main SMPS Block Diagram

the voltages across the secondary windings are clamped. When LP050 is completely demagnetized, the secondary diodes are no longer conducting and the voltages across the secondary windings fall. Thus the voltage across a secondary winding is used to switch the transistor TP161 so that it can inhibit the secondary regulation pulses from the PWM circuit (IP170, TP173, TP179) while LP050 is still magnetized. The 6Vr winding was chosen to drive this demagnetization circuit because it has the lowest voltage across its secondary winding. The capacitor CP162 is for filtering during fold-back conditions.

Primary side
An additional circuit with transistor TP034 ensures that any PWM pulse delivered from secondary side via LP070 is disabled during fly-back time of the auxiliary voltage that is taken from the winding between pin 4 and 5 of LP050. The auxiliary voltage is attenuated with the resistors RP033 and RP034 compared with the base voltage of the transistor



Main SMPS Block Diagram

TP034 that is the zener voltage of the diode DP022. This means the transistor TP034 is switched on during fly-back and the threshold of the first comparator from IP050 is set to a higher level than the pulse from LP070. Therefore, pin 7 can not be switched high and the driving circuit with the transistors TP050 and TP051 is still switched off.

Secondary Voltages

+USYSr

The system voltage windings are between pins 15, 16 and 17 of LP050. The rectifying components are CP110 and DP110. CP111 is necessary to reduce noise caused by the switching of DP110. The jumpers JP911 and JP912 select the required system voltage (+USYSr).

In "ACQUISITION" mode, the +USYSr is approximately 150-190V, which depends on the load. The regulation for the SMPS in "ON" mode is done using the +USYSr because of the high load variation on this voltage. The system voltage provides the main power source for the Diode Split Transformer (DST) sometimes also referred as Integrated High Voltage Transformer (IHVT) and the line deflection. The system voltage can supply the DST with enough picture power of 60W. The tuner is also supplied from the system voltage via RP113, RP114, RP117, RP120 and a 33V Zener diode that is located on the signal board. The capacitor CP562 improve EMC situation.

20Vr

The 20Vr winding is between pins 18 and 21 of LP050. The rectifying components are CP120, DP120 and noise suppresser CP121. The 20V supplies, in ON mode, the horizontal driver circuit and for an external module via connector BP120. It is also used for the 5V regulator located on SSB or the BSVM circuit located on CRT board.

10Vr

The 10Vr is between pins 19 and 20 of LP050. The rectifying components are CP140, DP140 and noise suppresser CP141. The 10Vr has a nominal value in "On" mode of 11.5V. In "ACQUISITION" mode, this voltage is approximately 11.8V. The 10Vr voltage supply in "ACQUISITION" and "ON" mode supplies the different 8V regulators on the signal board. The coil LP140 along with the capacitor CP512 gives an

additional filtering of the used input voltage for the different 8V regulators on the signal board. The capacitor CP511 parallel with CP512, ensure low impedance during arcing.

6Vr

The 6Vr winding is between 21 and 22 of LP050. The rectifying components are CP150 and DP150. The capacitor CP151 is necessary to reduce picture noise caused by switching of the diode DP150. The 6Vr supplies the "ACQUISITION" and "ON" mode for 5V regulation and 3.3V regulator on the small signal board. The inductance LP151 with the capacitor CP522 giving additional filtering of the input voltage of the 5V regulator. The capacitor CP521 parallel to CP522, ensure low impedance during arcing.

5V_A/5V_H

In "ACQUISITION" and "ON" mode, the 5V regulation is supplied by the secondary voltage 6Vr that was described previously. The voltage reference for the 5V regulation is the REF voltage that is generated by the UP converter. Dual transistor TP523 (A & B) are acting as a differential voltage stage with an advantage of temperature stabilization. The resistors RP527, RP523 and RP524 divide the 5V and, therefore; the voltage at the base of TP523B is compared with the reference voltage on the base of TP523A.

Because the current sum of the dual transistor TP523 flowing through RP522 is always the same, it depends on the level of the 5V either transistor or both is more or less conductive and thus the level of the gate voltage from TP520 which results in a regulated 5V. To ensure that the gate voltage of TP520 is high enough, the +20V is used via the resistor RP520. The diode DP520 limits gate voltage of TP520 during arcing or ESD. The resistor RP525 limits the base current of TP523 and is acting as a filter in conjunction with CP524 to reduce ripple on the reference voltage. The resistor RP520 and capacitor CP527 define the loop gain and frequency bandwidth of the regulation loop.

9Vr

The voltage regulator IP540 is used to generate the 9Vr voltage, which is located on the signal board and is mainly used for front end. The output voltage at pin 3 of IP540 has an additional smoothing capacitor CP544 and CP543 is used to avoid high frequencies and oscillations.

8Vr

The voltage regulator IP510 is used to generate the 8Vr, which is located on the small signal board and is used for 2H video processing. The output voltage at pin 3 of IP510 has an additional smoothing capacitor CP514 and capacitor CP513 is used to avoid high frequencies and oscillations.

3.3Vr

The 3.3Vr voltage regulator IP530 is located on the small signal board and is used for the UP-converter. The output voltage at pin 2 of IP530 has an additional smoothing capacitor CP534 and capacitor CP533 is used to avoid high frequencies and oscillations.

1.8Vr

The 1.8Vr voltage regulator IP531 is located on the small signal board and is used for the UP-converter. The output voltage at pin 2 of IP531 has an additional smoothing capacitor CP536 and capacitor CP535 is used to avoid high frequencies and oscillations.

Sound Voltages

The dual sound voltage windings are between pins 12, 13 and 14 of LP050 with pin 12 being the audio ground. The rectifying components are CP130, CP135, DP130, DP135 and noise suppressors CP131 and CP136. The resistor RP137 that is connected between audio ground and chassis ground ensures that the audio ground is not floating in relation

to the chassis ground. The sound voltages (±UA) have a nominal value in “ON” mode (sound muted) of ±17V.

In “ACQUISITION” mode, these voltages are approx. ±18V. The resistors RP130 and RP135 provide a small load on the ±UA that prevents the output voltages from rising above 20V in mute. Because of the large load variation between mute and full volume, the regulation of the sound voltages is poor relative to the other secondary voltages. The ±UA supply the audio output amplifiers and supply the requested output power that is needed for the different versions.

Protection

The protection in the ITC222 SMPS has been designed so that when a short circuit or overload occurs on a secondary voltage, the SMPS switches off completely. In addition the 6Vr is monitored to switch off the SMPS if an open loop of the PWM results in an over-voltage situation.

Primary Protection

On the primary side, a current limitation by cycle to cycle exists. The maximum transferable power is limited and all secondary voltages will drop down if this limit is reached for a certain length of time. The resistors RP072, RP073 and RP074 attenuate the voltage of RP052 to provide a voltage proportional to the drain current of the transistor TP020 and used as an input of the circuit with the transistors TP080 and TP081. The capacitor CP073 in conjunction with resistor RP073 are acting as a filter against voltage spikes. If the voltage at resistor RP052 becomes high enough, base current of transistor TP080 can flow and transistor TP080 will be switched on. Also TP081 is switched on to speed up the switch on of TP080.

The switch on of TP080 results in pin 1 of IP050 being switched to ground via the diode DP080. Because the input stage and the driving circuit is decoupled by the voltage comparators of IP050, the current limitation circuit will be reset by the diode DP081 if the input pulse of LP070 and pin 7 of IP050 is going from high to low. If the level of maximum drain current is reached, the transistor TP020 will be switched off and the input of the first comparator IP050 is still high.

Secondary Protection via Safety Circuit

Under voltage protection

The +20Vr is used to ensure correct connection of BP005 and BL111 via the lines CNT1_+20V and CNT2_+20V. The CNT2_20V is attenuated by the resistors RP540, RP521, RP530, RP526, RP193, RP196 and compared as an input voltage on pin 5 with the reference voltage on pin 6 of IP190. The reference voltage on pin 6 is generated by the +5Vs via RP571, RP189, RP199 and RP200 that charges the capacitor CP199 when the “PO” signal goes low. The time delay is necessary to ensure that all secondary voltages that are controlled are at nominal level before the safety circuit becomes active. To ensure the protection is disabled during switch on of the SMPS a small voltage drop will be generated by the voltage divider RP190/RP196.

If any of the secondary voltages (which are controlled by the circuit DP521, DP530, DP540, DP501, DP510, and DP193) drop below 50% of the nominal value, pin 7 of IP190 is switched to ground. Therefore, TP210 will be switched on and the transistor TP161 will disable the PWM pulses from pin 7 of IP170 to the base of transistor TP160. This means the SMPS will be stopped.

An additional safety circuit with TP197 controls (via RP198) the negative voltage -UA and will be switched on if the voltage -UA is less than 50% of the nominal value. This will cause base current from the voltage +UA via RP197. A switch ‘on’ of TP197 is the same result as before so the voltage on pin 5 is lower than on pin 6 of IP190. The same situation as described before results in a switched ‘off’ SMPS. The resistor RP192 together with capacitor CP158 is for filtering against crosstalk of the collector line from TP197. The diode DP197 ensures that the base voltage of TP197 is limited to a maximum negative voltage of -0.7V and the capacitor CP197 filter, in conjunction with RP197 and RP198, decreases the ripple of the audio voltage and ensures that TP197 is not switched on if a small spike occurs on +UA.

Over voltage protection

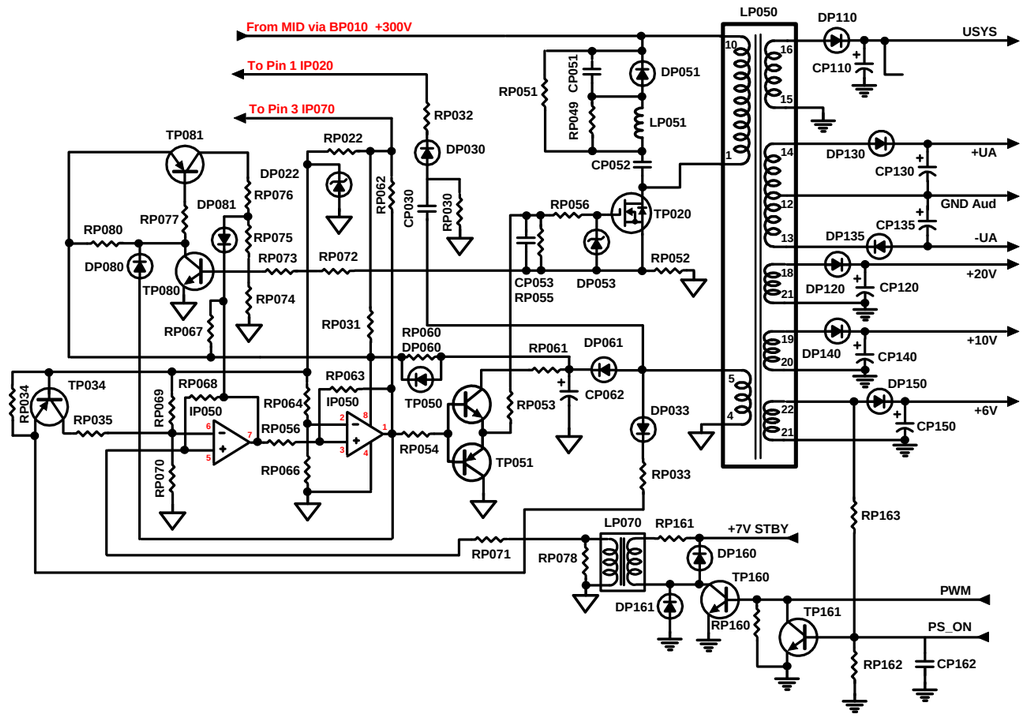
If there is a open loop of the PWM regulation, the +6Vr increases and the voltage comparator at pin 2 of IP190 becomes higher and pins 1 and 3of IP190 will be switched to ground. With pin 1 at ground, TP210 is switched on and as a result the transistor TP161 will disable the PWM pulses from pin 7 of IP170 to the base of transistor TP160 thus stopping the SMPS.

Fold-back Point

The fold-back point is where the load on the output of the power supply is increased until the SMPS can no longer regulate and the +USYSr starts to fall.

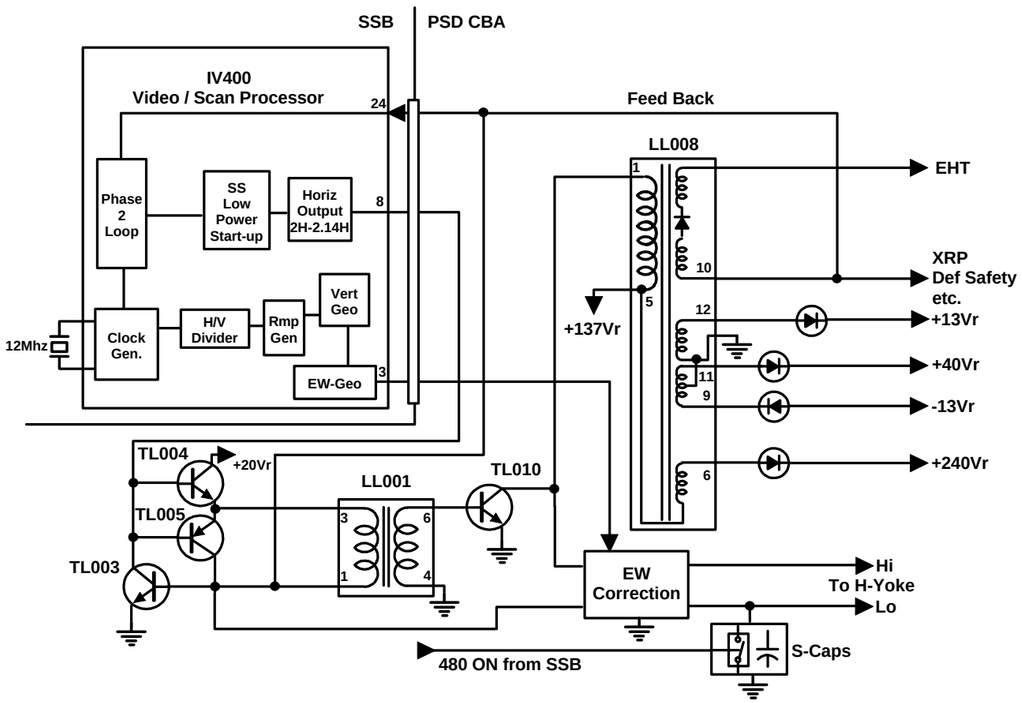
The reason that the power supply can no longer regulate for large loads is that the drain current of TP020 is so large that the current limit threshold is reached. This effectively limits the energy that can be stored in LP050 and hence the energy that can be transferred to the secondary side.

ITC222
CIRCUIT OVERVIEW

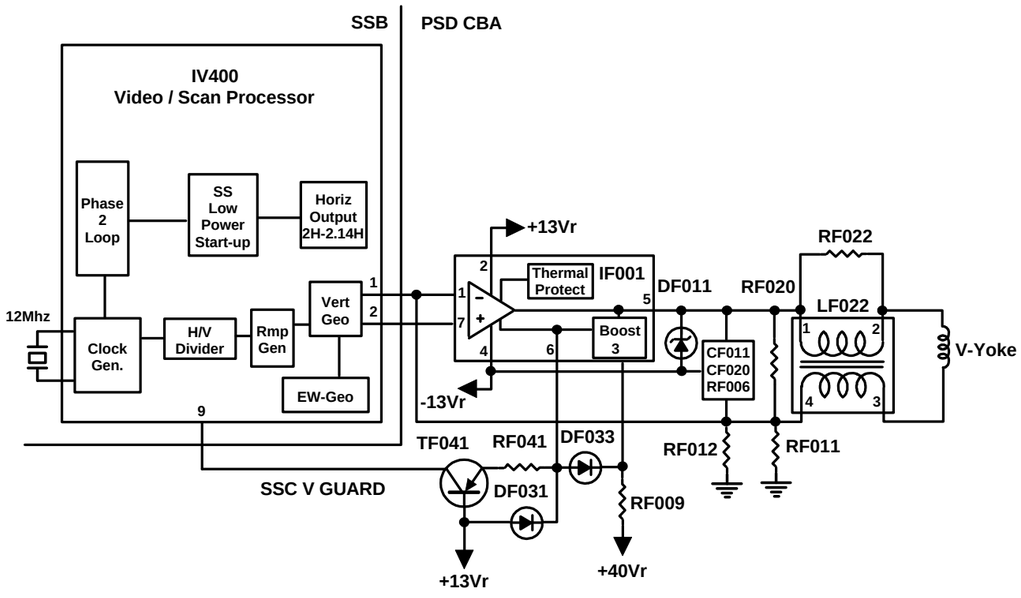


Main SMPS Block Diagram

Page 5-15 Return to Table of Contents



Horizontal Block Diagram



Vertical Block Diagram

Deflection Overview

The deflection overview can be divided in the following functional blocks:

- Deflection Controller – IV400 (HOP)
- Horizontal deflection
- **H**orizontal **O**utput **T**ransistor TL010
- High voltage source; **IHVT** LL008
- East/west correction - diode modulator
- 2H/2.14H adaptation
- Vertical deflection
- Earth field correction = Picture Rotation (**EFC**)
- Deflection safety circuitry
- X-ray protection circuitry

The heart of the deflection is the I²C-BUS- controlled video and scanning processor IV400. IV400 uses an external 12Mhz ceramic resonator for generating a stable clock that will be synchronized with h-sync (“H-DFL” signal) and v-sync (“V-DFL” signal) from the up conversion process by means of a “PHI 1 loop” on the 2H side.
The “HOP” driver generates the base currents for driving the horizontal output transistor in forward mode. An implemented current regulation ensures an ‘always-good’ driving condition independent from supply voltage variation given by different power supply loads.

Supply voltages delivered by the IHVT transformer are:

- Anode (EHT) voltage
- Static and/or dynamic focus and G2 voltage (from focus block)
- +200V video voltage (boosted by Usys)
- +Uvfb, vertical fly-back voltage
- +Uvert, positive vertical supply voltage (+13V)
- -Uvert, negative vertical supply voltage (-13V)
- Picture tube heater voltage

A diode modulator for modulation of the picture width is driven by a parabolic waveform to correct the pincushion distortion of the picture tube. The diode modulator also includes the linearity correction linearity coil and the dynamic S-correction at double the frequency.
The vertical amplifier IF001 is driven by two differential saw tooth currents from the “HOP”. The feedback information is generated from the voltage drop over the vertical sense resistor and the vertical yoke is driven to GND. This concept needs a positive and a negative supply voltage plus additional fly-back supply to guarantee the retrace time.

The safety circuit senses all output voltages from the deflection. It reacts when an open or short circuit occurs in the deflection (H and V) or excessive high voltage.

X-ray protection is detected by using a “window-comparator” (build with two OP-Amps IV820 and IV821), comparing a rectified retrace signal with an adjustable reference signal. The circuitry reacts on excessive EHT as well as on too low EHT.

The different safety information from the deflection is “DEFL_SAFETY”, “EHT_INFO”, “EW_PROT” and “SSC_V_GUARD”. These signals are passed to the signal processing board where they are processed and connected to the EHT-protection input (*Pin 4*).

The threshold for *Pin 4*, the EHT (over-voltage) protection is 3.9V. Once the level at this pin exceeds 3.9V the “HOP” goes to STBY via slow stop procedure. The XPR status bit will inform the µP. The µP configures the over-voltage input pin either to detection or protection mode. The detection mode is valid during alignment procedure and the protection mode is valid during normal operation.
The “SSC_V_GUARD” information leads to RGB blanking in case of a vertical defect. This signal is also used on the optional DFB module for generation of focus blanking during cut off measurement.

Deflection Processor (HOP)

IV400 is a combination of RGB output processor and deflection processor. It provides:

- A stable clock generation using an external ceramic resonator
- Horizontal synchronization with two control loops and alignment free oscillator
- Slow (soft) start and slow stop of horizontal drive output to enable low stress start- up and switch off
- Vertical countdown circuit for stable behavior, including absence of H and / or V sync.
- Vertical linear zoom from 75% to 138% of adjusted nominal amplitude
- Vertical scroll function used for raster panning
- Progressive scan
- Horizontal and vertical geometry control
- Several safety inputs

During “ACQUISTION” mode or after the main power supply comes up and the supply voltage for the “HOP” is present, all registers can be initialized with correct (adjusted) values. This means the deflection can start with defined settings.

The HOUT pin 8 is the driver for horizontal deflection. Under normal operation the duty cycle of HOUT pulse is 48.2% off (high) and 51.8% on (low). When a fly-back pulse is present at pin 13 (HFB), HOUT is always

set high irrespective the status of the output. In this way, switch on of the HOT during fly-back is prevented. The detection level is .3V.

A built in slow start/stop circuit ensures a smooth start/stop behavior of the deflection. During 'switch on', the horizontal output starts with a fixed off time of 48.2% while the on time increases from 0% to 51.8%. The "on time" increases from 0% to 6.2% and lasts 50ms, while the on time increase from 6.2% to 51.8% and lasts 100msec. These values lead to a linear build-up of the EHT voltage in 150msec while the horizontal frequency decreases from about double the final frequency to the final frequency. By using the ESS (**e**xtended **s**oft **s**tart) function the on time increases from 39% to 51.2% is extended to 1000msec. When switched off via the standby, the off time remains fixed on 48.2% while the on time decreases from 51.2% to 0% in 43msec. The on-time decrease starts after vertical scan and vertical fly-back is completed.

The saw tooth signal that is derived from an internal generator is controlled by I²C bus. Control functions are vertical amplitude, vertical shift, vertical s-correction, vertical expand (zoom), and vertical scroll. To prevent picture tube damage, a built-in blanking shunts the RGB outputs for vertical over scan larger than 105%. The vertical geometry processor has a differential current output for a DC coupled vertical output stage.

The horizontal geometry processor has a single-ended current output for EW drive. It offers I²C control for EW width, parabola width, corner parabola, and trapezium correction.

Both the vertical and the EW drive can be modulated for EHT compensation. This tracking makes the picture size independent from EHT variation due to the beam current.

Horizontal deflection
Horizontal driver
The transformer driver for the horizontal deflection output transistor is operated in forward mode. A positive voltage, depending on the duty cycle of the driving signal, appears at CL005 as a virtual ground. The primary winding input is switched to positive and negative voltages referenced to this ground.

The +20Vr is regulated by the linear operation of TL004. A current feedback via sensing resistor RL015, RL005 and TL005 is used for a temperature independent regulation of the base current.
RL006 and CL006 create the correct shape for the base current of TL003 to minimize the saturation losses. TV891, the first transistor of the driver circuit, which is located on the signal board, is highly saturated when TL030 (DV only) is switched off shorting the collector of the regulation transistor TL003. When TV891 is high impedance, by a low signal of H_DRIVE, the voltage at the collector of

TL003 is regulated to drive the output transistor TL030 (DV only) with the correct base current.

NOTE: TL030 (DV only): The implementation of a MOS transistor in the emitter of a bipolar transistor to improve its switching performances is well known and has been used in full-integrated driving solutions. The advantage of the MOS solution is that the emitter current being suddenly stopped, the current in the collector keeps on flowing through the base until switch-off. This switch-off characteristic is independent and no more a function of the driver.

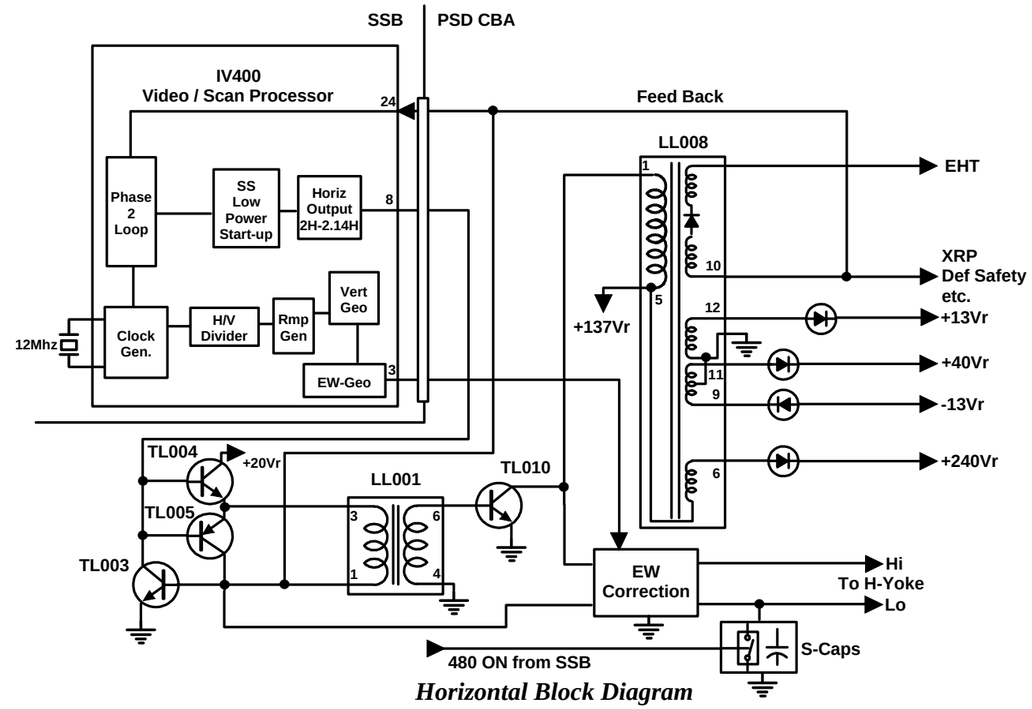
Diode modulator
A diode modulator is used to modulate the horizontal deflection current with minimum effect to high voltage. This can only be achieved, if the primary current is not influenced by the changes of the currents inside the deflection circuit.

The diode modulator is a bridge connection of 2 circuits with the same resonant frequencies. One part is the bridge coil LL029 together with CL032 in series connected with CL029. The other part is the deflection yoke together with the retrace capacitor CL031 in series connected with CL135. The L*C products of both circuits are the same.

The capacitive divider CL031 and CL032 produces a retrace voltage across CL032. The integrated value of this voltage could be seen across CL029 if the diode modulator is uncharged. In this case we have a minimum AC voltage across the deflection yoke and the deflection current is minimal. The voltage across CL029 reduces the supply voltage for the horizontal yoke. If CL029 is shorted, we have the whole supply voltage across the deflection yoke and the deflection current is at maximum. Current out of CL029 during the trace discharges CL029 so that the energy to be stored in LL029 is less at the beginning of the next retrace. As a consequence the retrace voltage across CL032 is less.

The circuit can also be described as two deflection circuits, which are in series and operate at the same frequencies. LL032 suppresses fast current transients

ITC222
CIRCUIT OVERVIEW



Horizontal Block Diagram

to reduce HF noise. RL032 will dampen the current in the coil in order to avoid spike lines.
In the DV version, CL130 and C131 are chosen together with the primary inductance of the DST to have no frequency change during the fly-back on the lower part of the diode modulator. LL034 and CL034 build a series resonant circuit for dynamic S-correction. It is adjusted slightly higher then double line frequency to correct the horizontal linearity. The network DL034, DL036, RL036 and CL036 create a dampening network to suppress oscillations on the S-capacitor CL035 after fast changes of the beam current.

East west correction
The east west correction occurs by using a MOSFET as a power transistor (TL029). This FET is driven by IV400 with a current sink, reducing the gate voltage defined by the feedback resistor RL028. Resistors RV026, RV026, and RL028 define the correct working range. Resistors RL021 and RL025 are connected between TL029 (source) and GND and are used for sensing the current in the EW circuit and improve the temperature behavior by terms of current feed back. DL029 and DL028 are needed to secure the EW circuitry. In “ACQUISTION” mode, current has to be high enough to safely activate overload protection of power supply. Capacitors CL025 or CL028 are needed to avoid oscillation. IHVT compensation is done inside the HOP IC.

2H-2.14H mode Retrace time adaptation
Due to the different horizontal frequencies, 2H (31.47KHz) and 2.14H mode (33.75KHz), there would normally be major changes in EHT. To avoid this, there are two possibilities. Either to change the B+ voltage or to make a retrace time adaptation.

To prevent major changes in EHT, a change in retrace time of 0.4µsec is needed. Therefore, 5.0µsec for nominal retrace time in 2.14H mode and 5.4µsec as retrace time for all 2H signals. Switching a second capacitor in 2H mode parallel to the upper and lower retrace capacitor provides the retrace time adaptation.

The switching signal from the µP is named 480_ON. This signal goes high during 2H mode and low during 2.14H mode. A high at signal 480_ON forces TL100 to conduct turning off TL104. The gate of MOSFET TL105 goes high through RL112 and diode of IL110(in DV only), switching capacitor CL105 parallel to CL032.

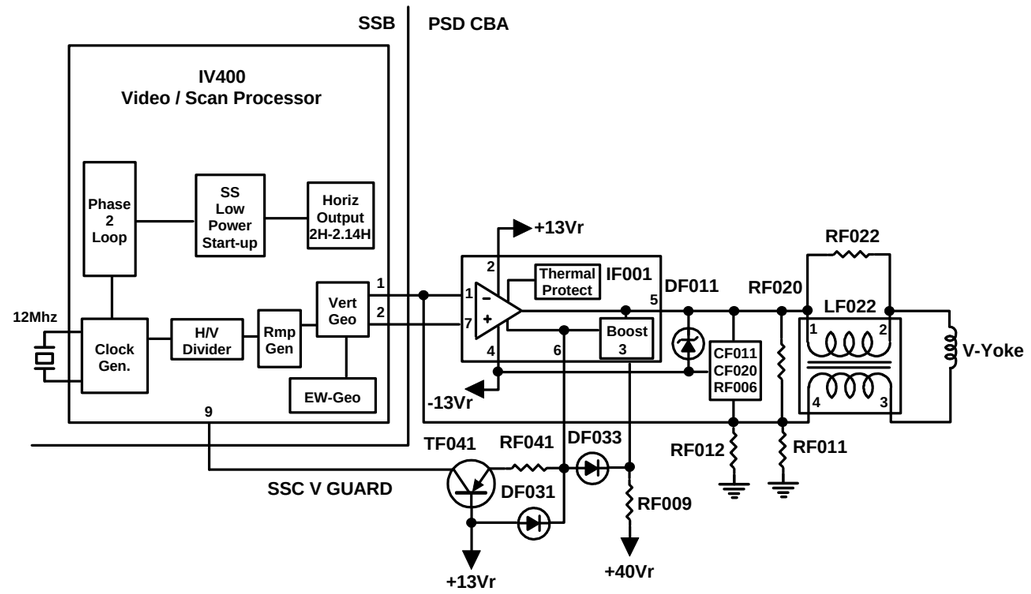
Because the upper retrace capacitor is floating, there needs to be a slightly more complicated driver circuit. The supply voltage for this driver circuit is stored in CL110. Diode DL106 is conducting during trace time and de-couples the +6V from the floating driver circuit during horizontal retrace. If TL100 is off, the base of TL111 goes high through RL106, DL105, DL104 and RL105. This causes a low at the base of TL120, forcing it to turn off. Once TL100 starts conducting by the 480_ON signal, TL111 is turned off. Now TL120 has base current through RL110 and RL120 allowing TL120 to switch CL120 parallel to CL031.

In the DV version, the signal at the base of TL105 is also connected via RL136 to the gate of MOSFET TL135. TL135 shorts out CL135 in 2H mode. This means the tuned circuitry of LL034 and CL034 works on a lower resonant frequency in 2H mode than in 2.14H mode. Where capacitor CL135 is series connected to CL034 this reduces the “effective” capacitance and therefore increases the resonant frequency. To get a proper linearity in 2H as well as in 2.14H mode, additional capacitor is switched for 2H mode in parallel to the main S-capacitor. MOSFET TL140 does the switching. TL140 is driven by opto-coupler IL140. The opto-coupler provides switching when using a diode modulator with IPIN correction, where the main capacitor is floating.

Vertical power stage
The ITC222 uses a plus and minus supply for the vertical power IC IF001. The vertical deflection yoke is connected over a sense resistor to GND. This makes the sensing of vertical current for feedback information very easy.

The power required for the first half of vertical deflection (trace), is drawn by IF001 from the +Uvert (+13V) rail. The –Uvert (-13V) rail supplies the second part of the vertical trace. For retrace, the power is taken from the special retrace voltage called +Uvfb. All three voltages are generated by the IHVT.

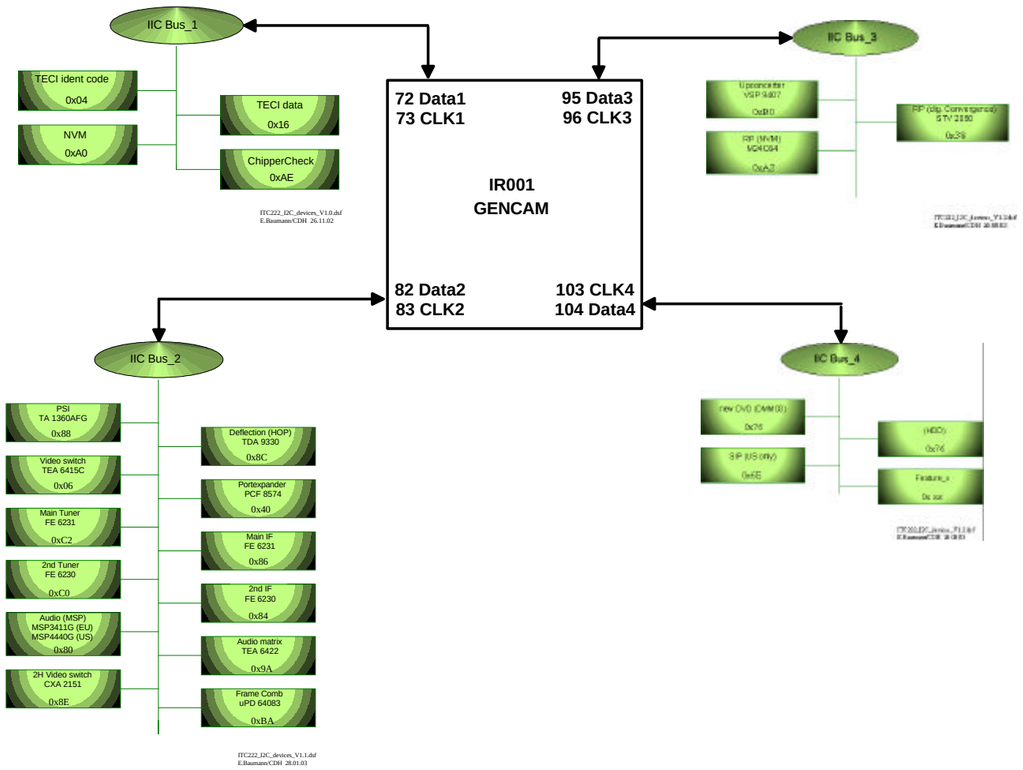
The deflection processor IV400 was originally designed to work together with a vertical power stage in bridge configuration. Due to the vertical IC used, it is necessary to make a current-voltage conversion of the two vertical signals (“v_drive_+” and “v_drive_-”). This is done with resistors RF003, RF004, RF005, and RF006. Transistor TF041 generates the vertical guard information together with RF041 and RF040. A small current goes into the SSC pin of the deflection processor during each vertical period of the SSC signal. If this information is missing, IV400 detects a vertical error and blanks the RGB outputs to avoid damaging the picture tube. The generation of vertical S-correction is done inside the HOP. The amount of correction is adjustable via I²C bus.



Vertical Block Diagram

EFC correction (Direct View Only)
The earth field correction will be controlled via software by means of the pulse width modulated signal “EFC”. The direction and the amount of current are dependent on the bias voltage of the earth field correction power stage. The user can control this voltage via menu option Picture Rotation. “EFC” is a 5V PWM signal that is converted to ±Uvert by TL801 and TL803. RL806 and CL806 are the integrator of the PWM. TL807 and TL808 is the power amplifier for the EFC current. The output signal of the EFC power stage is fed through BL200 to the CRT board and then to the two-pin connector BB007 where the EFC coil is plugged in.

Dynamic S-correction and 2H Correction (Direct View Only)
Flat panel CRT’s have a special geometry distortion. The correction of this distortion is called “dynamic S-correction” or “2H correction”. The 2H correction is a tuned circuit consisting of a transformer and a capacitor. The resonant frequency is 76kHz.



GemCam Communications Bus Block

SYSTEM CONTROL (GenCAM)

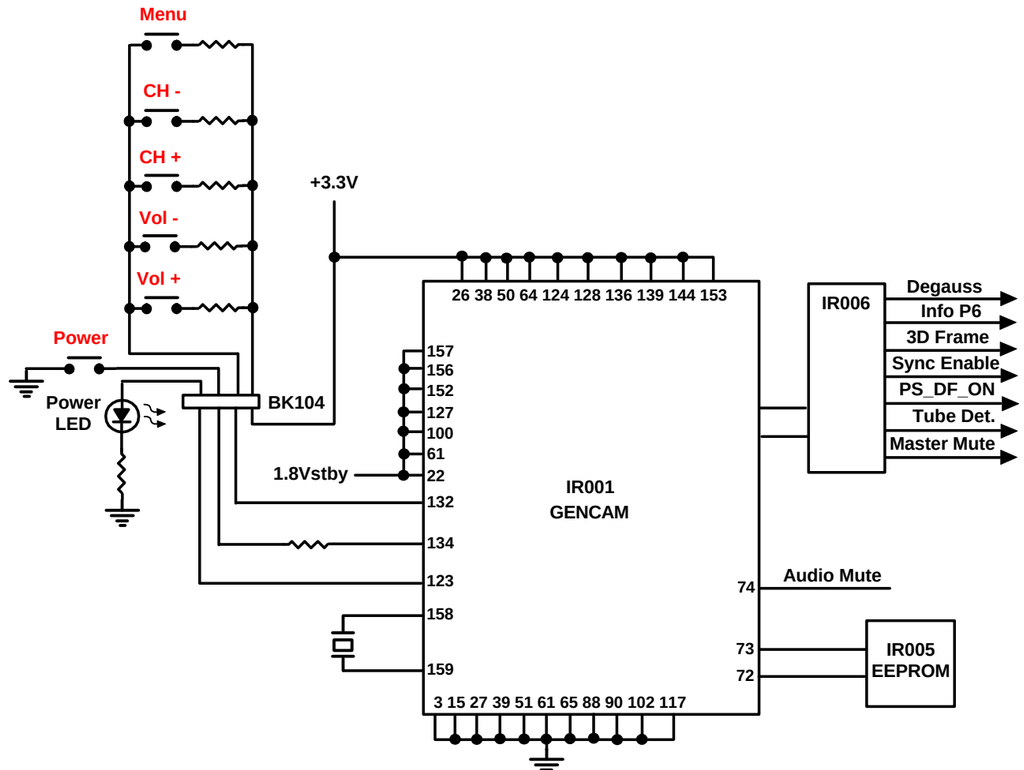
The GenCAM IC (IR001) is a fully integrated TV microcontroller and Electronic Program Guide (EPG) processor. It includes a 32-bit RISC processor core, bit mapped On Screen Display (OSD), Tele-text data slicer, 1x/2x Closed Caption data slicer, and TV control system. IR001s main functions are to act as a television controller and process Tele-text data, Closed Caption data, and EPG data.

IR001 controls the whole ITC222 chassis via four I²C buses and a few port lines. The I²C bus lines are labeled IIC Bus_1 through IIC Bus_4 and each bus line has any were from three to 12 devices to control.

Reset for IR001 comes from IR040. When the main power supply is switched ON, a RESET is generated with IR040. During RESET all GPIOs are in high impedance. After RESET, the system will configure the SDRAM and set all ports to a default state.

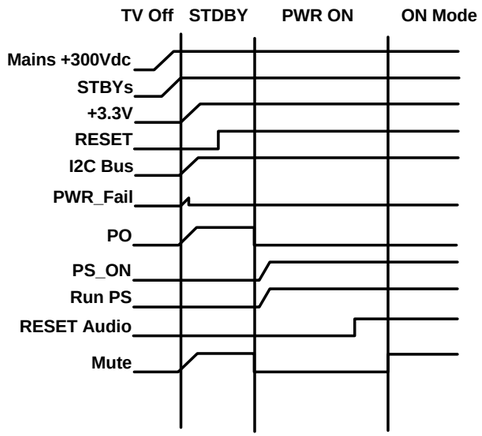
The Power LED is a single LED that is only illuminated during ON-mode. It is controlled by Software from pin 123 of IR001.

User interface is via a keyboard with six buttons and IR signal. The keyboard is configured as a voltage ladder with single input to IR001 at pin 132. The power switch is detected with a separate input at pin 134. IR001 reacts to commands from the remote control in the standard RCA infrared format. Also on the keyboard is the power LED.

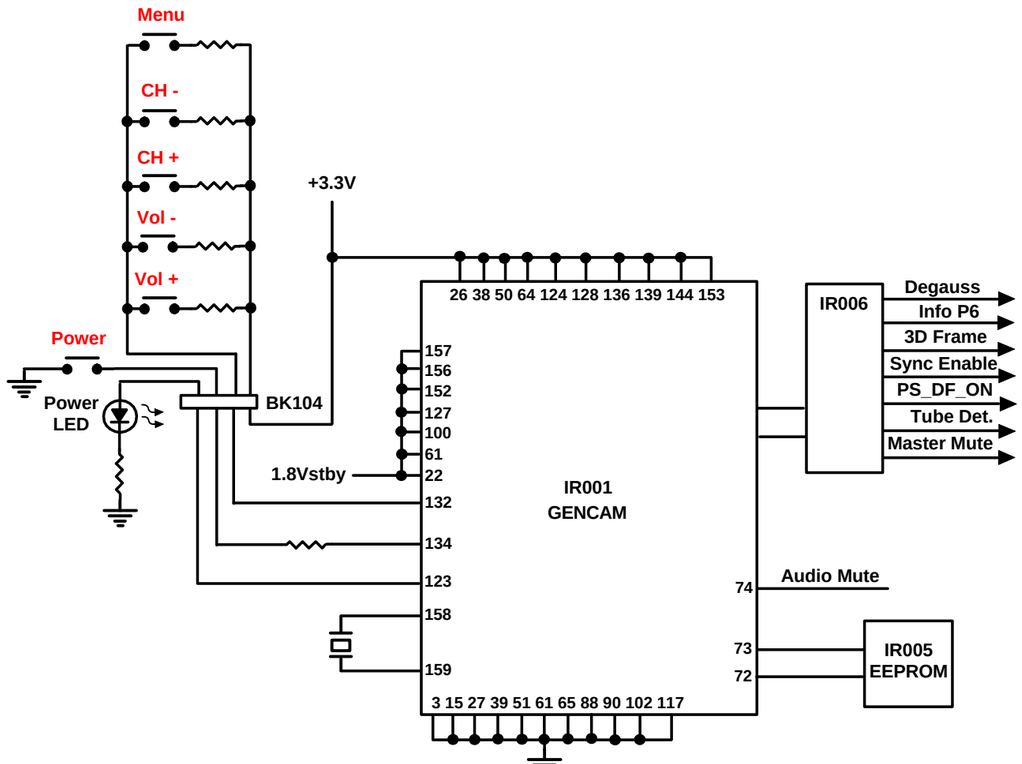


GemCam Block

Accompanying IR001 in its roll as system control are: IR005 (EEPROM), IR006 (Bus Expander), IR110 (SDRAM), and IR130 (ROM). IR110 and IR130 store the software needed by IR001 to control the ITC222 while IR005 stores setup features and user information. The bus expander, IR006, is used to control analog functions like master mute, degauss, 3D frame, PS_DF_ON (Convergence power supply turn on) etc..



Power ON Timing



GemCam Block

ECO mode for Standby power supply

- The Standby power supply is operating at Low Power Mode (17KHz), because the ECO_STANDBY port is set to "high".
- A total of around 200mA are available (but only an average of 35mA are used.)
- In ECO mode only the standby voltages (+6V_STBY, +3,3V_STBY and +1,8V_UP) are available. Therefore, only the **µC, ROM, SDRAM**, **IR** and **Keyboard** modules receive power.
- The GenCAM is set to low-power.
- To make the µC use as little power as possible, only the micro timer cell, the I/O ports and the A/D converter are enabled; all other internal peripherals are disabled.
- The frequency of the CPU clock is **16MHz**.
- Software is executed from external ROM and external SDRAM.
- Operating system is installed and running.
- Only the TECI address at I2C_bus1 is supported. All other I2C busses aren't supported.
- Chipper Check address at I2C_bus_1 is supported during ECO-mode.
- Both LEDs (Power-LED and TOPLIGHT-LED) are dark.
- The µC is waiting for an IR command, a Keyboard action, or Timer function. If a valid signal is detected, the system will start the power on sequence, otherwise the µC will stay in ECO mode.

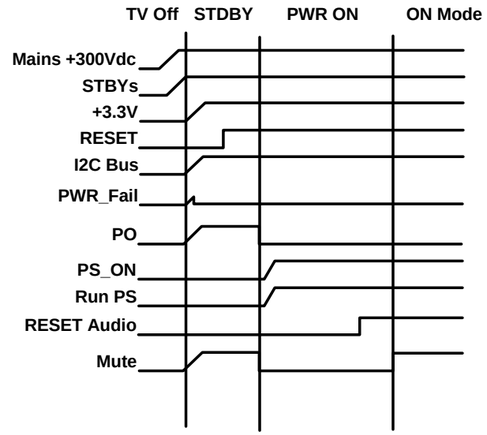
To make the µC use as little power as possible, only the micro timer cell, the I/O ports and the A/D converter are enabled; all other internal peripherals are disabled. The frequency of the CPU clock is **16MHz**. Software is executed from external ROM and external SDRAM. Operating system is installed and running. Only the TECI address at I2C_bus1 is supported. All other I2C busses are not supported. The LED is dark. The µC is waiting for an IR command, a Keyboard action or Timer information by monitoring the corresponding ports and cells. If a valid signal is detected, the µC will start the power on sequence, otherwise the µC will stay in ECO mode.

At AC power up the standby supply always starts in ECO mode and switches directly to Standby mode. Whether it switches back to ECO mode or switches ON is determined by the µC. This depends on the previous state of the set at AC power OFF, or if a valid switch ON command is detected either by IR or Keyboard.

STANDBY mode (this is only a temporary mode)
In the Standby mode, the main power supply is OFF and the Standby power supply is operating at a frequency of 28KHz. A total of 500mA are available from the Standby power supply. The µC, ROM, SDRAM, NVM, Port-Expander, IR and Keyboard have voltage supplied to them and are fully operational. The internal CPU clock is set to **72Mhz**. Software is executed from external ROM and external SDRAM. All IIC buses are enabled. Software has full control over all ports. Tuner, Video, Audio ICs, … are disabled and consume no power. The LED is still dark.

In STANDBY-mode, the µC, ROM, SDRAM, NVM and Port-Expander has voltage supplied to it.
If the µC switches from ECO mode to Standby or ON mode, the ECO_STANDBY line will be switched low. The Power supply will then be able to deliver around 500mA.

Note:
The **STANDBY** mode is only a temporary mode that is used for a short time while switching from ECO to ON or from ON to ECO mode. The system will never stay in the STANDBY mode.



Power ON Timing

ON-mode

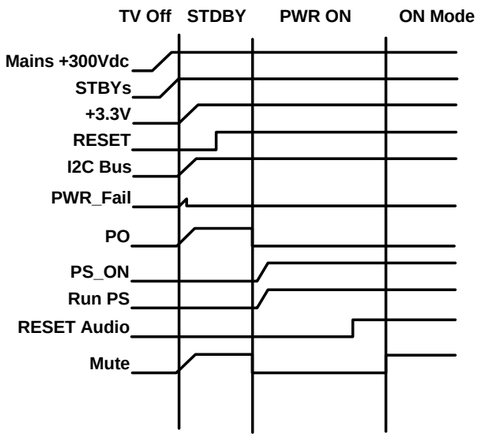
- Main power supply is ON, and Standby power supply is working at full capacity (28KHz, 500mA max)
- The internal CPU clock is set to **72MHz**.
- Software is executed from external **SDRAM** and external ROM.
- Operating system is installed and running.
- All devices are supplied with power and initialized.
- Deflection is active and audio is working normally.
- Also the Convergence Power Supply is switched on (PTV).
- Tuner, Video and Sound are enabled and operating.
- Both LED's (Power-LED and TOPLIGHT-LED) are illuminated, where the TOPLIGHT-LED is illuminated with "customer level".

The +5V_ON / +8V_ON will be switched on/off by the PO of the µC (pin115).
Also the deflection will be switched on via I2C bus_2. 100ms after deflection is switched ON, the power supply regulation is switched from Acquisition - to ON mode regulation (AQR_ON = low).

Power ON Sequence Summary
AC Power

MID comes on line producing the Mains +300Vdc for the standby and run supplies.
Standby comes up and goes from ECO mode to Standby and back to ECO awaiting IR001 command. With the 3.3V now active IR040 resets IR001. After IR001 is reset, Power Fail is checked and IIC bus is active. At this point IR001 awaits user input.

When the power on command is given, IR001 takes the Standby supply out of ECO mode to full power mode, mutes the audio, and turns on the Run supply. Deflection comes on line next and the audio is reset. After deflection is up and running, audio is un-muted and sound and picture are present.



Power ON Timing

Audio General description:
The audio circuit is located on the small signal board and includes the following components:

- **MSP (IA001):** Demodulation of the Sound IF signal for the BTSC standard, identification of mono, stereo and SAP, switching of 4 AV inputs and outputs for monitor out (fixed level), monitor out (variable level), headphones, subwoofer and L/R channels, Virtual SRS TruSurround XT processing.
- **TDA7269 (IA002):** Power amplifier for the left and right speaker signal.
- **TDA7298 (IA400):** Power amplifier for an optional subwoofer.
- **TEA6422D (IA900):** Audio matrix switch for additional inputs such as component inputs or an internal DVD or HDD module.
- **TS482D (IA003):** Stereo headphone amplifier.
- **IA180 and IA181:** Buffers for the variable monitor outputs (left, right, subwoofer).

Multi-standard Sound Processor: IA001
The **M**ulti-standard **S**ound **P**rocessor (**IA001**) contains the full TV sound processing. The MSP demodulates the BTSC multiplex signal and the SAP channel. The sound IF input (Pin 50) needs no pre filtering. After the Automatic Gain Control (AGC) the signals are A/D converted. The demodulation is done in digital form. The four stereo AV inputs (AV1, AV2, FAV, DRI) and the FM/AM input contain pre volume settings to compensate for level differences.

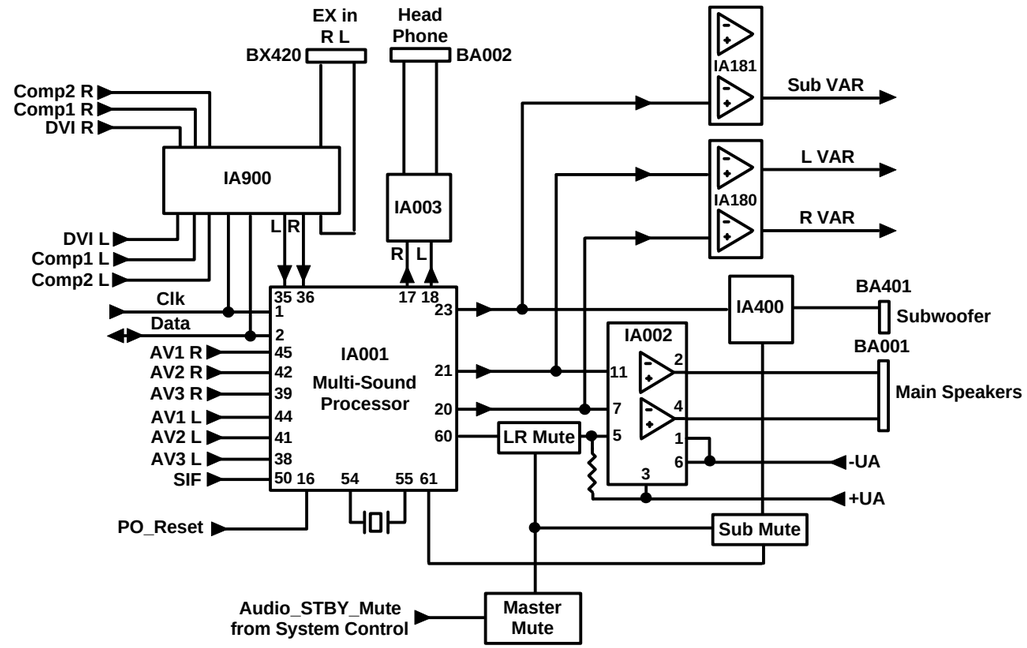
In the switching section, every input can be switched to every output. The speaker output path (Pins 20, 21) is used to carry the left and right channels to the variable monitor outputs and to the internal power amplifier IA002.
In this path the MSP offers several software controlled sound features:

- Volume in the range of -114 to +12 dB
- Five band equalizer or bass/treble with a range of ±12dB
- Loudness from 0dB to +17dB
- Balance control
- Stereo base width enlargement and pseudo stereo effect
- Automatic volume limiter
- Low pass / high pass filtering for subwoofer usage
- SRS TruSurround XT processing

The fixed monitor output path (Pins 28, 29) provides a fixed level output to an external amplifier.

The headphone output (Pins 17, 18) is used to supply the headphone amplifier (IA003). At this output, volume and bass/treble effects are available.

A subwoofer output (Pin 23) is also available with level and frequency response adjustments.



Audio Block

For the internal oscillator the MSP needs an external 18.432MHz crystal at pins 54 and 55.

There are two digital output pins 60 and 61 that are used to generate the Subwoofer and L/R mute. These are user- controlled functions from the audio menu.

The Power-On-Reset (Pin 16) is controlled by the microprocessor with a signal called RESET_AUDIO.

All functions are I²C bus controlled (Pins 1, 2).

Power amplifier: IA002
The stereo power amplifier IA002 receives the left and right signals from the MSP at pins 11 and 7. It delivers the amplified signal to the connector BA001and then to the speakers. IA002 runs with a symmetrical power supply (±UA). It includes two class AB amplifiers and a mute circuit.

Mute is activated if the voltage difference between pins 3 and 5 of IA002 is lower than 6V. Mute is deactivated if the difference between these pins is higher than 6V.

The power amplifier has an internal thermal shutdown and short circuit protection.

Headphone amplifier: IA003
The headphone amplifier IA003 is a TS482. It amplifies the signals coming from IA001-17,18 and delivers the signal to BA002.

Subwoofer amplifier: IA400
The subwoofer amplifier IA400 is a TDA7298. It amplifies the signals coming from IA001-23 and delivers the signal to BA401.

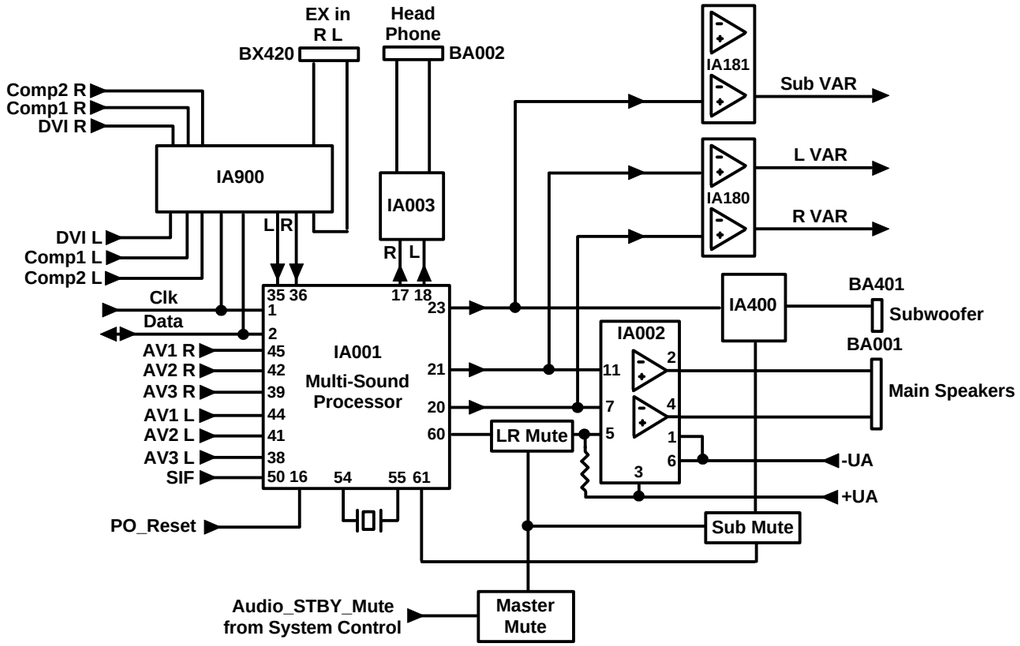
Audio Matrix: IA900
The audio matrix IA900 is a TEA6422D. It has 6 stereo inputs and 3 stereo outputs. It is also used to route additional inputs such as components, DVI or HDD/DVD to IA001.

Mute control:
There are four different mute signals:

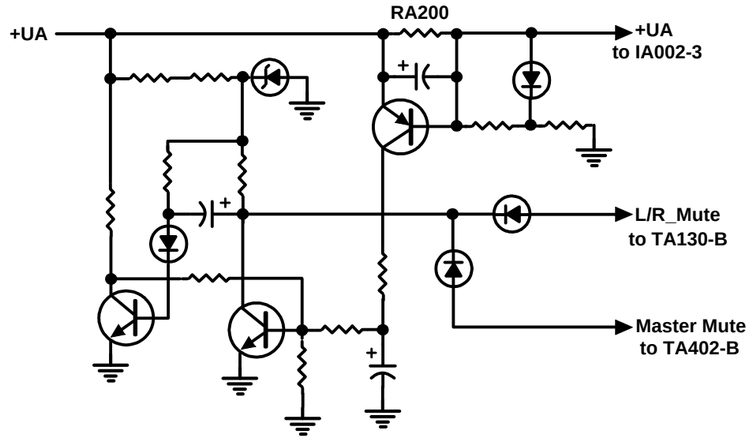
1. **MASTER_MUTE:** This signal comes either from the bus expander (IR006) or from the power fail circuit. It mutes the L/R amplifiers and the subwoofer amplifier. If the main voltage disappears, this mute is active as soon as possible in order to avoid pops.
2. **L/R_Mute:** Comes from IA001 and mutes the L/R amplifier. It will be active, if the user has selected “external amplifier Left/Right”.
3. **Mute_sub.:** Comes from IA001 and mutes the subwoofer amplifier. It will be active if the user has selected “external subwoofer”.
4. **AUDIO_STBY_MUTE:** This info comes from the microprocessor. It sets the L/R amplifier and the MASTER_MUTE into standby mode.

Safety Circuits:
To avoid failures caused by a defective speaker or speakers, there is an over-current detection circuit. The power supply current of the main amplifier is monitored. If the current through resistor RA200 increases, the power amplifier will mute. It will un-mute after several seconds if the current has decreased.

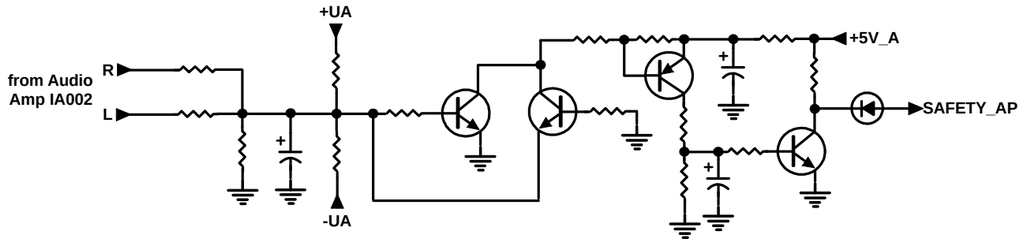
To protect the speakers from DC, the outputs are monitored. If DC is present on the outputs, the detection circuit pulls down the SAFETY_AP line which forces the power supply to switch off and the main processor will try to restart.



Audio Block



Over Current Detect Block



DC Detect Block

Video Signal Processing Path
The ITC222's video signal processing can be divided into two signal paths, NTSC video and component video. The NTSC signal path uses video switch IX300 and frame comb filter IC040 while the component video is switched using IX400. Outputs from both IX300 and IX400 are sent to the up-converter IV100. The signal then is processed by IV300 (YUV to RGB processor) and IV400 before being sent to the CRT(s).

In the ITC222 chassis, 480i input signals with 15kHz (1H), 480p input signals with 32kHz (2H) and 1080i input signals with 33.7 kHz (2.14H) can be processed.

IX300 Matrix Switch
The ITC222 chassis provides two rear inputs either CVBS or S-VHS and one front CVBS or one front S-VHS. The input signal selection is done by video matrix IX300. It has 8 inputs: AV1-3 Y/CVBS and Chroma, Monitor and Main-tuner. And it has 6 outputs: Y/CVBS master and slave, Chroma master and slave, monitor output and FRAME_OUT.

IC040 Frame comb filter (PTV only)
For projection TV a frame comb filter function must be provided. This is done with integrated frame comb filter IC040. The NTSC-CVBS input signal is input to IC040. It must be filtered (TC061, TC063 and TC065) and is AC coupled to AYI input pin 88 of IC040. On the other hand an external sync separator must be derived from the CVBS input signal. This is done with TC040, TC051, TC055 and TC056 and input at pin 76 of IC040. After the signal is separated inside IC040, the Y signal is post filtered with TC100, TC105 and TC107 and the C signal is post filtered with TC120, TC125 and TC127. These signals (Y_FRAME and C_FRAME) are then transmitted to IV100 pin 55 and 56.

IX400 Component Video Switch
There are four inputs to IX400 that are selected by INPUT_SEL (I²C bus). These inputs are: COMPONENT INPUT 1 and 2, DVI-input, and RGB_GRID from the convergence circuit. RGB_GRID is used for rear projection alignment.

The DVI signals are sent to IT600 before being sent to IX400 as YPrPb. IT600 is a DVI receiver / processor with YPrPb outputs.

The signals are output from IX400 SEL_OUT (Pins 22 H_OUT, 23 V_OUT, 25 CR_OUT, 26 CB_OUT and 27 Y_OUT). IX400 is able to convert YPrPb signals and RGB signals to YCrCb by an integrated matrix.

IT600 DVI

The DVI is a digital RGB/HV interface. It consists of the integrated DVI-decoder IC IT600 and an EEPROM (IC620), in which the standards are stored, that can be displayed by the ITC222. These are:
640 x 480p
720 x 480p
1920 x 1080i

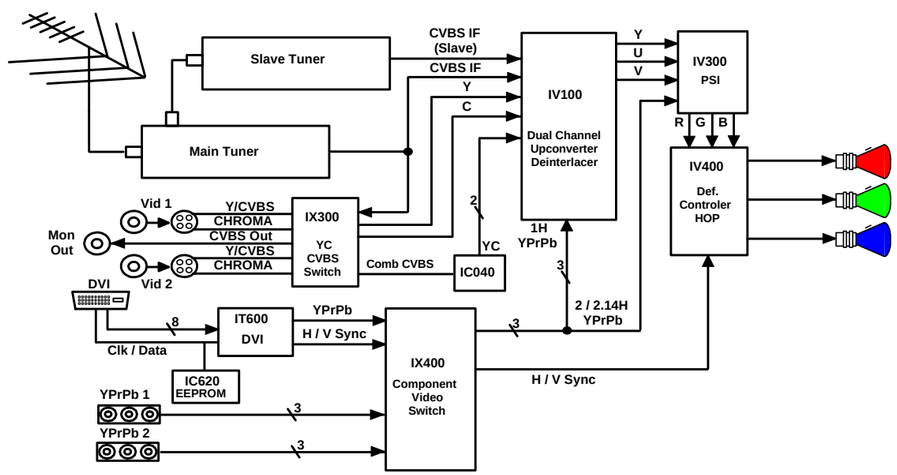
When a valid standard is recognized, the DVI_DETECT signal (BT600, pin2) goes high so that IR001 is informed. The DVI has no I²C-bus connection to IR001. For more detailed information about DVI please refer to "Digital Visual Interface Rev 1.0" from DDWG http://www.ddwg.org/ or "EIA/CEA-861".

IV100 Up-Converter De-Interlacer
Sync Processing
The sync processing is mainly performed by IV100. There can be two different types of sync: Either H- and V-syncs coming from IX400 V_EXT and AV2_FB/H, or sync on the Y- for composite signals from IX300.

IX400 input supports both positive and negative H/V sync signals. Existence distinction is first performed to determine whether the selected sync signals are input from H and V, and these results are sent as the existence status to the EV and EH status registers. On the other hand, polarity-matched H and V that passed through the polarity identification circuit are input to the priority ranking circuit. When inputting Sync on Y-input, it passes the sync select switch and then the signal is amplified by 6dB and output to YG_OUT (Pin 15). This output is returned to YG_IN (Pin 16).

The H and V sync signals selected by the HV sync signal-processing block are sent to the SYNC counter block. The SYNC counter block counts the frequency of the input H and V sync signals and counts the H sync signal input during a certain period (~5ms). This time is based on the clock obtained by the internal VCO from the 4MHz ceramic oscillator QX471 connected to EXTCLK/XTAL (Pin 20).

For the V sync signal, the number of reference clock (31.25kHz) pulses during 1 V cycle is counted. The H-sync signals coming out of IX400 must be improved with an integrated dual mono-flop 74HC123 (IX420). This is necessary to suppress disturbing H-pulses in the middle of a line during vertical blanking start/stop and to achieve rise times <100ns so that the sync processor can run without phase disturbances.



Video Block

The second mono-flop inside IX420 inhibits an additional H-pulse for about 23.5us. During HDTV V-sync, the H-sync pulse coming from IX400 is interrupted (due to original tri-level sync form) and wrongly triggers the mono-flop. To avoid this, an additional OR-gate is necessary (IX430-74HC1G32). With this additional OR-gate, the mono-flop cannot be triggered if one or both input signals are high. After that, the sync signals are given to sync processor IV100.

2H Post Filter
The 2H post filters are used to suppress all unwanted frequency components beyond the useful frequency range after the up conversion process. The Y path includes a group delay correction circuit to fine-tune the overall group delay performance. In order to adapt the signal levels coming from the up converter additional amplifiers are added for all three paths.

ADM1 Circuit

The ADM1 circuit has an ATSC (HD) tuner to allow tuning of terrestrial HD signals. ATSC signals are processed by the ADM1, but NTSC tuning is not supported. The autoprogramming list for ATSC channels is held on an EEprom located on the ADM1 board.
Due to the mixture of BGA's (ball grid array) and multi-pin "flat pack" IC's, the ADM1 module is warranty replaceable only.

ADM1 Troubleshooting

For troubleshooting, the video (2H) and audio (analog) signals are sent to the Small Signal Board through connector BX420. The pin outputs are as follows:

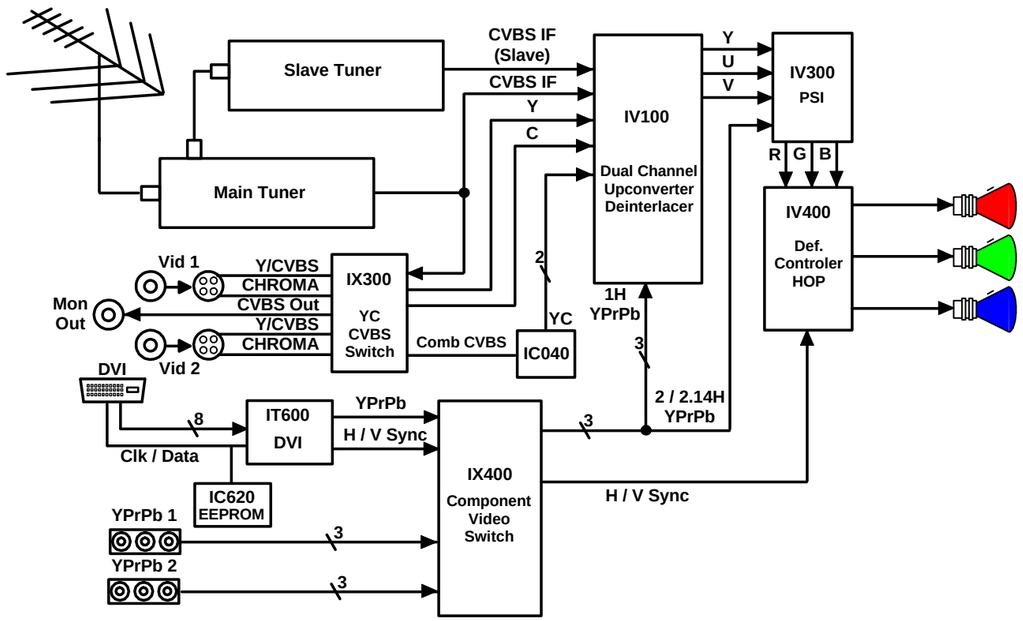
Pin 1 - Left Audio
Pin 3 - Right audio
Pin 9 - Deint_PR
Pin 11 - Deint_Y
Pin 13 - Deint_PB

The audio processing can be Mono or AC3 stereo. In the video circuit, the ADM1 has "automatic lip sync delay compensation" and the signal can be composite, component, or Y/C. The aspect ratio's are 4:3 and 16:9.

The ADM1 module supports the following signals: 480i, 480p, 720p, and 1080i.

The power is supplied from the Power/Deflection board through connector BP120. The pinouts are as follows:

Pin 1 - 20vdc 2 amps fuse FP403
Pin2/3 - Gnd
Pin 4 - 6vdc 2 amps fuse FP402
Pin 5 - 10vdc 2 amps fuse FP401



Video Block

IV300 YUV to RGB Matrix
The output format of IV100 is YUV, whereas the video processor IV400 requires a RGB signal. Therefore IV300 converts YUV to RGB and is output at pins 12, 13 & 14 to pins 30, 31 and 32 of IV400.

PSI (Picture Signal Improvement)
Picture Signal Improvement (PSI) and video user controls are performed inside IV300. The input signals are taken from the post filter outputs. All enhanced output signals are fed directly to the video processor IV400.

Input to the PSI processor is either an up-converted 1h signal (CVBS, Y/C or Component 1H) or a 2h/2.14h signal from the component or DVI inputs.

All enhanced output signals are weighted by external voltage dividers to adapt the three colors to the picture tube (tubes) needs (DV or PTV) and then fed to IV400.

Black Stretch
For video signals with a black level that deviates from the back-porch blanking level the signal is 'stretched' to the blanking level. The black level is detected by means of an internal capacitor. Black stretch is performed inside the PSI (IV300).

Sharpness
The Sharpness function is a combination of the peaking, Y-detail control, super-real-transient and color detail enhancement function of IV300 and the vertical peaking function of IV100. Depending on the users "Sharpness" setting, a predefined value for the peaking control and the steepness control is selected. Due to the smart sharpness controller function large input signals are more enhanced by IV300 while small input signals are enhanced by the vertical peaking function of IV100.

Contrast expand
The contrast expand function a combination of the static gamma, dynamic gamma and black stretch function. Depending on the "contrast setting", three different values are selected.

Green enhancement
Green enhancement is used to increase the saturation of low saturated green colors. This function is always on.

Tone Correction (Color Warmth)
The tone (color warmth) control adds and subtracts fixed offset values to the RGB output gain values to create different color tones called "warm, "neutral" and "cold"

CTI
Color Transient Improvement (called color SRT transient) is always on.

IV400 Deflection Controller Video Processor
Additional video processing is performed inside the High-level Output Processor (HOP) IV400. Only a few external components are necessary to support the internal functions.

Saturation control
Saturation control is valid for the YUV and 2H/2.14H RGB inputs. The OSD/Text - RGB input is **not** affected.

Contrast control
Contrast control is valid for the YUV and 2H/2.14H RGB inputs. The OSD/Text - RGB input is **not** affected.

RGB-TXT inputs
These inputs are used for OSD/Text signals. The nominal input amplitude for the OSD is 710mVpp.

Brightness control
Brightness control is valid for the YUV, OSD/Text and RGB inputs.

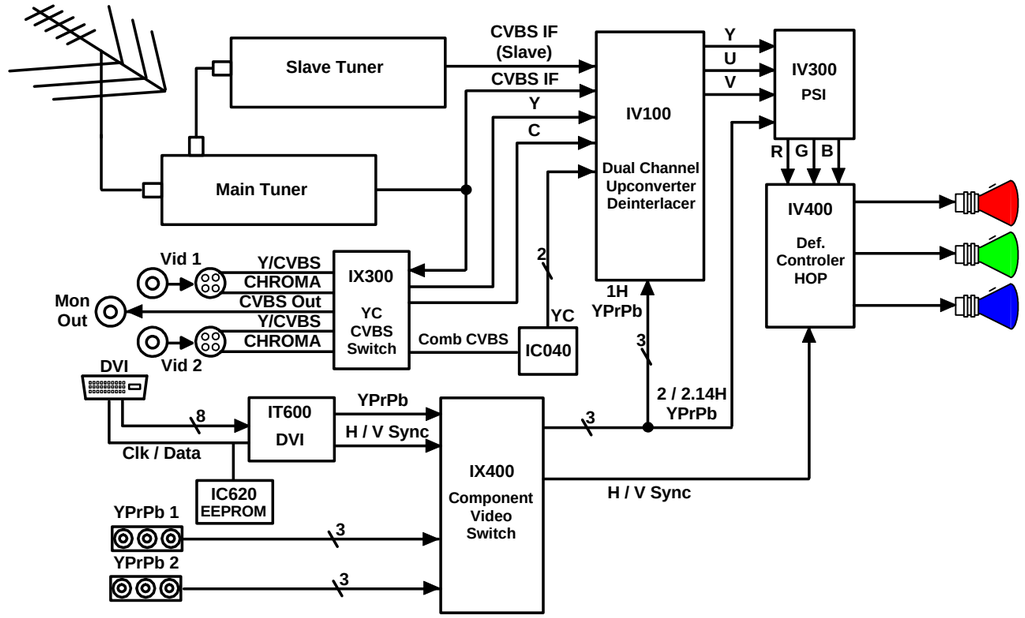
Beam current limiter
To avoid stress to the Picture tube, it is necessary to limit the average beam current to a specific value. This value is dependent on the tube size and tube type. To limit the average beam current, the contrast and brightness inside the video processor IV400 is reduced depending on the voltage at pin 43 (BCL).

NOTE: The beam current information is derived from the low end of the high voltage transformer.

The higher the beam current, the lower the voltage at DV471. The maximum voltage is limited by the zener diode DV470 to stay close to the BCL threshold if the beam current is low. DV471 is used to separate the slow time constant for the average signal and the fast time constant for the current transitions. With CV472 being discharged, the picture contrast and the brightness are gradually reduced. With the beam current receding and the voltage on CV470 rising, CV472 can again charge to its original voltage. The decay time is given by RV471 and CV472.

Transistor TV477 uses the PKS (Peak Sense) information to reduce the contrast instantly if a critical current jump occurs. This threshold is fixed by the reverse breakdown voltage of DV476. Resistors RV477/RV478 limit the minimum emitter voltage of TV277 to ~2.0 V, enough to sufficiently reduce the beam current of a full white picture in a worst-case situation.

Peak white limiter
The control circuit contains a Peak White Limiting (PWL) circuit and a soft clipper. The detection level of the PWL is adjustable via



Video Block

the I²C-bus and has a control range between 0.65 and 1.0 VBW (this amplitude is related to the Y input signal with typical amplitude 1 VBW) at maximum contrast setting. The output signal of the PWL detector is filtered by means of an external capacitor CV479 so that the high frequency components of the video signal will not activate the limiting action. The contrast reduction of the PWL is obtained by discharging the capacitor of the beam current limiting input. In addition to the PWL circuit the IC contains a soft clipper function that limits the high frequency signals when they exceed the peak white limiting level. The difference between the peak white limiting level and the soft clipping level is adjustable via the I²C-bus and can be varied between 0 and 10% in 3 steps (soft clipping level equal or higher than the PWL level). It is also possible to switch-off the soft clipping function.

Continuous Cathode Calibration

To maintain an accurate biasing of the picture tube a “Continuous Cathode Calibration” circuit has been developed. This function is accomplished by means of a 2-point black level stabilization circuit. By inserting two test levels for each gun and comparing the resulting cathode currents with two different reference currents, the influence of the picture tube parameters, the spread in cut-off voltage can be eliminated. This 2-point stabilization is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages.

An additional advantage of the 2-point measurement is that the control system makes the absolute value of Ik1 and Ik2 identical to the internal reference currents. Because this adjustment is obtained by means of an adaptation of the gain of the RGB control stage this control stabilizes the gain of the complete channel (RGB output stage and cathode characteristic). As a result variations in the gain figures during life will be compensated by this 2-point loop. An important property of the 2-point stabilization is that the off set as well as the gain of the RGB path is adjusted by the feedback loop.

ITC222
CIRCUIT OVERVIEW

Hence the maximum drive voltage for the cathode is fixed by the relationship between the test pulses, the reference current, and the relative gain setting of the 3 channels. This has the consequence that the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels the typical “cathode drive level” amplitude can be adjusted by means of an I2C-bus setting.

Dependent on the chosen cathode drive level the typical gain of the RGB output stages can be fixed taking into account the drive capability of the RGB outputs (pins 40, 41 and 42). The measurement of the “high” and the “low” current of the 2-point stabilization circuit is carried out in two consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100µA. When the TV receiver is switched-on the black current stabilization circuit is directly activated and the RGB outputs are blanked. The blanking is switched-off as soon as the loop has stabilized. This ensures that the switch-on time is reduced to a minimum and is dependent on the warm-up time of the picture tube.

RGB output filters

The three passive RGB output filters are used to eliminate high frequency distortions (mainly from RGB-TEXT/OSD insertions) before they are radiated from the connection cable to the CRT board. The filter outputs are buffered by NPN, emitter followers to keep the signals to the CRT board at low impedance and to shift the DC range of the RGB outputs down by one UBE. This shift is necessary since the high voltage video amplifiers on the CRT board do not allow any adaptation of the output DC range.

DVD Power Supply

Basic Operation

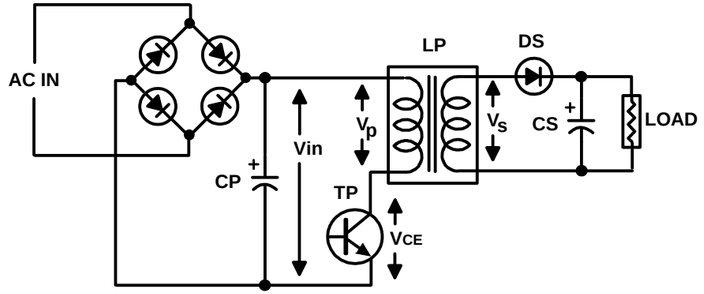
The power transistor TP operates as a switch, which is alternately closed (i.e. TP conducts in a saturated state) and opened (i.e. TP is off). The secondary winding of the transformer LP is phased so that DS is reverse biased, when transistor TP is closed.

When TP conducts, current flows across the primary winding of LP and DS is non-conducting. Current rises linearly in the primary winding until TP is switched off. When TP turns off, the current falls rapidly to zero. The energy stored in the primary inductance of LP makes the voltage across the primary and secondary windings reverse in polarity. These reverse voltages increase rapidly until the voltage across the secondary winding exceeds the voltage across the output capacitor CS. DP starts to conduct and transfer the energy that was stored in the primary inductance to the output capacitor CS and the LOAD.

When the energy transfer is finished, the voltages Vp and Vs quickly fall to zero and the voltage $V_{CE} = V_{in}$. They remain at these respective values for the remainder of the period. The diode DS is off. After a "dead" time, the power transistor TP switches on again and cycle repeats.

During the dead time and the conduction period of the power transistor, the load is supplied only by energy stored in the output capacitor CS that holds the output voltage constant over every cycle.

The term "discontinuous mode" refers to the current flowing through the primary inductance goes to zero before the start of the next cycle.



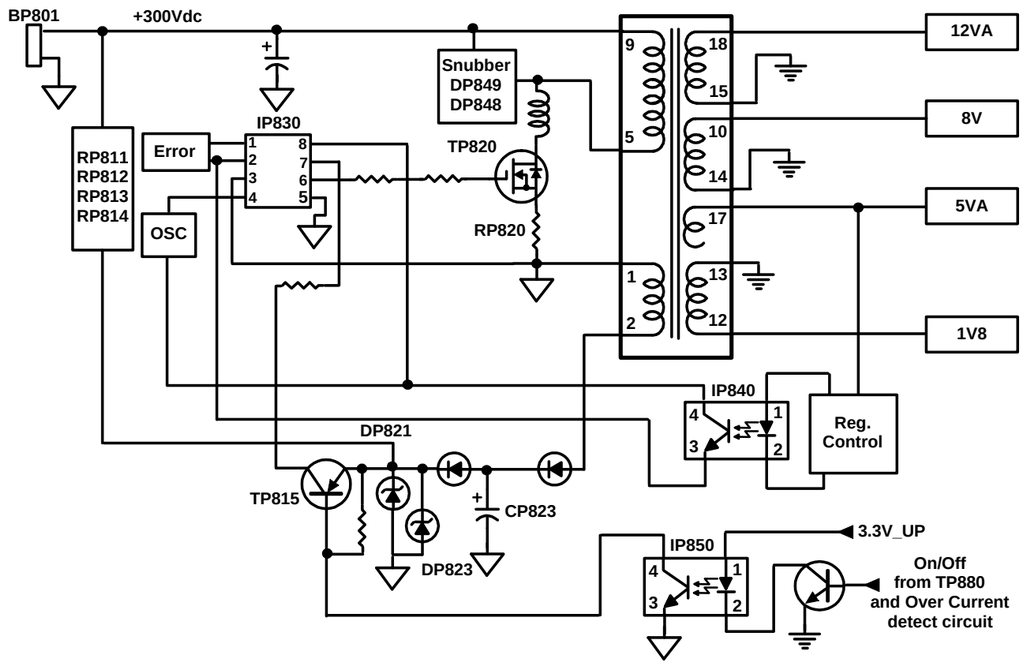
DVD Power Supply Operation

At mains plug in, the +300VDC charges CP823 via RP811, RP812, RP813, and RP814. The charge is limited by DP821 and DP823 zener diodes. CP823 is needed for the start up voltage that IP830 requires.

To switch ON the DVD power supply, a low level is generated by the chassis microprocessor to the DC_DC_ON signal. The transistor TP880 is switched OFF allowing the 3.3V_UP voltage to turn on TP881. The LED of IP850 turns on emitting light to the phototransistor connected to pins 3 and 4 of IP850 turning on the phototransistor. This turns on TP815 providing the VCC to IP830 pin 7 from CP823. Now the primary control (IP830) can drive the gate of TP820 and the SMPS will start from **OFF** to **ON** mode.

Switch ON phase (TP820)

When the rising edge of the output pulse from pin 6 of the IP830 switches the transistor TP820 on, the voltage across the transistor is almost zero. The capacitor CP821 and CP820 are discharged during switch on.



Conduction phase (TP820)

With TP820 now conducting, the current through the primary winding of LP850, and hence through the transistor's drain, rises linearly with the time.

Switch OFF phase (TP820)

When the power transistor switches off the current through the drain is abruptly cut off. At this time there is a large current flowing trough the primary winding of LP850. This causes the voltage across the primary and the IC, to rise rapidly. The snubber network limits this voltage.

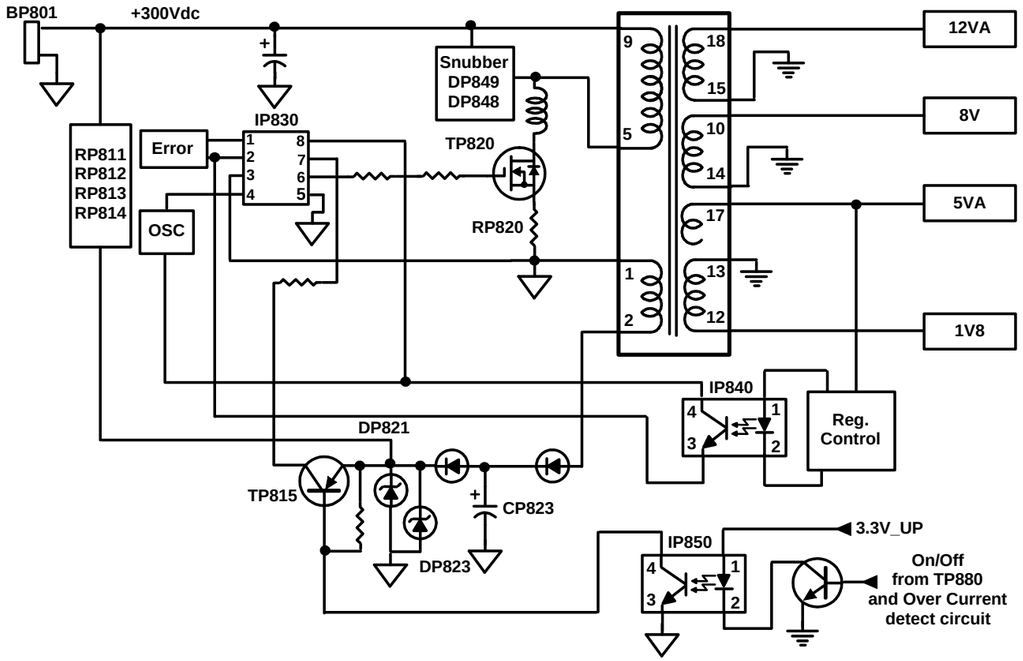
The Off time is separated into two parts: the energy transfer phase and the dead time.

Energy transfer phase

Immediately after the power transistor switches off, the energy transfer to the secondary starts. The output voltages of the SMT (LP850) become positive, the secondary diodes conduct and the magnetic energy that is stored in the SMT is transmitted to the secondary.

Dead time

After the energy transfer is complete, there is a dead time, which lasts until the next conduction pulse occurs. During this time, IP820 and the secondary diode DP863 are off and so there is no current in LP850. The voltages are oscillating with the winding inductance, the winding capacitance and snubber capacitance.



Protection

Primary protection
On the primary side there is a current limitation from cycle to cycle, which means that the maximum transferable power is limited and all secondary voltages will drop down if this limit is reached. The resistors RP836/RP835 attenuate the voltage of RP820 to provide voltage proportional to the drain current and used for the current sense input pin 3 of IP830. The capacitor CP835 in conjunction with resistor RP836 acting as filter against voltage spikes. If the voltage at RP820 becomes high enough the PWM of IP830 will stop thus terminating the output switch conduction. The typical input signal is 1.0V.

Over Voltage Protection

Primary: If there is a failure of the regulation all voltages increase. If the primary voltage VCC goes higher than 50%, the zeners DP821//DP823 will conduct and short out. IP830 is not supplied and the gate of TP820 isn't driven. The SMPS will be stopped.

Secondary: If the regulation voltage 5VA is higher than 20%, the transistor TP882 will turn ON turning off TP881 (no base voltage). The Opt coupler IP850 doesn't transmit information thus the transistor TP815 will be switched off and the VCC doesn't supply IP830. The power supply will switch off.

The protection circuit contains 2 functions:
- **SWITCH ON-OFF PSDVD**
- **SHORT CIRCUIT PROTECTION**

SWITCHING ON THE PSDVD:
To switch on the PSDVD we need a low from the DC_DC_ON. The transistor TP880 will switch off, the capacitor CP880 will charge during a certain time about 200ms.

During this time the transistor TP881 is switch on and remain on if the output voltages are present (power supply starts up).

SWITCHING OFF THE PSDVD:
To switch off the PSDVD we need a high from the DC_DC_ON signal (this level should be about 3.3v from the µP). The transistor TP880 will switch on, the capacitor CP880 will discharge from –3.3v to 0v. TP881 will switch off and all output voltage will switch off.

SHORT CIRCUIT:
In On mode all the voltages are present; the 1.8V is adjusted to 1.9V due to the lengths of the cable, so we have at the anode of DP855 a voltage of 2.23V,and on the base of TP881 a voltage of 0.6V.The two diodes DP856 and DP857 avoid the linearity of the transistor TP881 when the 1.8V go down. Similar for the 3.3V with the diode DP858 and DP859. The behavior of this circuit is the same for the other voltages. The 12V supply is the master to apply 0.6V on the base of TP881. All diodes DP851, DP852, DP853, DP854 and DP855 avoid mixing current/voltage of each line. After anomaly, the DVD will try to start 3 times then the DVD-KEY on remote control will be disabled.