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Abbrevations & Acronyms

480_on	Switching signal for 480P & up-converted 480i mode
ABL	Average Beam Current Limiting
ACQ	Acquisition power mode
ADB	Adaptor Board, PTV
APR_ON	uP signal to switch between 6V & USYS regulation
AQR_ON	Signal from uP to switch from 6V regulation to USYS regulation
BCL	Beam Current Limiter
Breathing	
BSVM	Beam Scan Velocity Modulation
CAB	Convergence Amplifier Board
CBA	Circuit Board Assembly
CCC	Continuous Cathode Calibration
CSB	Convergence Signal Board
CTI	Color Transient Improvement
CVBS	Composite Video Baseband Signal
DCR (R,G,B)	Dark Current Signal (cathode cutoff)
DCU	Digital Convergence Unit
DEGAUSS	Signal from uP to turn degaussing circuit on & off
DFB	Dynamic Focus Board
DP	Deflection Part
DRI	Digital Ready Interface
DST	Diode Split Transformer (IHVT)
DVI	Digital Visual Interface
ECO_ Standby	Signal from uP to switch stdby power supply modes
EFC	Earth Field Correction
EW	East West
H_DRIVE	Horizontal Drive Signal
HIP	Hi-Level Input Processor
HOP	Hi-Level Output Processor
IHVT	Integrated High Voltage Transformer
INF_POW_FAIL	signal from standby SMPS indicating loss of mains (120VAC)
LTI	Luminance Transient Improvement
MID	Mains Input Doubler (doubles Raw B+)
NVM	Non Volatile Memory or EEPROM
PA/SW	Power Amp Sub Woofer
PE	Protective Earth
PO	Power On signal from uP to start main SMPS
PP	Power Supply Part
PS_ON	signal derived from PO to start main SMPS, also controlled by safety circuits of the main SMPS
PS-ADB	PTV Power Supply/Adaptor Board (same as ADB)
PSB	Power and Scan Board
PSI	Picture Signal Improvement
PWM	Pulse Width Modulation
RP	Rear Projection

Abbrevations & Acronyms

SAFETY	**signal generated by safety circuit located on SPP CBA**
SMPS	**Switched Mode Power Supply**
SMT	**Switched Mode Transformer**
SPP	**Signal Power Part**
SSB	**Small Signal Board**
SSC	**Super Sandcastle Signal**
TFT	**True Flat Tube**
UP	**Micro-Processor**
USYS	**System voltage for the horz deflection or Reg B+**
XRP	**X-Ray Protect**

STANDBY POWER SUPPLY

Start Up

ECO Mode

When AC is connected the standby power supply starts in ECO mode. The chassis's microprocessor determines if it stays in ECO or goes to STANDBY and than to RUN. This depends on the previous state of the set at AC interruption or disconnection. The set will always come back to the last status before AC interruption.

When the AC is first connected, the integrated high voltage current source of IP020 provides a bias current from pin 3 to pin 2 during the start-up phase. As soon as the voltage on pin 2 reaches the threshold VDDON of IP020, the device turns into active mode and starts switching. The start up current generator is switched off, and the re-supply provides the needed current on the VDD pin 2 through the winding between pin 3 and 4 of LP020.
The oscillator at pin 1 starts working after VDDON at pin 2 is reached. It takes approx. 0.6s for the standby power supply to switch on after AC has been connected.

The oscillating frequency at pin 1 of IP020 is determined by the values of RP027 and CP027. The typical value of the oscillator frequency is approximately 28kHz in standby (mode just before run) and 17kHz in ECO mode. The first time that AC is connected the ECO_STANDBY IR001 pin 110 is high and TP150 is switched off. No current can flow from the opto coupler IP070 and the resistor RP029 to pin 1 of IP020.

STANDBY Mode

To switch from ECO mode to STANDBY (mode just before run), the ECO_STANDBY line will be switched to low turning on TP150 via 5V_STBY, resistor RP153 and RP152 to ground. This results in a switch on of TP150 and now current can flow from CP023 via the opto coupler IP070 and RP029 to pin 1 of IP020. This additional current results in a frequency shift and the standby SMPS is then running at approximately 28kHz.

The standby SMPS is synchronized to the main SMPS by differentiation of the auxiliary voltage at pin 5 of the SMT LP050 via CP030 and RP030. Only during the positive peak voltage current flows via the diode DP030 and the current limitation resistor RP032 to the oscillator input of IP020. To provide the desired transfer function of the regulation loop a compensation network CP026, RP024 and CP024 is connected to the COMP pin 5 of IP020 which is the output of the error amplifier and acts as soft start. In addition the transistor TP026 limits the output power. If the threshold of TP026 is reached, TP026 is switched on and the voltage on pin 5 of IP020 is below 0.5V causing shutdown of the power MOSFET of IP020. The capacitor CP031 in conjunction with resistors RP025 and RP026 define the time for TP026 to be active.

IP020 -One Complete Cycle in On Mode

Switch On Phase

When the internal driving circuit switches the power transistor of IP020 on, the voltage across the transistor is almost zero. This switches a large voltage across the capacitor CP021 of the snubber network and results in short charging current through the capacitor CP022 and CP021 and also through the drain of IP020. This explains the large drain current peak at the start of the conducting phase and is a source of power loss in the power transistor of IP020. The snubber network is described more in detail later on.

Conduction Phase

With IP020 now conducting, the drain current through the primary winding of LP020, and hence through the IC's drain, rises linearly with time.

Switch OFF Phase

When the power transistor of IP020 switches off the current through the drain is abruptly cut off. At this time there is a large current flowing through the primary winding of LP020. This causes the voltage across the primary and the IC to rise rapidly. In addition the power transistor's gate source voltage must be zero during switch off so that it can sustain a

high drain source voltage during this time. This is done internal of the IC IP020.

OFF Phase
The Off time must be separated into two parts: the energy transfer phase and the dead time.

Energy Transfer Phase
Immediately after the power transistor of IP020 switches off, the energy transfer to the secondary starts. The output voltages of the SMT LP020 become positive, the secondary diodes conduct and the magnetic energy that is stored in the SMT LP020 is transmitted to the secondary capacitors CP220 and CP240 with linear falling current of DP220 and DP240.

DEAD Time
After the energy transfer is complete, there is a dead time that lasts until the next conduction pulse occurs. During this time, IP020 and the secondary diodes are off and there is no current in the SMT LP020. The voltages are oscillating within the winding inductance, the winding capacitance and snubber capacitance.

MAIN POWER SUPPLY
Start Up of the Main-SMPS

Oscillator

During ECO or STANDBY the resistor RP177 charges CP171. When the upper threshold of the voltage comparator is reached, pin 1 of IP170 is switched to high and a current can flow via 5V_STBY, resistor RP170 into the base of TP170. The upper threshold of IP170 is determined by resistor RP173 and RP174. If the transistor TP170 is switched on, the capacitor CP171 will be discharged by DP171 and RP176.

The parallel resistance of RP174 and RP175 determines the lower threshold of IP170. By reaching this lower threshold, pin 1 of IP170 will be switched to low, transistor TP170 is switched off and capacitor CP171 will be charged. The oscillating frequency of the saw-tooth during ECO or STANDBY mode is approximately 2.5kHz.

PWM Circuit
The PWM circuit is active during ECO or STANDBY mode. The PWM pulse at pin 7 of IP170 is present but at a lower amplitude. The transistor TP161 is switched on in ECO and STANDBY keeping the main SMPS OFF.

The saw-tooth on pin 6 of IP170, which is generated by the oscillator, is compared with a DC voltage on pin 5. During ECO or STANDBY mode the frequency of the PWM pulse is 2.5kHz and shifted to 18kHz via the resistor RP225 during start up. An additional shift takes place when TP221 turns off because of the additional current that can flow from the 5V_STBY through the resistor RP222 and the diode DP222 that results in a decreased charge time of CP171. The frequency of approximately 28kHz will be synchronized to the horizontal deflection frequency (31.5KHz) via H_DRIVE after horizontal comes up. More details about the reason for frequency shift during start up can be found in the **Primary Control Circuit** section.

STANDBY to ACQUISITION Mode

When the SMPS is in ACQUISITION mode, which means the deflection stage is not running all secondary voltages are available to power up the signal board. Because the main SMPS is always going through ACQUISTION mode during start up this mode needs to be explained. This section describes this special mode.

If the standby power supply is running and the microprocessor (µP) has switched on the PO signal, the main SMPS starts up. If the PO signal is high, the base of TP210 is also high and no base current can flow, therefore; TP210 is switched off and also TP161. The PWM pulses from pin 7 of IP170 are now able to drive the base of TP160.

After a few pulses the primary control circuit with IC IP050, TP050, TP051, TP080, and TP081 is now supplied by the winding between pins 4 and 5 of the SMT LP050. The rectifying components are CP061 and DP061. The resistor RP060 decouples the smoothing capacitor CP062 from the signal stage during the switch from ECO to STANDBY mode. The diode DP060 ensures that the VCC of IP050 and current limitation circuit of TP080 and TP081 is only 0.7V below the voltage of CP062.

ACQUISITION Mode

The AQR_ON signal is high during ACQUISITION mode turning on TP221. If transistor TP221 is switched on, base current of TP180 can flow via the resistor RP187 and the diode DP180 to ground. Thus the transistor TP180 is also switched on during ACQUISITION mode and the PWM circuit monitors the 6Vr and provides the secondary regulation pulses in the form of Pulse Width Modulation (PWM). The resistor RP188 and the parallel resistance of PP180, RP184 and RP183 attenuate the 6Vr to provide a DC voltage proportional to the 6Vr. The divided 6Vr, which is given to the base of the transistor TP179, is compared with the reference voltage on the emitter. The reference voltage is based on the 5Vs_STBY but increased by a voltage drop of DP170 that gives a temperature compensation of the voltage comparator TP179. The generated voltage from TP179 is used as one control input (pin 5) by IP170. The capacitor CP182 ensures a stable regulation loop over the used frequency range with a limitation of the bandwidth. The oscillator generates the saw-tooth for the PWM. The values of RP179 and the parallel impedance of RP181 with RP182 in series of DP179 define the maximum t ON time. The comparator of IP170 compares the saw-tooth at pin 6 with the 6Vr proportional DC voltage at pin 5 and the difference between the two voltages controls the t ON time of the PWM signal.

The resistor RP164 provides a pull up for the open collector output of IP170. This PWM signal is applied to the base of TP160. If the PWM signal is high, current can flow from 7Vs_STBY through the winding on pins 3 and 4 of LP070. The resistor RP161 limits the collector current of TP160. LP070 works as a voltage transformer providing a positive signal to pin 5 of IP050. If TP160 is switched off by a low PWM signal the collector voltage will be clamped by diode DP160 to the 7Vs_STBY. The resistor RP078 is acting as damping resistor and therewith eliminating oscillating. The diode DP161 ensures that no negative voltage “spikes” on the collector of TP160 can generate a signal at pin 5 of IP050.

Primary Control Circuit

The primary control circuit with IP050, TP050 and TP051 is used as buffer and driving stage of TP020. The PWM pulses that will be transferred by LP070 are compared on pin 5 of IP050 with the threshold determined by the resistors RP069 and RP070 at pin 6. The result is a regenerated pulse to drive the second comparator of IP050. Because the outputs of IP050 are open collector the resistors RP067 and RP062 are needed as pull up resistors. The output pin 7 of the first comparator will be compared with the threshold on pin 2. This ensures during power up and down that only pulses at pin 1 can drive the push pull circuit of TP050 and TP051. This protects the transistor TP020 against high losses and reliability problems. The resistor RP054 limit the base current of transistor TP051 if pin 1 of IP050 is switched to ground. Two comparators in series are necessary because the first one is acting as pulse former and

with TP034 as demagnetization control. The second one is a driving circuit with the transistors TP050 and TP051.

The most critical period of operation for a SMPS, especially for the power transistor TP020, is the starting phase. All capacitors on the secondary side are discharged before switching on and present a short circuit to the SMPS for the first few cycles. The power supply has to be protected during this switch on phase.

For the first cycles the current limitation becomes active during start up of the main SMPS. The current through diode DP110 is very high and because of the low start up frequency of approximately 2.5kHz the current will be zero before next switch on of the transistor TP020. This is important because if the current of DP110 is not zero, which means there is still energy inside the SMT, and the transistor TP020 is switched on, will result in high peak reverse voltage of DP110.

ACQUISITION to ON Mode

After the main SMPS is in ACQUISITION mode it depends on the µP to switch on the horizontal deflection stage. When the horizontal deflection is running, the oscillator with IP170 and transistor TP170 is synchronized by the H_DRIVE signal. The H_DRIVE signal is started approx. 600ms after PO becomes high.

The transistor TP221 ensures that during ACQUISITION mode only the 6Vs regulation is active. This means if AQR_ON is high the transistor TP221 is switched on because a current can flow from the 5Vs_STBY via the resistor RP223 and RP221 in the base of TP221. The resistor RP224 in conjunction with capacitor CP221 is for filtering of horizontal disturbance on the AQR_ON signal. The time when AQR_ON is switched to low is approx. 100ms after H_DRIVE was started. This ensures that the switch from ACQUISITION mode regulation to ON mode regulation will be done when the horizontal deflection start up is nearly finished.

ON Mode with Secondary Regulation

The PWM circuit monitors the +USYSr voltage and provides the secondary regulation pulses in the form of Pulse Width Modulation (PWM). The resistors RP900, RP185, RP183, PP180, and RP184 attenuate the +USYSr to provide a DC voltage proportional to the +USYSr. The resistor RP900's value is dependent on the required system voltage for the picture tube. A fine adjustment of the system voltage can be done by variation of the resistor PP180.

The divided +USYSr that is given to the base of the transistor TP179 is compared with the reference voltage on the emitter. The reference voltage is based on the 5Vs_STBY but increased by a voltage drop of DP170 that provides temperature compensation of the voltage comparator TP179. The generated voltage from TP179 is used as one control input (pin 5) by IP170. The capacitor CP182 ensures a stable regulation loop over the used frequency range with a limitation of the bandwidth. The oscillator that is built with IP170 in conjunction with transistor TP170 generates the saw-tooth for the PWM.

During ON mode the lower threshold of the oscillator described in the Oscillator section will be impressed through the negative voltage produced by the differentiation of the H_DRIVE pulse. The differentiation will be done by resistor RP220 and capacitor CP175. This allows the oscillator to synchronize with the horizontal deflection frequency.

The maximum t ON time is defined by the values of RP181 and RP179 that is approx. 40% of the horizontal frequency. The comparator of IP170 compares the saw-tooth at pin 6 with the +USYSr proportional DC voltage at pin 5 and the difference between the two voltages controls the t ON time of the output signal PWM.

The resistor RP164 provides a pull up for the open collector output of IP170. This PWM signal is applied to the base of TP160. If the PWM signal is high, current can flow from 7Vs_STBY through the winding on pins 3 and 4 of LP070. The resistor RP161 limits the collector current of TP160. LP070

works as a voltage transformer providing a positive signal to pin 5 of IP050. If TP160 is switched off by a low PWM signal the collector voltage will be clamped by diode DP160 to the 7Vs_STBY. The resistor RP078 is acting as damping resistor and therewith eliminating oscillating. The diode DP161 ensures that no negative voltage "spikes" on the collector of TP160 can generate a signal at pin 5 of IP050.

TP020 - One Complete Cycle in On Mode

Switch On Phase

The rising edge of the pulse from pin 1 of IP050 switches the transistor TP020 on hence the voltage across the transistor is almost zero. This switches a large voltage across the capacitor CP052 of the primary snubber network. The capacitor CP020 will also be discharged during switch on. This results in a short charging current through the capacitor CP052 and discharging current of CP020 and thus through the drain of TP020. The resistor RP051 limits the size of this current peak.

Conduction Phase

With TP020 now conducting, the current through the primary winding of LP050, and hence through the transistor's drain, rises linearly with time. For the driving of the gate this conduction phase must be separated into two parts: the t ON time of IP050 in conjunction with TP050, TP051 and the storage time of TP020.

t ON Time of IP050, TP050

During this period the output from pin 1 of IP050 is high and current flows from the auxiliary voltage via resistor RP061, the transistor TP050 and resistor RP053 into the gate of TP020. The auxiliary voltage winding is between pins 5 and 4 of the SMT LP050. The rectifying components are CP062 and DP061. This voltage is approximately 14V and supplies the primary control circuit IC IP050, transistors TP050, TP051 and TP080 and TP081 during ACQUISITION or ON mode. The resistors RP061 and RP053 define the value of the positive gate current. The resistor RP055 gives the gate of TP020 low impedance and eliminates the risk of unwanted switching on. The diode DP053 ensures that the gate source voltage of TP020 is limited and a high energy or burst pulse from the AC can't destroy the transistor.

Storage Time of TP020

The storage time is the time required to cut off the drain source channel of the power transistor. At the beginning of this period the gate current is reversed in direction by pin 1 going low and the current flows from the gate via the transistor TP051 to ground. Resistor RP053 limits the negative gate current. The storage time of the power transistor TP020 is very small.

Switch OFF Phase

When the power transistor TP020 switches off, the current through the drain is abruptly cut off. At this time there is a large current flowing through the primary winding of LP050. This causes the voltage across the primary of LP050 and the transistor TP020, to rise rapidly. The snubber network limits the amount of this voltage. In addition the power transistor's gate source voltage must be zero during switch off so that it can sustain a high drain source voltage during this time.

OFF Phase

During the off phase the power transistors gate is held to zero. In a synchronized SMPS the off time must be separated into two parts: the energy transfer phase and the dead time.

Energy Transfer Phase
Immediately after the power transistor TP020 switches off, the energy transfer to the secondary starts. The output voltages of the SMT LP050 become positive, the secondary diodes conduct and the magnetic energy that is stored in the SMT LP050 is transmitted to the secondary capacitors with linear falling current of all secondary diodes.

During this energy transfer phase the voltage at the transistor TP020's drain is the sum of the rectified mains voltage across CP010 and the secondary system voltage multiplied by the primary secondary turns ratio of the transformer.

Dead Time
After the energy transfer is complete, there is a dead time that lasts until the next conduction pulse occurs. During this time, the transistor TP020 and the secondary diodes are off and there is no current in the SMT LP050. The voltages are oscillating with the winding inductance, the winding capacitance and snubber capacitance.

Primary Side Snubber Network
The primary snubber network consists of CP052, DP051 and RP051. When the transistor switches off CP052 is charged through DP051 by the current from the primary inductance (this current flows into CP010 thus returning some energy to the system). This has the effect of reducing the dV/dt on the transistor. Energy is now stored in CP052. The next time the transistor switches on CP052 is discharged through RP051. Thus the energy stored in CP052 is transferred to RP051 and dissipated as heat. For this reason RP051 has to be a large 10W resistor. The coil LP051 with damping resistor RP049 in parallel reduces the dI/dt flowing into the diode DP051 and thus reducing noise in the picture.

The additional snubber capacitor CP020 that is parallel to the transistor's drain and source has the additional effect of reducing the dV/dt on the transistor TP020. This helps to reduce noise generated by switching of transistor TP020. The capacitor CP019 works in the same direction as the capacitor CP220 with the difference that capacitor CP119 is connected via ferrite bead between drain of TP020 and ground. This provides a better result for EMI and the ferrite bead LP004 avoid oscillating from the falling edge of TP020's drain current.

Secondary Side Snubber Network
The snubber network on the secondary side consists of CP112, DP111, DP112, DP113, LP112 and RP112. When the transistor TP020 is on the capacitor CP112 is charged through the diode DP113 to the negative forward voltage of the system voltage winding. The inductance LP112 limits the slope of the charging current and thus provides a slow charging of the capacitor CP112 when the transistor TP020 switches on. When the transistor TP020 is switched off the voltage across the system voltage winding rises rapidly and also the voltage on the anode of the diode DP112. When the voltage on the anode of the diode DP112 reaches the level of the 10Vr, the diode DP112 starts to conduct. When the diode DP112 starts to conduct the capacitor CP112 discharges and reduces the dV/dt of the secondary (and hence the primary due to coupling) winding.

The resistor RP112 is necessary to dampen oscillations between the inductance LP112 and the capacitor CP112. An additional filter with the inductance LP114 in conjunction with capacitor CP114 is needed for picture disturbance improvement. The ferrite bead LP113 and the capacitor CP113 helps to reduce picture pollution generated by switching of the diodes DP112 and DP113. Energy that is stored in LP112 is also given back via the diode DP111 to the 10Vr. Unlike the primary snubber network the secondary snubber network returns the energy stored in the capacitor CP112 to the system. In this case the 10Vr capacitor CP140.

Demagnetization Control
The demagnetization control circuit prevents the power transistor TP020 from switching on while the SMT LP050 is still magnetized. Without this magnetization control the transistor TP020 could

switch on while the SMT LP050 is still magnetized. When this happens the switch on current through TP020 will be too high reducing the reliability of the transistor TP020.
Another problem is the diode DP110 will be damaged if the transistor TP020 is switched on and the SMT LP050 is still magnetized because this result in a high peak reverse voltage of DP110.

Secondary side
The circuit with RP162, RP163 and TP161 prevents the power transistor TP020 from switching on while the SMT LP050 is still magnetized. When the SMT LP050 is still magnetized the secondary diodes are still conducting and the voltages across the secondary windings are clamped. When the SMT LP050 is completely demagnetized the secondary diodes are no longer conducting and the voltages across the secondary windings fall. Thus the voltage across a secondary winding is used to switch the transistor TP161 so that it can inhibit the secondary regulation pulses from the PWM circuit (IP170, TP173, TP179) while the SMT LP050 is still magnetized. The 6Vr winding was chosen to drive this demagnetization circuit because it has the lowest voltage across its secondary winding. The capacitor CP162 is for filtering during fold-back conditions.

Primary side
An additional circuit with transistor TP034 ensures that any PWM pulse delivered from secondary side via LP070 is disabled during fly-back time of the auxiliary voltage that is taken from the winding between pin 4 and 5 of LP050. The auxiliary voltage is attenuate with the resistors RP033 and RP034 compared with the base voltage of the transistor TP034 that is the zener voltage of the diode DP022. This means if the transistor TP034 is switched on during fly-back, the threshold of the first comparator from IP050 is set to a higher level than the pulse from LP070, therefore; pin 7 can not be switched high and the driving circuit with the transistors TP050 and TP051 is still switched off.

Secondary Voltages
+USYSr
The system voltage winding is between pins 15, 16 and 17 of the SMT LP050. The rectifying components are CP110 and DP110. CP111 is necessary to reduce noise caused by the switching of DP110. The jumpers JP911 and JP912 select the required system voltage (+USYSr).

In ACQUISITION mode the +USYSr is approx. 150-190V, which depends on load. The regulation for the SMPS in ON mode is done using the +USYSr because of the high load variation on this voltage. The system voltage provides the main power source for the Diode Split Transformer (DST) sometimes also referred as Integrated High Voltage Transformer (IHVT) and the line deflection. The system voltage can supply the DST with enough power for a picture power of 60W. The tuner is also supplied from the system voltage via RP113, RP114, RP117, RP120 and a 33V Zener diode that is located on the signal board. The capacitor CP562 improve EMC situation.

20Vr
The 20Vr winding is between pins 18 and 21 of the SMT LP050. The rectifying components are CP120, DP120 and noise suppresser CP121. The 20V supplies, in ON mode, the horizontal driver circuit and for an external module via connector BP120. It is also used for the 5V regulator located on SSB or the BSVM circuit located on CRT board.

10Vr
The 10Vr is between pins 19 and 21 of the SMT LP050. The rectifying components are CP140, DP140 and noise suppresser CP141. The 10Vr has a nominal value in on mode of 11.5V. In ACQUISITION mode this voltage is approx. 11.8V. The 10Vr voltage supplies in ACQUISITION and ON mode the different 8V regulators on the signal board. The inductance LP140 with the capacitor CP512 gives an additional filtering of the used input voltage for the different 8V regulators on the signal

board. The capacitor CP511 parallel with CP512, ensure low impedance during arcing.

6Vr
The 6Vr winding is between 21 and 22 of the SMT LP050. The rectifying components are CP150 and DP150. The capacitor CP151 is necessary to reduce picture noise caused by switching of the diode DP150. The 6Vr supplies in ACQUISITION and ON mode the 5V regulation and 3.3V regulator on the small signal board. The inductance LP151 with the capacitor CP522 gives additional filtering of the input voltage of the 5V regulator. The capacitor CP521 parallel to CP522, ensure low impedance during arcing.

5V_A/5V_H
In ACQUISITION and ON mode the 5V regulation is supplied by the secondary voltage 6Vr that was described previously. The voltage reference for the 5V regulation is the REF voltage that is generated by the UP converter. The switch TP523 is acting as a differential voltage stage with an advantage of temperature stabilization. The resistors RP527, RP523 and RP524 divide the 5V and, therefore; the voltage at pin 5 of TP523 is compared with the reference voltage on pin 2 of TP523.

Because the current sum of both "transistors" in TP523, flowing through RP522, is always the same, it depends on the level of the 5V which transistor or both is more or less conductive and thus the level of the gate voltage from TP520 which results in a regulated 5V. To ensure that the gate voltage of TP520 is high enough, the +20V is used via the resistor RP520. The diode DP520 limits gate voltage of TP520 during arcing or ESD. The resistor RP525 limits pin 2 current of TP523 and is acting as a filter in conjunction with CP524 to reduce ripple on the reference voltage. The resistor RP520 and capacitor CP527 define the loop gain and frequency bandwidth of the regulation loop.

8.5Vr
The voltage regulator LF85CDT (IP540) is used to generate the 8.5Vr voltage, which is located on the signal board and is mainly used for front end and SCART.
The output voltage at pin 3 of IP540 has an additional smoothing capacitor CP544 and CP543 is used to avoid high frequencies and oscillations.

8Vr_1H
The voltage regulator KF80BDT (IP501) is used to generate the 8Vr_1H, which is located on the small signal board and is used for 1H video processing.
The output voltage at pin 3 of IP501 has an additional smoothing capacitor CP504 and capacitor CP503 is used to avoid high frequencies and oscillations.

8Vr_2H
The voltage regulator KF80BDT (IP510) is used to generate the 8Vr_2H, which is located on the small signal board and is used for 2H video processing.
The output voltage at pin 3 of IP510 has an additional smoothing capacitor CP514 and capacitor CP513 is used to avoid high frequencies and oscillations.

3.3Vr
The voltage regulator LD1117DT33 (IP530) is used to generate the 3.3Vr, which is located on the small signal board and is used for the UP-converter. The output voltage at pin 2 of IP530 has an additional smoothing capacitor CP534 and capacitor CP533 is used to avoid high frequencies and oscillations.

Sound Voltages
The dual sound voltage windings are between pins 12, 13 and 14 of the SMT LP050 with pin 12 being the audio ground. The rectifying components are CP130, CP135, DP130, DP135 and noise suppressers CP131 and CP136. The resistor RP137 that is connected between audio ground and chassis ground ensures that the audio ground is not floating in relation to the chassis ground. The sound voltages (±UA) have a nominal value in ON mode (sound muted) of ±17V.

In ACQUISITION mode these voltages are approx. ±18V. The resistors RP130 and RP135 provide a small load on the ±UA that prevents the output voltages from rising above 20V in mute. Because of the large load variation between mute and full volume

the regulation of the sound voltages is poor relative to the other secondary voltages. The ±UA supply the audio output amplifiers and supply the requested output power that is needed for the different versions.

Protection

The protection in the ATC221 SMPS has been designed so that when a short circuit or overload occurs on a secondary voltage the SMPS switches off completely. In addition the 6Vr is monitored to switch off the SMPS if an open loop of the PWM results in an over-voltage situation.

Primary Protection

On the primary side a current limitation by cycle to cycle exists, which means that the maximum transferable power is limited and all secondary voltages will drop down if this limit is reached for a certain length of time. The resistors RP072, RP073 and RP074 attenuate the voltage of RP052 to provide a voltage proportional to the drain current of the transistor TP020 and used as input of the circuit with the transistors TP080 and TP081. The capacitor CP073 in conjunction with resistor RP073 are acting as a filter against voltage spikes. If the voltage at resistor RP052 becomes high enough, base current of transistor TP080 can flow and transistor TP080 will be switched on. Also TP081 is switched on to speed up the switch on of TP080.

The switch on of TP080 results in pin 1 of IP050 being switched to ground via the diode DP080. Because the input stage and the driving circuit is decoupled by the voltage comparators of IP050, the current limitation circuit will be reset by the diode DP081 if the input pulse of LP070 and pin 7 of IP050 is going from high to low. If the level of maximum drain current is reached the transistor TP020 will be switched off and the input of the first comparator IP050 is still high.

Secondary Protection via Safety Circuit
Under voltage protection

The +20Vr is used to ensure correct connection of BP005 and BL111 via the lines CNT1_+20V and CNT2_+20V. The CNT2_20V is attenuated by the resistors RP540, RP521, RP530, RP526, RP193, RP196 and compared as input voltage on pin 5 with the reference voltage on pin 6 of IP190. The reference voltage on pin 6 is generated by the +5Vs via RP571, RP189, RP199 and RP200 that charges the capacitor CP199 when the PO signal goes low. The time delay is necessary to ensure that all secondary voltages that are controlled are at nominal level before the safety circuit becomes active. To ensure the protection is disabled during switch on of the SMPS a small voltage drop will be generated by the voltage divider RP190/RP196.

If any of the secondary voltages 5V, 3.3V, 8.5V, 8V_1H, 8V_2H, 20V, or +UA which are controlled by the circuit DP521, DP530, DP540, DP501, DP510 and DP193 drop below 50% of the nominal value, pin 7 of IP190 is switched to ground. Therefore TP210 will be switched on and the transistor TP161 will disable the PWM pulses from pin 7 of IP170 to the base of transistor TP160. This means the SMPS will be stopped.

An additional circuit with TP197 controls via RP198 the negative voltage -UA and will be switched on if the voltage -UA is also less than 50% of the nominal value because base current can flow from the voltage +UA via RP197. A switch on of TP197 is the same result as before so that the voltage on pin 5 is lower than on pin 6 of IP190. The same situation as described before results in a switched OFF SMPS. The resistor RP192 together with capacitor CP158 is for filtering against crosstalk of the collector line from TP197. The diode DP197 ensures that the base voltage of TP197 is limited to a maximum negative voltage of -0.7V and the capacitor CP197 filter, in conjunction with RP197 and RP198, the ripple of the audio voltage and ensures that TP197 is not switched on if a small spike occurs on +UA.

Protection by X-Ray circuit

If for any reasons the X-Ray circuit of the horizontal deflection with IV520 becomes active the capacitor CV524 will be charged via the resistor RV531. This time constant ensures that the transistor TV524 is not active during transitions between different horizontal scanning modes. It is important to note

that the main power supply can be switched off by transistor TV524.

Protection by Beam-Current control circuit of PTV

The transistor TV04 is blocked during ON mode because TV40 is switched on by the rectified DST voltage but can be active during ACQUISITION mode. If the transistor TV04 is active via the beam current control circuit on the ADB board the RP_SAFETY line which is connected via the jumper JL960 to SAFETY is low and the main SMPS is stopped.
It is important to note that the transistor TV04 can switch of the main power supply.

Over voltage protection

If there is a open loop of the PWM regulation the +6Vr increases and the voltage comparator at pin 2 of IP190 becomes higher then pin 3 and pin 1 will be switched to ground. With pin 1 at ground TP210 is switched on and as a result the transistor TP161 will disable the PWM pulses from pin 7 of IP170 to the base of transistor TP160 thus stopping the SMPS.

Fold-back Point

The fold-back point is where the load on the output of the power supply is increased until the SMPS can no longer regulate and the +USYSr starts to fall. The reason that the power supply can no longer regulate for large loads is that the drain current of TP020 is so large that the current limit threshold is reached. This effectively limits the energy that can be stored in the SMT LP050 and hence the energy that can be transferred to the secondary side.

DEFLECTION

Deflection Overview

The deflection overview can be divided in the following functional blocks:

- Deflection Controller – IV200 TDA9330H (HOP)
- Horizontal deflection
- **H**orizontal **O**utput **T**ransistor TL010
- High voltage source; **IHVT** LL008
- East/west correction - diode modulator
- 2H/2.14H adaptation
- Vertical deflection
- Earth field correction = Picture Rotation (**EFC**)
- Deflection safety circuitry
- X-ray protection circuitry

The heart of the deflection is the I²C-BUS- controlled video and scanning processor IV200. The TDA9330H (IV200) uses an external 12Mhz ceramic resonator for generating a stable clock that will be synchronized with h- sync ("H-DFL" signal) and v- sync ("V-DFL" signal) from the up conversion process by means of a "PHI 1 loop" on the 2H side. The HOP driver generates the base currents for driving the horizontal output transistor in forward mode. An implemented current regulation ensures an always-good driving condition independent from supply voltage variation given by different power supply loads.
Supply voltages delivered by the IHVT transformer are:

- Anode (EHT) voltage
- Static and/or dynamic focus and G2 voltage (from focus block)
- +200V video voltage (boosted by Usys)
- +Uvfb, vertical fly-back voltage
- +Uvert, positive vertical supply voltage (+13V)
- -Uvert, negative vertical supply voltage (-13V)
- Picture tube heater voltage

A diode modulator for modulation of the picture width is driven by a parabolic waveform to correct the pincushion distortion of the picture tube. The diode modulator also includes the linearity correction linearity coil and the dynamic S-correction at double the frequency.
The vertical amplifier IF001 (TDA8177F) is driven by two differential saw tooth currents from the "HOP". The feedback information is generated from the voltage drop over the vertical sense resistor and the vertical yoke is driven to GND. This concept needs a positive and a negative supply voltage plus additional fly-back supply to guarantee the retrace time.

The safety circuit senses all output voltages from the deflection. It reacts on opening of the deflection (H and V), short circuit, and excessive high voltage.
X-ray protection is detected by using a "window-comparator" (build with two OP-Amps IV520 and IV521), comparing a rectified retrace signal with an adjustable reference signal. The circuitry reacts on excessive EHT as well as on too low EHT.

The different safety information from the deflection is "DEFL_SAFETY", "EHT_INFO", "EW_PROT" and "SSC_V_GUARD". These signals are passed to the signal processing board where they are processed and connected to either, the "flash protection input" (*Pin 5* of IV200) or the EHT-protection input (*Pin 4*).
The "FLASH-Input" (*Pin 5*) reacts on a voltage higher then 2V by stopping the horizontal drive signal immediately. In order to avoid an automatic restart of the HOP, the voltage at the *pin 5* has to be kept over 2V until a new start is requested.

The threshold for *Pin 4,* the EHT (over-voltage) protection is 3.9V. Once the level at this pin exceeds 3.9V the HOP goes to STBY via slow stop procedure. The XPR status bit will inform the µP. The µP configures the over-voltage input pin either to detection or protection mode. The detection mode is valid during alignment procedure and the protection mode is valid during normal operation.
The "SSC_V_GUARD" information leads to RGB blanking in case of a vertical defect. This signal is

also used on the optional DFB module for generation of focus blanking during cut off measurement.

TDA9330H - deflection processor (HOP)
The TDA9330H is a combination of RGB output processor and deflection processor. It provides:

- A stable clock generation using an external ceramic resonator
- Horizontal synchronization with two control loops and alignment free oscillator
- Slow (soft) start and slow stop of horizontal drive output to enable low stress start- up and switch off
- Vertical countdown circuit for stable behavior, including absence of H and / or V sync.
- Vertical linear zoom from 75% to 138% of adjusted nominal amplitude
- Vertical scroll function used for raster panning
- Progressive scan
- Horizontal and vertical geometry control
- Several safety inputs

During acquisition mode or after the main power supply comes up and the supply voltage for the HOP is present all registers can be initialized with correct (adjusted) values. This means the deflection can start with defined settings.
The HOUT pin 8 is the driver for horizontal deflection. Under normal operation the duty cycle of HOUT pulse is 48.2% off (high) and 51.8% on (low). When a fly-back pulse is present at pin 13 (HFB), HOUT is always set high irrespective the status of the output. In this way, switch on of the HOT during fly-back is prevented. The detection level is .3V.

A built in slow start/stop circuit ensures a smooth start/stop behavior of the deflection. During switch on the horizontal output starts with a fixed off time of 48.2% while the on time increases from 0% to 51.8%. The "on time" increases from 0% to 6.2% and lasts 50ms, while the on time increase from 6.2% to 51.8% and lasts 100msec. These values lead to a linear build-up of the EHT voltage in 150msec while the horizontal frequency decreases from about double the final frequency to final frequency. By using the ESS (**e**xtended **s**oft **s**tart) function the on time increases from 39% to 51.2% is extended to 1000msec. When switched off via the stand by, the off time remains fixed on 48.2% while the on time decreases from 51.2% to 0% in 43msec. The on-time decrease starts after vertical scan and vertical fly-back is completed.

The saw tooth signal that is derived from an internal saw tooth generator is controlled by I²C bus. Control functions are **v**ertical **a**mplitude, **v**ertical shift, vertical **s**-**c**orrection, **v**ertical e**x**pand (zoom), **v**ertical **sc**roll. To prevent picture tube damage, a built-in blanking blanks the RGB outputs for vertical over scan, larger then 105%. The vertical geometry processor has a differential current output for a DC coupled vertical output stage.

The horizontal geometry processor has a single-ended current output for EW drive. It offers I²C control for **EW** width, **p**arabola **w**idth, **c**orner **p**arabola, and **t**rapezium **c**orrection.

Both the vertical and the EW drive can be modulated for EHT compensation. This tracking makes the picture size independent from EHT variation due to the beam current.

Horizontal deflection
Horizontal driver
The transformer driver for the horizontal deflection output transistor is operated in forward mode. A positive voltage, depending on the duty cycle of the driving signal, appears at CL005 as a virtual ground. The primary winding input is switched to positive and negative voltages referenced to this ground.

The +20Vr is regulated by the linear operation of TL004. A current feedback via sensing resistor RL015, RL005 and TL005 is used for a temperature independent regulation of the base current.
RL006 and CL006 create the correct shape for the base current of TL030 to minimize the saturation losses. TV513, the first transistor of the driver circuit, which is located on the signal board, is highly saturated when TL030 (DV only) is switched off shorting the collector of the regulation transistor TL003. When TV513 is high impedance, by a low

signal of H_DRIVE, the voltage at the collector of TL003 is regulated to drive the output transistor TL030 (DV only) with the correct base current.
NOTE: **TL030 (DV only):** The implementation of a MOS transistor in the emitter of a bipolar transistor to improve its switching performances is well known and has been used in full-integrated driving solutions. The advantage of the MOS solution is that the emitter current being suddenly stopped, the current in the collector keeps on flowing through the base until switch-off. This switch-off characteristic is independent and no more a function of the driver.

Diode modulator
A diode modulator is used to modulate the horizontal deflection current with minimum effect to high voltage. This can only be achieved, if the primary current is not influenced by the changes of the currents inside the deflection circuit.
The diode modulator is a bridge connection of 2 circuits with the same resonant frequencies. One part is the bridge coil LL029 together with CL032 in series connected with CL029 and CL1296. The other part is the deflection yoke together with the retrace capacitor CL031 in series connected with CL035. The L*C products of both circuits are the same.

The capacitive divider CL031 and CL032 produces a retrace voltage across CL032. The integrated value of this voltage could be seen across CL029 and CL129, if the diode modulator is uncharged. In this case we have a minimum AC voltage across the deflection yoke and the deflection current is minimal. The voltage across CL029 and CL129 reduces the supply voltage for the horizontal yoke.
If CL029 is shorted we have the whole supply voltage across the deflection yoke and the deflection current is at maximum. Current out of CL029 and CL129 during the trace discharges CL029 and CL129 so that the energy to be stored in LL029 is less at the beginning of the next retrace. As a consequence the retrace voltage across CL032 is less.
The circuit can also be described as two deflection circuits, which are in series and operate at the same frequencies.
LL030 and LL032 suppress fast current transients to reduce HF noise. RL030 and RL032 are damping the current in the two coils in order to avoid spike lines.
CL030 is chosen together with the primary inductance of the DST to have no frequency change during the fly-back on the lower part of the diode modulator.
LL034 and CL034 build a series resonant circuit for dynamic S-correction. It is adjusted slightly higher then double line frequency to correct the horizontal linearity.
The network DL034, DL036, RL036 and CL036 create a damping network to suppress oscillations on the S-capacitor CL035 after fast changes of the beam current.

East west correction
The east west correction is corrected by using a MOSFET as a power transistor
(TL029). This FET is driven by the TDA9330H with a current sink, reducing the gate voltage defined by the feedback resistor RL028. Resistors RV026, RV026, and RL028 define the correct working range. Resistors RL021 and RL025 connected between Source of TL029 and GND are used for sensing the current in the EW circuit and improve the temperature behavior by terms of current feed back. DL029 and DL028 are only needed to secure the EW circuitry. In acquisition mode current has to be high enough to safely activate overload protection of power supply. Capacitors CL025 or CL028 are needed to avoid oscillation.
IHVT compensation is done inside the HOP IC.

2H-2.14H mode Retrace time adaptation
Due to the different horizontal frequencies, 2H (31.47KHz) and 2.14H mode (33.75KHz), there would normally be major changes in EHT. To avoid this there are two possibilities, either to change the B+ voltage or to make a retrace time adaptation.

To prevent major changes in EHT a change in retrace time of 0.4µsec is needed; therefore, 5.0µsec for nominal retrace time and 2.14H mode and 5.4µsec as retrace time for all 2H signals is selected. Switching a second capacitor in 2H mode parallel to

the upper and lower retrace capacitor provides the retrace time adaptation.

The switching signal from the µP is named 480_ON. This signal goes high during 2H mode and low during 2.14H mode. A high at signal 480_ON forces TL100 to conduct turning off TL104. The gate of MOSFET TL105 goes high through RL112 and diode of IL110, switching capacitor CL105 parallel to CL032.

Because the upper retrace capacitor is floating, there needs to be a slightly more complicated driver circuit. The supply voltage for this driver circuit is stored in CL110. Diode DL106 is conducting during trace time and de-couples the +6V from the floating driver circuit during horizontal retrace. If TL100 is off, the base of TL111 goes high through RL106, DL105, DL104 and RL105. This causes a low at the base of TL120 forcing it to turn off. Once TL100 starts conducting because of 480_ON signal, TL111 is turned off. Now TL120 has base current through RL110 and RL120 allowing TL120 to switch CL120 parallel to CL031.

The signal at the base of TL105 is also connected via RL136 to the gate of MOSFET TL135. TL135 shorts out CL135 in 2H mode. This means the tuned circuitry of LL034 and CL034 works on a lower resonant frequency in 2H mode than in 2.14H mode. Where capacitor CL135 is series connected to CL034 this reduces the "effective" capacitance and therefore increases the resonant frequency.

To get a proper linearity in 2H as well as in 2.14H mode, additional capacitor is switched for 2H mode in parallel to the main S-capacitor. MOSFET TL140 does the switching. TL140 is driven by opto-coupler IL140. The opto-coupler provides switching when using a diode modulator with IPIN correction, where the main capacitor is floating.

Vertical power stage

The ATC221 uses a plus and minus supply for the vertical power IC TDA8177F (IF001). The vertical deflection yoke is connected over a sense resistor to GND. This makes the sensing of vertical current for feedback information very easy.

The power required for the first half of vertical deflection (trace), is drawn by IF001 from the +Uvert (+13V) rail. The –Uvert (-13V) rail supplies the second part of the vertical trace. For retrace, the power is taken from the special retrace voltage called +Uvfb. All three voltages are generated by the IHVT.

The deflection processor TDA9330H was originally designed to work together with a vertical power stage in bridge configuration. In order to use the TDA8177F vertical IC it is necessary to make a current-voltage conversion of the two vertical signals ("v_drive_+" and "v_drive_-"). This is done with resistors RF003/4/5/6.
Transistor TF041 generates together with RF041 and RF040 the vertical guard information, a small current that goes into the SSC pin of the deflection processor during each vertical period of the SSC signal. If this information is missing the TDA9330H detects a vertical error and blanks the RGB outputs to avoid damaging the picture tube.
The generation of vertical S-correction is done inside the HOP. The amount of correction is adjustable via I²C bus.

EFC correction

(This correction is only used on direct view TV.)
The earth field correction will be controlled via software by means of the pulse width modulated signal "EFC". The direction and the amount of current are dependent on the bias voltage of the earth field correction power stage.
The user can control this voltage via menu option Picture Rotation. "EFC" is a 5V PWM signal that is converted to ±Uvert by TL801 and TL803. RL806 and CL806 are the integrator of the PWM. TL807 and TL808 is the power amplifier for the EFC current. The output signal of the EFC power stage is fed through BL200 to the CRT board and then to the two-pin connector BB007 where the EFC coil is plugged in.

Dynamic S-correction and 2H Correction

Picture tubes with flat panel have a special geometry distortion. The correction of this distortion is called "dynamic S-correction" or "2H correction". The 2H correction is a tuned circuit consisting of a transformer and a capacitor. The resonant frequency is 76kHz.

Safety circuit

The safety circuit monitors all output voltages from the deflection, detects any shorts or opens in the deflection circuits (Horizontal and Vertical), and senses excessive beam current. The ATC221 uses the FLASH input pin of IV200 for all safety function and EHTIN pin for X-ray protection. This input will switch off deflection if the level becomes greater then 2V.

We can divide the complete safety circuit into four main blocks. One block senses via signal DEFL_SAFETY excessive beam current. The second block senses via signal EW_PROT current in the diode modulator (short-circuit or open deflection). The third block senses via signal "EHT_INFO" for too low EHT caused by short retrace time or small +Usys. The diodes DV520, DV534 and DV535, on the SSB board, separate the three blocks for independent reaction. The fourth safety block, the X-ray protection is connected via DV523 to pin 4 "EHTIN". The XRP-circuitry reacts on excessive EHT because of excessive +Usys or short retrace time.

The two comparators of IV520 are connected to the same reference voltage from the DACOUT of IV200. This reference voltage is connected to the inverting input for X-ray-protection (IV520 Pin2) and on the non-inverting (IV520 Pin5) input for under voltage detection. The signal "EHT_INFO" from the deflection board (rectified retrace information) is connected to the non-inverting input, Pin 6. The information at Pin 6 is additionally divided for the inverted input of the first OPAMP by RV532 and RV528. Under normal condition we get around 4V at Pin6 (under voltage detection) and around 2.7V at Pin3 (X-ray-protection). The reference voltage, preset with resistor divider RV524/RV529 and adjusted with signal DACOUT, will be between the two values.

The first OPAMP of IV521 (Pin 5,6,7) is used in the same way as IV520, but with a reference voltage of 1.3V. It reacts on a different signal named EW_PROT and is generated by integration of the EW voltage at the drain of TL029 (RL023, RL024 and CL023) and EW current, sensed at the source (RL025, RL021 and CL023). RV526 is used to secure the input of the OPAMP at arcing and ESD situations. DV533 and RV533 are used to avoid automatic restart.

The second OPAMP IV521 (pin1,2,3) has again the same reference 1.3V on the non-inverting input. The inverting input is connected with the DEFL_SAFETY signal, which is nominal 3.5V±1V. If the signal DEFL_SAFETY goes low during normal operation because of excessive beam current or a problem on RP_SAFETY, the output of the OPAMP goes high and activates the FLASH protection immediately. DV533 and RV533 are again to prevent on/off cycling.

The +10V serve as supply voltage of the HOP IC and the safety circuit.

During standby the signals DEFL_SAFETY and H_DEFL_PROT are not detected because the deflection is not active. The safety circuit needs to be disabled to allow the system time before all voltages are stable. This "safety disable" function is realized with TV522 and CV522. The µP has to set the signal

"SAFETY_ENABLE" to high immediately before the deflection starts. Then a current flows through CV522 into TV522. This current is valid until the capacitor CV522 is almost charged. During this time TV522 conducts and thus the cathode of DV535 is kept to low. Once the capacitor is charged, TV522 turns off and the circuitry from IV520 (Pin 5,6,7, H_DEFL_PROT under voltage) IV521 (Pin 1,2,3, DEFL_SAFETY) become active. Once the capacitor CV522 is charged the µP can't disable safety any longer.

Dynamic Focus Modulation

(DV only)

For direct view TV the focus modulation circuitry is located on a separate module called DFB. The module offers vertical and/or horizontal modulation. The supply voltage for vertical modulation and low impedance G2 input are on the power & scan board. It's generated via rectification of horizontal fly-back pulse at collector of line output transistor (DL500, RL570 and CL531).

Raster Shift – Horizontal DC Correction

(This correction is only used on direct view TV).

The raster shift circuitry is also located on the DFB module. A positive horizontal fly-back pulse is connected to the primary of LL550. The middle tap of LL550 secondary is connected to +Usys, creating a positive supply on CL551 and a negative supply on CL552 with respect to +Usys.

Potentiometer PL551 defines the dc-current, which is floating through TL554,

LL557 and RL559 to the "cold" end of the horizontal yoke or the dc-current, which is taken from the cold end of the yoke through RL559 and LL557 into TL551.

SYSTEM CONTROL (GenCAM)

The GenCAM Microcontroller

The GenCAM IC is a fully integrated TV microcontroller and Electronic Program Guide (EPG) processor that includes a 32-bit RISC processor core, bit mapped On Screen Display (OSD), Teletext data slicer, 1x/2xClosed Caption data slicer, and various TV control peripherals. GenCAM's main purposes are to act as a television controller, process Tele-text data, Closed Caption data, and EPG data transmitted on non viewable lines of a television broadcast and allow the data to be displayed on the television screen.

The GenCAM controls the whole ATC221 chassis via four I²C buses and some port lines. It supports the keyboard with 5 buttons as an analog keyboard. Also the POWER_SWITCH is detected with an analog input. It reacts to a command from the remote control in the standard RCA infrared format. Furthermore, the GenCAM will control the Audio mute, the power fail, and the Audio reset via ports. The ATC221 supports error identification via flashing the power LED and storage of the last five Error codes.

Power Mode Concept Overview

Besides the operation modes, the ATC221 is capable of a low-power function mode, called **ECO** mode. In this mode, the system will consume ~ 1.5 Watts. The temporary mode right after initializing software and before entering one of the other modes is called the **STANDBY** mode. The normal operational mode of the TV is called **ON** mode.

NOTE:

The ATC221 has 2 power supplies:

a) **STANDBY power supply.** This power supply delivers power to the uC and other digital circuitry. It has two software-controllable operational states, low power and high power. Low power (17Khz) is used to feed the uC and other peripherals in ECO mode, and in this state the supply also uses very little power for operation. High power (28Khz) is used for all other cases.

b) **MAIN power supply**. This power supply delivers power to hardware that uses high currents. The Power LED is a single LED that is only illuminated during ON-mode. It is controlled by Software from pin 123 of IR001.

ECO mode:

The Standby power supply operates at a frequency of 17KHz when the ECO_STANDBY port is set to "high". In ECO mode only the standby voltages +6V_STBY, +3,3V_STBY and +1,8V_UP are available. Therefore, only the **µC, ROM, SDRAM**, **IR** and **Keyboard** modules receive power.

To make the µC use as little power as possible, only the micro timer cell, the I/O ports and the A/D converter are enabled; all other internal peripherals are disabled. The frequency of the CPU clock is **16MHz**. Software is executed from external ROM and external SDRAM. Operating system is installed and running.

Only the TECI address at I2C_bus1 is supported. All other I2C busses are not supported. The LED is dark. The µC is waiting for an IR command, a Keyboard action or Timer information by monitoring the corresponding ports and cells. If a valid signal is detected, the µC will start the power on sequence, otherwise the µC will stay in ECO mode.

At AC power up the standby supply always starts in ECO mode and switches directly to Standby mode. Whether it switches back to ECO mode or switches ON is determined by the µC. This depends on the previous state of the set at AC power OFF, or if a valid switch ON command is detected either by IR or Keyboard.

When AC power is applied, a RESET is generated with IR040. During RESET all GPIOs are high. After RESET, the system will configure the SDRAM and set all ports to a default state.

STANDBY mode (this is only a temporary mode)

The main power supply is OFF. The Standby power supply is operating at a frequency of 28KHz. A total of 500mA are available from the Standby power supply. The µC, ROM, SDRAM, NVM, Port-

Expander, IR and Keyboard have voltage supplied to them and are fully operational. The internal CPU clock is set to **72Mhz**. Software is executed from external ROM and external SDRAM.
All IIC buses are enabled. Software has full control over all ¼C ports. Tuner, Video, Audio ICs, … are disabled and consume no power.
The LED is still dark.
In STANDBY-mode, the µC, ROM, SDRAM, NVM and Port-Expander has voltage supplied to it. If the µC switches from ECO mode to Standby or ON mode, the ECO_STANDBY line will be switched low. The Power supply will then be able to deliver around 500mA.

ON-mode
Main power supply is ON, and Standby power supply is working at full capacity (28KHz, 500mA max). The internal CPU clock is set to **72MHz**. Software is executed from external **SDRAM** and external ROM. Operating system is installed and running. All devices are supplied with power and initialized.
Deflection **is active** and the speaker's sound is **working normally**. Tuner, Video, Audio ICs, DRI board, … are enabled and operating. The +5V_ON / +8V_ON will be switched on/off by the Po_Port of the µC (pin115).
Also the deflection will be switched on via I²C bus_2. 100ms after deflection is switched ON, the power supply regulation is switched to ON mode regulation (AQR_ON = low).

DIGITAL READY INTERFACE (DRI)

DRI signal processing included Digital Visual Interface (DVI)

Video input select

The DRI-module has four possible input signals. The signals are: COMPONENT INPUT 4 and 5, DVI-input, and RGB_GRID. RGB grid is used for rear projection alignment. The component signals are connected directly to the cinch blocks BT940 and BT100 on the DRI-module. For common mode suppression of disturbances, all signal grounds are kept separated in the cinch blocks and pass through a filter (FT201 and FT202) before entering the input selection IC IT200. The DVI signals are connected to a special DVI plug also located on the DRI-module and after DVI decoding; they enter the input selection IC. The RGB_GRID signals for rear projection alignment are coming from the convergence board and are connected to BT110. IT200 handles the Video input selection. It has a built-in four system video switch, which can be selected by INPUT_SEL (I²C bus).

The input signals are:

- Input1: RGB_GRID and HV_SYNC signals
- Input2: RGB and HVsync signals coming from DVI input
- Input3: Component input 4 (upper row of DRI-module cinch plugs)
- Input4: Component input 5 (lower row of DRI-module cinch plugs)

Multi scan is provided for horizontal frequencies between 15 and 45kHz.

In the ATC221 chassis, 480i input signals with 15kHz (1H), 480p input signals with 32kHz (2H) and 1080i input signals with 33.7 kHz (2.14H) can be processed.

The selected signals are output from SEL_OUT (Pins 22, 23, 25, 26 and 27), respectively. The CXA2151Q is able to convert YpbPr signals and RGB signals into YCbCr by an integrated matrix. It is selectable with MAT_OUT (I²C bus) as follows according to the input.

For YCbCr input the matrix can be bypassed. The YCbCr signals can then be amplified by CBGAIN and CRGAIN to YUV levels. The YUV signals then have to pass a selection switch IT210, which is controlled by the 1H/2H_SELECT signal pin6 of BT400. According to the standard, which has been detected inside the CXA2151Q, the signals are either given to the 2H PSI IC (IT400) or the levels are adapted to the needs of the HIP-IC (IC500) on the small signal board. Therefore, U and V must be inverted with TT252 and TT253 and buffered with TT256 and TT257, whereas the Y level is adapted inside CXA2151Q by software setting YGAIN.

Sync processing

The sync processing is mainly performed by IT200 on the DRI-module. There can be two different types of sync: Either we get H- and V-syncs coming from DVI or RGB alignment grid, or we have sync on Y-signal for component inputs. HV sync signal input supports both positive and negative polarity. Existence distinction is first performed to determine whether the selected sync signals are input from H and V, and these results are sent as the existence status to the EV and EH status registers. On the other hand, polarity-matched H and V that passed through the polarity identification circuit are input to the priority ranking circuit. When inputting Sync on Y-input, it passes the sync select switch HYSW and then the signal is amplified by 6dB and output to YG_OUT (Pin 15). This output is returned to YG_IN (Pin 16) via transistor TT231 and sync tip clamping capacitor CT234.

The H and V sync signals selected by the HV sync signal processing block are sent to the SYNC counter block. The SYNC counter block counts the frequency of the input H and V sync signals and counts the H sync signal input during a certain period (~5ms). This time is based on the clock obtained by the internal VCO from the 4MHz ceramic oscillator QT231 connected to EXTCLK/XTAL (Pin 20).

For the V sync signal, the number of reference clock (31.25kHz) pulses during 1 V cycle is counted. The Hsync signals coming out of IT200 must be improved with an integrated dual mono-flop 74HC123 (IT230). This is necessary to suppress disturbing H-pulses in the middle of a line during vertical blanking start/stop

and to achieve rise times <100ns so that the sync processor on the chassis can run without phase disturbances. The first mono-flop generates a H-pulse with a length of about 3us and steep transients. The second mono-flop inside IT230 inhibits an additional H-pulse for about 23.5us. During HDTV Vsync, the Hsync pulse coming from IT200 is interrupted (due to original tri-level sync form) and wrongly triggers the mono-flop. To avoid this, an additional OR-gate is necessary (IT240-74HC1G32). With this additional OR-gate, the mono-flop cannot be triggered if one or both input signals are high. After that, the sync signals are given to sync processor on the Small Signal Board via BT010.

Projection TV only:
For convergence alignment, a selectable sync master is necessary. It must provide H and V syncs for 2H (480p) and 2.14H (1080i). This is done with a programmable logic divide, EPM3032 (IT220): At pins 33 and 34 an oscillator with 20.25MHz is connected. This oscillator is activated, when FB_GRID, coming from BT110 pin 2 is high; the H-frequency is determined by control signal 2H_214H coming from BT110 pin 9: High level = 2H (480p), low level = 2.14H (1080i). The 20.25MHz clock signal is divided to get 60Hz Vsync at pin 44 of IT220 and 33.75 / 31.4kHz Hsync pulses at pin 43.

PSI
For best picture, the STV2165 (IT400) provides some signal improvements to the 2H signals:

- Peaking
- Black stretch

For correct clamping a 2H sandcastle signal is required (BT400 pin8).
Since the process time for Y is 50ns less than for UV processing inside IT400, a delay line of 50ns (FT400) is necessary for Y.

YUV to RGB Matrix
The output format of IT400 is YUV, whereas the video processor on the chassis requires a RGB signal. Therefore a discrete matrix is implemented at the DRI output. The equations are:
R=Y+0.7U
G=Y-0.136U-0.356V
B=Y+0.7V
The **Y** signal is buffered by TT331 and afterwards AC coupled to the three adders, which are TT332 for Blue, TT354 for Green and TT374 for Red. The adders are grounded-base circuits.

The **U** signal is buffered by TT353, AC coupled for the Blue adder, also inverted by TT351 and buffered by TT352, and AC coupled for the Green adder.

The **V** signal is buffered by TT373 and AC coupled for the Red adder, inverted by TT371, buffered by TT372 and AC coupled for the Green adder.
Before the generated RGB signals leave the board via BT010, they are buffered by TT333, TT355, and TT375 for a 75Ohm termination on the chassis with correct levels.

DVI
The DVI is a digital RGB/HV interface. It consists of the integrated DVI-decoder IC IT600 and an EEPROM (IT620), in which the standards are stored, that can be displayed by the ATC221.
These are:
640 x 480p
720 x 480p
1920 x 1080i
When a valid standard is recognized, the DVI_DETECT signal (BT400, pin2) goes high so that the uP is informed. The DVI has no I²C-bus connection to the uP of ATC221 chassis. For more detailed information about DVI please refer to "Digital Visual Interface Rev 1.0" from DDWG http://www.ddwg.org/ or "EIA/CEA-861".

Frame comb filter (PTV only)
For projection TV a frame comb filter function must be provided. This is done with integrated frame comb filter uPD64082 (IT500). The NTSC-CVBS input signal is coming from signal chassis via BT400 pin 21 (FRAME_CVBS). It must be filtered (TT501, TT502 and TT503) and is AC coupled to AYI input pin 88 of uPD64082 (IT500). On the other hand an external sync separator must be derived from the CVBS input signal. This is done with TT511, TT512, TT513 and TT514.

After the signal is separated inside IT500, the Y signal is post filtered with TT531, TT532 and TT533 and the C signal is post filtered with TT541, TT542 and TT543. The signals (Y_FRAME and C_FRAME) are then transmitted back to Small Signal Board via BT400 pins19 and 18.

Audio processing

Audio input switching

With the audio matrix IT900 the stereo audio inputs from CMP1, CMP2, DVI, and, in case of an internal DVD player, the DVD input can be selected. The selected signal is fed to the SC4 input of IA001 on the small signal board via BT900. For common mode suppression of disturbances, all signal grounds are kept separated in the cinch blocks and pass a filter (FT940 and FT960) before entering the input selection of IA001 (TEA6422D). The TEA6422D switches 6 stereo audio inputs on 3 stereo outputs. After power-on reset all outputs are in mute mode.

Loudspeakers switching

The audio signal, coming from the power amplifier IA002 on the small signal board, goes to the DRI module at BT980. With the switch ST980 it is possible to feed this signal either to internal speakers BT982 right, BT983 left or to external speakers at BT985. The bipolar capacitors CT990, CT991, CT992 and CT993 in the external speaker output are inserted to decouple DC voltage in case of a defective power amplifier. This is a safety requirement to protect connected speakers from damage.

SMALL SIGNAL BOARD (SSB)

Small Signal Board (SSB)

The ATC221 **SSB** offers versatile CVBS and Y/C input possibilities:

- Three audio / video inputs:
  1. AV1: CVBS from jack input 1 or Y/C via SVHS connector
  2. AV2: CVBS from jack input 2 or Y/C via SVHS connector
  3. Front AV: CVBS from front-jack or Y/C via SVHS front-connector
- Internal CVBS signal (the demodulated terrestrial tuner signal) for the master and Secondary channel (PIP facility)
- Auxiliary CVBS (Sync) input for DVD RGB synchronization
- Additional 480i YUV input from the digital ready interface

The selected 1H signals (CVBS, Y/C, 480i or RGB) will be processed in the **H**igh-end **I**nput **P**rocessor (HIP) TDA9321, which delivers the resulting base band-signal (YUV) to the A/D converters (SDA9206).

The HIP consist of three main parts, the IF demodulator for the terrestrial tuner signal, the video matrix switch and the multi standard chroma decoder with embedded base band delay line.

CVBS - Y/C Signal Path

The CVBS signal path is switched by the external matrix switch TEA6415 (IX600) and by the matrix switch housed in the HIP IC TDA9321 (IC500 and IC700). The TEA6415 has 8 inputs for the external AV connections and the tuner signal and 6 outputs for the CVBS Y and C inputs. The TEA6415 also has monitor video output and the input signal for the frame comb filter. Each output can be switched to only one of the inputs whereas any same input can be connected to several outputs. Therefore the CVBS-Y/C selection of the secondary HIP is independent of the master HIP selection. All switching possibilities are controlled through the I²C bus 2.

The ATC221 is equipped with only one MSP. Therefore the sound processing of the antenna signal is always related to the main picture, never to the secondary one. Therefore if the antenna signal is selected as active main picture, the main tuner signal will be fed from IC500 to IX600 in order to switch the tuner signal to the SCART outputs.

IC500 output signals:
The COMB CVBS output provides the line comb filter TDA9181 (IC900) with the CVBS signal. This signal is also used for synchronization of the A/D converter in case of comb filter off or line comb on. The CVBS txt output is fed to the text processor inside the CPU and also to the CVBS1 input of IC700.
The third output CVBS PIP delivers the tuner or in case of SVHS detected by IC500 the related CVBS (Y+C) signal to IX600 in order to have the CVBS signals available at the monitor jack output.

Teki CVBS Input
There exists an additional CVBS input, which is used for factory alignments. Here, additional to the I2C bus 1 connection, a CVBS signal could be fed to the ATC221 chassis. This input is directly connected to the AV1 CVBS input.

DVD Signal
The DVD signal is always an RGB signal. To synchronize it, the CVBS signal of the DVD (AUX_CVBS) is fed via BX801 (Position L6) to CVBS1 input of IC500. To avoid a processing delay the comb filter is switched off.
To allow recording of the DVD signal, this CVBS signal is also fed via the CVBS PIP output of IC500 to IX600 and then to the monitor jack output. The RGB (nom 700mV, white) signals are fed to RGB2 input of IC500.
To display these RGB signals, it is necessary to enable the RGB via SW (Insertion Enable bit: IE2 =1) AND also to have a high Fast Blank signal (minimum level 0.9V) at the FB input of IC500 (pin40: RGBIN2). The FB signal does not come from the DVD player, but is generated by the bus expander IC IR006 (pin15) by SW control. A FB signal of less than or equal to 0.4V would switch RGB off. The RGB are converted by a matrix to YUV and are fed after level converting to the related inputs of the A/D converter.

480i Input
The Y, CB, CR (480i) signals have to be to supplied to the jack inputs of the DRI module. The CXA2151Q IC on the DRI module includes adjustable gain controls already, so that the Y, Pb and Pr signals are easily converted into the YUV levels, which the HIP needs: Y=1VBA, U= 1.33Vpp and V=1.05Vpp in case of a 75% color bar signal. As the HIP needs further –U and –V input signals, the signals are already inverted on the DRI board. These Y(-U)(-V) signals are fed from the DRI module via BX400 to the SSB board. To synchronize it, the level-adapted Y signal (YUV_SYNC) of the YUV signals is also fed via this connector to CVBS3 input of IC500. To avoid processing delays by the comb filter, the comb filter is switched off.

If the 480i input signal is selected, in order to avoid confusion with the 2H input signal, the jack monitor output will be blanked. The YUV signals are fed to RGB1 input of IC500. The input of IC500 is configured as YUV input. To display the YUV signals, two things are mandatory: The SW has to enable the YUV AND also Fast Blank signal (FB_YUV) of minimum 0.9VDC must be available at the FB input of IC500 (pin39: RGBIN1). A FB signal of less or equal 0.4V would switch off YUV. The YUV signals are fed to the related inputs of the A/D converter.

Video Processing
The video processing for the master and secondary channel is performed in each case by High Input Processors (IC500 and IC700) (TDA9321 2N). Optional IC500 can be equipped by an adaptive line comb filter or by a frame comb filter fitted on the DRI board. This section describes first the video processing for an ATC221 without comb filter and continues with the description of the LCF handling.

Luminance Processing
The selected CVBS Y signal is first back porch clamped and then supplied to a

chroma trap circuit (26dB attenuation of color carrier). In case of an active comb filter only the Y signal from the comb filter output is back porch clamped.

Luminance Delay and Adjustable Gain
The TDA9321H offers an adjustable luminance delay with a range of 0ns until 440ns with a minimum step size of 40ns. The luminance path is also equipped with an adjustable fixed gain (no AGC). Four steps are offered from -1dB until +2dB in 1dB steps. In order to compensate the gain drop in case of line comb filtering, the SW gain is used to increase the luminance amplitude by one dB, if the LCF is switched on. In all other case (LCF off, FCF on/off) the HIP gain is not used (0dB).

Chrominance Processing
Additional to the normal automatic color control ACC by the Burst amplitude, the TDA9321H (IC700) offers an automatic Color limiting ACL, which can be switch on and off by software. The ACL is a chroma amplitude detector, which is active, when the chroma / burst ratio exceeds approximately 3. The circuit prevents over saturation from occurring when a signal with a high chrominance to burst ratio is received.

Crystal and Color Standards
The color decoder (IC700) could decode PAL, NTSC and SECAM signals, but in the ATC221 only NTSC M is used. The decoder contains an alignment free X-tal oscillator.
In the ATC221 application only the 3.579545MHz crystal D at pin 57 is used.
The TDA9321H oscillator is optimized to suppress overtones of the nominal oscillation (e.g. 3rd harmonic). This leads to an increased sensitivity for oscillations of lower frequencies.

Comb filter Option
In the ATC221 application a line comb filter TDA9181 or a frame comb filter µPD64082 may be used. These ICs separate, in case of a NTSC M signal, the luminance signal from the chrominance signal with a decreased cross color and cross luminance behavior in comparison to a standard single notch/band pass filter of the HIP.

Line comb filter TDA9181
This comb filter works with switched capacitor circuits, which subsequently process the signal samples by transferring the charge of one capacitor to another capacitor. The internal clock oscillator, which is locked to the sub carrier (FSC) input signal of pin 9, has a frequency of 4*FSC. Because the voltage values are stored in capacitors (analog), the IC does not need any A/D or D/A converters. Thus the signal to noise ratio is better in comparison to a pure digital comb filter.

The HIP always provides the selected video signal to the line comb filter (LCF) input pin 12. The sandcastle pulse from the HIP (pin 59) ensures that the input signal will be clamped correctly. Depending on the level of standard selection, (SYS1 @pin25 and SYS2 @pin27), the comb filter is controlled. For correct comb filter function the IC needs the color sub carrier FSC (200mVpp) at pin 9, which is also comes from the HIP. The comb filter output signals COMBY (pin14) - the luminance - and COMBC (pin16) - the chrominance signal are fed to the corresponding HIP inputs. If the LCF is active, the luminance gain inside the HIP has to be increased by one dB (Software), in order to compensate for the voltage drop of the comb filter.

Comb filter, line or frame, is switched on by the ECMB bit of IC500. If IC500 detects Y and C signals at any other input, it ignores the signal from the comb filter and uses the internal YC signals for further processing. NOTE: IC500 delivers the Y+C signal via the COMBCVBS (IC500, pin 26) to the comb filter, if YC detection detects SVHS. If IC500 detects a black-white signal, the comb filter will be switched off. Correct clamping timing of the CVBS input signal of the line comb filter is controlled by the "three level" super sand castle pulse (SSC) from IC500 (pin39).

Frame Comb Filter
The frame comb filter FCF (IT500) is located on the DRI module. The processing of the frame comb

is similar to the line comb filter. If IC500 detects a SVHS or a B/W signal, the ECMB bit is switched off by the micro, so that the Y and C signals from the frame comb will be ignored.

Output 6 (pin13) of the video matrix switch IX600 delivers the frame comb filter with the needed input signal. The CVBS input signal (Frame_CVBS, BX400 pin 21) is first fed through a group delay correction circuit (TT501 with LT501/CT502) and then through a low-pass filter to pin 88 of the FCF. The same FRAME_CVBS signal is also used for the internal synchronization. Level clipping removes the video information from the signal, so that only the sync pulses are fed to pin 76 of the FCF. To achieve a good picture, the luminance and chrominance output signal of the frame comb filter are integrated by a low-pass filter and fed via BX400 to IC500. Because the frame comb filter causes additional processing delay, instead of the FCF input signal, the luminance output signal is used to synchronize the A/D converter, if it is active.

YUV Output Signals

The YUV output signals of the TDA9321H don't require further filtering, because an in house pre-filter is implemented in the A/D converters. There is also an internal amplifier in side the SDA9206 (IU003 and IU004) with 4dB amplification, therefore; it is only necessary to buffer and to attenuate the base-band signals to the required A/D input range to avoid any clipping of the signals.

TUNER

RF Splitter

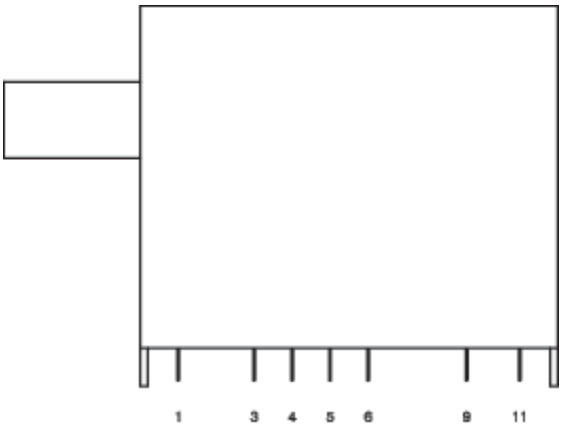
CPS24 is an active power splitter. The antenna input signal is filtered by a high pass filter with CB trap and amplified through a low noise, high linearity RF amplifier. The amplified signal is split into 2 paths via a balun transformer. The splitter module requires only a single +5V supply for operation. The splitter case is directly connected with the main tuner and the PIP tuner is connected via RF – cable.

Main Tuner

General description RF

The CTF5805 is a world standard tuner (WST). It is a frequency synthesized tuner with high gain and asymmetrical IF output. The tuner employs a switched 2-band concept. Bands 1 and 2 share a common RF amplifier, band-pass filter and oscillator. They are switched by using RF switching diodes. Band 3 has a RF amplifier, band-pass filter and oscillator of its own. A MOPLL IC is used for tuner mixer-oscillator & synthesizer function. Band-switching and oscillator tuning is controlled by I²C-BUS.

Tuner Pin out



1	AGC
2	N.C.
3	AS
4	SCL
5	SDA
6	UB
7	N.C.
8	N.C.
9	VT
10	N.C.
11	IF (Un-balanced)

General description IF

The IF has two SAW filters, FI025 (Video) PIF SAW filter and FI007 (audio) SIF SAW filter.

The PIF-signal passes through the picture filter FI025 (M3954M). The 45.75 MHz is used as the picture carrier (P.C.) frequency. The video signal is further processed in the IC IC500 (TDA9321H). The fixed 4.5MHz trap QI033 selects the video signal before it passes the internal video buffer of the IC IC500. The output signal is used for further video processing and the Video output jack.
The SIF-signal passes through the sound filter FI007 (M9370M). This filter selects the FM sound signal. The sound signal is further processed in the IC IC500. After IC IC500 the SIF is applied to the MSP for further audio processing.

PIP-Tuner CTF5805
The tuner of the main and PIP part are the same type. For a detailed descriptionof the CTF5805 see **Main Tuner.**

The PIF -signal passes through the SAW picture filter FI525 (M3954M). This filter selects the standard 45.75MHz used as picture carrier (PC). The PC signal is futher processed in the IC IC700 (TDA9321H). An internal group delay correction circuit is switched at flat group delay characteristic. The fix 4.5MHz trap QI533 selects the video signal before it passes the internal video buffer of the IC IC700. The ouput signal is used for further video processing and for SCART output.

NOTE: The PIP SIF input is not used. There is no sound processing with PIP.

UP-CONVERTER

Up-Converter
The up-converter, SDA9410 (IU030), is located on the small signal board.
The up-conversion is done after color demodulation. The signals used for up-conversion are luminance (Y) and color difference signals (U, V) from the color demodulator. The YUV signals are analog to digital converted by the external A/D converter SDA9206 (IU002 and IU003) prior to up-conversion. The output of the up-converter is field/line rate doubled video signals Y_OUT, U_OUT, V_OUT. They are converted digital to analog by DACs internal to the SDA9410 (IU030).

SDA9206 ADC with built in anti-aliasing filter and clock generation
The SDA9206 is a single monolithic IC containing three separate 8-Bit A/D converters for video (YUV) applications and a clock sync generator that is delivering the sample clock for the A/D converters. The device converts the YUV analog input signal into 8-bit coded words in a 4:2:2 format. The YUV processing consists of following functional blocks:

- Analog input buffers and clamping circuits
- Three 30 MHz A/D converters
- Digital decimation filters
- Delay compensation in Y-path
- Output formatter and buffer

The output is an 8-bit digital luminance signal (Y) and an 8 bit multiplexed chrominance (U/V) signal. The signals Y, U, and V are fed to the A/D converter IC SDA9206, pin 3, 8 and 13.

Beside the YUV digitalization the IC accommodates the sync processing and clock generation circuitry. The clock sync generator consists essentially of the following functional blocks:

- Analog clamping
- 7-Bit A/D converter
- Sync processor with digital horizontal PLL, vertical sync processor and pulse generator
- Clock generator with discrete timing oscillator, D/A converter, analog PLL and divider, as well as a crystal oscillator.

Video signal processing
The composite video input signals are AC coupled to IU002 and IU003. An internal AC clamping circuitry is provided for each of the analog channels. In this application the A/D converter has to clamp on the back porch of the video signal. The clamping voltages are generated digitally by on chip current sources, which load the external clamping capacitor during the clamping time.
The amplification of the input signals can be adjusted via I²C bus and internal pre-filtering of the analog input signals is implemented.
The data rates of the digital YUV signals are reduced in decimation filters following the A/D conversion. The input sampling rate is 27 MHz; the output-sampling rate is 13.5 MHz for the Y channel. For the UV channels the input sampling rate is 27 MHz and the output-sampling rate is 6.75 MHz. The decimator stages 1 and 2 have an adapted frequency response. Filter stage 3 of the UV channels is active for 4:1:1 mode (reduction from 6.75MHz to 3.375MHz).

Clock Sync generation
The clock sync generator is a PLL that locks on a horizontal SYNC input signal and generates the clock signals as well as additional control output signals. The input signal SYNC may be either a CVBS signal or a composite sync signal with variable polarity. A/D conversion takes place with 7 bits and a nominal frequency of 27 MHz.

The digital HPLL filters the signal with a cutoff frequency of 1 MHz. Following the low pass filtering a black and sync bottom level measurement takes place in order to calculate a threshold value. By means of this value the phase difference between the HPLL output and the SYNC input pulse is determined. Using a digital PI filter an increment is calculated from this for the Discrete Timing Oscillator (DTO). The DTO generates a saw-tooth with a frequency that is proportional to the increment. The saw-tooth is converted into a sinusoidal clock signal by means of a D/A converter and applied to an analog PLL that multiplies the frequency and minimizes residual jitter.

SDA9410 Display processor and scan rate converter
The SDA 9410 (IU030) is a single-chip up-conversion IC including scan rate conversion and the necessary field memories, which enables the system to reduce large area and line flickering of interlaced TV standards.

The scan rate conversion to 100/120 Hz interlaced or 50/60 Hz progressive scan is motion vector based. For the 100/120 Hz (50/60 Hz) conversion IU030 calculates 100/120 Hz (50/60 Hz) fields with continuous motion phases to avoid double contour effects in the motion display.
IU030 has two input channels, which can be used for different features like Picture-in-Picture (maximum approximately 1/9 picture) and "Double-window/Split-screen". The two input signals can be scaled horizontally and vertically with variable factors. Panorama modes will be supported.

Input format conversion (IFCM/IFCS)
The SDA9410 amplitude resolution for each input signal component is 8 bit. The maximum clock frequency is 27 MHz and the sample frequency relation of YUV 4:2:2.. The main memory of the SDA 9410 has an overall capacity of 6Mbit. It is divided into two identical and independent 3Mbit parts. In SCR operation mode the capacity to store 2 fields of the luminance and chrominance components of the master channel is supplied. Therefore the 4:2:2 data input format must be converted to either 4:2:0 or 4:1:1 format. Same conversion must be established for the slave channel.

Format conversion
The format conversion is divided into three blocks within IU030. Vertical compression and horizontal compression/expansion (panorama mode) is performed in the input-processing block. Vertical expansion is performed at the end of the digital signal processing. The format is chosen via I²C-Bus by changing coefficients and timing of vertical and horizontal filters within IU030. The input signal can be vertically and horizontally compressed or horizontally expanded by a large number of factors. Also the input signal can be processed by different noise reduction algorithms to reduce the noise in the signal. The noise measurement block determines the noise level of the input signal. The letterbox detection block finds the start and end line of letterbox pictures. This information can be used by a µC to calculate zooming factors and to control the IC for resizing the picture for a full screen display on 16:9 tubes.

Vertical expansion applies only to the master channel. It is located after the memory. For every output field, the scan rate converter generates a progressive frame. Thus for every output field period, a progressively scanned frame compensated to the correct motion is used for vertical expansion.

Changing coefficients and timing of vertical and horizontal filters within IU030does format conversion. On 16:9 tubes a vertical variable panning is added to the zoom formats.

VIDEO PSI

Video Picture Signal Improvement

2H post filter
The 2H post filters are used to suppress all unwanted frequency components beyond the useful frequency range after the up conversion process. The Y path includes a group delay correction circuit to fine-tune the overall group delay performance. In order to adapt the signal levels coming from the up converter additional amplifiers are added for all three paths.

PSI
Picture Signal Improvement (PSI) is completely performed inside the TDA9178 (IV100). The input signals are taken from the post filter outputs. All enhanced output signals are directly fed to the video processor inputs.
Since not all of the possible enhancement features of the TDA9178 are used in the ATC221, the following descriptions are the implemented functions.

Sharpness
The Sharpness function is a combination of the step improvement processor and the contour processor. Depending on the users "Sharpness" setting, a predefined value for the peaking control and the steepness control is selected. Due to the smart sharpness controller function large input signals are more enhanced by the step improvement processor while small input signals are enhanced by the peaking function. The video dependent coring function is always active and the coring level control is set to a fixed value.

Contrast expand
The contrast expand function is a combination of the histogram processing together with the adaptive black stretch function, the adaptive white-point stretching and the non-linear amplifier.

Green enhancement
Green enhancement is always on.

Skin tone correction
The skin tone correction is used to provide a kind of "auto flesh" function for NTSC signals. It is always on.

CTI
CTI is always on.

Video processing
The complete video processing is performed inside the High-level Output Processor (HOP) TDA9330H. Only a few external components are necessary to support the internal functions.

YUV input signals
The YUV input signals are taken from the corresponding outputs of the PSI (TDA9178) with the following nominal levels:

- Y = 1.00 VBW
- U = 1.33 Vpp
- V = 1.10 Vpp

2H/2.14H RGB inputs
These are the input signals coming from the DRI module in case of 2H/2.14H component or DVI sources. The nominal input amplitude is 0.7Vpp.

Saturation control
Saturation control is valid for the YUV and 2H/2.14H RGB inputs. The OSD/Text - RGB input is **not** affected.

Black Stretch
For video signals with a black level that deviates from the back-porch blanking level the signal is 'stretched' to the blanking level. The black level is detected by means of an internal capacitor. Black stretch is performed inside the PSI (IV100).

Contrast control
Contrast control is valid for the YUV and 2H/2.14H RGB inputs. The OSD/Text - RGB input is **not** affected.

RGB-TXT inputs
These inputs are used for OSD/Text signals. The nominal input amplitude for the OSD is 710mVpp.

Brightness control
Brightness control is valid for the YUV and both RGB inputs.

Beam current limiter
To avoid an electrical overstress of the Picture tube, it is necessary to limit the average beam current to a specific value. This value is depending on the tube size and tube type. To limit the average beam current, the contrast and brightness inside the video processor TDA9330H is reduced depending on the voltage at pin 43 (BCL) BCL control function
The beam current information is derived from the low end of the high voltage transformer.

The higher the beam current, the lower the voltage at CV270. The maximum voltage is limited by the zener diode DV270 to stay close to the BCL threshold if the beam current is low. The minimum (negative) voltage is limited through DL301/302/303.

DV271 is used to separate the slow time constant for the average signal and the fast time constant for the current transitions. With CV272 being discharged, the picture contrast and the brightness are gradually reduced. With the beam current receding and the voltage on CV270 rising, CV272 can again charge to its original voltage. The decay time is given by
RV271 and CV272.

Transistor TV277 uses the PKS (Peak Sense) information to reduce the contrast instantly if a critical current jump occurs. This threshold is fixed by the reverse breakdown voltage of DL301. Resistors RV276/RV275 limit the minimum emitter voltage of TV277 to ~2.0 V, enough to sufficiently reduce the beam current of a full white picture in a worst-case situation.

DV276 and RV277 are used to limit the E-B voltage of TV277. They do not contribute to the BCL function.

Peak white limiter
The control circuit contains a Peak White Limiting (PWL) circuit and a soft clipper. The detection level of the PWL is adjustable via the I²C-bus and has a control range between 0.65 and 1.0 VBW (this amplitude is related to the Y input signal with typical amplitude 1 VBW) at maximum contrast setting. The output signal of the PWL detector is filtered by means of an external capacitor CV279 so that the high frequency components of the video signal will not activate the limiting action. The contrast reduction of the PWL is obtained by discharging the capacitor of the beam current limiting input. In addition to the PWL circuit the IC contains a soft clipper function that limits the high frequency signals when they exceed the peak white limiting level. The difference between the peak white limiting level and the soft clipping level is adjustable via the I²C-bus and can be varied between 0 and 10% in 3 steps (soft clipping level equal or higher than the PWL level). It is also possible to switch-off the soft clipping function.

Continuous Cathode Calibration
To obtain an accurate biasing of the picture tube a “Continuous Cathode Calibration” circuit has been developed. This function is realized by means of a 2-point black level stabilization circuit. By inserting 2 test levels for each gun and comparing the resulting cathode currents with 2 different reference currents the influence of the picture tube

parameters like the spread in cut-off voltage can be eliminated. This 2-point stabilization is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages according to:

The feedback loop makes the ratio between the cathode currents Ik1 and Ik2 equal to the ratio between the reference currents (which are internally fixed) by changing the (black) level and the amplitude of the RGB output signals via 2 converging loops. The system operates in such a way that the black level of the drive signal is controlled to the cut-off point of the gun so that a very good grey scale tracking is obtained. The accuracy of the adjustment of the black level is dependent on the ratio of internal currents.

An additional advantage of the 2-point measurement is that the control system makes the absolute value of Ik1 and Ik2 identical to the internal reference currents. Because this adjustment is obtained by means of an adaptation of the gain of the RGB control stage this control stabilizes the gain of the complete channel (RGB output stage and cathode characteristic). As a result variations in the gain figures during life will be compensated by this 2-point loop. An important property of the 2-point stabilization is that the off set as well as the gain of the RGB path is adjusted by the feedback loop. Hence the maximum drive voltage for the cathode is fixed by the relation between the test pulses, the reference current and the relative gain setting of the 3 channels. This has the consequence that the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels the typical "cathode drive level" amplitude can be adjusted by means of an I2C-bus setting. Dependent on the chosen cathode drive level the typical gain of the RGB output stages can be fixed taking into account the drive capability of the RGB outputs (pins 40 to 42). The measurement of the "high" and the "low" current of the 2-point stabilization circuit is carried out in 2 consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100µA. When the TV receiver is switched-on the black current stabilization circuit is directly activated and the RGB outputs are blanked. The blanking is switched-off as soon as the loop has stabilized. This ensures that the switch-on time is reduced to a minimum and is dependent on the warm-up time of the picture tube.

The current divider RV342/343 is used to compensate a parasitic pulse error inside the HOP, which may cause a CCC loop flickering depending on the H-Position setting.

RGB output filters

The three passive RGB output filters (2. Order RLC filters) are used to eliminate high frequency distortions (mainly from RGB-TEXT/OSD insertions) before they are radiated from the connection cable to the CRT board. The filter outputs are buffered by NPN, emitter followers to keep the signals to the CRT board at low impedance and to shift the DC range of the RGB outputs down by one UBE. This shift is necessary since the high voltage video amplifiers on the CRT board do not allow any adaptation of the output DC range.

BSVM_Off signal

This signal is used to switch on/off the BSVM function depending on the user selection. Off = 0...0.4V, ON = 2V...3.3V

CONVERGENCE POWER SUPPLY

Convergence Power Supply

There are four secondary voltages generated by the convergence power supply. These are the ±53V and ±15V. Regulation is provided by the +15V via the opto-coupler IP50 to the SMPS control. The control (Switch off and control circuit) drives the power MOS transistor TP030 by adjusting the t-on time keeping the +15V well regulated. Due to the coupling of the switch mode transformer (SMT) all other voltages are regulated.

The *ON/OFF* is the +13V from the +UVERT. This voltage is used as the reference voltage for the secondary regulation and switch on/off the convergence power supply.

The startup circuit delivers a small current which loads the capacitor CP23 (Vcc). The zener diodes, DP23 and DP24, clamp the voltage across CP23 if the transistor TP24 is switched off. The stored energy in CP23 will be used for startup if the transistor TP24 is switched on via the +13V ON/OFF signal.
If TP24 is switched on, the driver circuit starts working and drives the switching transistor TP030.

Power stage
During forward cycle the switch mode transistor TP030 connects the primary winding of the transformer LP50 to ground causing current, for magnetization, to flow through the transformer. When TP030 switches off, there is a high dV/dt across the power transistor. This is caused by abruptly cutting off the high current through the SMT's primary inductance. This high dV/dt is undesirable for a number of reasons:

- High switching losses in the transistor
- Very robust transistor required to sustain simultaneously a high voltage and high current
- Cause of noise

Snubber networks, parallel to the switch mode transistor, can reduce the high dV/dt and maximum drain voltage of TP030. Between forward and fly-back cycle capacitor CP30 reduces the peak drain voltage and switch-off losses of the transistor TP030 and in addition limit the dV/dt in the transformer windings. To have a defined resistance between gate and source, the resistor RP33 is used.
The zener diode, DP31 suppress any high gate source voltage of the transistor TP030. With the resistor RP32, the source current of TP030 can be measured and used by the switch-off circuit.

Gate driver
The gate driver consists of a high impedance start-up and driver circuit.
The switch-on circuit is controlled by the secondary *ON/OFF*-voltage, because the SMPS is switched off during stand-by.
The start-up circuit RP10, RP11, RP12 and RP13 delivers current from the capacitor CP12, which is charged to the rectified main B+ voltage, into the capacitor CP23. At this point, the *ON/OFF*-voltage on the secondary side is not available and the transistor TP24 is switched off. If the main board is running and the ON/OFF-voltage comes up, current flows into the opto-coupler IP50 on the secondary side thus current flows from the base of TP24 via RP44 and CP49 on the primary side. With TP24 switched on, the stored energy in CP23 is used to deliver a current to the driver circuit. This start up circuit has high impedance and therefore very low power consumption. The driver circuit is connected on a positive fly-back winding (because TP24 is saturated) and delivers the current for the gate impedance. The positive fly-back voltage is rectified with the diode DP20 and charges CP23 via the resistors RP22 and RP23. The voltage across CP23 is used as Vcc of the driver circuit.
For safety reasons the resistors RP22 and RP23 suppresses peak voltages on CP24. Thus, the SMPS can go into a safe running mode if a short circuit on a secondary winding happens.
When the voltage difference between Vcc and the series connection RP25, DP38, DP37, and RP37 are more than the zener voltage of the two diodes DP37 and DP38, the transistor TP28 switches on. With TP28 conducting current flows from Vcc through the resistors RP28 and RP30 into the gate of TP030 turning on TP030.

Switch off circuit
The transistor, TP28 turns off the switch mode transistor TP030 via the resistor RP30 and diode DP30. TP28 holds the switch mode transistor off until the next cycle starts. The voltage drop on RP32, which is proportional to the drain current of TP030, is the control for TP28. TP27 speeds up the switch off time of TP28 and ensures that TP28 will not be switched on from the discharge of CP30.

FROSIN control (Free Oscillating Safe Intelligent)
The FROSIN control generates a delay after the finished fly-back cycle because of the storage behavior of the switch-off circuit. This is known as the oscillation cycle. The FROSIN-control holds the switch-off circuit active during the whole fly-back cycle and also for the oscillation cycle. During the oscillation cycle the drain voltage of the switch mode transistor TP030 oscillates down and the transistor switches on at around 0V. This FROSIN-control is done by the resistor RP48 and the transistor TP45 that are connected to the positive fly-back winding of the transformer LP50. The reference voltage on the emitter of TP45 is generated by the two diodes DP45 and DP46. To avoid a start up problem, the voltage after the switch on circuit is used with a time delay to generate this reference voltage. This insures that the transistor TP45 is always switched on if no oscillation happens. Therefore the transistor TP030 is protected.

t on-min control
The t on-min control guarantees proper switching of the switch mode transistor. Typical behavior for a self-oscillating power supply on reducing the load is the increasing of the switching frequency. Without t on-min control the frequency would rise up and the switch mode transistor TP030 would conduct very little current because of a very small t on time.
The t on-min control circuit (RP39, CP39 and CP40) holds the switch off circuit for a certain time, therefore; the transistor TP030 is switched on for a minimum amount of time compared to the off time.

Fold-back correction
The fold-back point is where the load on the output of the power supply is increased until the SMPS can no longer regulate and the secondary output voltages decrease. Generally, this maximum transferable power is due to minimum main B+ voltage more than maximum main B+ voltage. In order to compensate for this unwanted effect, a fold-back point correction circuit is used.
The capacitor CP42 is charged via DP41 and RP41 with the positive forward voltage edge, so that the voltage drop across the capacitor CP42 depends directly to the main B+ voltage. With minimum main B+ voltage the voltage at CP42 is at the minimum and the current, which flows from CP42 via RP42 to the switch off circuit, is also at the minimum. The influence on the base current of TP33 is low and the maximum drain current can be higher.
With maximum main B+ voltage the voltage of CP42 is at the maximum and the influence of the switch off circuit is high. In both cases the maximum power that can be transferred is nearly the same.

Soft-start circuit
The soft-start circuit modulates the drain current during start-up of the convergence power supply. The initial cycles are with very small drain current of TP030. The drain current increases until the nominal voltages are reached and the voltage regulation takes over control. Without soft-start the drain current would reach maximum value even for the initial cycles. This would stress the transistor TP030 and affect the reliability of other SMPS components in a negative way.
The soft-start capacitor CP49 is charged via DP49 and RP49. The voltage drop at CP49 generates a current through RP44 that has direct control of the switch off circuit. An additional advantage of the soft-start circuit is during a short circuit on a secondary voltage. In this case the soft-start circuit modulates the drain current to a minimum level and therefore the transferred power is also reduced to minimum level.

Over-voltage protection
If the positive fly-back voltage that is rectified with DP20 reaches more than 20% of normal running mode, the zener diodes DP23 and DP24 clamp the voltage across the capacitor CP23, thus the voltage drop across RP22 is high enough that the transistor

TP20 switches on. The transistor TP21 speeds up the switching behavior of TP20 and stops the SMPS.

Secondary voltage regulation

The current through the opto-coupler IP50 on the primary side is modulated with a current on the secondary side. This is done by transistor TP90 and TP91 that is used as a voltage comparator.
The reference voltage of the secondary regulation is generated from the ON/OFF-signal with the resistor RP87 and the zener diode DP87. The stabilized voltage of the diode DP87 is filtered with capacitor CP86 and CP87. TP91 works as voltage comparator and collector current flows if the base voltage is higher than the reference voltage on the base of TP90.
The capacitor CP91 and resistor RP93 define a time constant of the regulation loop.

For example:

1. The secondary voltage +15V increase a little bit.
2. The voltage at the base of TP91 increases.
3. TP91 will be more conductive, so that the current into the resistor RP91 increases.
4. As the voltage drop across RP91 increases, the base / emitter voltage of the transistor TP90 decrease.
5. As a result of a lower base / emitter voltage of TP90, the current into the opto-coupler decreases.
6. The current through the opto-coupler on the primary side decrease also.
7. The negative current from the base of TP24 via RP44 decreases thus the voltage at the base of TP24 is higher.
8. The switch off circuit allows less drain current of the switch mode transistor TP030.
9. This decreased drain current causes less transferred power with the result of decreased secondary voltages.
10. Now the regulation loop is closed.

CONVERGENCE SIGNAL BOARD

Convergence Signal Board

Power regulation and watchdog
Because STV2050A (IK01) is operating with 3.3V there is a 3.3V regulator (IK05) on the convergence signal board CSB. IK05 is a LD1117V33 low drop device. The circuit consisting of TK26, TK27, and TK04 is the watchdog circuitry, which creates the reset signal for IK01 in case the 3.3Vsupply is below 2.5V or above 4V.

I²C bus
At BK10 the I²C bus from the TV chassis is connected to the CSB. Parallel to BK10 is BK11 for direct factory access to the convergence CPU for alignment. Also connected to this bus is the EEPROM IK07, which is used to store the factory alignment data and parameters for the convergence auto-alignment. The EEPROM is write protected if the test pin is held high. The test pin is connected to pin 34 of the STV2050A. To allow writing into IK07 the test pin is switched low. TK47 and TK48 build a level converter from 5V to 3.3V and act as a buffer between the bus and IK01. This buffer is needed when IK01 is not supplied to avoid bus pull down.

Grid generator
At pins 16, 17 and 18 of IK01 there are the convergence grid signals. The emitter followers TK20, TK22, and TK24 buffer the convergence grid signals to drive 75 inputs. The output is at BK01 and goes to the DRI board to be entered as 2H RGB signal. At pin 10 of IK01 a fast blank signal is available which is a TTL output.

Synchronization
To synchronize the convergence, H and V sync pulses are entered at BK02-2,1 coming from the adapter board. The H signal enters IK01 at pin 27 after passing a level converter build around TK09. The V signal enters at pin 28 with a voltage swing of 3.3V coming from the adapter board.

Convergence data storage
The EPROM's IK08 and IK15 are used to store the convergence data. In each of them there is place for one set of dynamic data and 3 sets of register data. After the reset pin is released IK01 will automatically read the content of IK08. If the checksum test is ok, the convergence outputs are switched on with this data. Both EPROM's are connected to the master I2C bus at pin 1 and 2 of IK01. BK15 is a connector to access this bus for Lab use only. The master bus is operating with 3.3V.

Dynamic focus
The STV2050 produces a programmable vertical rate parabola signal. This signal is used for the vertical portion of a dynamic focus control. The DAC outputs at pin 68 and 69. The Opamp IK03 converts the DAC currents into a voltage. After the filter CK31, RK06 the parabola signal is connected to BK02 to be used on the adapter board.

Convergence output stages
The convergence signal outputs are located between pin 45 and 66. The Opamp IK03 converts the DAC currents into a voltage. They are designed to provide a max swing of ±2.5V. A simple integrating filter with two capacitors at each input of the Opamp is used to smooth the output signal. The STV2050 has internal digital filters. The output signals are sent to the power amplifiers via BK04.

Electrical stability loop
This feature is to keep offset and gain of the convergence system stable over temperature change and aging. During one line of the vertical retrace a reference signal is produced by the STV2050. The feedback signals at BK16 are an image of this reference signal after passing the output Opamp on the CSB and the power stage on the CAB. At the comparators IS02 and IS03 the feedback signals are compared with target values that are also produced by the STV2050. The signals for the target values are OGAV for vertical and OGAH for horizontal. The compared result is then read by the STV2050 at PORTA, PORTB and PORTC. The loop is working in a continuous sequential mode where first the offset is checked for the vertical

channels. Then the offset for the horizontal channels is checked. Then the gain for vertical channels is checked and finally the gain for horizontal channels. The loop algorithm inside the STV2050 corrects the offsets until it is zero by adding or subtracting a value in the digital processing. The gain is corrected by changing a multiplication factor in the digital processing. The precision of the loop is depending on the band gap reference inside the STV2050 and some resistors, which are all 1%.

8-sensor auto-alignment

Automatic alignment of the convergence uses 8 photo sensors hidden in the screen frame of the PTV. They are in parallel and connected to BS01 on the CSB. The hardware for this feature is split in three parts: First the optical sensor signal is filtered and amplified by preamplifier IK02. At the input, TS50 used to switch an integrating capacitor in parallel to the input. This is necessary when doing the blue alignment. The blue phosphor produces very high and short light pulse while red and green are doing small and long light pulses.
The second stage is built around TS36 and TS39 Schmitt trigger circuit. It triggers when the amplified opto signal is high enough. The output of this stage goes via TS41 to the OPTI pin 72 of IK01.
The third stage is built around TS48. It converts a pulse with modulated signal from the OPTT pin 74 into a current, which can shift the trigger level at TS36 up or down. This is used because of the different brightness conditions between center and corner on the screen.

Circuitry associated to the STV2050

- **Oscillator for master bus clock**: RK 50 connected to pin 22 and CK50 – RK52 connected to pin 21 form an oscillator for the clock of the master I²C bus.
- **PLL filter:** The RC combinations connected to pin 24 and pin 25 are the filters for the PLL. The filter at pin 24 is for 1H operation and the filter at pin 25 is for 2H and higher.
- **Reference:** RK25 at pin 54 is setting the reference current for all analog cells inside the chip. It is also the point where the band gap can be measured and aligned. CK26 at pin 55 filters the reference.

CONVERGENCE ADAPTER BOARD

Convergence Adapter Board

Vertical pulse generator

The convergence generator IC needs a 3.3Vpp vertical pulse, locked to the vertical deflection. The signal is called **Vsync** on BV12-1.

Horizontal fly-back pulse

The convergence generator IC needs horizontal sync. This is taken with RV72 and RV73 from the collector of the horizontal switch. This signal is the best reference of the deflection current. The signal is called **H-Flyb** on BV12-2.

Scan loss blanking

Main purpose of this circuit is to avoid "burned tubes" in case of missing either vertical or horizontal deflection. To achieve it, there is a detection of the vertical and horizontal pulses. If one or both are missing a very fast switch of the Video amplifier to black occurs to prevent tube burn.

RV50 and CV50 serve as high impedance decoupling of the vertical pulse. DV50 limits the positive voltage to 0.7V and DV52 rectifies the voltage to a negative value filtered by CV52 and given to the base of TV50. The base is also supplied by RV54 with a positive voltage. These two voltages are, during normal operation, in balance meaning the base voltage is roughly 0V and the collector is "positive". Due to RV56 the base of TV52 is positive and TV52 is on, that means the **S.L.B**. line has no voltage to activate the blanking of the Video amplifier IC on the CRT's. If the vertical deflection fails RV54 will supply the base of TV50, which will immediately ground the base of TV52 and the collector goes high. In other words the +12V coming from RV57 is able to activate the **S.L.B**. line and, through TV53, the **ABL** line of the video / scan processor will be set to 0.

The same functionality is given for the horizontal fly-back pulse taken with RV51, CV53, and DV53. RV52 and RV53 are used to keep the status. If a failure occurs, the base of TP50/TP51 will be more positive.

+240V supply current sensing and beam limiter
NOTE: *Current sensing "switch OFF" function is only working in acquisition mode or during start up.*

In case of overload or defects on the CRT boards the current in the +250 supply can cause safety or reliability problems; therefore, current must be monitored. The critical level is 120mA. If the critical level is exceeded, the beam current needs to be reduced or shutdown the set. The voltage drop at RV01 and RV09 generates the necessary base emitter voltage to switch on TV01. This current is given to the base of TV04. The collector of TV04 pulls down the RPSAFETY line on the power deflection CBA thus switching off the main power supply (same line is also used by the **S**mall **S**ignal **B**oard). CV01 filters spikes during normal operation of the set. DV01, DV02 and DV03 are clipping the maximum voltage at RV01/RV09 and also protecting TV02. The time constant before activating is given by RV11 and CV03. TV04 is also used to control the system voltage with RV14. If the system voltage is higher than +200V (nominal 137V), TV04 will conduct pulling the safety line to low level.

The switch OFF, of the main power supply is disabled during ON TV mode. The disable is done with +6V coming from the IHVT. TV40 disables this function by shorting base-emitter of TV04.

Beam limiter function:
Additional to the switch OFF functions the sensing circuit is also used to reduce the beam current in case of very high picture content to avoid overheating the Video amplifier IC's. TV02 and TV03 reduce the beam current by pulling the ABL line to low. The generated output signal goes to the ABL-pin of the video / scan processor on the small signal board.

+6V supply
The IHVT delivers a horizontal pulse (60 Vp-p) called V_SAW at pin 8. This voltage is rectified through DV90 and filtered with CV90. CV91 suppress the peak current caused by the diode during switch ON and OFF. LV90 is needed to filter residual high frequencies, which can cause noise on the picture. The rectified voltage is about +6V and is used in the convergence signal board (CSB) to supply the convergence IC with 3.3V via voltage regulator IK05.

+12V supply
The +15V coming from the convergence power supply is used to supply IV10. This IC generates a very stable +12V, which is used by all three CRT CBA's for the video amplifier IC and other circuits around the video stage. CV11 and CV12 are used to prevent oscillation of IV10.

Deflection signal distribution
Both horizontal and vertical deflection signals must be split into three signals for the three independent tubes. The yokes of the horizontal deflection are parallel connected. The vertical deflection yokes are in series. The horizontal frequency is 2H or 2.14H and the vertical frequency is 120Hz, progressive mode 60Hz.

1.1KV generator
The 1.1KV is generated for the supply voltage of the dynamic focus amplifier. The circuit consists of RV85 for current limitation; DV85 and DV86 to rectify the horizontal retrace pulse and CV85/CV86 for smoothing the rectified voltage.

Dynamic focus system
Working principle:
Depending on the vertical position of the beam the focus voltage changes to a bit more (corner) or a bit less (center) focus voltage. This is also valid for horizontal position of the beam from line start to line end. A variation of 580V focus voltage improves the sharpness over the entire screen. The dynamic focus voltage consists of a vertical and a horizontal section.

The horizontal dynamic focus voltage is generated in the transformer LV80 by a resonant effect. The saw tooth current of the deflection usually generates voltages known as fly-back peaks. Integrating and smoothing a mixture of sine wave and peak signals generate the parabola-like voltage. A part of the same signal is also used for the detection of horizontal scanning. The horizontal parabola has a voltage swing of 580V pp ±20%.

The ATC221 has to work in two horizontal frequency modes, 2H and 2.14H.
The frequency variation of ~2.3Khz causes a big horizontal parabola change of roughly 30% this is not acceptable in terms of sharpness and also of safety. To adapt the horizontal parabola to both frequency modes the tuning capacitors CV81 and CV82 have to be switched in. The MOSFET transistor TV92 is conducting in 2H (CV81 + CV82) and open in 2.14H (only
CV81). The opto-coupler is controlled by a line called "480_ON" coming from the power deflection CBA. TV90 is used as an inverter and TV91 is switching ON/OFF.

Function:

- **2H**>>>480_ON line is high>>>TV90 ON>>>TV91 OFF>>>opto-coupler open>>>TV92 ON because of voltage at the gate supplied by DV92, RV98, RV97 and as result CV82 is parallel to CV81.

- **2.14H**>>>480_ON line is low>>>TV90 OFF>>>TV91 ON>>>opto-coupler conducting>>>TV92 OFF and as result only CV81 is working.

The **S.L.B.** information, which is used to blank the CRT's in case of missing deflection, is generated with coupling to the horizontal parabola winding. If changing the horizontal frequency reduces this voltage, the Video signal will be unnecessary blanked.

The vertical parabola of the dynamic focus is generated in the convergence IC. This parabola voltage is amplified by TV80 to a high level of ~600Vpp. The vertical parabola modulates the horizontal parabola generated in the transformer. The common signal is given to the focus block to correct focus of the beam over the entire screen.

CCC-Loop: Continuous Cathode Calibration
All current information coming from CRT-boards is given to the video / scan processor. In order to protect the CCC-input of the video / scan processor, the voltage is limited by TV20 at a level of 7V. For equalizing the adjustment range of the current-loop there are current-dividers or current amplifiers on each CRT CBA (DCR-red, DCR-green and DCR-blue). The different values in efficiency of the phosphors and sensitivity of the human eye must be compensated for. The red current channel is amplified by TV21, compensated and measured with TV22 and RV21.
The green current channel is attenuated by RV23, RV24 and RV25.
The blue current channel is attenuated by RV27, RV28 and RV29.
The summarizing is done with RV21, RV91 and RV92 to the output at BV05-9.
The clipping of the output level, for protecting the HOP-IC is added separately with DV20, DV21 and DV22, coming from TV20.

Peak current limiter
The peak current levels are separated by diodes: DV23, DV24 and DV25. Because the current level is limited, the video IC is protected. The voltage level at the resistors RV22, RV26 and RV17 indicates the actual beam current. Two separate measuring points at this position allow controlling the peak current for servicing and adjustment. These signals are summed by transistor TV30 and the threshold level is selected by RV30, RV31 and RV45 so the peak current is selected at 6mA. TV31 does the voltage gain and signal inverting. TV32 generates the charging current for the filter group RV37. Pre-biasing by RV35 and RV36 helps for better response during channel change. The output buffer for a longer time constant is TV33 and TV34. The DC-level at the Emitter of TV35 is given to ABL-input of the video / scan processor on the small signal board.

The Video signal distribution, consisting of the connector BV05 as supplier, comes from the small signal board and the connectors BV06, BV07 and BV08 feeding all signals to the corresponding 3 CRT boards.

CONVERGENCE AMP

Convergence Amp

The convergence amplifier assembly contains six amplifiers and the watchdog circuit. There are three identical amplifiers for vertical and two identical amplifiers for horizontal. The sixth stage is the green horizontal stage, which does not have the booster stage for negative signal peaks.

Amplifier stages
One output amplifier consists of two stages. The pre-amplifier/driver and the power output stage. The pre-amplifier consisting of an integrated op-amp is the first stage. It is supplied with ±13V and generates the input signal for the driver stage. The reference level for the op-amp is zero at the non-inverting input IA10-3. At the inverting input IA10-2 there are three signals summed together:

- The input signal via RA01 coming from the CSB
- An image of the output current, which is sensed at the reference resistor RA09
- The output voltage via RA13-CA10

NOTE: *Do to identical circuits in the convergence amp stages, only the Red vertical stage will be used for discussion.*

The power output stage provides the current to drive the convergence yokes, which are part of the deflection yokes. The low frequency components of each convergence signal are driven under resistive load conditions. The higher frequencies are driving the convergence current under inductive load conditions. The power output stage has to work under both conditions.

To reduce power dissipation, the amplifier is supplied with four voltages. During the main part of the trace time, the output current is supplied from the lower voltages ±15V. But during retrace time, the output currents are fast changing and the higher supply voltages (±53V) are needed. The output stage (power transistors in Darlington configuration) has, for each polarity, two transistors in series. The transistors TA02 and TA03 are working with ±15V supply voltage during 80% of the time, when the picture is shown. Only at the borders and during retrace time the booster transistors TA01 and TA04 are switching on the higher supply voltages. During this time the lower supply voltages are switched off by diodes DA05 and DA06.
The six-volt level at the zener diodes DA08 and DA09 gives the time of crossover. This level avoids saturation and stepping effects. The power amplifier is a non-inverting stage. It takes the voltage swing from the pre- amplifier and increases it to the output swing with a voltage gain of six. This is determined by the resistor network RA07 and RA20 parallel to RA04. The voltage gain configuration is done with TA06 and TA05. The biasing of the complementary power output, with three diodes DA01, DA02, and DA03 is high enough to avoid B-curve distortions thus avoids ICEo current temperature drifts. The biasing of the zener diodes for the supply switching is generated with clamping diodes DA10 and DA11. The current is limited with RA08 and RA15 for the zener diode and the base current of the booster transistors. The time constant of discharging is given by the capacitors CA07 and CA08. The smaller capacitors CA15 and CA16 are for filtering spikes. The AC coupled feedback with RA13 and CA10 optimizes the settling time, reduces overshoots and ringing caused by the inductance of the convergence coils.

Watchdog
The watchdog circuit has three protective functions:

- Start the convergence power supply only if the + and -13V are present and stop the power supply when they drop
- Stop the convergence power supply in case of any overload condition during startup or normal operation where the + and -15V are not reaching their normal value
- Ensure a startup where the + and -13V are present before the ±15V. This avoids uncontrolled currents inside the power stages

Sensing of the –13V is done by RW12, RW13 and TW13. If the –13V is smaller than ~8.75V the base

of TW13 is at 0.7V and TW13 will conduct. Every time when TW13 conducts it means that TW14 is non-conducting and TW19 is blocked, thus the voltage is not supplied at the PS_ON line and the power supply is off.

Sensing of the +13V is done by RW10, RW11 and TW10. The base of TW10 is at 2.6V or lower if the +13V is lower than ~7.5V. In that case TW10 conducts and drives enough current to switch on TW13 stopping the power supply.

Presence and level of the + and -15V are checked by RW01, RW02, RW04, RW06, TW01 and TW02. If the voltages are too low than TW02 will be non-conducting. CW05 will be charged through RW05 and if the charge reaches ~8V it will trigger DW12; therefore, TW13 conducts stopping the power supply. The delay by CW05 and RW05 of ~0.8 seconds is needed during startup to cover the rise times of the voltages from the power supply.

DV CRT CBA

CRT Board

High bandwidth board with TDA6118

The RGB amplifying stage is based on 3 integrated circuits IB001, IB002 and IB003. The three independent high voltage amplifiers provide a small signal bandwidth of 22MHz (40Vpp) and a large signal bandwidth of 16MHz (100V). The gain of the IC is selectable via pin 2 (GS, Gain Select). A fixed gain is used to compensate for the attenuation of the terminated delay lines FB121, FB141 and FB161. The transistors TB120/121, TB140/141 and TB160/161 are emitter followers and provide coupling to the output stages with low impedances and low stray capacitances.

BSVM Coil

The resistors, RG002, RG003 and RG004 sum the R-G-B signals to generate a 'Y-signal'. This Y-signal is amplified by TG001 with the active load TG005. The push-pull emitter followers TG002 and TG004 provide a low impedance output and a symmetrical signal for the differentiation. The differentiation circuit consists of the components CG005, RG012 and RG013. TG006 and TG007 are the output stage, which drives the BSVM coil (connected to BG003). This auxiliary coil is located under the beam bender on the tube neck. The inductance is approximately 3µH. A damping circuit RG042/CG048 prevents current overshoot due to the inductance. The transistor TG011 reduces via the Fast Blank signal the BSVM action for RGB insertions to avoid text disadvantages.

AFTERGLOW SUPPRESSION

Referring to the schematic diagram CB003 is charged up to 200V. During normal operation of the TV set, constant current flows through the resistor RB002 and the diode DB004 so that the G1 voltage through RB004 is set to 0.7V

NOTE: *TB001 is always switched on, except during G2 alignment.*

After switching off the TV set the +200V supply voltage goes to zero and because of the charged capacitor (CB003) the voltage at the anode of DB004 becomes negative. Therefore DB004 is

switched off so that the negative voltage at G1 is present for more than a minute and causes the screen to be blanked during the time where afterglow effects can occur.

The CRT board has two functions:

1. Video amplifier with blue gamma correction (Blue CRT only), signal clipping for green and blue.
2. BSVM deflection circuit.

Other components are spot killer, G2-alignment and filter elements for the CRT.

Video Amplifier

The amplifying stage is based on the Integrated Circuit **TDA6120Q** (IB101, IB201 and IB301). The TDA6120Q is a single video output amplifier contained in a plastic DIL-bent-SIL power package. The device uses high-voltage DMOS technology and is intended to drive the cathodes of High Definition CRTs.

PTV CRT

Blue Gamma Correction (*Only on the blue CRT board*)

The gain of the blue CRT board must be higher for higher video or intensity levels, otherwise the grey scale is not linear because the efficiency of the blue phosphor is not linear and drops in the range of medium and higher levels. The gain is switched in two steps in order to achieve an optimized gamma response.

TB332 (first step) is switching pin1 of TDA6120 via RB330 to lower impedance when the first insertion level is reached. TB331 (second step) is switching RB331 when the second level is reached. The gain will be increased in 2 steps.

The black-level tracking circuit, depending on the blanking level of the Input-signal of IB301, generates the insertion level.

Video-Signal Clipper (*Only for Green and Blue CRT board*)

To limit very short peaks that are not limited by the peak current limiter, the green and blue video signals are clipped at the level of the action of the peak current detector. This clipper function is realized by TB*12 **acting on the video-signal input of** IB*01 **pin2. The clipping level is selected by** RB*28 **and** RB*37 **depending on the black level as reference. Because the higher efficiency of the red phosphor, the signal level on red CRT is much lower, therefore; no clipper function is needed for red signal.**

NOTE: **** indicates 1 for Red CRT, 2 for the green CRT and 3 for the red CRT.***

Beam Current Measurement

It is necessary to provide the actual beam current information to the CCC (Continuous Cathode Calibration) loop in the video controller (**HOP TDA9330**).

The CCC-loop (or two point stabilization loop) is an auto-tuning loop that stabilizes the black level and the cathode drive level of each CRT.

The actual beam current information is also needed for the spot field limiter on the Adapter-board.

The CCC-loop can be divided into two loops:

- Black level stabilization loop (cut-off compensation)
- Cathode drive stabilization loop (gain compensation)

Besides these two loops a leakage current compensation loop is present. This loop compensates the total offset current of the three picture tubes and the offset of the three amplifiers.

TB*40 acts as base grounded amplifier for this work.

DB*40 and **CB*40** are shorting this stage for high frequencies.

RB*51 shortens the **TB*40** for currents below 100uA.

In this case the internal measurement circuit (pin7) takes over the measurement.

RB*44 acts as limiting resistor, also with **CB*44** and **RB*45** as high frequency filter, to avoid over shooting in the measurement and ringing in the video signal.

NOTE: * *indicates 1 for Red CRT, 2 for the green CRT and 3 for the red CRT.*

Spot Killer Circuit

The spot killer is triggered by a falling heater-voltage. TB*61 **is biased by the rectified Heater-voltage. In case of missing Heater-voltage** TB*61 **is blocked and switches via** TB*66 **the inverted U VIDEO (+230VAr) (stored in** CB*66**) to G1.**

A high negative voltage (-240V) at G1 blocks the beam-current.

The discharging time is done with the time constant of **RB*66** and **CB*66**, till the temperature of the cathode has dropped.

If AC is switched off, G1 drops to -240V and the cathode to zero.

The blanking effect is determined by the difference of cathode-voltage and G1-voltage.

DB*62 prevents the +12V (stored in **CB*62**) from discharging in case of missing +12V.

DB*64 prevents **CB*66** from discharging in case of missing U VIDEO (+230VAr).

BSVM Circuit

The sharpness impression is usually improved by increased video voltage for higher frequencies. Higher current is always defocusing the beam and reducing the improvement. Therefore it is better not to influence the video signal, but to move the beam in the horizontal direction. This additional horizontal deflection accelerates the horizontal moving at the beginning of a video slope and delays it at the end of the level jump. The beam is in the centre of the video signal slope longer and raises the visual impression by increasing the intensity.

BSVM pulse generation

NOTE: * *indicates 1 for Red CRT, 2 for the green CRT and 3 for the red CRT.*

TG*35 separates the BSVM-input-circuit from video-input in order to avoid any influence on signal-amplitude or bandwidth of the picture signal. In order to avoid saturation effects of the BSVM output amplifier the incoming signal is limited by a clipper circuit. (**DG*36**, **DG*37**, **CG*37** and **RG*37**)

TG*11 shuts off the input-signal for BSVM circuit and reduces via the Fast Blank signal the BSVM action for RGB insertions to avoid visible text distortion. The resistor **RG*41** provides the input-signal to the amplifying transistors **TG*01** and **TG*05**. **TG*01** and **TG*05** are acting as push-pull voltage amplifier. **TG*02** and **TG*04** are providing a low impedance output.

BSVM output amplifier

TG*06 and **TG*07** are the output stage which drives the BSVM coil (connected to **BG*03**). This auxiliary foil coil is located on the tube necks. The inductance is approximately 4µH. A damping circuit (**RG*42 and CG*48)** prevents overshoot of the coil. Because of the circuitry and the small number of components, the signal delay time is about 40ns and is appropriate to the delay time of the video processing (including the video-delay-line).

AUDIO OVERVIEW

Audio General description:
The audio circuit is on the small signal board and includes the following components:
MSP3441G (IA001): Demodulation of the Sound IF signal for the BTSC standard, identification of mono, stereo and SAP, switching of 4 AV inputs and outputs for monitor out (fixed level), monitor out (variable level), headphones, subwoofer and L/R channels, Virtual Dolby processing.
TDA7269 (IA002): Power amplifier for the left and right speaker signal.
TS482D (IA003): Stereo headphone amplifier.
MC4558CD (IA180 and IA181): Buffers for the variable monitor outputs (left, right, subwoofer).

Multi-standard Sound Processor: IA001
The **M**ulti-standard **S**ound **P**rocessor (MSP3441G) contains the full TV sound processing, starting with analog sound IF in, to processed analog AF out. The MSP demodulates the BTSC multiplex signal and the SAP channel. The sound IF input (ANA_IN1) needs no pre filtering. After the Automatic Gain Control (AGC) the signals are A/D converted. The demodulation is done in digital form. The four stereo AV inputs (AV1, AV2, FAV, DRI) and the FM/AM input contain pre volume settings to compensate for level differences. In the switching section, every input can be switched to every output. The speaker output path (DACM_L/R pins 20, 21) is used to carry the left and right channels to the variable monitor outputs and to the internal power amplifier IA002.
In this path the MSP offers several software controlled sound features:

- Volume in the range of -114 to +12 dB
- Five band equalizer or bass/treble with a range of ±12dB
- Loudness from 0dB to +17dB
- Balance control
- Stereo base width enlargement and pseudo stereo effect
- Automatic volume limiter
- Low pass / high pass filtering for subwoofer usage
- Virtual Dolby Surround processing

The fixed monitor output path (SC_1_OUT_L/R pins 28, 29) provides a fixed level output to an external amplifier.

The headphone output (DACA_L/R pins 17, 18) is used to supply the headphone amplifier (IA003). At this output, volume and bass/treble effects are available.

A subwoofer output (DACM_SUB pin 23) is also available with level and frequency response adjustments.

For the internal oscillator the MSP needs an external 18.432MHz crystal at pins 54, 55 (XTAL_IN/OUT).

There are two digital output pins D_CTR_OUTI/O pin 60 and C_CTR_OUTI/O pin 61 that are used to generate the Subwoofer and L/R mute. These are user- controlled functions from the audio menu.

The Power-On-Reset (RESETQ pin 16) is controlled by the microprocessor with a signal called RESET_AUDIO.
All functions are I²C bus controlled (I2C_DA, I2C_CL pins 1, 2).

Power amplifier: IA002
The stereo power amplifier IA002 receives the left and right signals from the MSP at DACM_L/R and delivers the amplified signal to the connector BA980. IA002 runs with a symmetrical power supply (±UA), which is delivered at BA010. It includes two class AB amplifiers and a mute circuit that is activated by TA130 and some additional components. Mute is activated if the voltage difference between the pins 3 and 5 of IA002 is lower than 6V and higher than 2.5V. Between 2.5V and 0V difference the IC is in standby mode where the final stage is muted. Mute is deactivated if the difference between these pins is higher than 6V. The power amplifier has an internal thermal shutdown and short circuit protection.

Headphone amplifier: IA003

The headphone amplifier IA003 is a TS482. It amplifies the signals coming from the MSP at DACA_L/R and delivers the signal to BA009.

Mute control:

There are four different mute signals:

1. **MASTER_MUTE:** This signal comes either from the bus expander (IR006) or from the power fail circuit. It mutes the L/R amplifiers and the subwoofer amplifier. If the main voltage disappears, this mute is active as soon as possible in order to avoid pops.
2. **L/R_Mute:** Comes from the MSP and mutes the L/R amplifier. It will be active, if the user has selected "external amplifier Left/Right".
3. **Mute_subw.:** Comes from the MSP and mutes the subwoofer amplifier. It will be active if the user has selected "external subwoofer".
4. **AUDIO_STBY_MUTE:** This info comes from the microprocessor and sets the L/R amplifier together with the MASTER_MUTE into standby mode.