CIRCUIT OVERVIEW

System Control

The CTC195 chassis is a digitally controlled television receiver. The system control circuit governs the entire operation of the television. The control circuits are not only responsible for turning the set on and off, but also for aligning the different circuits such as deflection and signal. Adjustments that were aligned with a potentiometer on other chassis are now aligned digitally via the microprocessor with the values stored in the EEPROM. This means the values stored may be changed by invoking the correct parameters for the EEPROM to allow writing to it, then writing the new values. The EEPROM will hold all values written to it even during and after loss of power. The EEPROM also stores certain user settings. This ensures that these settings will not be lost during long power outages.

The CTC195 Control System is based on a single 8-bit ST9296 Microcomputer. The micro has several new features over others used in the past. The new features include an IR Preprocessor, Sync Presence Detector, Frequency Multiplier for the CPU Clock, a UART, a Closed Captioning Decoder, 3 A/D inputs, Digital Convergence, CRT Control circuitry and an On-Screen-Display that supports 3-bit D/A outputs.

The I²C busses communicate with the majority of the digital devices. The standby buss is connected to the main EEPROM and the decoder interface microcomputer, when present. The run bus is connected to the remainder of the I²C devices. The Standby and Run busses run at approximately 50 kHz. The standby bus is always active, while the run bus is only active after power up.

The CTC195 main chassis devices that are controlled by the I²C bus are the main EEPROM (U3102), Main Tuner PLL (U7501), Stereo Decoder (U1600), T4-Chip (U6201), Audio Compressor (1501) and the Video Switch (U6901). Other devices include the PIP EEPROM (U7903), PIP DAC (U7902), PIP PLL (U7401), Gemstar, Digital Convergence and FPIP (U8100).

User Settings

During shutdown, all current user settings will be stored in EEPROM. Most settings now are written to the EEPROM as they are changed, with no shadowing of the EEPROM in RAM. It is no longer necessary to guarantee RAM retention with this system configuration. The microprocessor has approximately 10ms to allow any writes to the EEPROM in order to store the present condition of the TV.

EEPROM and T4-Chip Power Control

The microprocessor controls the power to the EEPROM (U3102) and T4-Chip (U6201). After the microprocessor is reset, U3101 pin 20 goes LO turning on Q3109. This supplies 5V to the EEPROM (U3102). The T4-chip uses a 7.5 volt supply derived from the +12 Volt Run supply. A simple voltage divider reduces the 12 volt to 7.5 volts. Although the 7.5 volt supply is labeled "Standby" in the service literature, it is actually not active at all times. 7.6V to the T4-Chip is available only when the run 12V supply comes up. The power control circuitry of the microprocessor gives it the ability to turn off the power to the EEPROM and T4-Chip in the event one of the devices locks up. Because the micro goes through a power up sequence every time the instrument is turned on, the T4-Chip and EEPROM are turned off and then back on each time the TV is turned on. This resets the EEPROM and T4-Chip each time the TV is powered up.

Main Power Supply On/Off Control

The CTC195 chassis are turned on and off by controlling the main power supply *and* the T4-Chip. When the power cord is first connected to AC, standby supplies come up, Q3503 resets the micro by sending a HI to pin 51. Pin 20 then goes HI applying power to the EEPROM. The microprocessor then checks the EEPROM address for an acknowledgment. If the EEPROM is acknowledged, the microprocessor waits for the next command. If there is no EEPROM acknowledgment, the microprocessor continues to try to contact the EEPROM. This can be seen on the oscilloscope as continuous data activity on the I²C data line.

With AC power already applied to the set, and the power button is pressed or a remote control ON command is received, pin 20 goes momentarily LO resetting the EEPROM. This makes certain it is a normal state. Immediately the +16 Volt Standby Supply dips. During this time, the video and audio mute lines are low so that no picture or sound can be processed accidently by circuitry having some residual voltage supply remaining.

Once circuit stability has been established the OSD and tuner are allowed to function. As soon as a channel is captured, the video blanking is turned off allowing video to pass normally. When the high voltage supplies have reached their normal operating voltages, a picture will appear on the CRT.

Power Down

When either the power button is pressed or a remote control OFF command is received, the micro immediately mutes the video. The volume level is reduced, then the speakers are muted and the T4-Chip is ordered to stop deflection. The Run/Standby (pin 19 of U3101) is turned to Standby, shutting down the 5 and 12 volt run supplies, shutting down the instrument.

Batten Down the Hatches

The batten down sequence is invoked during any problem sensed by the microprocessor and acts to save off all settings and alignments, plus an error code to cue the technician as to the possible cause of the failure. It's most important function is to shut down the set as normally as possible during loss of incoming AC, whether long term or short term.

The batten down sequence will occur when the standby 16 volt supply drops to about +9.5 volts during a power up cycle, or to about 2 volts below the reading of the standby D/A on pin 39 of the microprocessor, U3101 1.5 seconds after power up or 1.5 seconds after power down.

Some power supply dip or surge is expected during start up and shut down, so 1.5 seconds was chosen to make certain any ringing or dipping of the supply had stabilized before taking a reading that might lead to a batten down sequence, when the only thing occurring was a normal power supply dip or surge during start-up or shut down.

Anytime after the 1.5 second power on cycle, if the 16 volt standby supply falls below approximately 9.5 volts the batten down sequence begins. The first actions are to reduce drain on the residual power supply. The speaker outputs, run supplies, OSD display and any other circuit not necessary to saving information to the EEPROM are cut loose. All instrument information is written to the EEPROM during the next 10 milliseconds. After that, the EEPROM is disabled by pin 20 of the micro going HI. When this sequence is

CIRCUIT OVERVIEW (Continued)

completed, two things may happen depending upon the condition of the standby supply. The 15 second timer on pin 17 tells the micro how long the power has been disconnected. If it has been less than 15 seconds, the set is powered up with no loss of data, including the clock time. If it has been greater than 15 seconds, the clock time is lost. When the EEPROM has stabilized, one more write containing device status after the batten down the hatches routine started is written.

Feature Auto Detection

Certain features of the CTC195 chassis family are auto detected. The microprocessor checks for the appropriate hardware and if detected, supports that feature. If not, it assumes that feature is not supported in the chassis and runs without it. In these instances, the set will not shutdown, but will run minus the feature.

Microprocessor Input Signals

Certain video and deflection signals are input to U3101. Selected video out is buffered by Q3306 and applied to pin 13 for the closed caption decoder contained within U3101. Video out of the T4-Chip is buffered by Q3101 and applied to pin 38 for tuning sync. Horizontal and vertical deflection pulses are applied to U3101 pins 24 and 25 respectively to provide a synchronization reference for correct positioning of the on screen display.

Keyboard Interface

The keyboard interface is the same interface as used in the past. Key drive line KD1 drives the POWER, VOL. UP and VOL. DN. When one of these buttons is pressed, KD1 pulses the corresponding sense line LO. U3101 detects which button has been pressed by monitoring the key sense (KS) lines for the KD1 pulse. The other three switches pull KS1, KS2 and KS3 to ground. When U3101 sees a constant LO instead of a HI to LO pulse, it knows one of the other three buttons has been pressed and will initiate the appropriate function based on which sense line is pulled LO.

IR Input

Infrared remote signals are amplified by IR3401 and appear at U3101 pin 36 as 5 Vp-p negative going data pulses. When no IR is received, the DC level at U3101 pin 36 is 5V. IR3401 is powered by the 5V standby supply. There is no power indicator LED on the normal CTC195 chassis.

OSD Circuit

The CTC195 *O*n *S*creen *D*isplay circuit consists of red, green and blue analog signals from U3101 pins 28, 27 and 26 respectively. These signals along with the FSW (fast switch) signal from pin 25 are sent to the T4-Chip through buffer transistors Q2701, Q2703 and Q2702 and input to U6201 pins 34, 35 and 36. These on screen display signals include the television user menus and also any closed caption information. The FSW signal is also used by the T4-Chip to turn off edge replacement during the time interval OSD is active, preventing incoming video from appearing in the OSD.

Error Codes

Upon certain errors occurring in the chassis, an error code will be stored in the EEPROM. This error code is displayed to the service technician as the value located at parameter 0 01, 0 02 and 0 03. If a 0 is stored, there have been no errors. If errors occur, the first error is stored in 01, the second error is stored in 02 and the last error to occur is stored in 03. Because only the last error location (03) is incremented upon each additional error, the error codes should all be reset to 0 upon completion of the service effort so that a three error code history will be available in the future. The error code numbers are changed just like the other alignment parameters

Unfortunately, many failures will prevent the television from turning on, making the error codes impossible to read via the service menu. These error codes can only be checked by reading the EEPROM directly. This can be accomplished by using "Chipper Check®." Chipper Check® allows the service technician to perform digital alignments, read the diagnostic error codes and check the hardware integrity of EEPROM.

CTC195 "Main" Power Supply

The CTC195 main power supply is a variable frequency/ variable pulse width switch mode power supply. It uses a power supply controller IC (U14101) that drives the power MOSFET, Q101. The CTC195 is a "cold" chassis and the electrical isolation between the power supply and chassis is achieved using a ferrite core transformer, T101. Energy is stored in the transformers primary winding during the power MOSFETS On time and is transferred to the secondary windings when the MOSFET switches off (flyback period). The transformer (T101) must expend all it's stored energy before the start of the next "On" period of the MOSFET. The power supply is self oscillating and the frequency is dependent on the load and the AC line voltage in. The frequency can vary between approximately 25kHz and 90kHz. This supply uses "hot side" regulation which means that there is no actual physical sampling of the secondary voltages. The feedback winding (Nf) on the hot side of the transformer is tightly coupled to the Reg B+ windings on the secondary. Voltage variations in Reg B+ are reflected back into the feedback winding (Nf). The regulator IC U14101 has its own internal reference voltage. The power supply operates whenever it is connected to the AC line and supplies current on demand up to its current output limit. The maximum input power to the supply is 180 watts.

When the instrument is first plugged into an AC source, approximately 150VDC Raw B+ is developed by the bridge rectifier diodes and the Raw B+ filter capacitor C208. This is coupled through the primary winding (Np) of T101 (pin 3) and to the drain of the power MOSFET (Q101) via pin 4 of the transformer. The source of the MOSFET is connected to ground through R124 (.22 ohm/2 watt). At the instant that the instrument is plugged in, the power supply is not oscillating and IC U14101 needs a source of power to turn on Q101 the first time. IC U14101 pin 6 (Vcc) receives B+ via resistor R104 which is connected to raw B+.

With B+ applied to pin 6 of the regulator, U14101 outputs a voltage at pin 5 that is applied to the gate of Q101. This turns the MOSFET (Q101) on for the first time and results in a current flow through the primary (Np) of T101 and Q101. The IC senses this current indirectly. This is accomplished by the circuitry consisting of C146 and R146. One side of R146 is connected to Raw B+ while the other side is connected to C146 to form a simple RC network. This network is connected to pin 2 of U14101. This is the primary current sensing input. The capacitor is held in a discharged state by pin 2 of IC U14101 until the gate of the MOSFET is turned on at which time C146 is allowed to start charging. With the MOSFET

CIRCUIT OVERVIEW (Continued)

turned on, the current increases through it and the voltage on pin 2 of the IC also starts to increase. When the voltage at pin 2 reaches approximately 3 volts, the IC shuts off the drive to the MOSFET. At this point, the energy stored in the primary of transformer (Np) is transferred to the secondary windings. At the same time, the energy transfer is also coupled back into the feedback winding (Nf) between pins 8 and 9. The voltage developed at pin 8 of T101 is rectified by CR111 and filtered by C127. This voltage is applied to pin 6 (Vcc) of U14101 and now serves as the Run Vcc instead of the voltage across R104. The voltage across R104 is only used during initial start-up. After all of the energy is depleted in the secondary windings, the voltage at pin 8 of T101 starts to decay down to zero. This decreasing voltage is applied to pin 8 of the IC through R105. This is the zero crossing input to the IC. When this waveform goes through zero, it signals the start of another cycle and the IC turns the power MOSFET back on. Current will again start increasing through Q101 and the voltage on pin 2 of the IC starts increasing again.

Once the power supply is operating, a method is needed to regulate the output voltages. This is accomplished by the feedback input at pin 1 of IC U14101 The physical construction of the transformer is such that the feedback winding is tightly coupled to the Reg B+ winding on the secondary. For this reason, the voltage across the winding Nf closely follows the voltage fluctuations on the secondary. This voltage is rectified by CR102 and filtered by C147 where it is applied to a precision voltage divider. This divider is formed by R147 and R149. The output of the divider is connected to pin 1 of IC U14101. If this voltage exceeds 400 mV, the IC terminates the drive signal to the MOSFET. In this way the output drive signal from pin 5 of the IC is regulated so that 400mV is maintained at pin 1 of the IC. The voltage divider is adjusted so that this corresponds to the required Reg B+ (140VDC). There are two ways of turning off the MOSFET, one; exceeding 400mV on pin 1 or two; the voltage on pin 2 (primary current sense) exceeds 3 volts. Pin 1 senses the output voltage while pin 2 limits the maximum output current. If the output load increases, then more energy must be stored in the primary of the transformer. This requires the MOSFET be turned on longer. If it is on too long, C146 on pin 2 charges above 3 volts and shuts off the drive to the MOSFET, acting as overcurrent protection.

Horizontal Processing (T4Chip)

The T4Chip employs a two loop horizontal AFC system. The first loop is used to lock an internal 1H clock to the incoming horizontal sync signal. The second loop is used to lock the 1H clock to a feedback pulse derived from a secondary winding on the IHVT. As with the other TChip versions, a horizontal-to-video phase control is available via the I^2C bus. The phase control can be used as a horizontal centering control during instrument alignment.

The first loop employs a 32 fh VCO referenced to a 503 kHz ceramic resonator. To offset sync confusion caused by various copy protection schemes, the T4-Chip provides a `4 {sec window to capture sync and ignore other pulses.

U16201 (T4-Chip) performs the low level horizontal processing. The functions performed in U16201 are very similar to previous chassis. The horizontal processing circuits contained in U16201 are : Horizontal Automatic Frequency Control (AFC), Horizontal Automatic Phase Control (APC), Horizontal Drive, East West (EW) Pincushion Correction, X-ray Protection and Horizontal Vcc Standby Regulator.

Horizontal AFC and APC

The purpose of the AFC (*A*utomatic *F*requency *C*ontrol) and APC (*A*utomatic *P*hase *C*ontrol) is to maintain proper synchronization between the beginning of horizontal scan and the incoming sync signal. The T4-Chip employs a "two-loop" approach to accomplish this task. The first loop is the AFC and second loop is the APC. The AFC phase locks the horizontal oscillator to the incoming sync signal. The APC locks the phase of the horizontal output to the phase of the horizontal oscillator. This system is superior because it is adjustable for good noise immunity in the presence of noisy signals and can track rapid phase changes in signals from VCR's. The external circuit at pin 21 of U16201 is the loop filter for the phase lock loop (PLL) and is used to optimize the frequency response of the AFC loop.

The APC loop is used to track out the phase errors due to variable delays in the horizontal driver and output circuit. The APC has a two bit register (APC Gain) that controls the gain of the APC loop. APC Gain like AFC Gain is preset at the factory and cannot be adjusted by the service technician. The reference signal for this loop is a flyback pulse applied to an RC network and input to U16201 pin 23.

Horizontal Driver

The horizontal driver circuit serves as an interface between the low level horizontal output of the T4Chip and the high power horizontal output circuit. The driver operates in a flyback configuration. Energy is stored in the driver transformer, T14301, during the conduction cycle of Q14301. When Q14301 turns off, the stored energy is dumped into the base of Q14401, the horizontal output transistor (HOT).

Horizontal Output

The horizontal output circuit generates the high current ramp waveform used to drive the horizontal yoke. It also drives the flyback transformer, which in turn produces the supplies necessary for picture tube operation. The supplies include the High Voltage, the focus supply, the screen supply, cathode B+, and the heater voltage. Additional secondary supplies are provided for use by the Vertical amplifier.

CR4401 and C4403 are the damper diode and retrace capacitor. CR4402 is the pin damper that provides a virtual ground to permit the pincushion circuit to modulate the current in the horizontal yoke. CR4403, CR4404, R4402 and SW4401 provide horizontal centering control of the raster by producing a small DC offset voltage.

The pin correction circuit controls the voltage at the junction of L14801 and C14805. Since the amount of horizontal scan is proportional to the voltage across the S-capacitor, C14404, the pin circuit can control the amount of horizontal scan by controlling the voltage at the bottom of C14404. The voltage at the top of C14404 is essentially held at reg B+. Thus, to achieve pin correction, a vertical rate parabolic waveform is produced by the pin circuit and applied to the S-capacitor. This, in turn, produces the desired modulation of the horizontal scan. Another feature of the diode modulator is that it allows width adjustment. This is achieved by varying the dc voltage at the bottom of the S-capacitor.

CIRCUIT OVERVIEW (Continued)

X-Ray Protection Circuit

Q4902 is the XRP switch that will shut off horizontal deflection in the event high voltage becomes too high. The base reference is preset at the factory. A filament pulse is rectified and applied to the cathode of CR4902, a 10V zener diode. When the voltage on the cathode exceeds the 10V breakdown voltage of the zener, the resulting voltage is applied to the emitter of Q4902, turning it on. This applies a positive potential to pin 28 of U2001, turning off horizontal deflection. When an XRP condition occurs, system control will try to restart the set. If three XRP conditions occur within 1 minute, system control places the TV in the off mode. Pressing the POWER button will turn the set back on, starting the XRP detection process over again.

Vertical Output

The vertical circuit used in the CTC195 chassis acts as a voltage to current converter. It converts the vertical rate DC ramp signal out of the T2-Chip to a current ramp through the yoke to deflect the electron beam from top to bottom on the CRT. U4501 is an inverting amplifier that sinks current at pin 5 when pin 1 is high and sources current from pin 5 when pin 1 is low. U4501 is supplied by the 26 volt run source from the main power supply.

When the vertical ramp is at the bottom of the slope, pin 5 of U4501 sources current from the 26 volt supply through the yoke to the approximate 13 volt half supply deflecting the electron beam to the top of the screen. As the ramp climbs in voltage on pin 1, the current source from pin 5 proportionally decreases lowering the voltage across the yoke, deflecting the beam towards the center of the screen. When the voltage on pin 1 of U4501 reaches the same voltage as pin 7, pin 5 is at approximately half the 26 volt supply. Because the low side of the yoke is tied to the half supply, there is no current through the yoke resulting in the electron beam being at the center of the screen. As the voltage on pin 1 of U4501 rises higher than pin 7, pin 5 begins to sink current. This causes the current to flow from the supply, through the yoke to pin 5. Because the current flow reverses, the beam is deflected towards the bottom of the screen. During retrace, the ramp resets causing pin 5 of U4501 to go high, deflecting the beam back up to the top of the screen. The extra current required to deflect the beam from the bottom to the top of the screen is produced by C4505.

FPIP

The FPIP (*Comb* **F***ilter plus* **P***ix-***I***n-***P***ix IC*) is a CMOS IC designed to be a 1-chip solution for the single moving picture-in-picture function in a television receiver. In addition, it provides a digital comb filter for the main picture Y/C separation. The FPIP contains analog switches to perform the swap and overlay functions, A/D's, D/A's, crystal clock, and the digital circuits necessary to process the small overlay picture. The FPIP is divided into several sections, the PIP processor, clock, comb, analog and bus sections. The PIP Processor section includes the decode, encode and field RAM subsections. The decode subsection takes a composite video waveform and decodes it to Y, R-Y and B-Y for storage into the internal field memory. The encode subsection takes the information stored in the internal field memory and encodes chroma and outputs separate Y/C small picture signals which can be combined to form a composite video signal for overlaying on the main composite video signal. The Burst Locked Clock section generates the clock for the system which is locked to the color subcarrier of the main composite video signal. The analog section converts between the analog and digital domain and performs the video switching functions. The bus section controls the FPIP functionality. The registers which hold the control information are distributed throughout the IC.

The FPIP Switching IC U18100 serves as the center of the video switching circuits. The two selected composite video signals are input at pins 1 and 51 after buffering. The external S-Video is input directly into U18100 at pins 3 (luma) and pin 5 (chroma). Once inside the IC the S-Video luma and chroma signal are combined to form a third composite signal. The three composite video signals are applied to two analog switching circuits within the IC. One is the "Main" picture analog switch and the other is the "PIP" picture analog switch. The S-Video is also applied (separate luma and chroma) to the S-Video Switch. The output of both analog switches are applied to 8 bit A/D (analog-to-digital) converters.

The output of the analog switch (Main) is applied to a digital comb filter that separates the luma and chroma signals. After Main picture digital video is separated at the comb filter, the digital luma and chroma signals are converted back to analog signals by an 8 bit (luma) and a 10 bit (chroma) D/A converters. The luma signal then exits the IC at pin 49, buffered by Q18108 and reenters the IC at pin 43 where it is applied to the S-Video switch. The selected main chroma signal exits the IC at pin 47 for buffering and amplification and reenters at pin 45 and is also applied to the S-Video switch.

The output of the PIP analog switch is also digitized and is then applied to a PIP processing circuit that separates the luma and chroma signals. The separate PIP luma and chroma signals are both converted back to analog via two D/A converters. The analog PIP luma signal then exits the IC at pin 33, is buffered and reenters the IC at pin 35. The PIP luma is then applied to the "Over-Lay" switch. The PIP chroma signal exits at pin 31, is buffered and reenters at pin 37. The PIP chroma signal is also applied to the overlay switch.

Automatic Kine Bias

The CTC195 AKB is different from most AKB's that have been implemented in the past. Most AKB systems do a sample and correction of the cathode current at most every fourth video field. This is reasonable when the system is hardware based. However, because of the chassis' microprocessor overhead, the CTC195 system does a sample and compare every 10 seconds. The intent of the AKB system is to allow the picture tube to operate at the correct color temperature over the life of the tube. Because of this, there is really no reason to correct every field or every fourth field. Most field based AKB's have capacitors to hold the required bias level, and since the capacitors will discharge over time, these systems must operate on a field basis anyway. The CTC195 uses registers in the T4-Chip to "hold" the required bias level, and if the chip remains powered, the register will hold the value indefinitely.

The AKB operates on the principle that if a pedestal imposed on the RGB signal is alternated in peak voltage such that the voltage resulting from the current feedback is above and

CIRCUIT OVERVIEW (Continued)

below a reference voltage, the long term average of the feedback signal is the same as the reference voltage. The required pulses are generated by the T4-Chip.

The RGB signals are added to the AKB pedestals in the T4-Chip. The RGB signals are then amplified to CRT drive levels and passed through a "push-pull" buffer that drives the cathodes of the CRT. The cathode current is carried by the transistors and their collector currents are essentially the cathode currents. The cathode currents are passed through a resistor to develop a voltage that is proportional to the cathode current. The voltage is passed back to the T4-Chip for sampling and measurement. The amplitudes of the RGB AKB pulses are alternated such that the AKB_IN signal goes above and below the reference voltage, called the threshold. As long as the CRT is stable, the system will have an equal number of measurements above the threshold as below the threshold. There are three bias controls that allow the DC levels of the RGB signals to be adjusted independently of one another and a sub brightness control that can adjust all three colors DC level together. These adjustments affect the sample pulses as well as the video.

Sample pulses are generated during the vertical blanking interval. The sampling pulses are generated on lines 18, 19, and 20 for red, green, and blue respectively. These pulses generate cathode current that generates a sample voltage during those lines. Since the collector currents are "summed" in the sample resistor, the result is a voltage that has pulses on lines 18, 19, and 20. The sample line is capacitively coupled to the T4-Chip.

When the receiver is turned on, the AKB routine is disabled for 20 seconds. This gives the picture tube some time to warm up. The initialization values for the T4-Chip are recalled from EEPROM. The bias and sub brightness values are those that were in use just prior to the last turnoff. The system assumes that the sample pulses will alternate above and below the threshold starting with the pulses being above the threshold. The number of occurrences of high and low are kept in an accumulator for each of the RGB channels. The accumulators are set initially to 2. After the 20 second delay, the system makes a measurement of the feedback signal. It should be noted that the sample pulses are always present. Only the sampling is at the 10 second rate. The software measures the red, green, and blue samples in that order. If the measurement is above the threshold, the accumulator is incremented; if it is below the threshold, the accumulator is decremented. As long as the accumulator value is 1, 2, or 3, nothing is done. If the accumulator value is 0 or 4, the software makes an adjustment. If all three accumulators have a value of 0 (or 4), it is assumed that all three guns of the tube are biased too low (or high), and the value of the sub brightness is increased or (decreased). This affects all three colors equally, and thus raises (or lowers) the current of all three guns. If any one color's accumulator has a value or 0, that color's beam current is too low, and the bias value of that color is increased. If the value is 4, the beam current is too high and the bias value is decreased. This continues for as long as the set is running. If any measurement indicates the system has run out of adjustment range on any or all colors, no further adjustments are allowed. This keeps the system from adjusting the color temperature of the colors that can still be adjusted. If those colors were to be adjusted, the color temperature would be very poor due to the lack of response of the color that has run out of adjustment range. When the set is turned off, the current values of bias and sub brightness are stored for use the next time the set is turned on.

Video Processing

The video section is composed of 4 main areas: luma processing, chroma processing, external RGB inputs, and RGB outputs. Essentially all circuitry for these functions is contained in the LA7612 (T4 Chip).

Luma Processing

The video input is applied to [Y In] from an input buffer and clamp capacitor. Following the input clamp, the video signal is applied to the luma filters. In the CTC195, the wide-band mode will be selected when Y/C separation is provided prior to the T4 chip, and the 3.58 MHz mode will be used when no external Y/C separation is available. The luma filter block includes a transversal peaking circuit, controlled via the I^2C bus.

After filtering, the luma signal is once again clamped, and passed through the black stretch circuitry. This circuit modifies the video transfer function to enhance contrast on low light scenes.

External RGB Input Processing

The external RGB inputs are used for OSD processing on the CTC195. OSD signals from the micro are applied to the external RGB inputs through a set of low impedance buffers and input clamp capacitors. These clamps are keyed during the burst gate interval. Following the clamps are limiters set at approximately 714 mVpp (corresponding to 100 IRE). In the CTC195, the input drive level should be somewhat less than this, typically in the range of 70 IRE (or 500 mVpp). These external RGB signals will then be matrixed to form Ext Y, Ext R-Y, and Ext B-Y.

RGB Output Section

Internal Y from the Luma section, internal R-Y and B-Y from the Chroma section, and external Y, R-Y, and B-Y from the external RGB inputs all come together in the Int/Ext Switch. The Fast Switch line controls which set of signals is displayed. A low level on the Fast Switch selects the internal signals, a high level selects external.

After source selection, the pix control adjusts the amplitude of the Y, R-Y, and B-Y signals. These are then clamped during back porch and the brightness control is applied to the Y signal. R-Y and B-Y are matrixed to form G-Y and the Y component is summed with all three color difference signals to form Red, Green, and Blue.

Chroma Processing

The video signal is applied to [C In] through a high pass filter. This high pass is necessary to remove low frequency luma components in order to stay within the DC dynamic range of the 1st chroma amp. Following the 1st chroma amp, the signal passes though the chroma filter section. The chroma filter can be configured as a chroma peaker or a symmetrical bandpass, or can be bypassed completely. Control is by means of the I^2C bus. The chroma peaker mode will be selected to compensate for the IF response, and the symmetrical bandpass mode will be used for auxiliary inputs. The ACC detector monitors burst amplitude at the output of the filter section and adjusts the 1st chroma amp gain to maintain a constant level.

The output of the ACC detector is also compared to a kill

CIRCUIT OVERVIEW (Continued)

threshold reference in the killer amp. If the detected burst amplitude is below approximately 2.4 IRE, the killer is activated, shutting down the overload amp.

From the ACC point, the filtered chroma signal is then sent to the overload amp and from there to the 2nd chroma amp. The 2nd chroma amp is made up of two identical stages in parallel. The output of the "B" stage drives the chroma overload detector which then controls the overload amp gain to form a low gain AGC circuit. This loop attempts to maintain the average chroma saturation within some prescribed limits. Chroma overload is enabled over the I^2C bus. Chroma saturation is applied to the 2nd chroma amp "A" stage, and from there the chroma signal reaches the demodulator inputs. After the demodulators, there are lowpass networks to reduce demodulator products.

The chroma VCO is a single pin design. The chroma VCO amp output passes though a tunable filter back to it's positive input providing positive feedback. From this point it is also connected through an impedance to it's negative input, providing negative feedback. A series resonant crystal filter is connected from the negative input to ground. At frequencies off resonance, the positive and negative feedback components will cancel. At the resonant frequency of this filter, the negative feedback will be shunted to ground. This results in a net positive feedback, sustaining oscillation. By tuning the VCO filter, frequency control is obtained.

In the Autoflesh block, a phase detector compares chroma from the output of the 2nd chroma amp "B" section to the subcarrier from the tint control. When the incoming chroma phase is in the vicinity of "flesh" (approximately 123° and dependent on the customer preference tint setting) a phase correction is applied to the subcarrier such that the demodulated chroma is moved towards "flesh". Autoflesh is enabled over the I^2C bus.

Tuner

The CTC195 tuner continues to employ TOB (Tuner On Board) topography with a zinc surround. It is a single conversion, electronically aligned tuner based on the CTC 179/189 chassis family tuner. There will be two variations. A single input tuner and a single input tuner with PIP RF output

The second tuner is not based on the CTC 195 but is a "cold" version of the CTC 185 tuner. There are many similarities between the two. The PLL communicates with the main microprocessor for channel selection information, then converts the digital information to analog voltages needed to tune the RF and mixer/oscillator to the proper frequency.

Chassis variations with a single tuner will have only a VHF/UHF splitter to route those frequencies to the proper RF amplifier. PIP chassis will use an input splitter that will send a reduced (7-9 dB) RF signal to the PIP tuner and an RF signal on to the main VHF/UHF splitter. The splitter then routes the proper signals to one of two RF amplifiers.

The PLL IC controls the frequency response curve of the input filter by using output voltages from pins 6 and 14 to change the characteristics of the tank circuit and the RF amplifier. Pin 6 is a variable DAC output voltage while pin 14 is a high or low voltage depending upon the selected band. As channel selection goes up through the VHF, then the UHF bands, the tuning voltage on pin 6 rises until the first UHF channel selection (14). At that point, the band switching on pin 14 goes from high to low and the DAC output voltages go down and begin the tuning cycle again. This becomes the beginning of the tuning cycle.

U17701 comprises an entire mixer/oscillator network with very few external components. The IC contains circuitry that performs traditional mixer/oscillator duties, heterodyning the incoming RF signal against an internally generated frequency to always produce a 45.75 MHz IF signal. This IF is then sent to the T4 Chip for further processing and to separate the video and audio IF signals.

The purpose of the PLL circuit is to process channel selection information from the microprocessor, receive feedback from the mixer/oscillator and adjust the incoming RF filters, the local oscillator and associated tank circuits to provide the proper tuner IF output signal based on the channel selection. It also selects the proper band response for the entire tuner.

The PLL has three DAC and three Bandswitching outputs. There are also several inputs to monitor the local oscillator frequency. The bandswitch outputs are either high (either +12V or +5V) or low (0V) while the DAC outputs can vary between 0 and +33 Volts.

The bandswitch outputs are what determines the overall response of the tuner based upon the channel selection. The three bandswitch outputs, pins 14, 15 and 17 select between the VHF and UHF broadband components of the tuner. Pin 14 selects the UHF or the VHF RF amplifier. Pin 15 selects the VHF or UHF mixer that is internal to U17701. Pin 17 switches the VHF or UHF local oscillator circuitry on and off. Bandswitching is accomplished by using varactor or voltage-controlled diodes to switch in and out inductors and capacitors to shape the frequency response characteristics of the tuning circuitry.

Fine tuning down to a single station is dependant upon the PLL open collector output voltages from pins 6, 7 and 8 and control the RF filter voltages used to center the RF frequency response curve over the desired channel. Pin 6 controls the frequency response of the incoming single-tuned filter. Pin 7 controls the frequency response of the primary coil of the double-tuned filter stage, while pin 8 controls the secondary. Each of the lines provide different outputs depending upon the frequencies being tuned.

Digital Convergence Circuit

The Digital Convergence System uses a single integrated circuit, IC19501, and a serial EEPROM IC, U19500. The DigiCon IC is directly connected to the I^2C bus, but the EEPROM is connected only to the DigiCon IC. This means all control is accomplished from the main microprocessor, but when values of alignments are changed, the DigiCon IC must do the reading and writing to the DigiCon EEPROM.

The DigiCon IC controls all functions of the DigiCon System. There is an internal pattern generator to supply the three video patterns required during consumer and technician level alignments. The pattern is output from pins 27, 28 and 29 through buffers, to the video input of the CRT drivers on the Kine Socket boards. The pattern receives horizontal and vertical sync information from the sync separater circuits via pins 22 and 55.

CIRCUIT OVERVIEW (Continued)

An additional D/A provides a correction signal for vertical dynamic focus from pin 34. This signal is amplified and added to a horizontal dynamic focus correction signal from a current transformer that transforms corrects deflection yoke current.

Pin 26 is used to monitor the +5V and `15V convergence power supply voltages. If the current draw exceeds safe limits, the DigiCon IC will adjust the DAC outputs to reduce the output transistor current draw to zero.

It should be noted that pin 26 monitors only the total current draw of the power supply, not individual output devices. If any output device fails, the IC will act to shut down all current draw, making troubleshooting difficult.

Also, as the IC monitors this voltage, if it drops too low or goes too high, the outputs of the DAC's are lowered to decrease current flow in the convergence yoke output transistors. This prevents any overcurrent conditions due to improper power supply voltages. The voltage is also monitored during power up cycles and a mute voltage sent to the power amplifiers. This guards against excessive power supply drain during the start up period where there might be a tendancy for the DigiCon IC to attempt to over correct the yoke currents.

Convergence Yoke Drivers

There are six yoke drive outputs from the IC, one each for the horizontal and vertical convergence yokes for each color. The output pins are 43, 44 and 45 for the red, green and blue vertical drives and pins 48, 49 and 50 for the red, green and blue horizontal drives. The six circuits and their output devices function identically. The DAC outputs are connected to an op-amp predriver which in turn provides drive to the differential amplifiers, Q19300/Q19301. The output from this device drives Q19304 which drives the main output devices, Q19306/Q19307. The outputs are connected to the digital convergence yokes. The entire amplifier line is direct coupled and forms a tightly closed-loop servo system. Because the output is current driven, waveforms may be very difficult to distinguish. Yoke current feedback is monitored by R19301 and Q19301. If yoke current increases, the voltage across R19301 increases causing more current to be drawn through Q19301. This causes the emitter voltage to increase (towards the +45V supply) decreasing current flow through the class A driver, Q19300. As the emitter voltage increases, the collector drive signal to Q19304 decreases and the collector voltage decreases. This begins decreasing the base drive to the output darlington amplifiers, which in turn decreases their output.

Convergence Power Supply

The convergence auxiliary power supply is a variable frequency-variable pulse width switch mode power supply. During start-up, raw B+ is applied to the convergence power supply. The Raw B+ is generated by the main power supply rectifiers. With Raw B+ applied, the gate of TR1 begins to charge up through R03 and R22. When the turn-on voltage of the FET inside U700 (TR1) is reached, the FET begins conducting. With TR1 conducting, current flows through the primary (Np) of the transformer (T701), FET (U700), and through the current sense resistor R14 (U700-8). The current flowing through the primary winding causes a electromagnetic field to develop around the winding of Np (pins 7 and 5). As the field around Np rises a voltage is induced into winding Nd1 (pins 2 & 3). The voltage developed at pin 2 of T701 is coupled by R10 and C700 to the gate of TR1 (U700-4). The polarity of this winding is such that it generates a positive voltage which keeps TR1 conducting. When the current through TR1 reaches the current limit threshold set by R14 and C05, TR1 is turned off. When the FET (TR1) turns off, the magnetic field around the winding Np collapses and the energy stored in the primary of the transformer is transferred to the secondaries. As the field around Np collapses, a positive pulse is generated at pin 2 of Nd1 that is applied to the gate of TR1 turning it on again. This will continue for several cycles until stable oscillation is achieved.

The voltage developed across Nd2 is rectified by CR5 and compared to an internal reference of -40.5V (+/- .5V) at pin 1 of U700. Once operation begins, this feedback winding controls the duty cycle of TR1. The Nd2 winding is responsible for regulating the output voltages. The duty cycle of the power supply is altered so that the voltage across winding Nd2 is maintained at -40.5V. The secondary supply voltage windings (Ns1 through Ns4) are wound so they reflect any load changes on the secondary back to winding Nd2.

During normal operation as the load on the power supply increases, the On time of the FET increases. This increased On time causes higher currents to flow through the FET and the primary winding of T701 (Np). When the voltage across R14 reaches approximately +.6V, TR3 (inside U700) turns on. This turns off the FET and causes the output voltage to decrease. Zener diode CR01 and resistor R11 are used to compensate for any fluctuations in line voltage that result in changes in the Raw B+.

ON/OFF Control

The power supply starts when the gate voltage of the FET (pin 4 of U700) is allowed to charge up thus turning on TR1. However, the power supply only needs to run when the instrument is turned on. Transistor Q700 is responsible for holding the gate of the FET low (OFF) until an On/Off signal is received from the Digital Convergence CBA. When raw B+ is present, transistor Q700 is biased On via R700, R701 and R702. With Q700 on, the gate of the FET is pulled low thus preventing the power supply from starting. The On/Off signal is obtained from the digital convergence board by rectifying the filament pulse and is approximately +23V when the instrument is running. This On/Off signal voltage supplies the B+ to the emitter of Q1 via R4. This allows Q1 to turn on providing a current path through the photo-diode. Initially the current flowing through the photo-diode of the opto-coupler is supplied by Q3 on the ground end of the circuit. The components (Q5, C14 and R20) on the base of Q3 form a delay circuit that turns off Q3 after a short delay to allow the supply to start and stabilize. When the +23V is present, capacitor C14 begins to charge up through R20. As the base voltage of Q5 rises, Q5 turns off, thus turning off Q3 removing the current path for the photo-diode. By this time the supply is up and running and the current path for the photo-diode (ground end) is provided via Q4. This allows the photo-transistor to remain on, keeping the base of Q700 grounded thus keeping it turned Off. This allows the gate voltage of TR1 to rise and the power supply to operate normally.

CIRCUIT OVERVIEW (Continued)

As mentioned earlier, the current path for the opto-coupler during normal operation is provided by Q1 and Q4. Q4 is turned on only when the +15V and -15V supplies are within a specific operating range. When an excessive load is put on the supply, the supply goes into current limiting. In order not to damage the convergence amplifiers, we need to turn off the supply whenever a major overload or over-voltage occurs. When the +15 or the -15 volt supply drops to approximately 13V the transistor Q1 is turned off. Since Q3 is already off (after the initial startup delay) the current path for the opto-coupler is removed. This causes the supply to immediately turn off until the instrument is turned off and back on again. Monitoring the +/- 45V is not required since a failure in the convergence amplifier causes a large enough load on the supply that the current limiting circuit within U700 will shut down the power supply. Q4 is biased on by the output of the secondary voltage supplies. In this way the secondary output is monitored for overload on the supplies or in the event that a supply is lost. Q4 monitors the +15V supplies for "Under 13V" (CR12) and Q6 monitors for "Over 20V" via CR15. If the +15V secondary output supply falls below 13V, Q4 turns off. If the +15V rises over 20V, Q6 turns on and grounds the base of Q4, turning it off causing the power supply to shut down because Q700 will turn back on. Q7 monitors the -15V supply via CR16. If the -15V supply rises to -13V (supply falls) Q7 turns on grounding the base of Q4. Whenever Q4 is turned off, this removes the current path for the photo-diode in U700. This causes the photo-transistor in U700 to turn off allowing Q700 to turn back on grounding the gate of the FET (TR1) thus shutting down the power supply.

Transistor Q2 is responsible for monitoring the +23 volts from the convergence CBA. If the +23 volts starts to fall, Q2 turns on when the emitter falls below the level that the base is biased at via R6 and R5. When Q2 turns on the emitter of Q1 is grounded, removing its B+ supply and turning it off. This instantly turns off the opto-coupler U700. With the opto-coupler off, Q700 turns back on and shuts down the power supply.

AVR (Automatic Volume Reduction)

Automatic Volume Reduction lowers the signal to the output amplifiers during possible over-current conditions that may damage the output device or speakers. The circuit has one control line and thus 2 states. The AVR control line is polled periodically (approx. 10Hz rate) to check the status of the output level. Whenever the input to the System Control Microcomputer at pin 48 is LOW, no action is required. When it goes HIGH, the VOLUME register is decremented at a 10Hz rate until the AVR sense line drops LOW again. Then the register stops decrementing and a 5-sec timer is started. If the line goes HIGH again, the timer is canceled and VOLUME is again decremented until the line goes LOW. If the timer runs down and the line has stayed LOW, VOLUME is incremented back toward the customer setting, one step every 5 seconds. If the line goes HIGH at any time, incrementing stops and the decrementing loop is again entered.

The audio from the power amps are applied to CR11901/902. These diodes act as rectifiers to generate a filtered DC voltage at the base of Q11902 & 903. As the output level goes up, the corresponding DC voltage at the base of Q11902 & 903 goes up. A reference voltage is generated by zener diode CR11903 and transistor Q11904. This reference, which sets the emitter voltage of Q11902 & 903 to approximately 4.2VDC. If the voltage on the base of either of these transistors rise to approximately 4.9VDC, the transistor turns on. This puts a low on the base of Q11901, which turns it on. With Q11901 on, a Hi from the emitter is applied to pin 48 of IC13101.