CIRCUIT OVERVIEW

Circuit Overview

The signal processing and deflection circuits of the CTC187 chassis are very similar to the signal processing and deflection circuits of our previous one (1) chip chassis. The CTC187 chassis utilizes the T-Chip IC and is Bus Controlled. All chassis alignment, service adjustments, and user controls are accessed via the instrument control buttons and the remote transmitter. See the Alignment Procedure and Service Adjustment sections of this manual for the necessary access codes.

NOTE: The CTC187 chassis is virtually the same as the CTC177 with the addition of a Stereo Decoder / Comb filter board. Technicians servicing this chassis will find the following related technical training manual helpful.

T-CTC176/177-1

This publication may be ordered for a nominal fee from:

TCE Technical Publications

10003 Bunson Way

Louisville, Ky. 40299

AC Input, Regulation and Standby Voltages

The CTC187 uses a variable frequency variable pulse width regulator. U4101, the hybrid IC, contains most of the regulator circuit components including the power switching FET.

When power is first applied to the instrument, approximately 150 VDC is developed by the bridge rectifier diodes and filter capacitor. This voltage is applied through the primary winding of T4101 pins 1 and 3 into U4101 pins 11 and 12. Pins 11 and 12 are the drain of the power FET (internal to the IC, U4101). The source of the FET is connected to pins 8 and 9. R4124 is connected from these pins to ground. R4101, the start up resistor, provides enough bias to the gate of the FET through pin 4 of the IC (U4101) to turn the FET on.

When the FET is turned on the drain current flows through the primary winding of the transformer, T4101, through the FET to ground. Current flowing in the primary induces a voltage on the winding between pins 5 and 6 on the transformer. This voltage is coupled from pin 5 through R4125 and C4123 into pin 4 of the IC, U4101. Pin 4 is connected to the gate of the FET (internal to the IC). The polarity of the voltage is such that it turns the FET on harder. As more current flows, a larger voltage is built up on R4124, the FET source resistor.

Eventually the voltage will be large enough to turn on the over-current protection circuit (OCP) internal to the IC (U4101). This will cause the FET to turn off. When the FET turns off, energy is transferred to the secondary windings charging filter capacitors C4107 and C4108. This sequence repeats for several cycles until stable oscillation begins. The frequency of oscillation will vary with load from approximately 100 kHz at standby to 38 kHz at full load.

The feedback winding between pins 5 and 7 on T4101 is tightly coupled to the secondary windings. The voltage on the feedback winding will tend to follow the voltage changes on the secondary windings. The voltage developed on pin 7 of T4101 is rectified by CR4111 and filtered by C4127. This negative voltage is applied to pin 1 of U4101. Internal to U4101 is a precision voltage reference. This reference is trimmed to -40.5 volts +/- .5 volts. The error amp works to keep the voltage on pin 1 of U4101 equal to the reference voltage. If the load on the secondaries increases and the voltage drops, the voltage developed at pin 7 of T4101 would decrease. This would let the FET stay on longer thus increasing the output voltage. In this way the IC is able to hold the output of the supply constant with varying line voltages and loads. If an excessive load is placed on the power supply outputs, the on time of the FET will increase. This will result in more current through the FET and source resistor R4124. A voltage drop will be developed proportional to the current and this voltage will be applied to the over-current protection circuit internal to U4101. This circuit is also connected to pin 7 of the IC. A capacitor, C4124, is connected to pin 7. As the current increases, it will charge C4124 and turn on the over-current protection circuit. This will turn off the FET. Increasing the value of C4124 increases the overcurrent protection trip point.

The network composed of C4122, C4128, R4126, and CR4112 is a snubber network used to reduce the high voltge spike developed when the FET turns off. C4103 and R4105 are part of a compensation network which tends to stabilize the supply from parasitic oscillations. R4129 is an ESD protection resistor for the gate of the FET. R4122 and CR4109 help stabilize the overcurrent protection with line voltage variations. All of the ferrite beads are for RFI emission reduction. C4107, L4102, and C4105 form a filter network to reduce the ripple in the REG B+ and to reduce high frequency switching noise.

The secondary windings of T4401 provide standby voltages of +12 and +5 volts plus a regulated +140.5 volt supply used to power the horizontal deflection circuit.

Start-Up

The regulator circuit is active at all times while AC power is applied to the instrument. The Bus Control circuit, when addressed by activation of the power ON button, will provide a signal to turn on the horizontal count down circuit internal to the T-Chip. Horizontal drive pulses are then output at pin 24 of the T-Chip, U1001. Since the regulator circuit is active at all times power is supplied to the horizontal driver and output stages at all times. Therefore activation of the horizontal drive pulse will start horizontal deflection. With the horizontal deflection circuit active, power is supplied to the rest of the chassis via the derived supplies from the secondary of the IHVT, T4401.

Horizontal AFC

The purpose of automatic frequency control is to maintain proper syncronization between horizontal scan and the incoming sync signal. The new T-Chip employs a “two-loop” approach to accomplish this task. The two-loop system uses one PLL to phase lock the horizontal oscillator and the incoming sync signal and a second PLL to lock the phase of the horizontal output to that of the horizontal oscillator.

CIRCUIT OVERVIEW (Continued)

Horizontal Drive

The output at pin 24 of the T-Chip is an open collector which is low (on) when the horizontal output is on. A buffer stage has been incorporated between the T-Chip and the horizontal driver to reduce coupling.

X-Ray Protection Circuit

A pulse from the filament winding of the IHVT secondary is rectified and applied to pin 26 of the T-Chip, U1001. If a fault occurs which allows the voltage applied to pin 26 of the T-Chip to exceed an internal reference of about 3.0 volts the horizontal drive pulse output at pin 24 will be inhibited causing the instrument to shut down. As a protection feature the system control micro will count the number of times the instrument shuts down. If the instrument shuts down more than three times in one minute, no further attempt will be made to restart the instrument. At this point it will be necessary for the user to select OFF then ON to restart the instrument.

Vertical Deflection

The vertical deflection circuit in this chassis is DC coupled. Because of the DC coupling, the DC level of the reference ramp from pin 17, U1001, affects the vertical centering. A new adjustment, "Vertical DC", is included in the adjustments to reduce centering errors. The "S" correction is accomplished internal to the T-Chip, U1001.

System Control

The control microprocessor (U3101) communicates with the rest of the chassis via three distinct bus communication lines. They are the "T-BUS", the "IM BUS", and the "IIC-BUS". The "T-BUS" is used for communications between the T-Chip and the control micro. The "IM-BUS" is used for communications between the D-PIP circuit (when used) and the control micro. The "IIC-BUS" is used for communications between the tuner and the control micro. The control micro receives commands from the user control panel or remote control and conveys this information over the correct bus line to the rest of the chassis.

Signal Processing

The tuner IF output is applied via a saw filter to the T-Chip at pins 10 and 11. RF AGC is output at pin 12 of the T-Chip and routed to the tuner. Video is output at pin 63 and selected video is output at pin 51. They are both routed to the D-PIP circuit when it is used. Selected video is routed to a comb filter (FL2651) when it is used. The video signal is then routed back into the T-Chip with luminance applied to pin 48 and chroma applied to pin 49. The on screen display signals from the control micro are applied to the T-Chip at pins 40, 41, and 42. The red, green, and blue signals are output at pins 36,37, and 38 respectively.

All user control adjustments are bus controlled. They include brightness, contrast, color, tint and sharpness.

Sound Processing

The stereo decoder (U1600) receives wideband audio from the main board and decodes left and right audio information. Wideband audio enters the board at JS107 and is capacitively coupled to U1600 pin 11. Decoded left and right signals are output at pins 29 and 28 respectively. U1601 buffers the left and right output and provides the expanded stereo feature in conjunction with Q1601. When the expanded stereo line (JS112) goes LO, Q1601 turns on and cross-mixes the left and right channel information to produce a perceived increase in stereo separation. Pins 1 and 7 of U1601 output the left and right signals respectively that are capacitively coupled back to the main board via JS105 and JS106.

U1600 is digitally controlled over theIIC bus. Analog lines that were used in the CTC177 for stereo sense and stereo select (see the *Audio Processing* section of the CTC177 training manual) are no longer used. Instead, communications between U1600 and the television's microprocessor are carried out over the serial bus.

Tuning System

The tuning system used in this chassis is similar to tuning systems used in previous chassis. However the phase-lock-loop (PLL) portion of the system is now an integral part of the tuner. Tuner band switching and tuning frequency commands are sent to the tuner via the micro's clock and data lines and the tuner responds accordingly. Tuning sync is input to the control micro (U3101) at pin 38 and is periodically sampled using a sync presence detection algorithm.

Autoprogramming

Autoprogramming is a feature which automatically programs the scan list by progressively searching for channels at the antenna input. Autoprogramming starts by determining if the TV is connected to a cable system or an "off-air" antenna.

NOTE: Because the system is looking for valid sync, weak off-air signals may not be programmed. These channels can, however, be manually programmed by selecting the Channel Memory feature in the Set Up menu.

Video Controls

The T-Chip has dedicated registers used to control the video parameters (brightness, contrast, color, tint and sharpness). The volume parameter is also controlled by a dedicated register.

Non-Volatile Memory (EEPROM)

The EEPROM will be incorporated in all instrument models. These instruments will have non-volatile scan lists.

IF Signal Processing

The IF signal from the tuner is processed by the Saw Filter (SF2301), then applied to pins 10 and 11 of the T-Chip IC (U1001). Signal processing internal to U1001 generates baseband video, AFT and AGC signals. The AFT consists of a 12 stage counter that sends a digital count of the IF frequency directly to the microprocessor U3101. No alignment is required. The AGC signal is returned to the tuner to control the gain of the incoming RF signal.

Comb Filter

This board contains an analog comb filter that is used to separate luminance and chrominance. Composite video is routed from the main board from E2601 and applied to the input at pin 2 of the comb filter IC (FL2651). Luma is output at pin 5 and chroma is output at pin 3. These signals are sent back to the main board at E2602 and E2603 where they are input to the T-Chip (U1001). Refer to the luminance and chrominance processing section of the CTC177 training manual for signal processing on the main board.