CIRCUIT OVERVIEW

Standby Power Supply

The standby power supply in the CTC 185 is derived from a simple dropping resistor connected to a three terminal 12 volt regulator IC. The power comes from a half wave rectified ac waveform. What makes this simple scheme provide enough power to operate the chassis in standby is that the microprocessor turns off the T4-Chip when it is not needed. Timing for the switching of the T4-Chip power is important because the current needed to run the micro and the T4-Chip together is derived from a capacitor until the +26v_run supply supplements it.

The ac power line is rectified by CR4109 and CR4004 and fed through R4002 to filter capacitor C4154. Zener diode CR4110 limits the voltage to 27 volts so that regulator U4102 is not damaged by excessive voltage. Diode CR4703 supplements the standby power supply when the chassis is in the on state from the +26v_run supply. The power necessary to run the chassis during turn on comes from C4154. U4102 provides a regulated 12 volt output to run the standby loads in the chassis. Zener diode CR4104 is used to provide two reference voltages for the control system to use.

The circuit which switches the T4-Chip power consists of Q4115, R4143, R4144, and the microprocessor. Pin 20 on U1001 is pulled low to turn on Q4115 and apply power to the chassis.

Main Power Supply

The power supply in the CTC 185 is a non-isolating modified buck converter. It uses a winding on the IHVT to provide a voltage boost and a series PWM controlled MOSFET to regulate the output voltage to 130 volts DC. The supply has no alignments since it uses a precision 1% voltage reference IC. The control circuit is synced to the horizontal oscillator by using a flyback pulse as a timing reference for the sawtooth ramp generator. When the chassis is in standby mode the MOSFET is kept on by a drain to gate resistor which forces the output voltage to be equal to the RAW B+ voltage.

The winding on the IHVT sums an inverted retrace pulse on the RAW B+ voltage. This provides the pre-boost so the supply will regulate even when RAW B+ falls below 130 volts. The number of turns on winding WI determines the lowest voltage at which the supply will regulate. The 25 and 27 inch chassis regulate down to 95 volts ac and the 19 and 20 inch chassis regulate to 90 volts.

Raw B+ comes from a full wave bridge rectifier and filter capacitor C4007. R4172 is a bleeder to discharge C4007 when the AC power is disconnected. Capacitors C4104, C4122, C4124, C4134, and C4135 are for RFI suppression. R4146 and C4137 form a snubber for MOSFET Q4114. R4103 is a current limit resistor for Q4114. It limits the gate drive by reducing the 9 volt gate supply with respect to the source terminal of Q4114. R4108 provides gate drive when the chassis is in standby. CR4106 is a protection diode for the gate of Q4114.

The 9 volt gate supply consists of C4106 and CR41 I 1. The charge pump is C4138, R4147, CR4113 and CR4112. C4138 is charged through CR4112 during retrace, and discharged into C4106 during trace through CR4113. MOSFET Q4114 is switched on though R4138 and is turned off by Q4113 turning on and bleeding the gate charge off through R4114.

The comparator block consists of Q4102 and Q4103. The inputs to the comparator are the bases of the two transistors. Q4113 serves as a high voltage buffer to switch Q4114. One input is fed from the error amp and reference block which is formed by U4103 and the voltage sense resistors R4136, R4137, R41 I 1, and R4112. The parallel combination allows the output voltage of the supply to be trimmed to exactly 130 volts. U4103 contains a 1% voltage reference and the error amplifier. C4103 and R4149 provide the gain compensation for the error amp to ensure the power supply is stable into any expected load.

Q4104 provides the time delay which is necessary to keep the MOSFET on until the current through it has dropped to zero. The collector is capacitively coupled to the base of Q4108 to provide a short duration pulse which charges C4109. C4109, Q4108, R4118 and R4120 form a ramp generator.

Tuning System

The CTC185 tuner on the master boardis a single conversion, electronically aligned tuner with a hot/cold barrier. It is capable of tuning from 57 MHz through 801 MHz in three bands.

The tuning system used in this chassis is similar to tuning systems used in previous chassis. Tuner band switching and tuning frequency commands are sent to the tuner via the micro's clock and data lines and the tuner responds accordingly. Tuning sync is input to the control micro (U3101) at pin 12 and is periodically sampled using a sync presence detection algorithm.

IF Signal Processing

The IF signal from the tuner is processed by the Saw Filter (SF2301), then applied to pins 9 and 10 of the T4-Chip IC (U1001). Signal processing internal to U1001 generates baseband video, AFT and AGC signals. The AFT consists of a 12 stage counter that sends a digital count of the IF frequency directly to the microprocessor U3101. No alignment is required. The AGC signal is returned to the tuner to control the gain of the incoming RF signal.

Signal Processing

The tuner IF output is applied via a saw filter to the T4-Chip at pins 9 and 10. RF AGC is output at pin 5 of the T4-Chip and routed to the tuner. Video is output at pin 42. The video signal is then routed back into the T4-Chip with luminance applied to pin 38 and chroma applied to pin 40. The on screen display signals from the control micro are applied to the T4-Chip at pins 34, 35 and 36. The red, green and blue signals are output at pins 30,31, and 32 respectively.

All user control adjustments are bus controlled. They include brightness, contrast, color, tint and sharpness.

CIRCUIT OVERVIEW (Continued)

System Control

The control microprocessor (U3101) communicates with the rest of the chassis via two bus communication lines, clock and data. Clock is pin 20 and data is pin 19. The control micro receives commands from the user control panel or remote control and conveys this information over these two bus lines to the rest of the chassis.

Vertical Deflection

The vertical circuit in the CTC 185 is almost exactly like the circuit which was used in the CTC 175/176 family. The major differences are contained inside the T4-Chip. The power section is identical with the exception of some part value changes. Also the power supply for the vertical has been reduced to 23 volts but the name has remained the +26v_run supply.

The T4-Chip vertical registers are DC, Size, Linearity, 'S' correction, Size Compensation and Countdown Mode. The settings for 'S' Correction and Size Compensation will be contained in the microprocessor ROM and will not be adjustable. The Linearity control is a new ATE alignment and its value will be stored in the EEPROM. The DC and Size controls are instrument level alignments and they perform the same functions as they did on the CTC 175 except the alignment range has been made greater and the step size has been reduced.

The T4-chip contains an automatic level control circuit (Vertical Ramp ALC Filter) which maintains the vertical at a constant level even if the vertical interval changes which would happen if a non-standard video signal is used for example. Capacitor C4501 sets the time constant of the sample and hold circuit of the amplitude regulating servo circuit. If this capacitance were too small it would first have some affect on vertical linearity, and in extreme cases an instability could develop in the servo which would show up as a field to field vertical jitter.

The vertical signal is output from pin 15 on U1001. The signal is amplified by U4501 and sent to the yoke. Resistor R4517 provides a relatively high dc resistance which limits the current in the vertical yoke should the output IC fail. This resistor also reduces the vertical rate voltage ripple in the +12v_run supply to an acceptable level. Resistor R4518 acts with R4517 to form a voltage divider to reduce the half supply voltage to be approximately half of the +26v_run supply. Capacitor C4502 reduces the ripple on the half supply voltage. The parallel combination of R4502 and R4519 make up the current sense resistance to provide a voltage signal for the error amplifier to use. The resistor network RN4501 is used to provide a proportional feedback signal to U4501. Any voltage ripple in the half supply is nulled out because of the matched resistor dividers inside the resistor network. The voltage to current gain of the circuit is set by the value of the current sense resistors together with the resistor network. R4501 provides damping to prevent overshoot or undershoot at the amplifier output. R4507 and C4504 are useful in preventing oscillation.

Horizontal Deflection

The horizontal deflection system has two main functions in the CTC 185 chassis. First, it supplies the current for the horizontal yoke coils. Second, it provides a number of power supplies needed for operation of the chassis and picture tube. The horizontal yoke current is provided by a circuit consisting of a switch (HOT), the primary inductance of the IHVT, a retrace capacitor, the trace capacitor (S-Shaping capacitor) and the horizontal yoke coils.

The voltage supplies provided by the horizontal deflection system are derived from secondary and tertiary windings on the IHVT. The supplies are used by the video amplifier, the tuner, the CRT and the vertical amplifier.

The Horizontal AFC is the same as the one used in previous chassis models CTC 175 thru CTC187. The purpose of the automatic frequency control is to maintain proper synchronization between horizontal scan and the incoming sync signal. The T4-Chip (U1001) employs a two-loop approach to accomplish this task. The two-loop system uses one PLL to phase lock the horizontal oscillator and the incoming sync signal and a second PLL to lock the phase of horizontal flyback to that of the horizontal oscillator. The T4-Chip has a one bit register which can be used to change the gain of the AFC loop to obtain optimum performance. The register is called AFC gain and will be present in the CTC185 chassis. The external circuit at pin 21 of the T4-Chip is the loop filter for this PLL and is used to optimize the frequency response of the AFC loop.

The horizontal drive section of the T4 chip is the same as the circuit used in previous chassis models CTC 175 thru CTC 187. The output at pin 22 is an open collector which is low (on) when the horizontal output transistor is on. The pulse width is adjustable from 35 {sec to 37 {sec via bus commands to the T4-Chip register H-Duty. A buffer stage has been added to the horizontal driver in the CTC185 as in previous chassis. This consists of Q4302 and a handful of biasing resistors. This purpose of this circuit is to reduce coupling between the horizontal driver and low level circuits near the T4-Chip.

The T4-Chip obtains a regulated supply for those portions of the chip which must operate during standby via internal shunt regulator. This 7.6V standby supply is derived from the +12 volt standby supply and appears at pin 20 of the T4 chip. All other T4-Chip circuits use the 7.6 volt run supply in order to minimize standby power.

CIRCUIT OVERVIEW (Continued)

X-Ray Protection

The XRP in the T4-Chip operates the same as previous chassis models CTC 1 75 thru CTC 187. The XRP operates by inhibiting the horizontal drive output when the voltage at pin 24 exceeds an intemal reference of 3V +/- 4%. The pin 24 voltage is derived from the CRT heater voltage which is a good indication of anode voltage. Gain has been added via Q4901 to provide noise immunity and to avoid nuisance trips during kine arcs, ESD discharges, etc.

The XRP bit is latched after detection and is reset on the ON to OFF transition of the ON/OFF control. Thus the micro will have to toggle the ON/OFF bit in order to restart the set after XRP trip. As a protection feature the micro will also count the frequency of the XRP trips with respect to the time of day clock. If more than three XRP trips are detected in one minute, no attempt will be made to restart the set. At this point, it will be necessary for the customer to select OFF then ON to restart the set.

Sound Processing

Monaural Version

Preemphasized composite audio comes from the wideband audio output of the T4-Chip, pin # 6. Full deviation (25KHz) corresponds to 424 mVrms, +/- 2% by T-chip alignment. The WBA signal is deemphasized by a 2122Hz lowpass filter consisting of R1202/C1202 and applied to mono input pin 4 of the T4-Chip. Volume-controlled mono audio then exits the T4-Chip from pin 48. The audio is applied to the input of the monaural audio amplifier, U1950, through attenuator network R1902/RI951. This amplifier produces 1 watt into a 32 ohm speaker, with THD less than 1%.

A power ON/OFF pop suppression function, controlled bv the microcomputer, is furnished by Q1903 and C1950. The input signal to the mono power amplifier is shorted to ground momentarily when Q1903 is turned on or off, thereby preventing the DC transient which occurs at the T4-Chip output from coupling into the input of the mono power amp. C1950 charges slowly through R1902, which makes the DC power-up inaudible.

Stereo Versions

Wideband audio from the T4-Chip is decoded by U1701, the XS stereo IC. Stereo left and right signals are then routed to the T4-Chip, pins 2 and 4, respectively. Here the signals are processed by the volume control and mute functions, under microcomputer control. The signals exit the T4-Chip from pins 50 and 48 and are routed to the stereo power amplifier.

The integrated amplifier supplies one-watt per channel into 32 ohm speakers with less than 1% THD. Channel gains are set at 33dB by R1903/1904 and R1905/1906. R/C networks R1909/C1911 and R1907/C1907 provide resistive loads directly at the outputs of the amplifiers at rf frequencies to prevent instability. The speaker on/off function utilizes Q1903, R1915 and C1910 in conjunction with pin 3 of the power amp IC.

Composite wideband audio (WBA) from the IF enters pin 5 of the stereo IC, U1701. Reconstruction of the 2H subcarrier is accomplished by phase locking the transmitted IH pilot tone (from WBA, pins 1 and 2) and the divided-down 1H from the 24H crystal-controlled VCO (pin 22). The 2H subcarrier is picked off from a previous point in the counter chain. The low-pass filter for the phase locked loop, consisting of R1717, C1708, and C1709 is located between pins 3 and 4.

When phase lock between divided VCO and PILOT is achieved, 2H is allowed to pass to the (L-R) demodulator. Also, a stereo presence signal becomes present at pin 20, for use by the CTC185 control circuitry to illuminate the "STEREO" lamp. Logic high = mono (greater than 3.7 vdc.) Logic low = stereo (less than 0.6 volts)

If pin 21 (stereo/mono) is grounded (mono) by the microcontroller in response to a customer remote-control command, the pilot signal is blocked from reaching the (L-R) demodulator. Also, in this case, the stereo presence signal is forced to mono = logic high.

Autoprogramming

Autoprogramming is a feature which automatically programs the scan list by progressively searching for channels at the antenna input. Autoprogramming starts by determining if the TV is connected to a cable system or an "off-air" antenna.

NOTE: Because the system is looking for valid sync, weak off-air signals may not be programmed. These channels can, however, be manually programmed by selecting the Channel Memory feature in the Set Up menu.

Video Controls

The T4-Chip has dedicated registers used to control the video parameters (brightness, contrast, color, tint and sharpness). The volume parameter is also controlled by a dedicated register.

Non-Volatile Memory (EEPROM)

The EEPROM will be incorporated in all instrument models. These instruments will have non-volatile scan lists.