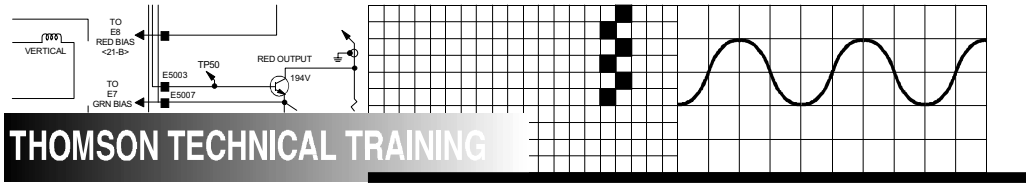


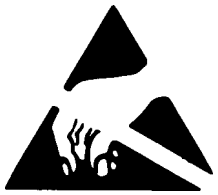
FOREWORD

This publication is intended to aid the technician in servicing the CTC195/197 television chassis. It will explain the theory of operation, highlighting new and different circuits associated with the digitally controlled chassis. The manual covers power supply, horizontal and vertical deflection, video signal processing, and audio signal processing theory of operation along with practical, proven troubleshooting methods. It is designed to assist the technician to become more familiar with the chassis operation, increase confidence and improve overall efficiency in servicing the product.

Note: This publication is intended to be used only as a training aid. It is not meant to replace service data. Thomson Consumer Electronics Service Data for these instruments contains specific information about parts, safety and alignment procedures and must be consulted before performing any service. The information in this manual is as accurate as possible at the time of publication. Circuit designs and drawings are subject to change without notice.

SAFETY INFORMATION CAUTION

Safety information is contained in the appropriate Thomson Consumer Electronics Service Data. All product safety requirements must be complied with prior to returning the instrument to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages and may expose themselves and others to possible injury.



All integrated circuits, all surface mounted devices, and many other semiconductors are electrostatically sensitive and therefore require special handling techniques.

First Edition 9726 - First Printing

Printed in U.S.A.

Prepared by
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Technical Training Department
PO Box 1976
Indianapolis, Indiana 46206 U.S.A.

THOMSON CONSUMER ELECTRONICS RCA PROSCAN®

Contents

General Features:

The CTC195/197 chassis is the latest in the Thomson Consumer Electronics line of digitally controlled television receivers. It relies on microprocessor control to govern the entire operation of the television, including consumer operation, system operation, system monitoring and maintenance. The control circuits are not only responsible for turning the set on and off, but also for aligning the different circuits such as deflection and signal. Adjustments that were previously aligned with a potentiometer on other chassis are now aligned digitally via the microprocessor with the values stored in the EEPROM (Electrically Erasable Programmable Read Only Memory). The CTC197 will eventually replace a wide range of current TCE chassis', including the CTC169 and CTC176/177 series direct view chassis. Video and audio feature requirements reflect a range of performance from previous core line products to midrange featured sets. The basic feature package will include dBx stereo, 8 jack panel, and an on-screen program guide.

Screen Sizes

The CTC197 covers direct view screen sizes from 27" to 35", measured diagonally. The CTC195 will be used in PTV screen diagonal sizes from 46" to 61".

The projection television CTC195 chassis utilizes the CTC197 basic chassis plus additional circuitry to adapt it for projection TV operation. The additional circuitry consists of the "Digital Convergence" circuit board and it's own dedicated power supply. The CTC195, unlike earlier PTV's that used analog convergence, uses the all new "Digital Convergence" circuitry to provide near perfect convergence and linearity. The CTC195 will replace previous PTV chassis CTC169, CTC178/188 and CTC187.

Video

The video performance of the CTC197 covers both low and mid levels. Models are specified to include comb filter and S-VHS (where 600 LOR (Lines of Resolution) is required) or non-comb filter without S-VHS (where 280 LOR is required). Auto Color and AKB (Automatic Kine Bias) are basic for all chassis versions.

Tuning

CTC197 tuners incorporate the necessary specifications to follow normally accepted cable TV tuning capabilities and will also meet the latest FCC "cable ready" requirments. Channel tuning is also enhanced through a Fast Tune option.

Audio

CTC197 audio circuitry includes dBx stereo and is configured for both 1 watt and 5 watt output version. The CTC195 will add a 10 watt audio amplifier.

The CTC197 contains a wide array of consumer selections and controls. Among them are:

Sleep Timer

The sleep timer has four hour functionality and can be set in increments of fifteen minutes. The OSD counts down time remaining when the sleep timer function is enabled. The Sleep Time function also includes a descending audio taper automatically implemented the last one minute of Sleep Timer operation.

On Screen Time and Channel Display

The On Screen Time and Channel features allows the current time and channel to be displayed on screen. This feature can be programmed for continuous display through a menu item (continuous display is not an option on PTV). This includes both AM and PM selections. In cases where time has not been set, only the channel will be displayed.

Factory Reset

Resets all consumer picture quality adjustments to one of three factory present conditions.

Auto Program

Automatically locates and enters into memory all active channels.

Commercial Skip

Commercial Skip is user implemented in thirty second increments up to four minutes and then 60 second increments up to one hour. When CS times out, the programming will return to the channel that was on screen when CS was initially entered. When CS is enabled in two tuner PIP sets, the original channel will automatically appear in the second tuner PIP. When CS times out, PIP is disabled.

Multilingual OSD

The CTC197 will support up to three customer-selectable OSD languages. Languages will include: English, Spanish or Portuguese.

Alarm Timer

The Alarm Timer feature permits the user to set the TV to come on automatically at a preset time every day. *The TV will automatically turn off after two hours if no other function is accessed by the consumer (i.e., volume, channel, etc.).*

Parental Control

The parental control feature permits the user to engage a secondary scan list with more limited channel choices. This may be used by parents to control the channel selection capabilities of the set when they are not able to supervise program selection.

Auto Tune (VCR/Cable/DSS Set-Up)

Auto select allows the user to select which channel or external input should automatically be selected when the VCR1, VCR/LD or cable/DSS key is pressed on the remote. Auto select set-up is accessible via on screen menu.

Channel Labeling

Channel labeling is permitted for no less than 28, four-character or 14, eight character labels.

Channel Directory

The Channel Directory Feature permits up to 28 channels and their consumer input labels to be displayed on-screen as an index. The channel directory presentation may consist of more than one display screen.

TV Guide Plus+

Displays program title, length, elapsed time, program description, channel labeling and EDS (Extended Data Service) broadcast early warning display in areas where the system is broadcast. A menu item assisting in the selection of "Eastern Standard, Central Western" standard time will be provided.

Closed Captioning

Field one and Field two of closed captioning are supported (CC1, CC2, CC3, CC4, T1, T2, T3, T4). CCD enabling is through TV menu selection.

Color Temperature

A three position, user-selectable color temperature switch is available via the on screen display system.

Interface

The CTC195/197 will support two levels of consumer feature operation. On select chassis versions, the basic interface will be augmented with an ICON based "Fetch" Menu. Highlighting and enabling a Fetch Icon automatically implements the set-up menu of the feature or enables it. Fetch Menu items include: sleep timer, front panel lockout, parental control, alarm timer, initial setup, and channel directory.

Mute

The Mute feature can be enabled via remote control or TV menu selection. Mute with automatic CCD (Closed-Captioning) operation is consumer selectable via a menu selection. When Mute and automatic CCD is selected the consumer CCD preference will automatically be displayed. If no consumer preference has been noted, CC1 will be selected. Text will not be permitted as an option.

Front Panel Lock-Out

Front Panel Lock-Out disables the front TV access buttons. It can be enabled through either the remote control or via menu option. Once enabled, the Front Panel Lock-Out feature can be disabled through either remote command or by disconnecting AC power to the set for more than sixty minutes.

Fast Track Tuning

The CTC197 will support, via the front panel or remote, a two speed tuning feature. When the channel up/down key is depressed, the set will continuously select and tune the next highest/lowest channel and displays it with OSD for 500 ms. If the channel up/down key is held down for three or more seconds, the Fast Track Tuning feature is enabled and the TV will select and tune the next highest/lowest channel at a more rapid rate.

Cable Ready

Provides the channel capacity to provide the accepted "cable ready" standard.

FPIP

Basic Color PIP (FPIP) will be an optional feature on select chassis versions. PIP features are similar to the CTC187 implementation including swap, and PIP continuous move. Channel labeling will only be supported in the main picture. PIP can utilize Aux 1 (or S-VHS) as the second video source. Where a second source is not available, both the big picture and small picture will be the same. Fast Track tuning is provided for either small or large pix.

Two Tuner PIP

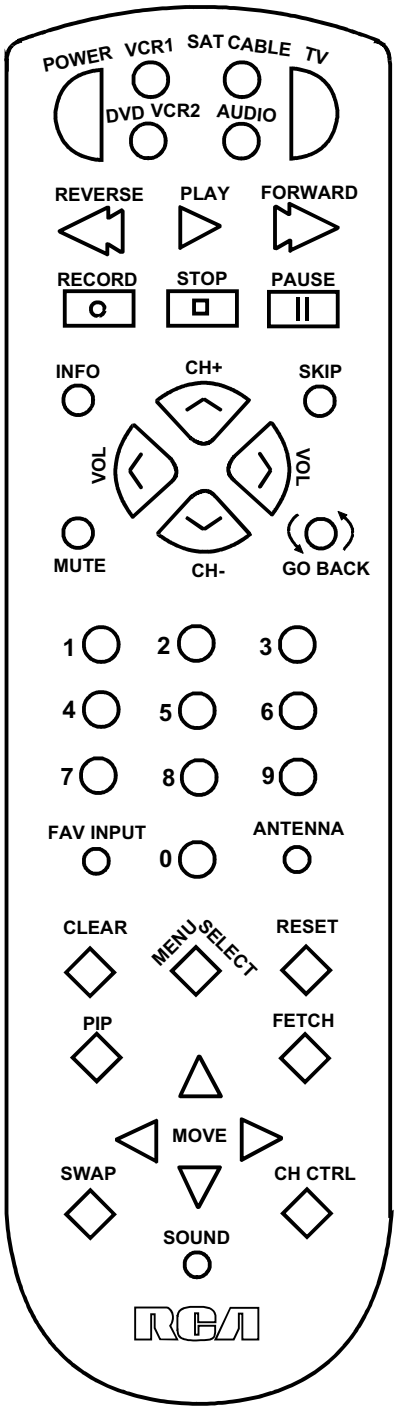
Two tuner PIP (T2FPIP) will be supported on select chassis versions. T2FPIP features will be the same as those of FPIP but also include channel labeling of both main and small PIP. Fast Track tuning is active for both small and large pix. The CTC197 does not support separate main picture vs PIP color controls.

A/V Jack Panel

The jack panel will include two video inputs, one pair of left and right audio inputs and an S-Video input jack. There will also be one pair of variable (hi-fi) left and right audio outputs.

S-Video

Select CTC197 chassis will support S-Video with auto detection of the signal when there is an active S-Video input. The S-Video input will replace Video Input 1.



CRK70 Series Remote Control

Comb Filter

A digital comb filter will be employed on select chassis versions. Comb filter versions will also support consumer switchable video noise reduction.

No Signal Present

When the TV is placed in the S-Video or Video Input mode, and no signal is present, a gray screen with the caption "No Signal Present" will be displayed.

dbx/SAP Audio

The CTC197 will support dbx/SAP. SAP (Separate Audio Programming) is a selectable user feature that is specific to the channel selected. When Commercial Skip is enabled while on a station broadcasting SAP programming, when the original channel is retuned, SAP is re-enabled.

Audio Speaker Select

A menu option will permit the customer to turn internal speakers on or off.

Treble/Bass/Balance

The audio treble, bass and balance may be adjusted from the menu system.

SRS (Sound Retrieval System)

Basic SRS is supported via OSD. SRS audio is implemented through the internal speakers. There is no external SRS speaker terminals.

Front Panel Controls

The front panel will provide Menu, Channel Up, Channel Down, Volume Up, Volume Down and Power buttons.

Remote Use

The CTC197 uses the CRK70, CRK74, CRK83, & CRK84 remote controls.

Technical Overview

The CTC197 was designed to provide a mid/high end replacement chassis for a broad spectrum of TCE product line.

The CTC197 chassis begins with a bus controlled, tuner on board concept similar to the CTC175/176/177 family and begins to expand on this base. The key developments in the CTC197 are the T4 Chip, the FPIP IC, and a new Stereo IC.

The new T4 (U16201), used in part in the CTC185 chassis, allows more bus control of adjustments and incorporates AKB (*A*utomatic *K*ine *B*ias) and places the calculations for AKB control with software.

The FPIP IC (U18100) is new to the CTC197 and allows bus control of PIP functions. Although similar to the DPIP found in the CTC187, the FPIP also incorporates video switching and a digital comb filter. A significant improvement over previous PIP IC designs is that it requires no external memory. All RAM is internal to the IC.

The audio stereo decoder IC (U11600) allows bus control of the dBx decoder by the I^2C bus. The tone, volume and balance functions previously performed by a separate IC, are now included in the stereo IC. In addition, two pairs of auxilliary line level inputs are available. The IC also contains a "loop out/in" function to facilitate connection of external processing circuitry such as SRS.

The SRS circuit used in the CTC197 was jointly developed by TCE and Hughes to provide a lower cost version of the system used in the CTC169 and CTC179.

The tuner uses tuner-on-board technology. The design is very similar to the CTC179 with two exceptions. First, the tuner must meet new FCC Class B requirments. New shielding was required to meet these specifications. Second, the main tuner uses the combined PLL/DAC IC first used in the CTC185.

The PIP tuner is similar to the CTC179-2 chassis second tuner.

Signal processing will be familiar to the technician. IF/Video/Chroma processing is again handled by the T-Chip and very similar to the CTC175/176/177 chassis. The T4 is the latest version. AFT changes from analog to I^2C digital control. The 4.5 MHz trap has been deleted from the IC. An external trap is now required.

The T4 also contains ACC (autoflesh/chroma autocolor control), black stretch, adaptive coring and the low level AKB functions.

The microprocessor is an enhanced version of the ST9 series previously used in the CTC187. New features include a new OSD to support the "Fetch" menu icons and an EPG (*E*lectronic *P*rogram *G*uide). The OSD is an anolog RGB system capable of 512 colors and 255 charactors. There also is increased ROM and RAM space.

The power supply is an isolating, variable frequency/variable pulse-width, switch mode supply using a separate control IC and MOSFET switch. The design provides for overcurrent and overvoltage protection. It can also be adapted over a wide range of inputs (90-270 VAC).

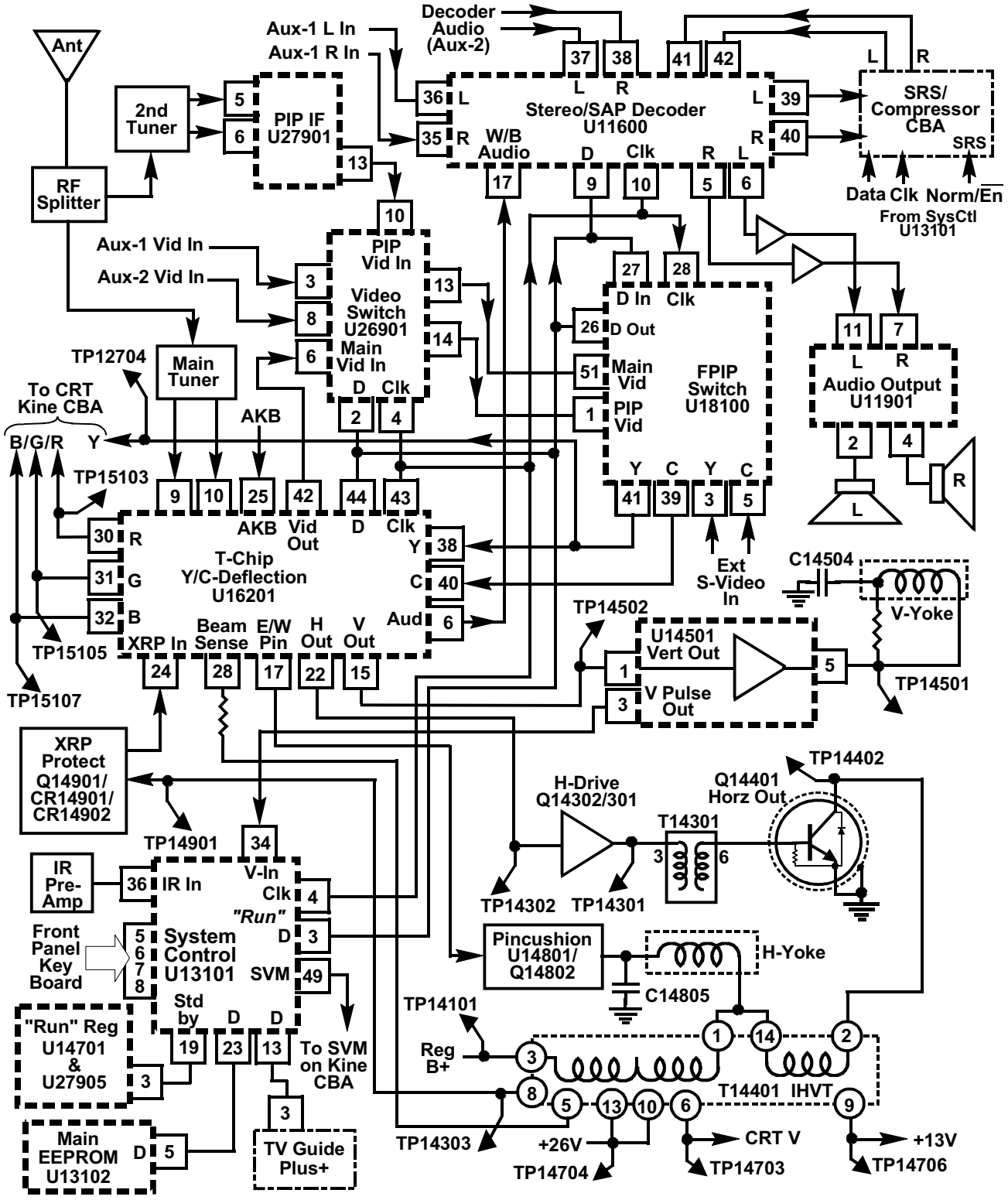


Fig. 1-1 CTC195/197 Block Diagram

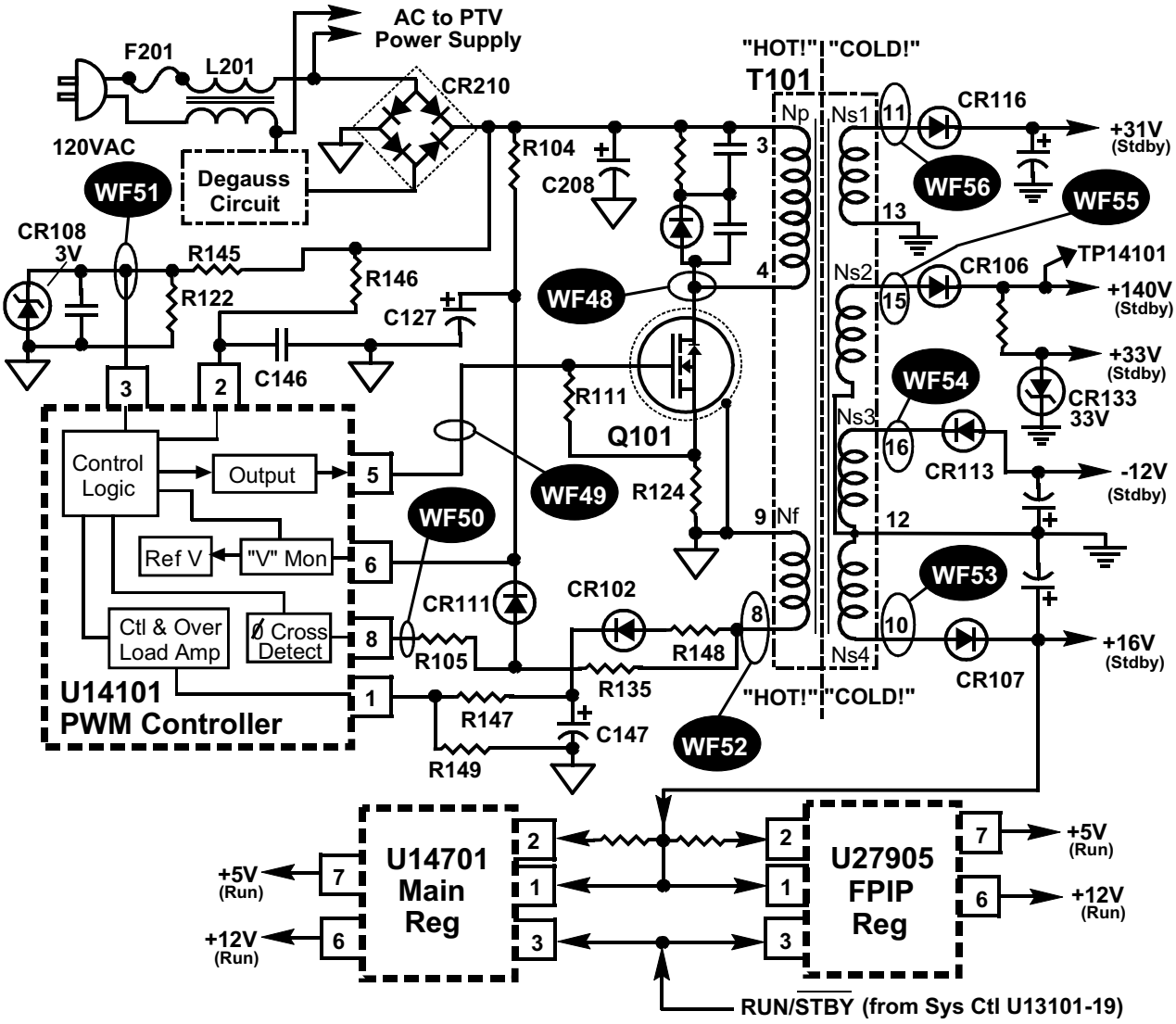


Fig. 2-1 Main Power Supply

See Waveforms Page 21.

CTC195/197 "Main" Power Supply

The CTC195 and CTC197 main power supply is a variable frequency/variable pulse width switch mode power supply (refer to Fig. 2-1). It uses a power supply controller IC (U14101) that drives the power MOSFET, Q101. The CTC195 & CTC197 are "cold" chassis and the electrical isolation between the power supply and chassis is achieved using the ferrite core transformer, T101. Energy is stored in the transformers primary winding during the power MOSFETS On time and is transferred to the secondary windings when the MOSFET switches off (flyback period). The transformer (T101) must expend all it's stored energy before the start of the next "On" period of the MOSFET. The power supply is self oscillating and the frequency is dependent on the load and the AC line voltage. The frequency can vary between 25kHz and 90 kHz. This supply uses "hot side" regulation which means that there is no actual physical sampling of the secondary voltages. The feedback winding (Nf) on the hot side of the transformer is tightly coupled to the Reg B+ windings on the secondary. Voltage variations in Reg B+ are reflected back into the feedback winding (Nf). The regulator IC U14101 has its own internal reference voltage. The power supply operates whenever it is connected to the AC line and supplies current on demand up to its current output limit. The maximum input power to the supply is 180 watts. A diagram of the power supply is shown in Figure 2-1.

AC In and Degaussing

The AC input to the supply is passed through fuse F201 and then choke L201. It then enters the bridge diode, CR210. C208 is the Raw B+ filter capacitor and the unregulated voltage at this point is approximately 150VDC at 120VAC input.

The degaussing circuit is connected in the line via thermistor RT201 and degauss relay K201. Power for the relay comes from the +12V RUN2 supply. The +12V RUN2 supply is only present when the instrument is turned on. The relay K201 is closed and current flows through the degauss coil and thermister RT201. This heats the thermistor and reduces the current through the degauss coil. After approximately 1.5 seconds the current through the thermistor falls enough that the relay de-energizes allowing the relay to open, ending the degauss cycle.

Power Supply Operation

When the instrument is first plugged into an AC source, approximately 150VDC Raw B+ is developed by the bridge rectifier diodes and the Raw B+ filter capacitor C208. This is coupled through the primary winding (Np) of T101 (pin 3) and to the drain of the power MOSFET (Q101) via pin 4 of the transformer. The source of the MOSFET is connected to ground through R124 (.22 ohm/2 watt). At the instant that the instrument is plugged in, the power supply is not operating and IC U14101 needs a source of power to turn on Q101 the first time. IC U14101 pin 6 (Vcc) receives B+ via resistor R104 which is connected to raw B+.

With B+ applied to pin 6 of the regulator, U14101 outputs a voltage at pin 5 that is applied to the gate of Q101. This turns the MOSFET (Q101) on for the first time and results in a current flow through the primary (Np) of T101 and Q101. The IC senses this current indirectly using a circuit consisting of C146 and R146. One side of R146 is connected to Raw B+ while the other side is connected to C146 to form a simple RC network. This network is connected to pin 2 of U14101. This is the primary current sensing input. The capacitor is held in a discharged state by pin 2 of IC U14101 until the gate of the MOSFET is turned on at which time C146 is allowed to start charging. With the MOSFET turned on, the current increases through it and the voltage on pin 2 of the IC also starts to increase. When the voltage at pin 2 reaches approximately 3 volts, the IC shuts off the drive to the MOSFET. At this point, the energy stored in the primary of transformer (Np) is transferred to the secondary windings. At the same time, the energy transfer is also coupled back into the feedback winding (Nf) between pins 8 and 9. The voltage developed at pin 8 of T101 is rectified by CR111 and filtered by C127. This voltage is applied to pin 6 (Vcc) of U14101 and now serves as the Run Vcc instead of the voltage across R104. The voltage across R104 is only used during initial start-up. After all of the energy is depleted in the secondary windings, the voltage at pin 8 of T101 starts to decay down to zero. This decreasing voltage is applied to pin 8 of the IC through R105. This is the zero crossing input to the IC. When this waveform goes through zero, it signals the start of another cycle and the IC turns the power MOSFET back on. Current will again start increasing through Q101 and the voltage on pin 2 of the IC starts increasing again.

Once the power supply is operating, a method is needed to regulate the output voltages. This is accomplished by the feedback input at pin 1 of IC U14101. The winding on pins 8 and 9 of T101 serves three functions. As already explained, it serves to power the IC and also serves as the zero crossing input to the IC. Its third function is to provide voltage feedback information from the secondaries back to the IC. The physical construction of the transformer is such that the feedback winding is tightly coupled to the Reg B+ winding on the secondary. For this reason, the voltage across the winding Nf closely follows the voltage fluctuations on the secondary. This voltage is rectified by CR102 and filtered by C147 where it is applied to a precision voltage divider. This divider is formed by R147 and R149. The output of the divider is connected to pin 1 of the IC U14101. If this voltage exceeds 400 mV, the IC terminates the drive signal to the MOSFET.

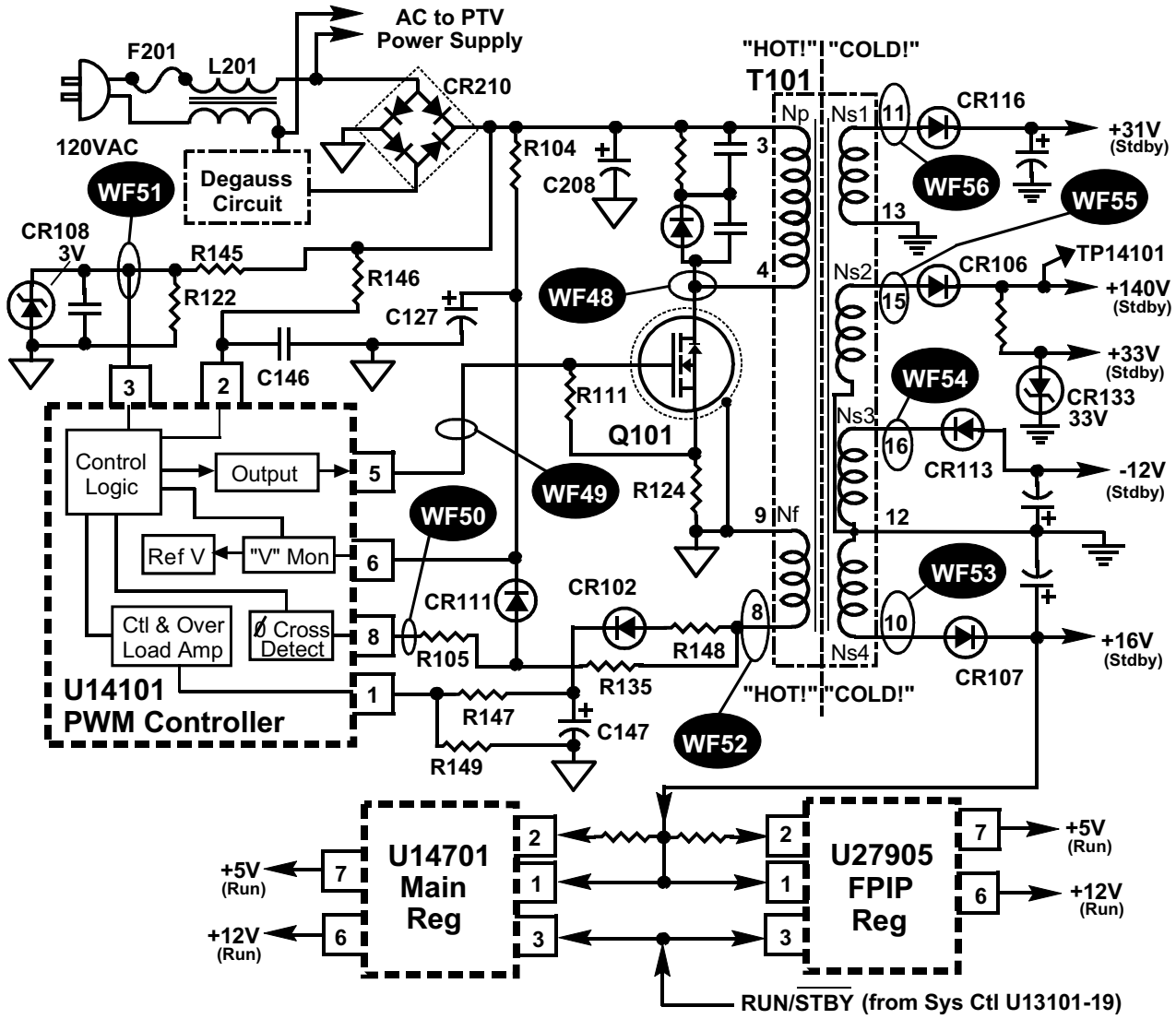


Fig. 2-1 (Repeated) Main Power Supply

See Waveforms Page 21.

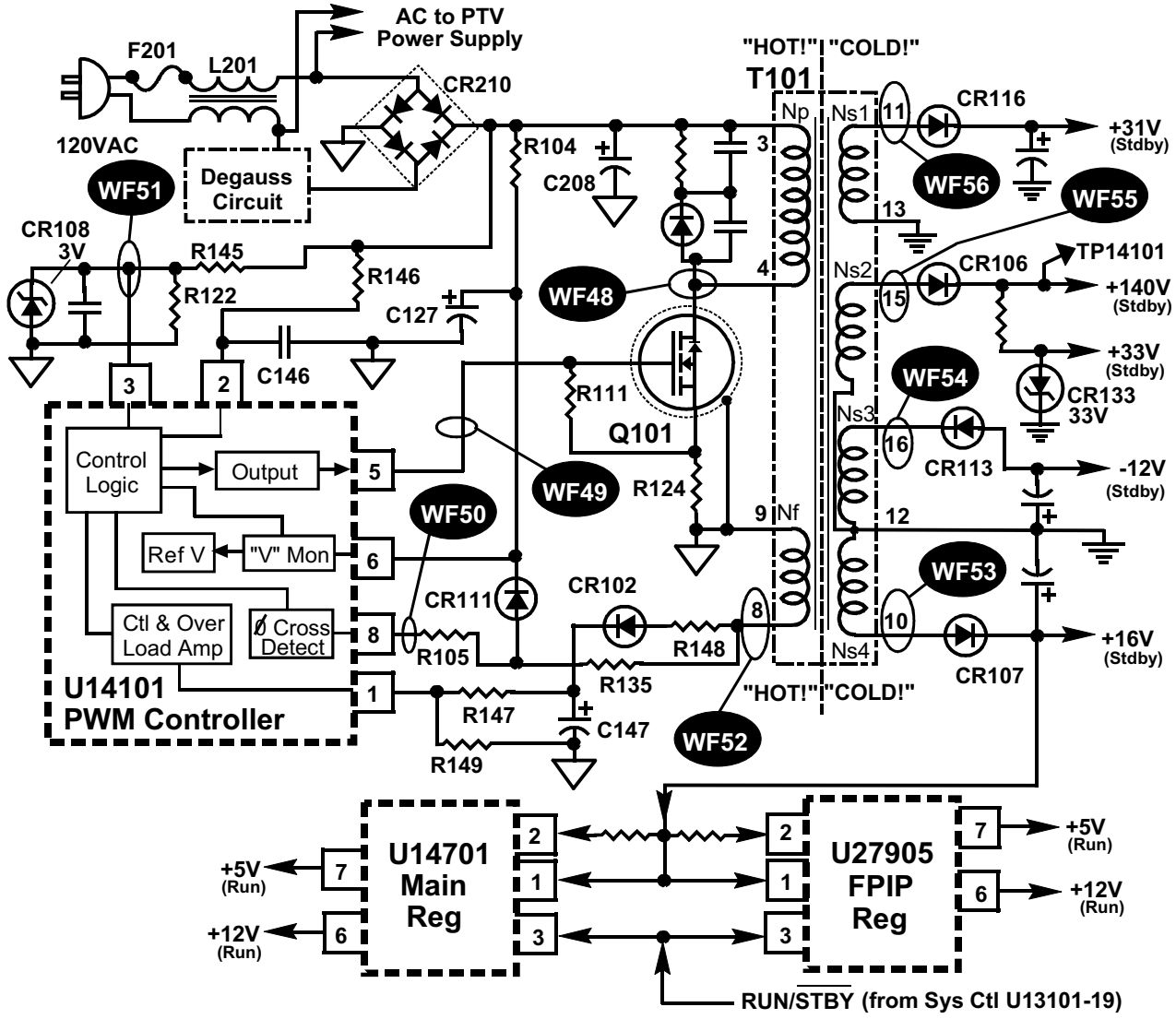


Fig. 2-1 (Repeated) Main Power Supply

See Waveforms Page 21.

In this way the output drive signal from pin 5 of the IC is regulated so that 400mV is maintained at pin 1 of the IC. The voltage divider is adjusted so that this corresponds to the required Reg B+ (»140VDC).

There are two ways of turning off the MOSFET. First, by exceeding 400mV on pin 1. Second, the voltage on pin 2 (primary current sense) exceeds 3 volts. Pin 1 senses the output voltage while pin 2 limits the maximum output current. If the output load increases, then more energy must be stored in the primary of the transformer. This requires the MOSFET be turned on longer. If it is on too long, C146 on pin 2 charges above 3 volts and shuts off the drive to the MOSFET, acting as overcurrent protection.

Now let's take a look at some of the other components in the power supply. R145 and R122 form a voltage divider from raw B+. This voltage is applied to pin 3 on the IC and forms a "Voltage In" monitor. If the voltage on pin 3 falls below approximately 1.0 volt the supply shuts down. This is to protect against "Low Line" voltages. The R/C/Diode network across pins 3 and 4 of T101 form a snubber network to help dampen any ringing when Q101 turns on and off.

Secondary Supply Operation

The output voltages on the secondary side of the supply are +140, +16, -12, and the audio supply which varies depending on which audio system in the unit. The secondary supplies are operational as long as AC power is applied to the instrument. Each of these voltages are provided by an individual winding on the transformer with a single rectifier/filter combination.

A 33 volt low power supply for the tuner is derived from the +140V supply. This supply is composed of a 33 volt zener diode and filter capacitors. A switchable +12 and +5 volts are provided by regulator U14701. These are both derived from the +16 volts. Pin 1 is the +16V input while pin 2 is the input for the +5V. The +16V at pin 2 is passed through a resistor which drops the +16 down to a lower value reducing the amount of dissipation in the IC. The outputs are filtered before being sent to the respective circuits. A unique feature of the IC is that their outputs are switchable (on or off) by a TTL control signal from the system control circuit. The outputs of regulator IC can be turned off by pulling pin 3 low. IC U27905 is the same type of regulator as U14701 but provides the supplies for the FPIP module.

Troubleshooting

Many of the malfunctions in the power supply can be quickly resolved with simple resistance and voltage measurements. However step-by-step check lists for some of the more common problems are provided below. One item in particular deserves special attention. If the main supply is not running, first check for presence of Raw B+. This can be checked at the +/- terminals of the Raw B+ capacitor C208. There should be approximately 150VDC at this point. If Raw B+ is present, connect an oscilloscope to pin 6 of U14101. If you see a oscillating or varying waveform of approximately 4.5 volts to 12 volts, then the IC is not getting enough Vcc voltage to run. As C127 charges through R104, the voltage on pin 6 of U14101 will rise, then fall when IC U14101 attempts to turn on.

At this point, it will begin to output pulses on pin 5 of the IC to turn on Q101. If the supply does not start the voltage on pin 6 starts to decay and the IC turns off. This process then repeats itself. The result is an oscillation on pin 6. The most likely cause is an open CR111. If CR111 is shorted, the voltage on pin 6 would be very low and there would be no oscillation. In any case, if the voltage is oscillating on pin 6 then the supply is not starting or is trying to start but not getting enough Vcc from pin 8 of the transformer to pin 6 on the IC.

Another important area that needs to be addressed is what happens to the power supply during a heavy load or a short on one of the outputs. During heavy load the voltage ramp on pin 2 of U14101 exceeds 3 volts and the supply shuts down in the current limit mode. At this point the power supply then tries to restart and if the load (or short) is still present, it shuts down again. This sequence repeats itself at an interval of approximately 1/2 second. A large amount of current will be flowing through the primary of the transformer as the supply tries to restart which results in an audible “chirp”. If you hear this, suspect a short on one of the secondaries such as a shorted horizontal output transistor, etc.

Symptom: Fuse Opens

Check for shorted Q101. If shorted, replace Q101 and check R124. If Q101 not shorted, check CR210 (bridge rectifier) for short.

If fuse opens again, suspect U14101 and varify Q101.

Symptom: No Raw B+

Check fuse F14201. If open, replace and check Raw B+. If fuse OK, check for output from bridge diodes (CR14210). If bridge OK, check surge resistor R14203.

Symptom: No Secondary Supplies

Check Raw B+. If Raw B+ not present, go to No Raw B+ check above.

If Raw B+ OK, use scope and check U14101-6 for oscillation. If oscillation present check for open CR111 or R135. If oscillation not present go to step 3.

Is power supply “Chirping”? If yes, check for shorts on the secondary side of supply. If no, check for shorted CR111 or shorted R135.

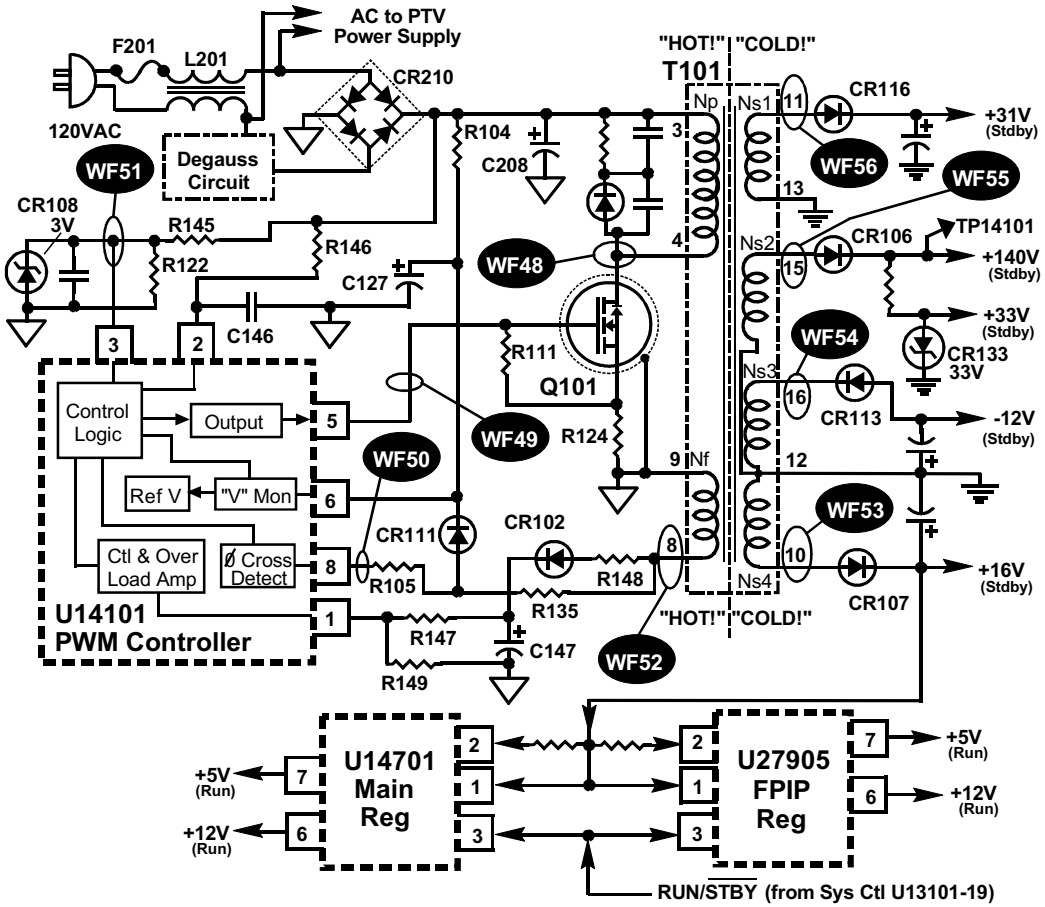
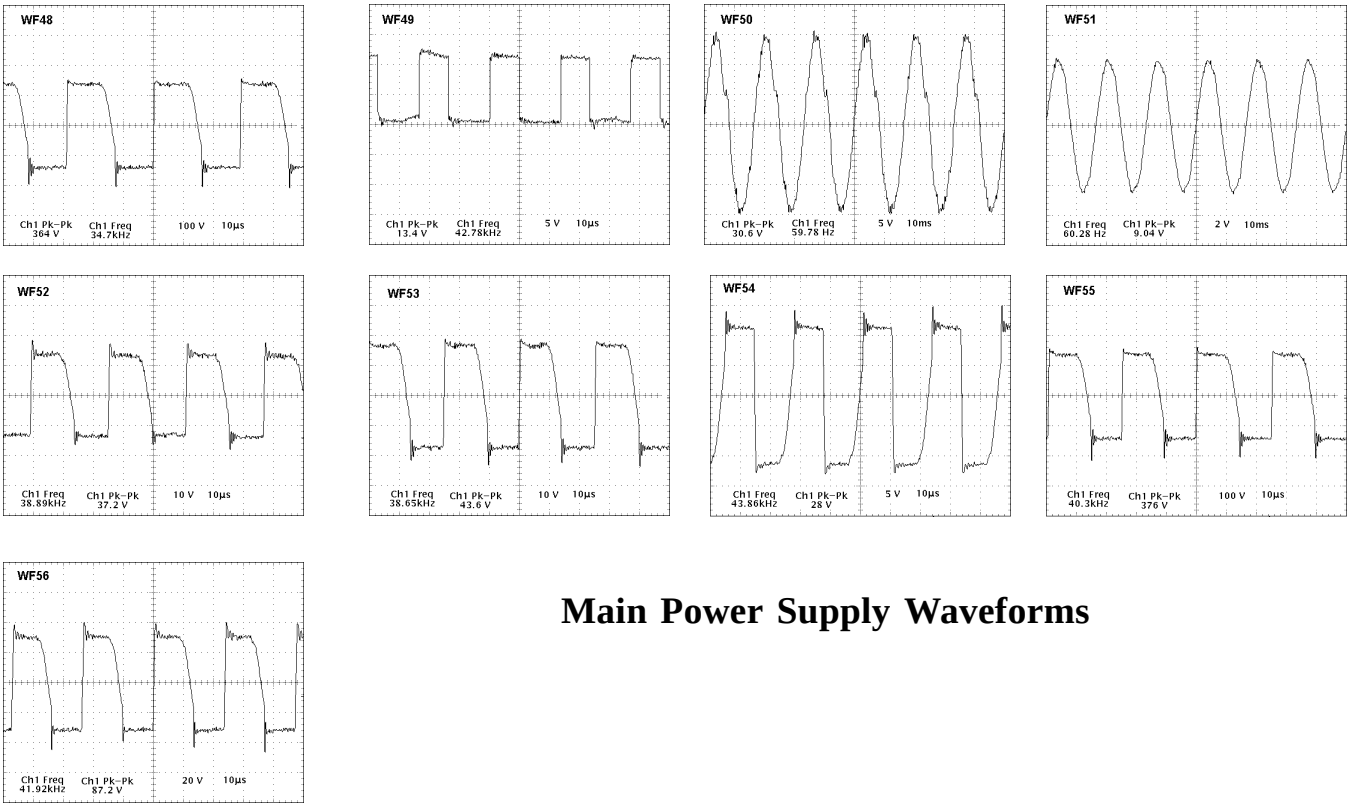


Fig. 2-1 (Repeated) Main Power Supply



Main Power Supply Waveforms

Auxiliary Power Supply Operation

The auxiliary power supplies on the Main CBA consist of three (3) regulator IC's U14104 (+7.5VDC), U18101 (3.3VDC) and U14601 (+5VDC). Series pass transistor regulator Q11600 provides the +9.5VDC supply. U14104, U18101 and Q11600 obtain their input voltages (+12V & +5V) from Main Regulator U14701. These power supplies are only On when U14701 is power up, which occurs only when the instrument is turned on. Regulator IC U14601 uses the +16VDC supply from the Main Power supply and outputs the StandBy +5V for the microcomputer and EEPROM. This power supply is always present whenever the instrument is plugged into AC power.

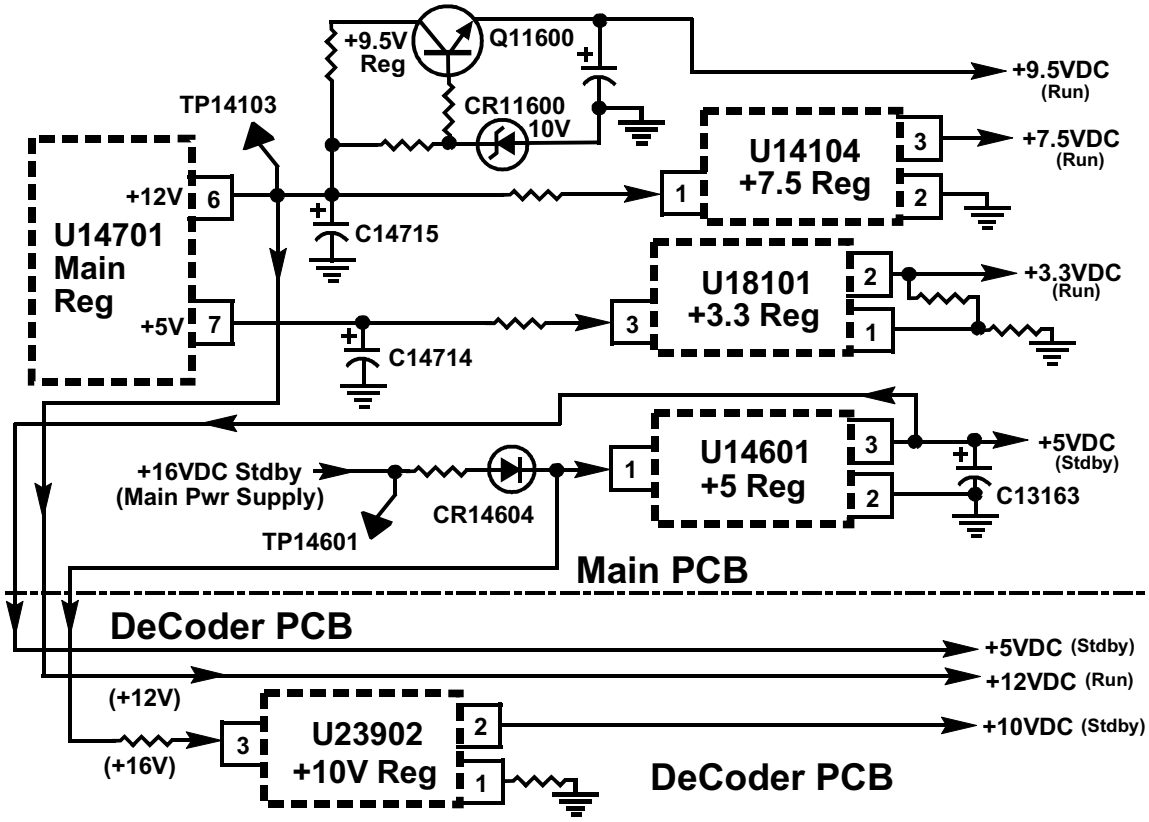


Fig. 2-2 Auxiliary Power Supply

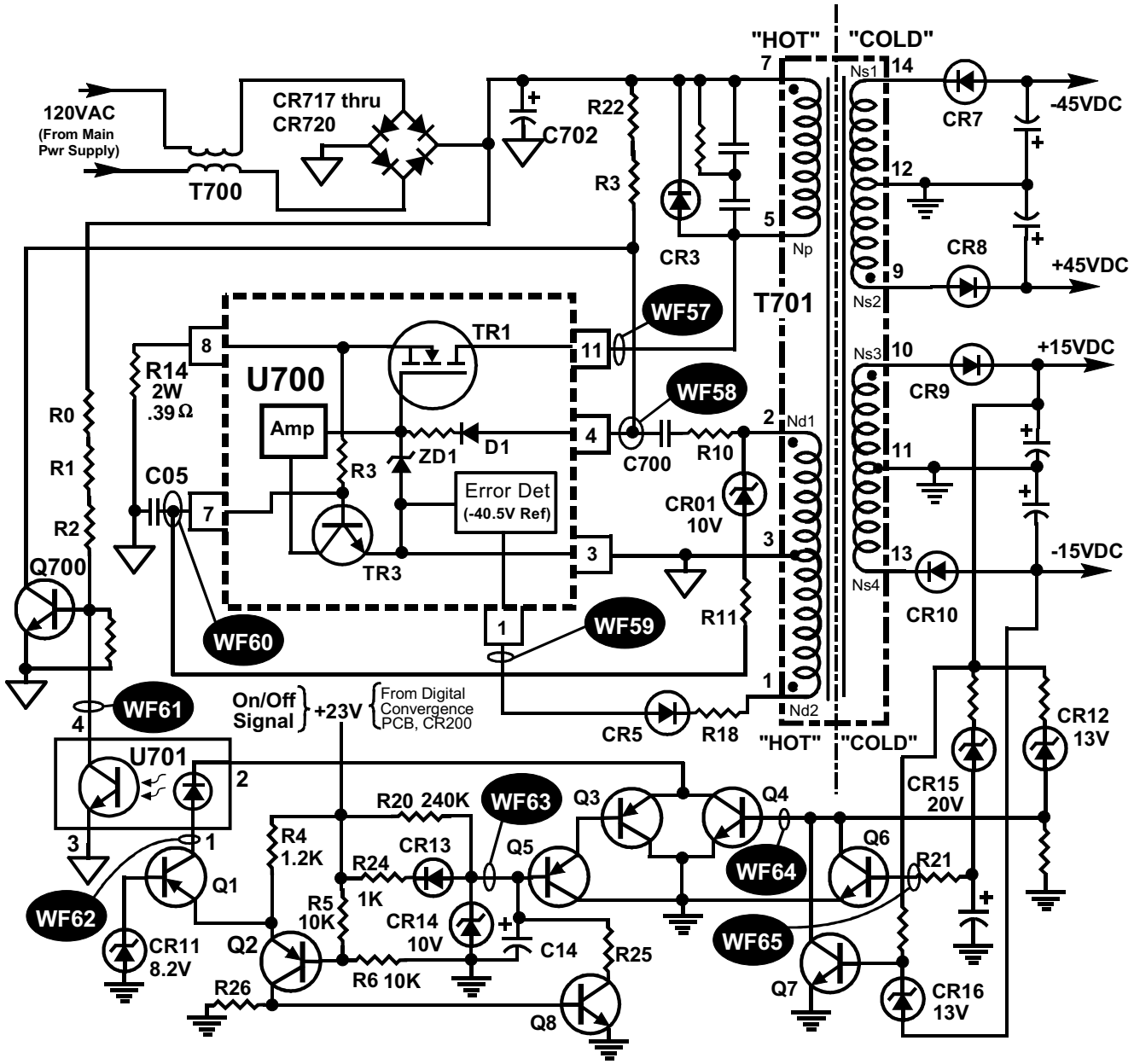


Figure 3-1 Digital Convergence Power Supply

See Waveforms Page 29.

CTC195 Convergence Power Supply Overview

The convergence auxiliary power supply is a variable frequency-variable pulse width switch mode power supply. AC power is supplied to the rectifier from the main chassis. The Raw B+ for the PTV power supply is generated by a bridge rectifier (CR717 thru CR720) and filtered by C702. With Raw B+ applied, the gate of TR1 begins to charge up through R03 and R22. When the turn-on voltage of the FET inside U700 (TR1) is reached, the FET begins conducting. With TR1 conducting, current flows through the primary (Np) of the transformer (T701), FET (U700), and through the current sense resistor R14 (U700-8). The current flowing through the primary winding causes a electromagnetic field to develop around the winding of Np (pins 7 and 5). As the field around Np rises a voltage is induced into winding Nd1 (pins 2 & 3). The voltage developed at pin 2 of T701 is coupled by R10 and C700 to the gate of TR1 (U700-4). The polarity of this winding is such that it generates a positive voltage which keeps TR1 conducting. When the current through TR1 reaches the current limit threshold set by R14 and C05, TR1 is turned off. When the FET (TR1) turns off, the magnetic field around the winding Np collapses and the energy stored in the primary of the transformer is transferred to the secondaries. As the field around Np collapse, a positive pulse is generated at pin 2 of Nd1 that is applied to the gate of TR1 turning it on again. This will continue for several cycles until stable oscillation is achieved.

The voltage developed across Nd2 rectified by CR5 and compared to an internal reference of -40.5V (+/- .5V) at pin 1 of U700. Once operation begins, this feedback winding controls the duty cycle of TR1. The Nd2 winding is responsible for regulating the output voltages. The duty cycle of the power supply is altered so that the voltage across Nd2 is maintained at -40.5V. The secondary supply voltage windings (Ns1 through Ns4) are wound so they reflect any load changes on the secondary back to winding Nd2.

During normal operation as the load on the power supply increases, the On time of the FET increases. This increased On time causes higher currents to flow through the FET and the primary winding of T701 (Np). When the voltage across R14 reaches approximately +.6V, TR3 (inside U700) turns on. This turns off the FET and causes the output voltage to decrease. Zener diode CR01 and resistor R11 are used to compensate for any fluctuations in line voltage that result in changes in the Raw B+.

Power Supply Operation

As mentioned earlier, the power supply starts when the gate voltage of the FET (pin 4 of U700) is allowed to charge up thus turning on TR1. However, the power supply only needs to run when the instrument is turned on. Transistor Q700 is responsible for hold the gate of the FET low (OFF) until an On/Off signal is received from the Digital Convergence CBA. When raw B+ is present, transistor Q700 is biased On via R700, R701 and R702. With Q700 on, the gate of the FET is pulled low thus preventing the power supply from starting. The On/Off signal is obtained from the digital convergence board by rectifying the filament pulse and is approximately +23V when the instrument is running. This On/Off signal voltage supplies the B+ to the emitter of Q1 via R4. This allows Q1 to turn on providing a current path through the photo-diode. When the ON/OFF signal reaches approximately 16V, Q1 allows current to flow through the photo-diode. Initially the current flowing through the photo-diode of the opto-coupler is supplied by Q3 on the ground end of the circuit. The components (Q5, C14 and R20) on the base of Q3 form a delay circuit that that turns off Q3 after a short delay to allow the supply to start and stabilize. When the +23V is present, capacitor C14 begins to charge up through R20. As the base voltage of Q5 rises, Q5 turns off, thus turning off Q3 removing the current path for the photo-diode. By this time the supply is up and running and the current path for the photo-diode (ground end) is provided via Q4. This allows the photo-transistor to remain on, keeping the base of Q700 grounded thus keeping it turned Off. This allows the gate voltage of TR1 to rise and the power supply to operate normally.

As mentioned earlier, the current path for the opto-coupler during normal operation is provided by Q1 and Q4. Q4 is turned on only when the +15V and -15V supplies are within a specific operating range. When an excessive load is put on the supply, the supply goes into current limiting. In order not to damage the convergence amplifiers, we need to turn off the supply whenever a major overload or over-voltage occurs. When the +15 of the -15 volt supply drops to approximately 13V the transistor Q1 is turned off. Since Q3 is already off (after the initial startup delay) the current path for the opto-coupler is removed. This causes the supply to immediately turn off until the instrument is turned off and back on again. Monitoring the +/- 45V is not required since a failure in the convergence amplifier causes a large enough load on the supply that the current limiting circuit within U700 will shut down the power supply. Q4 is biased on by the output of the secondary voltage supplies. In this way the secondary output is monitored for overload on the supplies or in the event that a supply is lost. Q4 monitors the +15V supplies for “Under 13V” (CR12) and Q6 monitors for “Over 20V” via CR15. If the +15V secondary output supply falls below 13V, Q4 turns off. If the +15V rises over 20V, Q6 turns on and grounds the base of Q4, turning it off causing the power supply to shut down because Q700 will turn back on. Q7 monitors the -15V supply via CR16. If the -15V supply rises to -13V (supply falls) Q7 turns on grounding the base of Q4. Whenever Q4 is turned off, this removes the current path for the photo-diode in U700. This causes the photo-transistor in U700 to turn off allowing Q700 to turn back on grounding the gate of the FET (TR1) thus shutting down the power supply.

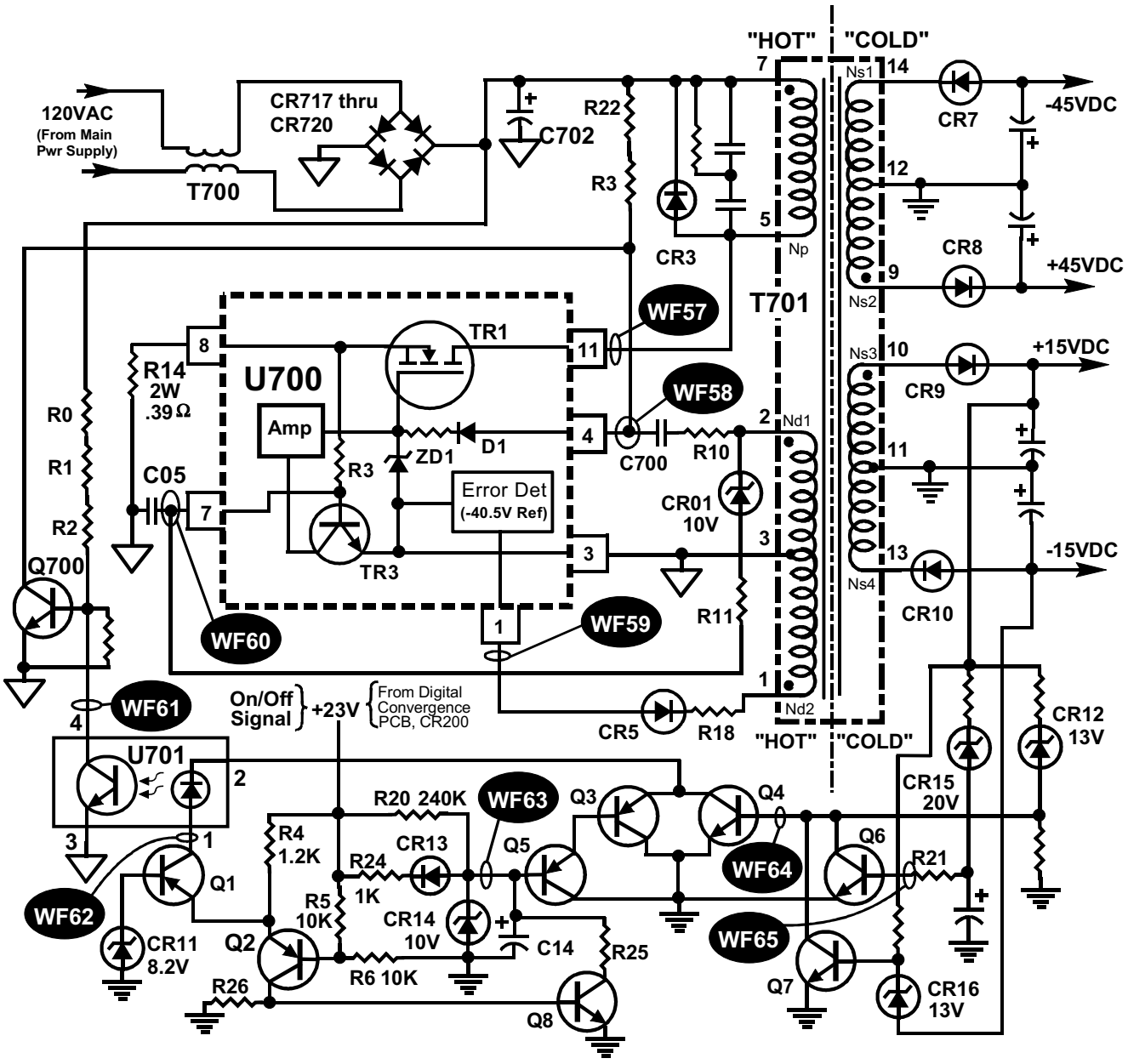


Figure 3-1 (Repeated) Digital Convergence Power Supply

See Waveforms Page 29.

The differential pair consiting of Q1 and Q2 alos control the turn off of the power supply. When the On/Off voltage starts to fall, the comparator switches the current to Q2 when the voltage falls below 16VDC. This allows current to flow into the base of Q8, turning it on. This discharges the voltage on C14 readying it for the next ON cycle. Since Q1 is off, current flow to the opto-coupler is stopped. With the opto-coupler turned off, Q700 turns back on and shuts down the power supply.

Transistor Q2 is responsible for monitoring the +23 volts from the convergence CBA. If the +23 volts starts to fall, Q2 turns on when the emitter falls below the level that the base is biased at via R6 and R5. When Q2 turns on the emitter of Q1 is grounded, removing its B+ supply and turning it off. This instantly turns off the opto-coupler U700. With the opto-coupler off, Q700 turns back on and shuts down the power supply.

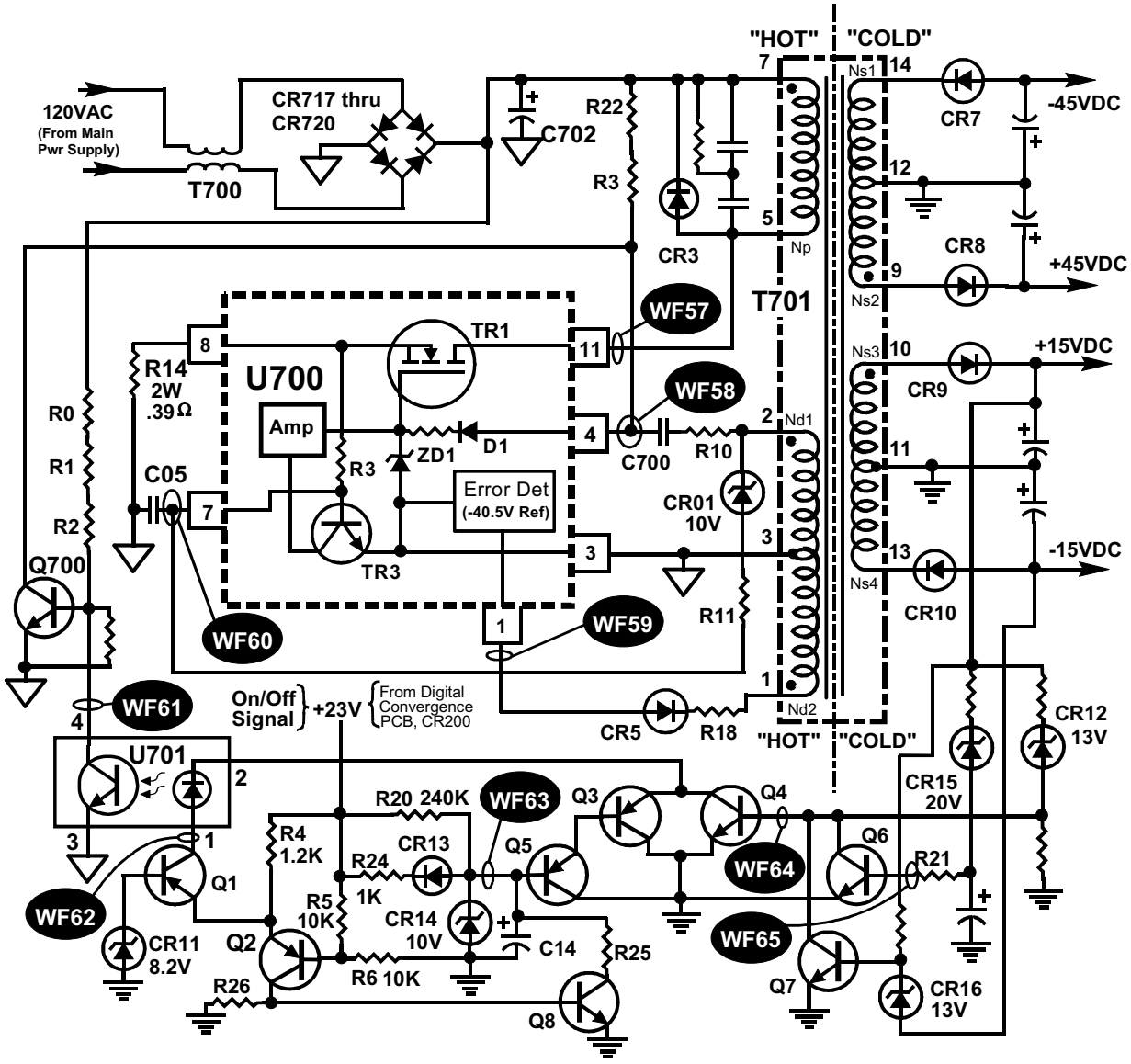
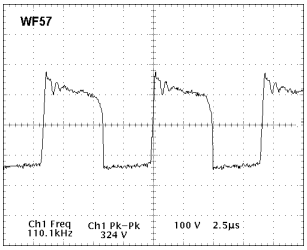
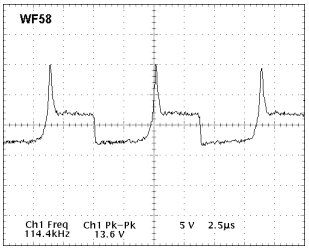
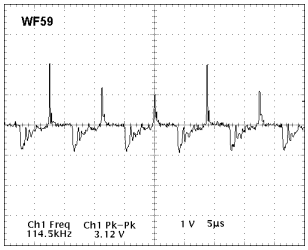
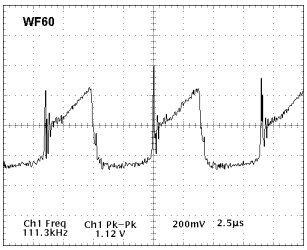


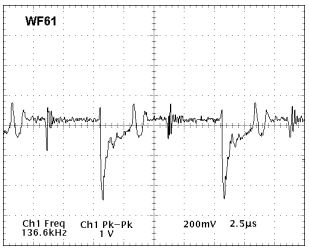
Figure 3-1 (Repeated) Digital Convergence Power Supply

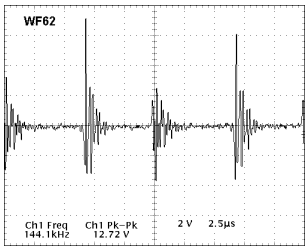


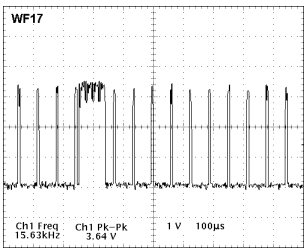


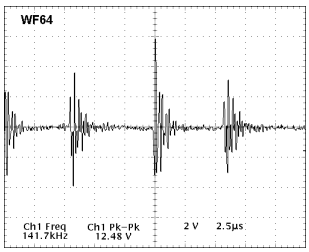


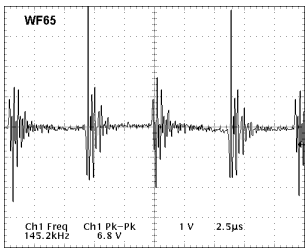












Convergence Power Supply Waveforms

Horizontal Deflection Overview

The horizontal deflection system has two main functions in the CTC195/197 chassis. First, it supplies the current for the horizontal yoke coils providing the energy necessary to move the electron beam horizontally across the face of the picture tube. Second, it provides a number of power supplies needed for operation of the chassis and picture tube.

The horizontal yoke current is provided by a circuit consisting of a switch (HOT), the primary inductance of the IHVT, a retrace capacitor, the trace capacitor (S-Shaping capacitor), and the horizontal yoke coils.

The voltage supplies provided by the horizontal deflection system are derived from secondary and tertiary windings on the IHVT. From the previous discussions of the power supplies, they are used by the video amplifier, the tuner, the CRT, and the vertical amplifier.

The low level signal processing circuits for the horizontal deflection system are contained in the T4 Chip. These include the horizontal sync separator and a two-loop horizontal AFPC system. The T4 allows bus control of several parameters associated with the horizontal deflection system including horizontal drive pulse width, AFC Gain, Sync Kill, and ON/OFF.

The XRP circuit in the CTC195/197 is similar to that of CTC179 and CTC185. A peak detector sets a latch in the T4 Chip. The latch can then be reset only by I^2C communication.

The T4 Chip also generates the ramp waveform used to drive the vertical amplifier. Bus-controlled vertical parameters include DC bias, amplitude, linearity, and S-Correction. The same ramp that is used to generate the vertical driving waveform is also used to create the parabola used for East-West pin correction. Bus controllable parameters in East-West pin correction include bias (width), amplitude (pin), tilt, and top and bottom corner. These same parameters are adjustable in both the CTC195 and CTC197. The CTC195 uses a slightly different method to achieve proper adjustment due to the Digital Convergence system. Discussion on that is provided in the Digital Convergence section of this manual.

East-West pincushion correction and horizontal width adjustment are provided by a diode modulator for the direct view CRT assemblies that do not include yoke pin correction. The modulator is driven by a linear pincushion driver. The parabola used to develop the correction waveform is generated in the T4 Chip. The T4 provides bus control of the horizontal width and pin amplitude as well as horizontal trap and corner correction. In addition, a voltage developed across the high voltage return resistor is summed at the pin driver to compensate for the decrease in width that occurs as the high voltage increases with decreased beam current.

A new feature in the CTC197 chassis is the bus controlled Z-Axis correction. This will allow Z-Axis correction via the remote control, making it much easier for the user than prior back panel switches. This circuit is used in 32" and larger direct view instruments.

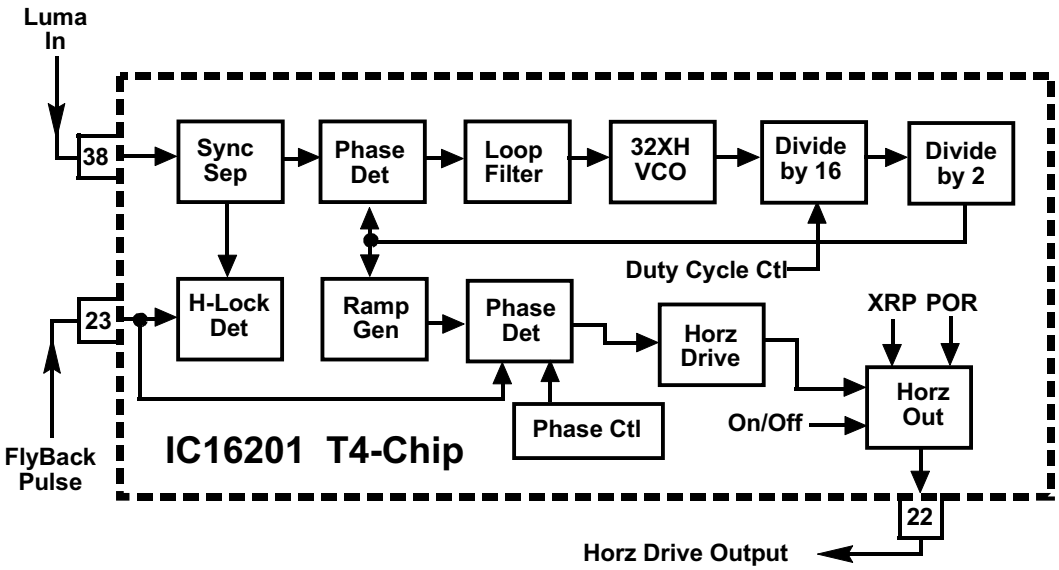


Figure 4-1 T4 Chip Low Level Horizontal Processing

The T4 Chip employs a two loop horizontal AFC system. The first loop is used to lock an internal 1H (standard horizontal rate) clock to the incoming horizontal sync signal. The second loop is used to lock the 1H clock to a feedback pulse derived from a secondary winding on the IHVT. As with the other T-Chip versions, a horizontal-to-video phase control is available via the I^2C bus. The phase control can be used as a horizontal centering control during instrument alignment.

The first loop employs a 32H (32 times the Horizontal Frequency) VCO referenced to a 503 kHz ceramic resonator. To offset sync confusion caused by various copy protection schemes, the T4 Chip provides a ±4 µsec window to capture sync and ignore other pulses.

U16201 (T4-Chip) performs the low level horizontal processing. The functions performed in U16201 are very similar to previous chassis. The horizontal processing circuits contained in U16201 are:

- Horizontal Automatic Frequency Control (AFC)
- Horizontal Automatic Phase Control (APC)
- Horizontal Drive
- East West (EW) Pincushion Correction
- X-ray Protection
- Horizontal Vcc Standby Regulator

Horizontal Circuits

AFC and APC

The purpose of the AFC (*A*utomatic *F*requency *C*ontrol) and APC (*A*utomatic *P*hase *C*ontrol) is to maintain proper synchronization between the beginning of horizontal scan and the incoming sync signal. The T4 Chip employs a "two-loop" approach to accomplish this task. The first loop is the AFC and second loop is the APC. The AFC phase locks the horizontal oscillator to the incoming sync signal frequency. The APC locks the phase of the horizontal output to the phase of the horizontal oscillator. This system is superior to previous designs because it is continuously adjustable for excellent noise immunity in the presence of marginal input signals and can track rapid phase changes in signals from VCR's or similar devices. The external circuit at pin 21 of U16201 is the loop filter for the phase lock loop (PLL) and is used to optimize the frequency response of the AFC loop.

The APC loop is used to track out the phase errors due to variable delays in the horizontal driver and output circuit. The APC has a two bit register (APC Gain) that controls the gain of the APC loop. APC Gain, like AFC Gain, is preset at the factory and cannot be adjusted by the service technician. The reference signal for this loop is a flyback pulse applied to an RC network and input to U16201 pin 23.

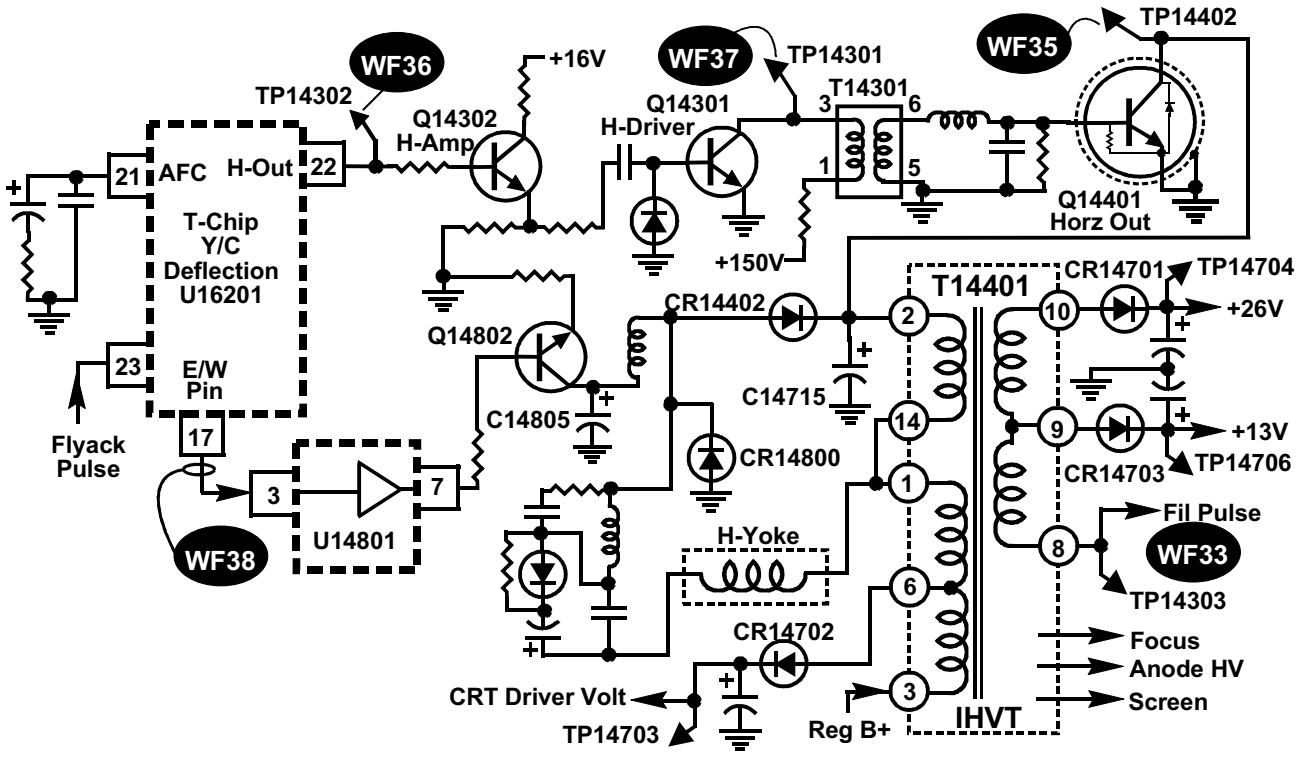


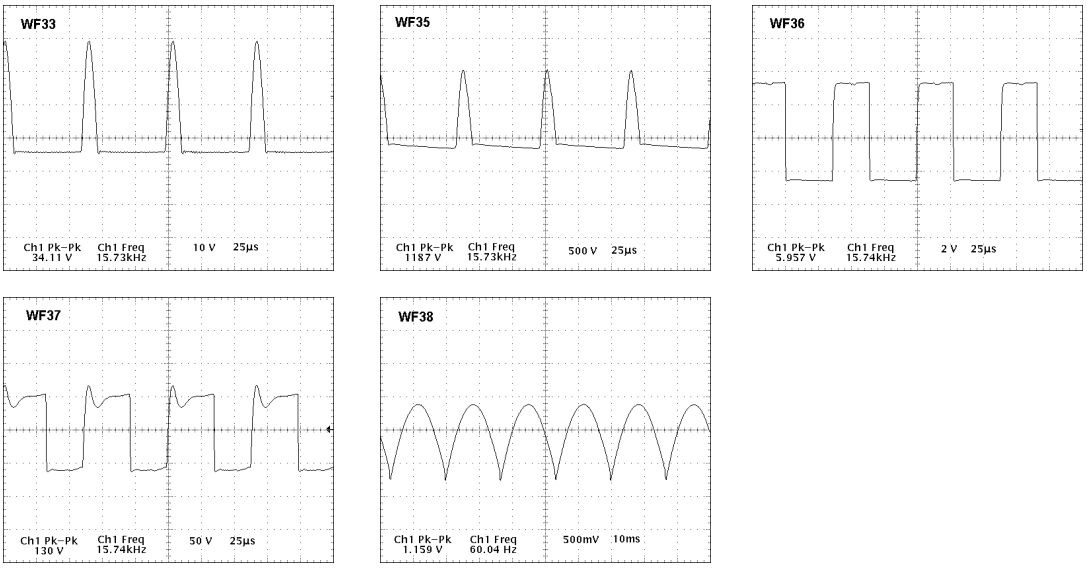
Figure 4-2, Horizontal Circuitry Block Diagram

Horizontal Driver

The horizontal driver circuit serves as an interface between the low level horizontal output of the T4 Chip and the high power horizontal output circuit. The driver operates in a typical flyback configuration. Energy is stored in the driver transformer, T14301, during the conduction cycle of Q14301. When Q14301 turns off, the stored energy is dumped into the base of Q14401, the horizontal output transistor (HOT). A buffer stage, Q14302, has been added between the horizontal driver, Q14301, and the T4 Chip to reduce the amount of current that must be handled by the T4 Chip output stage.

Horizontal Output

The horizontal output circuit generates the high current ramp waveform used to drive the horizontal yoke. It also drives the flyback transformer, which in turn produces the hi-voltage supplies necessary for picture tube operation. The supplies include hi-voltage, focus supply, screen supply, cathode B+, and the heater voltage. Additional secondary supplies are provided for use by the vertical amplifier.



Horizontal Waveforms

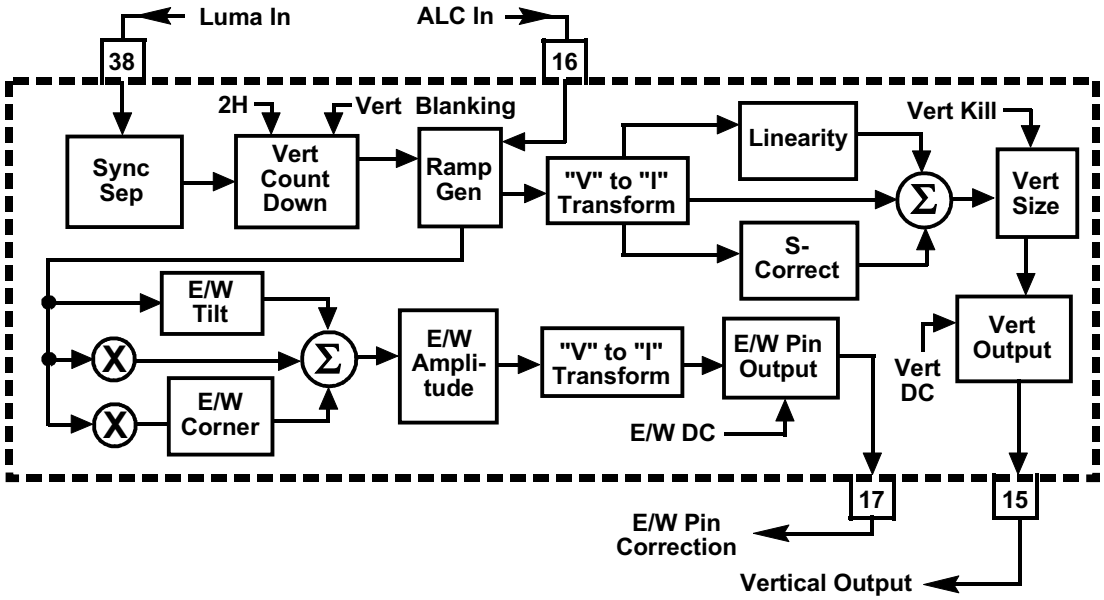


Figure 4-3, T4 EW Pin Correction Processing

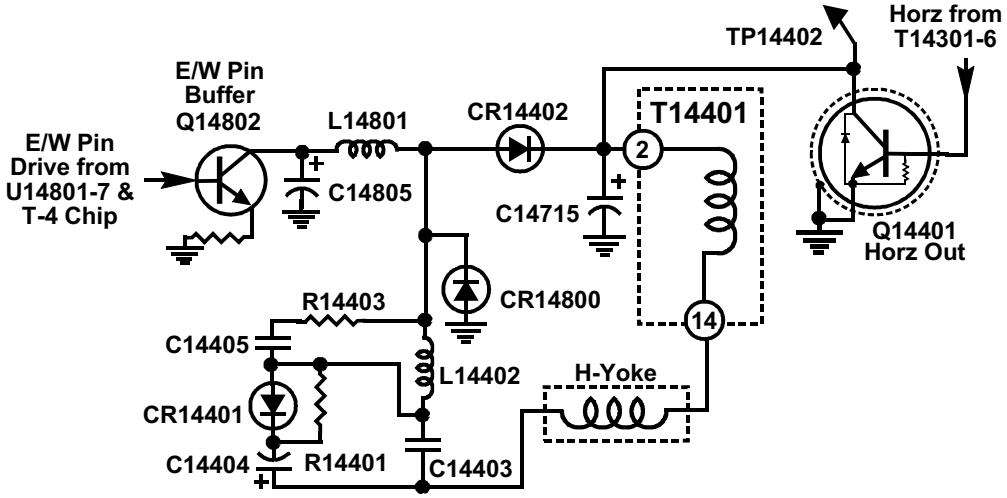


Figure 4-4, E/W Pin Correction Modulator and Components (CTC197 Only)

E/W Pin Correction & S-Correction (CTC197)

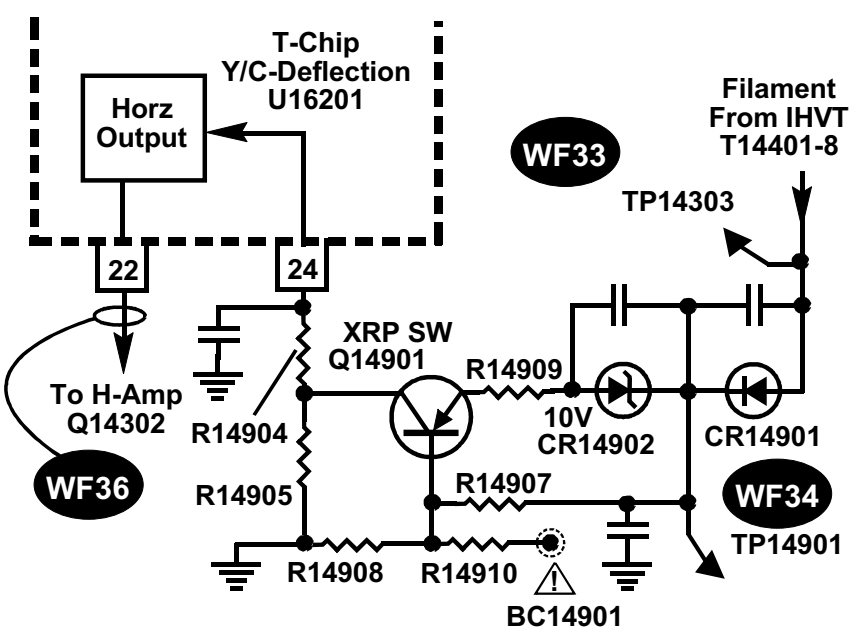
The horizontal processing circuits of the T4 contain provisions for geometry correction including vertical linearity correction, vertical S-correction, and EW pin correction. Horizontal linearity correction is provided by the linearity coil, L14402. The parallel damping network consisting of C14405 are included to reduce ringing in the linearity coil at the beginning of scan. S-correction is achieved inside the T4 Chip and further by the S-capacitor, C14404. Another parallel network is added to the S-capacitor to reduce further raster deformations. This network consists of C14401, R14401, and C14403. EW pin correction is done by a diode modulator circuit. Figure 4-4 is a simplified schematic which illustrates the principle of the diode modulator.

> **Note:** EW pin correction is not needed in 25" and 27" IR sets. These sets use pin corrected horizontal yokes.

Figure 4-4 shows the circuit arrangement of the diode modulator. The pin correction circuit controls the voltage at the junction of L14801 and C14805. Since the amount of horizontal scan is proportional to the voltage across the S-capacitor, C14404, the pin circuit can control the amount of horizontal scan by controlling the voltage at the bottom of C14404. The voltage at the top of C14404 is essentially held at reg B+. To achieve pin correction, a vertical rate parabolic waveform is produced by the pin circuit and applied to the S-capacitor, C14404. This, in turn, produces the desired modulation of the horizontal scan. Another feature of the diode modulator is that it allows width adjustment. This is achieved by varying the dc voltage at the bottom of the S-capacitor.

E/W Pin Correction & S-Correction (CTC195)

E/W Pin Correction and S-Correction are accomplished differently in the projection chassis version CTC195 chassis. See the chapter on Digital Convergence for an explanation of this circuit.



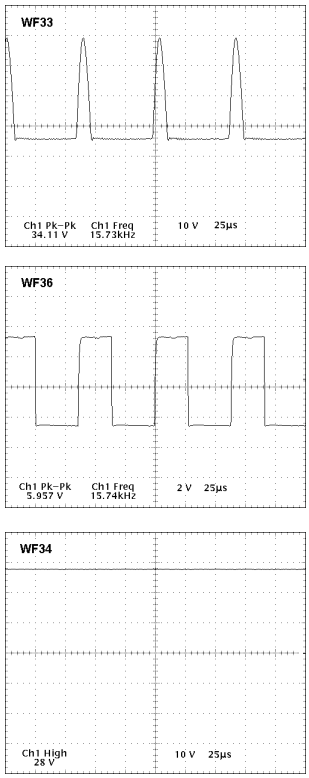


Fig 4-5, XRP Block Diagram

X-Ray Protection Circuit

The X-Ray Protection (XRP) circuit used in the CTC197 is contained in the T4 Chip. The input for XRP is pin 24 and is used to turn the Horizontal Drive Output on and off. A reference voltage of 3 Volts ±12 mV (4%) is generated inside the T4 chip. The reference voltage is produced by a bandgap reference, which is very stable even under temperature differences. If the voltage at pin 24 exceeds the 3 volt reference, a latch is set inside the T4 which inhibits, or turns off, the horizontal output circuit. This action defeats the ability of the chassis to produce high voltage, thus eliminating an X-ray threat.

The XRP detector voltage is produced by a secondary winding, pin 8, on the IHVT. This output is designed to closely track high voltage. The pin 8 voltage is peak detected by CR14901, thus producing a dc voltage proportional to the high voltage. This voltage is applied to the precision resistor divider consisting of R14907 and R14908. The values of the divider are carefully chosen to produce the correct XRP trip threshold for each picture tube. If the voltage across R14907 becomes large enough, Q14901 turns on, allowing current to flow through R14905. When the current becomes large enough, the voltage at R14905 exceeds the 3 volt level of the XRP comparator in the T4 Chip and the XRP latch is set.

The only way to reset the XRP latch is by a transition of the T4 on/off register. To restart the horizontal output after an XRP trip, it is necessary for the micro to send the T4 an “off” command, then an “on” command. For a typical XRP trip, the micro will try to restart the horizontal output after a short time delay of around 1.5 seconds without user intervention. However, if the micro counts three of these attempted restarts within a minute, the system shuts down and an error, 8 (XRP) will be logged. At this point it is necessary for the customer to turn the set back on via the front panel or the remote.

Z-Axis Correction

The Z-Axis correction circuit is used to counteract raster rotation when the picture tube is oriented in a north or south direction. This is accomplished by adding a DC magnetic field to counteract the Earth's magnetic field.

On 32" screen sizes and larger, the CTC197 will use a microprocessor controlled approach to Z-Axis correction. The microprocessor controlled approach is superior to the back cover switch approach in several ways. First, it frees valuable space in the back of the instrument since no manual adjustment is required. It also allows adjustment to be performed from the front of the receiver making control much easier for the service person or the customer. Also, since the control circuit utilizes an eight-bit D to A, much finer resolution is possible. Linearity of the output and sensitivity to component variations was improved by using the approach shown in the figure below.

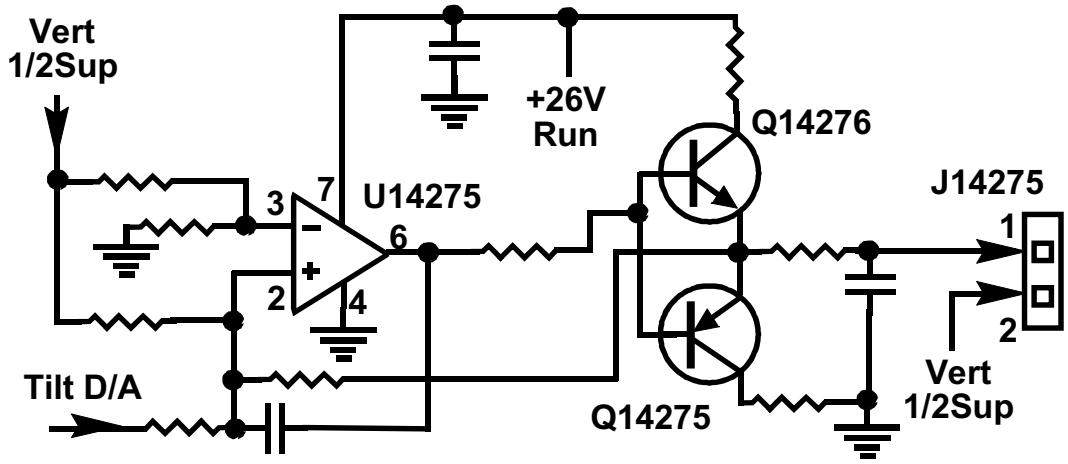


Figure 4-6, Z-Axis Correction Circuit

Troubleshooting

Dead Set

A failure in the horizontal circuitry will most likely cause a dead set symptom.

1. Check the collector of Q14401 for +140 volts. If missing, check for a shorted Q14401 and troubleshoot the power supply. If present, go to the next step.
2. Check for 7.6 volts on pin 20 of U16201. If it is not there, check the 12 volt standby supply. If it is there go to the next step.
3. Check pin 22 of U16201 for horizontal drive pulses when the power button is pressed. If no pulses are seen, see dead set troubleshooting in the “System Control" section of this publication. If they are present, go to the next step.
4. Check for horizontal drive pulses on the emitter of Q14302 and the collector of Q14301. If they are missing, check the corresponding stages. If they are present, go to the next step.
5. Check the drive to signal to the base of the horizontal output transistor, Q14401. If it is present, suspect a defective Q14401. If it is not, suspect a defective T14301

No Horizontal Sync

1. Make sure the problem is a horizontal sync problem by comparing the horizontal drive signal to incoming video sync (one complete horizontal drive cycle begins and ends with the horizontal sync in the video).
2. Check for the AFC feedback signal to pin 23 of U16201. If missing, trace it back to T14401, the IHVT. If the signal is present, go to the next step.
4. Check the AFC filter voltage on pin 21 of U16201 with service data. If it is incorrect, suspect the components off pin 21.

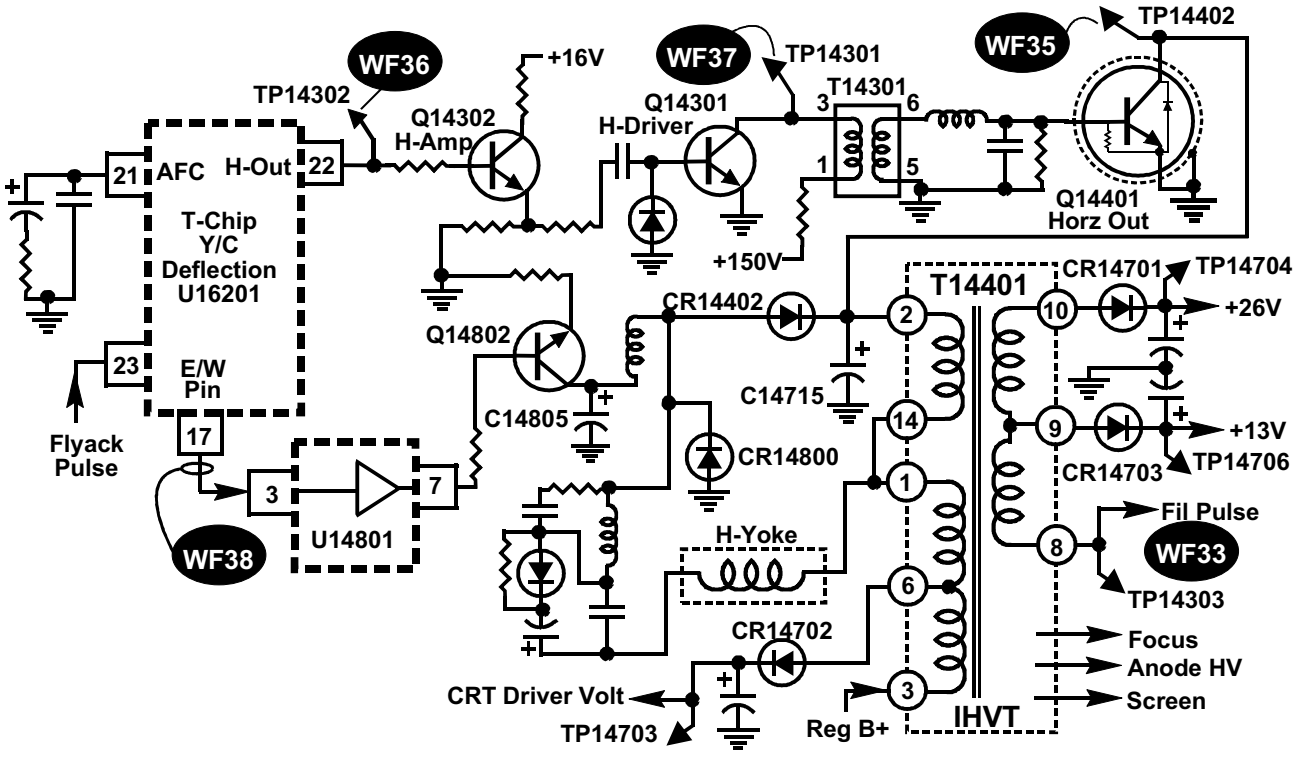
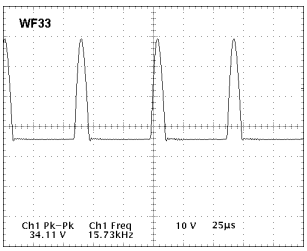
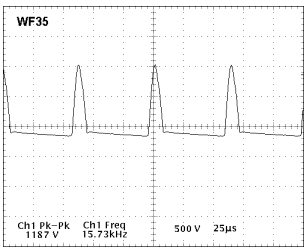
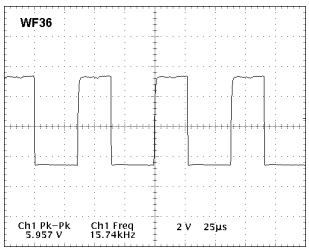
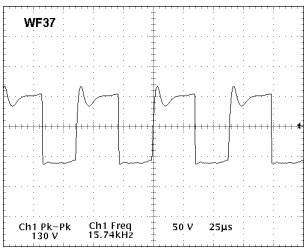


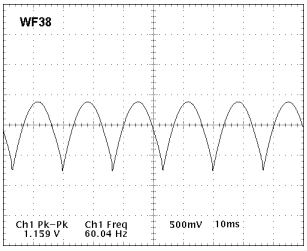
Figure 4-2 (Repeated), Horizontal Circuitry Block Diagram











Horizontal Waveforms

See Waveforms Page 44

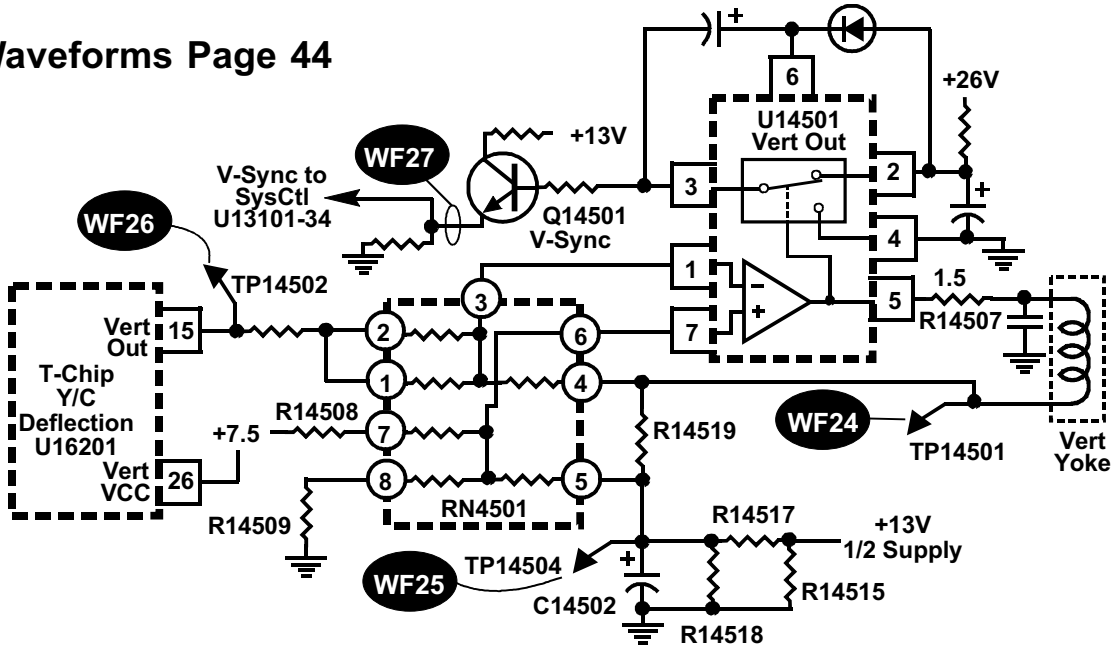


Figure 5-1, Vertical Deflection Circuit

Vertical Circuits

The vertical circuit in the CTC195/197 is very similar to the CTC179/189 and the earlier CTC177 vertical circuits. Like the earlier chassis, the output amplifier is DC coupled instead of capacitively AC coupled. The DC coupled circuit has the advantages of fewer parts, lower cost and linearity becomes less dependent on electrolytic capacitor tolerance and aging. "S" correction, the tendency of the horizontal lines to be spaced closer at different points in the screen, is accomplished inside the T4-chip.

Because of DC coupling, the DC level of the vertical reference ramp from U16201 pin 15 affects vertical centering. This allows vertical DC (vertical centering) to be included in the digital alignments. By moving the vertical ramp higher or lower around a DC voltage, vertical centering can be accomplished. This also compensates for tolerances in the reference ramp DC voltage.

The vertical circuit acts as a voltage to current converter. It changes the vertical rate DC ramp signal out of the T-Chip to a current ramp through the yoke to deflect the electron beam from top to bottom on the CRT. Figure 5-4 shows a typical output waveform from the T-Chip and other waveforms associated with the vertical circuitry. The vertical output IC, U14501, is an inverting amplifier that sinks current at pin 5 when pin 1 is high and sources current from pin 5 when pin 1 is low. U14501 is supplied by the 26 volt run source from the main power supply.

Half-Supply

An important aspect of the vertical circuitry is the "half supply". It is connected to the low side of the yoke and remains at approximately half of the 26 volt supply. The supply is developed from a secondary winding of the IHVT and CR14703. The 26 volt supply is taken from a portion of the same winding which means the 26 volt and the 13 volt supply track each other. The purpose of the half supply is to provide a reference voltage to the vertical circuitry, around which yoke current is generated. The current through the yoke must travel in two directions. First, during the active portion of scan, current flows in such a direction to cause the beam to travel down the face of the CRT. During retrace, the yoke must stop the downward travel of the beam and return it to the top of the screen by reversing the yoke current. The beam travels down the screen in 1/60th of second, but has to return to the top in much less time. The vertical circuitry uses some tricks to accomplish the task.

R14508 and R14509 limit the current in the yoke to keep the beam from deflecting off the screen in the event U14501 might short to ground or to the 26 volt source. C14502 acts as a filter and with R14518 helps reduce the vertical rate ripple current on the “half supply.” R14519, whose value is less than one ohm, and R14502, (which is in parallel to provide finer adjustment), form a current sense resistor that develops a voltage drop directly proportional to yoke current. The half supply is input to pin 5 of RN4501 and through R14519 to pin 4 of RN4501. The bias voltage at RN4501 pin 5 goes out pin 6 to the vertical IC noninverted input at U14501 pin 7. The bias voltage at RN4501 pin 4 goes out pin 3 to the inverted input of the vertical IC, U14501 pin 1. The helps to cancel any modulation of the half supply resulting from vertical rate current on C14502. The quality of the canceling effect is determined by the match of the resistors in RN4501. These are normally matched to within 0.5 percent.

Pin 15 of U16201 provides a 2 volt p-p vertical sawtooth to pins 1 and 2 of RN4501. The average DC level of the ramp is approximately half the T-Chip vertical supply voltage (7.6V) supplied to pin 26 (approximately 3.81 Vdc). The ramp can be adjusted +/- 150mV via the Vertical DC Centering adjustment over the I^2C data bus using either the front panel service menu or Chipper Check. The vertical ramp and the error signal superimposed on the half supply from the current sense resistors, R14519 and R14502, are added together by the resistor network, RN4501, and input to the inverting input pin 1 of U14501. The 7.6 volt supply is input to pin 7 of RN4501 where it is divided down to half Vcc. It is then added to the error signal riding on the half supply from the current sense resistors, output from pin 6 of RN4501 and applied to the non-inverting input pin 7 of U14501. The average DC voltage on pin 7 is approximately 9 volts during normal operation.

Following full trace, the input of U14501 at pin 1 is increasing, which causes the output at pin 5 to decrease. As this input decreases, the output increases. When the vertical ramp is at the bottom of the slope, pin 5 of U14501 sources current from the 13 volt half supply through the yoke to the 26 volt supply, deflecting the electron beam to the top of the screen. As trace begins, the ramp voltage on pin 1 climbs and the current source from pin 5 proportionally decreases, lowering the voltage across the yoke, allowing the beam to lower towards the center of the screen. When the voltage on pin 1 of U14501 reaches the same voltage as pin 7, pin 5 is at approximately half the 26 volt supply. Because the low side of the yoke is tied to the half supply, at this time there is no current through the yoke. Without deflection current, the electron beam will be at the center of the screen.

As the voltage on pin 1 of U14501 rises higher than pin 7, pin 5 begins to sink current. This causes the current to flow from the half supply, through the yoke to pin 5. Because the current flow reverses, the beam is deflected towards the bottom of the screen.

During retrace, the ramp resets causing the output of U14501 at pin 5 to go high, deflecting the beam back up to the top of the screen. The extra current required to deflect the beam from the bottom to the top of the screen is produced by C14505. During scan time, the negative lead of C14505 is grounded through pin 3 of U14501 The positive lead is charged to +26 volts. At retrace, the flyback generator switch inside U14501 connects pin 3 to pin 2 applying +26 volts to the negative side of C14505. The charge stored on C14505 plus the 26 volts on the negative terminal produce 52 volts on pin 6. The increased supply voltage quickly retraces the beam to the top of the screen.

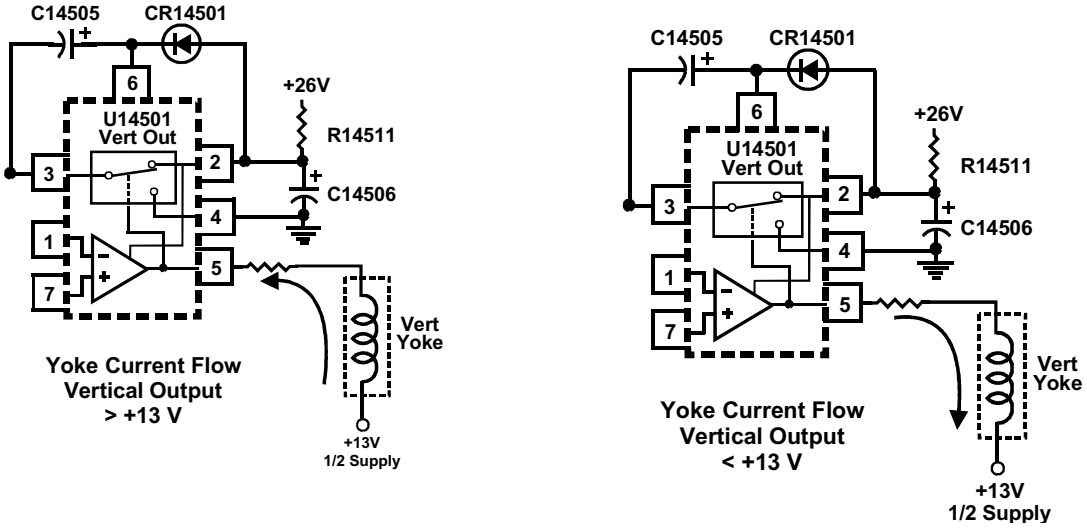


Figure 5-2, Vertical Output Current Flow

Vertical size compensation with varying beam current is achieved via pin 28 of U16201. The vertical output ramp at U16201 pin 15 will change about 1 percent per volt change at pin 28. Pin 28 is nominally 6.1-7.3 volts during normal operation. As beam current increases toward the beam limiter threshold, a point is reached when the beam sense line will begin pulling down the voltage reference at pin 28. This causes a drop in the vertical reference ramp at U16201 pin 15 reducing vertical scan slightly. This prevents the picture from blooming vertically during high beam current scenes.

U16201 pin 16 is the vertical ramp ALC (automatic level control) that maintains the vertical ramp at a constant level, even if the vertical interval changes, as with a nonstandard signal. C14501 and C14503 set the time constant of this amplitude regulating servo circuit. If the total capacitance were too small, vertical linearity would be affected. In extreme cases, field-to-field vertical jitter might be seen.

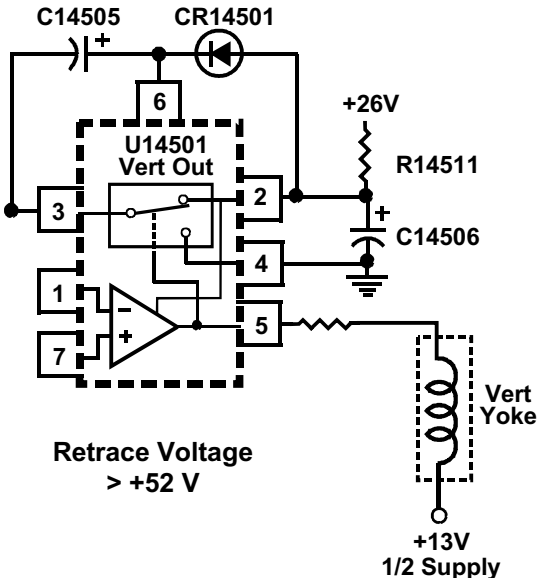


Figure 5-3, Vertical Output

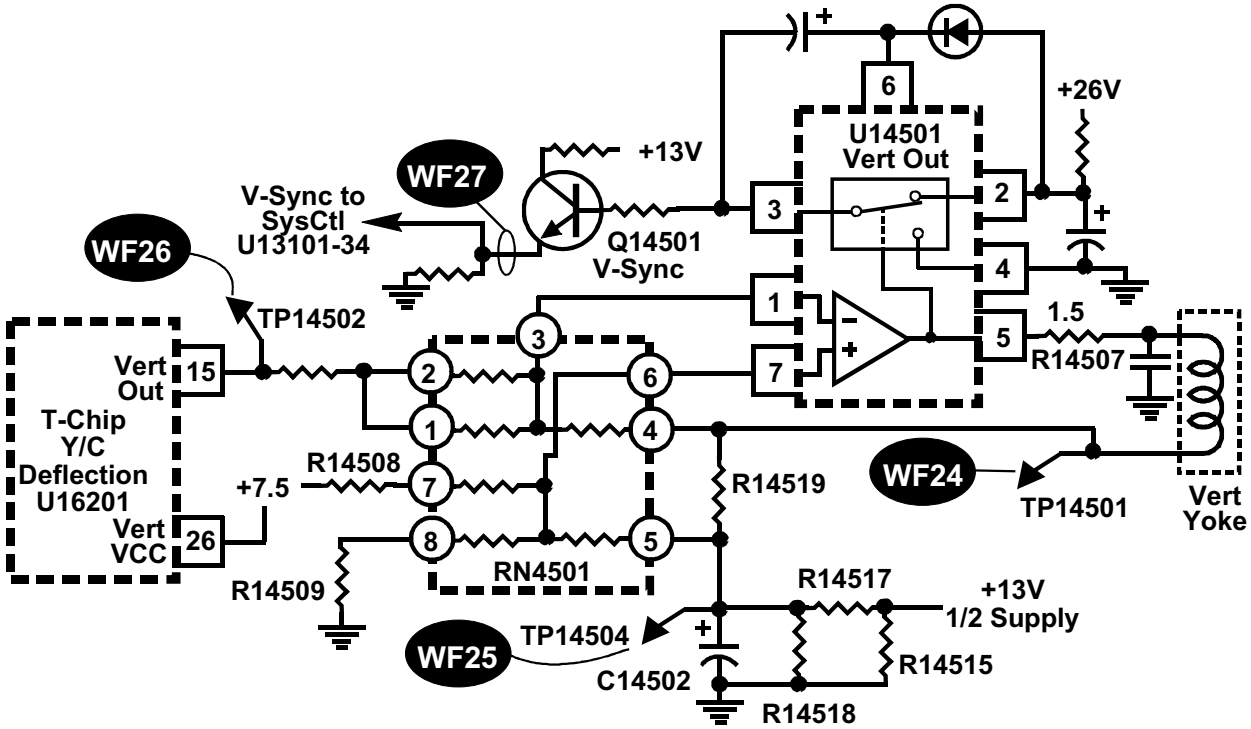


Figure 5-1, (Repeated), Vertical Deflection Circuit

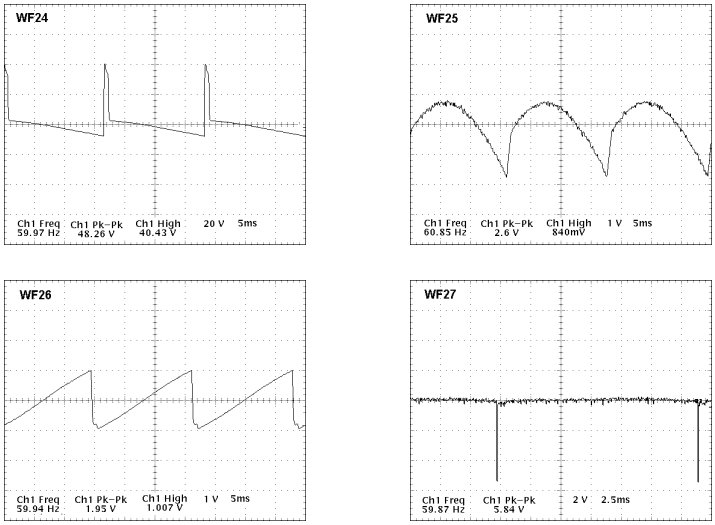


Figure 5-4, Vertical Circuit Waveforms

Troubleshooting

The vertical circuit is direct DC coupled and does not rely on capacitors for S-shaping and feedback. As a result, vertical troubleshooting can be accomplished with a digital volt meter and an oscilloscope.

Warning: Do not try to check the DC operation of U14501 by grounding pin 1 or applying 26 volts. Damage to U14501 or any of the direct coupled stages may result.

No Vertical Deflection

1. Check for the presence of the 26 volt supply on pin 6 of U14501. If it is not present, suspect R14511 being open, possibly as the result of a shorted U14501. If it is correct, go to the next step.
2. Check for the half supply of approximately 13 volts at TP14501 (vertical yoke connector). If it is not there, check for an open R14519 or R14517. If it is there, go to the next step.
3. Check for a 2 Vp-p vertical parabola on pin 1 of U14501. If it is not there, check pin 15 of U16201 for a 2 Vp-p vertical ramp signal. If the ramp signal is present, suspect a defective U14501. If it is not present, go to the next step.
4. Check for 7.62 volts on pin 26 of U16201. If it is not there, troubleshoot the main power supply. If the voltage is correct, check pin 16 of U16201 for approximately 3.5 volts. If the voltage is wrong suspect a defective C14501, C14503 or U16201.

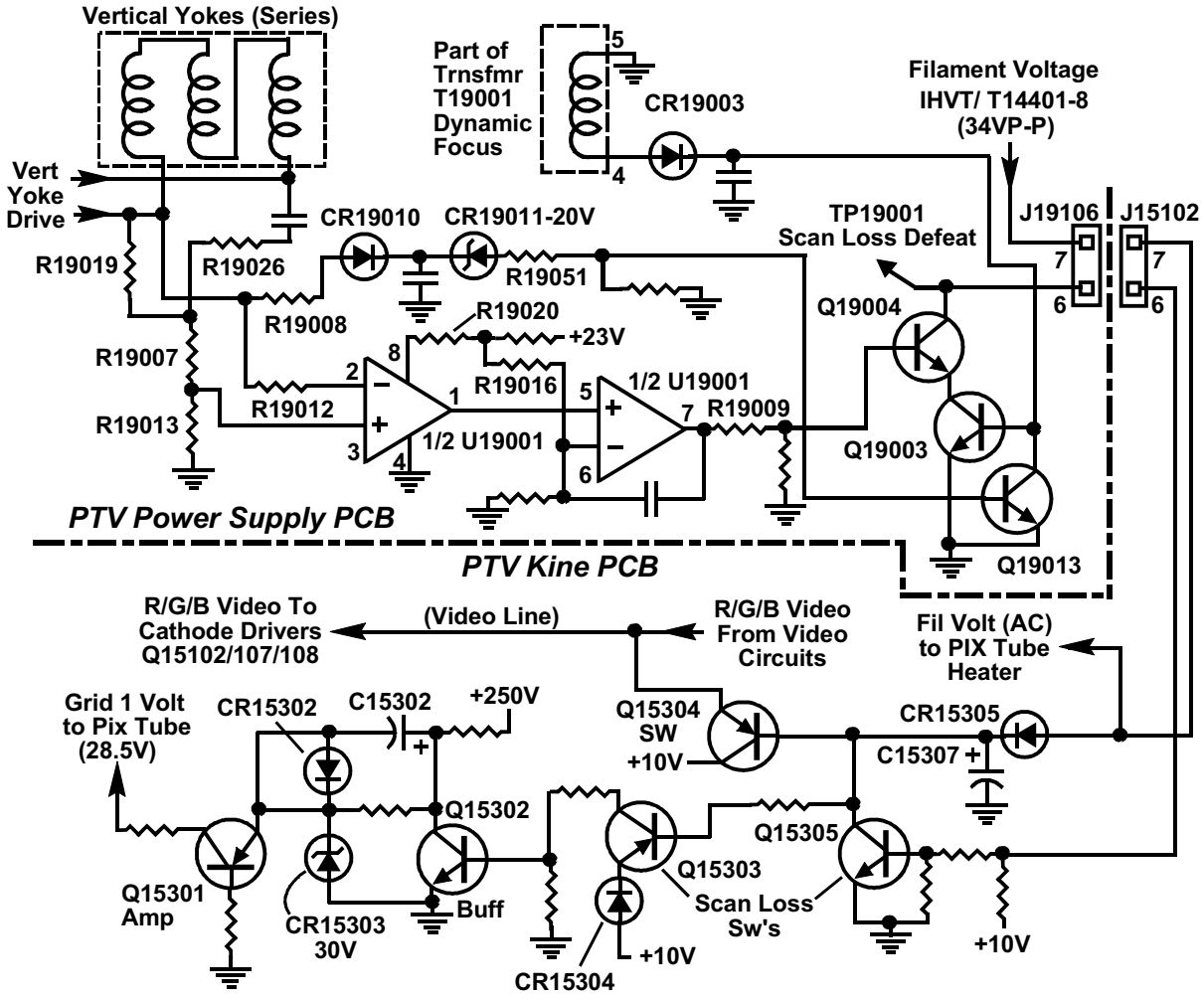


Figure 5-4, Scan Loss Detect & Shutdown Circuit

Scan Loss Detect & Shutdown Overview

The primary function of the Scan Loss Detect and Shutdown circuit is to detect loss of scan. This is needed in order to protect the picture tubes and also to protect the convergence yoke driver circuits in the event of a catastrophic failure in the deflection circuits. This is accomplished almost instantaneously by the circuits shown in Fig. 5-4 above. Both the horizontal and vertical are monitored for "unscheduled" shutdowns failure. Horizontal is monitored by using the filament heater voltage as an indicator. Vertical is monitored by comparing the voltage across the vertical yoke to a reference voltage. If and when a failure occurs two things happen, one: the video drive signals to the picture tubes are muted and two: the Grid 1 voltage to the tubes are turned off.

Scan Loss Detect Operation

The scan loss circuit in CTC195 instantly detects the loss of current in the vertical deflection yokes and blanks the video. This is necessary to prevent damage to the phosphor on the picture tube by the extreme energy of an undeflected electron beam. The circuit in Figure 5-4 directly monitors the vertical yoke current and provides various methods of removing the vertical yoke drive.

In previous PTV chassis the horizontal scan loss was measured indirectly. It was measured by detecting the picture tube filament pulse. The filament pulse is obtained from a separate winding on the flyback transformer that is coupled to the winding that drives the horizontal yoke. Using this method there is a possibility that vertical yoke scan current could be lost and its loss may not be detected quickly enough to prevent damage.

The CTC195 detects horizontal yoke current by means of the dynamic focus transformer T19001. The dynamic focus transformer is a current transformer with the horizontal yoke current flowing in the primary (not shown). A small secondary winding (pins 4-5) generates a voltage signal whenever the horizontal yoke current is present. This signal is peak detected by CR19003 and filtered to provide drive for transistor switch Q19003. Q19003 forms a logical AND with vertical scan loss detection transistor (Q19004). With these two transistors on, ground is appled to the base of Q15305 keeping it off

The three vertical deflection yokes are wired in series. Two inputs provide the connection back to the chassis. One side is connected to the vertical amplifier output. The other side connects to ground through a current sensing resistor (R19019). If vertical scan is lost, the scan loss comparator circuit (U19001-7) outputs a Lo to the base of Q19004, allowing it to turn off. When Q19004 turns off the ground is removed from the base of Q15305 and the pull-up B+ turns it on. This in turn causes the video and Grid 1 voltage to be shutdown.

Vertical scan loss occurs when one or more vertical deflection yokes are unplugged or an open occurs due to the breaking of the series connection. When the open occurs, it is important that the video is blanked quickly. Ideally blanking would occur instantly when the next vertical scan is missed. In the circuit the differential amplifier (U19001-1,2,3) amplifies the voltage across the vertical sense resistor (R19019). The negative half of the output signal is clipped because the negative power pin of the opamp is grounded and the amplifier output can not go below ground. The output of amplifier (U19001-1,2,3) is a 2 volt peak sawtooth shaped pulse repeated at a 60 Hz rate. This pulse is applied to the non-inverting input of integrating amplifier (U19001-5,6,7). The inverting input of amplifier (U19001-5,6,7) is biased at approximately 1 volt. When ever the non-inverting input exceeds 1 volt, once per vertical cycle, pin 7 integrates positive (outputs a Hi). The integrating time constant is chosen to keep the worst case minimum ripple voltage on pin 7 slightly above 1.2 volts when the integrator is pulsed at a 60Hz rate. Whenever pin 7 of U19001 is above approximately 1.2 volts, transistor Q19004 is turned on and if the horizontal detector Q19003 is also on, video and Grid 1 voltage are enabled.

If vertical yoke current stops, there is no pulse signal to refresh the integrator and pin 7 quickly falls below 1.2 volts and turns the video off. A feature of this circuit is that it uses no electrolytic capacitors. Electrolytic capacitors deteriorate in value with heat and time. They are suitable for power filtering but not for critical timing applications.

Previous projection TV's detected vertical scan by measuring the AC voltage on the "S" capacitor located on the main chassis. This is adequate to detect an open of both inputs but fails to detect a problem with only the "S" cap and/or ground end of the yoke string (J19101-3). This type of failure could occur because of a fault with the "S" Cap and/or the ground path opens up in the feedback loop of the vertical amplifier and the vertical output at the top of the series yoke string. If this type of failure occurs a 60Hz 26V p-p square wave is passed through the yokes to the AC scan loss detector and is interpreted incorrectly as a valid vertical scan signal. A similar failure can occur but for a different reason. Previously, only a current sense resistor (R19019) and a differential amplifier (U19001-1,2,3) to produce a voltage that is proportional to the vertical yoke current. If the feedback portion of the circuit opens, a 26 volt square wave appears at the input of the op-amp (U19001-2). Ideally, the signal should be rejected by the amplifier, however this doesn't happen because of the high impedance input characteristics, the amplifier can't reject such a large signal.

The solution to this problem is to use a peak detector consisting of CR19010 and zener diode CR19011. This circuit detects the loss of the "proper vertical feedback" signal. During normal operation the voltage on the "S" cap (ground side…J19101-3) has a 3VAC (60Hz) riding on 13VDC. The feedback loss detector has a 20 volt zener diode (CR19011) between its peak detector CR19010 and its output transistor Q19013. In normal operation the output transistor Q19013 is off. When the feedback loss detector sees the 26V p-p square wave signal which in turn is rectified and filtered to provide approximately 26VDC. This is enough to cause the zener CR19011 to conduct so that transistor Q19013 is turned on. The output transistor Q19013 turns On and transistor Q19003 turns Off. This allows Q15305 to turn on shutting down video the Grid 1 voltage.

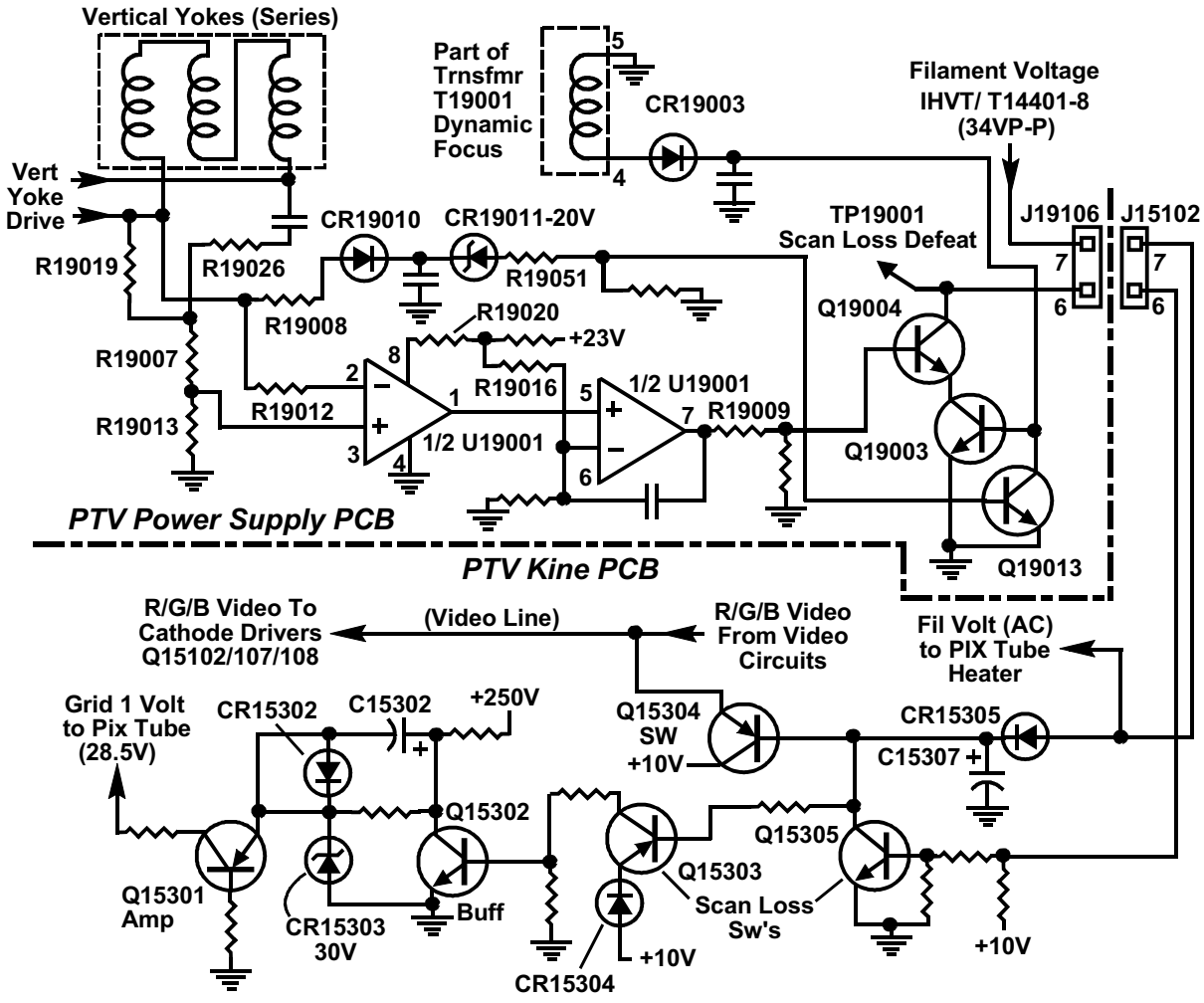


Figure 5-4 (Repeated), Scan Loss Detect & Shutdown Circuit

System Control

Overview

The CTC195/197 chassis is a digitally controlled television receiver. The system control circuit governs the entire operation of the television. The control circuits are not only responsible for turning the set on and off, but also for aligning the different circuits such as deflection and signal. Adjustments that were aligned with a potentiometer on other chassis are now aligned digitally via the microprocessor with the values stored in the EEPROM (**E**lectrically **E**rasable **P**rogrammable **R**ead **O**nly **M**emory). This means the values stored may be changed by invoking the correct parameters for the EEPROM to allow writing to it, then writing the new values. The EEPROM will hold all values written to it even during and after loss of power. The EEPROM also stores certain user settings. This ensures that these settings will not be lost during long power outages.

The CTC197 Control System is based on a single 8-bit ST9296 Microcomputer. The micro has several new features over others used in the past. The new features include an IR Preprocessor, Sync Presence Detector, Frequency Multiplier for the CPU Clock, a UART, a Closed Captioning Decoder that can run without H and V from Deflection (needed for TV Guide Plus+), 3 A/D inputs and an On-Screen-Display that supports 3-bit D/A outputs (also needed for TV Guide Plus+).

The three I²C busses communicate with the majority of the digital devices. The three busses are called the Standby, Run and GemStar (TV Guide Plus+) bus. The standby bus is connected to the main EEPROM and the decoder interface microcomputer, when present. The run bus is connected to the remainder of the I²C devices. The TV Guide Plus+ bus will be connected to the TV Guide Plus+ module only. The Standby and Run busses run at approximately 50 KHz while the TV Guide Plus+ bus runs at about 100 KHz and will use clock stretching. The TV Guide Plus+ bus runs faster than the main bus because full screens of display data are sent over the bus from the module to the main chassis microprocessor. The standby bus is always active, while the run bus is only active after power up. The TV Guide Plus+ bus can be activated via software control without powering up the remainder of the chassis. This is to allow updates to the TV Guide Plus+ material at any time via downloads from the source station.

The CTC195 chassis uses the same main chassis as the CTC197. However, additional circuitry for PTV (***P***rojection ***T***ele***V***ision) operations are added. These include; digital convergence, higher power audio amplifiers, an additional power supply and various CRT control circuitry. I²C bus control is provided for all circuitry.

The CTC197 main chassis devices that are controlled by the I²C bus are the main EEPROM (U13102), Main Tuner PLL (U17501), Stereo Decoder (U11600), T4 Chip (U16201), Audio Compressor (11501) and the Video Switch (U26901). Other devices include the PIP EEPROM (U27903), PIP DAC (U27902), PIP PLL (U17401), and FPIP (U18100). The optional TV Guide Plus+ module is also controlled via a dedicated I²C bus. The CTC195 chassis has a Digital Convergence/Convergence Power Supply board, and an Audio Board with I²C bus controlled devices. The Digital Convergence microcontroller (U19501) and EEPROM are on a dedicated I²C bus.

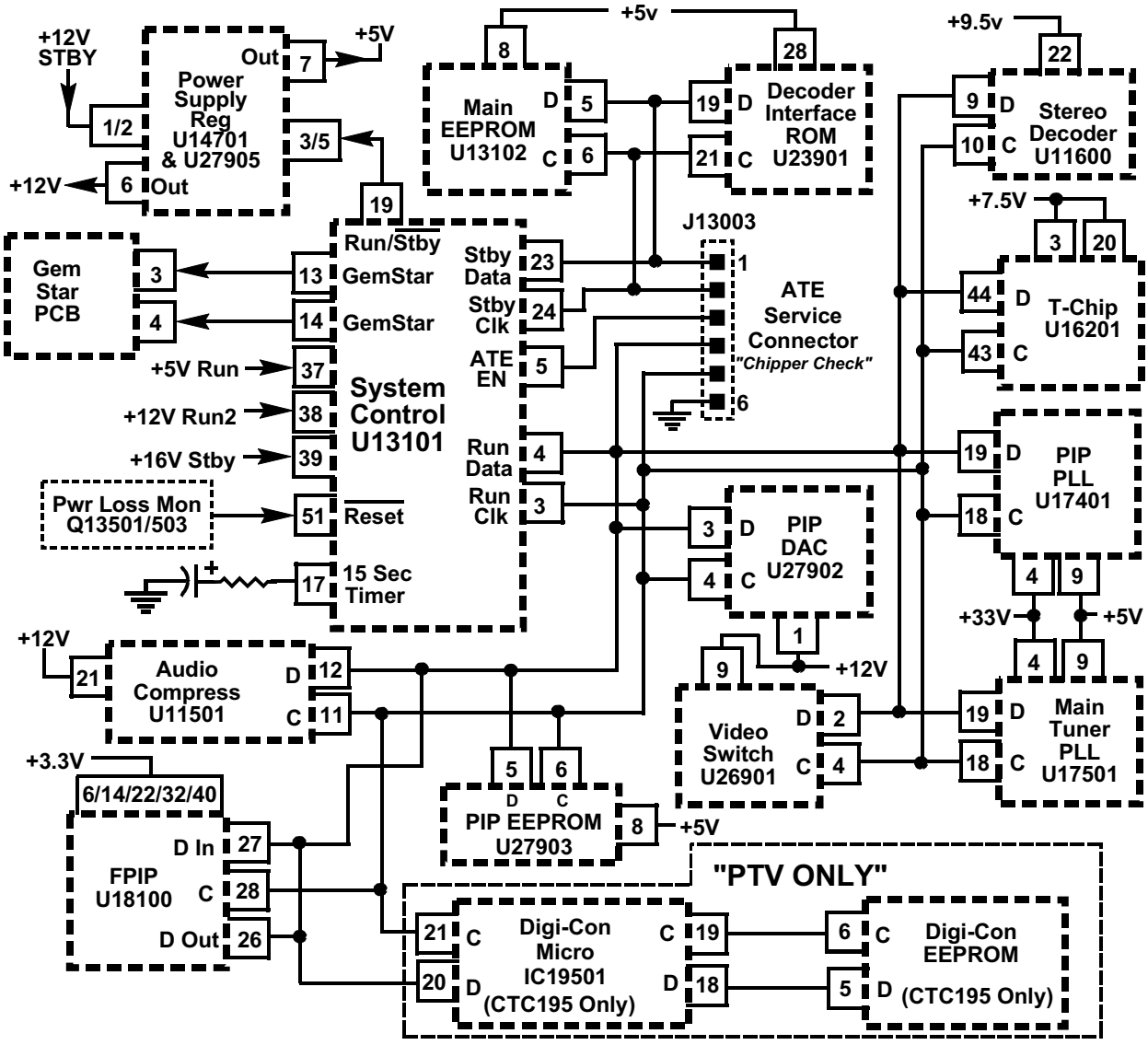


Figure 6-1, System Control Block Diagram

Standby/AC Line Dropout Detector and Reset

The reset circuitry of the microprocessor monitors the standby +5 and +16 volt supplies and warns the micro when a power failure may be occurring. Standby, when used in this application, means that the supply is always on as long as the AC cord is plugged in. These supplies are available at all times. This contrasts with the Run supplies, which can only supply power when turned on by the micro. Pin 51 of U3101, the main microprocessor, is normally held hi by the presence of the +5 Volt standby power supply voltage. A simple voltage divider network consisting of R13504, R13505, R13507 and R13510 keeps pin 51 high as long as there is +5 volts coming from the standby supply. Q13503 is normally biased off when the standby +16V supply is present. When the standby +16V supply drops to about +7.5V, Q13501 turns on which turns on Q13503 applying a LO to pin 51 of U13101. When this occurs, the microprocessor disconnects the busses internally and proceeds to go into a backup routine.

Reset, Recovery, Initialization and BrownOut

The reset circuitry of the control microcomputer monitors the +16V Standby Supply and resets the microcomputer when the supply drops below roughly 6 volts, making reliable operation of the microcomputer impossible. With the micro in reset, all the local controls and the IR inputs are disabled. The RUN/STBY line will be switched to low removing power to the T4 Chip and all Run regulators.

Software detection

The +16V standby supply is monitored by the microcomputer using an A/D to determine if a reset condition is imminent, or brownout conditions are present. As the +16V supply begins to drop, at approximately 12 volts, the micro will turn off the run supplies and activate the “batten-down-the hatches” routine to save off chassis operational conditions such as;

1) Current time
2) Current channel
3) On/Off state
4) Input source (Aux/SVideo)
5) Volume Setting

+16V Standby

The +16V Standby supply input is sampled directly by the micro on pin 39 via a 6-bit A/D. This is used to verify that the supply is active and within regulation. Failure to meet the level specification will result in a power cycle of the entire instrument using the “batten down the hatches” routine which will save off the appropriate error code in the EEPROM. In addition, this input is monitored to control the reset of the main micro and provide a sense level for the TV Guide Plus+ module low power monitor. The +16V power supply is designed not to allow a sag of <12 volts to occur. Any drop to less than 12 volts will cause the micro to run through “batten down the hatches”.

15 Second Timer

Once a shutdown condition occurs, a 15 second timer begins its countdown. This circuit is shown in Figure 6-2 and are the components connected to pin 17. It assures that the time-of-day is maintained until the timer input on pin 17 of the micro fails to maintain a logic 1 condition. As indicated by the pin title, this normally happens about 15 seconds after a power failure. This enables the chassis to maintain the time-of-day through minor power outages or brownouts that may dip below the minimum AC supply tolerance for less than 15 seconds.

POR (Power Off Reset)

Circuitry in the T4 chip detects when the standby-power voltage has dropped too low and shuts off deflection, effectively shutting down the set. The output of the POR-detector is latched and may be read as a status bit over the serial bus by the microcomputer. This POR latch is reset on the OFF-to-ON transition of the ON/OFF control bit in the T-Chip. Therefore, if the detector is latched when the TV is ON, it is necessary to send an OFF command followed by an ON command in order to again start the instrument. If the standby voltage is still too low when the ON command is received, the IC will stay in the OFF mode, and the process must be repeated.

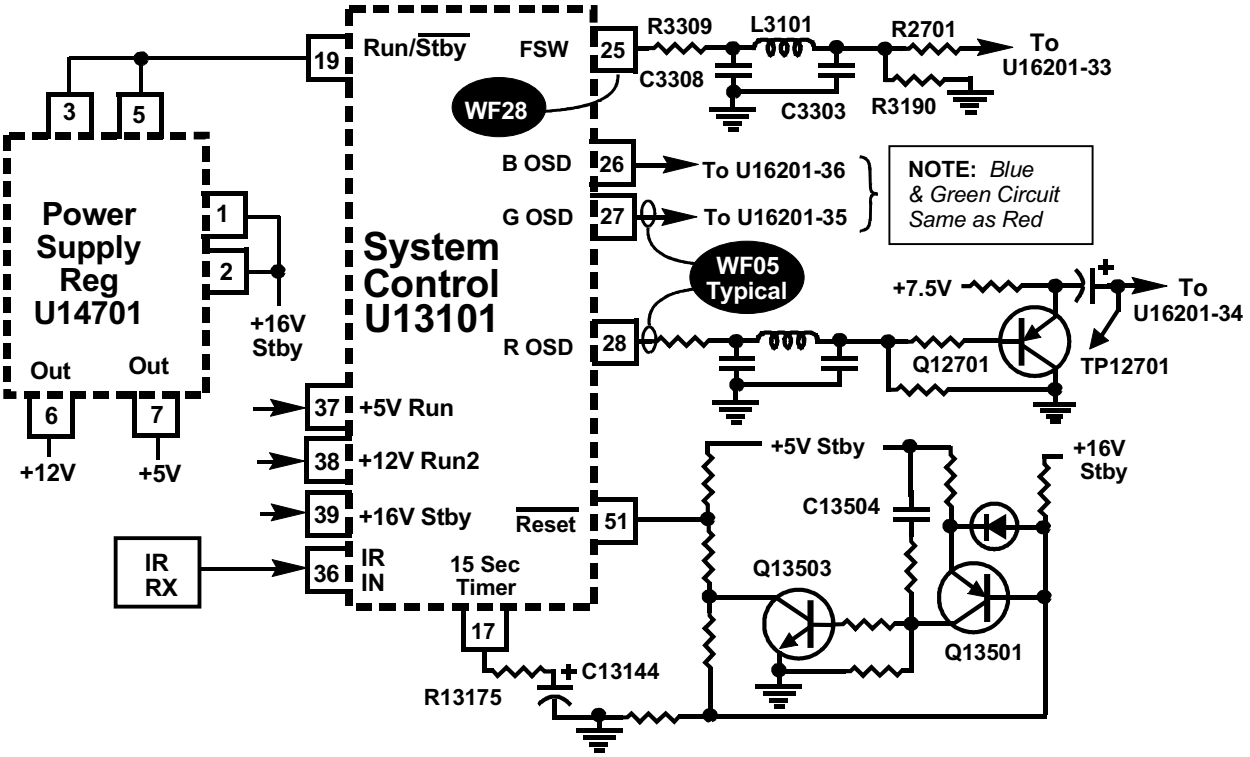
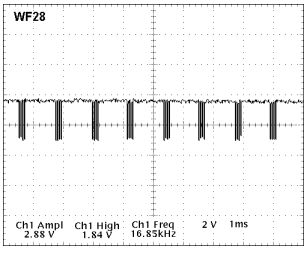
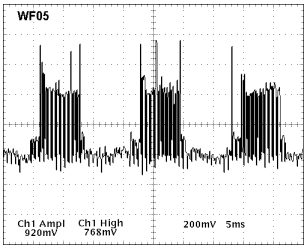


Figure 6-2, System Control Reset





User Settings

During shutdown, all current user settings will be stored in EEPROM. Most settings now are written to the EEPROM as they are changed, with no shadowing of the EEPROM in RAM. It is no longer necessary to guarantee RAM retention with this system configuration. The microprocessor has approximately 10ms to allow any writes to the EEPROM in order to store the present condition of the TV.

EEPROM and T4 Chip Power Control

The microprocessor controls the power to the EEPROM (U13102) and T4-Chip (U16201). After the microprocessor is reset, U13101 pin 20 goes LO turning on Q13109. This supplies +5V to the EEPROM (U13102). The T4 Chip uses a +7.5 volt supply derived from the +12 Volt Run supply. A simple voltage divider reduces the 12 volt to 7.5 volts. Although the 7.5 volt supply is labeled "Standby"

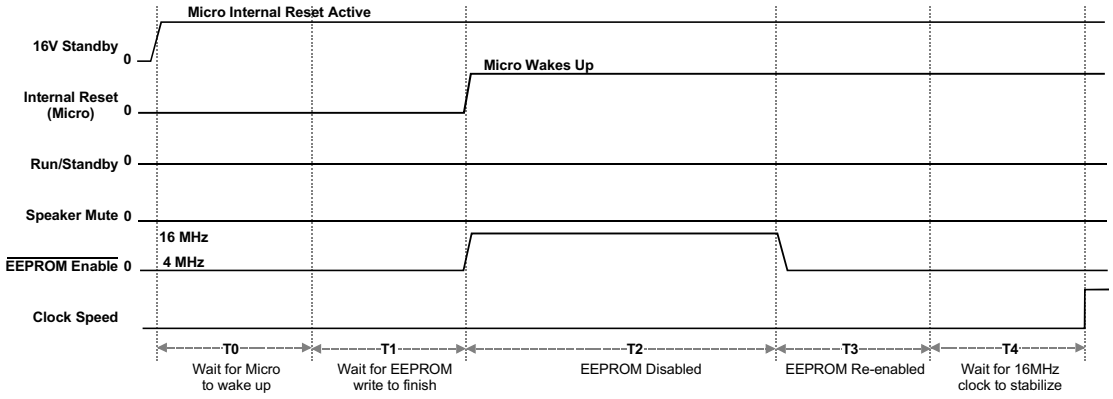


Figure 6-3, Micro Reset Sequence

in the service literature, it is actually not active at all times. +7.6V to the T4 Chip is available only when the run +12V supply comes up. The power control circuitry of the microprocessor gives it the ability to turn off the power to the EEPROM and T4 Chip in the event one of the devices locks up. Because the micro goes through a power up sequence every time the instrument is turned on, the T4 Chip and EEPROM are turned off and then back on each time the TV is turned on. This resets the EEPROM and T4 Chip each time the TV is powered up.

Main Power Supply On/Off Control

The CTC195/197 chassis are turned on and off by controlling the main power supply *and* the T4-Chip. When the power cord is first connected to AC, standby supplies come up, Q13503 resets the micro by sending a HI to pin 51. Pin 20 then goes HI applying power to the EEPROM. The microprocessor then checks the EEPROM address for an acknowledgment. If the EEPROM is acknowledged, the microprocessor waits for the next command. If there is no EEPROM acknowledgment, the microprocessor continues to try to contact the EEPROM. This can be seen on the oscilloscope as continuous data activity on the I2C data line.

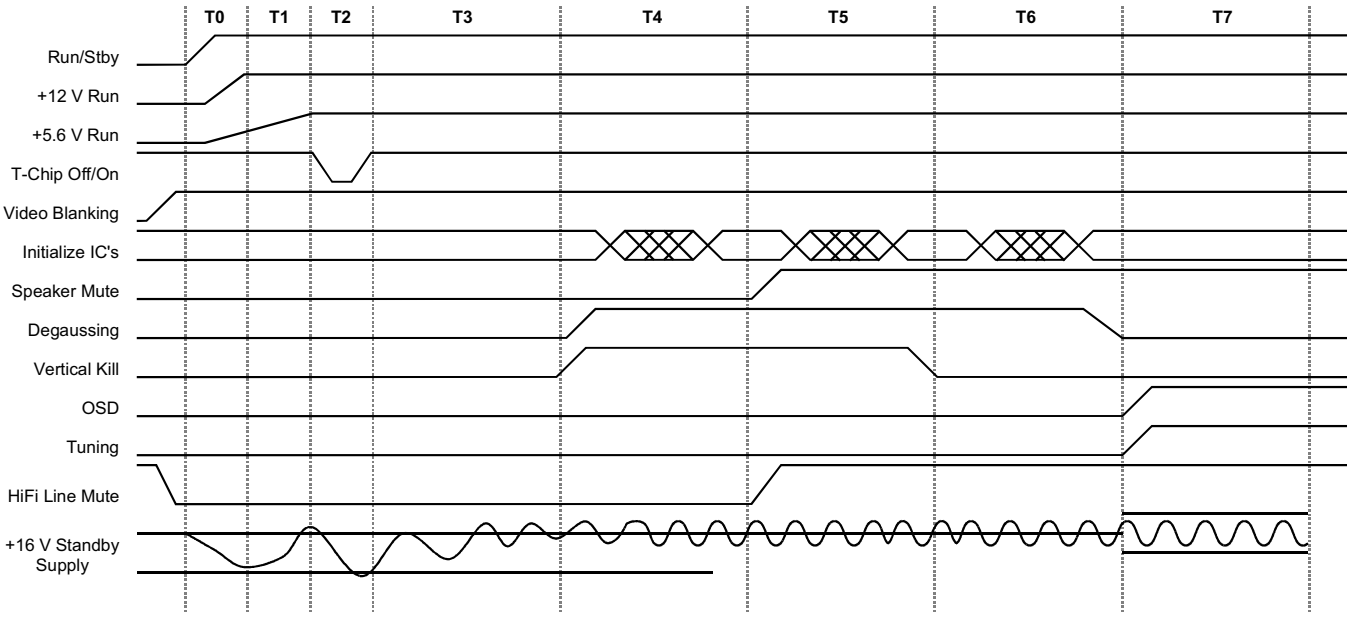


Figure 6-4, Micro Power Up Sequence

The timing diagram in Figure 6-4, while not being a good troubleshooting tool, can be a useful learning tool if understood by the technician. Refer to it during the next section.

With AC power already applied to the set, when the power button is pressed or a remote control ON command is received, pin 20 goes momentarily LO resetting the EEPROM. This makes certain it is a normal state. Immediately the +16 Volt Standby Supply dips. This can be seen at the bottom of the chart during time periods T0-T2. During this time, the video and audio mute lines are low so that no picture or sound can be processed accidently by circuitry having some residual voltage supply remaining. During time T0 the Run/Standby signal at pin 19 goes HI activating the +12 and +5.1 volt run supplies. These supplies ramp up during the remainder of T0 and T1. When the +12 volt supply reaches about 90%, the micro assumes that the +7.5 volt supply derived from it is stable enough to activate the T4 Chip which begins starting the deflection circuits. After this, there is a short amount of time for the Run supplies to completely stabilize before the I²C devices are initialized. This is also the time when auto-detect is looking for features on the instrument and continues through time T4-T6. When IC initialization begins, the micro also stops vertical deflection and degausses the CRT.

Note that the Hi-Fi and Line outputs are muted normally and held in a non-muted state. This is so that any power supply drop out will cause the line outputs to mute, reducing the risk to high-power amplifiers that may be connected to them.

By the end of T6, circuit stability has been established. The OSD and tuner are allowed to function. As soon as a channel is captured, the video blanking is turned off allowing video to pass normally. When the high voltage supplies have reached their normal operating voltages, a picture will appear on the CRT.

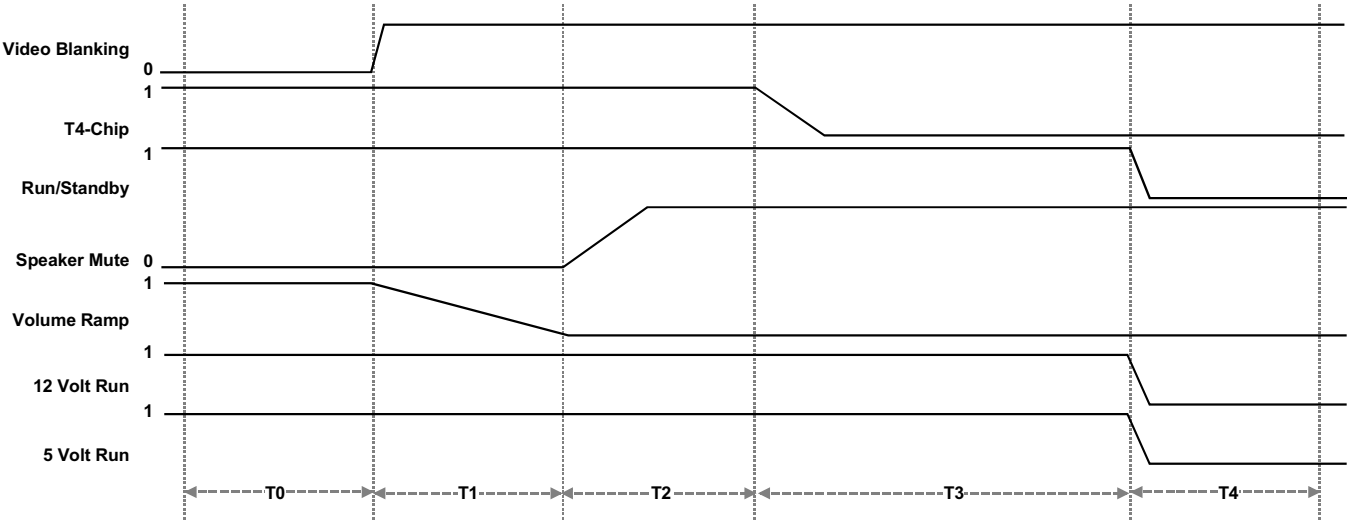


Figure 6-5, Micro Power Down Sequence

Power Down

Figure 6-5 shows the normal power down sequence for the CTC195/197 chassis. Again, this will not greatly aid in troubleshooting, but only in the technicians understanding of what is happening during a normal power off event. It is always advantageous to understand what is happening, before being able to pinpoint what is not happening.

The exact time frame involved is unimportant, only the sequence. When either the power button is pressed or a remote control OFF command is received, the micro immediately mutes the video. The volume level is reduced, then the speakers are muted and the T4 chip is ordered to stop deflection. This all happens between T0 and shortly into T2. During the remainder of T2 and T3, high voltage and deflection are shutting down. At the beginning of T4 Run/Standby (pin 19 of U3101) is turned to Standby, shutting down the 5 and 12 volt run supplies, shutting down the instrument.

Batten Down the Hatches

The batten down sequence is one of the most important for the technician to understand. This is invoked during any problem sensed by the microprocessor and acts to save off all settings and alignments, plus an error code to cue the technician as to the possible cause of the failure. It's most important function is to shut down the set as normally as possible during loss of incoming AC, whether long term or short term.

The batten down sequence will occur when the standby 16 volt supply drops to about +9.5 volts during a power up cycle, or to about 2 volts below the reading of the standby D/A on pin 39 of the microprocessor, U3101 1.5 seconds after power up or 1.5 seconds after power down.

Some power supply dip or surge is expected during start up and shut down, so 1.5 seconds was chosen to make certain any ringing or dipping of the supply had stabilized before taking a reading that might lead to a batten down sequence, when the only thing occurring was a normal power supply dip or surge during start-up or shut down.

Figure 6-6 shows the timing during a typical batten down sequence. The "Power Fatal" trigger is the +16 volt standby supply monitor on pin 39 of the microprocessor, U3101. Anytime after the 1.5 second power on cycle, if the 16 volt standby supply falls below approximately 9.5 volts the batten down sequence begins. The first actions are to jettison all devices the drain the residual power supply. The speaker outputs, run supplies, OSD display, Star Sight and any other circuit not necessary to saving information to the EEPROM are cut loose. All instrument information is written to the EEPROM during the next 10 milliseconds. After that, the EEPROM is disabled by pin 20 of the micro going HI. When this sequence is completed, two things may happen depending upon the condition of the standby supply. The 15 second timer on pin 17 tells the micro how long the power has been disconnected. If it has been less than 15 seconds, the set is powered up with no loss of data, including the clock time. If it has been greater than 15 seconds, the clock time is lost. When the EEPROM has stabilized after T4, one more write containing device status after the batten down the hatches routine started is written.

The microprocessor continuously monitors the +5 and +12 volt run supplies and can write an error code when it detects the failure of either. This might not be extremely valuable considering the set will not run without both supplies working. However, if either supply drops out longer than 500 milliseconds, an error code will be logged. See the error code list for the code explanations.

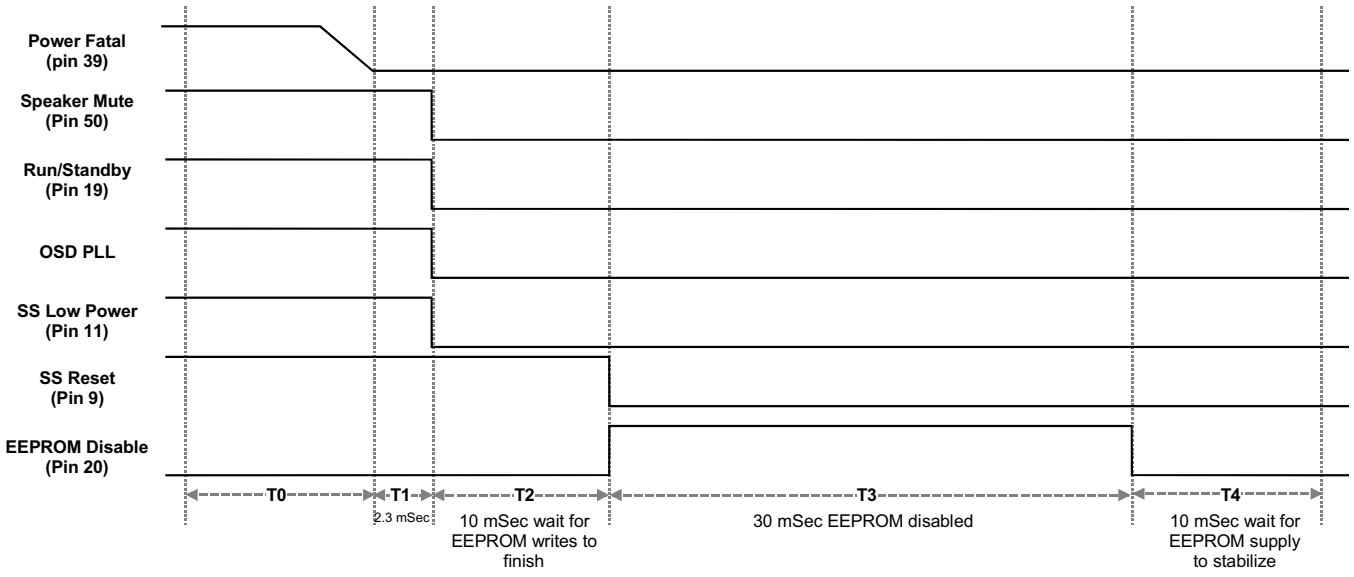


Figure 6-6, Micro Batten Down the Hatches Sequence

Feature Auto Detection

As with the CTC179/189, certain features of the CTC195/197 chassis family are auto detected. The microprocessor checks for the appropriate hardware and if detected, supports that feature. If not, it assumes that feature is not supported in the chassis and runs without it. In these instances, the set will not shutdown, but will run minus the feature. One example is the digital convergence board for the CTC195 projection sets. If the convergence board is disconnected or malfunctioning, the micro will not receive an acknowledgment and revert to a direct TV mode. Currently auto-detected features include; TV Guide Plus+, MCR (Commercial Chassis), Digital Convergence on PTV's, and 2 Tuner PIP.

Run Supply Detector

As previously discussed, the system control circuitry monitors the +5 and +12V run supply directly from inputs to pins 37 and 38, once the set has been turned on. If for any reason the run supply is not present when the set is initially turned on, the microprocessor will abort the power on sequence and then try to restart the set. If after three tries the run supply is not detected, the microprocessor places the TV in the off mode. This is known as the "three strikes and your out" sequence. Pressing the power button will restart the detection process. Remember there are only three error code locations and that every start attempt will fill one of the locations. If the set is restarted, the new error codes will overwrite the ones recorded during the previous power up attempt.

The +16 volt supply is also directly monitored by pin 39 of the microprocessor. After the 1.5 second delay at start up for the supply sag to recover, system control begins to monitor the supply. If at any time the normal operating voltage drops farther than 2 volts, the micro will enter the batten down sequence.

A loss of horizontal deflection may cause the run supply detector to trip. Without the load of the horizontal deflection circuitry, the 140 volt B+ starts to climb. The power supply error amplifier, which monitors the +140 volt line for regulation, shortens the duty cycle of the power supply to reduce the B+. However, the +12 volt supply is still fully loaded and consequently may slump to less than the required voltage the microprocessor is looking for, causing the run detector to trip. This will cause the microprocessor to log a run supply error code. In some cases, the +5 volt supply may also exhibit the same problem, but the +12 volt supply would be the most likely suspect.

Microprocessor Input Signals

Certain video and deflection signals are input to U13101. Selected video out is buffered by Q13306 and applied to pin 13 for the closed caption decoder contained within U13101. Video out of the T4 Chip is buffered by Q13101 and applied to pin 38 for tuning sync (see tuning algorithms for more information). Horizontal and vertical deflection pulses are applied to U13101 pins 24 and 25 respectively to provide a synchronization reference for correct positioning of the on screen display.

Microprocessor Pin Assignments

Understanding the role of the microprocessor in the operation of the instrument will greatly assist the technician in any troubleshooting. Many of the outputs and inputs of the micro are digital, which means they are either a logic 0 or 1. They can be measured with a standard DVM as either a HI (2.5–5.0 volts) or a LO (< 2.5 volts). Activity on data and clocks can be seen as in Figures 6-7 and 6-8. On an oscilloscope very little detail can be distinguished, but the presence of activity is generally all that is needed to be known. If the clock line is flat, there is probably micro trouble. If the data line is flat, it first must be understood what communication should be taking place before assuming that no activity means a defect.

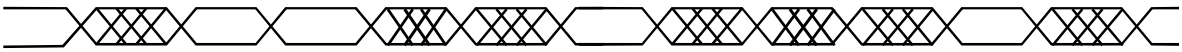


Figure 6-7, Data Line Activity

Figure 6-8, Clock Line Activity

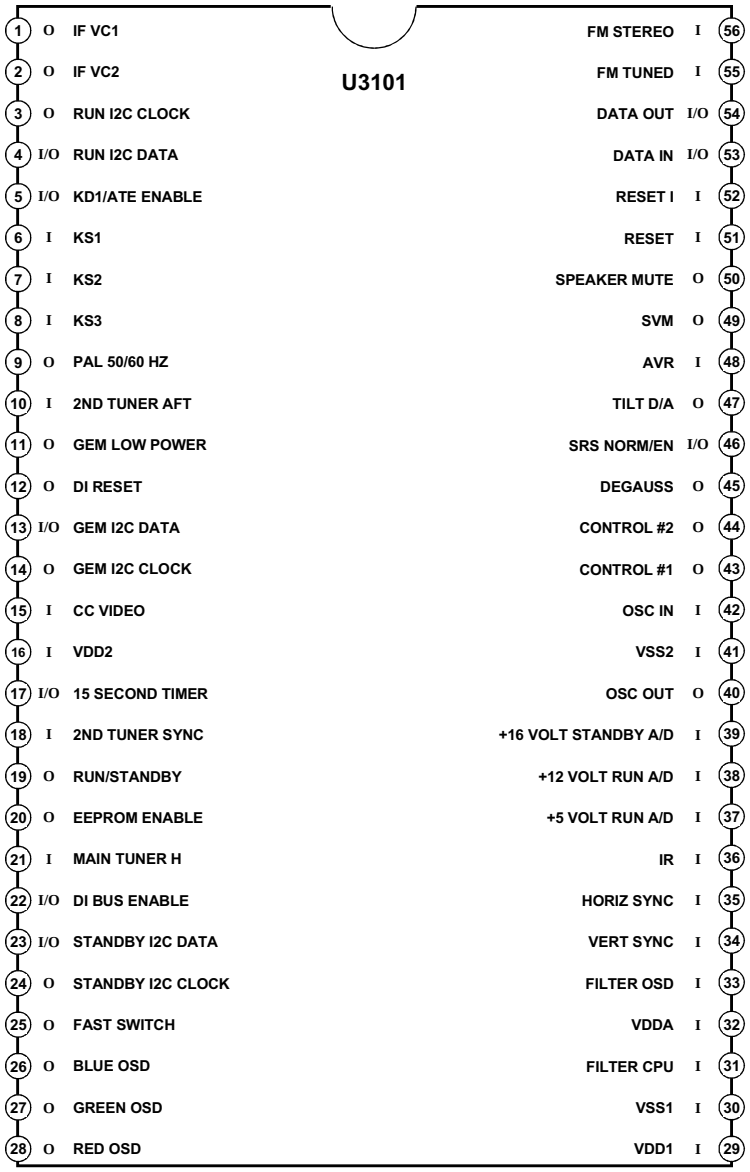


Figure 6-9, U13101 Microprocessor Pinout

U13101 Pin Functions:

The accompanying diagram describes the functions of the microprocessor, U3101. The function is outlined briefly and whether the pin is an output, input, both, or power supply or ground.

1. IF VC1: The IF VC1 output of the microcomputer is an integrated pulse width modulated digital to analog converter signal used to control the alignment of the IF output stage of the main tuner. D/A Output.

2. IF VC2: The IF VC2 output of the microcomputer is an integrated pulse width modulated digital to analog converter signal used to control the alignment of the IF output stage of the main tuner. D/A Output.

3. Run I^2C CLOCK: The Run I^2C CLK line is an output line which conforms to the Philips I^2C Bus Specification. The maximum clock rate is 100kHz. The Run I^2C CLK line is operational only when the receiver is in "Run" mode (Run mode is defined as either the TV is on, the TV Guide+ timed download is active or the Decoder Interface download is active).

4. Run I²C DATA: The Run I²C Data line is an I/O line, which conforms to the Philips I²C Bus Specification. The Run I²C CLK line is operational only when the receiver is in "Run" mode (Run mode is defined as either the TV is on, the TV Guide Plus+ timed download is active or the Decoder Interface download is active) .

5. KD1/ATE ENABLE: The KD1 line is configured as an output that switches between logic 0 and 1 levels to detect key presses from the front panel assembly. Following a Reset, the ATE_EN pin is read to determine if ATE mode has been selected. ATE mode is enabled if the input is >3.78V, normal user mode is selected if the line is <1.38V.

6. KS1: The KS1 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect front panel key presses. The lines are normally high (5V) and are pulled to ground by a key closure.

7. KS2: The KS2 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect key presses. The lines are normally high (5V) and are pulled to ground by a key closure.

8. KS3: The KS3 line is one of three lines (KS1, KS2, KS3) configured as inputs to detect key presses. The lines are normally high (5V) and are pulled to ground by a key closure.

9. PAL 50/60 HZ: The PAL_50/60HZ output line is used to control the mode of a PAL module, when installed. A logic 1 indicates 50HZ mode.

10. 2ND TUNER AFT: The 2nd Tuner AFT is an input from the 2nd tuner IF. It is the output of a comparator whose input is controlled by a bus controlled D/A IC. The 2nd tuner AFT signal is used during channel tuning to determine the presence of AFT crossover. The Channel Tuning for the 2nd tuner is controlled by the main micro.

Logic 1>3.8V, Logic 0<1.0V

11. GEM_LOW POWER: The TV Guide Plus+ Low Power Mode input is used to tell the TV Guide Plus+ micro that the +5V supply used by the TV Guide Plus+ micro will drop out within 50 msec. The TV Guide Plus+ micro will then properly power down.

12. DI RESET: The DI Bus Reset is not used.

13. GEM_I²C DATA: The GEM I²C DATA line is an I/O line, which conforms to the Philips I²C Bus Specification. The maximum clock rate is 100kHz. The GEM I²C Data line is operational as long as the receiver is plugged in.

14. GEM_I²C_CLK: The GEM I²C CLK line is an output line, which conforms to the Philips I²C Bus Specification. The maximum clock rate is 100kHz. The GEM_I²C_CLK line is operational as long as the receiver is plugged in.

15. CC Video: CC Video is an input to the control system. The line contains 1.0Vp-p (negative going sync) NTSC video. This is used to provide the Closed Caption signal to the microprocessor for decoding into usable text.

CC Video input level 1.0Vp-p +/-.2V (from 100 IRE to -40 IRE sync tip)

DC Level 2.5V nominal

16. VDD2: The microcomputer and EEPROM use the +5V_STBY1.

Input Level 5.0V +/-8%

Current Requirement 5mA min (Standby Mode), 70mA max (Run Mode)

Ripple 100mVp-p max.

17. 15 Second Timer: The 15 second timer determines whether time-of-day clock information is discarded after a power dropout. If a dropout lasts longer than 15 seconds, the time-of-day information will be cleared. If it is less than 15 seconds, it will be retained.

18. 2ND TUNER SYNC: The 2ND_TUN_SYNC input is horizontal sync from the 2nd tuner. The separated sync is sampled by the micro to determine the presence of valid video during channel tuning.

Logic 1>3.8V (Sync active high), Logic 0 <1V

19. RUN/STANDBY: The RUN/STBY is a buffered output line used to turn on the Run supplies. Run Mode is selected when the output is a logic 1.

Logic 1>3.5V, Logic 0 <.6V

20. EEPROM ENABLE: The EEPROM ENABLE output is used to control the standby supplies going to the EEPROM. This line allows the EEPROM to be reset in the event of an SCR latch.

21. MAIN TUNER H: The Main Tuner Low-Passed Video or "Main Tuner H" input is baseband video (negative going sync) from the main tuner which will be separated by a control system sync separator. The separated sync is sampled by the micro to determine the presence of valid video during channel tuning.

Input Video 1Vp-p (sync tip to 100IRE white)

22. DI BUS ENABLE: The DI Bus Enable is not used.

23. STANDBY I^2C DATA: The STBY I^2C Data line is an I/O line, which conforms to the Philips I^2C Bus Specification. The maximum clock rate is 100kHz. The standby I^2C Data line is operational as long as the receiver is plugged in.

24. STANDBY I^2C CLOCK: The STBY I^2C CLK line is an output line, which conforms to the Philips I^2C Bus Specification. The maximum clock rate is 100kHz. The standby I^2C CLK line is operational as long as the receiver is plugged in.

25. Fast Switch (FSW): The fast switch line is the output of a 1-bit D/A. The output is active high when OSD is present.

Logic 1; >2.7V (OSD active), Logic 0; <.4V (OSD not active)

Output Bandwidth 100HZ-7MHZ

26. Blue OSD: The blue on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec.

Output Bandwidth 100HZ-7MHZ

27. Green OSD: The green on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec.

Output level 0.5Vp-p (for nominal 70 IRE OSD)

Output Bandwidth 100HZ-7MHZ

28. Red OSD: The red on-screen display signal is the output of a 3-bit D/A. The pin voltage is 1.0Vp-p (100IRE) and is divided down to 0.5Vp-p for roughly (70IRE) OSD characters. Rise and fall times after the filter are nominally 70nsec.

Output level 0.5Vp-p (for nominal 70 IRE OSD)

Output Bandwidth 100HZ-7MHZ

29. VDD1: +5V Standby Supply Voltage.

Input Level 5V +/- 8%

Current Requirement 100uA min 20mA max

Ripple 100mVp-p max.

30. VSS1: Ground return path

31. Filter CPU: Filter used to keep various unwanted signals from interfering with microprocessor functions

32. VDDA: +5V Standby Supply Voltage.

Input Level 5V +/- 8%

Current Requirement 100uA min to 20mA max

Ripple 100mVp-p max.

33. Filter OSD: Filter used to keep various unwanted signals from interfering with microprocessor functions, in this case with OSD.

34. VERTICAL SYNC: The Vertical Sync input signal to the control system is used to synchronize the OSD signal to vertical. Only the leading edge is used. The Vertical Sync signal is used to blank the OSD during vertical retrace. An internal delay is used in the main micro to insure that the leading edges of Vertical and Horizontal do not overlap. A single value of the internal Vertical delay is intended for all chassis. A spike filter, which ignores any glitch of < 2usec after an active edge is detected was added to prevent double vertical pulses on PTV instruments.

Input Level 0-5.2V max DC (active high)
Logic 1 >3.5V (Vertical active)
Logic 0 <1.0V (Vertical not active)
Max variation in edge 32usec relative to video

35. Horiz Sync or "FBP": The FBP input signal to the control system is used to synchronize the micro OSD to the flyback pulse. Only the leading edge is used. The width of the Control Horizontal Sync signal derived from the Flyback Pulse is used to

blank the OSD during horizontal retrace. The 5V level of the flyback waveform was chosen to minimize OSD variation with flyback loading.

36. IR: The IR is the infrared input to the microcomputer accepting IR from the Remote Control IR Receiver. The circuitry allows for a simultaneous 2nd IR receiver on a separate FPA for use on consoles in addition to an IR input from the Smart Plug interface which is used on commercial products.

37. +5.1V RUN A/D: The +5.1V Run supply input is sampled by a 6-bit A/D in the micro and used to verify that the supply is active and within regulation. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine which will save off the appropriate error code is the EEPROM.

Input Level 5.1V +/- 20%

Ripple 100mVp-p max.

38. +12V RUN A/D: The +12V RUN supply input is sampled by a 6-bit A/D in the micro and used to verify that the supply is active and within regulation. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine which will save off the appropriate error code is the EEPROM.

Input Level 12V +/- 20% (for valid 12V_RUN)

39. +16V STANDBY A/D: The +16V STANDBY supply input is sampled by a 6-bit A/D in the micro and used to verify that the supply is active and within regulation. Failure to meet the level specification will result in a power cycle of the entire instrument using the "batten down the hatches" routine which will save off the appropriate error code in the EEPROM. In addition, this input is sensed to control the reset of the main micro and provide a sense level for the TV Guide Plus+ Low Power Monitor. Any drop to less than 12 volts will cause the micro to run through "batten down the hatches".

The 16V STBY is also used as a power supply for the TV Guide Plus+ module

Current Requirement @16V: 25mA typical 50mA max. The total TV Guide Plus+ requirement is 50mA typical, 100mA max for both the 5VSTBY and 16VSTBY supplies.

40. OSC OUT: 4 MHz clock crystal

41. VSS2: Ground return path

42. OSC IN: 4 MHz clock crystal

43. CONTROL 1: The CTRL 1 output line is one of two audio/video control lines.

Logic 1>3.7V, Logic 0<0.4V

44. CONTROL 2: The CTRL 2 output line is one of two audio/video control lines.

Logic 1 >3.7V, Logic 0 <0.4V

45. DEGAUSS: The Degauss signal is a buffered output signal sent to operate the degauss relay. Once a power-on sequence has been initiated and the power supplies

reach a specified voltage, the Degauss line is held low (Degauss active) for approximately 1.5 seconds. Under normal conditions the Degauss line is high. The Degauss buffer transistor is located in the Deflection area.

46. SRS NORM/EN: The SRS Normal/Enhanced output is used to switch the SRS mode from normal (active high) or enhanced (active low). The SRS Norm/En line is also used to auto-detect the SRS feature at power-up. Following a reset, the SRS Norm/En line will be read as an input to determine if SRS is present. A logic 0 on the input indicates that SRS is present.

47. TILT D/A: The Tilt D/A output allows the user to compensate for the affects of the earth's magnetic field on the raster alignment. The Tilt D/A will allow a minimum of 64 customer adjustment points.

48. AVR: The AVR line is a digital input to the micro. A logic 1 indicates that the average power being delivered to the speaker is in excess of the continuous rating of the speaker. The micro senses this input and reduces the volume at a rate of 3 steps per 100msec until the AVR line is cleared. The micro will then increase the volume at a rate of 1 step per 100 msec until the AVR line is set or the original volume setting is reached.

49. SVM: The SVM (scan velocity modulation) output is used to control SVM. SVM will be turned off whenever the Sharpness control is reduced below the specified step. A logic HI indicates SVM is active. In addition, SVM will be turned off whenever the OSD is active to prevent ghosting.

50. SPEAKER_MUTE: The Speaker Mute output is used to force the power amp into a low-power / muted mode.

51. RESET: The Reset is an input to the Control System providing a reference voltage for sensing the level of the 16 Volt Standby Supply. It is normally 5.6 volts, obtained from a zener reference used for the +5V STBY1 and +5V STBY2 supplies.

Reference Voltage: 5.6V +/- 8%, Ripple: 100 mV p-p.

52. RESET I Not used for normal instrument operation at this time.

53. DATA_IN: The Data In line is a UART input line to the micro. It will be used by both the Comphone and MCR modules to communicate to the main micro. Comphone and MCR are mutually exclusive features.

54. DATA_OUT: The Data Out line is the output from a UART in the micro. It will be used by the MCR to communicate to the main micro. The Comphone On/Off output line is used to activate the Comphone feature. A Logic 1 (high) indicates that the Comphone IC is active. A Logic 0 indicates that the Comphone feature is in low-power mode. The DATA_OUT line is auto-detected to determine the presence of either the Comphone or MCR feature.

55. FM_TUNED:

The FM Tuned input is active high when an FM channel is present. The micro uses the input state to control the tuning and OSD.

56. FM_STEREO: The FM Stereo input is active high a stereo FM channel is present. The micro uses the input state to control the OSD.

IR Input

Infrared remote signals are amplified by IR3401 and appear at U3101 pin 36 as 5 Vp-p negative going data pulses. When no IR is received, the DC level at U3101 pin 36 is 5V. IR3401 is powered by the 5V standby supply. There is no power indicator LED on the normal CTC197 chassis.

OSD Circuit

The CTC195/197 *O*n *S*creen *D*isplay circuit consists of red, green and blue analog signals from U3101 pins 28, 27 and 26 respectively. These signals along with the FSW (fast switch) signal from pin 25 are sent to the T4 Chip through buffer transistors Q12701, Q12703 and Q12702 and input to U16201 pins 34, 35 and 36. These on screen display signals include the television user menus and also any closed caption information. The FSW signal is also used by the T4 chip to turn off edge replacement during the time interval OSD is active, preventing incoming video from appearing in the OSD.

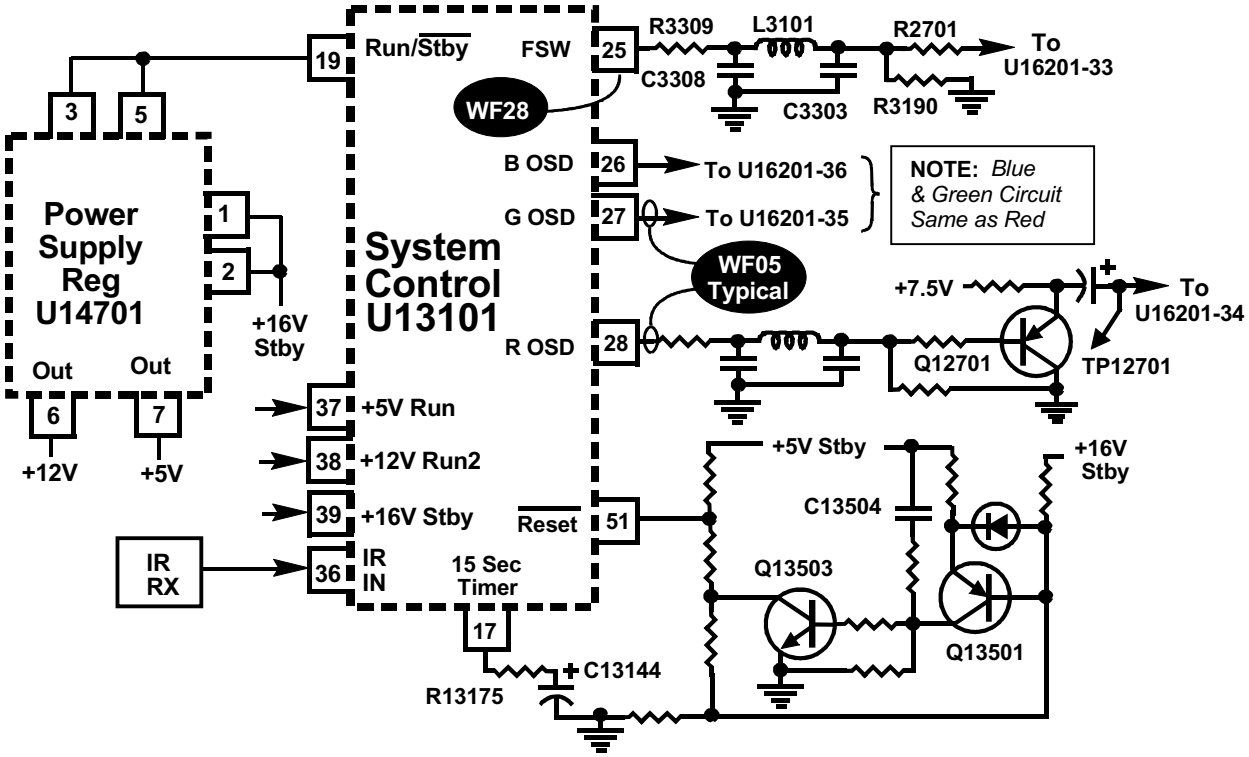
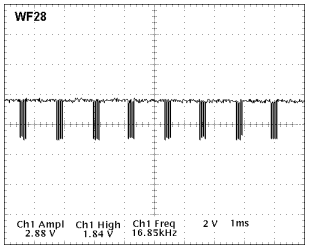
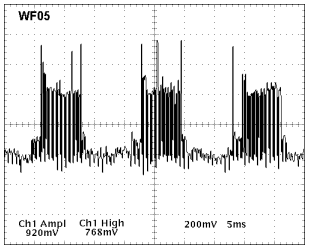


Figure 6-10, OSD Output Buffer





Service Menu

The CTC195/197 chassis has a more limited built-in service menu than the previous CTC177/187 and CTC179/189 chassis. Only a few CRT setup alignments and picture geometry adjustments are provided for internally.

All other alignments must be performed with a computer using Chipper Check™, TCE's computer-based troubleshooting/alignment software.

To enter the on-board service menu, with the instrument on, press and hold the **Menu** button. Then while continuing to hold the **Menu** button, press and release the **Power** button. Then press and release the **Volume +** button. The instrument should immediately display a one line menu on the screen. The decimal value on the left is the parameter number and the decimal value on the right is the current value of that parameter. The **Channel-Up** and **Channel-Down** buttons increment and decrement the parameter number, while the **Volume+** and **Volume-** buttons adjust the current value of that parameter. When parameters are modified, the corresponding T4-Chip (or tuner) registers and EEPROM locations are updated. The **Power-On**, **Power-Off** buttons on the menu, or **Power-Toggle** button on the front panel exit service mode. The number below and in the center is the software version number.

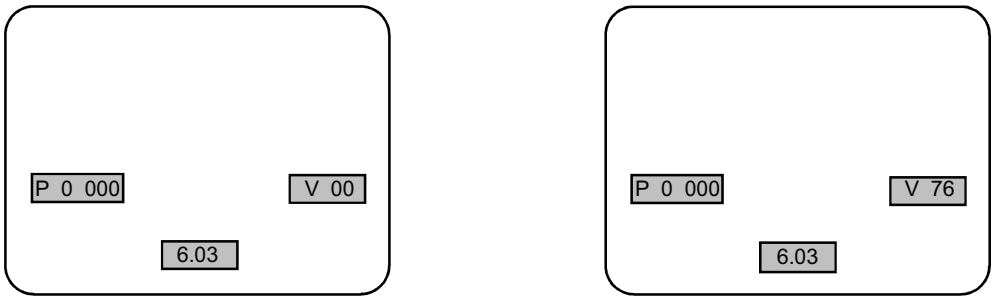


Figure 6-11, Service Menu Access

Under normal conditions, a failure of an I^2C device will prevent the TV from turning on. Because a possible reason for needing service is a failed bus IC, the normal check for acknowledge is disabled in the service mode. If an I^2C device has failed, its address will be stored in the error code area (see next section).

When the service mode is first turned on, the parameter will be 0. This 0 parameter is used for security purposes to protect the factory alignments from inadvertent modification by requiring a specific value be selected before other parameters may be accessed. If channel up is pressed while in parameter 0, the service mode will be exited. One security parameter must be selected before the service technician proceeds to any of the main groups. Each parameter group will also have a prefix number displayed between the P and parameter number used to tell the service technician which set of parameters he is currently adjusting. To select the security parameter, while in parameter 0, change the value (using volume up/down) to 76 or 80 for levels 0 or 1 respectively. These will be the only parameters available to the technician from the front panel of the instrument. All other alignments or adjustments are only accessible via the Chipper Check™ troubleshooting software and a PC.

Error Codes

Upon certain errors occurring in the chassis, an error code will be stored in the EEPROM. This error code is displayed to the service technician as the value located at parameter 0 01, 0 02 and 0 03. If a 0 is stored, there have been no errors. If there is a nonzero value, however, the following table describes what error occurred. If multiple errors occur, the first error is stored in 01, the second error is stored in 02 and **the last error to occur is stored in 03**. Because only the last error location (03) is incremented upon each additional error, the error codes should all be reset to 0 upon completion of the service effort so that a three error code history will be available in the future. The error code numbers are changed just like the other alignment parameters

If an IC error code is found that is the same as one in the table, then that device did not acknowledge. For example, if the error code is 128, the Stereo Decoder (U11600) did not acknowledge. If the error code is the same as any in the table, but incremented by 1 (129) then the read register did not respond. The problem indicated is still the Stereo Decoder.

Error Codes (DEC)	Chassis	Error	Device	Condition
0	All	Power OK		No Error Codes Thrown
2	All	5V Run Supply	Micro	5.1V supply low
3	All	12V Run Supply	Micro	12V supply low
8	All	XRP	U6201	XRP detected by T4
9	All	T4 POR	U6201	Power On Reset at T4
10	w/FPIP	FPIP POR	U8100	Power On Reset at FPIP
11	All	Stereo Decoder POR	U1600	Power On Reset at Stereo Decoder
12	All	AVR Latched	Micro	AVR input to micro held low
16	All	I2C Run bus Latched	Micro	Run I2C clock or data line clamped at logic 0
20	All	Software Stack Overflow	Micro	Note Condition in which Occured
21	All	FPIP/Vid Sw Mismatch	Micro	Vid Sw Detected but FPIP Doesn't ACK on I2C bus
22	All	4 Strikes Your Out	Micro	Code is thrown after 4th unsuccessful try to Re-Start
44	w/FPIP	FPIP Fault	U8100	Failure to receive ACK from FPIP
56	w/Digital Convergence	Digital Convergence I2C bus		Failure to receive ACK from Digital Convergence Module
64	w/2nd Tuner	2nd Tuner DAC bus fault	U7902	Failure to receive ACK from 2nd Tuner DAC
102	All w/GemStar	GemStar Fault	GemStar	GemStar module did not ACK to Sys Ctl Micro
103	All w/GemStar	GemStar Fault	GemStar	GemStar module did not ACK to Sys Ctl Micro
128	All	Stereo Demodulator	U1600	Failure to receive ACK from Stereo Demodulator
130	w/Audio Compressor	Audio Compressor	U1501	Failure to receive ACK from Audio Compressor
134	All	Video Matrix	U6901	Failure to receive ACK from Video Matrix Switch
186	All	T4 Chip	U6201	Failure to receive ACK from T4
196	All	Main Tuner PLL	U7501	Failure to receive ACK from Main Tuner PLL
198	All	Main Tuner DAC	U7501	Failure to receive ACK from Main Tuner DAC
220	w/Decoder Interface	Interface Bus Fault	Decoder Module	Failure of communicaions with Decoder Interface Micro

Table 6-1, Error Code Table

Other error codes may indicate a failure condition some other place in the chassis, such as the power supply. It is important to understand how these error codes are detected by the system control circuitry so they can be interpreted correctly and used accordingly. Most of the error codes are self-explanatory. However some require additional explanation

There are four power supply error codes – 1, 2, 3 and 4. They monitor the run supplies for any voltages dipping below a preset level. A detailed explanation of the microprocessors role in monitoring the power supplies and incoming AC power has been given in previous discussions.

Unfortunately, any of the above failures will prevent the television from turning on, making the error codes impossible to read via the service menu. These error codes can only be checked by reading the EEPROM directly. This can be accomplished by using the industry's first color television computer based alignment software called "Chipper Check™." Chipper Check™ allows the service technician to perform digital alignments, read the diagnostic error codes and check the hardware integrity of EEPROM. This can literally reduce repair time by hours by accelerating the alignment process, preventing unnecessary parts orders and by giving the technician a means of checking the EEPROM even when the TV will not turn on. Chipper Check™ is now available. Contact TCE Publications at (502) 491-8110 for more information.

Error code 4 is a Run Supply Momentary Dropout. This error code is logged when the microprocessor realizes the power supply turned off for a moment but when checked 500 msec later, it was back on. This is detected by U3101 pin 37 and 38 by monitoring the +5 and +12 volt run supplies.

Troubleshooting

The system control circuit controls every function of the TV. A failure in this circuit will cause the entire TV to malfunction. Provided U13101, U13102, and U16201 are functioning, the set can be forced to turn on in the service mode by holding down the MENU button and pressing POWER and VOLUME UP in that order. Entering the service menu and reading the error codes will lead the technician to the defective circuit area. In some cases, the set will not be able to be forced on even in the service mode. In these cases, the set will most likely try to start three times and then stop or remain silent and do nothing at all. When the technician encounters this, the TCE troubleshooting and alignment software, Chipper Check™, may be used to read the EEPROM error codes to begin repair efforts.

I²C Bus

When the set is first plugged in, the Standby I²C data and clock lines (U13101 pins 23 & 24) will have about 50 milliseconds of 5 volt p-p data and clock. The pulses are at approximately 50 kHz. After the initial data and clock activity are sent by the micro, both the standby data and clock lines should go low and remain.

Before sending out an I²C command, the software checks that the lines are high. If something is clamping the bus, the software will remove power from the EEPROM for 30 milliseconds and then attempt to send the command again. If the bus worked, the micro will write an error code (bus latch) to the service menu location.

When an attempt is made to turn the set on, the RUN/STANDBY line (U13101 pin 19) will be set high and the T4 Chip will be toggled off, then an ON command will be sent. The micro will check the Run Data and Clock lines the same as it did the Standby lines before attempting to send the command. If the set does not turn on, check the level of the of the Run Data and Clock lines at the time the RUN/STANDBY pin goes high. The data line should have information within 40 milliseconds after the RUN/STANDBY line goes high. If both do not go high, something is loading one of the lines. The micro should have written the appropriate error code in the service menu location.

Three Strikes and You're Out

This is the term used to describe what the software does following the detection of an I²C Bus error indicating hardware or software failure. Normally, the micro sends out commands, then waits for an acknowledgment that the command was received. The software attempts to re-send any commands when it does not receive that acknowledgment. If the command is not acknowledged after the second attempt, the "batten down the hatches" sequence is initiated. "Batten" stores off information to the EEPROM and then removes power from the instrument. The software will then attempt to restore power to the instrument. If the error is not corrected, the software will repeat the "batten down the hatches" routine two more times before shutting the set off again. The set must then be manually turned on for the "three strikes and you're out" counter to be reset.

Dead Set - Degauss Relay Clicks

If the television tries to start three times and then stops (you can hear the clicking sound of the Degauss relay energizing), this means the EEPROM (U13102) and T4 Chip (U16201) are working (hardware is OK). Therefore the problem is most likely power supply and/or deflection related. To isolate the fault, perform the following steps.

1. Check the +16 volt standby supply input at pin 39 for proper voltage. Also check for a HI signal from the RUN/STANDBY pin 19.

2. Confirm proper power supply operation by checking the inputs to pins 37, 38 and 51. These are the +5.1 and +12 Volt Run supply voltages and the micro reset pin.

3. Apply normal AC and confirm that horizontal pulses are momentarily output at pin 22 of U16201, the T4 Chip, when the power button is pressed. If pulses are not output suspect a defective U16201 or corrupt data in U13102. If pulses are output, go to the next step.

4. Unsolder the collector of the horizontal output transistor, Q14401.

5. Press the power button so the set attempts to start. Before the third start attempt, apply an external +16 volt supply to the cathode of CR14107. This will hold up the +12 volt run supply satisfying the run detector at U13101 pin 38. Once the main power supply comes up, the external supply can be removed. Confirm horizontal drive pulses continue to be output at U16201 pin 22. This confirms a horizontal deflection problem. See page 36 for horizontal deflection troubleshooting procedures.

Dead Set - No Clicking Relay

1. Press the power button and check for U13101 pin 19 to go HI (+5V). If it goes HI, check power supply regulator, U14701, and its associated circuitry in the power supply on/off control circuitry. If they check OK, suspect a power supply problem. See page 18 for power supply troubleshooting. If U13101 pin 19 does not go HI, go to the next step.

2. Check U13101 pins 16, 29 and 32 for the +5V standby supply. Check pin 8 of U13102 for +5V standby supply. Check pins 3 and 20 of U16201 for the +7.6 volt supply. If all the supplies are present, go to the next step. If any of the standby supplies are missing, check the respective +5V standby supply source and the EEPROM / T4 Chip power control circuit.

3. Check the reset signal on U13101 pin 51 for approximately 5 volts. If this pin is LO, troubleshoot the reset circuitry. If this pin is HI, go to the next step.

4. Check U13101 pins 40 and 42 for ~ 4.5 Vp-p 4MHz sine-wave (using X10 probe). If it is not present, suspect a defective Y13101, C13106, C13107, R13107 or U13101. If the oscillator is present, go to the next step.

5. Monitor U13101 pin 23 with an oscilloscope set at 10 msec/div when 120 V.A.C. is applied to the set. Check for the presence of momentary clock and data pulses after the data line rises to 5 volts. If the data line goes HI and the pulses appear, go to step 7.

6. If the data line does not go to +5 volts, unsolder pin 23 of U13101 and see if the pad goes up to +5V. If it does, U13101 is most likely loading down the bus and is defective. If it does not go up, check the +5V pull-up supply from R13327 and check for a device loading down the data line. If the data line goes HI but the negative going pulses do not appear, unsolder the clock line (U13101- pin 24) and check for continuous pulses from pin 23. If the pulses do not appear, suspect a problem with U13101. If the negative going pulses appear when power is first applied or when the clock line is disconnected, go to the next step.

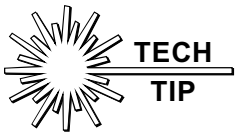
7. Reconnect the clock line if it was disconnected in the previous step. Press the power button and look for data activity from the data line, U13101 pin 23. If data pulses appear when the power button is pressed, go to the next step. If no pulses appear, suspect a problem with the front panel or the keyboard drive and scan lines.

8. Check pins 43 and 44 of the T4 Chip to see if the clock and data pulses are present. If they are present, suspect a problem with U16201 or U13102.

No Remote Control

Check for an idle voltage of 5V (logic HI) at pin 36. Press any IR button and check for a series of 5V p-p pulses at pin 36 of U3101. If the pulses are not present, suspect a defective IR13401 or a missing +5V standby supply to pin 2 of IR13401

NOTE: *Some IR receivers may be oversensitive to fluorescent lighting. If pin 36 shows 5Vp-p of constant noise, remove the lighting and recheck. Also note that the keyboard input has priority over the IR input. If a keyboard button is stuck, the IR input will be ignored.*



No Keyboard Operation

The keyboard drive line, pin 51 of U3101, should have a 5Vp-p square wave on it at all times. The sense lines, pins 6, 7 and 8 should be at logic HI (5V). The Power, Volume-up and Volume-down buttons will cause the respective sense lines to follow the drive line. Menu, Channel-up and Channel-down will cause the sense lines to go low (ground).

No OSD

While trying to display OSD, trace the red , green and blue OSD signals from U13101 pins 28, 27 and 26 to U16201 pins 34, 35 and 36 respectively. Also check for the presence of horizontal and vertical sync at U13101 pins 34 and 35.

No Closed Caption Display

In the CTC195/197, the same circuitry that drives the closed caption circuitry also drives the OSD. If there is OSD but no closed caption, check the video signal at U13101 pin 15. If there is no OSD, troubleshoot the OSD circuitry.

XRP Shutdown

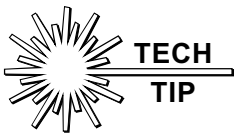
An XRP code (#8) in the service menu signifies that an error condition exists that may cause the set to emit X-Rays. The XRP trip code is sent back to the micro from the T4 Chip. The XRP circuitry must be examined.

POR (Power On Reset)

Several of the I²C devices have internal POR registers that indicate when the power supply voltage has dropped below where the internal registers can guarantee reliable data transfers. The micro reads this data as part of its Periodic Update routine. If a supply has dropped below the set levels in any of the IC's, the set will be turned off and then go into the "three strikes and you're out" routine. If the set does not start back up, read the error codes with Chipper Check™ to determine which IC has generated the POR.

Run Bus Latch

This will occur when either the RUN Data or Clock lines are clamped to ground. This could be caused by a circuit path short in the Data or Clock lines or the power supply to the I²C device shorting to ground or pulled high. The error codes will indicate which device to troubleshoot.



NOTE: *Any IC connected to the I²C Bus must be fully powered to prevent protection diodes, used to prevent ESD on the bus line, from clamping the bus.*

Power Supply Error

The microprocessor monitors three supplies directly and one indirectly. They are the +5, +12 and the +16 Volt Run supplies and indirectly the +7.5 Volt standby supply. If the error codes indicate a Run supply error, the supplies can be checked at Regulator U14701. Pin 7 is the +5V and Pin 6 is the +12V. The +7.6V Run supply can be checked at pin 3 of regulator U14104.

Main Tuner

The CTC 195/197 tuner continues to employ TOB (Tuner On Board) topography with a zinc tuner wrap. It is a single conversion, electronically aligned tuner based on the CTC 179/189 chassis family tuner. There will be two variations:

1) A single input tuner
2) A single input tuner with PIP RF output

The second tuner is not based on the CTC 197 but is a "cold" version of the CTC 185 tuner. There are many similarities between the two. Refer to the *Second Tuner/IF* section of this manual for a further description of the circuitry.

The evolution in the CTC195/197 tuner is a result of the need for improved performance electrically and in direct pickup immunity.

Changes made initially for the CTC195/197 include use of a PLL (Phase Locked Loop) with DAC (Digital to Analog Converter) IC. Although this IC will cause an increase in tuning time over the very fast CTC179/189 tuner, it will eliminate the need for external RF DAC's.

A new splitter has been developed which will improve main tuner performance at the expense of some PIP tuner noise figures. The newly developed UHF/VHF interface has resulted in reduced manufacturing cost and improved performance.

The tuner can be separated into three distinct sections for discussion. First, the RF stage which processes the incoming antenna or cable RF signal. This stage captures, filters and amplifies the RF for further processing. Next, the mixer/oscillator converts the different high frequency RF carriers to a single IF frequency for use by the remainder of the television circuitry. The PLL IC controls the RF and mixer/oscillator circuit. The PLL communicates with the main microprocessor for channel selection information, then converts the digital information to analog voltages needed to tune the RF and mixer/oscillator to the proper frequency.

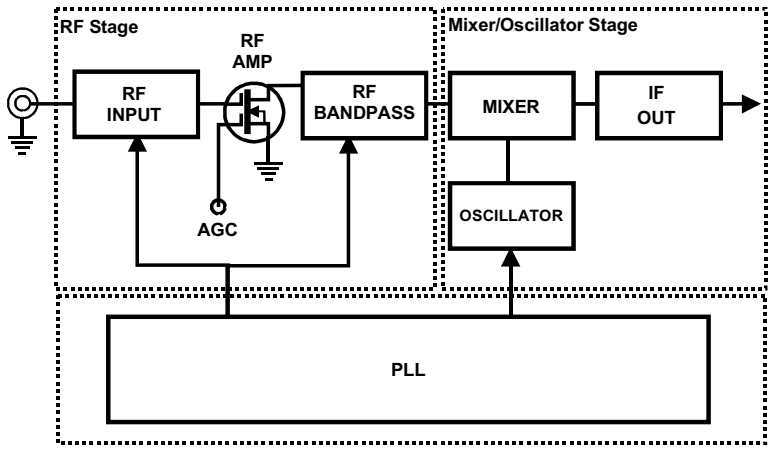
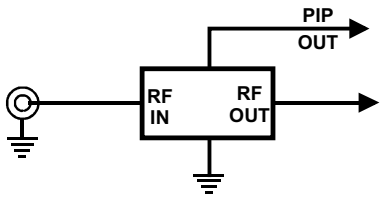


Figure 7-1, Tuner Block Diagram

Figure 7-2, RF Input Splitter (Twin-Tuner Chassis Versions)



Input Splitter

Chassis variations with a single tuner will have only a VHF/UHF splitter to route those frequencies to the proper RF amplifier. PIP chassis will use an input splitter to send a reduced (7-9 dB) RF signal to the PIP tuner and pass the RF signal on to the main VHF/UHF splitter. The splitter then routes the proper signals to one of two RF amplifiers.

Single Tuned Input Filtering

Single tuned input filtering is a method of narrowing the RF bandwidth closer to the specific channel selection. The narrowed signal is then input to the RF amplifier. This reduces interference problems and increases the gain and AGC of the stage. The PLL IC controls the frequency response curve of the input filter by using output voltages from pins 6 and 14 to change the characteristics of the tank circuit and the RF amplifier. Pin 6 is a variable DAC output voltage while pin 14 is a high or low voltage depending upon the selected band. The chart in figure 7-3, shows the voltage selection for the different RF bands and channels. The chart is a representation of tuning voltages for off-air channel selection. Notice that as channel selection goes up through the VHF, then the UHF bands, the tuning voltage on pin 6 rises until the first UHF channel selection (14). At that point, the band switching on pin 14 goes from high to low and the DAC output voltages go down and begin the tuning cycle. This becomes the beginning of the tuning cycle.

Channel	U17501 Pin 6 (Single-tuned Filter)	U17501 Pin 14 (Band Switching)
2	1.2 V	HIGH
6	7.8 V	HIGH
7	4.5 V	HIGH
13	6.9 V	HIGH
14	5.1 V	LOW
69	25.4 V	LOW

Figure 7-3, Input Band Filter Switching Chart

RF Amplifier

The CTC195/197 uses a single-stage dual-gate depletion type FET (Field Effect Transistor). FET's are used in the first RF amplifier to provide the highest gain and lowest noise. These FET's are voltage controlled devices that operate very similar to vacuum tubes. When negative voltage is applied to the gate with respect to the source, drain current is reduced. If the negative voltage is high enough, drain current is pinched off completely. Positive voltage on the gate with respect to the source will increase drain current.

Both gates on the dual-gate MOSFET's affect drain current. In this chassis, the RF input is on gate 1 and the AGC (Automatic Gain Control) is placed on gate 2. As the AGC voltage increases (positive with respect to the source) drain current also increases. When AGC voltage decreases drain current decreases. The AGC voltage is generated from the T4 chip that is monitoring the IF signal level. If the IF signal level increases, AGC voltage is reduced, lowering the gain of the RF amplifier. If the IF signal decreases, AGC voltage increases raising the gain of the RF amplifier.

RF Bandpass

The CTC195/197 tuner uses a double-tuned bandpass filter after the RF amplifier to further increase the signal selectivity and noise rejection of the RF stage of the tuner. Using varactor and PIN diodes, the stage is "tuned" to the desired range of frequencies by the output voltages of the PLL IC. Transformers provide impedance matching for the remainder of the RF stage.

Mixer/Oscillator

U17701 comprises an entire mixer/oscillator network with very few external components. The IC contains circuitry that performs traditional mixer/oscillator duties, heterodyning the incoming RF signal against an internally generated frequency to always produce a 45.75 MHz IF signal. This IF is then sent to the T4 Chip for further processing and to separate the video and audio IF signals.

IF Bandpass

To further filter the IF signal after it leaves the mixer/oscillator, there is an IF filter and buffer transistor. The varactors are controlled by the U13101, the main microprocessor. Generally, these are used to fine-tune the IF bandpass as measured by the T4 Chip.

PLL / Frequency Synthesizer

The PLL uses a Motorola PLL/DAC IC previously used in the CTC185. The PLL section of the IC is similar to others. What is unique is that it contains three DAC's (Digital-to-Analog Converters) for electronic alignment. The DAC's in the PLL/DAC IC eliminate the need to use microprocessor or individual DAC's, with the exception of the IF DAC's. The DAC's use higher voltage outputs than before capable of generating proper RF filter voltages without the addition of discrete amplifiers.

The purpose of the PLL circuit is to process channel selection information from the microprocessor, receive feedback from the mixer/oscillator and adjust the incoming RF filters, the local oscillator and associated tank circuits to provide the proper tuner IF output signal based on the channel selection. It also bandswitches the local oscillator and RF circuits. It isolates the channel selection by first broadband tuning the frequency response of the tuner to break the entire RF broadcast band into three smaller bands, then retuning the input RF filter and double-tuned tank circuits to closely define the channel and finally matching the local oscillator frequency to the incoming channel carrier to provide the proper IF output frequency.

Figure 7-4 is a block diagram of a basic PLL circuit. The voltage-controlled oscillator (VCO) output is sampled by a phase/frequency comparator. The comparator compares the sampled frequency against a reference signal provided by a stable crystal–controlled oscillator. When the sampled frequency is not the same as the crystal–controlled

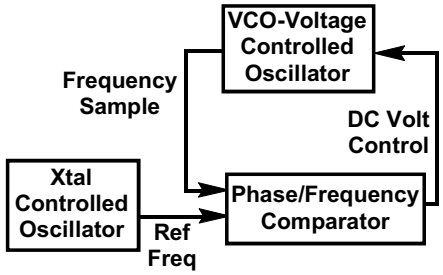


Figure 7-4, Basic PLL Diagram

oscillator, an error signal is generated by the comparator. The error voltage corrects the VCO until the two frequencies are identical again. The VCO will now stay locked to the reference crystal oscillator.

The PLL has three DAC and three bandswitching outputs. There are also several inputs to monitor the local oscillator frequency. The bandswitch outputs are either high (+12V or +5V) or low (0V) while the DAC outputs can vary between 0 and +33 volts.

Bandswitching

The bandswitch outputs are what determines the overall response of the tuner based upon the channel selection. The three bandswitch outputs, pins 14, 15 and 17 select between the VHF and UHF broadband components of the tuner. Pin 14 selects the UHF or the VHF RF amplifier. Pin 15 selects the VHF or UHF mixer that is internal to U17701. Pin 17 selects either the VHF or UHF local oscillator circuitry on and off. Bandswitching is accomplished by using PIN diodes to switch in and out inductors and capacitors to deermine the frequency range of the tuning circuitry. This filter network is refined enough to easily narrow down the broadcast spectrum to isolate one channel in less than 150 milliseconds.

The following charts show the PLL output pin voltages associated with band switching and the channels in each of the three tuning bands. Notice that these bands do not follow the standard off-air or cable band designations, but are based upon the linear progression of the individual channels within the broadcast frequency range

Tuning

Fine tuning down to a single station is dependant upon the PLL open collector output voltages from pins 6, 7 and 8 and the control of the RF filter voltages used to center the RF frequency response curve over the desired channel. Pin 6 controls the frequency response of the incoming single-tuned filter. Pin 7 controls the frequency response of the primary coil of the double-tuned filter stage, while pin 8 controls the secondary. Each of the lines provide different outputs depending upon the frequencies being tuned.

U17501 Pin	Callout	Band 1	Band 2	Band 3
14	BV/U	Low	Low	High
15	BSX	Low	Low	High
17	BS1/2	High	Low	High

Figure 7-5, Band Switch Chart

Band	Channels		Frequency Range
	Cable	Off-Air	
1	1-6, 95-99, 14-17	2-6	54-144 MHz
2	7-13, 18-50	7-13	144-384 MHz
3	51-125	14-69	384-804 MHz

Figure 7-6, Frequency Band Tuning of RF Amplifiers

In order to compress the amount of information stored in the EEPROM, only the exact information required to tune a few channels, known as *alignment channels*, have been chosen. *Only the exact value needed to tune these channels are stored by the EEPROM.* When a channel selection is made, the microprocessor decides what band it is in, then what two alignment values it lies between. It must then interpolate or *calculate* the DAC values required to tune the channel. This information is then sent via the I²C bus to the PLL IC, which changes the frequency response of the tuner for proper channel reception. Because changing one alignment value may affect the interpolation of many of the alignment channels, if any of the alignment values are changed, every value must be checked.

Channel Selection

The microprocessor goes through a routine to effect channel selection. Although the instruction routine is lengthy, it is accomplished in less than 150 milliseconds. First, all information necessary to select the channel is retrieved from the EEPROM. This includes the Local Oscillator data for the channel, the band switch information and the upper and lower alignment channel DAC values for the frequency range that the channel lies within. Now the actual electrical tuning of the RF receiver section may begin.

The LO and Band Switch information is delivered to the PLL IC and the PLL sets the RF bandpass filters and the LO frequency to the desired values. Next, the interpolation process begins. The correct DAC values for the specific channel selection are calculated by the microprocessor and sent to the PLL IC which then sets the proper voltages on the RF tuning filters to correctly center the tuner frequency response for the selected channel.

For example, the microprocessor has a request (from the IR remote control or front panel keyboard) to tune cable channel 53. First, the local oscillator frequency is retrieved and sent to the PLL for output from pin 5, the loop filter. A feedback loop insures the local oscillator remains on frequency. Then the bandswitches values are retrieved and sent to the PLL and the outputs on pins 14, 15 and 17 are set. In this case, channel 53 is within tuning band 3 so all three pins would be set high. Channel 53 lies between alignment channels 51 and 57, so the microprocessor must now calculate the exact DAC values to send the PLL in order to place the proper voltages from the DAC's on pins 6, 7 and 8. These voltages tune the RF stage to the exact channel requested. The microprocessor may use any combination of adjacent frequencies to interpolate the required channel values as long as the frequencies remain in the same band.

Channel	Band	Midrange (MHz)	Pix Carrier (MHz)	Local Oscillator (MHz)
2	1	57	55.25	101
3	1	63	61.25	107
6	1	85	83.25	129
98	1	111	109.25	155
14	1	123	121.25	167
17	1	141	139.25	185
18	2	147	145.25	191
13	2	213	211.25	257
29	2	255	253.25	299
35	2	291	289.25	335
41	2	327	325.25	371
45	2	351	349.25	395
48	2	369	367.25	413
50	2	381	379.25	425
51	3	387	385.25	431
57	3	423	421.25	467
60	3	441	439.25	485
64	3	465	463.25	509
68	3	489	487.25	533
76	3	537	535.25	581
83	3	579	577.25	623
88	3	609	601.25	653
93	3	639	637.25	683
105	3	681	679.25	125
110	3	711	709.25	755
115	3	741	739.25	785
120	3	771	769.25	815
123	3	789	787.25	833
125	3	801	799.25	845

Figure 7-7, Tuner Alignment Channels

Software Control

The PLL/DAC IC is controlled from the micro over the I²C bus. Data is sent, according to I²C bus specifications, in packets of two to five bytes with the first byte being the address byte. There is a *start* condition at the beginning of an address byte and a *stop* condition at the end of the data with an *acknowledge* condition at the end of each byte.

EEPROM Requirements

Since the tuner's RF filters are electronically aligned, the alignment values need to be stored in nonvolatile memory to be used only when tuning channels. This section lists the data format and amount of memory required for alignment data storage in the chassis EEPROM. Three bytes are needed for each alignment channel. There are 29 alignment channels which totals 87 bytes of memory. The segment of memory for alignment data is stored in the order of frequency of the alignment channels. The lowest 3 bytes contain the lowest frequency alignment channel data and the highest 3 bytes contain the highest frequency alignment channel data. The alignment values for a second PIP tuner are different and therefore require a second set of storage locations. The DAC values stored in the EEPROM and that show up on the Chipper Check tuner alignment screen, return values from 0 to 63. The actual alignment values are -31 to +31. The alignment values are translated before storing them in the EEPROM by adding 31.

IF Alignment

The IF bandpass circuits are also voltage controlled, but not by the PLL. The IF alignment voltages come directly from the microprocessor based on feedback from the T4 Chip and the original IF alignment. The IF filters remove any remnants of the "sum" frequencies created from the mixing of the incoming RF with the LO that might have escaped from U11701, leaving only the "difference" frequency of 45.75 MHz. The purpose is to improve adjacent channel selectivity. The values from the EEPROM for the IF alignments are recovered and written to the two D/A ports on the microprocessor. These values are the same for all channels, and no further adjustments beyond initial setup are needed.

IF DACS

The D/A conversion for the IF alignment and filters is supplied by the microprocessor on the main board and range from 0-12V.

Tuner Alignment

The purpose of the tuner alignment is to tell the microprocessor what the correct DAC values for each of the 29 alignment channels are. Once these values are known, the required values for any channel can be calculated using mathematical formulas. For example, referring back to the previous discussion of a request to tune channel 53, we will assume that the DAC output voltage for the primary of the double-tuned filter for alignment channel 51 is 20 volts and alignment channel 57 is 25 volts. (These values may not be exact. Always consult the service literature for more reliable voltage references.) The microprocessor has memorized these values from the alignment procedures. Using an internal formula, the microprocessor can now calculate the voltage needed to tune channel 53, send that information in digital form to the PLL IC which in turn will convert it to an analog voltage output from pin 7. The other PLL DAC

outputs are similarly changed by microprocessor communication based upon the channel selection. The microprocessor EEPROM also contains a table of the local oscillator frequencies for every off-air and cable channel. This table allows the microprocessor to send out a digital code that is interpreted by the PLL as the exact LO frequency. This reference frequency is compared to a sample of the LO provided by pins 1 and 2 of IC U17701, the Mixer/Oscillator. Any difference in the frequencies results in an error correction output from PLL pin 2 which changes the LO frequency at U17701 until the exact frequency, as determined by the reference provided by the 4 MHz Crystal and data from the microprocessor, is reached.

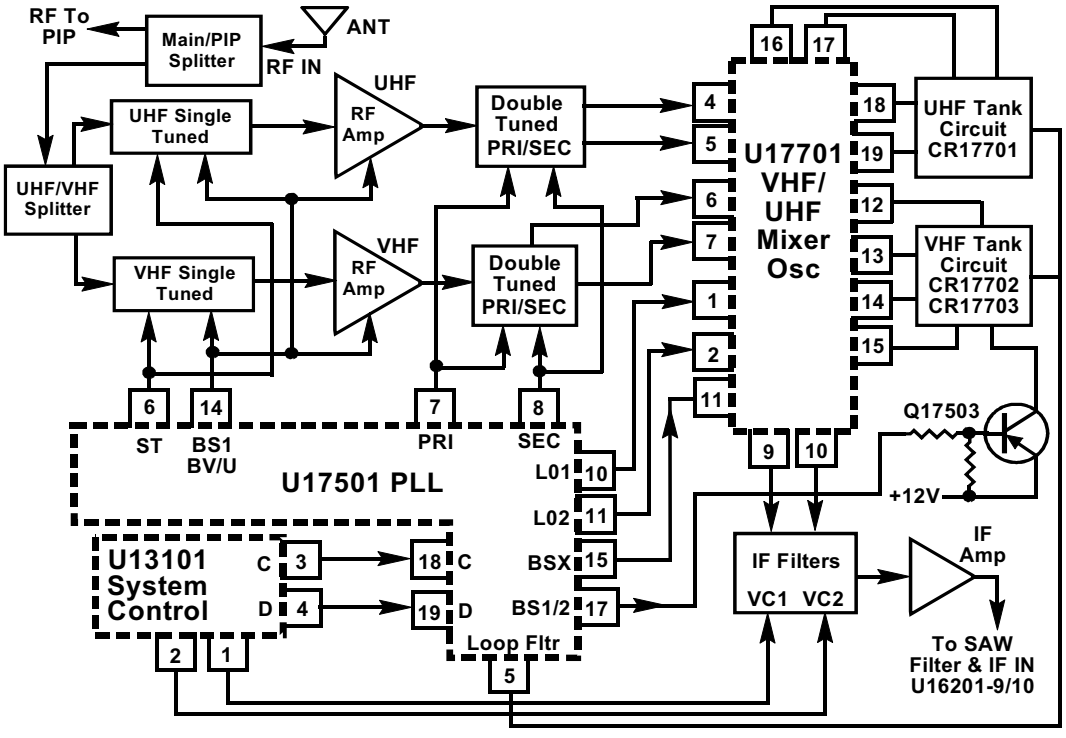


Figure 7-8, Main Tuner Block Diagram

Troubleshooting

The technician will be required to troubleshoot the CTC195/197 tuner down to the component level. Past experience with the TOB technology is essential. A basic knowledge of tuner theory, a good DVM and Chipper Check™ will enable the technician to troubleshoot, repair and align the tuner.

For a review of tuner and TOB fundamentals refer to these previous TCE publications:

- T-CTC175/6/7-1,
- T-CTC177/187-TSG,
- T-CTC185-1

Electronic Alignment

After any component replacement the tuner must be checked for proper alignment and if needed, realigned. Electronic alignment should begin with the lowest alignment channel of each band and continue to the top channel. The bands should be aligned in order. Preset all three RF filters to 0, input a signal at the midrange of the channel frequency for the channel being aligned. Adjust the RF filter DAC for peak tuner gain as measured at the proper test point.

For Band 1, the secondary DAC is aligned first, then the primary and last the single tuned. For bands 2 and 3, the secondary DAC is aligned first followed by the single tuned, then the primary. The single tuned DAC is then repeated.

RF Bandswitching

There are three bandswitching outputs from the PLL IC that affect the RF circuits and the Mixer/Oscillator. The bandswitching charts shown in Figures 7-9 and 7-10 should be the basis for troubleshooting in this area. Pin 14 of U17501, the PLL IC, controls the RF amplifiers, switching the supply voltages off and on using a single transistor.

U17501 Pin	Callout	Band 1	Band 2	Band 3
14	BV/U	Low	Low	High
15	BSX	Low	Low	High
17	BS1/2	High	Low	High

Figure 7-9, Band Switch Chart (Repeated)

Figure 7-10 shows typical voltages used by the PLL to switch between the three tuning bands. Remember again, that these bands are not the traditional Low VHF, High VHF and UHF/Cable bands, but are bands based on the frequencies of the channels. Refer to Figure 7-7 in this chapter for the actual tuning bands and the channels located within those bands. There are no alignment values or procedures associated with the bandswitch circuitry.

	Channel Frequencies 54-144 MHz	Channel Frequencies 144-384 MHz	Channel Frequencies 384-804 MHz
U17501 Pin 14	+11.7V	+11.7V	+0.3V
U17501 Pin 15	+0.1V	+0.1V	+4.8V
U17501 Pin 17	+11.7V	+0.2V	+11.7V
Q17504 B	+11.7V	+11.7V	+11.0V
Q17504 C	+0.4V	+0.4V	+11.7V
Q17505 C	+0.1V	+0.1V	+11.7V
Q17503 B	+11.7V	+11.0V	+11.7V
Q17503 C	-11.1V	+11.6V	-11.1V

Figure 7-10, Bandswitching Voltage Chart

There are two power supply voltages associated with band switching, the +12V and +5V. If the +12V supply is inoperative, all bandswitching would cease. Since the PLL depends on the +5V supply for power, if it were inoperative, bandswitching would cease. However, if the +5V supply did not reach the PLL bandswitch circuits, the PLL would still be operative, but the BSX line going to U17701, the Mixer/Oscillator would cease switching. Providing all other circuitry is operative, the only symptom will be the tuners inability to select band 3, and all associated channels.

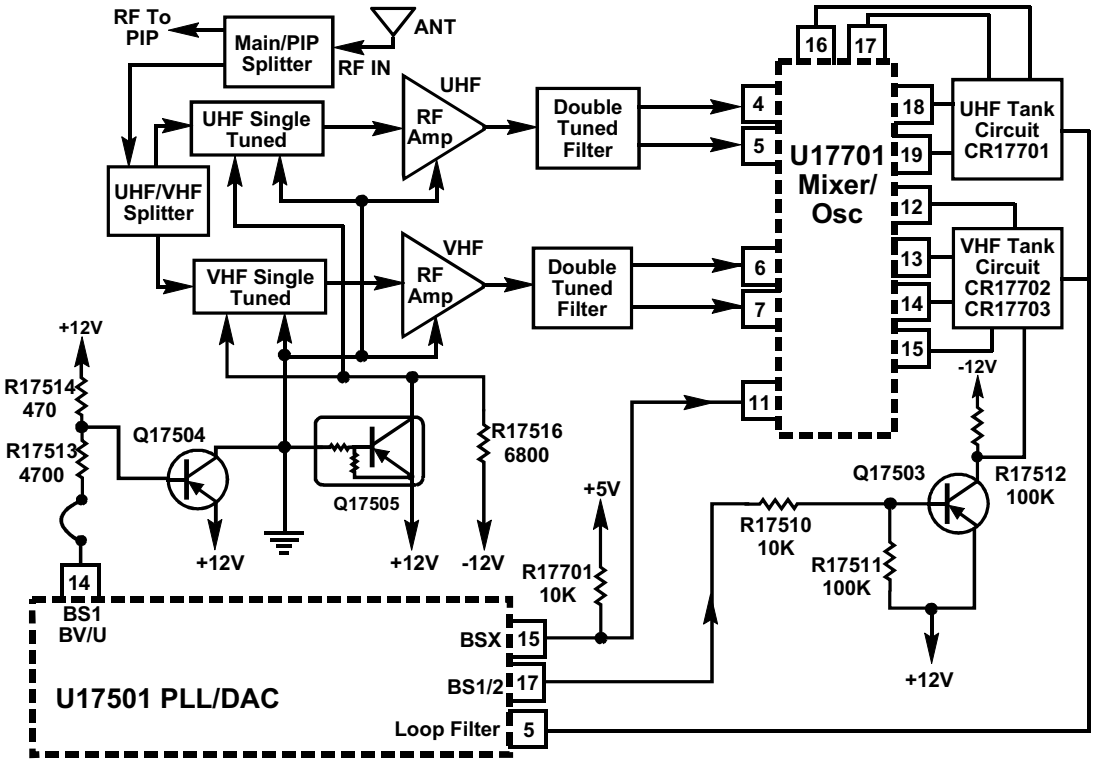


Figure 7-11, Band Switch Circuits

Channel Switching

Troubleshooting the channel switching circuitry is straightforward and can be accomplished by knowing the tuner voltages present during any channel selection. A DVM (Digital VoltMeter) is all that is required to narrow list of possible component failures.

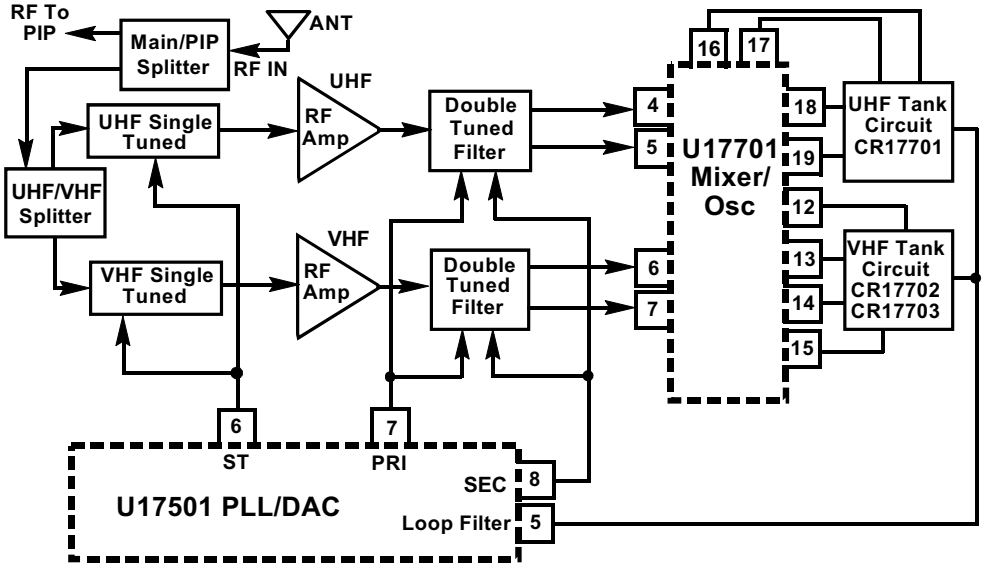


Figure 7-12, Channel Selection

PIN diodes and Varactors are used in the channel switching circuitry to shape the frequency response of the tuner. If any of these diodes fail, the circuit that has the failure will be unable to change frequency, resulting in locked or no tuning. Using a DVM, the voltages coming from pins 6, 7 and 8 of U17501, the PLL IC, should be checked first. If they are correct, follow the circuit path to the diodes. If the DC voltage disappears at any time along the path, this will most likely be the cause of the failure. In any event, the DC voltage path needs to be confirmed as operational before any RF troubleshooting should be attempted. In most cases, component failure, resulting in the loss of one or more DC voltages will be found. Capacitive diodes and varactors for the CTC195/197 are normally replaced as a matched set. Consult the service material for the chassis version for the latest information.

No Tuning

The technician must further investigate a no tuning complaint before beginning troubleshooting efforts to the component level. The following steps should assist in those efforts.

1. Verify the on-screen display shows the channel change. If it does not, the problem lies with system control, not the tuner.
2. There are four power supply voltages to the tuner. These are +12V, -12V, +33V and +5V. These should all be confirmed to be OK.
3. Check the bandswitch voltages on pins 14, 15 and 17 of the PLL IC, U17501.
4. Check the output voltages of the bandswitching transistors.
5. Check the tuning voltages on pins 6, 7 and 8 of the PLL IC, U17501. Also note that if a tuning voltage is "stuck" either high or low, there may be a problem in the PLL loop, not the IC. Check the 4 MHz oscillator signal on the capacitor side of crystal Y17501. Normal p-p voltage should be around 250 millivolts.
6. Monitor the LO voltage on pins 10 and 11 of the PLL IC. Normal operating voltage will rise as channel selection goes up and lower when channel selection goes down.
7. Check the single tuned, and the primary and secondary double-tuned filter voltages at the varactors.
8. Monitor the AGC voltage on the collector of Q32102, the ACG amplifier. Under no signal conditions, it should be around +7.5 volts. If it is not, troubleshoot the AGC path.
9. Check the supply voltage to the RF amplifiers, Q17301 and Q17101. When they are on, the supply should be 10 to 12 volts.
10. Check the IF supply voltages on the IF filter varactor diodes. The voltages should read between 1.5 to 3.0 volts.
11. The oscillator tank circuit components may be checked using continuity readings with a DVM.

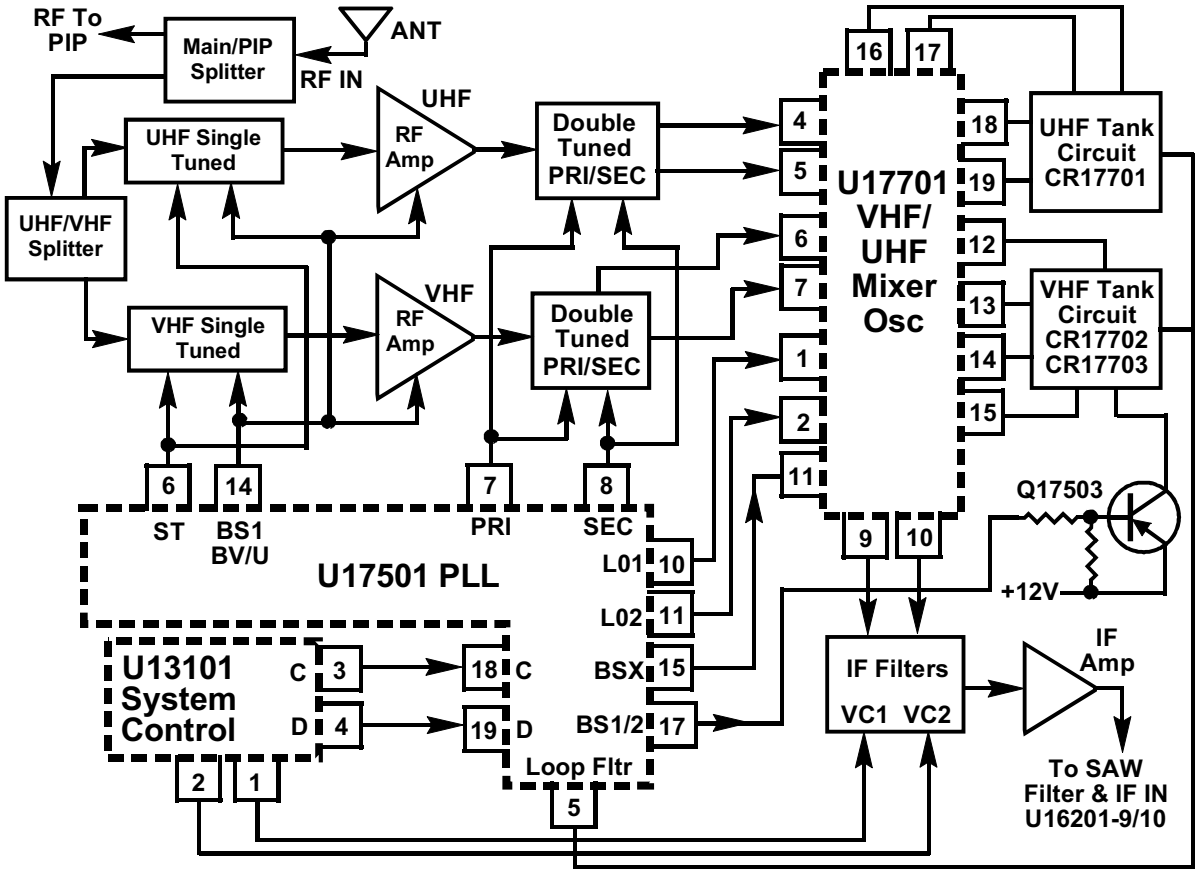


Figure 7-13 (Repeated), Tuner Block Diagram

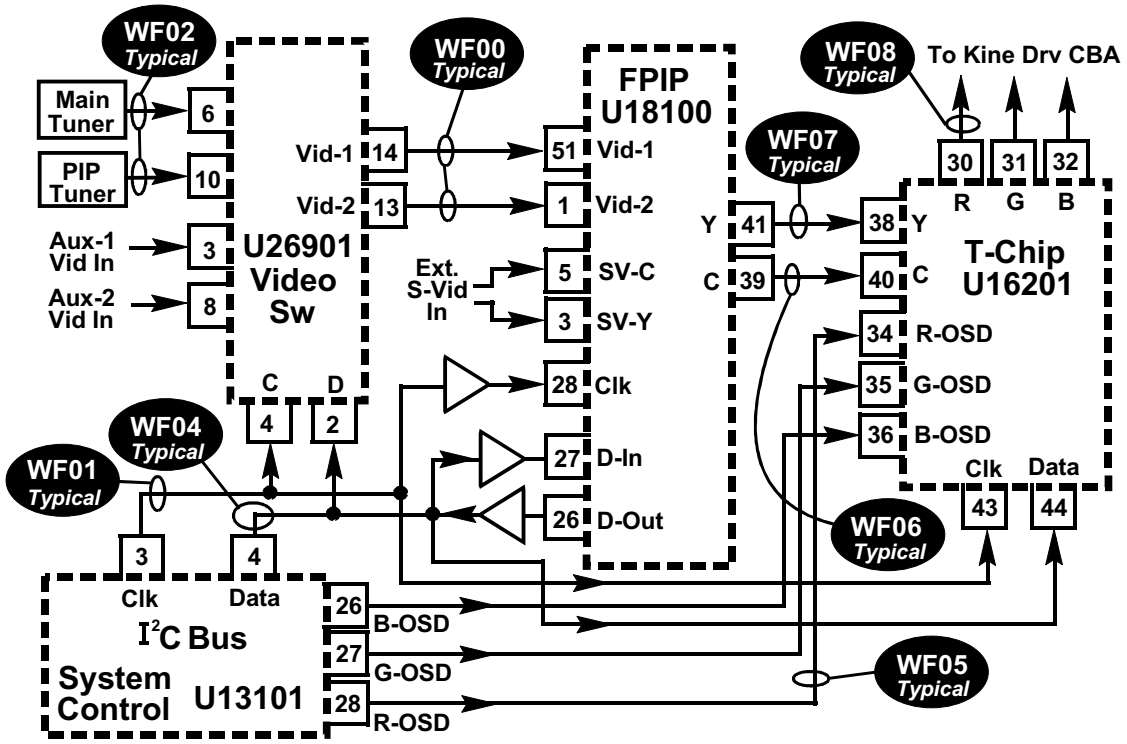


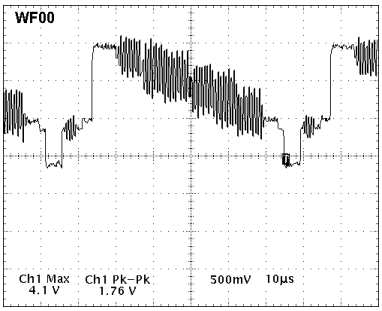
Figure 8-1, FPIP System Block Diagram

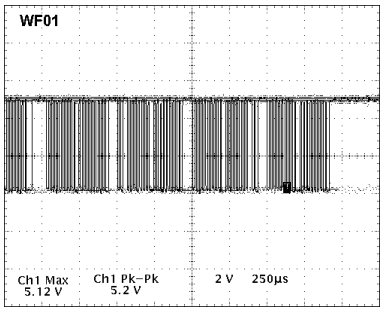
FPIP/2nd Tuner Overview

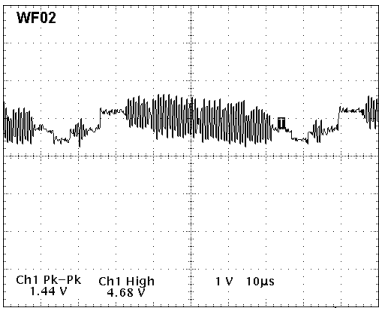
The FPIP circuitry is centered around the FPIP (*Comb* **F***ilter*/**P***ix*-**I***n*-**P***ix*) IC. This IC is designed to be a 1-chip solution for the single moving picture-in-picture function. In addition, it provides a digital comb filter for the main picture Y/C separation. The FPIP contains analog switches to select from two composite or two component (S-Video) sources from either the main picture or the small picture. The FPIP IC contains all A/D's, D/A's, burst-locked clock, analog video switching, and RAM needed to perform both the Pix-In-Pix and comb filter functions.

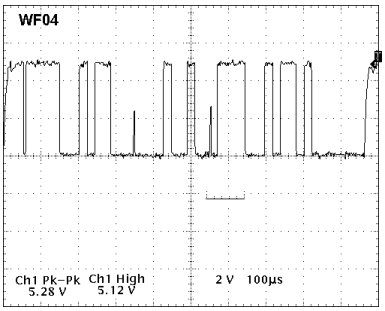
The FPIP IC can generate its own burst for timing references, if only a luma signal is available. The PIP picture is cropped by 15% instead of compressed as in previous PIP modules.

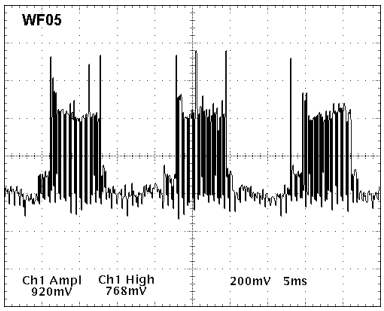
The design of the FPIP IC is intended to keep external components to a minimum. All inputs are designed to accept industry standard 1 volt (p-p) video sources (a 20% overhead is allowed), and all outputs are designed to provide industry standard 1 volt outputs.

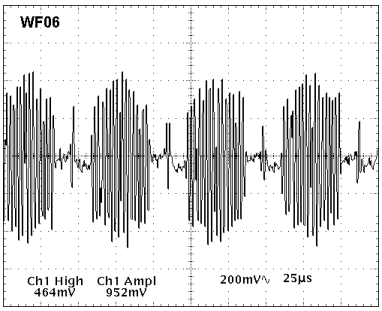


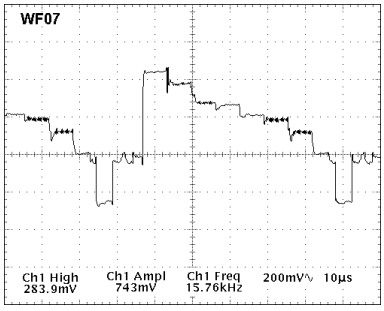


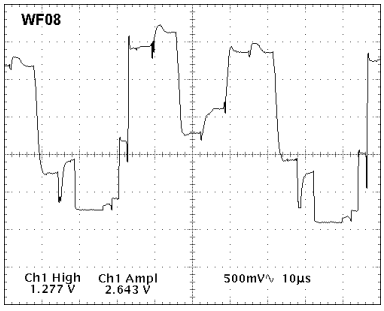












In the following discussions, the larger on-screen picture will be referred to as the "main" picture and the small window will be referred to as the "PIP" picture. The main tuner will always be responsible for the main picture, while the PIP tuner will always be responsible for the PIP window. If the two pictures are swapped, the main tuner will retune to the PIP channel selection for the large screen presentation and the PIP tuner will retune to the prior large screen channel selection and present it in the PIP window.

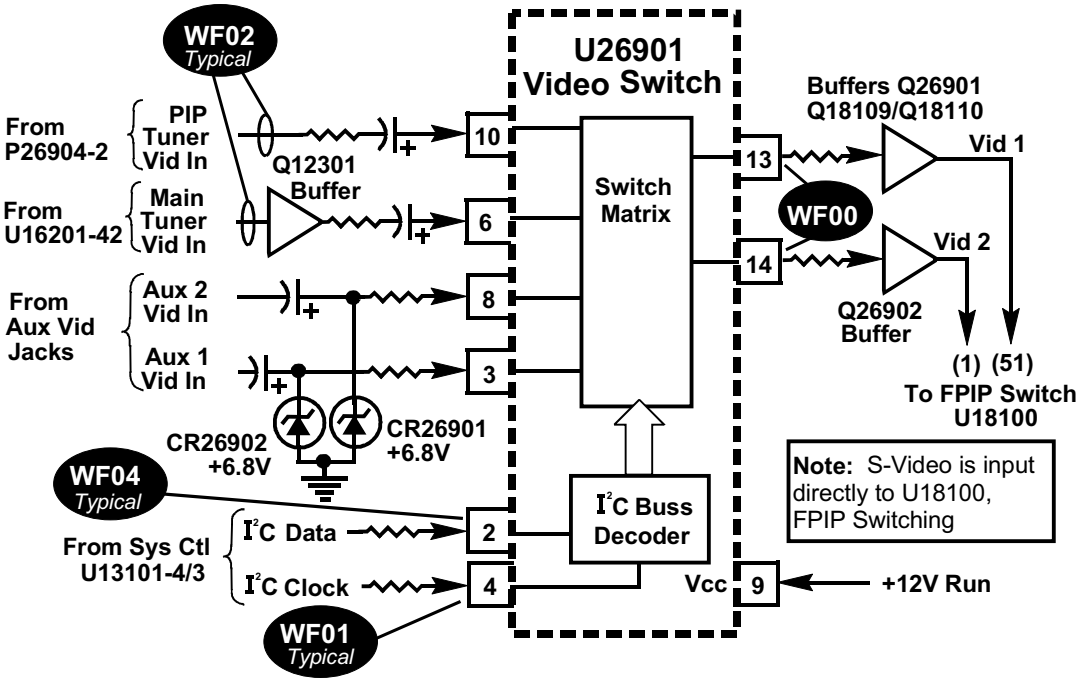
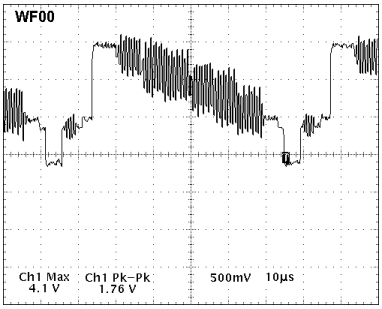
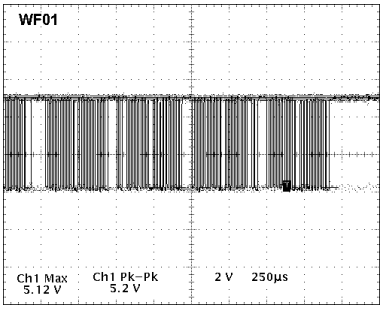
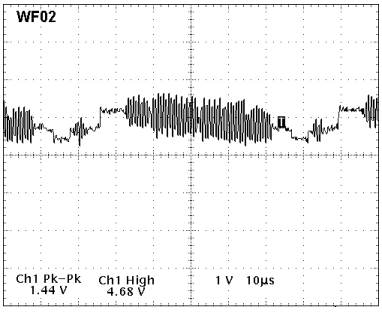
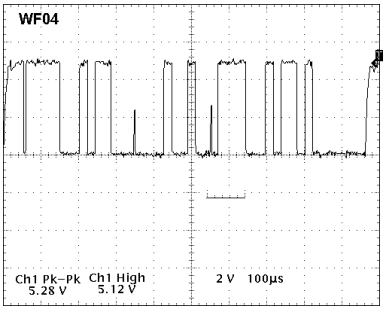


Figure 8-2, Video Input Switching





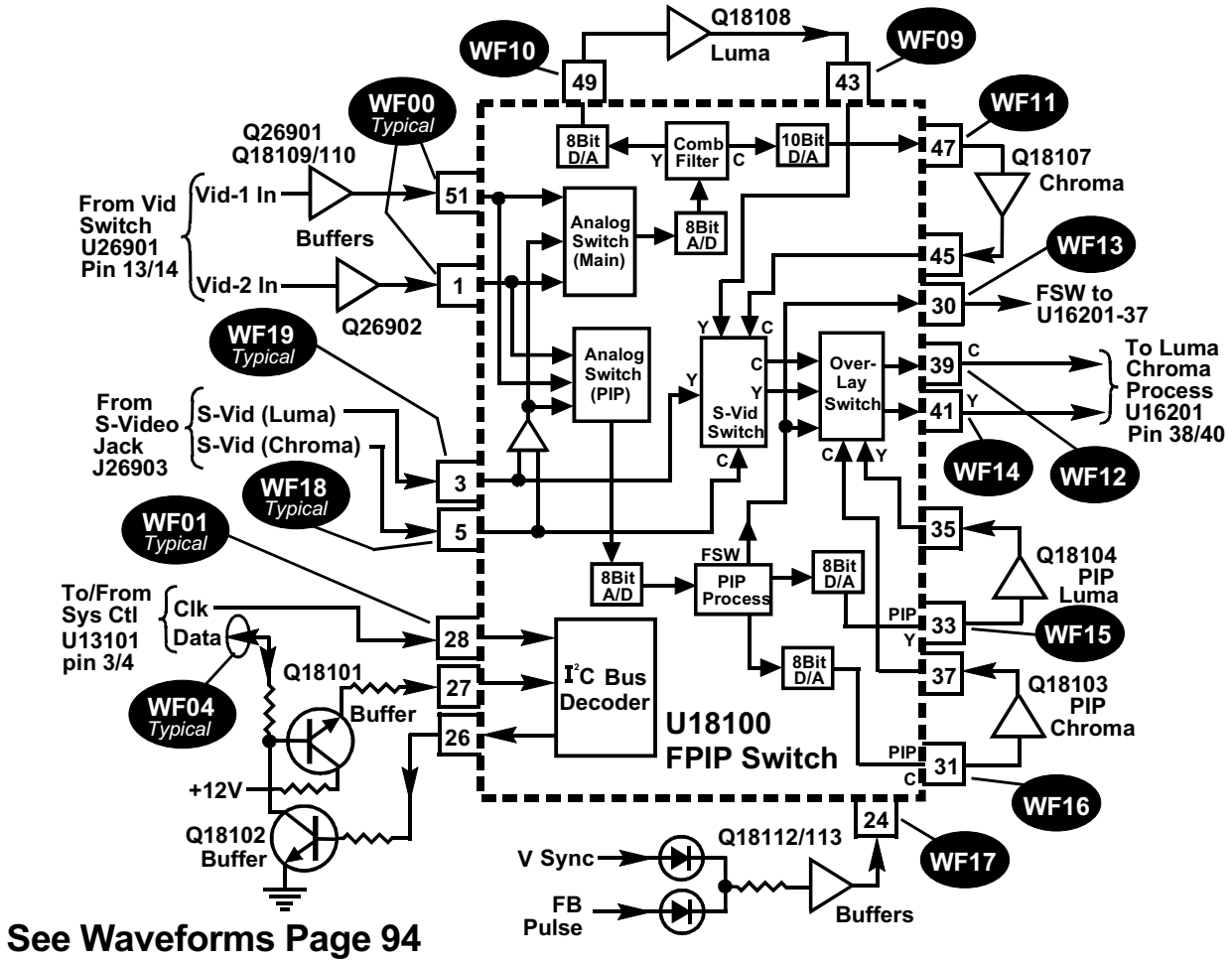




Video Input Switching

Video input switching is accomplished via two integrated circuits. These are the FPIP/Video Switching IC, U18100 and the Video Switch IC, U26901. The video switch can have a maximum of eight inputs and six outputs. Only four inputs are used; PIP Tuner Video at pin 10, Main Tuner Video at pin 6 and Aux 1 and Aux 2 at pins 3 and 8 respectively. Only two of the six outputs are currently used. Any of the four inputs may be routed to either, or both of the outputs.

Zener diodes are attached to the aux inputs at pins 3 and 8 to prevent excessive video input levels from damaging the IC. The internal switching matrix is controlled via the I^2C bus from the System Control Microprocessor, U13101, pins 3 and 4. The two selected outputs exit the IC at pins 13 and 14. The composite video outputs are buffered before they are applied to the FPIP Switching IC, U18100, at pins 1 and 51. Although discussed later, it should be noted that the Video Switch IC has no provisions for direct S-Video inputs. The S-Video signals are input directly to the FPIP IC, U18100.



See Waveforms Page 94

Figure 8-3, FPIP Switching IC U18100

FPIP (U18100) Overview

The FPIP IC accomplishes most of the operation of the Pix-in-Pix function of the CTC195/197. The FPIP contains analog switches, (to perform the swap and overlay functions), A/D's (Analog-to-Digital converters), D/A's (Digital-to-Analog Converters), a crystal clock, and digital circuits necessary to process and control the small overlay picture.

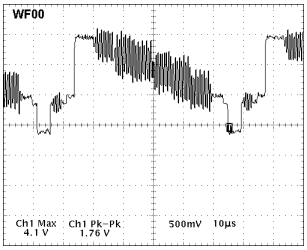
The FPIP is divided into several sections; the PIP processor, clock, comb, analog and I^2C bus sections. The PIP Processor section includes the decode, encode and field RAM subsections. The decode subsection takes a composite video waveform and decodes it to Y, R-Y and B-Y for storage into the internal field memory. The encode subsection which takes information stored in the internal field memory and encodes chroma onto it, then outputs separate Y/C small picture signals which can be combined to form a composite video signal for overlaying onto the main composite video signal. The Burst Locked Clock section generates the clock signal for the system. The BLC is locked to the color subcarrier of the main composite video signal. The analog section converts between the analog and digital domain and performs video switching functions. The bus section controls the FPIP functionality. Registers which hold control information are distributed throughout the IC.

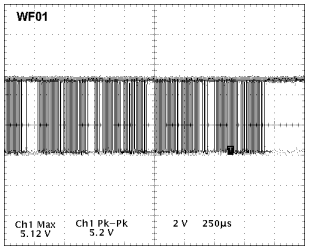
FPIP Signal Switching

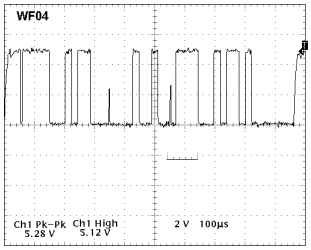
The FPIP IC serves as the center of the video switching circuits. The two selected composite video signals from switching IC U26901 are input at pins 1 and 51(WF00) after buffering. S-Video is input directly into U18100 at pins 3 (luma, WF19) and pin 5 (chroma, WF18). Once inside the IC, the S-Video luma and chroma signal are combined to form a third composite signal. The three composite video input signals are applied to two analog switch circuits within the IC. One is the “Main” picture analog switch and the other is the “PIP” picture analog switch. The outputs of both analog switches are applied to 8 bit A/D (analog-to-digital) converters. The uncombined S-Video input is applied to an S-Video switch.

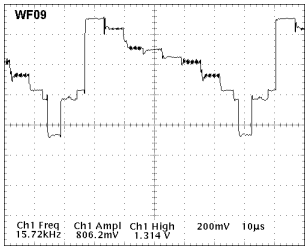
The output of the analog switch processing the "main" signal is applied to an A/D converter producing an 8 bit digital representation of the composite signal. From here, the digital comb filter separates the luma and chroma information. After main picture digital video is separated by the comb filter, the digital luma and chroma signals are converted back to analog signals by an 8 bit (luma) and a 10 bit (chroma) D/A converter. The luma signal then exits the IC at pin 49 (WF10), is buffered by Q18108, and reenters the IC at pin 43 (WF09) where it is applied to the S-Video switch. The selected main chroma signal exits the IC at pin 47 (WF11) for buffering and amplification and reenters at pin 45 and is also applied to the S-Video switch.

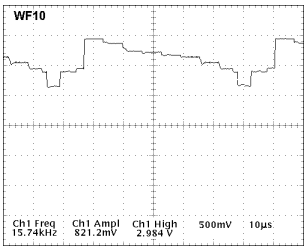
The output of the PIP analog switch is also digitized and applied to a PIP processing circuit that separates the luma and chroma signals and also a "Fast-Switch" signal derived from the sync. The separate PIP luma and chroma signals are both converted back to analog via two D/A converters. The analog PIP luma signal then exits the IC at pin 33 (WF15), is buffered and reenters the IC at pin 35. The PIP luma is then applied to the “Over-Lay” switch. The PIP chroma signal exits at pin 31 (WF16), is buffered and reenters at pin 37. The PIP chroma signal is also applied to the overlay switch. Remember the output of the Main Analog switch is processed by the digital comb filter and always serves as the main picture except in the event that the S-Video signal is selected as the main picture by the S-Video switch. The function of the S-Video switch is to select between the output from the Main Analog switch and the S-Video input at pins 3 and 5. The output of the S-Video switch always serves as the Main picture video and is applied to the Overlay Switch. The PIP picture Y/C signals are also applied to the Overlay switch. The Overlay switch combines the analog luma and chroma (Y/C) signals of both the main pix and the PIP pix with the PIP signal overlaid on top of the main picture. This signal is then output at pins 39 (luma, WF12) and 41 (chroma, WF14) where they are sent to the T4 Chip, U16201, pins 38 and 40 for further processing.

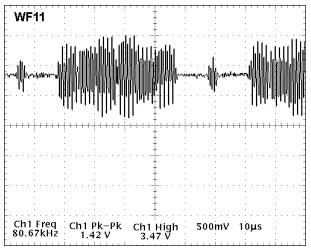


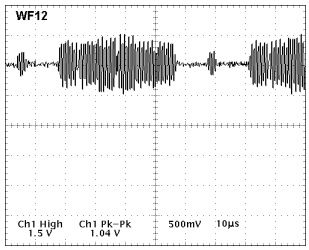


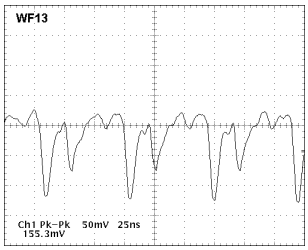


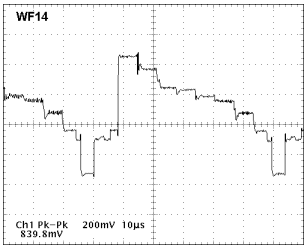


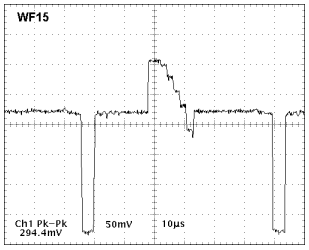


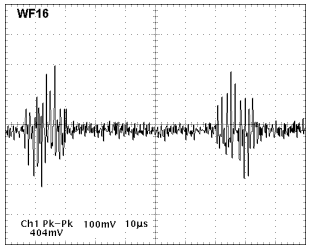


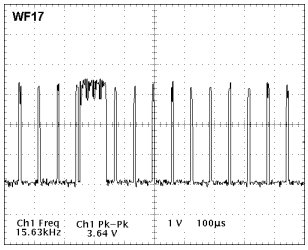


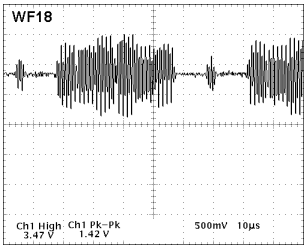


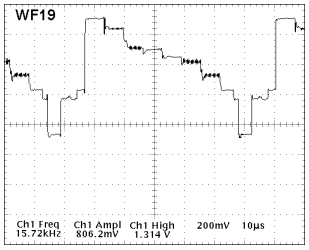












The FPIP Switch, U18100, is controlled via the I^2C bus. However, the data line from the microcomputer to IC U18100 is a two-way data communications line. The data going *to* the IC (function and control information) is buffered by Q18101 and input into pin 27 (WF04). The data coming out of the IC (status information) exits the IC at pin 26 and is buffered by Q18102 before its sent back to the System Control Microcomputer U13101. The I^2C bus decoder in U18100 is responsible for controlling all the switching circuits inside the IC according to instructions from system control. For internal synchronization and switching purposes, a vertical sync signal and a horizontal signal are combined and input at pin 24 (WF17) of the IC.

The PIP signal is sampled using a 4fc (Four times the clock frequency) clock locked to the main picture burst. In order to avoid line to line jitter of the small picture overlaid onto the main picture, the display of the small picture must be done using a 4fc clock that is phase locked to the horizontal sync pulse of the display. While these two clock signals have the same frequency, the phase of the two signals will be asynchronous with respect to each other. The purpose of this circuit is to re-time the output samples. Internally, FPIP does as much processing as possible using the input (or burst-locked) clock. The PIP luma output D/A converter is clocked by the output (or line-locked) clock. This circuit insures that data presented to the input of the PIP luma D/A will not have distortion during the active video portion of the display. A Vertical Peaking circuit takes the low pass filtered line difference signal (vertical detail) and processes it through a nonlinear processing block and a gain stage. The gain is bus controllable (1, 0.75, 0.5, 0.25 and OFF). Vertical Peaking Gain is set to zero during vertical to preserve Closed Captioned information.

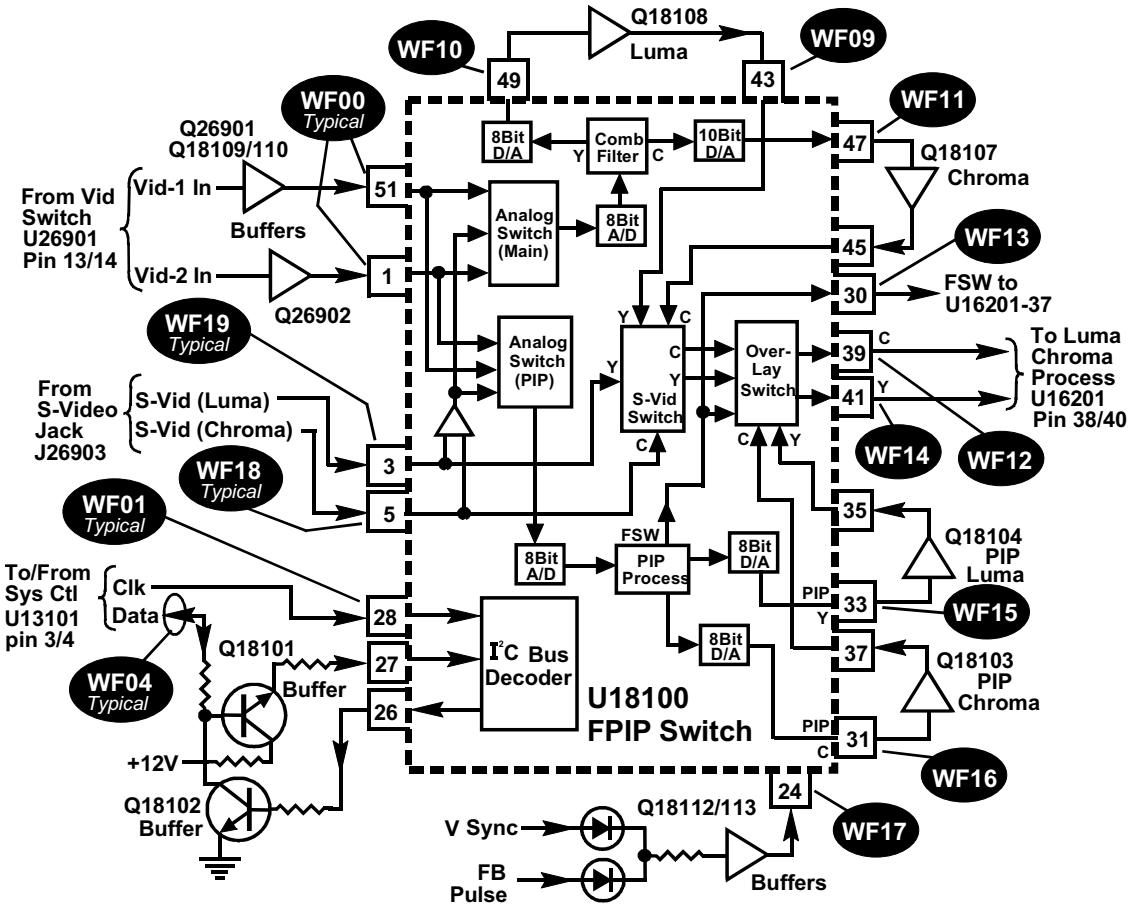
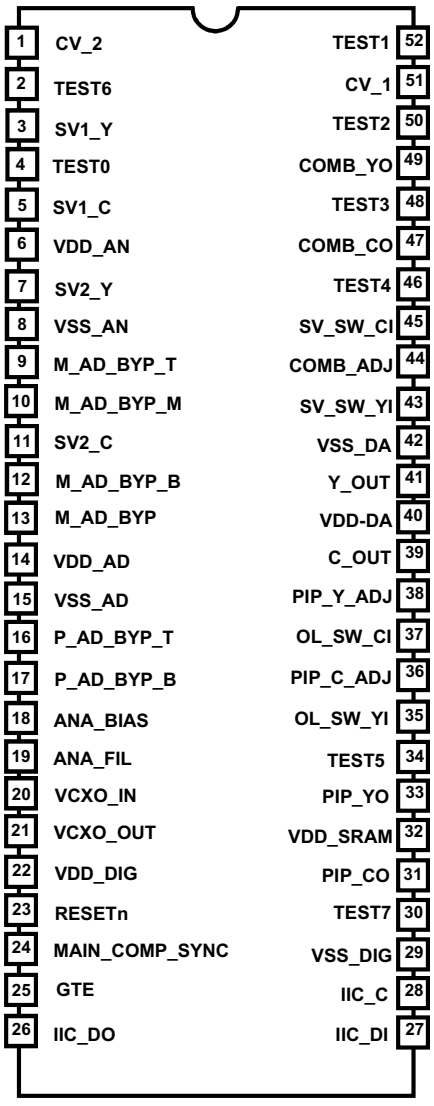


Figure 8-3, (Repeated) FPIP Switching IC U18100

FPIP IC U18100 Pinout

The next pages contain a complete pin out diagram of the FPIP IC and descriptions for the pin functions.



FPIP IC Pinouts

Pin Descriptions

1 CV_2 One of the four Composite Video inputs available as a source for either the Main Picture or the PIP Picture

2 TEST 6 (Manufacturing Use Only)

3 SV1_Y One of the two S-Video Luminance inputs available as a source of Luminance for either the Main Picture or the PIP Picture

4 TEST 0 (Manufacturing Use Only)

5 SV1_C One of the two S-Video Chrominance inputs available as a source of Chrominance for either the Main Picture or the PIP Picture

6 VDD_AN Supply voltage, all analog blocks (except A/Ds D/As and VCXO)

7 SV2_Y One of the two S-Video Luminance inputs available as a source of Luminance for either the Main Picture or the PIP Picture

8 VSS_AN Ground reference for pin 6, analog

9 M_AD_BYP_T Pin for bypass capacitor for Main Picture A/D.

10 M_AD_BYP_M Pin for bypass capacitor for Main Picture A/D.

11 SV2_C One of the two S-Video Chrominance inputs available as a source of Chrominance for either the Main Picture or the PIP Picture

12 M_AD_BYP_B Pin for bypass capacitor for Main Picture A/D.

13 M_AD_BYP Pin for bypass capacitor for Main Picture A/D.

14 VDD_AD Supply voltage, analog (A/Ds and VCXO)

15 VSS_AD Ground reference for pin 14, analog

16 P_AD_BYP_T Pin for bypass capacitor for PIP A/D.

17 P_AD_BYP_B Pin for bypass capacitor for PIP A/D.

18 ANA_BIAS Clock Generator Bias

19 ANA_FIL Clock Generator Bias Filter

20 VCXO_IN Timing Crystal Input

21 VCXO_OUT Timing Crystal Output

22 VDD_DIG Supply voltage, digital

23 RESETn Power-On Reset (active low)

24 MAIN_COMP_SYNC Composite Sync Input

25 GTE Global Test Enable (Not used)

26 IIC_DO I^2C bus data output

27 IIC_DI I^2C bus data input

28 IIC_C I^2C bus clock

29 VSS_DIG Ground reference, digital

30 TEST 7 (Manufacturing Use Only)

31 PIP_CO **PIP** Small Picture Chrominance

32 VDD_SRAM Supply voltage, digital

33 PIP_YO **PIP** Small Picture Luminance

34 TEST5 (Manufacturing Use Only)

35 OL_SW_YI Overlay switch Y input

36 PIP_C_ADJ Pin for bypass capacitor for PIP Chrominance D/A Adjust D/A.

37 OL_SW_CI Overlay switch C input

38 PIP_Y_ADJ Pin for bypass capacitor for PIP Luminance D/A Adjust D/A.

39 C_OUT Main Picture Chrominance with PIP Picture Chrominance overlay output

40 VDD_DA Supply voltage, analog (D/As and Sub-D/As)

41 Y_OUT Main Picture Luminance with PIP Picture Luminance overlay output

42 VSS_DA Ground reference for pin 40, analog

43 SV_SW_YI S-Video switch Y input

44 COMB_ADJ Pin for bypass capacitor for Comb D/A Adjust D/A. There is one adjustment D/A for two Comb output D/A's.

45 SV_SW_CI S-Video switch C input

46 TEST 4 (Manufacturing Use Only)

47 COMB_CO Digital Line Comb Main Picture Chrominance Output

48 TEST 3 (Manufacturing Use Only)

49 COMB_YO Digital Line Comb Main Picture Luminance Output

50 TEST 2 (Manufacturing Use Only)

51 CV_1 One of the four Composite Video inputs available as a source for either the Main Picture or the PIP Picture

52 TEST 1 (Manufacturing Use Only)

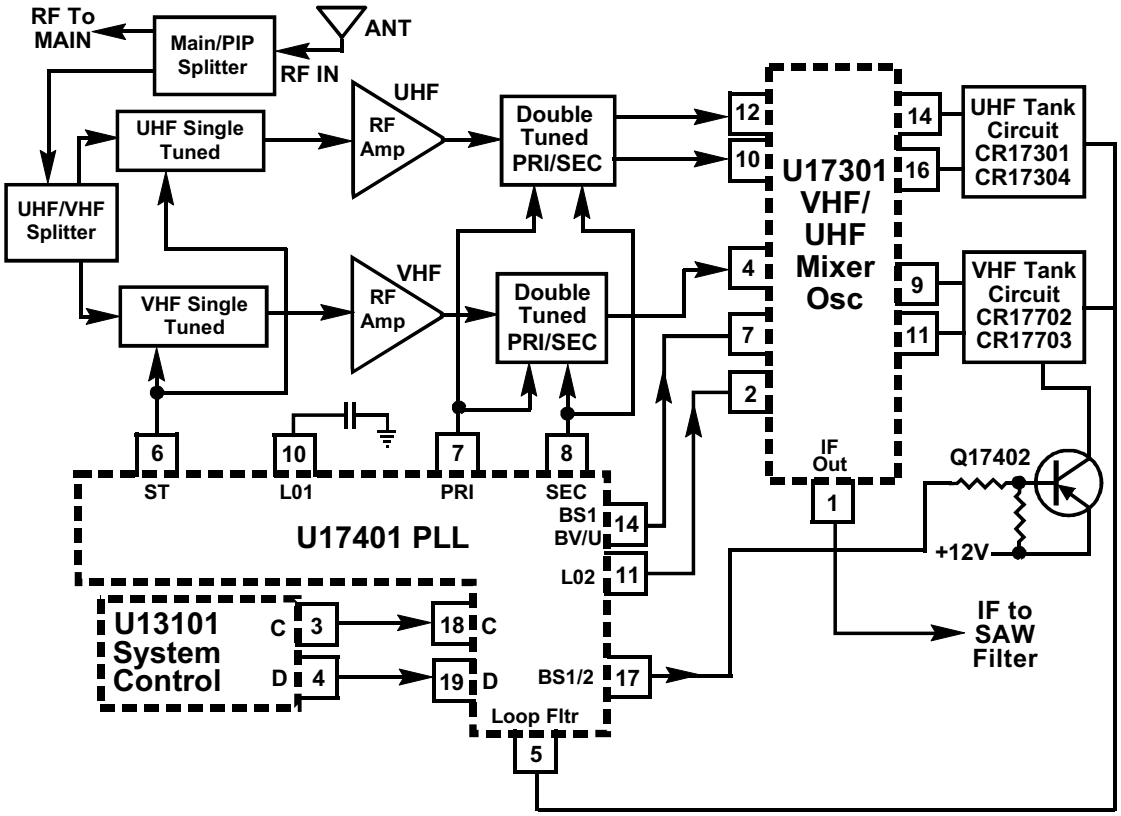


Figure 8-4 , Second Tuner

Second Tuner (PIP)

The second tuner, known as the PIP tuner, is very similar to the main tuner in the CTC195 chassis. All functionality is identical to the main tuner. There is a separate PIP EEPROM for the values required by the PIP tuner, IF and window alignments. The tuner is capable of receiving off-air channels 2–69 and cable channels 01–125.

One difference is the front end of the tuner. Instead of dual control of the single-tuned RF stage, the PIP tuner only has single control. Many of the input or output lines are single-ended where the main tuner uses balanced lines. This means one side of the signal is at ground potential. This makes signal transfers between the PIP module and main chassis less prone to interference. The tank circuits on the VHF and UHF outputs are also not as selective as the main tuner. In general, the picture quality needed in the PIP window is not as great as that needed in the main window. That is why the main window is always controlled by the main tuner. If the PIP and main windows are swapped, the two tuners are retuned so that the PIP channel desired by the user, is tuned by the main tuner and placed in the main window. The channel that was in the main window is tuned by the PIP tuner and placed in the PIP window.

All alignments and troubleshooting efforts of the PIP Tuner are the same as for the main tuner. The tuning bands are the same. The only differences are the alignment channels. Figure 8-5 shows the table of alignment channels.

Channel	Band	Midrange (MHz)	Pix Carrier (MHz)	Local Oscillator (MHz)
2	1	57	55.25	101
6	1	85	83.25	129
98	1	111	109.25	155
15	1	129	127.25	173
17	1	141	139.25	185
18	2	147	145.25	191
9	2	189	187.25	233
29	2	255	253.25	299
39	2	315	313.25	359
46	2	357	355.25	401
50	2	381	379.25	425
51	3	387	385.25	431
61	3	447	445.25	491
75	3	531	529.25	575
101	3	657	655.25	701
114	3	735	733.25	779
122	3	783	781.25	827
125	3	801	799.25	845

Figure 8-5, Second Tuner Alignment Channels

PIP 2nd Tuner/IF

Figure 8-6 is a block diagram of the PIP system with waveforms that may assist in troubleshooting efforts. All waveforms were taken with a standard color bar input.

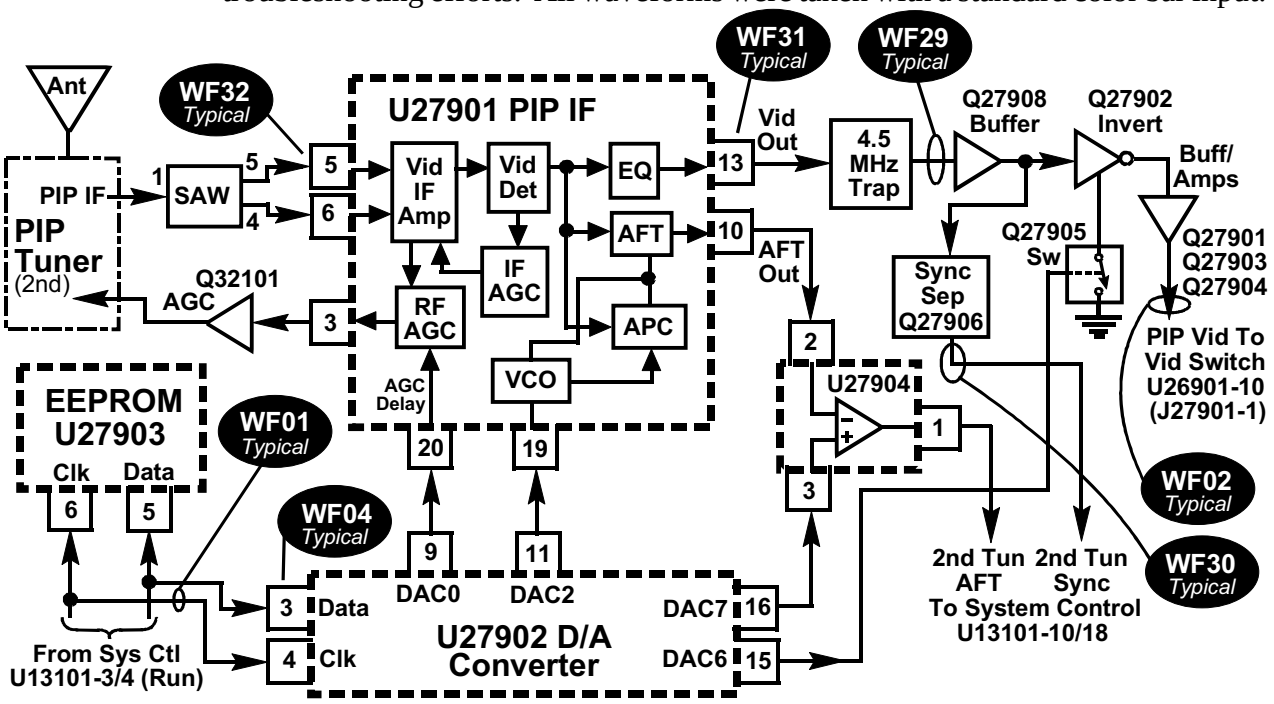
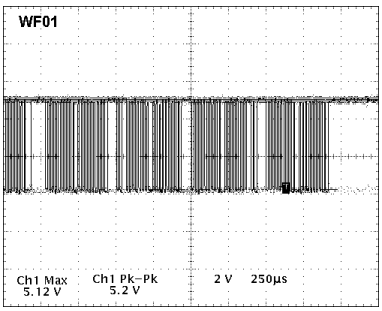
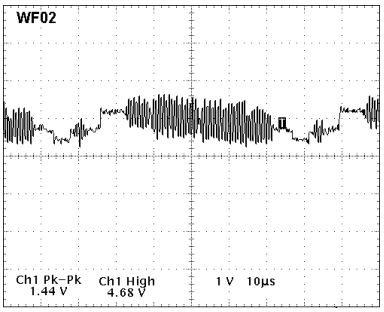
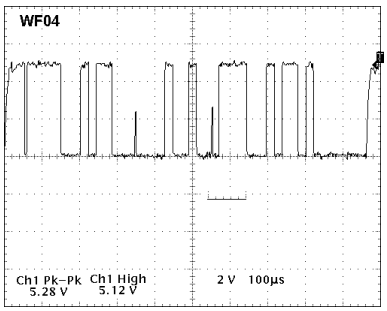
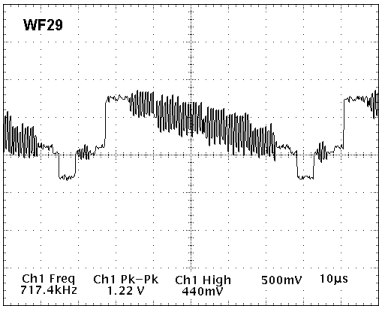


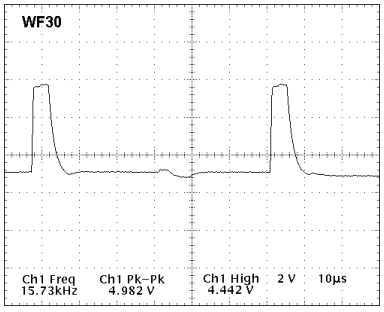
Figure 8-6 , 2nd Tuner/PIP IF Block Diagram

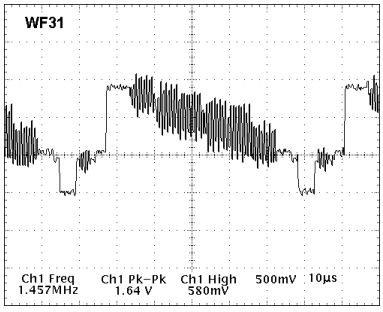


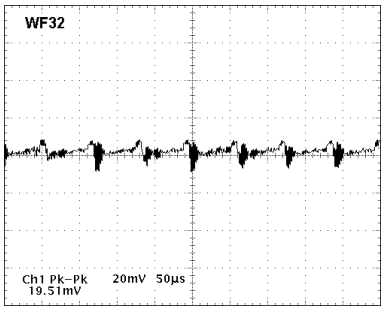












T4 Chip U16201

T-Chip Overview

The CTC197 chassis uses the latest in a series of television specific "one-chip" IC's designed to perform most low level signal processing in a television chassis. It is very similar to the CTC185 T-Chip. The T4 Chip is compatible with the Philips Inter IC (I^2C) bi-directional 2-wire serial data communications bus. Low level signal processing including; IF, audio detection, video processing, CRT management and deflection processing, are performed by the T4 and controlled by the microprocessor via the I^2C bus. IF, audio detection and deflection processing are discussed in other chapters. This chapter will focus on the bus structure and video processing performed by the T4.

T4 Chip Bus Specifics

This section is a general overview of the I^2C bus standard and not intended to be a detailed description. Within the I^2C bus definition, the T4 Chip is considered to be a slave-only device. This is because the IC cannot initiate a data transaction and can only respond to commands from an I^2C bus master device such as the chassis micro. The T4 Chip bus transceiver supports only one write mode and one read mode.

POR (Power-On Reset) Operation

The T4 Chip includes a standby power supply monitor referred to as the POR. This circuit detects when the Standby Vcc voltage has dropped below the normal range and shuts the IC off by stopping the horizontal output. The output of the POR circuit is available to the micro for status control. The POR circuit output is latched and will reset only with an OFF to ON transition of the ON/OFF bit. This means that when a television is ON and a Standby Vcc transient occurs, triggering the POR circuit, it is necessary to send an OFF command, followed by an ON command in order to get the set started again. If the Standby Vcc is still too low when an ON command is received, the IC will stay in the OFF mode and the process must be repeated.

Bus Transceiver Reset

The T4 Chip bus transceiver contains an internal reset circuit sensitive to the Standby Vcc level. This reset circuit is separate from the IC's Power-On-Reset (POR) circuit and is designed to keep bus communications active at Standby Vcc levels that may be lower than normal. POR occurs at 6.3 volts while the bus transceiver will remain operational to Standby Vcc levels as low as 2.5 volts. When a bus transceiver reset is detected the circuit enters an idle mode in which SDA (Data Bus) is left high and bus communications are ignored. When the Standby Vcc is lower than normal but above 2.5 volts, the bus transceiver will remain operational. However, the saturation voltage of the SDA line is not guaranteed. Both the SDA and the SCL (Bus Clock) lines are internally clamped to Standby Vcc via protection diodes.

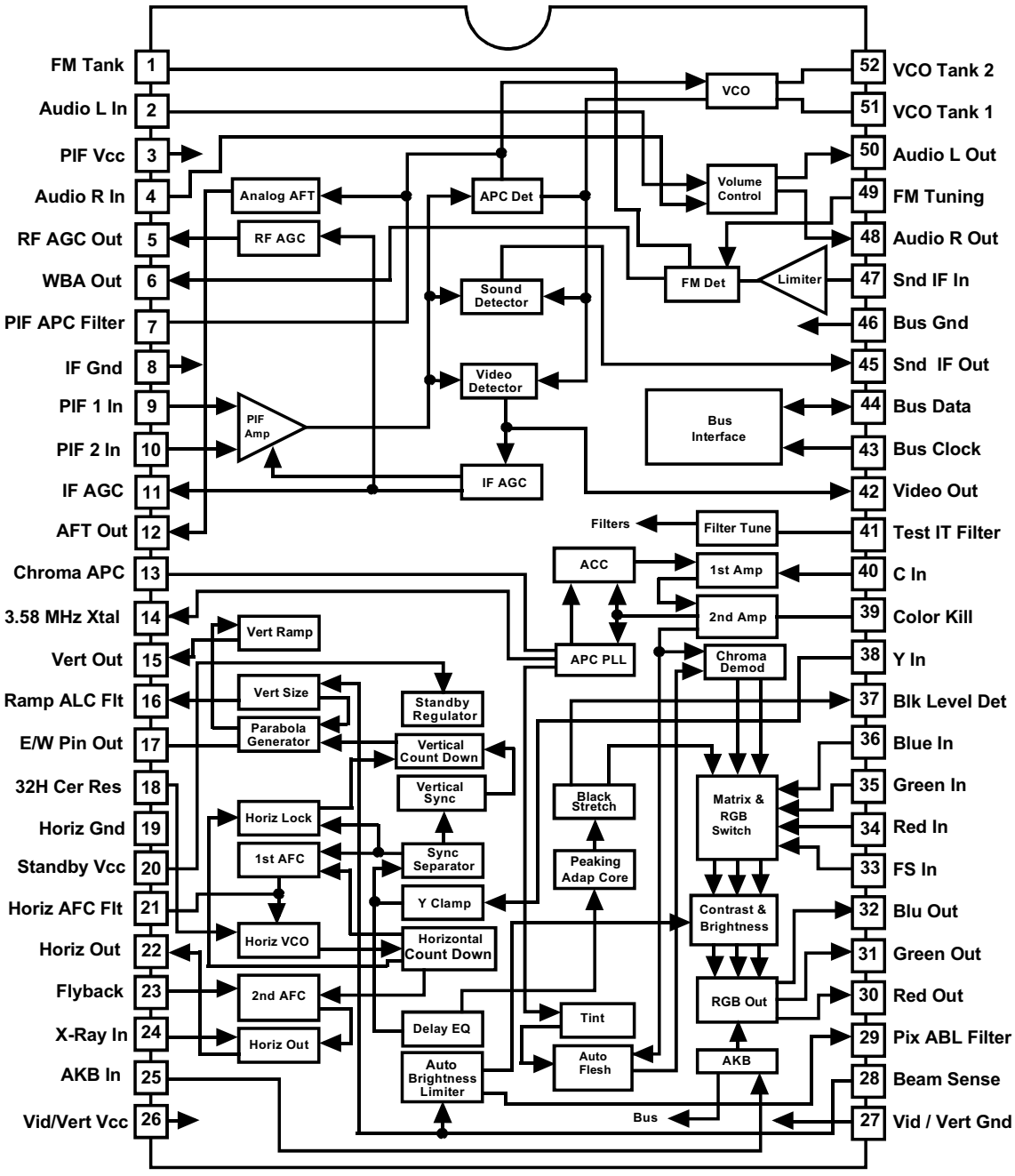


Figure 10-1, T-Chip Block Diagram

Transceiver Power Supply and Register Volatility

Each register is powered by the same Vcc as the circuit it serves. For example, the registers controlling the vertical ramp are powered by the Vid/Vert Vcc. This means that each register must be refreshed if its Vcc drops below the normal operating range. The only registers with guaranteed power-up values are Video Mute and Audio Mute.

IF Processing

The T4 Chip accepts an IF signal from the tuner circuitry and provides all the processing required to separate the signal into the component luma and chroma signals, then output a standard NTSC baseband video signal. Also provided is an AGC voltage for signal level control. See the section on tuner/IF for more information.

Audio Detection

The sound IF signal is input to the T4 where it is first level limited, then detected. Finally the wide band audio signal is sent to the Stereo Decoder chip for final processing.

CRT Management

AKB, XRay Protection, E-W correction and Beam Limiting are all integral circuitry within the T4. All are discussed elsewhere in this manual.

Deflection Processing

All low level vertical and horizontal deflection signal processing and control and all sync signal processing is performed within the T4 Chip. See the section on Deflection for more information.

Video Processing

The video processing circuitry in the T4 Chip is responsible for receiving video signals from the FPIP/Switch and allowing either user or technician control of the shape of the waveforms exiting to other processing circuits or the CRT. Video processing includes brightness, color, tint, contrast and sharpness. All alignments performed by the T4 Chip are controlled by the microprocessor via the I^2C bus.

Video Processing

The video section of the CTC197 is composed of 4 main areas; luma processing, chroma processing, external RGB inputs, and RGB outputs. With only a few exceptions, all circuitry for these functions is contained in the T4 Chip.

The video processing of the CTC197 chassis is similar to the processing in the prior CTC185 chassis. Both chassis use the T4 generation T-chip for IF, audio detection, video processing, and deflection processing. As has been discussed earlier, the T4 chip is an I^2C bus controlled IC.

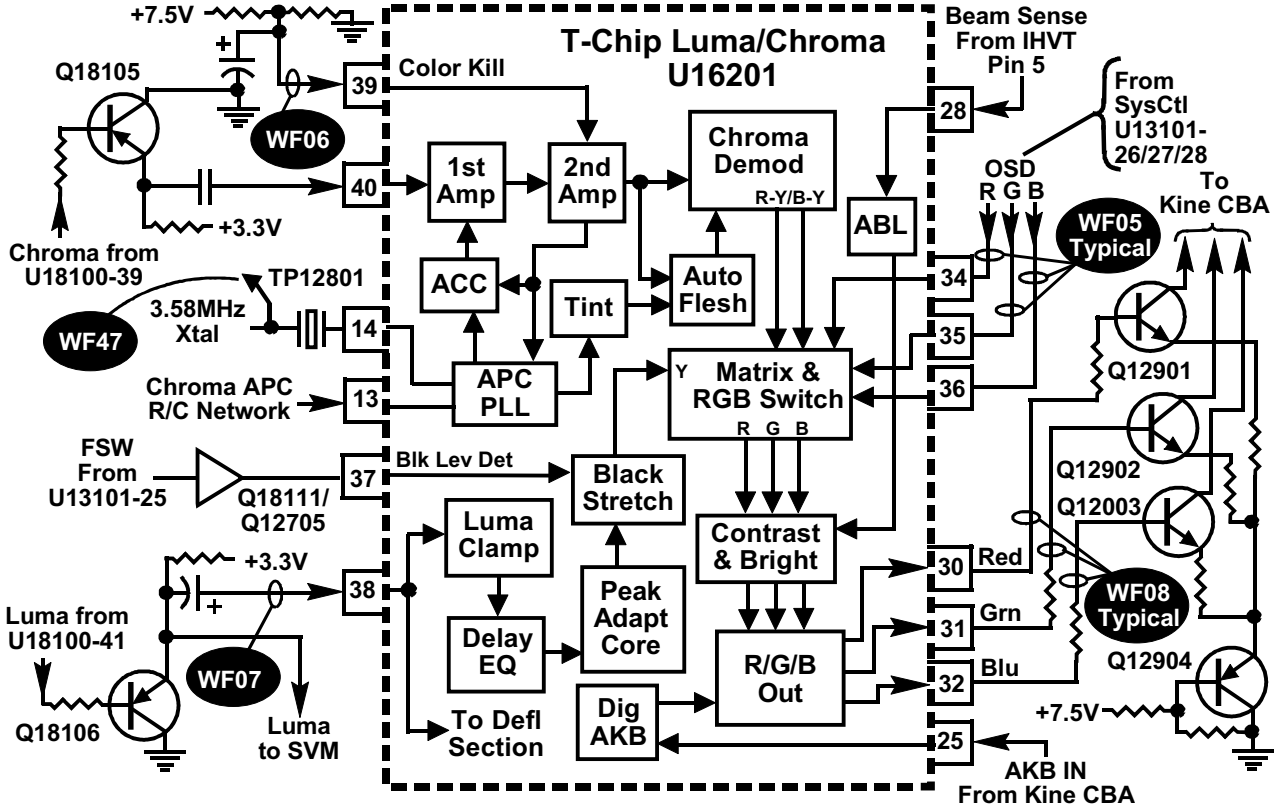
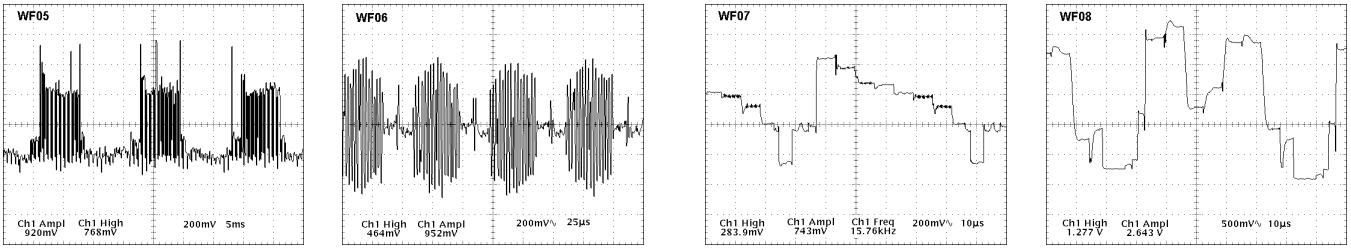
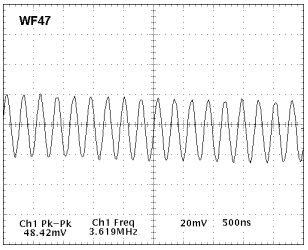


Figure 10-1, Video Processing





Video Processing Waveforms

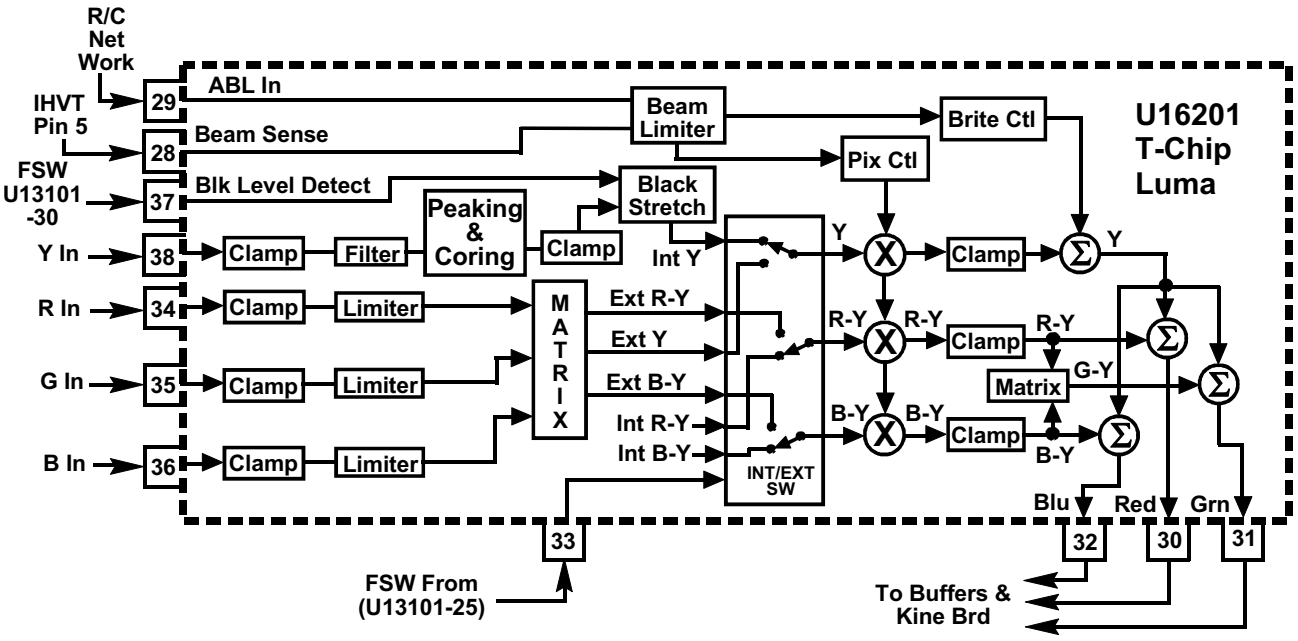


Figure 10-2, Luminance Processing

Luma Processing

The luminance section video input is applied to pin 38, (WF07) from an input buffer, Q18106, and a clamp capacitor. The input is approximately 1 volt p-p to assure the input filter can operate linearly. Too much signal would send the filter into an area where the nonlinear characteristics would make the output slightly unpredictable. The filter section is bus controlled and can be switched between a 3.58 MHz notch (used when no external Y/C separation is available), 4.2 MHz notch, and an 8.0 MHz all pass filter, selected when Y/C separation is provided prior to the T4 chip. Because the CTC197 uses the FPIP IC, which includes a digital comb filter, the 8 MHz all pass filter is normally used. This provides attenuation above 8 MHz, but does not affect luminance in the chroma carrier frequency region. Using this filter, the chassis is capable of a 0–7.6 MHz response at the CRT cathodes when adjusted for maximum sharpness. The luma filter block includes a transversal peaking circuit, controlled via the I^2C bus. Included in this block is an adaptive core filter which operates on the peaking component only.

After filtering, the luma signal is once again clamped, and passed through the black stretch circuitry. This circuit modifies the video transfer function to enhance contrast on low APL scenes in an adaptive manner. Black stretch operates selectively on the luma levels and is disabled in the PIP window. The luminance block also includes the sharpness function, delay equalization to match luminance timing to chroma and black level clamping.

Chroma Processing

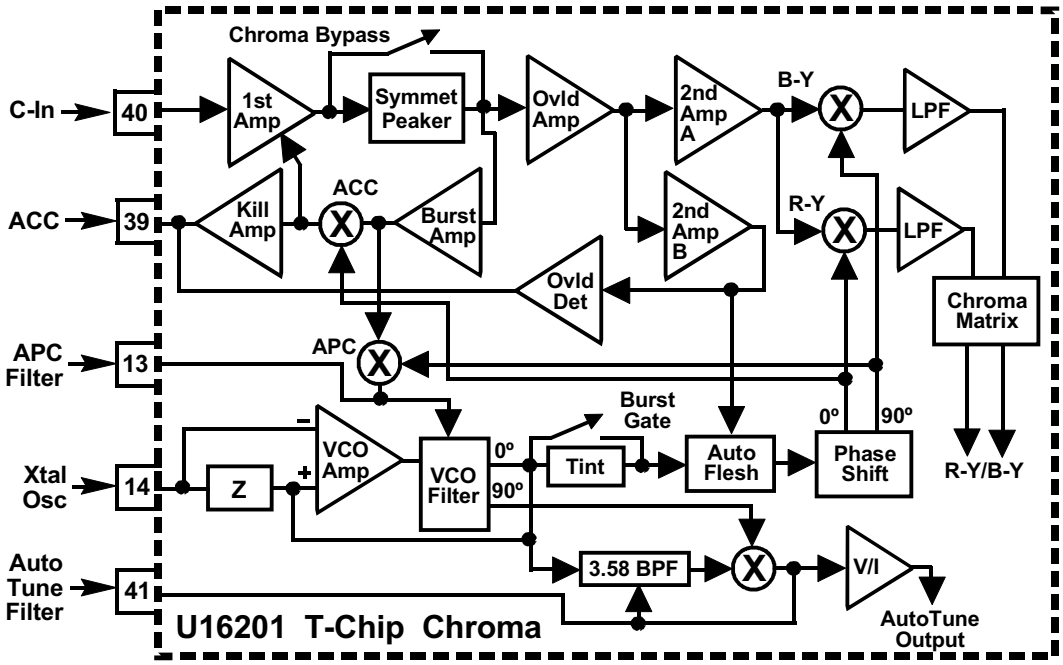
Chroma processing in the CTC197 is identical to the CTC185 except that the chroma comes separated from the luminance. This is done in the FPIP IC using a digital comb filter. The chroma section expects a signal whose amplitude is approximately 290 mVpp burst at pin 40. The chroma section includes a filter that is either a symmetrical filter (used for aux and S-video mode) or peaked (used for tuner/if operation). The filter is controlled by the I^2C bus and can be bypassed. The ACC (*A*utomatic *C*olor *C*ontrol) detector monitors burst amplitude at the output of the filter section and adjusts the 1st chroma amplifier gain to maintain a constant level. The burst signal is used as the reference.

The output of the ACC is compared to a kill threshold reference in the color killer amplifier. If the detected burst amplitude is below approximately 2.4 IRE, the killer is activated, shutting down the overload amplifier. The burst amplifier is also used to drive the ACC and APC (*A*utomatic *P*hase *C*ontrol) detectors.

From the ACC point, the filtered chroma signal is sent to an overload amp and from there to the 2nd chroma amp. The 2nd chroma amp is made up of two identical stages in parallel. The output of the "B" stage drives the chroma overload detector which controls the overload amp gain to form a low gain AGC circuit. This loop attempts to maintain the average chroma saturation within some prescribed limits. Chroma overload is enabled over the I^2C bus. Chroma saturation is applied to the 2nd chroma amp "A" stage, and from there reaches the demodulator inputs. After the demodulators, lowpass networks reduce demodulator artifacts.

The chroma VCO (*V*oltage *C*ontrolled *O*scillator) is a single pin design. The crystal oscillator inputs through pin 14 and is connected directly to the negative input of the VCO amplifier. The amplifier output passes though a tunable filter back to the positive input providing feedback. At frequencies off resonance, the positive and negative feedback components will cancel. At the resonant frequency, negative feedback will be shunted to ground. This results in a net positive feedback, sustaining oscillation. By tuning the VCO filter, frequency control is obtained.

The output of the VCO goes through a filter whose outputs are 0 degrees and 90 degrees out of phase with the input signal. The 0 degree output drives the tint control and auto flesh stages, and the 90 degree output is used to drive the auto tune section. After the tint control, the subcarrier passes through the Autoflesh processing and then to the demodulator phase shift filter. In the Autoflesh block, a phase detector compares chroma from the output of the 2nd chroma amp "B" section to the subcarrier from the tint control. When the incoming chroma phase is in the vicinity of "flesh tone" (approximately 123°, dependent on the customer tint setting), a phase correction is applied to the subcarrier to move it back towards the "flesh" setting. Autoflesh is enabled over the I^2C bus.



Chrominance Processing Block Diagram

Figure 10-3, Chroma Processing

The chroma circuitry includes an auto tune loop which is used to compensate for the effects of variations in the components of the filters. Auto tune works by making a phase comparison of the 90 degree output of the VCO and the VCO amplifier input after the 3.58 MHz bandpass filter. This will tend to tune the bandpass filter such that the center frequency is equal to the frequency of the chroma oscillator. If the resonant frequency of the bandpass is not correct, the auto tune detector sees the error and supplies a correction voltage. Additionally, the auto tune output is used to continuously tune the chroma and luminance filters.

RGB Interface

The RGB interface is a switching, level control and matrixing section. External RGB signals are clamped and de-matrixed into luma (Y), R-Y and B-Y. The external video signals are then applied to a switch. The internal Y, R-Y and B-Y signals are also applied to the switch. The switch selects either the internal or external signals depending on the voltage at the fast switch input. Any voltage above approximately 0.7 Volts will select the external RGB signals. After the switch, the selected signals go to the picture control circuits. These circuits adjust the amplitude of the Y, R-Y and B-Y signals from the switch across a range of 12dB. The Brightness Control adjusts the level of the luma (Y) signal that is mixed with the R-Y, G-Y and B-Y signals. This raises the DC level of these signals. After the picture control multipliers, the signals are clamped.

After clamping, R-Y and B-Y are matrixed to obtain G-Y, and then the three color difference signals (R-Y, G-Y & B-Y) and luminance (Y) are matrixed to obtain component R, G, and B signals.

External RGB Input Processing

The external RGB inputs are used for OSD (On Screen Display) processing for the CTC197. OSD signals from the microprocessor are applied to the external RGB inputs (pin 34, 35 & 36, typical waveform WF05) through a set of low impedance buffers and input clamp capacitors. Following the clamps are limiters set at approximately 700mVpp (corresponding to 100 IRE). In the CTC197 the input drive level will be somewhat less than this, typically in the range of 70 IRE or 500 mVpp. These external RGB signals will then be matrixed to form Ext Y, Ext R-Y, and Ext B-Y as shown if Figure 10-3.

RGB Output Section

Internal Y from the Luma section, internal R-Y and B-Y from the Chroma section, and external Y, R-Y, and B-Y from the external RGB inputs all come together in the Int/Ext Switch. The Fast Switch line, generated by the microprocessor, controls which set of signals is displayed. A low level on the Fast Switch selects the internal signals, a high level selects external.

After source selection, the pix control (picture control) adjusts the amplitude of the Y, R-Y, and B-Y signals. These are then clamped and the brightness control is applied to the Y signal. R-Y and B-Y are matrixed to form an additional signal, G-Y, and the Y component is summed with all three color difference signals to form Red, Green, and Blue component signals. These signals are output from pins 30, 31 & 32 (typical waveform WF08) to drive the kine circuitry.

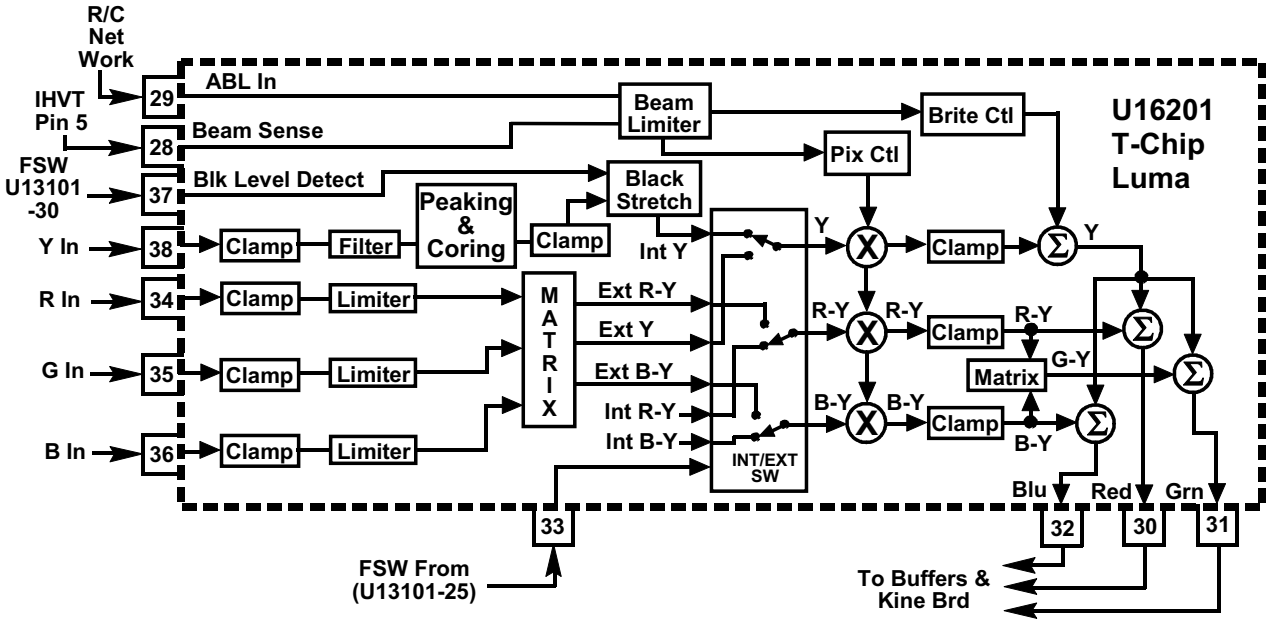


Figure 10-4, RGB Processing & Beam Limiting

CRT Management

The T4 chip also supplies low level signal processing for CRT management functions including AKB, black level and beam limiting. Although not a part of the T4 chip, SVM is an independent circuit deriving its signals from the luma output but will be discussed here.

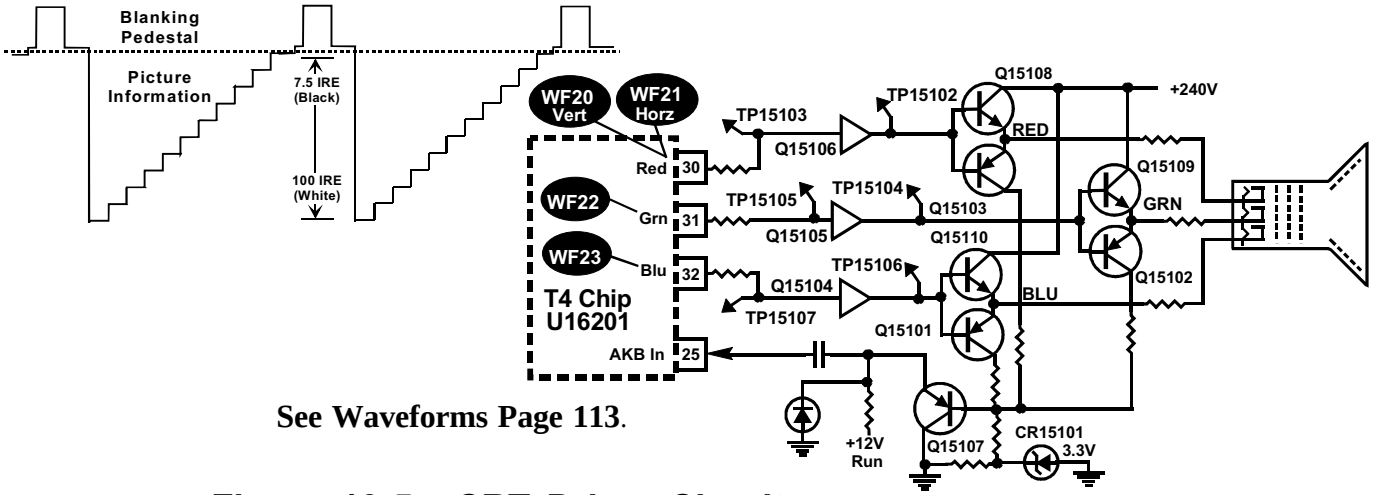
Beam Current Limiting

The beam limiter addresses the picture control as well as the brightness control inside the T4 video processing circuits. Beam current is sensed by pin 28 monitoring the secondary winding of the IHVT that supplies beam current. Normal beam limiting is done by reducing contrast, the amplitude of the Y, R-Y & B-Y signals at this stage (See Figure 10-4). However, if black level is adjusted too high by the consumer controls, and beam limiting is called for, the brightness control reduces the Y level first, without moving the consumer OSD. If insufficient beam current reduction is not achieved, the limiter can go into emergency brightness reduction. In this mode, the brightness is reduced to a very low level (it can be reduced to almost black). Emergency situations are determined by the microprocessor. An ABL (*A*utomatic *B*rightness *L*evel) filter on pin 29 sets the response time of the ABL circuit. Normally beam limiting will begin within 30 to 40 horizontal lines.

CRT Drivers

The CTC 197 uses cascode CRT drivers with PNP followers to provide a current reference for AKB. The RGB output of the T4 chip is amplified from approximately 2 Vpp to about 125 Vpp at the CRT cathodes. (Actual gain is tailored in software, depending on viewing screen size and gun). The CRT driver configuration will be used with direct view and projection CRT's. Video response is optimized to support 600 lines of resolution.

For this discussion, we will consider only the green channel. The Red and blue are identical circuits. The luma signal is output from pin 31 of the T4 and amplified by Q15105. The signal is then applied equally to the base of Q15109 and Q15102 (a PNP transistor which is the CRT driver). Note that as this signal increases, it is actually moving towards the blanking pedestal, or black. As the signal increases, the emitter voltage of Q15102 begins to increase towards the collector supply voltage, +240V, through Q15109. Beam current in a CRT is proportional to the bias voltage between the cathode and the screen grid. As the bias voltage increases, beam current increases. As bias voltage decreases, beam current decreases. Since the screen grid is normally fixed at around +300–400 volts, as the emitter voltage tracks towards the power supply voltage of +240V, bias decreases, decreasing beam current. As the drive signal



See Waveforms Page 113.

Figure 10-5, CRT Driver Circuitry

decreases, going towards white, Q15102 emitter moves away from +240V, increasing the bias voltage which increases beam current. Q15109 acts to limit the signal voltage. Part of the incoming drive signal is rectified and placed on Q15109 base. As the signal increases, bias voltage to the base increases, tracking the signal. This allows the emitter to follow the drive voltage until it reaches a voltage determined by the base bias resistor, R15109. The value of this resistor is determined according to screen size. Once this limit is reached, Q15109 shuts off, removing power supply from the CRT driver, Q15102, effectively shutting off beam current. AKB monitors all three cathode currents directly through the PNP transistor, Q15107. It is protected from excessive base voltage by a zener diode, CR15101. This effectively limits base voltage to about 8.5 volts. If the diode fails, the base-emitter junction of Q15107 would be in jeopardy as would input pin 25 of the T4 Chip.

Automatic Kine Bias & Scan Velocity Modulation

Scan Velocity Modulation

SVM is unchanged with the exception of the addition of a switch (Q15205) to shut off SVM effects during on-screen portions of scan. The entire horizontal line is shut off, not just the OSD portion of the line.

To mute the SVM, the normally high signal from the microprocessor to the base of Q15205 is switched low, turning it off. This shuts off current flow to the differential amplifier pair, Q15203 and Q15204. Without the differential amplifiers, the luminance signal cannot pass through to drive the SVM buffer, shutting down the SVM outputs and SVM effects. The circuit below represents the Direct View instruments however, the circuits found in the PTV (projection) are virtually identical with exception of the component callout numbers and the fact that the PTV has three (3) circuits because of the separate tubes.

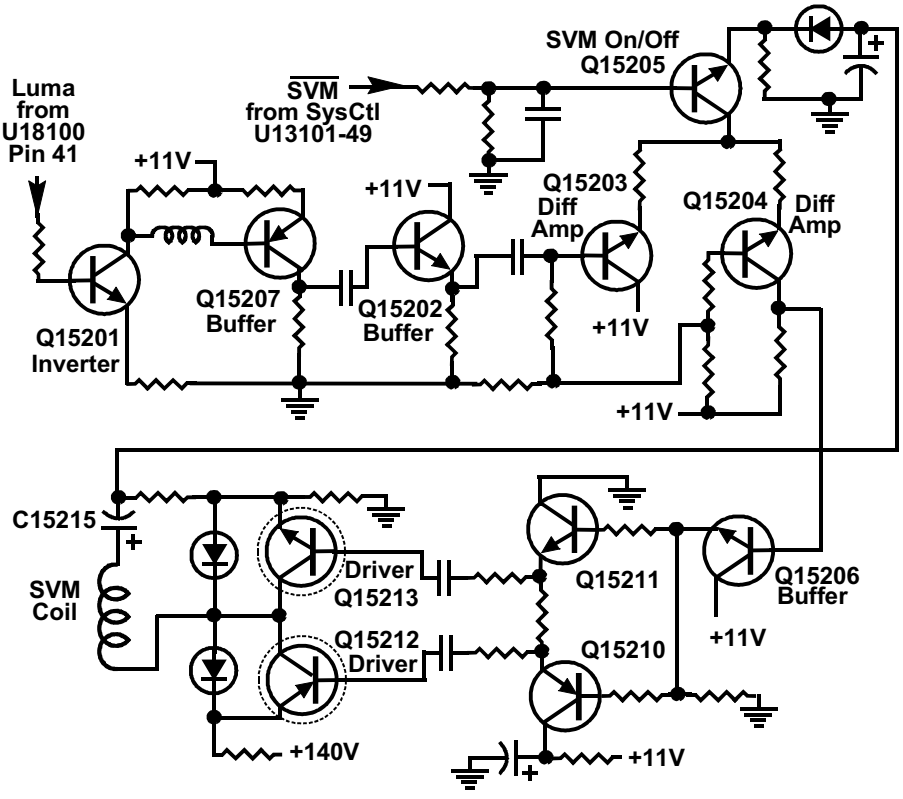


Figure 11-1, Scan Velocity Modulation

Automatic Kine Bias

As with previous chassis, the CTC195/197 employs an *A*utomatic *K*ine *B*ias (AKB) system to track and compensate for the normal drift in beam current cutoff bias of a CRT. Recall from the CRT driver discussion that beam current cutoff is reached at a specific bias voltage between the cathode and screen grid. If the incoming video level black level is not matched to the actual cutoff level of the CRT, the color temperature, or *apparent color tint*, of the CRT will change. Maintaining this match will allow the original color temperature setup to provide the same quality picture over the lifetime of the CRT.

The CTC195/197 AKB differs from prior circuitry and operation. Previous AKB systems used a sample and hold circuit that attempted cathode bias correction on every field. Components were picked to allow small but constant adjustments to the cathode bias based on the hardware limitations. The CTC195/197 does a sample and compare every 10 seconds. This does not allow any rapid changes in CRT bias, but since the intent is allow the CRT to operate at the correct color temperature over the life of the tube, there is really no reason to correct on every field. The new AKB system utilizes a digital comparator for the cathode feedback signal and is referred to as Digital AKB. The actual measurement and correction calculations are done in the main microprocessor by software and the results are stored in the EEPROM. This is a much different approach than that taken in the CTC179/189 family of chassis which was entirely hardware based.

Beginning with the CTC195/197, black level management will be provided with digital AKB. The digital AKB function contained within the T4 Chip is a one-bit system which samples the RGB cathode currents on lines 18, 19, and 20 of the raster, respectively. AKB reference pulses are added to the video black level on these lines and sampled by the T4 at pin 25, the cathode current sense input. This input is AC coupled and clamped at black to eliminate leakage current contributions to the sampled pulses. The signal is then compared by the T4 to a fixed reference level derived from power supply voltage samplings. The output of the comparator is latched into the status register where it is read and processed by the chassis microprocessor. The output pulse is derived from a net average of the RGB AKB latch states. AKB response time will be limited to an update rate which adequately corrects long term cutoff bias drift without causing noticeable instantaneous changes in color temperature. The intent is to track tube drift only. Instantaneous black level shifts will be ignored by AKB.

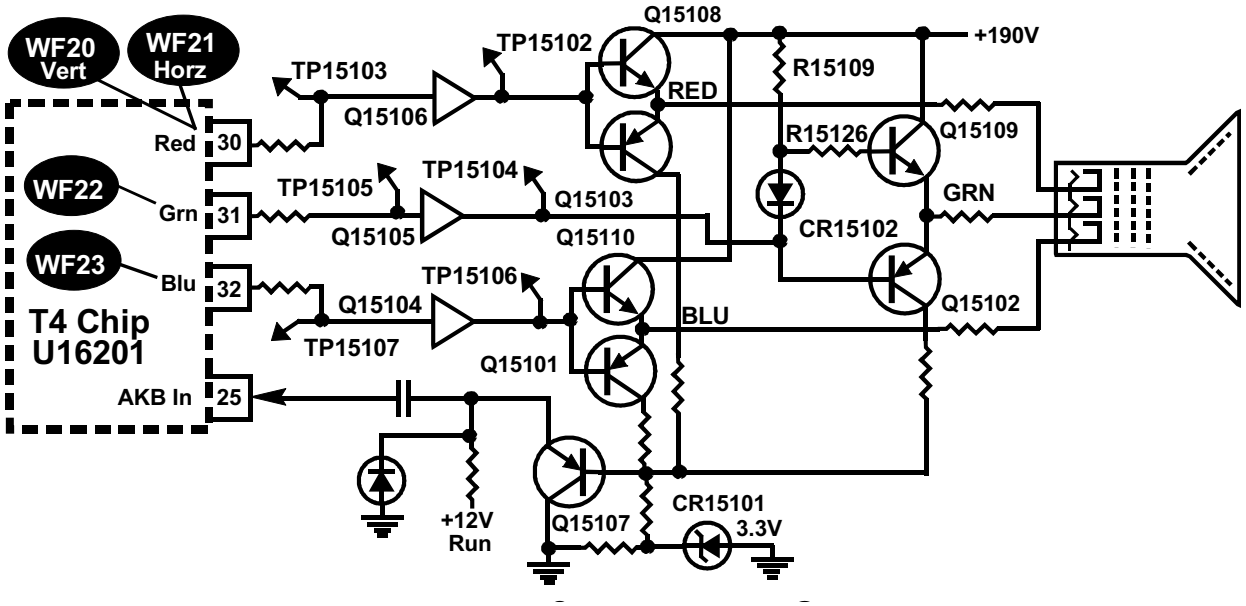
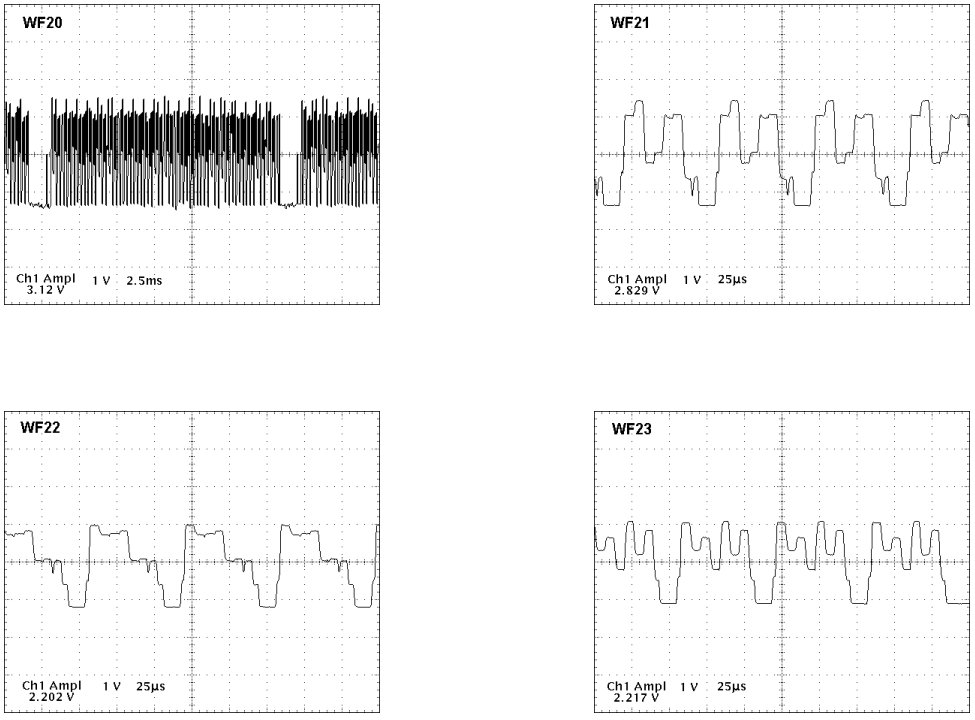


Figure 11-2, AKB and CRT Driver Block Diagram



AKB and CRT Driver Waveforms

Figure 11-3 shows three NTSC waveforms appearing at the cathode of a CRT. The resulting picture would be a gray scale bar pattern going from 100 IRE on the left just after the blanking pedestal to 7.5 IRE on the right, just before the blanking pedestal begins. The first illustration shows the effect of beam cutoff set too high. Notice that the blanking pedestal has cutoff the picture information long before the beam current has reached a cutoff voltage. This means that the higher IRE portion of the signal may max out beam current before the whitest part of the picture information is displayed.

Next is the effect of beam cutoff set too low. Now the dark or low IRE portions of the signal occur after the cutoff bias has stopped beam current. Also, since the peak to peak voltage of the waveform has not changed, the white portions of the signal will not have enough amplitude to reach full brightness. The final waveform shows a normal NTSC waveform at the correct cutoff bias. 7.5 IRE on the waveform occurs precisely at beam current cutoff. 100 IRE would occur at just below the maximum beam current obtainable with the particular CRT. It is not important what the particular cutoff voltage is, only that AKB recognizes the value and compensates over time to make certain the incoming signals sync with it to match the 7.5 IRE blanking level with the CRT cutoff bias voltage.

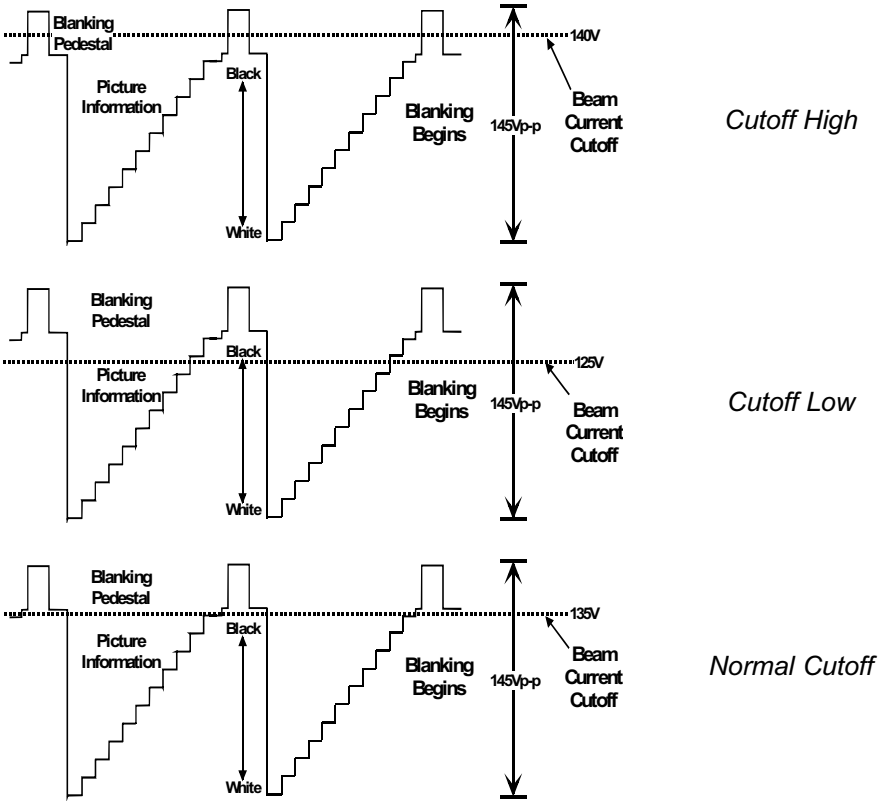
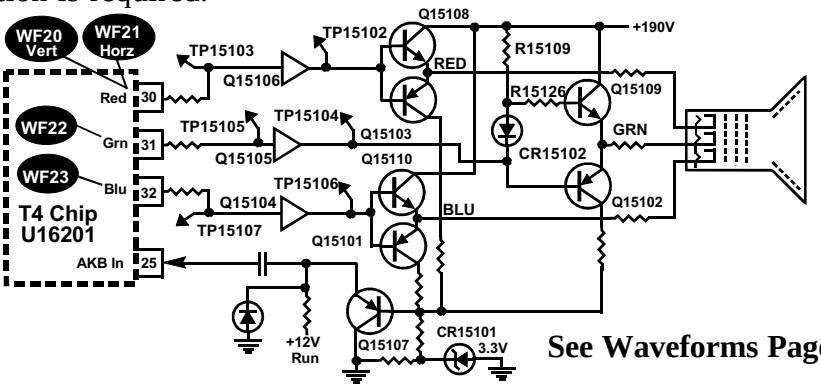


Figure 11-3, Cutoff Bias Comparison

AKB Operation

AKB operates on the principle that if a voltage pulse imposed on the RGB pedestal signal is alternated in peak voltage such that the voltage resulting from the current feedback is above and below a reference voltage, the long term average of the feedback signal should be the same as the reference voltage. If it is not, correction is required.



See Waveforms Page 113.

Figure 11-2 (Repeated), AKB and CRT Driver Block Diagram

AKB pedestals at specific levels are added to the RGB signals within the T4 Chip. The outgoing RGB signals with the AKB pulses are then amplified by the CRT drivers to begin CRT cathode current draw. Since cathode current is carried by the CRT drivers, the collector currents are essentially also the cathode currents. All three cathode currents are passed separately through resistors developing a voltage that is directly proportional to the cathode current. The voltage is passed back to the T4Chip through Q15107 for sampling and measurement. The amplitudes of the RGB AKB pulses are alternated such that the AKB_IN signal on pin 25 goes above and below a reference voltage, called the threshold, established in the T-Chip. As long as the CRT is stable, the system will have the same number of measurements above the threshold as below the threshold. The three bias controls allow the DC levels of the RGB signals to be adjusted independently of one another. A sub-brightness control can adjust all three color DC levels together. These adjustments affect the sample pulses as well as the video. Note that the consumer brightness control affects only the incoming video, not the AKB pulse amplitude.

The sample pulses are generated during the vertical blanking interval on lines 18, 19, and 20 for red, green, and blue respectively. These pulses generate cathode current resulting in a sample voltage during those lines. Since the collector currents are “summed” in the sample resistor, the result is a voltage that has a pulse on lines 18, 19, and 20. The sample line is capacitively coupled to the T4 Chip to remove any DC component. The CRT Management System block diagram, Figure 11-3, shows the T4 Chip AKB system. The system has three blocks called Red Color Temp, Grn Color Temp, and Blu Color Temp. These correspond to the amplitude of the inserted sampling pedestals or pulses. During lines 18 through 20, the RGB signals from the RGB block are replaced with a ‘’nominal” black level. At the same time, the pedestals are summed with the sub-brightness DC value and then added to the RGB signal after RGB Drive adjustments. The RGB Bias levels are then added to the RGB signals, and the signals are output from the T4 Chip. Note that blanking is disabled during lines 18 through 20 which allows the AKB RGB pulses to draw beam current.

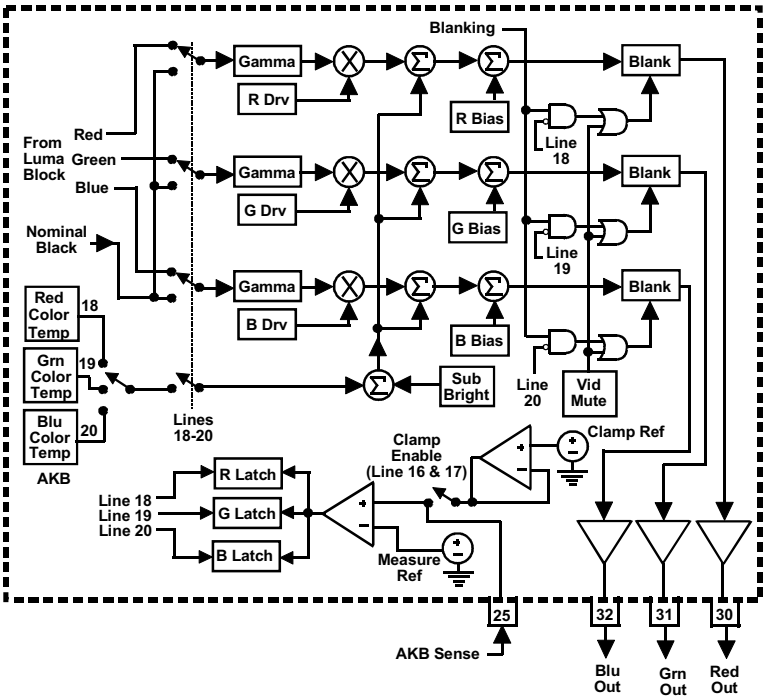


Figure 11-4, CRT Management Block Diagram

Start-up

The initialization values for the T4Chip are recalled from EEPROM. Bias and sub-brightness values are those that were in use just prior to the last shutdown of the set. The system assumes that the sample pulses will alternate above and below the threshold starting with the pulses above.

The feedback signal, called “AKB Sense”, is clamped to 3.8 volts during line 16 & 17. The clamped signal is compared to a 5.1 Volt reference. The output of the comparator is put into a one bit latch that is "1" if the voltage is above the reference and "0" if the voltage is below the reference. The latches are gated at the correct line so that the bit is set properly. There are I^2C registers that allow adjustment of the sample pedestal amplitude, disabling the AKB Sense clamp and turning off the pulses. This is the only control the T4 has for the AKB pulses. The decisions made as a result of the pulse information for AKB are in software control.

The number of occurrences of high and low are kept in an accumulator for each of the RGB channels. The accumulators are initially set to 2. After the 20 second delay, the system makes a measurement of the feedback signal at pin 25. It should be noted that the sample pulses are always present in the vertical blanking pulse. Only sampling is at the 6-10 second rate. Software measures the red, green, and blue samples in that order. If the measurement is above the threshold, the accumulator is incremented; if it is below the threshold, the accumulator is decremented. As long as the accumulator value is 1, 2, or 3, nothing is done. If the accumulator value is 0 or 4, the software makes an adjustment. If any one color accumulator has a value or 0, beam current for that color too low, and the bias value of that color is increased. If the value is 4, the beam current is too high and the bias value is decreased.

AKB Accumulator	Bias Control
4	Decrement by 1
3	No change
2	No change
1	No change
0	Increment by 1

Red AKB Accumulator	Green AKB Accumulator	Blue AKB Accumulator	Sub-brightness
Any Two Colors = 4			Decrement by 1
4	4	4	Decrement by 1
3	3	3	No change
2	2	2	No change
1	1	1	No change
0	0	0	Increment by 1
Any Two Colors = 0			Increment by 1

If all three accumulators contain a 0 but more adjustment is needed, AKB assumes the CRT is biased too low and the value of the sub-brightness is incremented by one. If all three accumulators contain a 4 and more adjustment is required, the sub-brightness is decremented by one. These two adjustments affect all three colors equally, and raises (or lowers) the current of all three guns.

If a sub-brightness adjustment has been done, all three sample pulses are decreased by one step. Only one sample pulse adjustment is allowed per color per cycle. After the second pass, the sample pulse amplitudes are increased by the same rules as they were decreased in the first pass. *This continues for as long as the set is running.* If a measurement indicates the system has run out of adjustment range on any or all colors, no further adjustments are allowed. This keeps the system from changing the temperature of the colors that may still have adjustment. If those colors were to be adjusted, the color temperature might be mistracked due to lack of response of the color that has stopped adjustment. When the set is turned off, the current values of bias and sub-brightness are stored for use the next time the set is turned on.

CTC195 AKB

The AKB system for the projection chassis, CTC195, varies slightly from the CTC197. The CRT management is split into three separate kineboards for the three color CRT's, but the common line is still brought back to the T4 Chip and functionally, at that point operation becomes the same.

AKB and Color Temperature Alignment

AKB alignment is strictly a software function. What the technician will adjust is the screen control(s) and the color temperature via the RGB bias and drive controls. It will be possible to set color temperature, thus aligning AKB, without the use of Chipper Check in the CTC195 and the CTC197, however, the adjustment is both "touchy" and critical. Chipper Check is the preferred method under all circumstances. The following steps will enable the technician to set color temperature, aligning AKB, using only the front panel buttons. Using Chipper Check, AKB is located under the "Color Temperature" alignment section. Instructions are included for performing the alignments.

To align Color Temperature in the CTC197 chassis:

1. Enter the customer control menu and reset the video controls to factory default values by selecting the "Picture Reset" control (Use reset selection 3, "Bright").
2. Apply a gray scale staircase pattern to the VID 1 input.
3. Enter the service alignment program;

   Press and hold the MENU button, then
   Press and release the POWER button, then
   Press and hold the VOL UP button.
   Release the MENU and VOL UP buttons at the same time.
   Increment the V: number to 76 by using the VOL UP button.
   Press the CH UP button to enter the service mode.

4. Press CH UP until P:13 (Red Bias) is reached. Set this value to 63. Also set the green (P:14) and blue (P:15) bias controls to 63.

   NOTE: The remote control may be used to increment or decrement parameters or values unless the service menu is exited. The service menu may be entered only by using the front panel.
5. Set the drive parameters (P:16, 17 & 18) to a nominal value (normally 32, but in the case of "AEG" high performance tubes, 40). Consult the latest service literature for further explanation of the setting of this value.
6. Return to P:13 and bring up the service line by pressing the MENU button.
7. Turn the CRT screen control off (full counterclockwise) then slowly increase (clockwise) until the service line is barely visible, regardless of the color of the line. Continue slightly past the point where the line becomes visible.
8. Note which line became visible first and do not touch this bias control for the remainder of the color temperature alignment procedure. Go to the remaining two bias adjustments, increasing them to produce a white line.
9. Exit the service menu. Readjust the screen control to produce even steps of the gray scale. The darkest bar should remain black.
10. Reenter the service menu and go to P:16,17 &18, the red, green and blue drive controls. Adjust them to obtain a gray pattern from the mid portion of the gray scale to the upper IRE (white) portion.

NOTE: Bias controls affect the low level portions of a picture. Drive controls affect the brighter portions.

12. Recheck the gray scale, observing it to make certain the screen is shades of gray, with no red, green or blue tinting. If some tinting is observed, return to the beginning of the color temperature alignments and repeat.

13. Exiting the service menu will initiate the automatic AKB alignment. The screen will flash green if AKB setup was successful. If the screen flashes red, return to the beginning and perform the color temperature setup again.

To align Color Temperature for the CTC195 chassis;

1. Enter the customer control menu and reset the video controls to factory default values by selecting the "Picture Reset" control (Use reset selection 2, "Normal").

2. Apply a gray scale staircase pattern to the Aux 1 video input.

3. Enter the service alignment program;

   Press and hold the MENU button, then
   Press and release the POWER button, then
   Press and hold the VOL UP button.
   Release the MENU and VOL UP buttons at the same time.
   Increment the V: number to 76 by using the VOL UP button.
   Press the CH UP button to enter the service mode.

4. Press CH UP until P:13 (Red Bias) is reached. Press MENU twice to reset the biases and preset the sub-brightness settings.

   NOTE: From this point, the remote control may be used to increment or decrement parameters or values unless the service menu is exited. The service menu may be entered only by using the front panel.

5. Set the drive parameters (P:16, 17 & 18) to 45. Consult the service literature for further explanation of the setting of this value.

6. Turn all three CRT screen controls off (full counterclockwise) and slowly increase each control (clockwise) until the second bar from the dark side of the pattern is slightly visible for each of the three colors.

7. Adjust P:13 (red), P:14 (green) and P:15 (blue) to fine tune the second lowest level (10 IRE) bar to a gray color.

8. Adjust P:16, P:17 and P:18 drive controls to make the brighter portions (40-100 IRE) of the gray scale pattern a neutral white.

9. Readjust P:13, P:14 and P:15 as needed to assure the low light areas remain gray.

   NOTE: Bias controls affect the low brightness level portions of a picture. Drive controls affect the brighter portions.

10. Exit the service menu by pressing the PWR button. If AKB alignment was successful, the screen will flash green. If it was not, the screen will flash red. If AKB setup was not successful, repeat the procedure from step 3.

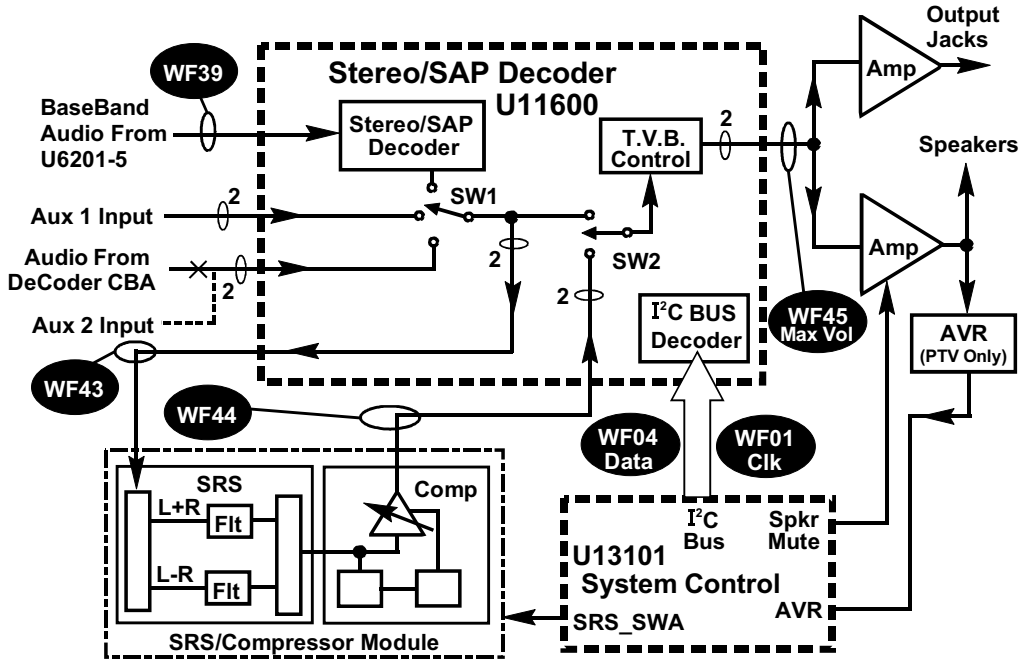
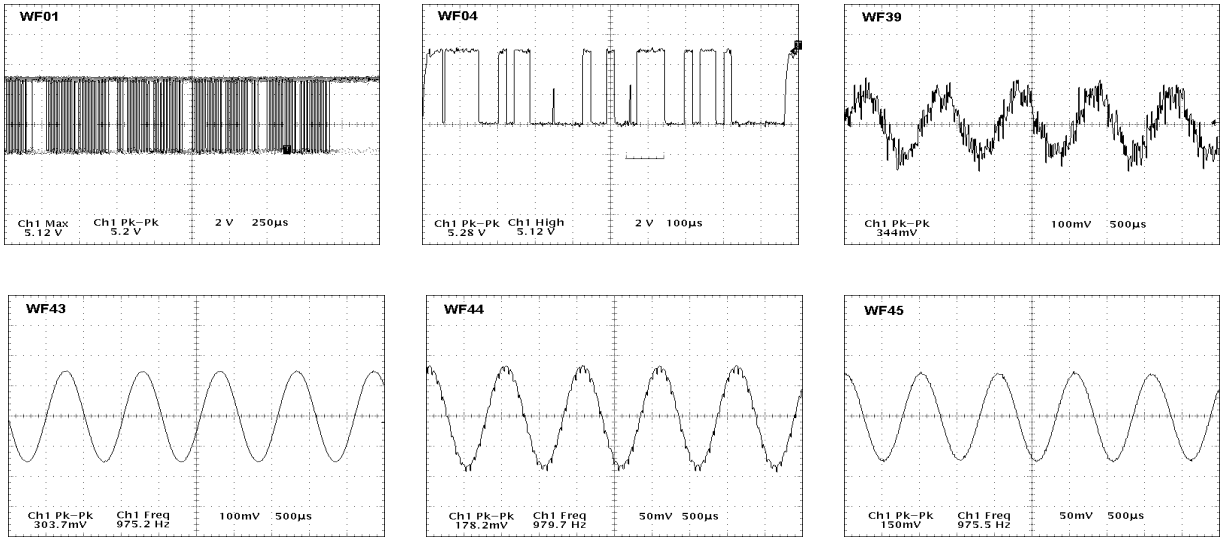


Figure 12-1, Audio Block Diagram

Audio Processing Overview

Audio processing IC U11600 is the central core to the CTC195/197 audio system. As shown in the block diagram above, the IC contains the Stereo/SAP decoders, switches, tone, volume and balance (TVB) processing, along with the I²C bus interface. All functions, alignments and control of U11600 is performed by the System Control Microcomputer U13101 via the I²C bus. The main audio processing IC U11600 is located on the main chassis. The alignment values are stored in nonvolatile memory (EEPROM) and can be updated by a field-alignment mode. These alignment values are rewritten to the audio IC any time the IC loses power. The audio IC registers are volatile and lose all settings if power is removed from the IC.



Audio Block Diagram Waveforms

The input audio signal source is selected by SW1 in U11600. These inputs are Base Band audio from U16201 pin 5, Aux1 or Decoder CBA (Aux2) inputs. The output of switch #1 is then routed through the SRS/Compressor Module or is applied directly to the TVB controls of U11600. Switch #2 determines if the audio is routed through the SRS/Compressor circuit. The SRS/Compressor module is controlled via the SRS_SWA output of the System Control Microcomputer U13101. After processing by U11600 the audio exits the IC and is applied to the speaker and output jack amplifiers. The 10 watt audio PTV's (projection television) contain an AVR (Automatic Volume Reduction) circuit that monitors the audio output and protects for momentary over-current conditions on the output. The speakers are muted via the Spkr Mute output of the System Micro U13101.

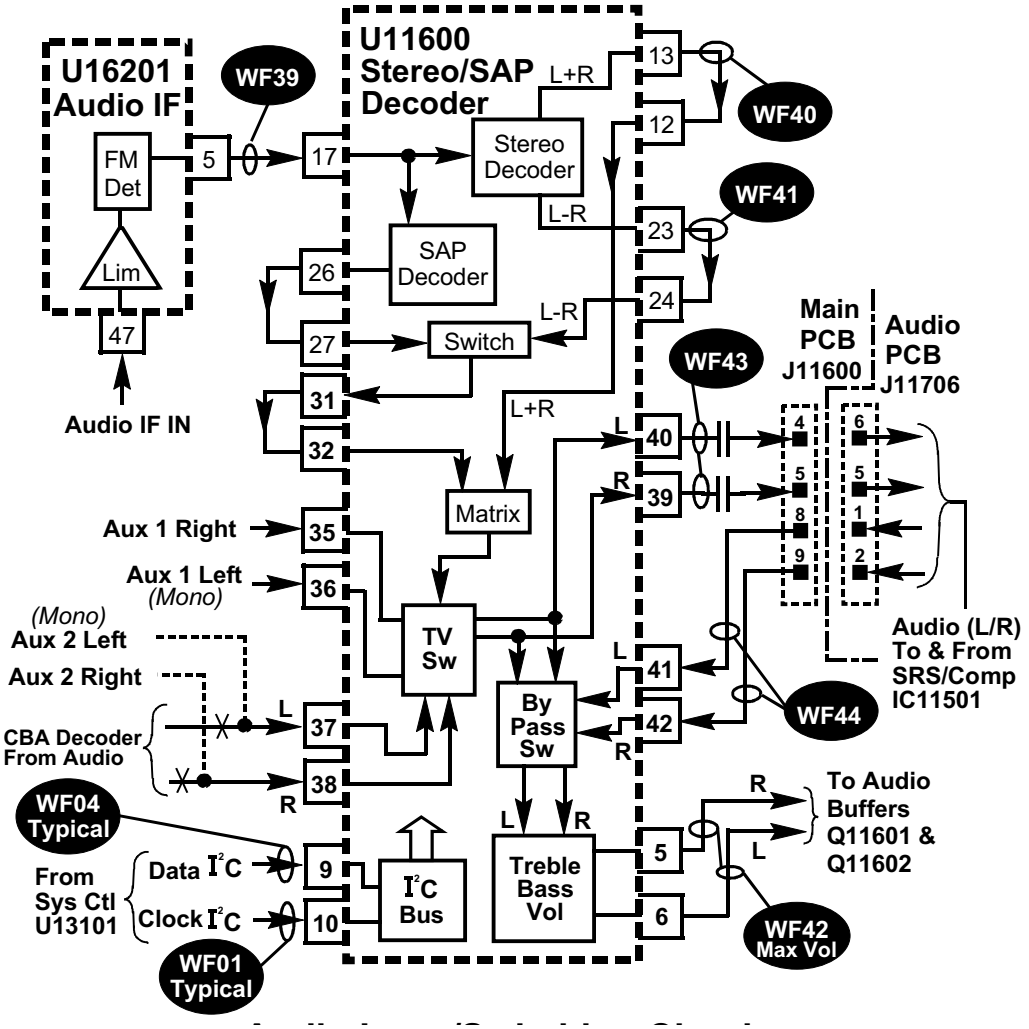


Figure 12-2, Audio Input

See Waveforms Page 123.

Audio Input/Switching Circuit

Demodulated wideband audio (WBA) exits the Audio IF portion of the one-chip IC (U16201 pin 5) and is routed to the WBA input, pin 17, of the audio IC U11600. The audio signal is first applied to the Stereo and SAP decoders inside IC U11600. These decoders are aligned via I^2C bus. When Stereo and/or SAP are detected, their "presence" is made known to the system control microprocessor via the I^2C data bus. The recovered stereo and/or SAP signals are sent to a switch inside U11600 that routes the appropriate one to the dbx expander. All dbx expander alignments are bus-controlled as well. The instructions as to which signal to process are returned to the audio IC. The desired signal is then sent to the 3-position "input select" **TV SW**itch. Customer commands, via the microcomputer and I^2C bus, operate this switch to process received audio or an INPUT source applied to pins 35,36, 37 or 38.

This "selected" signal is applied to the "Loop Out" pins (40 and 39) and the two position "Bypass" switch. Customer commands again determine whether the selected signal, or the SRS/Compressor audio returned via the "Loop In" pins (41 and 42), is processed. The "Loop Out" (40 and 39) pins permit the connection of SRS/Compressor circuit board. The fixed level signal is available at the "Loop Out" pins and is then applied to the SRS/Compressor circuit. The audio signal is returned from the SRS/ Compressor CBA via "Loop In" pins (41 and 42). The audio is then applied to an internal (U11600) Bypass Switch. The Bypass switch allows "SRS ON/OFF" control without the SRS processor having to have bypass circuitry itself. The output of the Bypass switch is then routed to the Tone/Volume/Balance (TVB) section of U11600. The signal is processed according to the customer settings of volume, bass, treble, and balance. The audio signal next exits the IC at pins 5 and 6 where it is applied to the audio buffers and output power amplifiers.

Balance Control

Audio IC U11600 does not have a separate balance control. Balance is controlled by adjusting the Left and Right VOLUME registers to different values. If the Balance control is centered, Volume setting for both left and right would be the same. If the Balance is moved to one side or the other, the opposite volume control would be lowered accordingly. If Balance is off-center this means that the VOLUME levels have been set unequally. If the VOLUME is changed, each VOLUME control register is incremented or decremented at the same rate but they remain unequal by the same amount. If VOLUME is decremented and the lower VOLUME register reaches 0 before the other VOLUME, that register remains at 0 as the other one continues to decrement.

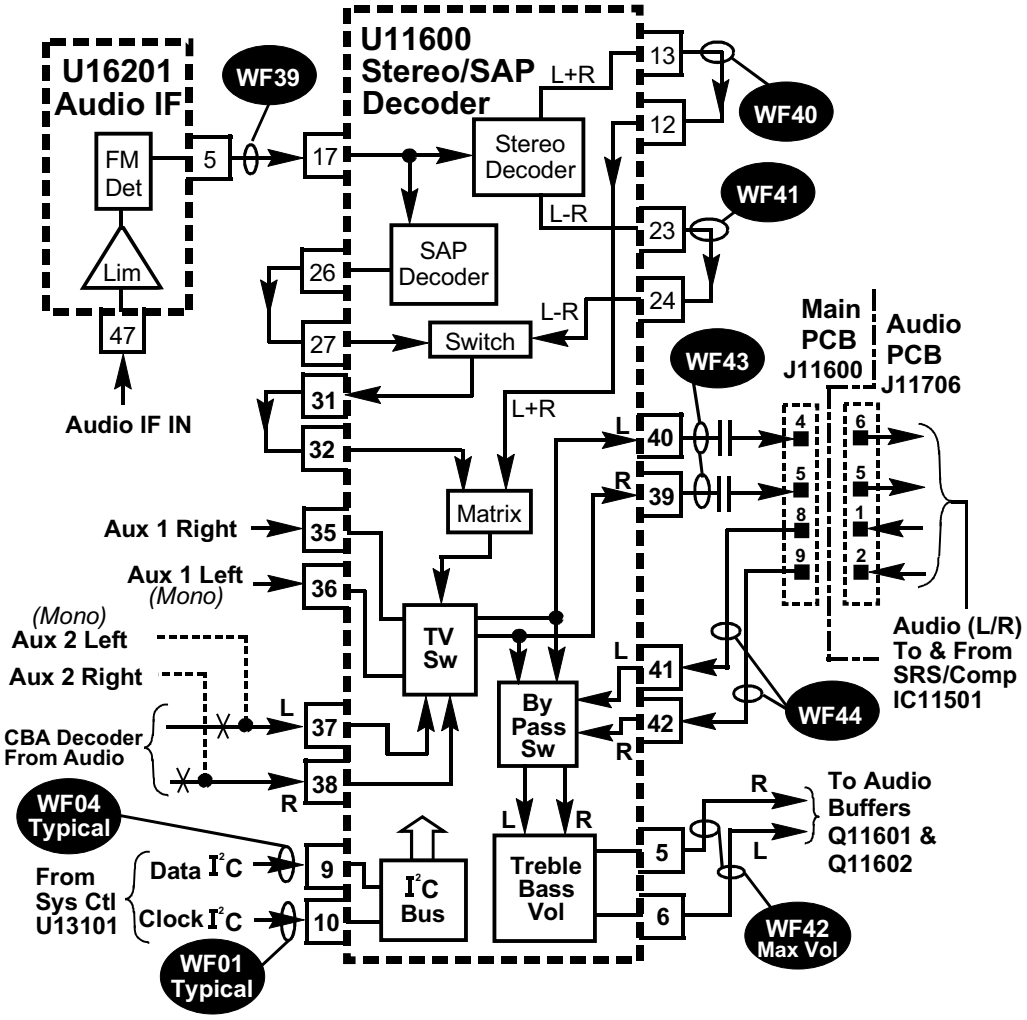
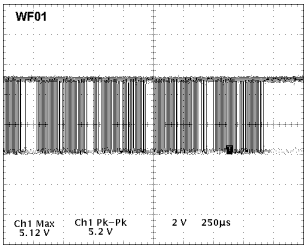
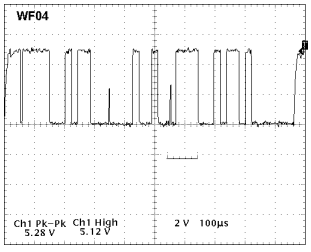
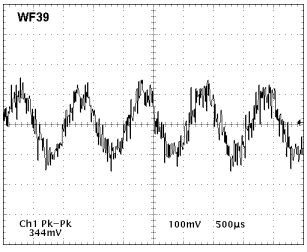
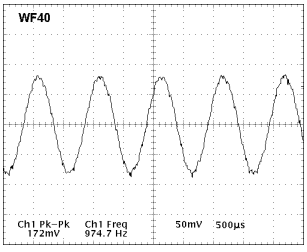


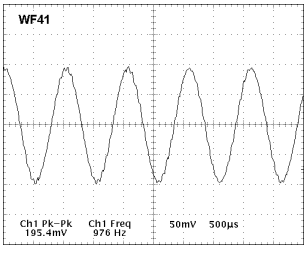
Figure 12-2 (Repeated), Audio Input

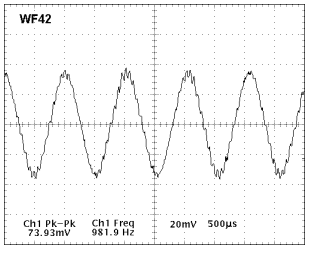


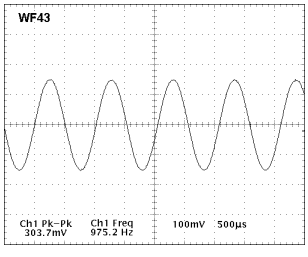


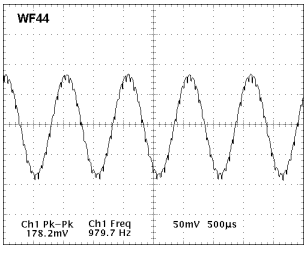












Volume Taper & Fletcher-Munson Network

Fletcher-Munson compensation is an attempt to correct for the ear's decreased sensitivity to bass and treble frequencies at lower sound levels. The Fletcher-Munson correction function is performed automatically within U11600 by utilizing the Bass, Treble and Volume controls. This is performed by having the main micro volume control algorithm adjust the BASS and TREBLE controls in U11600 to compensate for consumer volume adjustments. As Volume is decreased, the BASS is increased slightly making low-frequency sounds disproportionately louder so that tonal balance seems more constant as the volume goes up. A limited range of bass boost is available so the amount of increase is a trade-off with how much range is left for customer control. In general the algorithm modifies the BASS register data by a "delta factor" from the customer setting. The BASS menu (customer menu) is not changed as the register is changed automatically by the system. The Volume register is assumed to have 64 states.

Fletcher-Munson curve, also referred to as equal-loudness contours, pertains to a set of curves depicting the characteristics of the human ear (refer to figure below) for different intensity levels between the threshold of hearing and the threshold of feeling. The base reference frequency is 1KHz. The volume curve should theoretically be a straight line (linear), however because of the characteristics of the human ear, the curve should be steeper for about the first half and shallower for the last half (see accompanying graph). Correction for the Fletcher-Munson effect is corrected for internally within IC U11600 via the Treble/Bass/Vol control section.

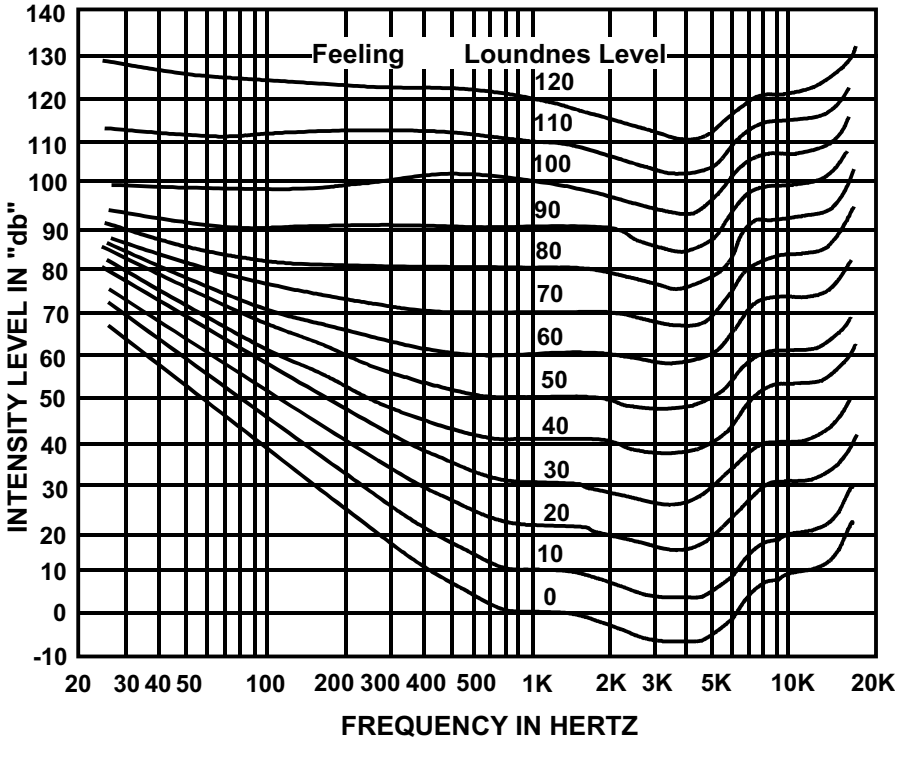
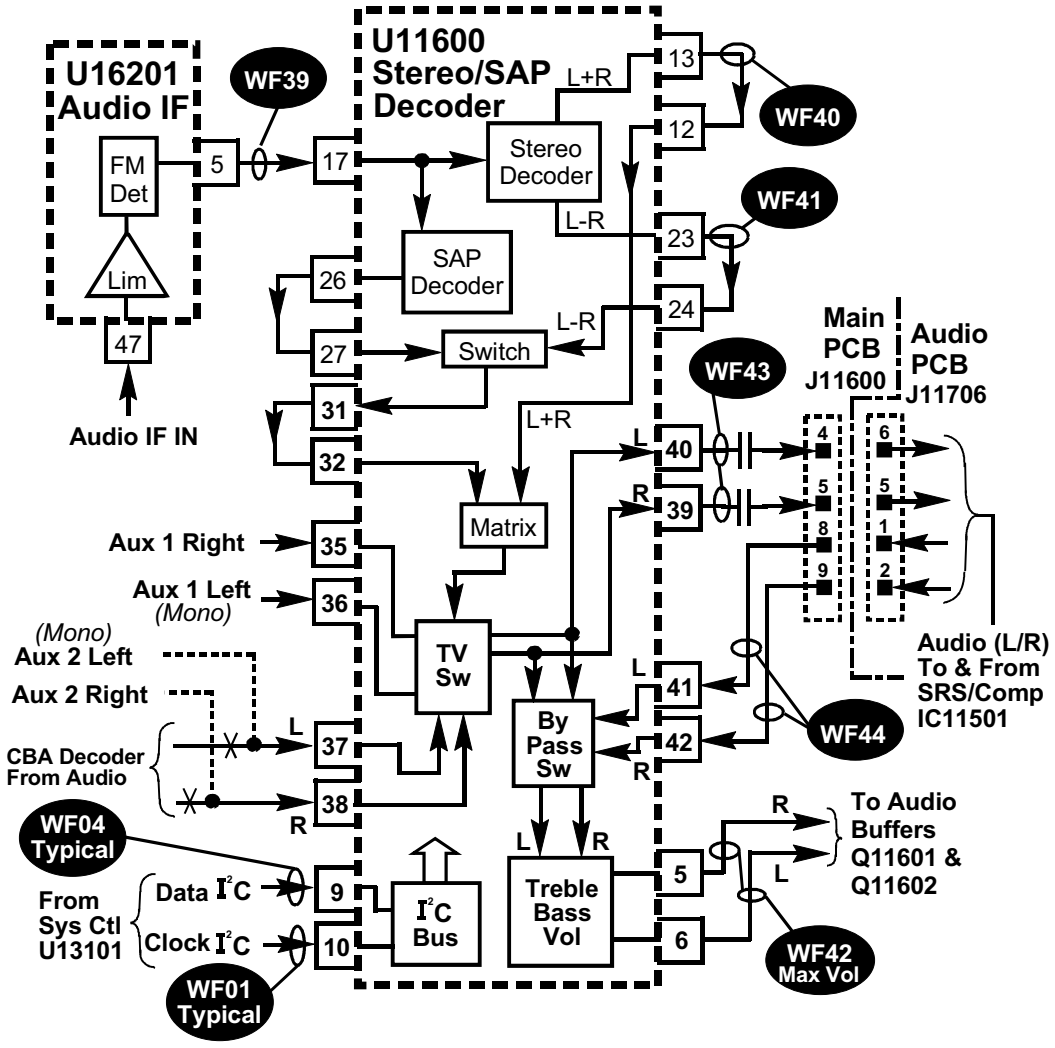


Figure 12-3, Fletcher-Munson Curve



See Waveforms Page 123.

Figure 12-4, Audio Input Switching & Waveforms

Audio Output Circuit

The audio output signal from pins 5 and 6 of IC U11600 (Figure 12-5, Page 122) is first applied to buffer transistors Q11601 and Q11602. The output of the buffers are then sent to the power amps and the HiFi jack drivers. The power amp (IC U11901) is a stereo, multi-watt IC. The IC is biased for single-supply operation with an external network. It is powered from a separate, isolated supply. The supply for the audio power amp is 24V for the 1W and 5W per-channel audio systems (Direct View & PTV) and 35V for 10W PTV only versions. Power is always applied to the power amps. The audio amp is placed in STANDBY when the set is shut off (or the speakers are turned off in the menu). Speaker impedance is 8 ohms for 5W and 10W versions and 32 ohms for 1W versions. No external speaker connection is provided.

The audio output jacks are driven by IC U11401. The audio input to this IC is the same audio applied to the speaker power amps. The jack driver utilizes a non-inverting op-amp circuit with a gain of approximately 5. It isolates the levels in the system from various load impedance's applied to the HiFi jacks and provides about 500mVrms at the jacks at typical volume settings.

In 10W versions, the output is also sent to the "AVR" (Automatic Volume Reduction) circuit. The average voltage level is compared to a reference and if it exceeds it, an output signal notifies the micro to begin decreasing the volume setting to reduce the output power. In this way power is limited to less than 15W steady-state and clipping is reduced, which can prevent output device or speaker damage.

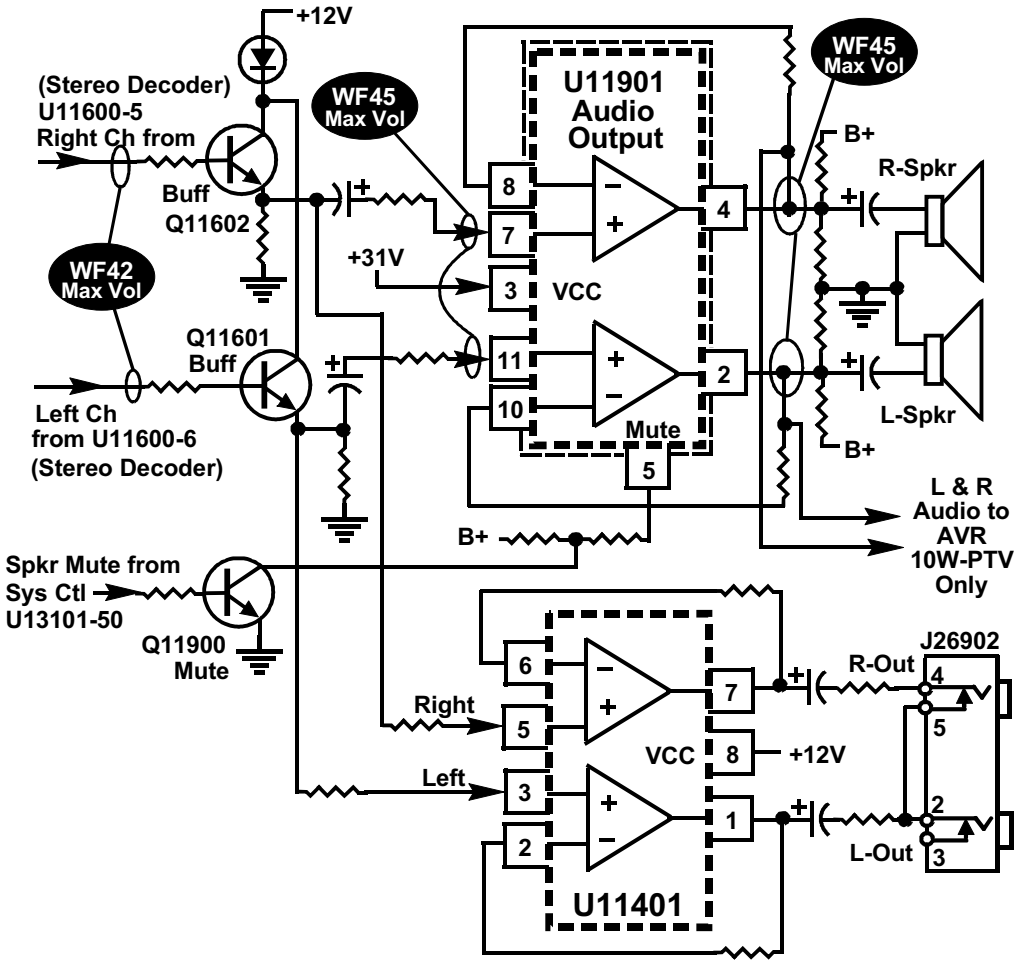
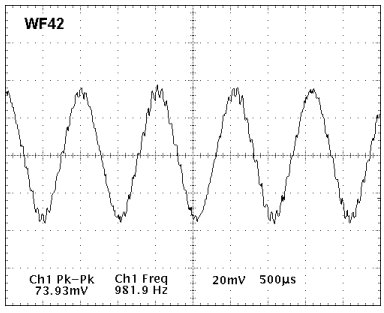
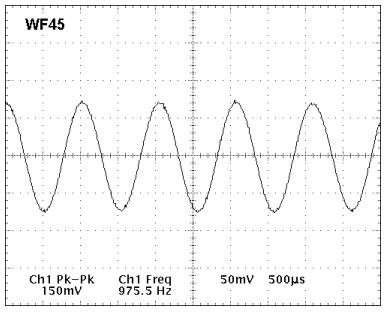


Figure 12-5, Audio Output





AVR (Automatic Volume Reduction)

Automatic Volume Reduction lowers the signal to the output amplifiers during possible over-current conditions that may damage the output device or speakers. The 197 has one control line and thus 2 states. The AVR control line is polled periodically (approx. 10Hz rate) to check the status of the output level. Whenever the input to the System Control Microcomputer at pin 48 is LOW, no action is required. When it goes HIGH, the VOLUME register is decremented at a 10Hz rate until the AVR sense line drops LOW again. Then the register stops decrementing and a 5 second timer is started. If the line goes HIGH again, the timer is canceled and VOLUME is again decremented until the line goes LOW. If the timer runs down and the line has stayed LOW, VOLUME is incremented back toward the customer setting, one step every 5 seconds. If the line goes HIGH at any time, incrementing stops and the decrementing loop is again entered.

The audio from the power amps are applied to CR11901/902. These diodes act as rectifiers to generate a filtered DC voltage at the base of Q11902 & 903. As the output level goes up, the corresponding DC voltage at the base of Q11902 & 903 goes up. A reference voltage is generated by zener diode CR11903 and transistor Q11904. This reference, which sets the emitter voltage of Q11902 & 903 to approximately 4.2VDC. If the voltage on the base of either of these transistors rise to approximately 4.9VDC, the transistor turns on. This puts a low on the base of Q11901, which turns it on. With Q11901 on, a Hi from the emitter is applied to pin 48 of IC13101.

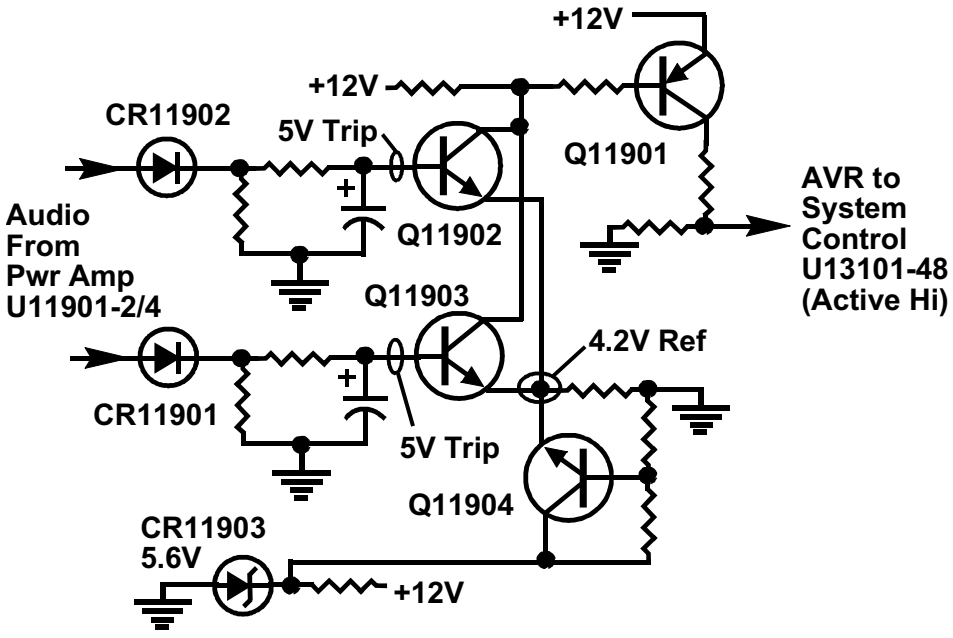


Figure 12-6, AVR (Automatic Volume Reduction)

SRS/Compressor Circuits

The Compressor feature used in the CTC197 audio system is contained (with SRS) on a SIP-type module that plugs into a connector on the main chassis. Interconnections are Left & Right input, Left & Right output, +12V power, ground, I^2C bus, and one control line. The Compressor (and SRS) can be described as "inserted" processors because the main fixed-level audio path is opened and they are inserted into the path. Compression occurs after SRS processing. The reason for this that compression negates or minimizes much of the SRS effect (if SRS is in Normal mode). Although the compressor's effect is maintained, SRS can be left turned on in "Compression Only" modes with little noticeable difference. Only three modes are needed:

STEREO/(no features)

SRS ONLY

COMPRESSOR/(SRS)

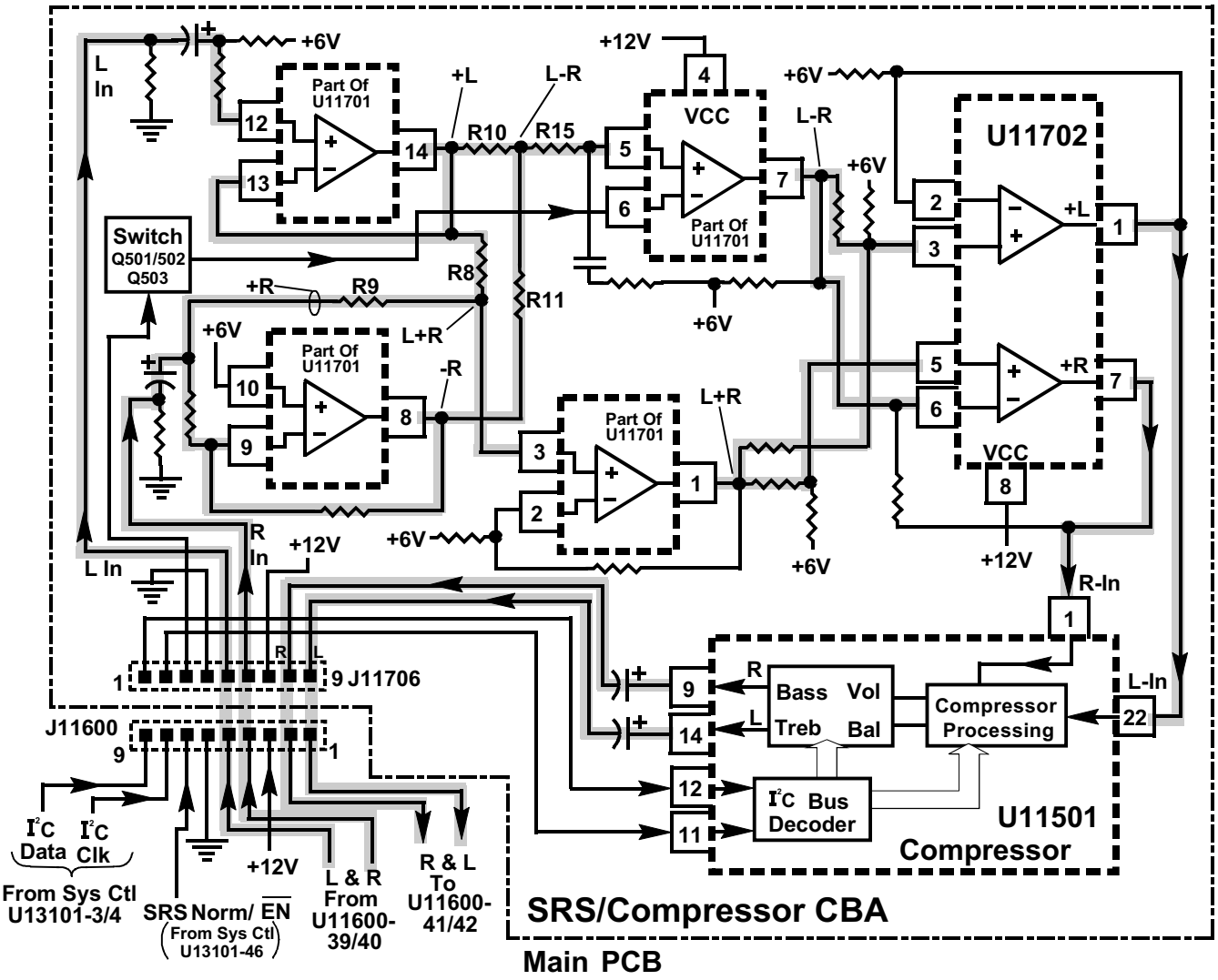


Figure 13-1, SRS/Compressor

The bypass switch in the stereo IC selects the direct signal, bypassing all features. For SRS ONLY the compressor function is turned off in the IC via I^2C Commands. For COMPRESSOR/(SRS), the compressor is activated and SRS is always on. The IC (U11501) and it's associated components implements the compressor function. This part contains, in addition to the compressor circuitry, TVB, pseudo-stereo, and simple surround, however, these other functions are not used. During turn-on initialization these functions are defeated as necessary (tone controls are set flat, volume set to unity gain, the other features defeated, etc.). Subsequently the only register changed is the Compressor ON/OFF.

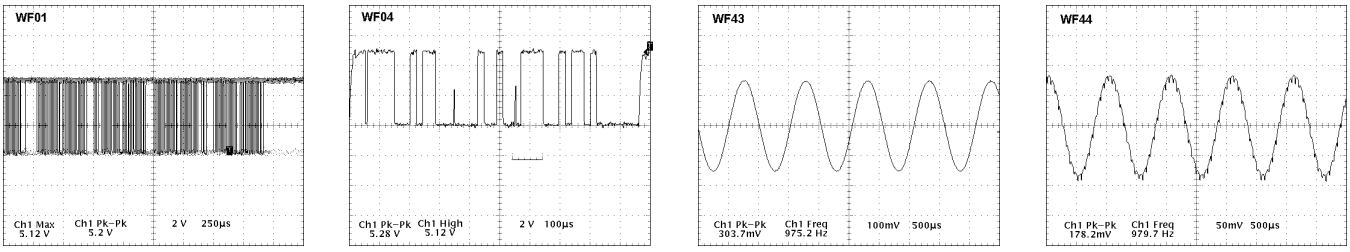
The IC contains two compressor circuits, one "open loop" and one "closed loop". The Open-loop configuration causes nonlinear compression curves so this section is designed to have the most effect at lower inputs while providing unity gain for inputs below 10mV and a small amount of for inputs in the 10 to 100mV range.

The Closed-Loop portion of the circuit produces it's effect at higher levels and establishes unity gain at about 200mV and a 2:1 compression curve (or nearly constant output) for inputs in the 100mV to 1V range. The overall response thus applies near-unity gain to low level signals, which reduces "noise pumping". It applies several db gain to mid-level signals to make them more easily heard, and compresses the high levels to reduce annoying loudness changes.

The SRS feature used in the CTC197 audio system is contained on a module connected to the main chassis with a cable. Interconnections are Left & Right input, Left & Right output, +12V power, ground along with data and clock lines. In response to requirements for a more cost-effective system, the companding sections were removed since they are the most complex and can introduce audible artifacts in some material. The L-R channel has a moderate gain factor to enhance weak stereo sources and widen the image somewhat. Filtering also helps keep the midrange from being overly boosted. Both paths have filters to help restore directional clues by compensating for the ear's directional frequency response. The L-R channel is defined as carrying the "side" information and the L+R channel the "front" sounds.

OVERALL SYSTEM STATE CONTROL

SRS CONT LINE	**SRS MODE**
LOW	OFF
MID	SRS NORMAL
HIGH	SRS ENHANCED



SRS/Compressor Waveforms

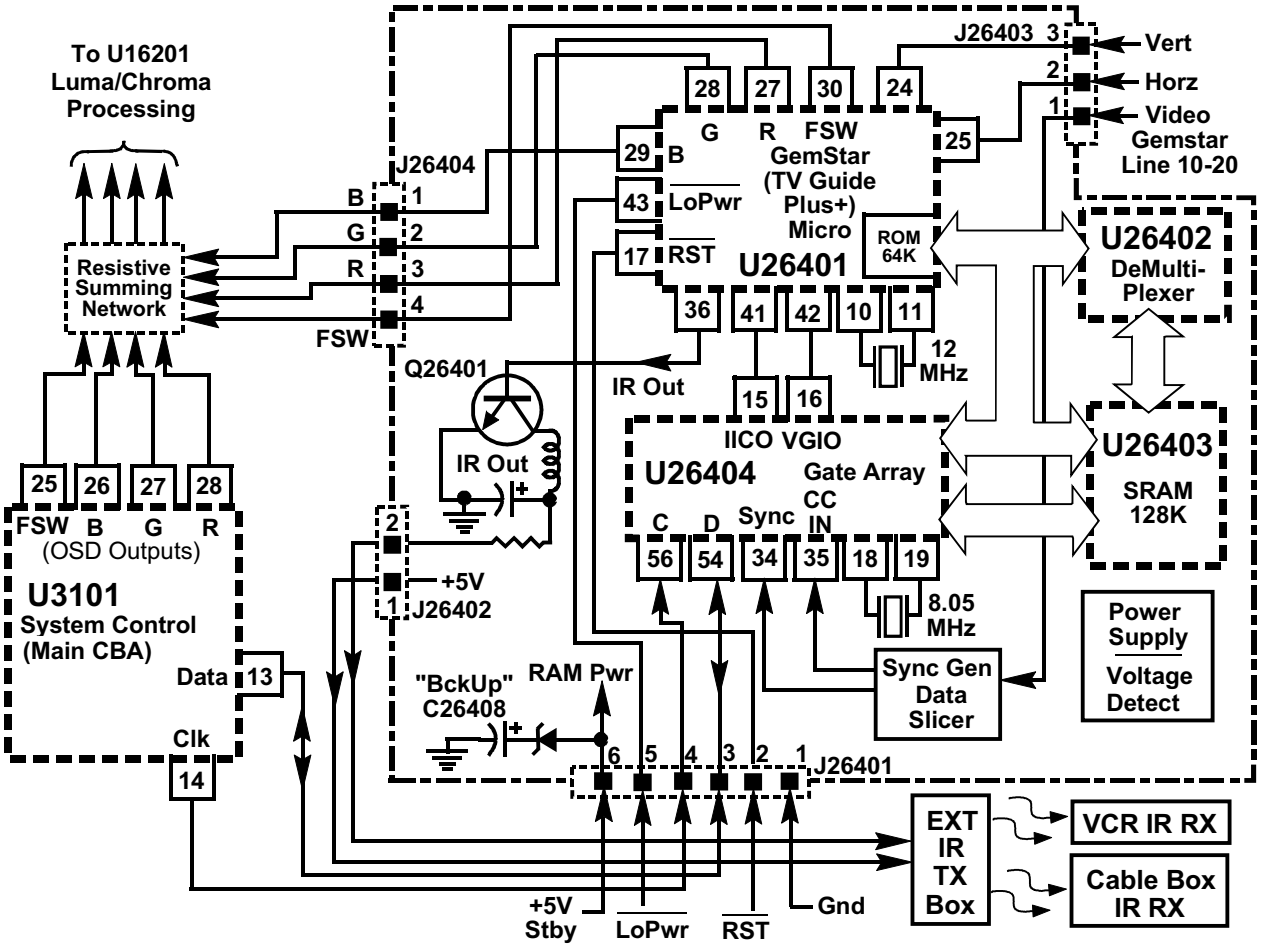
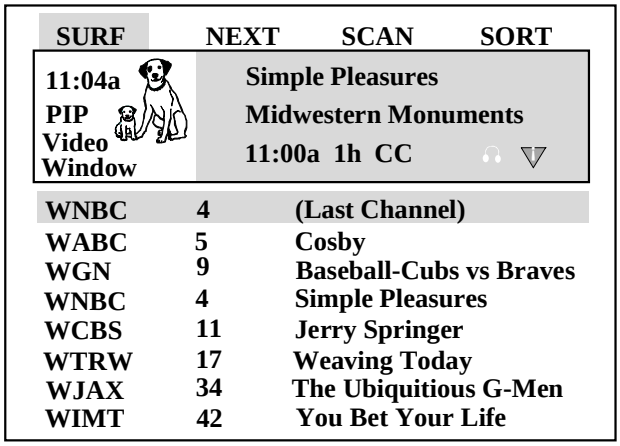


Figure 14-1, GemStar Decoder Block Diagram (TV Guide Plus+)



"TV Guide Plus+" Sample On-Screen-Display

TV Guide Plus+

TV Guide Plus+ is an interactive on-screen program guide that lists TV schedules for an area and allows the TV to have direct control of the cable box and VCR. There are three sections to a TV Guide Plus+ menu.

- A row of menus or options across the top of the screen
- Program information
- Channel listing

New program information is downloaded to TV Guide Plus+ daily at predetermined times. The download times are always "Local Time" occur at the following times: 2:05AM, 7:00AM, 10:45AM and 2:00PM. These download times are administered by the local broadcaster and cable companies. Currently, program information may include title, brief description, time program starts, length, and the availability of closed captioning, stereo, and additional program information.

- During installation and setup a series of screens asks about cable TV setup. If a cable box is being used, the TV Guide Plus+ should control it, otherwise, TV Guide Plus+ may not be able to locate and download the correct program information. TV Guide Plus+ checks a variety of codes to find one that exactly matches your cable box. When the brand and type of cable box is correctly identified, the cable box automatically changes to channel 9.

If more than one cable company services an area, TV Guide Plus+ may download a channel map for each company. After the TV completes its first download, the operator is prompted to manually select the channel map. If TV Guide Plus+ does not recognize the cable box or VCR after several tries, a screen reading, ***"Cable Box (VCR) test failed… Please consult manual and try again"*** appears. If this happens:

- Double check the codes listed in the

tables and make sure the correct code was entered.

- Check to make sure the IR controllers are positioned correctly

EPG Self-Diagnositcs

The TV Guide Plus+ Electronic Program Guide utilizes a customer assessable "Diagnostic" menu. This should only be used as a last resort by the customer because when the diagnostic is acitvated all program information in the EPG is lost. This involves a lengthy re-load of the customers EPG information. To access the self-diagnostic menu perform the steps below.

1. Go to EPG Setup Menu.
2. Press "Go-Back" Button
3. Press "TV" Button (1st time).
4. Press "TV" Button (2nd time).

NOTE: All EPG information is "Dumped" when the Self-Diagnostic menu is activated.

Menu's

TV Guide Plus+ offers four major types of menus for browsing program listings, these are: **SURF, NEXT, SCAN**, and **SORT**.

"Surf" Menu: The Surf Menu displays the current program on each channel. The channel displayed in the video window changes as you surf through program listings.

"Next" Menu: The Next Menu displays the programs on a selected channel from the current time to midnight of the next day.

"Scan" Menu: The Scan Menu shows programming schedules for all channels from the current time to midnight on the following day.

"Sort" Menu: The Sort Menu lets you browse programs by category. The channel you are currently tuned to is displayed in the video window and by name.

Obtaining More Information

If an information icon appears in the program information, additional information is available about that program by pressing INFO. This feature is available in all four menus. Even if the icon isn't displayed, pressing INFO will show a PlusCode which allows you to program your VCR to record using VCR Plus+. Press INFO a second time to return to the TV Guide Plus+ menu.

Customizing The Channel Listing

You may customize the channel listing by enabling or disabling the display of certain channels. For instance, you may disable channels that you never watch. You can restore disabled channels at a later point in time, of course.

One Touch Recording

TV Guide Plus+ allows one touch recording if you have connected the IR controller to your VCR.

Recording Options

DAILY records the same program Monday through Friday. *ONCE* records only on that day. *WEEKLY* records the program each week at the same time. *REVIEW* displays a list of programs set to be recorded. You may delete programs from this list.

Troubleshooting

Blank Screen

- Check that device is connected to the input jacks is turned on.
- Try another channel.
- Press RESET, in case the picture controls are set too low.

No Sound, Picture Okay

- Check that sound is not muted. Try pressing volume up button to restore sound.
- Check that speakers are not turned off. Check the Audio Output and Speakers control panel in the Audio menu.
- If using an S-VHS component, remember to also connect the component's L and R AUDIO OUT jacks to the
- TV's L and R INPUT 1 jacks.

Can't Select Desired Channel

- Channel may be blocked or not approved in the Parental Controls menu.
- If using a VCR, check to make sure the TV/VCR switch on the VCR is in the correct position.

Noisy Stereo Reception

- May be a weak station. Use SOUND button to change to mono mode instead of stereo.

No Picture, No Sound but TV is on

- Maybe the cable/air function is set to the wrong position.
- Maybe a vacant channel is tuned.
- If watching VCR (connected only through antenna input), make sure TV is tuned to channel 3 or 4 – same as
- CH3/4 switch on VCR. Also check to make sure TV/VCR switch on VCR is in correct position.

Sound Okay, Poor Picture

- Check antenna connections.
- Try adjusting sharpness function to improve weak signals.

Black Box Appears on the Screen

- Captioning may be turned on. Check the Closed-Caption Display control panel in the Channel menu.

TV Guide Plus+ IR Controllers Not Working

- Check to make sure the controllers are positioned correctly over the IR remote sensors.
- Your remote may be interfering with the IR controller. Place a piece of dark tape over the IR controller.
- TV Guide Plus+ control of cable box is slower than direct control of the box itself. Keep this in mind when changing channels.

TV Guide Plus+ Cable Box Codes

ABC..... 22,46,53,54
Anvision 07,08
Cablestar 07,08
Cheyenne 81
Diamond 56
Eagle 07,08
Eastern Int. 02
General Instruments ... 46,92,93,94
GI 400 04,05,15,23,24,25,30,36
Hamlin 03,12,13,34,48
Hitachi 37,43,46
Jerrold 04,05,15,23,24,25,30,
..... 36,45,46,47,62,65
Macom 37,43
Magnavox 07,08,19,21,26,28,
..... 29,32,33,40,41
NSC 09
Oak 01,16,38
Oak Sigma 16
Panasonic 03,27,39,61
Philips 07,08,19,21,26,28,
..... 29,32,33,40,41
Pioneer 18,20,44
RCA..... 00,27,66
Realistic 84
Regency 02,33
Samsung..... 44
Sci. Atlanta 03,22,35,63,64
Signature 46
Sprucer 27
Starcom 46
Stargate 2000 58
Sylvania 11,59
Teknika 06
Texscan 10,11,59
Tocom..... 17,21,49,50,55
Unika 31,32,41
Universal 51,52,60
Viewstar 07,08,19,21,26,28,
..... 29,32,33,40,41
Warner Amex..... 44
Zenith 14,42,57,61

TV Guide Plus+ VCR Codes

Admiral 06,79
Aiwa 15
Akai 03,17,22,23,63,66
Audio Dynamics 14,16
Bell&Howell 02
Broksonic 10
Candle 07,09,13,44,
..... 45,46,52
Cannon..... 08,53
Capehart 01
Citizen 07,09,13,44,
..... 45,46,52
Colortyme 14
Craig 07,12
Curtis-Mathes 00,07,08,14,
..... 15,44,46,53,64,67
Daewoo..... 13,45,52,76
DBX 14,16
Dimensia 00
Dynatech 15
Electrohome 27
Emerson 08,09,10,13,15,20,23,
..... 27,34,41,42,47,49,
..... 57,62,65,67,68,70
Fisher 02,12,18,19,43,48,58
Funai 15
GE 00,07,08,32,37,53
Goldstar 09,14,46,60
Harman Kardon 14
Hitachi 05,15,35,36
Instant Replay 08

PTV Digital Convergence Overview

Beginning with the CTC195, convergence will no longer be done by physically tweaking pincushion controls. Instead, an internally generated crosshatch pattern can be displayed on-screen and the technician is able to access 195 points across the screen adjusting the red, green and blue, horizontal and vertical lines where they intersect those points via software control. The range of adjustment of these cross points affects only the immediate linear area and provides enough "play" to move the line about half the size of the box in either the vertical or horizontal direction.

Digital Convergence (DigiCon) decreases not only the material cost of convergence circuitry, but allows factory setup in about 5% of the time previously required. Convergence becomes more consistent and also more accurate. From prior techniques, where converging a set had become almost an "art" to accomplish, convergence has been taken to a more exact alignment, replacing potentiometers and "tweaking" with digital registers and "incrementing". The control interaction with each other is very small.

Centering geometry for the consumer is provided to correct for physical location in the Earth's magnetic field. Geometry and convergence are provided to the service technician to facilitate correction of small convergence errors in a large number of locations across the screen.

The digital convergence system, shown in simplified form by Figure 15-1, uses a single convergence IC, a dedicated digital convergence EEPROM, separate convergence yokes and associated driver circuitry to allow a large number of convergence alignment points, each independently adjustable. Geometry and convergence both benefit.

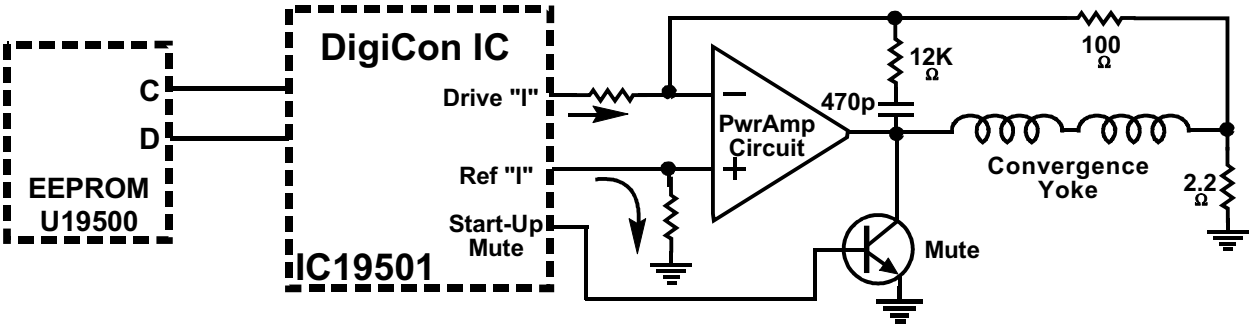


Figure 15-1, Simplified Digital Convergence Block Diagram

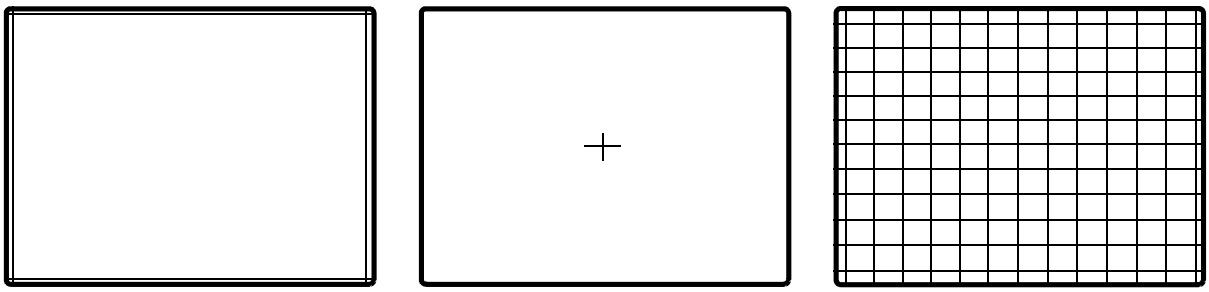


Figure 15-2, Digital Convergence Patterns

Circuit Description

The Digital Convergence system generates 6 convergence yoke drive signals that correct the geometry of the 3 rasters from the projection CRT's in the horizontal and vertical direction such that they are rectilinear and convergent on the PTV screen. Each of the three colors includes a matrix of 13 vertical points by 16 horizontal points (208 convergence points) stored in nonvolatile digital memory. This information is converted by the DigiCon IC digital-to-analog converters (DAC's) into 6 analog signals (horizontal and vertical for each of the three CRT's) that are power amplified to supply the drive current for the convergence yokes. Since there are only 13 horizontal lines defining the entire vertical scan, signals for scan lines that are between the adjustment point convergence lines are calculated by the IC using linear interpolation.

In the horizontal direction the IC output becomes digital steps that are smoothed by low pass filtering. An additional matrix with 6 bit resolution supplies a vertical signal for dynamic focus correction. All data values are adjustable via I^2C bus commands. Each data point can be individually changed (dynamic adjustment) or the entire raster of a color may be moved (static adjustment). Static adjustment of green, red and blue by the customer is used to partially correct the misconverging effects of the Earth’s magnetic field. Three different video test patterns are generated by the digital convergence IC to aid in the customer and service adjustments. Customer patterns consist of a green boundary frame used to center the pattern and a crosshair pattern used to center the red and blue CRT's to the green. Technicians have access to a digital convergence alignment pattern. All three are shown in figure 15-2.

The green boundary and crosshair patterns are accessible from the customer convergence menu and are known as "static" convergence correction. This mode gives the user horizontal and vertical movement of the green, red and blue rasters for the purpose of eliminating raster displacement due to changes in the Earth's magnetic influence on the set. The green boundary is used to center the raster and the red and blue crosshairs are used to align the red and blue rasters to the green.

The convergence alignment pattern, accessible only by the technician, provides adjustment of the digital convergence points as indicated by a yellow cursor for the red adjustment and a cyan cursor for blue adjustments. From the front panel, no access is provided to the green pattern, only the red and blue. They are aligned to the green pattern. This is because the green pattern is used to compensate for a phenomenon known as "banding" (more on banding later). The anti-banding compensation would be irretrievably lost if the green convergence adjustment points were changed.

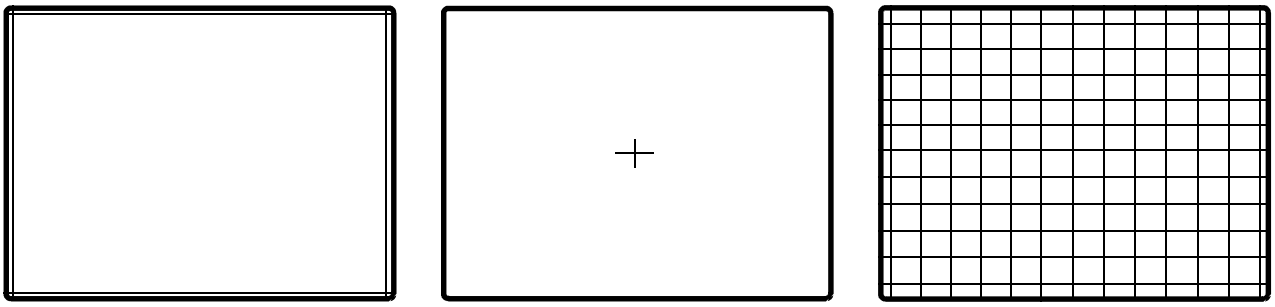


Figure 15-2 (Repeated), Digital Convergence Patterns

A "clean" modulated video signal input is required during any time the digital convergence pattern is on-screen. The DigiCon IC does not generate sync signals and must use the sync from incoming video for stability.

Geometry and/or convergence adjustment is required for the initial factory setup, when a major component is replaced or when the set is moved to a different magnetic field. A fully automated convergence system called the "Vision System", consisting of a high resolution camera and computer controller, will be used to initially determine proper geometry and the convergence data values. Tolerances from the manufacturing point are stringent and consistent over a wide spectrum of screen sizes. For field servicing, Chipper Check, operating on a PC platform, will be used to accomplish convergence alignments after any catastrophic failure of components that directly affect convergence. All geometry and convergence controls will also be available via Chipper Check computer controls.

There are two aspects of the DigiCon System that must be understood by the technician in order to competently troubleshoot and align the set. They are the circuit descriptions and alignment procedures. In most cases component failure and replacement will be followed by alignment procedures. The technician must understand the purpose of the circuitry in order to accomplish proper alignment at the completion of the repair. A circuit description is presented, with complete alignment procedures following.

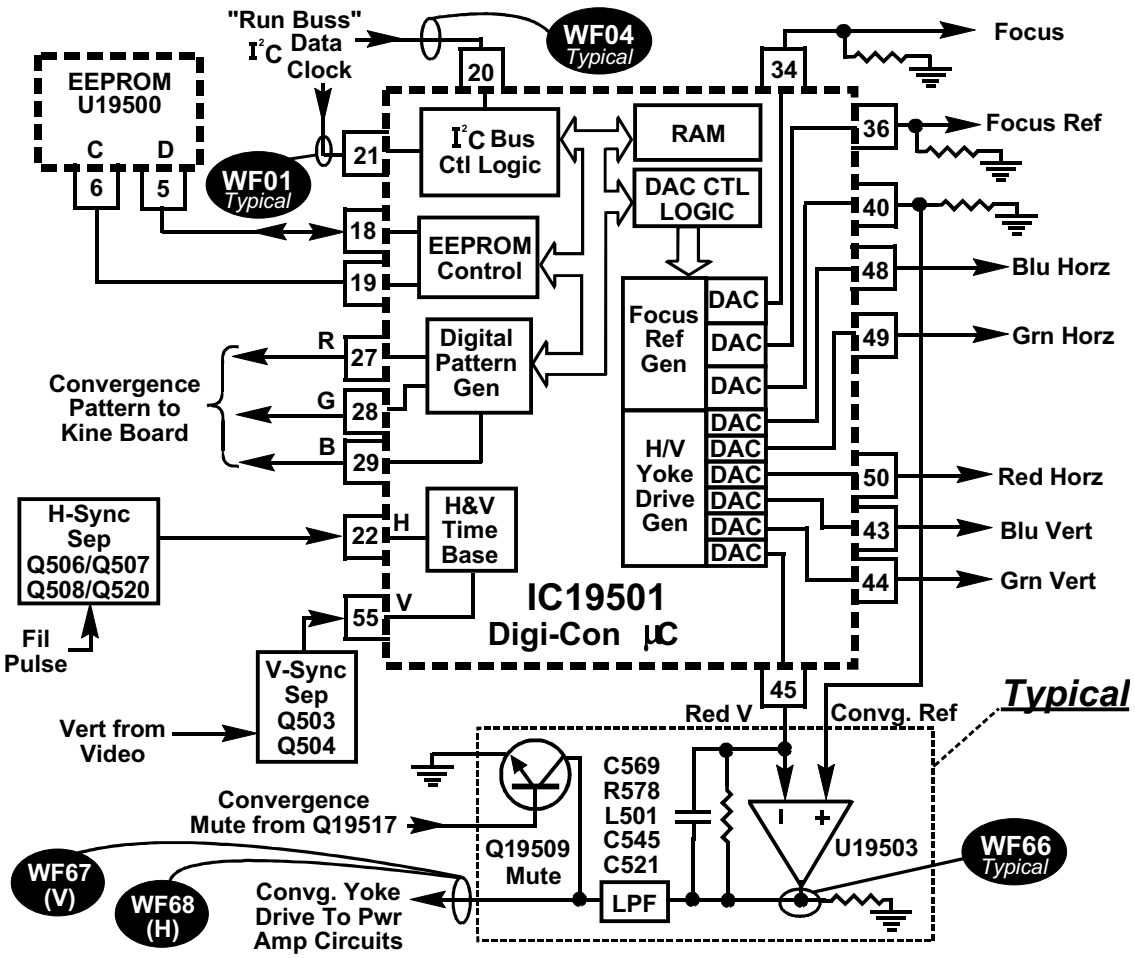


Figure 15-3, Digital Convergence Block Diagram

Digital Convergence Circuit

The Digital Convergence System shown in figure 15-3 uses a single integrated circuit, IC19501, and a serial EEPROM IC, U19500. The DigiCon IC is directly connected to the I²C bus, but the EEPROM is connected only to the DigiCon IC. This means all control is accomplished from the main microprocessor, but when values of alignments are changed, the DigiCon IC must do the reading and writing to the DigiCon EEPROM.

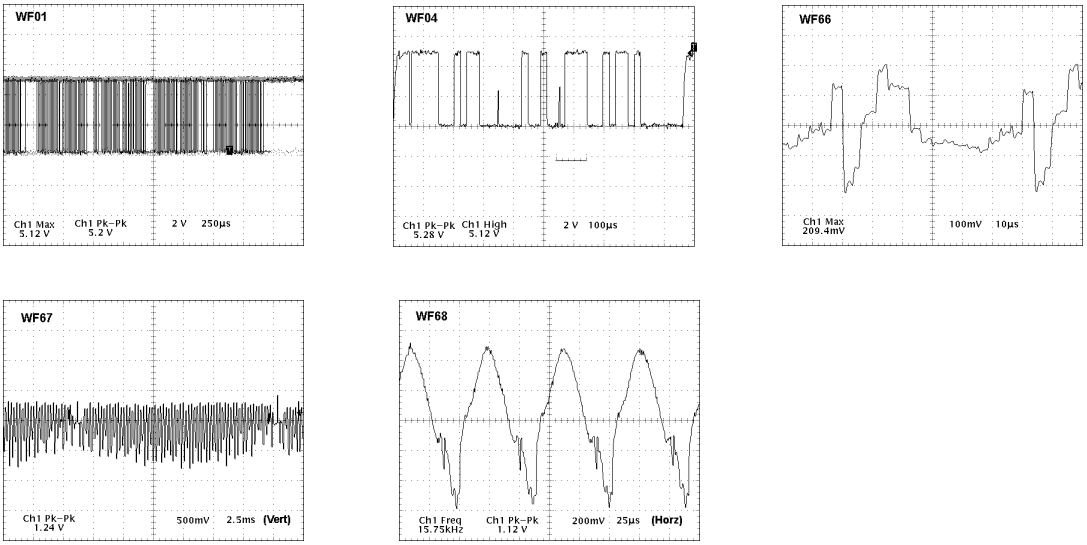
The DigiCon IC controls all functions of the DigiCon System. There is an internal pattern generator to supply the three video patterns required during consumer and technician level alignments. The pattern is output from pins 27, 28 and 29 through buffers, to the video input of the CRT drivers on the Kine Socket boards. It receives horizontal and vertical sync information from the sync separator circuits via pins 22 and 55.

An additional D/A provides a correction signal for vertical dynamic focus from pin 34. This signal is amplified and added to a horizontal dynamic focus correction signal from a current transformer that transforms horizontal deflection yoke current.

Pin 26 is used to monitor the +5V and ±15V convergence power supply voltages. If the current draw exceeds safe limits, the DigiCon IC will adjust the DAC outputs to reduce the output transistor current draw to zero.

It should be noted that pin 26 monitors only the total current draw of the power supply, not individual output devices. If any output device fails, the IC will act to shut down all current draw, making troubleshooting difficult. However, operation for troubleshooting efforts can usually be restored by unplugging one or more of the convergence yokes and cycling the TV on and off.

Also, as the IC monitors this voltage, if it drops too low, the outputs of the DAC's are lowered to decrease current flow in the convergence yoke output transistors. This prevents any overcurrent conditions due to improper power supply voltages. The voltage is also monitored during power up cycles and a mute voltage sent to the power amplifiers. This guards against excessive power supply drain during the start up period when the DigiCon IC RAM may have incorrect data but is being loaded with proper data from the DigiCon EEPROM.



Digital Convergence Waveforms

Convergence Yoke Drivers

There are six yoke drive outputs from the IC; one each for the horizontal and vertical convergence yokes for each color. The output pins are 43, 44 and 45 for the red, green and blue vertical drives and pins 48, 49 and 50 for the red, green and blue horizontal drives. The six circuits and their output devices function identically. The DAC outputs are connected to an op-amp predriver (shown in Figure 15-3) which in turn provides drive to the differential amplifiers, Q19300/ Q19301. The output from this pair drive Q19304 which drives the main output devices, Q19306/Q19307. The outputs are connected to the digital convergence yokes. The entire amplifier line is direct coupled and forms a tightly closed-loop servo system. Because the output is current driven, waveforms may be very difficult to distinguish. Yoke current feedback is monitored by R19301 and Q19301. If yoke current increases, the voltage across R19301 increases causing more current to be drawn through Q19301. This causes the emitter voltage to increase (towards the +45V supply) decreasing current flow through the class A driver, Q19300.

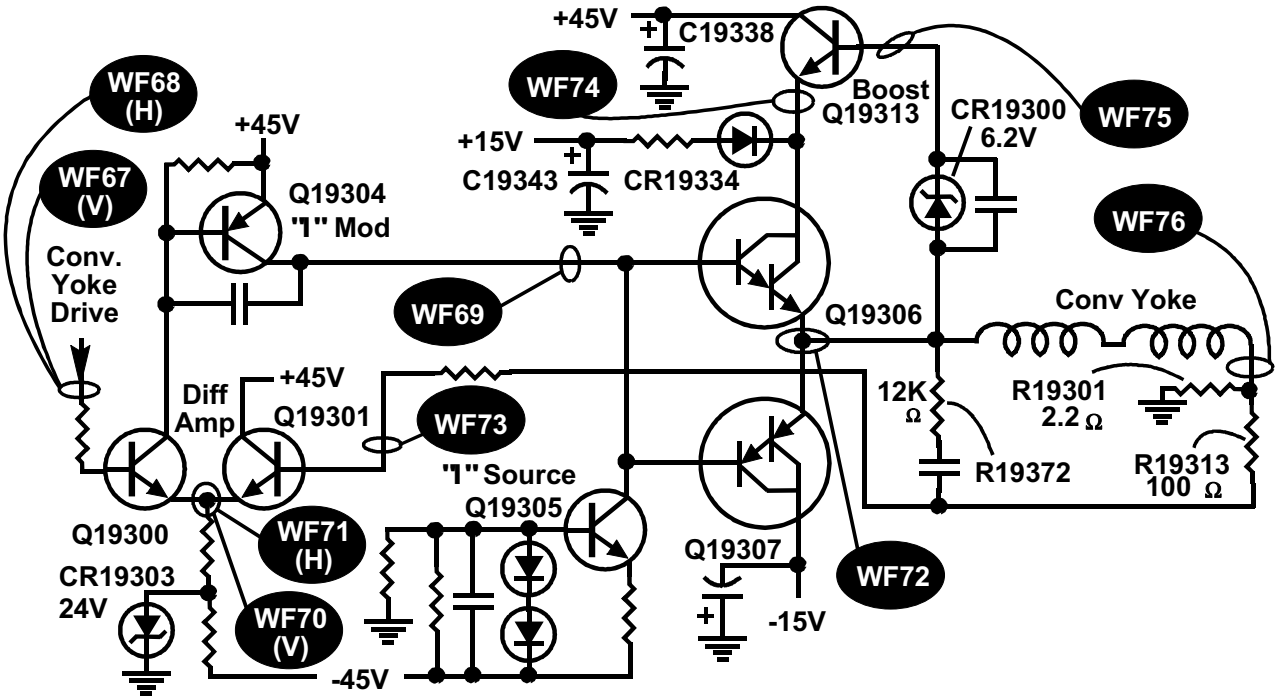
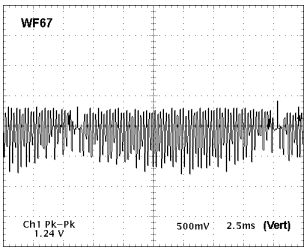
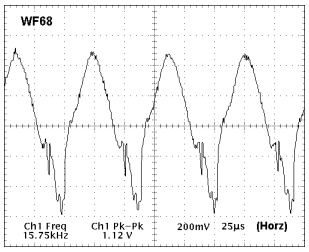
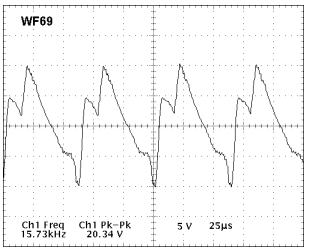
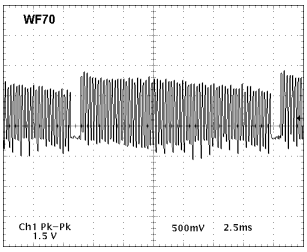


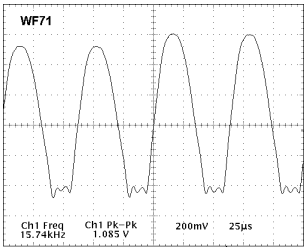
Figure 15-4, Convergence Yoke Drivers

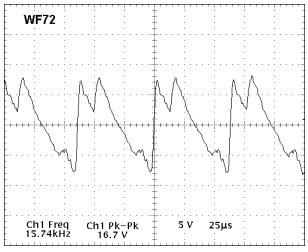


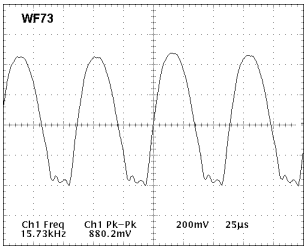


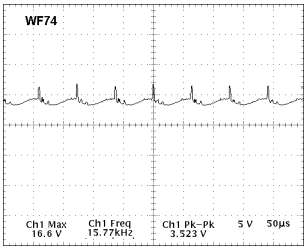


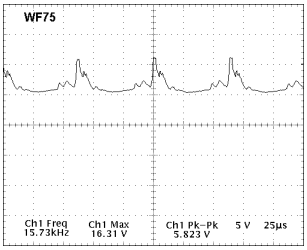


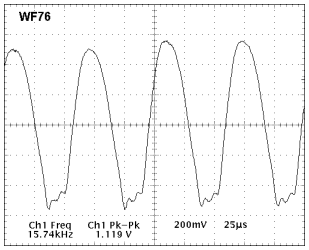












Convergence Power Amp Waveforms

As the emitter voltage increases, the collector drive signal to Q19304 decreases and the collector voltage decreases. This begins decreasing the base drive to the output darlington amplifiers, which in turn decreases their output. The whole exercise is to keep the current in the yoke very tightly controlled and a nearly exact replica of the input voltage at the base of Q19300. The voltage at the amplifier input, Q19300, is compared to the voltage across the yoke current sense resistor R19301 via Q19301 and any error is minimized by the gain and speed of Q19304, Q19306 & Q19307. During fast input signal changes, very high transient “boost” voltages are required across the yoke coil to maintain the same speed of change in the yoke current. All of the vertical amplifiers and some of the horizontal amplifiers require extra high “boost” voltages to obtain the required speed of yoke current change. These amplifiers incorporate extra “boost” transistors such as Q19313 that switch on a higher voltage when it is required. This arrangement saves power and heat in the output Darlington transistors Q19307 & Q19307. On the screen this is seen by the way each adjustment of the DigiCon controls interfere as little as possible with the lines prior and after the adjustment point.

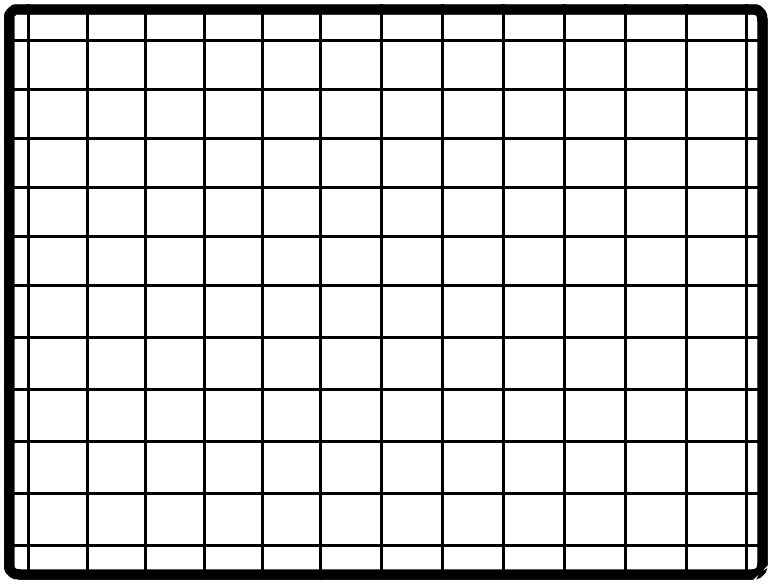


Figure 15-5, Digital Convergence Pattern

Crosspoint Adjustments

The 13 vertical and 15 horizontal lines generated by the DigiCon IC, cross at right angles to each other on the screen. This 13 by 15 matrix of adjustment points, shown in Figure 15-5, is where the convergence yoke centers its influence. The video pattern provides a convenient location reference for adjustments. On initial power up, transistor switches mute (greatly reduce) the outputs of the convergence power transistors while the contents of the EEPROM memory are transferred to a RAM memory in the convergence IC. This communication is over a dedicated I^2C bus that is mastered by the DigiCon IC. Using a separate bus helps to prevent memory contamination from kine arcs or other voltage variations. A second I^2C bus allows the convergence IC to be adjusted as a slave of the main chassis microprocessor (refer to "System Control") in the projection instrument.

The convergence IC supplies horizontal and vertical convergence signals for each of the three colors. These signals originate from the convergence IC digital to analog converters. Vertical signals have 12 bit resolution. Horizontal signals have 10 bit resolution.

For each convergence signal (red, green and blue), the horizontal line in a picture field has 16 periods of constant output from the D/A. These are smoothed by the low pass filter. The signal is then power amplified and sent as a current to the convergence yoke coil. In the vertical direction, scan lines between the adjustment lines are determined by linear interpolation. This helps to maintain a more acceptable spacing between the horizontal lines in the vertical direction. Squares look more like squares instead of rectangles. Because of interlacing, alternate fields add a correction to maintain vertical interlace. To prevent line density modulation (banding) of the raster, the vertical corrections are linearized in the initial factory alignment. In field service, Chipper Check will be required to reset the vertical corrections.

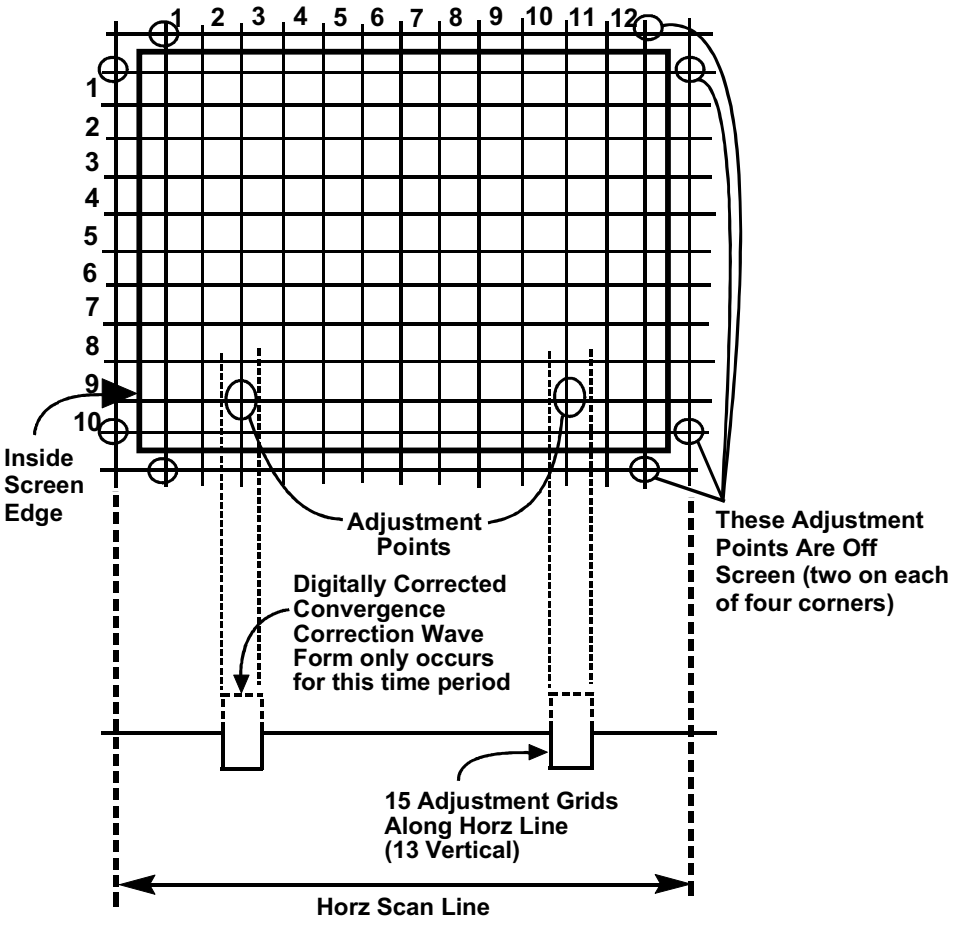


Figure 15-6, Yoke Effect on DigiCon Pattern

Front Panel Service Mode

If Chipper Check is not being used, the instrument may still be converged via the front panel controls and the IR remote control. Adjustments via menu 76 may be used for minor geometry corrections of up to +/- 2 adjustment steps as long as the DigiCon EEPROM has not been replaced. When major components are changed, Chipper Check must be used to return the set to optimum performance.

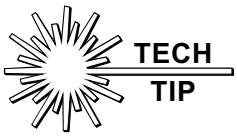
The front panel service mode allows the adjustment of the digital convergence cursor and the setting of data for the 195 dynamic alignment points where the horizontal and vertical lines cross each other. Many of these alignment points are 1/2 square off the screen making them not totally viewable, however, they may still be adjusted so that the convergence can be corrected out to the farthest viewable edge of the screen. This allows the adjustment of the 1/2 line (horizontal & vertical) that trails off on the edge of the pattern. This service mode is intended for final “touch up” only (corrections of up to +/- 10 steps) and can be performed (by the technician) using the front panel service screens (menu #80) and the remote hand unit .

The main micro fetches and holds the current setting of a cursor point from the RAM of the digital convergence IC, modifies it and then writes it back to the RAM. The main micro needs only to retain a few bytes during this operation.. From the perspective of the main micro, the digital convergence IC looks like a large RAM chip which can be accessed and modified via the I^2C bus.

Remote Control Service Functions

Although service mode must be entered from the front panel, it is not advisable to make convergence adjustments from this viewing position. The directional gain in the screen does not permit a service person using the front panel mounted controls to clearly see the picture detail. The remote control should be used for all adjustments and the technician should stand at a position enabling a clear view of the screen detail during adjustments.

When the chassis is in service mode the following remote control functions are enabled:



Prior to entering the service mode, a channel with clean signal, or a good video signal on the aux input line must be selected to provide sync.

Service mode is accessed via a security code entered from the front panel.

Press and Hold MENU; Press and Release PWR, then press VOL DN; Release MENU and VOL DN at the same time. On either the remote control or the front panel buttons use VOL UP to advance the right side screen number (V:) to 80. Then push CH UP.

In service mode undefined buttons do nothing.

The display will have incoming video blanked and be the digital convergence crosshatch pattern with a small YELLOW centered cursor. At this time, red will be adjustable. Green is fixed.

The volume and channel buttons will move the cursor (indicating the selected adjustment point) up, down, left and right in single steps. Only a portion of the cursor will be seen when the cursor is positioned to adjust the off-screen points along the picture edges. Use the small line segments that extend to the picture edge to adjust these points.

NOTE: In the extreme corners, the cursor is invisible but the point is still adjustable. Do not adjust these off-screen corner points. The cursor movement does not “wrap around” left to right or top to bottom.

For best results, adjust the pattern beginning at the upper left of the screen. Then continue the adjustments from left to right and top to bottom as if reading a book.

The four navigation "MOVE" buttons adjust the movement of the selected color at the cursor point. They will move the color up, down, right or left. Adjust the selected color so that it is centered on green with minimum fringing on either side.

The "INFO" or “DISPLAY” button will toggle the display between these 2 states:

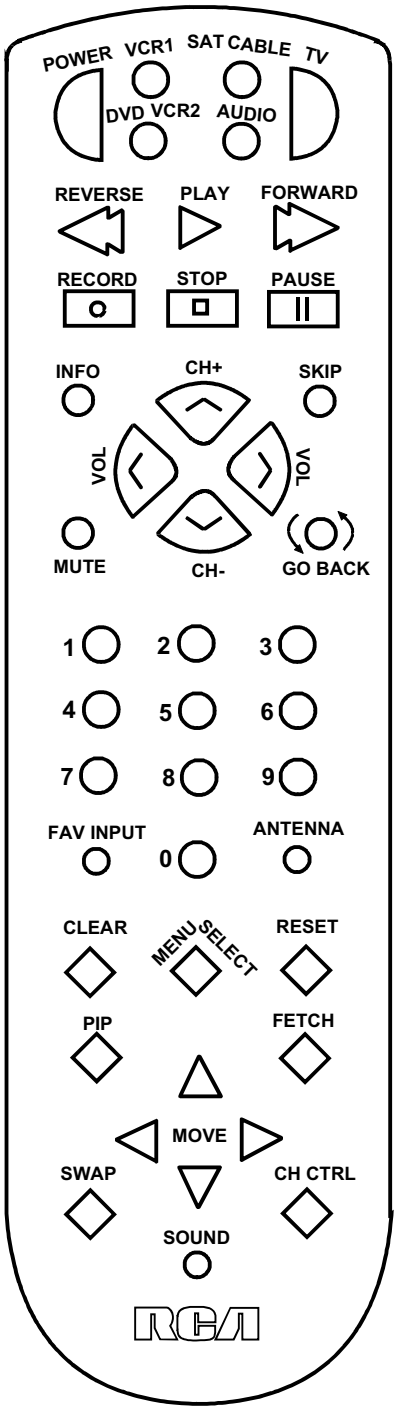


Figure 15-7, CRK70 Remote Control

1. White crosshatch, Yellow cursor, Red adjustment, no other OSD or video.
2. White crosshatch, Cyan cursor, Blue adjustment, no other OSD or video.

The PWR button returns the receiver to normal operation and commands the DigiCon IC to write the contents of its RAM to the DigiCon EEPROM. The digital convergence IC takes about 2 seconds to download all the RAM values to the EEPROM.

Convergence and Alignment Specifications

These specifications are for the maximum allowable horizontal or vertical distance between the RED, GREEN & BLUE digital convergence pattern line centers and ideal geometry on the screen at the digital convergence adjustment points. Either the English or Metric limits may be used but not a mixture.

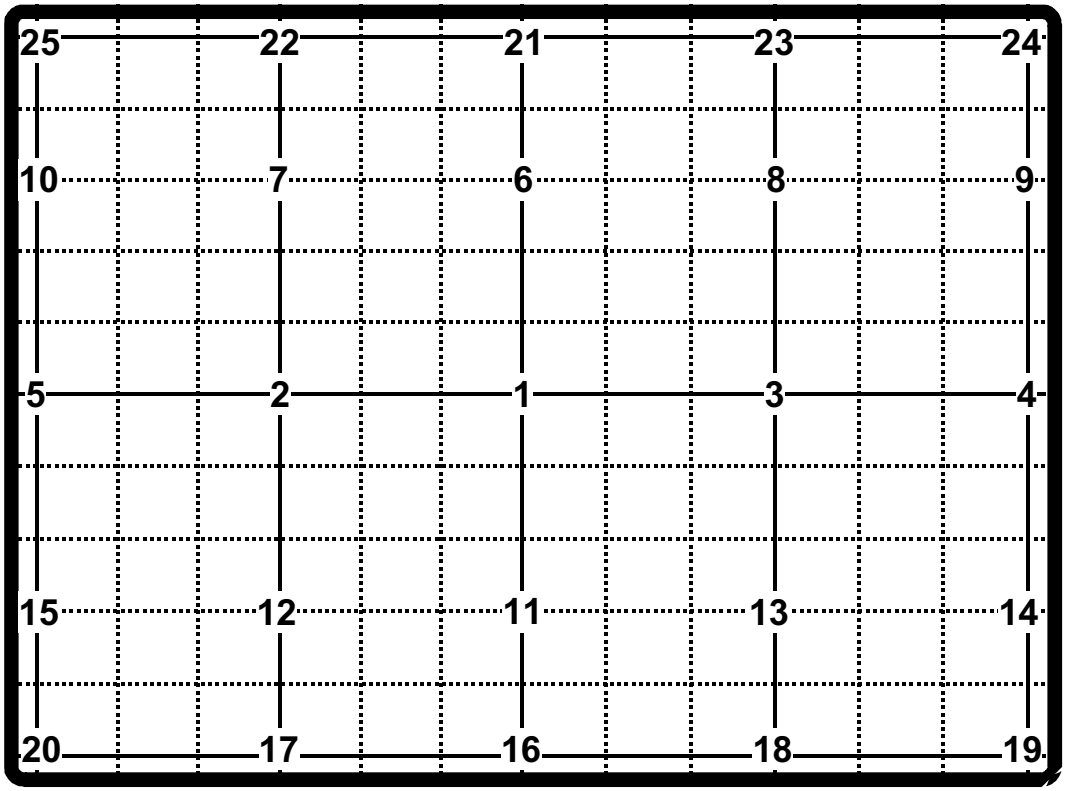


Figure 15-8, Alignment Steps

In field service or factory convergence, when Chipper Check and a PC computer are used, adjustment points 1 through 25 are adjusted, for each color, in ascending order beginning with green, then progressing to red, then blue until, on a 46" screen, all are within +/- 0.04" (+/- 1 mm) of ideal geometry. For green, this would be the ideal geometry pattern. For blue and red, it would be ideal convergence to the green pattern. The positions of all pints not adjusted are calculated and placed by the computer. All points should then be within +/- 0.12" (+/-3 mm) of ideal geometry.

To minimize line density modulation (banding), points 6-10 and 11-15 of the green vertical pattern are not adjusted. These points are calculated and placed by the software.

R/B, R/G and G/B errors greater than 0.1" (2.5 mm) may then be reduced to 0.1" (2.5mm) or less via point by point adjustment. If another screen size is used the tolerances change in proportion to the ratio of the new screen size to 46". A screen size ratio is shown in Figure 15-9.

SIZE	RATIO
42"	.91
46"	1.00
50"	1.09
52"	1.13
56"	1.22
60"	1.30
61"	1.33
80"	1.74

Figure 15-9, Screen Ratios

DigiCon Service

The DigiCon convergence board output amplifiers are direct coupled. When a component in one of the amplifiers fails, the DigiCon power supply, monitoring output current, shuts down and convergence turns off. The problem is flagged by an error code read by the system control micro on the main chassis. The error code only indicates that there is a problem in the DigiCon power supply or DigiCon circuit, not what that problem might be. To troubleshoot, unplug the power supply from DigiCon board, start the set and check the DigiCon power supply outputs. If they are OK, go to the DigiCon board. The method used to troubleshoot the DigiCon board is very similar to troubleshooting a switch mode power supply. Check for any damaged or burnt devices first. Ohm check discrete devices, looking for an open or shorted component. It is very important to check all possible components for failures before powering up the DigiCon. If one failed component is overlooked, it could very well cause any components already replaced to fail again. Similar to direct coupled audio amplifiers, one failed component can cause cascade failure of an entire circuit. Attempts to defeat the power supply shut down circuits or jump start the system with an external supply may cause further component failures. Disconnect the convergence yokes and power up the DigiCon board. Check the power supplies for normal operation and check for normal convergence signals at the convergence power amplifier inputs. The convergence IC will not work unless there is +5V at pins 2, 4, 5, 13, 24, 26, 35, 41, 46, 51 & 53, HSync at pin 22, Vsync at pin 55, 0V at pin 25, approximately 1V at pin 40 and an 8.5 MHz square wave at pin 14. Repair any problems or marginal components that are found. If everything seems normal, plug in one convergence yoke at a time. Watch for distortion in the pattern on the screen or for a power shut down. Either may be an amplifier fault. An amplifier test pattern is supplied with Chipper Check. This allows the transient behavior of the 6 amplifiers to be viewed.

T-Chip Alignment

All basic chassis geometry data needed by the T4 chip is stored in the Main EEPROM. If the T4 chip fails and the EEPROM data is not corrupted, replace only the T4. A complete alignment of chassis geometry should not be necessary. A touch-up of screen geometry using the chassis alignments in menu 76 (Limit adjustments to +/- 2 steps. If more adjustment is required, use Chipper Check to do a complete alignment) and the convergence using alignments in menu 80 should be sufficient to bring the set back to specifications.

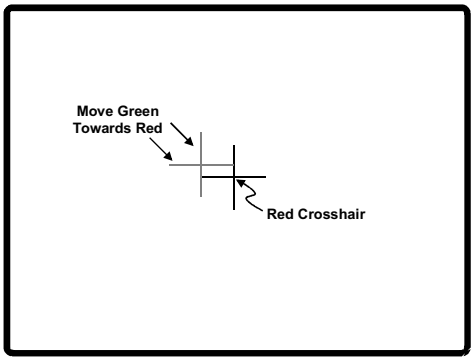
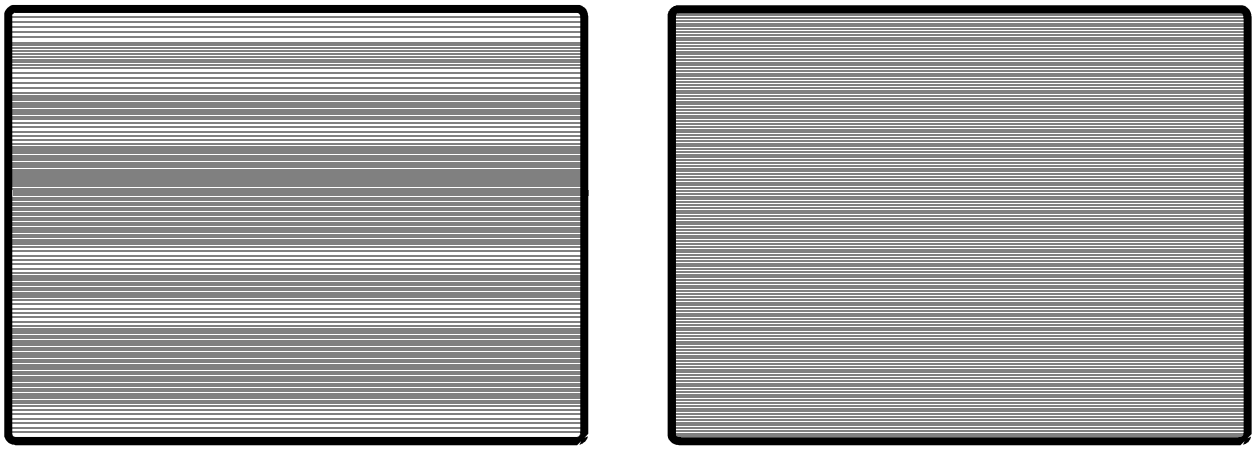


Figure 15-10, Aligning Green to Red

If a green tube (worst case scenario) is replaced, activate the red customer centering pattern (the "+" in the middle of the screen) and use the green centering rings on the CRT to align the green gun back to the red pattern. At this point, size the pattern using menu 76 alignments and perform a general touch-up of convergence using menu 80. This should bring the set back close to specs, if it does not, a complete chassis geometry and convergence procedure may have to be done using Chipper Check. This assumes that the set was correctly converged to begin with and that no other major components were replaced.



Without Anti-Banding *With Anti-Banding*

Figure 15-11, Screen Appearance with and without Anti-Banding

Banding

Banding is caused when the spacing of the regularly spaced scan lines of the raster abruptly changes along a horizontal digital convergence alignment line. See Figure 15-11. Scan lines close together appear brighter than scan lines spread apart and an abrupt change in spacing is very visible. To minimize the appearance of banding, the Chipper Check program that adjusts green vertical, calculates the values so as to achieve minimum geometric distortion without abrupt changes in scan line spacing at the digital convergence alignment lines. When the Chipper Check software is used, banding is minimized. Point by point adjustment of green geometry is not available because banding would result. If green vertical is aligned for perfect vertical geometry, banding will occur near the top and bottom of the raster. If green vertical correction is linear (i.e. each correction in the series along a column is incremented by the same amount) banding does not occur but the resulting picture may be distorted in the vertical pin. The Chipper Check software and the factory Vision Alignment machine software compromise between these extremes so that banding and pin distortion are minimized.

When the set is first aligned with the factory Vision System, the top, center and bottom horizontal reference lines are placed at exact locations as determined by the picture taken by the camera. Then the DigiCon IC makes its calculations. The results are placed in the DigiCon EEPROM. Anti-banding calculations involve only the green CRT. The red and blue CRT's are then aligned to the green pattern. As long as this information remains intact, there should not be any reason to worry about the anti-banding. However, if an EEPROM becomes corrupt, requiring replacement, it becomes necessary to use Chipper Check to perform a complete alignment.

Digital Convergence Failure

The red/green/blue geometry is aligned at the point of manufacture to very close tolerances and at more on-screen locations than the service technician will be able to replicate in the field. Unless catastrophic failure of the digital convergence IC's or a CRT failure occurs, the field technician will not have to do any major geometry alignments. If green alignment becomes necessary, Chipper Check will allow geometry to be restored to a condition closely approximating the original factory alignment. Placing markers on the screen will provide the technician with an accurate geometry reference.

CRT Replacement

Physical replacement of the CRT's in the CTC195 is straightforward, posing no new problems to the service technician. Once a tube is replaced, the yoke rotation and centering rings should be adjusted to align the new tube to the remaining tubes. A crosshatch pattern fed to the video input, is useful in this alignment. Check the electrical focus, lens focus and screen settings. Check the picture geometry and distortion using menu 76. If there is visible picture distortion, realign via menu 76 limiting the changes to about +/-2 steps. For severe cases requiring changes in excess of +/- 2 steps use Chipper Check. Usually the geometry and picture distortion will be good enough so that only minimum touchup geometry alignment will be needed and use of menu 80 will be sufficient to converge red and blue to green.

If complete geometry adjustment becomes necessary, Chipper Check uses the placement or location of three green horizontal lines (top/bottom and middle) along with five vertical lines to calculate the exact location of the remaining horizontal and vertical lines. The technician must adjust or place these eight reference, or base, lines manually in the correct position through the use of Chipper Check and the alignment aid described earlier (placement of horizontal and vertical strings or lines in a given pattern).

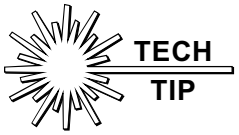
Unless a DigiCon or main chassis EEPROM is replaced, when performing any type of service, if the “green consumer frame” is OK (or close) no major readjustment of the convergence or chassis geometry should be necessary. The only requirement might be some minor touch-up of convergence using service menu 80, or Chipper Check, to bring the set back to acceptable specifications. This is a judgment call on the acceptability of the green consumer frame and the appearance of the video.

The two service situations that could arise that would “mandate” the use of Chipper Check are the replacement of the main EEPROM or the failure of the DigiCon EEPROM. The replacement of either of these devices dictates that Chipper Check be used to bring instrument back to acceptable specifications. However, this does not mean that Chipper Check is not needed in other instances, only that it is absolutely necessary in those two circumstances. There may be other situations arise with service in other areas that would require Chipper Check, but again this would be a judgement call on the part of the technician as well as what the customer is willing to accept in the way of convergence performance.

Digital Convergence IC

Most components on the Digital Convergence Board may be replaced with only minor touchup of the convergence controls. If the digital convergence EEPROM is replaced, the factory alignment will be lost. In this case, Chipper Check will be needed to download a set of nominal factory alignment values, bringing the geometry back to where the technician will be able to begin the catastrophic failure alignment procedure. Since the CRT's have not been changed, it will be assumed they are still mechanically centered.

The screen must be marked for the alignment before beginning the procedure. Using the chart and measurements given by Chipper Check, 8 strings must be placed to mark the 25 alignment points.



HINT: Elastic string works best to minimize horizontal string sagging.

When the strings have been placed, use Chipper Check to align the green on-screen pattern to match the string marked pattern. Next align the red and blue patterns to green using the Chipper Check 25 point convergence program. When alignment is complete, final fine tuning of the pattern can be achieved by manually adjusting each crosspoint, either from front panel menu "80" or using the fine-alignment portion of Chipper Check. The 25 point convergence should always be performed first, so that fine adjustment is limited to about +/- 8 steps.

Convergence "Jumps"

Digital Convergence normally operates as a stand alone system that reads its own EEPROM and self coordinates at power up. Convergence is initially off for about 0.5 seconds to allow transfer of data from the EEPROM to RAM. When this process is complete, convergence output is activated. This action may cause a visible convergence “jump” after a power glitch which will not be seen at normal turn on due to picture tube warm up time. Convergence output is also deactivated and the picture is distorted when a circuit fault causes the convergence power supply voltages to be incorrect.

Troubleshooting (General)

Troubleshooting the digital convergence circuitry may be complex, but can always be resolved with the use of the proper tools and the application of some new theory. If discrete component failure occurs, a definite warp in the pin correction will be observed. Replacement of individual active or passive components, other than the DigiCon IC and EEPROM should not require anything other than a touchup of the digital convergence controls. There are five failure scenarios that may only be corrected with the use of Chipper Check software diagnostic programming. These are:

- CRT replacement,
- Digital Convergence microprocessor replacement,
- Digital Convergence EEPROM replacement,
- T4 Chip replacement,
- Main Chassis EEPROM replacement.

After any of these failures, proper alignment technique will bring the performance of the set back to factory specifications.

In order to perform these alignments, the technician must understand the differences between "convergence" and "geometry" adjustments and what the two affect.

Troubleshooting Geometry

Geometry adjustments are performed by the main chassis and affect the green, blue and red picture the same. Geometry adjustments are done in the T-chip by the main microprocessor and the alignments are stored in the main EEPROM. These adjustments directly affect yoke current to correct geometry. There are nine chassis geometry adjustments. Seven are available from the front panel. The same adjustments plus two additional* are available using Chipper Check. These are:

- Horizontal Size
- Vertical Size
- Vertical Centering
- East/West Pincushion
- Pincushion Amplitude
- Pincushion Top
- Pincushion Bottom
- Vertical 'S' *
- Vertical Linearity *

The controls and their affect on the geometry of the screen are shown if figure 15-12. Note that all controls are +/- meaning that the pattern is adjusted in two directions.

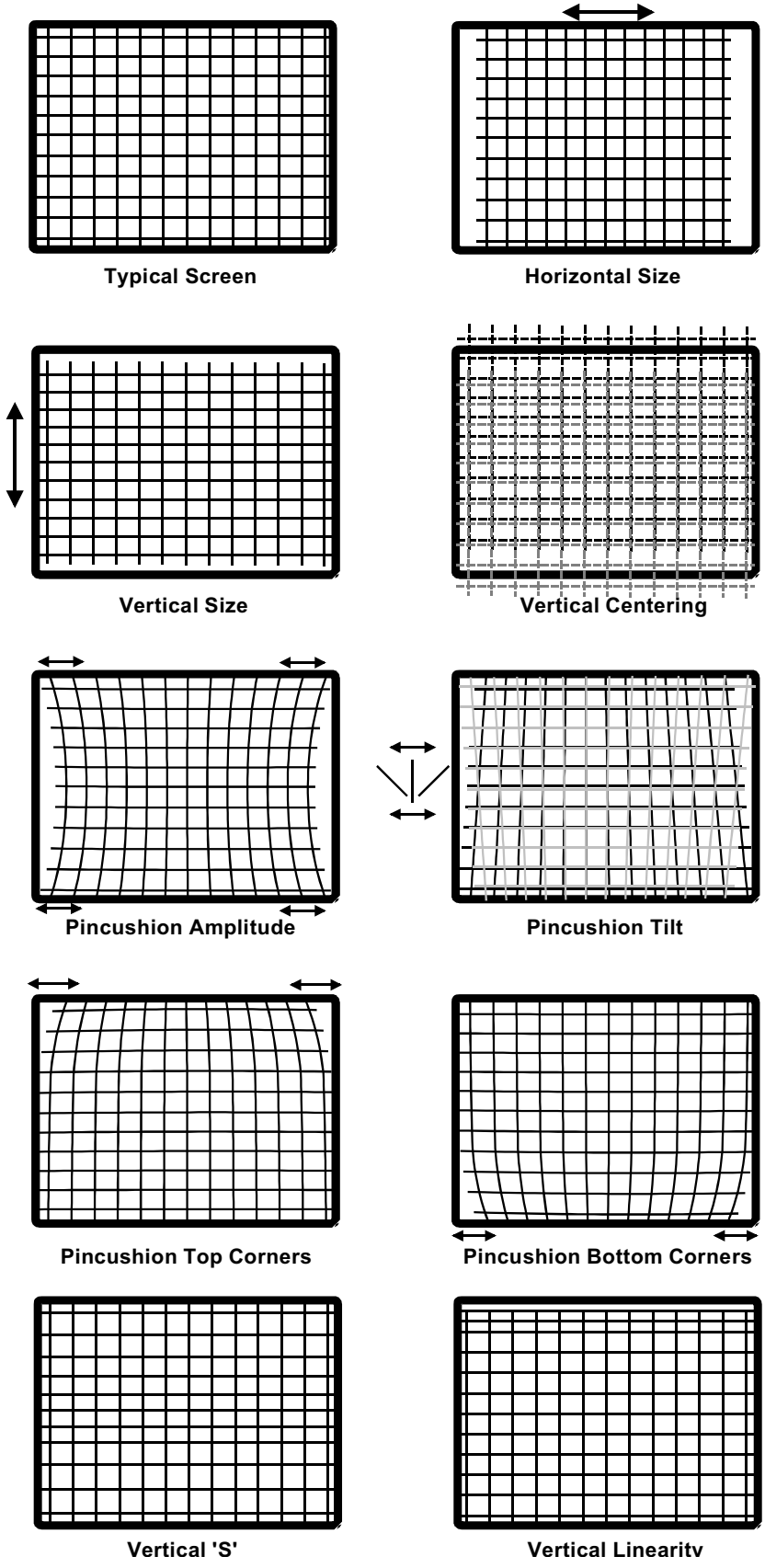
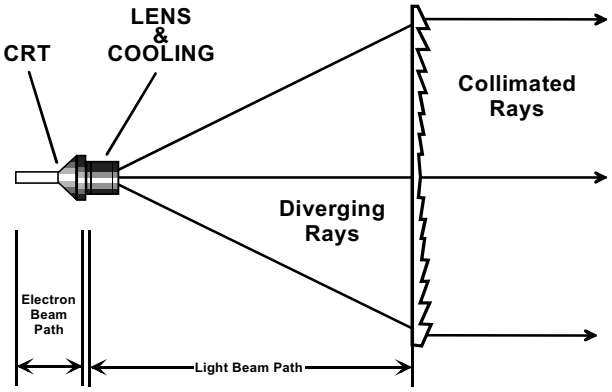


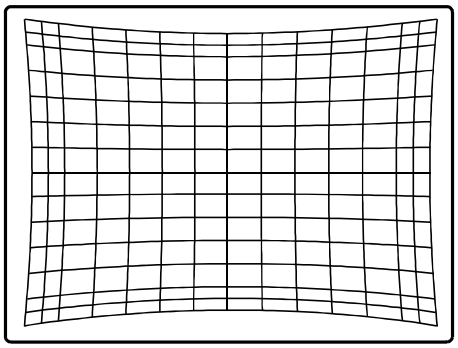
Figure 15-12, Geometry Screens

Troubleshooting Convergence

Digital Convergence affects the pattern by using separate electromagnets on the yoke assembly to "deflect" the beam differently for each of the three tubes so that the unique distortion of each tube is corrected. Think of convergence as the "fine-tuning" adjustment after the deflection yoke has placed a "course" adjustment on the beam pattern. In projection television the green tube makes a vertically shaped pincushion image on the screen. The red and blue tubes make opposing keystone shaped images also with vertical pincushion distortion. To optimize the optical design of the lens, projection tubes have spherical phosphor surfaces that curve inward toward the electron gun at the screen center. The beam striking the outer part of the tube phosphor screen must travel a much greater distance than the beam striking the center. This adds to the pincushion distortion and makes dynamic focusing necessary.



Projection Tube Beam Path



Alignment Pattern with no Convergence Correction

Figure 15-13, Geometry Pattern without Correction

Without any correction, for the green tube, this produces a pattern on the screen similar to Figure 15-13. The image on the tube phosphor surface is, depending on screen size, magnified as much as 6-10 times by the optics to form the final screen image. This makes any distortions that occur on the face of the CRT seem much greater to the viewer.

Figure 15-13 shows the beam path from a projection CRT to the screen and how the digital convergence alignment pattern would appear if no convergence correction were applied. This pattern can be (and is) used for chassis geometry, allowing the technician to use the chassis geometry controls to correct the pattern as much as possible. From this point, convergence correction must be used to square up the pattern.

CRT Replacement

CRT replacement may be broken down to the replacement of the center (green) CRT or one of the outer (red or blue) CRT's. At the manufacturing location special optical recognition equipment is used to not only center the geometry of the screen, but to align the three color patterns to each other. The optimized values of the digital convergence DAC outputs are then stored in the EEPROM. When any CRT is changed, not only are the electrical characteristics of the replacement CRT different from the tube that was replaced, but it would be almost impossible to place the new CRT back in the exact physical location of the old one. Therefore, some mechanical and electrical "tweaking" may be needed.

As previously stated, the ATE (Automated Test Equipment) fixtures used during manufacturing, key on the green CRT, performing an exact electrical centering adjustment on it. This can be done easily with optical recognition equipment. The red and blue CRT patterns are then placed "on top" of the green pattern. Since both the red and blue patterns depend upon the correct placement of the green, failure of the green CRT becomes the more critical problem. The only customer size and centering control that shows a full screen pattern for picture geometry is the green one. The remaining centering controls for the blue and red pattern require aligning them to the green one.

NOTE: The consumer centering patterns are made up of only two colors. The yellow crosshair consists of the green and red colors, and the cyan crosshair consists of the blue and green. If the blue or red CRT's are replaced, these crosshairs may be used to center the replaced tube. Center the customer range by running the control to its limits and averaging the difference. Chipper Check can do this more accurately by placing the center adjustments at 0. Use the centering rings on the CRT to center the center cross. This procedure preserves the customer adjustment range for later use and minimizes the power used by the convergence circuits. After the rings are set, "fine-tuning" with the digital (consumer) controls provided in the centering menu is acceptable as long as it is limited to +/- 5 steps. If the blue CRT is replaced, enter the blue consumer centering menu and center the blue controls. Then align the blue part of the cyan crosshair to the green using the blue CRT centering rings. If the red CRT is replaced, use the red centering menu to center the customer controls, then align the red crosshair to the green one using the red CRT centering rings.

The steps after replacement of the green CRT are:

1. Adjust the electrical and mechanical lens focus. Use the crosshatch pattern available from the convergence pattern displayed by entering the serviceman menu and selecting P:80.
2. Center the horizontal and vertical customer convergence controls in their range by:
   a. Using Chipper Check and moving the green centering buttons to the midrange value or,
   b. Using the green customer centering controls, move the centering pattern through its range, noting the limits, then choose an approximate center.
3. Return to the convergence alignment pattern at P:80 and align the green CRT rotation and centering rings to place the green pattern over the blue and red patterns.
4. Using the customer convergence menu for green centering, observe the border lines. The lines should be just inside the frame around the screen. A 70-80% accuracy for this border is acceptable. If not, adjust the pattern using the customer centering controls.
5. The size and geometry of the raster may be optimized using the T4 chip service adjustments. To access these adjustments, enter the service mode by using the front panel buttons.

6. Now use CH UP to increment the left side number bank to 5. The following table is the parameter (P:) number for the geometry adjustments. Table 15-14 shows the area of the screen that is affected by each adjustment parameter. Parameters 4 through 11 automatically bring up the convergence pattern for the adjustments. The pattern along with the outer frame of the set, is used to optimize chassis geometry.

Parameter	Description	Comments
4	Horizontal Phase of video to Deflection	Syncs incoming video to convergence patterns. Set at factory. Adjustment requires a video test pattern with an accurate vertical center line. The adjustment matches the position of the video vertical center line to the convergence pattern vertical center line. Chipper Check will be required to bring up the convergence pattern and video at the same time.
5	EW DC	Horizontal Size. This is adjusted with convergence off so that the outer most right and left convergence pattern lines at their intersection with the horizontal centerline are the same distance apart as the width of the visible area of the screen. The border lines will probably not line up with the viewable area with convergence off. Final size may be a matter of close estimation.
6	Pincushion Amplitude	Adjusts the straightness of the right and left outer border lines. Adjust for straight sides.
7	Pincushion Tilt	Affects angle of right and left border lines. Adjust for a straight vertical right side. ADJUST VERTICAL HEIGHT FIRST.
8	Pincushion Top Corners	Adjusts the curvature of the right and left border lines at the top corners. ADJUST VERTICAL HEIGHT FIRST.
9	Pincushion Bottom Corners	Adjusts the curvature of the right and left border lines at the bottom corners. ADJUST VERTICAL HEIGHT FIRST.
10	Vertical Centering	DO NOT ADJUST! This is set at the factory to minimize vertical deflection yoke current at video line 141. Use the CRT vertical centering rings to adjust vertical centering.
11	Vertical Size or Height	Adjust so that the outside edges of the top and bottom border lines at their intersections with the first full box from the outside edge of the pattern are the same distance apart as the height of the visible screen area. (See Figure 15-16)
Chipper Check Only	Vertical "S"	Adjust so that the size of the squares is uniform and equal along the vertical line, 2 lines to the right of the vertical centerline.
Chipper Check Only	Vertical Linearity	Adjusts the difference in distance between the center line to the top and the center line to the bottom. Adjust along the height so that the top and bottom border lines are exactly at the visible area edges as specified for height.

Figure 15-14, Service Menu Parameters

7. The values for the green parameters stored in the EEPROM at this point are the original factory values. They may be very close to optimum. The tolerances of the replacement CRT will be slightly different than the original requiring at least some touchup. Centering tolerances between the CRT, lens assembly and cooling coupler will throw the geometry off, at least a little. These errors may cause the raster to fall on a different position on the curved surface of the CRT face and add small geometry defects.

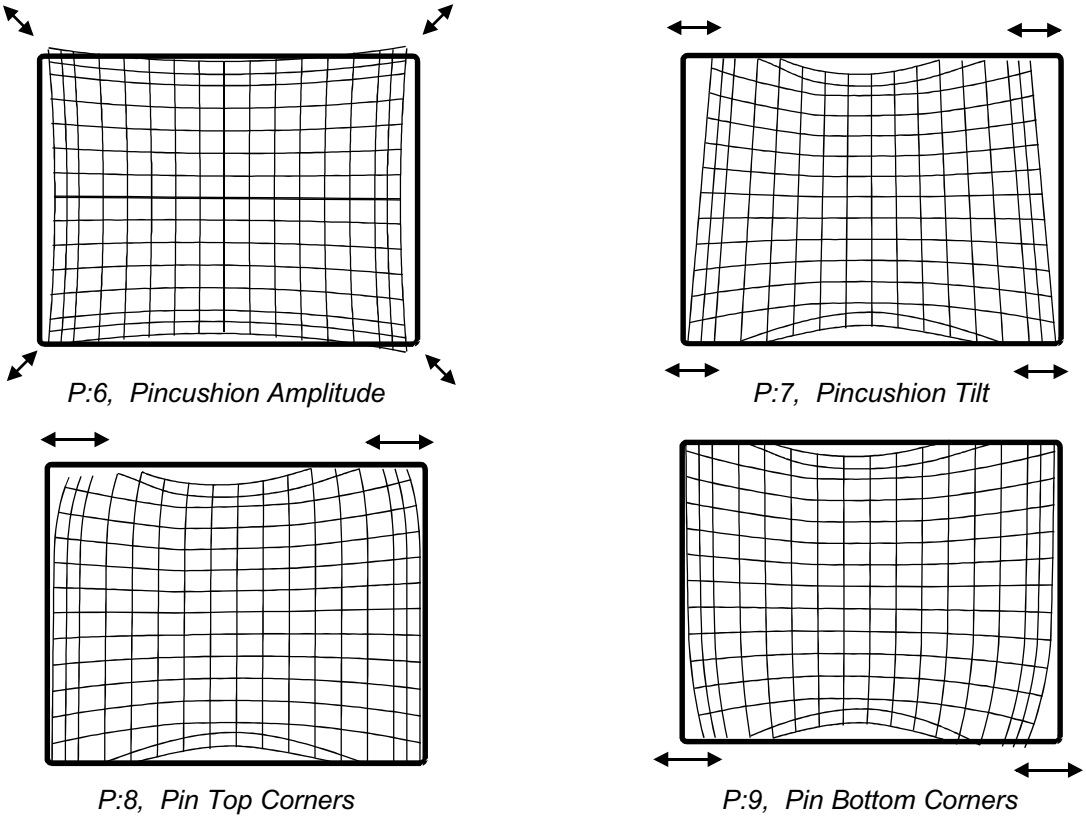


Figure 15-15, Adjustment Parameter Screens

Because of the spherical phosphor surface, the geometric distortion is both a displacement (left and right or top and bottom) and a bowed edge stretch. The 4 T-chip adjustments that deal with the geometry distortions are parameters 6 through 9. They are called "chassis" geometry adjustments because they correct all three CRT's equally. In addition, there are 4 more T-chip adjustments that adjust the raster size and location. Again, these are "chassis" adjustments because they affect all three CRT's equally. They are parameter 5, 10 and 11.

8. Adjust Vertical Size or Height (P11) (if using Chipper Check, Vertical Size) so that, with convergence off, the crosshairs circled below just touch the inner part of the screen frame. If all four crosshairs cannot be located properly, the right side of the screen is considered to be more critical and should be adjusted.

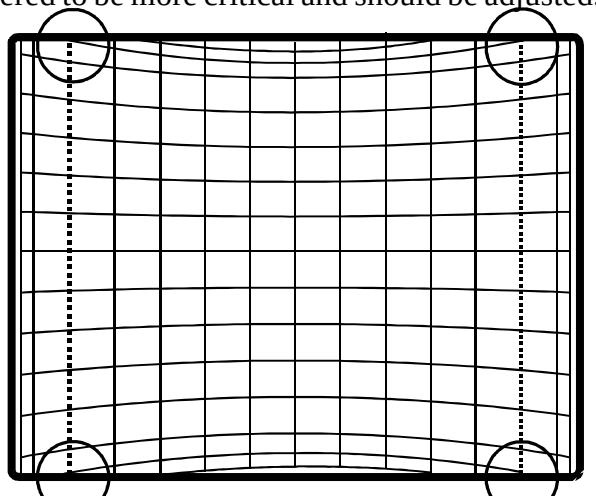


Figure 15-16, Vertical Size

9. Horizontal Size is adjusted with convergence off so that the outside edges of the right and left convergence pattern border lines at their intersection with the horizontal centerline are the same distance apart as the width of the viewable area of the screen The border lines will probably not line up with the viewable area with convergence off. Estimate the width.

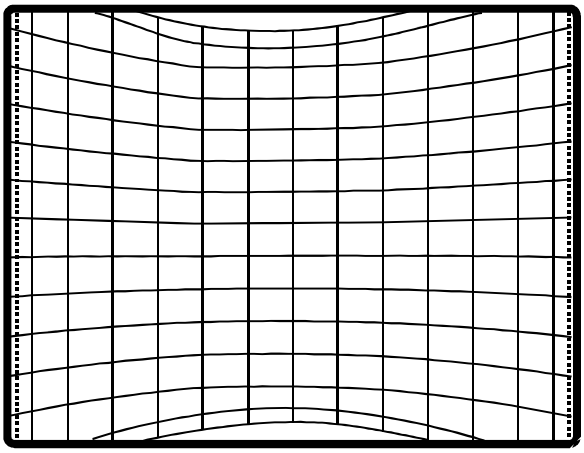


Figure 15-16, Horizontal Width

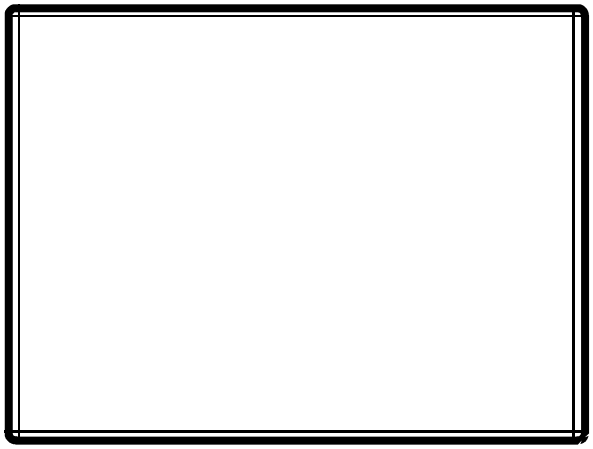


Figure 15-18, Green Boundary

10. Pincushion adjustments located at P:6 through P:9 should now be done. Remember, only slight adjustments should be needed. The vertical lines should be adjusted as straight as possible. If a compromise is required, adjust the right side of the picture more accurately.
11. P:10, Vertical Centering, is adjusted at the factory to provide 0 yoke current at line 141 of the first field of video. P:11, Vertical Countdown should not be touched.
12. Exit the geometry adjustments by pressing the PWR button on the remote or the front panel. This exits the service mode and adjusts AKB.
13. Enter the green customer centering menu selection and observe the border pattern. It should lie just within the frame of the screen. The coarse size and distortion correction has just been set with convergence off. When convergence is turned on the values will be optimized for old coarse geometry settings and if a tube has been changed to old tube performance. If there is less than 0.5" of difference between the green frame and the screen opening then center the green frame, center red and center blue and reconverge red and blue to green using menu 80. If the green frame error is more than 0.5" then attach alignment strings and realign green, red and blue using the Chipper Check 25 point program and then touch up local convergence with menu 80.

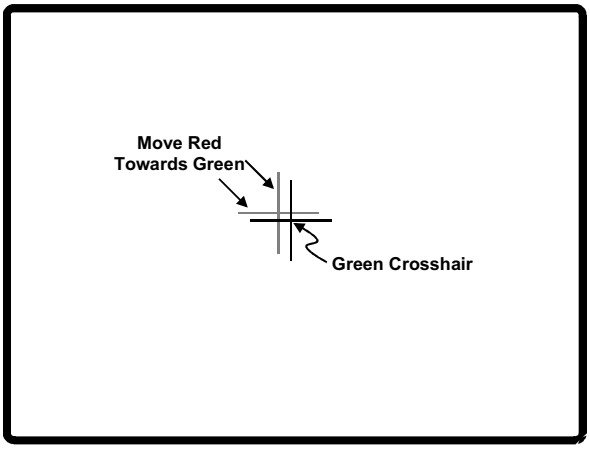


Figure 15-19, Consumer Centering Screen

EEPROM Replacement

There are two EEPROM's in the CTC195 whose failure represents problems for the digital convergence circuitry. The first is the DigiCon EEPROM, which affects all convergence alignments. The second is the main chassis EEPROM, which affects the geometry alignments. Although Chipper Check will initialize a replacement EEPROM with nominal values, until a complete alignment is done, picture quality may suffer.

Main EEPROM Replacement

Since the main EEPROM contains all the chassis geometry alignments, these adjustments are the only ones that need to be checked. The CRT replacement procedure may be used, beginning with Step 2.

DigiCon EEPROM Replacement

All DigiCon alignment values are stored in the DigiCon EEPROM. Further, the anti-banding calculations are also here. If the EEPROM values can be stored by Chipper Check before the replacement of the EEPROM, no further alignments should be necessary. However, since a decision has been made to replace the EEPROM, the data values contained should be assumed to be corrupt. Chipper Check must be used to restore the EEPROM data.

The steps to restore the set to proper specifications and alignments after a DigiCon EEPROM replacement are:

1. Unplug the R/G/B yoke plugs. This will prevent a power supply overload latch out. If the yokes are connected, the DigiCon IC will rail the power output transistors against the power supply if the EEPROM is blank and the power supply will latch off.
2. Connect Chipper Check and place the set into service mode (menu 200).
3. Using the initialization file in Chipper Check, transfer those files to the DigiCon EEPROM. This sets the DigiCon EEPROM data to a nominal set of values allowing set operation with no danger to DigiCon circuitry.
4. Power down the set and reconnect the R/G/B yokes.
5. Enter service mode using Chipper Check.
6. Perform the Band Gap adjustment. (Set voltage across R19539 to exactly 1 volt using as accurate a meter as available.)
7. Using Chipper Check, enter the consumer green centering adjustment set it to midrange or 0. If the frame is not straight or differs from the size of the screen frame by more than 0.5" check the geometry menu, using Chipper Check or menu 76 settings, apply strings to the screen and align green red and blue with the Chipper Check 25 point convergence program.
8. Apply strings as follows: Measure and mark the physical center of the screen. It is acceptable to measure the distance from the inside of the screen frame and divide this length by 2. For example, if the screen measures 36 $^{5}/_{8}$" from one side to the other inside the frame, the physical center of the screen will be 18$^{5}/_{16}$" from either side. Mark this point at the top and bottom of the screen, then place a string or other suitable reference between the two marks. This will serve as the horizontal center reference line as shown in Figure 15-20.
9. In the same manner, measure and mark the vertical physical center by measuring the screen distance from inside the frame from the top to the bottom. After placing the string, the screen should look like figure 15-21.

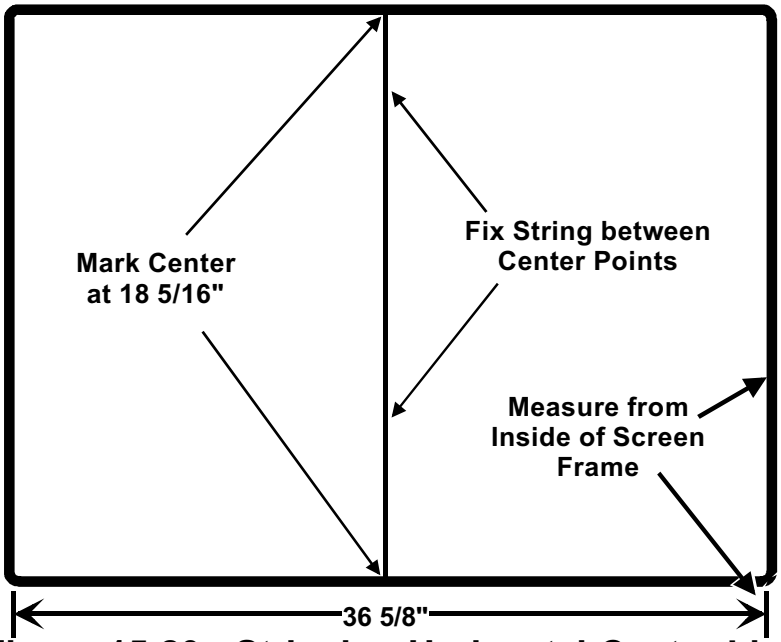


Figure 15-20, Stringing Horizontal Center Line

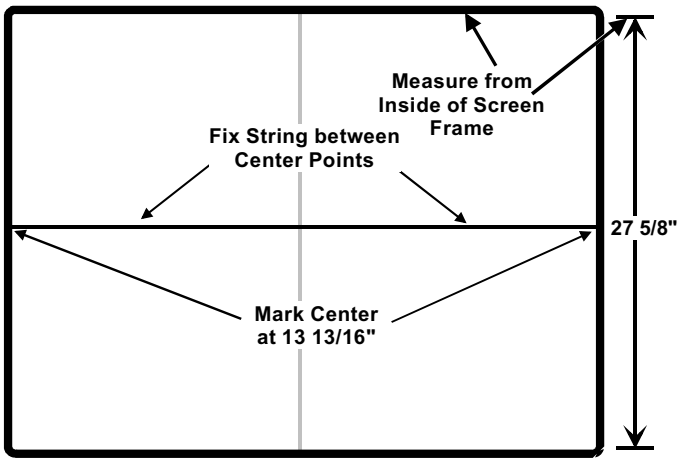


Figure 15-21, Stringing Vertical Center Line

10. Now that the exact center of the screen is known, place the remainder of the convergence reference strings on the screen by measuring outward from the center lines. Chipper Check will provide the exact dimensions for the remaining 2 vertical and 6 horizontal lines. The screen should now look like figure 15-22.
11. Check the green screen geometry first, making certain the pattern is centered via the CRT centering rings to the strings. No more than slight adjustments should be needed at this point. If there appear to be large discrepancies in the location or orientation of the pattern, return to the geometry adjustments and begin course alignment again.
12. Chipper Check will now allow the technician to begin the dynamic alignment of the green pattern using a preset configuration. At each point, move the green pattern to be centered, on the screen crossing. Be careful to view the screen perpendicular to the string crossing at each point to minimize parallax errors. Note that only horizontal motion is possible at the 5 mid upper and 5 mid bottom points. The vertical positions of these points are calculated to minimize banding.
13. Move through the complete pattern as allowed by the software.

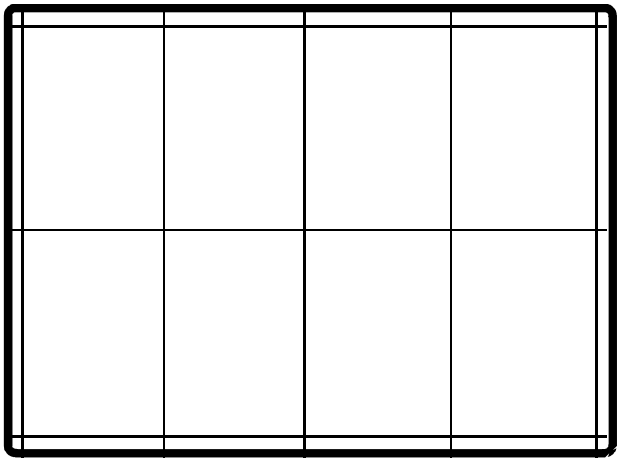


Figure 15-22, Completed Convergence Alignment Screen

14. When the pattern is aligned to the specifications, the pattern should appear to have perfect squares and be centered on the screen at this point.
15. If the pattern looks satisfactory, the alignment strings may be removed. If it does not, go back to step 13 and repeat the sequence until the screen alignment is acceptable.
16. Move to the red pattern and perform static centering, first setting the customer controls to midrange (0) and centering the pattern with the CRT centering rings to the green pattern. Then perform dynamic alignment of the red pattern to the green according to the preset route of Chipper Check.
17. Move to the blue pattern and perform static centering, first setting the customer controls to midrange (0) and centering the pattern with the CRT centering rings to the green pattern. Then perform dynamic alignment of the red pattern to the green according to the preset route of Chipper Check.
18. When the patterns are adjusted to specifications, exit the alignment and move to the full screen convergence pattern. This provides access to all adjustment points and enables the technician to perform additional "fine-tuning" of the convergence pattern. Chipper Check will now allow a "random" access to any crosspoint of the convergence pattern.
19. When the adjustments are complete, exit the Digital Convergence section of Chipper Check. All alignment data will be written to the new EEPROM.

DigiCon IC Replacement

The DigiCon IC stores all alignment data in the DigiCon EEPROM. During any power up, these values are retrieved and stored in RAM (Random Access Memory) in the IC during the operation of the set. The geometry settings for the set are located in the main EEPROM and used by the T-Chip. There is only one adjustment needed upon replacement of the DigiCon IC. The proper steps are:

1. Power the set back up and perform the Band Gap Adjustment with Chipper Check. (Set the voltage across R19539 to exactly 1 volt.)
2. Check the screen convergence with the full-screen digital convergence pattern. Touch up as necessary.

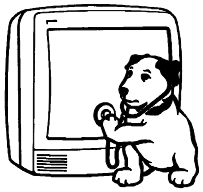
   NOTE: Once the band gap adjustment has been made, Chipper Check is not required to touch up the convergence alignments. Parameter 80 from the front panel may be used.

No major adjustments in either the geometry or convergence should be required.

Red/Green/Blue CRT's

In some cases, all three CRT's may have been removed. When they are replaced, there will be no references to which the CRT's may be compared. In this case, the following procedure may be used.

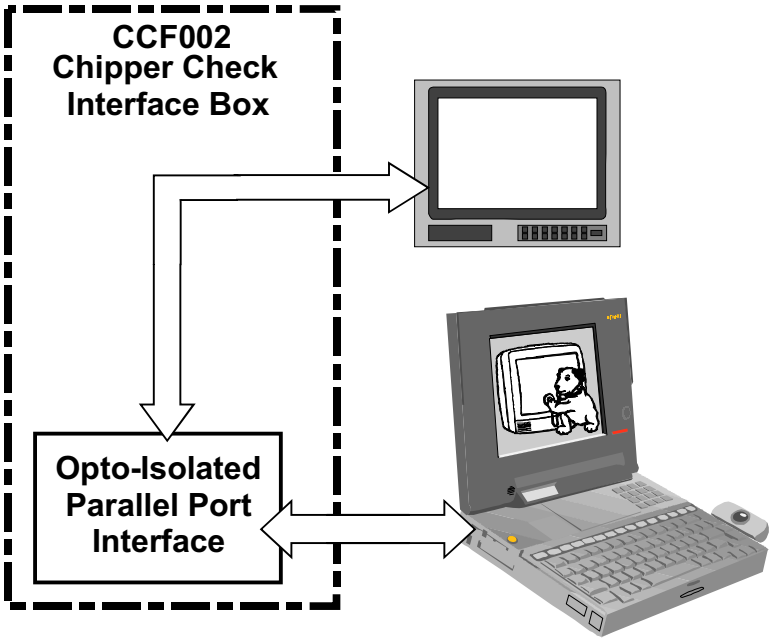
1. Using Chipper Check, access the R/G/B crosshairs (centering) and align the "Optical" and then "Electrical" focus on each tube.
2. Mark mechanical center of PTV screen using strings. Begin with the green CRT. Using the crosshair pattern of Chipper Check, use the CRT centering ring magnets to bring the crosshair to mechanical center. NOTE: First, bring the magnets together and rotate the assembly 360 degrees around neck of tube to bring the crosshair as close as possible to the marked mechanical center (where center strings cross). If proper centering cannot be reached, begin separating the magnets to bring the crosshair to exact mechanical center. Once the green CRT is done, move to the red, then the blue carefully centering the crosshair pattern to the center of the screen. Check the yoke rotation to make the horizontal centerline agree with the horizontal string.
3. Once optical and electrical focus and mechanical centering is done, perform all "Chassis Geometry" adjustments as outlined in the CRT replacement procedure.
4. After Chassis Geometry is complete, perform the "25 Point" Chipper Check adjustment.
5. After the "25 point" procedure the strings may be removed and the full DigiCon adjustment pattern may be accessed. The technician may perform fine-tuning adjustments on the pattern.
6. Recheck overall focus and chassis geometry adjustments to make certain nothing has changed dramatically. Minor adjustments may be made, but if specific areas of the screen seem to be off more than 1/8 inches, begin this procedure again.



Chipper Check™

Chipper Check Overview

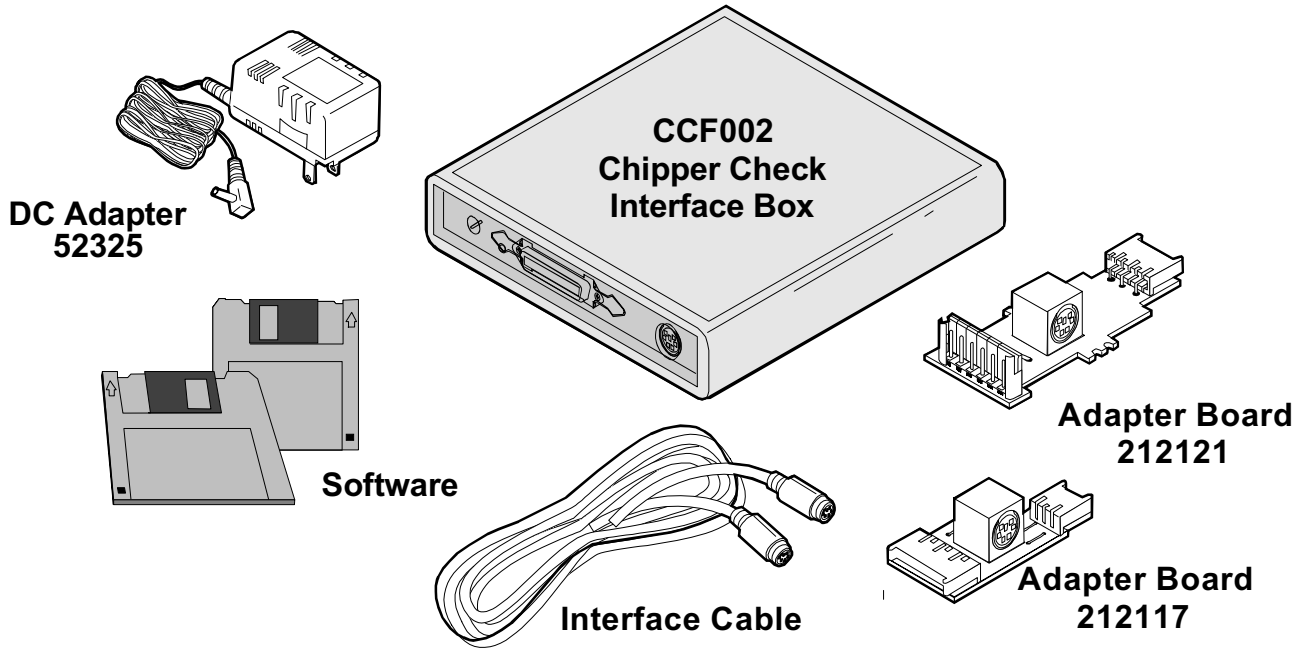
The evolution from early analog televisions to the modern digitally controlled TV has produced a number of new challenges for the service technician. These new microcomputer controlled televisions can exhibit a variety of symptoms that do not follow the logic of older analog television receivers. In addition, the alignments are no longer performed by adjusting a potentiometer, rather they have been replaced by a digital value that is stored in memory and converted to a DC voltage that is applied to the appropriate circuit. At first, this type of system can be confusing since it is not always obvious which adjustment is being performed by simply looking at the display on the picture tube. Some adjustments are not incorporated until the receiver is turned off and back on, which makes it very difficult to know when the adjustment is correct. Chipper Check was developed to address these differences and to provide the technician with a convenient method of performing adjustments and diagnosing problems. The Chipper Check system is composed of two (2) major components. The first component and the most visible is the hardware interface. The interface is responsible for physically connecting the TV and personal computer together. The second part is the software that runs the personal computer. This software provides the instructions on what to do and how to do it.



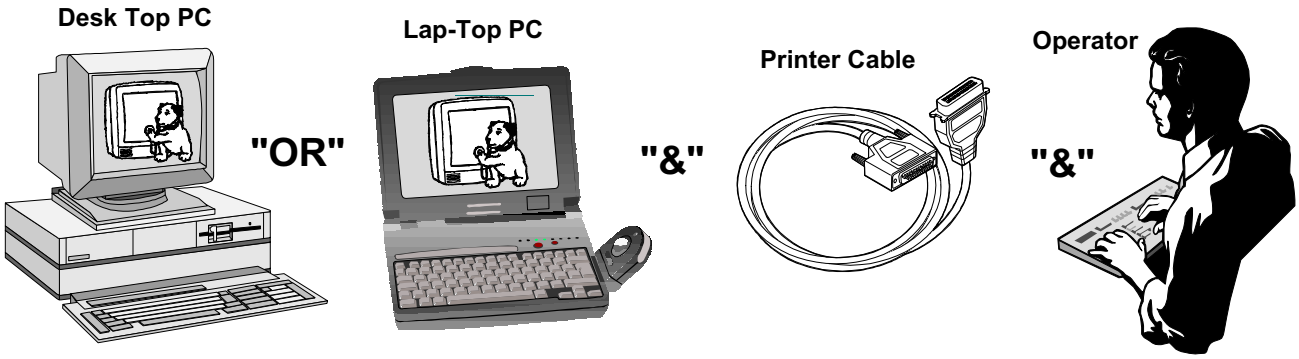
Chipper Check Simplified Block Diagram

Chipper Check Hardware

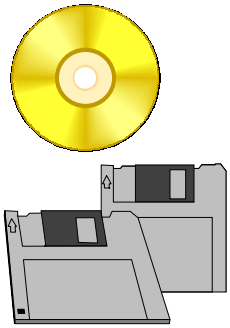
The hardware consists of small adapter boards that attache directly to the chassis via a communications port, an interconnect cable and the Chipper Check interface box. A printer cable is used to connect the interface box to the parallel port on the personal computer, however this cable is not part of the Chipper Hardware package. The adapter board allows the flexibility of connecting the interface box to a number of different chassis families. The communications format may vary from one chassis family to the next, and rather than developing a new interface box for each chassis, changing the adapter board allows the same interface box to be used. The Chipper Check interface box provides electrical isolation between the personal computer and the television receiver under test. The portion of the interface which connects to the personal computer is powered from the computer's parallel port. The interface contains a power supply that provides power to the television receiver side of the interface. The interface converts the signals from the parallel port of the computer into the correct protocol for the television microprocessor.



Chipper Check Items

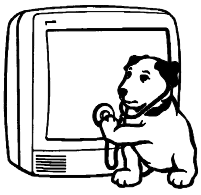


Chipper Check Items "Not Supplied"



Chipper Check Software

The Chipper Check software allows the technicians PC (personal computer) to troubleshoot, communicate with and perform alignments in a digitally controlled television. The Chipper Check software is composed of many different routines that are unique to each major chassis family. There is also a set of standard drivers for the interface hardware that are used for all chassis families. The software has been designed to be easily updated as new chassis and models are introduced. The software contains chassis auto-detection function, customer information screens, diagnostic routines, alignment routines along with on-line help files to guide the technician. The chassis auto-detection is used to ensure that only the alignments required for a specific chassis are performed. The customer information screen allows the service technician a way to match the information stored by Chipper Check to the specific instrument being serviced. The diagnostic routines are used to read any error codes stored in the instrument and identify which integrated circuit in the chassis is not responding. The alignment routines provides all alignment procedures needed on each chassis. The help files provide information on how to use the software how to perform the alignments, test point locations, and troubleshooting tips.



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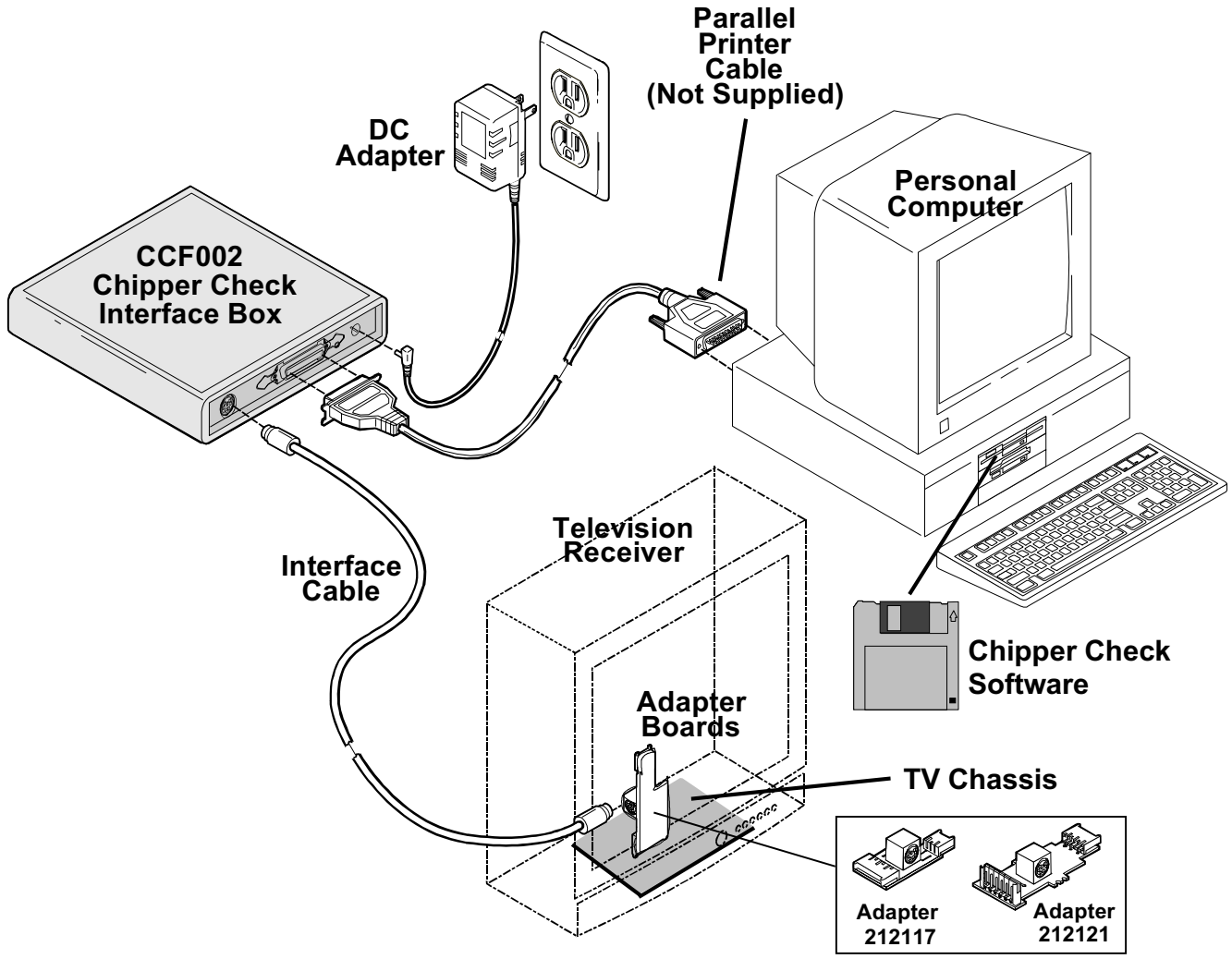
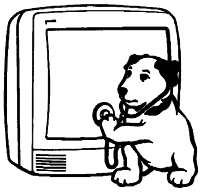


"Dead Set" Troubleshooting with Chipper Check

Chipper Check has two basic modes of operation, **"Dead Set"** and **"Normal"**. The dead set mode is helpful when the television receiver does not turn on. Chipper Check can be used to read the fault codes that were stored in the EEPROM. These fault codes remain in the EEPROM as long as there is standby power to the EEPROM. In this mode, the chassis auto-detection feature does not function, so the chassis type must be manually selected from a list. When the fault codes are recovered they indicate to the technician which IC was not responding to the microprocessor. It's important to remember that this does not necessarily mean that the IC called out is defective, merely that it is not communicating with the microprocessor. The reason for this could well be something other than the IC itself, such as a external component on the IC, etc. However, it does give the technician a good starting point for troubleshooting a "Dead Set". Likewise, if the standby power supply is not functioning, Chipper Check cannot read the error codes. This situation indicates the problem is probably located in the standby power supply and the technician should not need to use Chipper Check to find a failure in the standby power supply. In addition to reading the fault codes, it is possible to read and store the contents of the EEPROM's. The contents of the EEPROM's are stored in a customer file which allows the original settings to be reinstalled in the EEPROM after troubleshooting the dead set. The PIP EEPROM data cannot be read or re-initialized in the dead set mode.



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Chipper Check Hookup

To use Chipper Check in the normal mode, it is necessary to place the television microprocessor in the "slave" mode to prevent communication problems with the interface hardware. The adapter board and cable is connected to the Chipper Check port on the television chassis before the television is turned on, as long as the other end of the cable is not connected to the interface box. Having both ends of the cable connected may load the communications lines and prevent the television from turning on. After the television is in the slave mode and the cable is connected to the interface box, the Chipper Check software can be started.

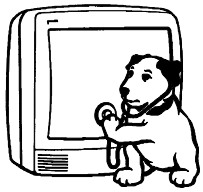
Chipper Check Operation

The first thing the program does is to check communications between the television and the computer. Part of this process is to detect which chassis is connected. If the wrong chassis is detected, it is possible to select the correct chassis type. Use caution when changing chassis types because the alignments are different, and selecting the wrong chassis can cause the computer to lock up, or store incorrect information in the television EEPROM. After communications are established, a customer information screen appears. This allows customer information such as name and model/serial number data to be stored. It is important to note that when the information on this screen is saved, the contents of the EEPROM are not yet associated with the file. This screen is placed here as a convenience to the service technician. The customer information or job ticket number, etc. is stored at the beginning of the process when the information is still readily available.

Diagnostic Function

The next screen after the customer information gives three choices, diagnostics, alignments, or a major part that has been replaced. The diagnostic portion gives the option of reading fault codes, checking the EEPROM, or reinitializing the EEPROM. The fault code again tells you which major component or IC is not responding. When the EEPROM is checked, data is ***"written to"*** and ***"read from"*** every location in the EEPROM. If the computer can read and write to every location, the EEPROM is functioning correctly and should not be replaced. However, this does not mean that the data stored in the EEPROM is correct. For this reason, the option of re-initializing the EEPROM is provided. Initializing the EEPROM will write the ***"factory values"*** to certain locations of the EEPROM. These are the items that need to be set to certain values to ensure proper initial operation. None of the alignment data is modified, nor is customer information such as scan lists and channel labels changed. During initialization, the customer controls are set to the factory preset values. These include the convergence settings on projection sets.

Alignments Function



Chipper Check™

The alignment function has the service alignments grouped into circuit areas or by the effect they have on the picture. Each group of alignments are performed in the proper order for that group. That is, once a group of alignments is selected, they should be performed in the order indicated, but the order in which the groups are selected does not matter. The highlighted text in the alignment procedure shows test point locations on the chassis and gives other helpful tips on performing the alignment. The help button on the alignment screen provides information on what to do if the alignment cannot be adjusted properly.

Part Replaced Function

The last option is ***"Replaced Part".*** When this option is selected, the technician must enter which major part has been replaced. The Chipper Check software then steps the technician through all alignments that should be performed or checked after that part has been changed. For example, if a component was changed in the PIP tuner, all PIP tuner alignments should be checked, however it is not necessary to perform the PIP color and tint alignments so these would not be brought up.

Notes:

T-CTC195/197-1

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