LINEAR TECHNOLOGY

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1994 Linear Databook
Volume III

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The founding theme of Linear Technology Corporation was to create a company capable of leading and directing linear circuit technology and design concepts of the future and thus become the linear market specialist.

Significant changes in the role of suppliers in the marketplace have evolved since the Company's founding in 1981. Shortened end product life cycles, sharply increased integrated circuit complexity and a large increase of new products have combined to present a potentially overwhelming burden on the system designer.

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This databook along with our first and second volumes, contains the solutions needed to facilitate your system design. We describe the circuit, give specific applications information and explain how to use the part effectively and efficiently.

LTC now offers approximately 5000 pages of product and applications information for approximately 3000 individual products, presented in a three volume set of databooks. The first volume issued in 1990, contains products which were introduced in the first 8 years of the Company's history. The second volume issued in 1992, showcases the products introduced in the next three years and this 1994 databook is the third, which presents the latest two years of LTC products.

The Table of Contents and the alphanumeric index in this volume provide guides to locate each LTC product within the three volume set. Be sure to use one of these guides to find the correct page in the appropriate volume.

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NOTES

Linear Technology Corporation

1994 Linear Databook Volume III

Note: *The 1994 Linear Databook is the third volume in our series of databooks to date totaling approximately 5000 pages of product and applications information for approximately 3000 individual products, presented in a three volume set of databooks. The 1990 Linear Databook when reprinted will be entitled Volume I; the 1992 Linear Databook Supplement when reprinted will become Volume II. The 1994 Linear Databook Volume III Table of Contents references device types included in both the 1990 Volume I and 1992 Volume II databooks.*

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Note: All products in **BOLD** are in this Databook, others appear in LTC's 1990 and 1992 Databooks ('90DB = LTC's 1990 Databook and '92DB = LTC's 1992 Databook Supplement).

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NOTES

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SECTION 1—GENERAL INFORMATION

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I. ORDER ENTRY

Orders for products contained herein should be directed to: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Boulevard, Milpitas, California 95035. Phone: 408-432-1900.

II. ORDERING INFORMATION

Minimum order value is $2000.00 per order; minimum value per line item is $1000.00.

Each item must be ordered using the complete part number exactly as listed on the data sheet.

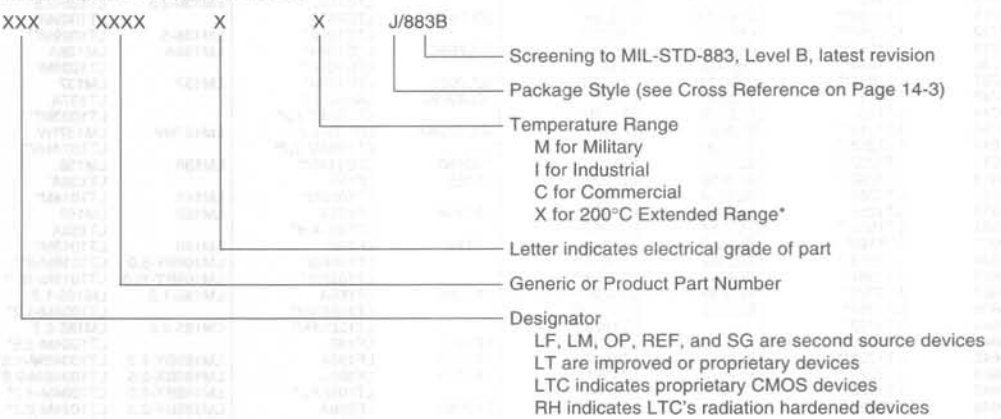
F.O.B.: Milpitas, California.

III. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

A. JAN QPL devices.
B. DESC drawings.
C. MIL-STD-883, Level B, latest revision for all military temperature range devices.
D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.
E. Radiation Hardened (RH) products.

IV. PART NUMBER EXPLANATION



V. PACKAGE SUFFIX EXPLANATION

Letter Designator	Description
D8	8-Lead Side Brazed Hermetic DIP
D	14, 16, 18, 20, and 24-Lead Side Brazed Hermetic DIP
F	20-Lead Molded TSSOP
G	20, 28-Lead Molded SSOP
H	Multi-Lead Metal Can
J8	8-Lead Ceramic DIP
J	14, 16, 18, and 20-Lead Ceramic DIP
K	TO-3 Metal Can (Steel)
M	3-Lead DD package Molded
N8	8-Lead Molded DIP
N	14, 16, 18, 20, 24, and 28-Lead Molded DIP
P	3-Lead TO-3P Molded
Q	5-Lead DD package Molded
R	7-Lead DD package Molded

Letter Designator	Description
S8	8-Lead Small Outline (SO) package (Note 1)
S	14, 16, 18, 20, 24, and 28-Lead Small Outline (SO) package (Note 1, 2)
ST	SOT-223 Molded
T	3 and 5-Lead TO-220 Molded
W	10-Lead Flatpack (Cerpak)
Y	7-Lead TO-220 Molded
Z	3-Lead TO-92 Molded

Note 1: Pinout and electrical specifications may differ from standard commercial grade N8 package. See SO data sheet for specific information.

Note 2: These devices are delivered in either 150 MIL (SO) or 300 MIL (SO-L) wide packages depending on device die size. See specific SO data sheet for pin counts and package dimensions.

LINEAR TECHNOLOGY

ALTERNATE SOURCE CROSS REFERENCE GUIDE

P/N	LTC DIRECT REPL
AD101A	LM101A
AD232	LT1081*
AD235	LT1130A**
AD237	LT1138A**
AD238	LT1139A**
AD239	LT1137A**
AD241	LT1137A**
AD381	LT1022**
AD510	LT1001*
AD517	LT1001**
AD518	LM118**
	LT118A**
AD524	LT1101**
AD536	LT1088**
AD580	LT580
AD581	LT581
	LT1031**
AD586	LT1027*
AD589	LT1034**
AD636	LT1088**
AD637	LT1088**
AD642	LT1057**
AD647	LT1057**
AD704	LT1114*
AD705	LT1097
AD706	LT1112*
AD707	LT1097
AD711	LT1056**
AD712	LT1057**
AD713	LT1058**
AD736	LT1088**
AD737	LT1088**
AD743	LT1113*
AD744	LT1122
AD790	LT1016**
AD810	LT1252**
AD811	LT1252**
AD813	LT1260**
AD817	LT1360*
AD818	LT1363
AD821	LT1006**
AD822	LT1169*
AD824	LT1014**
AD826	LT1361*
AD827	LT1229**
AD828	LT1364*
AD840	LT1222**
AD841	LT1220**
AD842	LT1221**
AD844	LT1223**
AD845	LT1122
AD846	LT1223**
AD847	LT1360
AD848	LT1192**
AD849	LT1226
	LT1192
AD7306	LT1318**
AD7572	LTC1272**
AD7579	LTC1091**
AD7580	LTC1092**
AD7820	LTC1099*
AD7821	LTC1096/
	LTC1098**
AD7870	LTC1275**
AD7875	LTC1273**
AD7876	LTC1276**
AD7883	LTC1282**
AD7890	LTC1290**
AD7892-1,2	LTC1278-5**
AD7892-3	LTC1279**
AD9617	LT1223
AD9618	LT1223
AD9686	LT1016**

P/N	LTC DIRECT REPL
ADC0820	LTC1099*
ADC0832	LTC1098*
ADC08061	LTC1198**
ADC08231	LTC1196
ADC1031	LTC1091**
ADC1034	LTC1093**
ADC1038	LTC1094**
ADG201A	LTC201A
ADG202	LTC202
ADG221	LTC221
ADG222	LTC222
ADOP07	OP07
	LT1001*
ADOP27	OP27
	LT1007*
ADS7800	LTC1276**
ADS7803	LTC1293**
ADS7804	LTC1272-8**
CLC406	LT1227**
CLC414	LT1252
CLC415	LT1230
CLC430	LT1206**
CLC520	LT1228**
CLC532	LT1203**
CMP01	LT1011**
CMP02	LT1011**
DAC8512	LTC1257**
DG201A	LTC201
DG202	LTC202
DS1232	LTC1232
DS14C335	LT1331**
DS3695	LTC485*
EL2020	LT1223*
EL2028	LT1220
EL2029	LT1221
EL2030	LT1223
EL2038	LT1222
EL2039	LT1222
EL2040	LT1222
EL2041	LT1220
EL2044	LT1252**
EL2045	LT1363*
EL2082	LT1228**
EL2090	LT1228**
EL2099	LT1206**
EL2120	LT1191**
	LT1223**
	LT1227**
EL2130	LT1227**
EL2210	LT1361*
EL2211	LT1364*
EL2224	LT1229**
	LT1208**
EL2232	LT1229**
EL2242	LT1229**
	LT1358*
EL2244	LT1361*
EL2245	LT1364*
EL2260	LT1229
EL2444	LT1362
EL2445	LT1254**
EL2460	LT1230
EL4089	LT1228**
EL4393	LT1260**
EL4094/5	LT1256**
GT4123	LT1256**
GY4102	LT1203**
GX4314	LT1205**
HA2500	LT1220
HA2502	LT1220
HA2505	LT1220
HA2510	LT118A**
	LM118**
HA2512	LT118A**

P/N	LTC DIRECT REPL
	LM118A**
HA2515	LT318A**
	LM318**
HA2520	LT1220
HA2541	LT1220
HA2544	LT1224
HA5004	LT1223
HA5130-2	OP07A
	LT1001AM*
HA5130-5	OP07E
	LT1001C*
HA5135-2	OP07
	LT1001M*
HA5135-5	OP07C
	LT1001C*
HAOP07	OP07
	LT1001M*
HAOP07A	OP07A
	LT1001AM*
HAOP07C	OP07C
	LT1001C*
HAOP07E	OP07E
	LT1001C*
HI5810	LTC1272-8
ICL232	LT1081
ICL7650	LTC1050*
	LTC1052**
ICL7652	LTC7652
	LTC1052*
ICL7660	LTC1044*
	LTC1054**
ICL7662	LTC1144*
ICL8069C	LM385-1.2
	LT1004C-1.2*
ICL8069M	LM185-1.2
	LT1004M-1.2*
ISO150	LTC1145**
LF155	LF155
	LT1055M*
LF155A	LF155A
	LT1055AM*
LF156	LF156
	LT1056M*
	LT1022M*
LF156A	LF156A
	LT1056AM*
	LT1022AM*
LF198	LF198
LF198A	LF198A
LF355A	LF355A
	LT1055AC*
LF356A	LF356A
	LT1056AC*
	LT1022AC*
LF357	LT1022*
LF398	LF398
LF398A	LF398A
LF400	LT1122DC
	LT1122CC
LF400A	LT1122BC
	LT1122AC
LH0002	LT1010M**
LH0044	LT1001M*
LH0070	LH0070
	LT1031M*
LH2108	LH2108
LH2108A	LH2108A
LM10	LM10
LM10B	LM10B
LM10C	LM10C
LM101A	LM101A
LM107	LM107
LM108	LM108
	LT1008M*

P/N	LTC DIRECT REPL
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM112	LT1012M*
LM113	LT1004M-1.2*
LM117	LM117
	LT117A*
LM117HV	LM117HV
	LT117AHV*
LM118	LM118
	LT118A*
LM119	LM119
	LT119A*
LM123	LM123
	LT123A*
	LT1003M*
LM124	LT1014M*
LM129A	LM129A
LM129B	LM129B
LM129C	LM129C
LM133	LT1033M*
LM134	LM134
LM134-3	LM134-3
LM134-6	LM134-6
LM136-2.5	LT136-2.5
	LT1009M*
LM136-5	LT1029M**
LM136A	LM136A
	LT1009M*
LM137	LM137
	LT137A
	LT1033M**
LM137HV	LM137HV
	LT137AHV*
LM138	LM138
	LT138A*
LM148	LT1014M*
LM150	LM150
	LT150A*
LM158	LT1013M*
LM168BY-5.0	LT1019M-5**
LM168BY-10.0	LT1019M-10**
LM185-1.2	LM185-1.2
	LT1004M-1.2*
LM185-2.5	LM185-2.5
	LT1004M-2.5*
LM185BX-1.2	LT1034BM-1.2*
LM185BX-2.5	LT1034BM-2.5*
LM185BY-1.2	LT1034M-1.2*
LM185BY-2.5	LT1034M-2.5*
LM196	LT1038M**
LM199	LM199
LM199A	LM199A
LM199A-20	LM199A-20
LM234-3	LM234-3
LM234-6	LM234-6
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM318	LM318
	LT318A*
LM319	LM319
	LT319A*
LM323	LM323
	LT323A*
	LT1003C**
LM329A	LM329A
LM329B	LM329B
LM329C	LM329C
LM329D	LM329D

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

LINEAR TECHNOLOGY

P/N	LTC DIRECT REPL
LM333	LT1033C*
LM333A	LT1033C
LM334	LM334
LM336-2.5	LM336
	LT1009C*
LM336-5	LT1029C*
LM336B-2.5	LM336B
	LT1009C*
LM338	LM338
	LT338A*
LM350	LM350
	LT350A*
LM368-5.0	LT1019AC-5*
LM368-10.0	LT1019C-10**
LM368Y-5.0	LT1019AC-5*
LM368Y-10.0	LT1019C-10**
LM385-1.2	LM385-1.2
	LT1004C-1.2*
LM385-2.5	LM385-2.5
	LT1004C-2.5*
LM385BX-1.2	LT1034BC-1.2*
LM385BX-2.5	LT1034BC-2.5*
LM385BY-1.2	LT1034C-1.2*
LM385BY-2.5	LT1034C-2.5*
LM396	LT1038C**
LM399	LM399
LM399A	LM399A
LM399A-20	LM399A-20
LM399A-50	LM399A-50
LM1524	SG1524
	LT1524*
LM2575	LT1076**
LM2575N	LT1176
LM2576	LT1074**
LM2577	LT1071**
LM2935	LT1005**
LM2940	LT1086**
LM3524	SG3524
	LT3524*
LM6181	LT1227**
LM6218	LT1203**
LM6361	LT1195**
LP2950-5	LT1117-5**
LP2951	LT1121**
µA96172	LTC486
µA96174	LTC487
µA96176	LTC485
MAX120	LT1278-5**
MAX122	LTC1276**
MAX153	LTC1198**
MAX162	LTC1273*
MAX163	LTC1273*
MAX164	LTC1275*
MAX165	LTC1198**
MAX167	LTC1275**
MAX172	LTC1272*
MAX202	LT1381*
MAX207	LT1138A**
MAX211	LTC1337**
MAX212	LTC1348**
MAX220	LT1281A**
MAX222	LT1280A*
MAX223	LT1237
MAX232A	LT1281A*
MAX235A	LT1130A**
MAX237A	LT1138A**
MAX238A	LT1139A**
MAX239A	LT1137A**
MAX241A	LT1136A**
	LT1137A**
MAX242	LTC1384*
MAX280	LTC1062
MAX281	LTC1065**
MAX400	LT1001
MAX420	LTC1150*
MAX422	LTC1150**
MAX430	LTC1150
MAX432	LTC1150**
MAX441	LT1204**
MAX454	LT1204**
MAX478	LT1178
MAX479	LT1179
MAX480	LT1077*
MAX481	LTC1481
MAX485	LTC485
MAX487	LTC1487*
MAX538	LTC1257**
MAX539	LTC1257**
MAX560	LT1331**
MAX561	LTC1327**
MAX630	LT1173**
MAX631	LT1173-5**
MAX632	LT1173-12**
MAX633	LT1173**
MAX634	LT1173**
MAX635	LT1173-5**
MAX636	LT1173-12**
MAX637	LT1173**
MAX638	LT1173-5**
MAX639	LTC1174*
MAX641	LT1173-5**
MAX642	LT1173-12**
MAX643	LT1173**
MAX654	LT1073-5
MAX655	LT1173-5**
MAX656	LT1073-5**
MAX657	LT1073**
MAX658	LT1108-5**
MAX659	LT1108-5**
MAX660	LT1054**
MAX662	LTC1262*
MAX667	LT1129**
MAX680	LT1026
MAX690	LTC690
MAX691	LTC691
MAX692	LTC692*
MAX693	LTC693*
MAX694	LTC694
MAX695	LTC695
MAX699	LTC699
MAX741D	LTC1147**
MAX741U	LT1171**
	LT1172**
MAX756	LT1303-5**
MAX757	LT1303**
MAX873	LT1019-2.5
MAX875	LT1019-5
	LT1021-5
	LT1027
MAX876	LT1019-10
	LT1021-10
MAX1232	LTC1232
MAX9686	LT1016
MC78T05	LM323T
	LT323AT*
MC1400AU2	LT1019CN8-2.5**
MC1400AU5	LT1019CN8-5**
MC1400AU10	LT1019CN8-10**
MC1400U2	LT1019CN8-2.5*
MC1400U5	LT1019CN8-5*
MC1400U10	LT1019CN8-10*
MC1558	LT1013M*
MC145406	LT1039-16*
MC34166	LT1074
MF5	LTC1059*
MF10	LTC1060
	LTC1060*
MX7572	LTC1272*
MX7820	LTC1099*
OPA27	OP27
	LT1007*
OPA37	OP37
	LT1037*
OPA177	LT1001A
	LT1097
OPA404	LT1216**
OPA603	LT1252
OPA620	LT1227**
OPA1013	LT1013
	LT1211
OPA2107	LT1169**
OPA2111	LT1169**
OPA2604	LT1124**
OP04	LT1013*
OP05	OP05
	LT1001
OP07	OP07
	LT1001
OP10	LT1002
OP11	LT1014*
OP12	LT1012
OP14	LT1013**
OP15	OP15
	LT1055*
OP16	OP16
	LT1056*
OP27	OP27
	LT1007*
OP37	OP37
	LT1037*
OP42	LT1122*
OP77	LT1001
	LT1097*
OP97	LT1012
	LT1097*
OP177	LT1001
OP207	LT1002
OP215	OP215
	LT1057
OP220	LT1078*
OP221	LT1013*
OP227	OP227
OP270	OP270
	LT1124*
OP290	LT1078**
OP297	LT1112*
OP400	LT1014*
	LT1114*
OP420	LT1079*
OP421	LT1014*
OP467	LT1359*
OP470	OP470
	LT1125*
OP490	LT1079**
OP497	LT1114*
PM108	LM108
	LT1008M*
PM108A	LM108A
	LT1008M*
PM155	LF155
	LT1055M*
PM155A	LF155A
	LT1055M*
PM156	LF156
	LT1056M*
PM156A	LF156A
	LT1056M*
PM308A	LM308A
	LT1008C*
PM355A	LF355A
	LT1055C*
PM356A	LF356A
	LT1056C*
PM1008	LT1008
PM1012	LT1012
PM1558	LT1013M*
PM2108	LH2108
PM2108A	LH2108A
REF01	REF01
	LT1019-10*
	LT1021-10**
REF02	REF02
	LT1019-5*
	LT1021-5**
REF03	LT1019-2.5*
REF43	LT1019A-2.5*
REF101	LT1019-10
	LT1021-10
REF102	LT1019-10
	LT1021-10
REG1117	LT1117-2.85
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG1526	LT1526
SG1527A	SG1527A
	LT1527A*
SG1558	LT1013M*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*
SG3526	LT3526
SG3527A	SG3527A
	LT3527A*
SN75172	LTC486*
SN75174	LTC487*
SN75176	LTC485*
SN75186	LT1134**
SP301	LTC1321*
SP302	LTC1322*
TL431A	LT1431*
TLC2543	LTC1296
TSC04	LT1004-1.2
TSC05	LT1004-2.5
TSC170	LT3846**
TSC171	LT3847**
TSC232	LT1080**
	LT1081**
TSC911	LTC1050*
TSC913	LT1078**
	LTC1051*
TSC914	LT1079**
	LTC1053*
TSC918	LTC7652**
TSC962	LTC1046**
TSC7650	LTC1050*
TSC7652	LTC7652
	LTC1052
TSC7660	LTC1044*
TSC9491	LT1004-1.2
TSC9495	REF02
	LT1019M-5
	LT1021-5**
TSC9496	REF01
	LT1021-10**
UC117	LM117
	LT117A*
UC137	LM137
	LT137A*
	LT1033M**
UC150	LM150
	LT150A*

*LTC Improved Replacement: 100% Pin-for-pin compatible with better electrical specifications.
**Similar Device: Please consult the data sheet to determine the suitability of the replacement for specific applications.

ALTERNATE SOURCE CROSS REFERENCE GUIDE

P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL
UC317	LM317						
	LT317A*						
UC337	LM337						
	LT337A*						
	LT1033C**						
UC350	LM350						
	LT350A*						
UC1524	SG1524						
	LT1524*						
UC1525A	SG1525A						
	LT1525A*						
UC1527A	SG1527A						
	LT1527A*						
UC1846	LT1846						
UC1847	LT1847						
UC2525A	SG3525A						
	LT3525A*						
UC3524	SG3524						
	LT3524*						
UC3527A	SG3527A						
	LT3527A*						
UC3842	LT1242*						
UC3843	LT1243*						
UC3844	LT1244*						
UC3845	LT1245*						
UC3854	LT1248*						

*LTC Improved Replacement: 100% Pin-for-pin compatible with better electrical specifications.
**Similar Device: Please consult the data sheet to determine the suitability of the replacement for specific applications.

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SECTION 2—AMPLIFIERS

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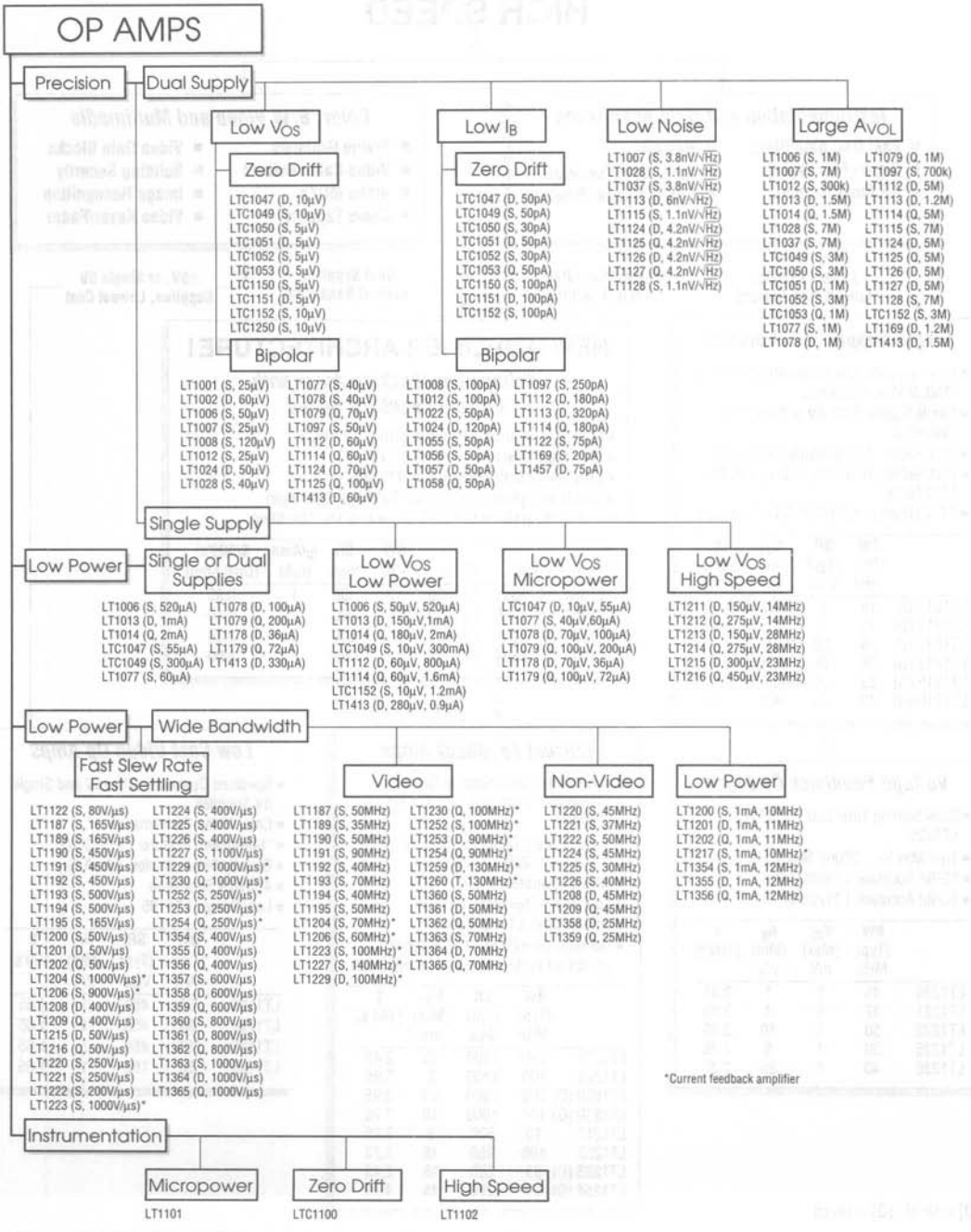

OP AMPS
Precision
Dual Supply
Low VOS
Zero Drift
LTC1047 (D, 10µV)
LTC1049 (S, 10µV)
LTC1050 (S, 5µV)
LTC1051 (D, 5µV)
LTC1052 (S, 5µV)
LTC1053 (Q, 5µV)
LTC1150 (S, 5µV)
LTC1151 (D, 5µV)
LTC1152 (S, 10µV)
LTC1250 (S, 10µV)
Bipolar
LT1001 (S, 25µV)
LT1002 (D, 60µV)
LT1006 (S, 50µV)
LT1007 (S, 25µV)
LT1008 (S, 120µV)
LT1012 (S, 25µV)
LT1024 (D, 50µV)
LT1028 (S, 40µV)
LT1077 (S, 40µV)
LT1078 (S, 40µV)
LT1079 (Q, 70µV)
LT1097 (S, 50µV)
LT1112 (D, 60µV)
LT1114 (Q, 60µV)
LT1124 (D, 70µV)
LT1125 (Q, 100µV)
LT1413 (D, 60µV)
Low IB
Zero Drift
LTC1047 (D, 50pA)
LTC1049 (S, 50pA)
LTC1050 (S, 30pA)
LTC1051 (D, 50pA)
LTC1052 (S, 30pA)
LTC1053 (Q, 50pA)
LTC1150 (S, 100pA)
LTC1151 (D, 100pA)
LTC1152 (S, 100pA)
Bipolar
LT1008 (S, 100pA)
LT1012 (S, 100pA)
LT1022 (S, 50pA)
LT1024 (D, 120pA)
LT1055 (S, 50pA)
LT1056 (S, 50pA)
LT1057 (D, 50pA)
LT1058 (Q, 50pA)
LT1097 (S, 250pA)
LT1112 (D, 180pA)
LT1113 (D, 320pA)
LT1114 (Q, 180pA)
LT1122 (S, 75pA)
LT1169 (S, 20pA)
LT1457 (D, 75pA)
Low Noise
LT1007 (S, 3.8nV/√Hz)
LT1028 (S, 1.1nV/√Hz)
LT1037 (S, 3.8nV/√Hz)
LT1113 (D, 6nV/√Hz)
LT1115 (S, 1.1nV/√Hz)
LT1124 (D, 4.2nV/√Hz)
LT1125 (Q, 4.2nV/√Hz)
LT1126 (D, 4.2nV/√Hz)
LT1127 (Q, 4.2nV/√Hz)
LT1128 (S, 1.1nV/√Hz)
Large AVOL
LT1006 (S, 1M)
LT1007 (S, 7M)
LT1012 (S, 300k)
LT1013 (D, 1.5M)
LT1014 (Q, 1.5M)
LT1028 (S, 7M)
LT1037 (S, 7M)
LTC1049 (S, 3M)
LTC1050 (S, 3M)
LTC1051 (D, 1M)
LTC1052 (S, 3M)
LTC1053 (Q, 1M)
LT1077 (S, 1M)
LT1078 (D, 1M)
LT1079 (Q, 1M)
LT1097 (S, 700k)
LT1112 (D, 5M)
LT1113 (D, 1.2M)
LT1114 (Q, 5M)
LT1115 (S, 7M)
LT1124 (D, 5M)
LT1125 (Q, 5M)
LT1126 (D, 5M)
LT1127 (D, 5M)
LT1128 (S, 7M)
LTC1152 (S, 3M)
LT1169 (D, 1.2M)
LT1413 (D, 1.5M)
Single Supply
Low Power
Single or Dual Supplies
LT1006 (S, 520µA)
LT1013 (D, 1mA)
LT1014 (Q, 2mA)
LTC1047 (S, 55µA)
LTC1049 (S, 300µA)
LT1077 (S, 60µA)
LT1078 (D, 100µA)
LT1079 (Q, 200µA)
LT1178 (D, 36µA)
LT1179 (Q, 72µA)
LT1413 (D, 330µA)
Low VOS Low Power
LT1006 (S, 50µV, 520µA)
LT1013 (D, 150µV,1mA)
LT1014 (Q, 180µV, 2mA)
LTC1049 (S, 10µV, 300mA)
LT1112 (D, 60µV, 800µA)
LT1114 (Q, 60µV, 1.6mA)
LTC1152 (S, 10µV, 1.2mA)
LT1413 (D, 280µV, 0.9µA)
Low VOS Micropower
LTC1047 (D, 10µV, 55µA)
LT1077 (S, 40µV,60µA)
LT1078 (D, 70µV, 100µA)
LT1079 (Q, 100µV, 200µA)
LT1178 (D, 70µV, 36µA)
LT1179 (Q, 100µV, 72µA)
Low VOS High Speed
LT1211 (D, 150µV, 14MHz)
LT1212 (Q, 275µV, 14MHz)
LT1213 (D, 150µV, 28MHz)
LT1214 (Q, 275µV, 28MHz)
LT1215 (D, 300µV, 23MHz)
LT1216 (Q, 450µV, 23MHz)
Low Power
Wide Bandwidth
Fast Slew Rate Fast Settling
LT1122 (S, 80V/µs)
LT1187 (S, 165V/µs)
LT1189 (S, 165V/µs)
LT1190 (S, 450V/µs)
LT1191 (S, 450V/µs)
LT1192 (S, 450V/µs)
LT1193 (S, 500V/µs)
LT1194 (S, 500V/µs)
LT1195 (S, 165V/µs)
LT1200 (S, 50V/µs)
LT1201 (D, 50V/µs)
LT1202 (Q, 50V/µs)
LT1204 (S, 1000V/µs)*
LT1206 (S, 900V/µs)*
LT1208 (D, 400V/µs)
LT1209 (Q, 400V/µs)
LT1215 (D, 50V/µs)
LT1216 (Q, 50V/µs)
LT1220 (S, 250V/µs)
LT1221 (S, 250V/µs)
LT1222 (S, 200V/µs)
LT1223 (S, 1000V/µs)*
LT1224 (S, 400V/µs)
LT1225 (S, 400V/µs)
LT1226 (S, 400V/µs)
LT1227 (S, 1100V/µs)
LT1229 (D, 1000V/µs)*
LT1230 (Q, 1000V/µs)*
LT1252 (S, 250V/µs)*
LT1253 (D, 250V/µs)*
LT1254 (Q, 250V/µs)*
LT1354 (S, 400V/µs)
LT1355 (D, 400V/µs)
LT1356 (Q, 400V/µs)
LT1357 (S, 600V/µs)
LT1358 (D, 600V/µs)
LT1359 (Q, 600V/µs)
LT1360 (S, 800V/µs)
LT1361 (D, 800V/µs)
LT1362 (Q, 800V/µs)
LT1363 (S, 1000V/µs)
LT1364 (D, 1000V/µs)
LT1365 (Q, 1000V/µs)
Video
LT1187 (S, 50MHz)
LT1189 (S, 35MHz)
LT1190 (S, 50MHz)
LT1191 (S, 90MHz)
LT1192 (S, 40MHz)
LT1193 (S, 70MHz)
LT1194 (S, 40MHz)
LT1195 (S, 50MHz)
LT1204 (S, 70MHz)*
LT1206 (S, 60MHz)*
LT1223 (S, 100MHz)*
LT1227 (S, 140MHz)*
LT1229 (D, 100MHz)*
LT1230 (Q, 100MHz)*
LT1252 (S, 100MHz)*
LT1253 (D, 90MHz)*
LT1254 (Q, 90MHz)*
LT1259 (D, 130MHz)*
LT1260 (T, 130MHz)*
LT1360 (S, 50MHz)
LT1361 (D, 50MHz)
LT1362 (Q, 50MHz)
LT1363 (S, 70MHz)
LT1364 (D, 70MHz)
LT1365 (Q, 70MHz)
Non-Video
LT1220 (S, 45MHz)
LT1221 (S, 37MHz)
LT1222 (S, 50MHz)
LT1224 (S, 45MHz)
LT1225 (S, 30MHz)
LT1226 (S, 40MHz)
LT1208 (D, 45MHz)
LT1209 (Q, 45MHz)
LT1358 (D, 25MHz)
LT1359 (Q, 25MHz)
Low Power
LT1200 (S, 1mA, 10MHz)
LT1201 (D, 1mA, 11MHz)
LT1202 (Q, 1mA, 11MHz)
LT1217 (S, 1mA, 10MHz)*
LT1354 (S, 1mA, 12MHz)
LT1355 (D, 1mA, 12MHz)
LT1356 (Q, 1mA, 12MHz)
*Current feedback amplifier
Instrumentation
Micropower
LT1101
Zero Drift
LTC1100
High Speed
LT1102

HIGH SPEED

Instrumentation and Data Acquisition

- Fast DAC Amplifiers
- Signal Processing
- RF Amplification
- RADAR
- Fiber-Optic Systems
- Copiers/Laser Printers

Color, B/W Video and Multimedia

- Frame Grabbers
- Video Cable Drivers
- Video MUXs
- Cable Tappers
- Video Gain Blocks
- Building Security
- Image Recognition
- Video Keyer/Fader

Lowest Offsets, Lowest Bias Current

Fastest Slew Rate, Fastest Settling

Dual Supplies, Largest Bandwidth

±5V, or Single 5V Supplies, Lowest Cost

Single Supply, DC Precision

- Low V_{OS} with High Bandwidth/Slew Rate (150µV Max, A-Grades)
- Single Supply 3.3V, 5V or Dual ±15V Operation
- Low Power (1.3mA/Amp): LT1211/12
- Fast Settling to 0.01%, 250ns, 2V Step: LT1215/16
- SO-8 (Duals) and 0.150" SO-16 (Quads)

	BW (Typ) MHz	SR (Typ) V/µs	V_{OS} (Max) µV	$ (100's)
LT1211 (D)	14	7	150/275	3.40
LT1212 (Q)	14	7	275	6.10
LT1213 (D)	28	12	150/275	3.40
LT1214 (Q)	28	12	275	6.10
LT1215 (D)	23	50	300/450	4.10
LT1216 (Q)	23	50	450	7.40

NEW AMPLIFIER ARCHITECTURE!

Voltage Feedback Op Amps with Current Feedback Speed

- Low Supply Current/Amplifier (1mA): LT1355/6
- Very High Slew Rate (1000V/µs): LT1363
- Low V_{OS} (0.6mV Maximum): LT1358/9
- Low Power (6mA/Amplifier for 1000V/µs Slew Rate)
- Fast Settling (80ns to 0.01%, 50ns to 0.1%, 10V Step)

Single	Dual	Quad	BW MHz	SR V/µs	I_S/Amp (mA)	$(100's) (Dual Amp)
LT1354	LT1355	LT1356	12	400	1	3.95
LT1357	LT1358	LT1359	25	600	2	4.10
LT1360	LT1361	LT1362	50	800	4	3.50
LT1363	LT1364	LT1365	70	1000	6	3.80

Voltage Feedback Op Amps

- 90ns Settling Time to 0.1%: LT1220, LT1226.
- 1mV Max V_{OS}, 300nA Max I_B: LT1220/1/2
- 12-Bit Accurate: LT1220/1/2.
- 10-Bit Accurate: LT1225/6

	BW (Typ) MHz	V_{OS} (Max) mV	A_V (Min) V/V	$ (100's)
LT1220	45	1	1	3.85
LT1221	37	1	4	3.85
LT1222	50	1	10	3.85
LT1225	30	1	5	2.85
LT1226	40	1	25	2.85

Current Feedback Amps

- Bandwidth Independent of Gain
- "Shutdown" Feature: LT1217, LT1223, LT1227.
- Single Supply Operation/Best for Video: LT1227, LT1229, LT1230.
- 12-Bit Accurate: LT1223
- Low Power (I_S=1mA): LT1217
- Lowest Cost: LT1252/3/4
- Operates on ±2V to ±15V Supplies*

* LT1223 & LT1217 Min Supply Voltage = ±5V

	BW (Typ) MHz	SR (Typ) V/µs	V_{OS} (Max) mV	$ (100's)
LT1227	140	1100	10	2.45
LT1223	100	1300	3	2.85
LT1229 (D)	100	1000	10	3.95
LT1230 (Q)	100	1000	10	7.25
LT1217	10	500	3	3.25
LT1252	100	250	15	1.75
LT1253 (D)	90	250	15	2.49
LT1254 (Q)	90	250	15	4.49

Low Cost Video Op Amps

- Specified Operation with ±5V and Single 5V Supplies
- Color Video Performance
- "Shutdown" Feature: LT1190/1/2
- Directly Drives Cables: 50mA I_{OUT}
- 450V/µs Slew Rate
- Low Power: LT1195

	BW (Typ) MHz	SR (Typ) V/µs	A_V (Min) V/V	$ (100's)
LT1190	50	450	1	1.65
LT1191	90	450	1	1.65
LT1192	350	450	5	1.65
LT1195	50	165	1	1.65

(D) = Dual, (Q) = Quad

Video Products

In addition to high speed amplifiers, LTC offers the following products tailored to video, multimedia and computer graphics applications.

Low Cost Dual/Triple 130MHz CFAs with Shutdown

- LT1260: Triple CFA for RGB Video, $4.49
- LT1259: Dual CFA with Shutdown, $3.95
- 90MHz Bandwidth on ±5V
- 0.1dB Gain Flatness, 30MHz: Good for HDTV
- 1600V/µs Slew Rate
- ±2V to ±15V Supply Range
- 100ns/40ns Turn On/Off Times
- Makes 2 or 3 Input MUX Amp
- Low Supply Current (5mA/Amp)
- Narrow SOIC Packages

±5V Video Difference Amps

- 50dB CMRR @ 10MHz
- Input Voltage Range: (–2.5V to 3.5V)
- ±4V Output Voltage Swing
- Color Video Performance
- "Shutdown" Feature
- Can Directly Drive Cables
- 500V/µs Slew Rate: LT1193/LT1194
- Low Power: LT1187/LT1189

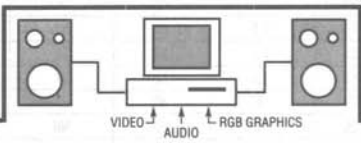
	Gain	A_V (Min) V/V	BW (Typ) MHz	$ (100's)
LT1187	Adj.	2	50	2.95
LT1189	Adj.	10	35	2.95
LT1193	Adj.	2	70	2.95
LT1194	10	–	350	2.95

Video Distribution Amplifier

- LT1206: 250mA Minimum Output Current
- 60MHz, 900V/µs Current Feedback Amplifier
- Drives 10 Video Cables
- Drives Low Impedance of High Capacitances
- Color Video Performance
- Low Current "Shutdown" Mode Available
- 8-Pin P DIP ($3.45), 7-Lead DD ($4.45), and 7-Lead TO-220 ($4.45)
- 8-Pin SOIC ($3.95)

2:1 and 4:1 Video Multiplexers Very Fast for Pixel Switching

- LT1203 (2:1), LT1205 (2 × 2:1 or 4:1)
- 150MHz, –3dB Bandwidth
- 90dB Channel Separation
- 30MHz, 0.1dB Gain Flatness (HDTV)
- 25ns Channel Switching Time
- 50mV Switching Transient
- 10MΩ Disabled Output Impedance
- Expandable
- 8- and 16-Pin Narrow SOIC Packages
- LT1203 PDIP $2.85, LT1205CS $5.30



4:1 Video Multiplexer with

- LT1204: 4:1 MUX w/ Current Feedback Amp
- 0.1dB Gain Flatness to >30MHz: for HDTV
- 1000V/µs Slew Rate
- 75MHz, –3dB Bandwidth (A_V = 2)
- 90dB Channel Separation
- Expandable
- 16-Pin SOL and P DIP Packages
- PDIP $4.95, SOL $5.40

Current Feedback Amp with DC Gain Control

- LT1228: 75MHz Transconductance Amp with 100MHz Current Feedback Amplifier
- Color Video Performance
- Differential Input
- Operates on ±2V to ±15V Supplies
- For Auto-Gain, Tunable Filters, and Specialized Video Circuits.

Video Fader/Gain-Controlled Amplifier

- LT1251: 40MHz Video Fader
- LT1256: 40MHz Gain-Controlled Amplifier
- Accurate 1% Linear Gain Control
- Low Differential Gain/Phase, 0.1%/0.1%

Multimedia

Multimedia systems combine **audio, composite video** (broadcast quality TV) and **high resolution computer graphics**. Typical requirements are:

Video: NTSC or **PAL** need minimum 50MHz, –3dB bandwidth
HDTV needs 0.1dB flatness to 30MHz

Suggested Products (Refer to above and reverse):

General Purpose Gain Blocks/Video A/D Buffers	LT1360/63: Single/Dual/Quad Voltage Feedback Op Amps with Current Feedback Speed
	LT1227/29/30: Single/Dual/Quad Current Feedback Amplifiers
	LT1252/3/4: Low Cost Curent Feedback Amplifiers
Multiplexer	LT1204: 4:1 Video MUX with Current Feedback Amplifier
Video Distribution	LT1206: 250mA Output Current Feedback Amplfiers
DC Restoration	LT1228: Current Feedback Amplifier with Gain Control
Gain Control	LT1228: Current Feedback Amplifier with Gain Control
COAX Loopthrough/ Twisted-Pair Receiver	LT1187/89/93/94: Video Difference Amplifiers

Graphics: VGA needs >50MHz, **19" monitors** need >100MHz

RGB, YUV, YC, Amps	LT1259/60: Dual/Triple, 130MHz, 1800V/µs Current Feedback Amplifiers with Shutdown
Pixel Switching	LT1203/05: 2:1 and 4:1 Video Multiplexers

Audio: For 8× Oversampling, 200kHz Bandwidth is Required

Gain Blocks	LT1115: Low Noise Preamplifier
	LT1124/26: Dual Low Noise Preamplifier
	LT1211/12: High Slew Rate, Single Supply Dual/Quad Op Amps
	LT1122: Ultra-Low Distortion Op Amp with Symmetric Slew Rates.
	LT1355/56: Ultra-High Slew Rate, Low Supply Current Op Amps

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS						PACKAGES AVAILABLE	MIL/ IND TEMP	IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)			
SINGLE									
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	M	Extremely Low Offset Voltage, Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8, S8	M	
LT1006AC	50	1.3	15	1000	0.25	24†	H, J8	M	Single Supply Operation, Fully Specified for 5V Supply
LT1006C	80	1.8	25	700	0.25	24†	H, J8, N8	M	
LT1006S8	400	3.5	25	700	0.25	25	S8		
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	M	Extremely Low Noise, Low Drift
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8, S8	M,I	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	M, I	Low Bias Current, Low Power
LT1012C	25	0.6	100	300	0.1	30	H, N8	M, I	Low V_{OS}, Low Power
LT1012AC	50	1.5	0.15	200	0.1	30	H, N8	M	
LT1012D	60	1.7	150	200	0.1	30	H, N8		
LT1012S8	120	1.8	0.28	200	0.1	30	S8		
LT1022AC	250	5.0	0.05	150	23	50	H	M	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022C	600	9.0	0.05	120	18	60	H	M	
LT1022CN8	1000	15.0	0.05	100	18	60	N8		
LT1028AC	40	0.8	90	7000	11	1.7	H, J8, N8	M	Lowest Noise, High Speed, Low Drift
LT1028C	80	1.0	180	5000	11	1.9	H, J8, N8, S	M	
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	M	Extremely Low Noise, High Speed
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8, S8	M, I	
LT1055AC	150	4	0.05	150	10	50	H	M	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055C	400	8	0.05	120	7.5	60	H	M	
LT1055CN8	700	12	0.05	120	7.5	60	N8		
LT1055S8	1500	15	0.1	120	7.5	70	S8		
LT1056AC	180	4	0.05	150	12	50	H	M	
LT1056C	450	8	0.05	120	9	60	H	M	
LT1056CN8	800	12	0.05	120	9	60	N8		
LT1056S8	1500	15	0.1	120	9.0	70	S8		
LT1077AC	40	0.4	9	250	0.12	40	H, J8, N8	M, I	Micropower, Single Supply, Precision, Low Noise
LT1077C	60	0.4	11	200	0.12	29†	H, J8, N8	M, I	
LT1077S8	150	3.0	11	240	0.05	28†	S8		
LT1097C	50	1.0	0.250	700	0.1	16†	N8	I	Low Cost, Low Power Precision
LT1097S8	60	1.4	0.350	700	0.1	16†	S8	I	
LT1115C	280	0.5 (Typ)	380	2000	10	1.8	N8, S		Lowest Noise, Ultra Low Distortion Audio Optimized Op Amp
LT1128AC	40	1.0	90	7000	5.0	1.7	J8, N8, S8	M, I	Lowest Noise, High Speed, Precision
LT1128C	80	1.0	180	5000	4.5	1.9	J8, N8, S8	M, I	
LTC1049C	10	0.1	0.050	3162	0.8†	1.0μV_{P-P}**	J8, N8	M, I	Auto Zeroed Precision Op Amp, No External Capacitors Required
LTC1050AC	5	0.05	0.035	3162	4†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	
LTC1050C	5	0.05	0.050	1000	4†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	
LTC1052C	5	0.05	0.03	1000	3†	0.5μV_{P-P}**	H, N8, N	M, I	Low Noise, Auto Zeroed Precision Op Amp
LTC7652C	5	0.05	0.03	1000	3†	0.5μV_{P-P}**	H, N8	M, I	
LTC1150C	5	0.05	0.03	10000	3†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	Auto Zeroed Precision Op Amp That Operates on Standard ±15V Supplies. No External Capacitors Required
LTC1152C	10	0.1	0.1	316	1†	0.5μV_{P-P}	N8, S8		Rail-to-Rail Input and Output. Auto Zeroed Precision Op Amp. C-Load™ Stable.
LTC1250C	10	0.05	0.02	10000	10†	0.3mV_{P-P}**	J8, N8, S8	M	Low Noise, Auto Zeroed Precision Op Amp

† Typical spec * 100Hz noise ** DC to 1Hz noise C-Load is a trademark of Linear Technology Corporation

NOTE: See page 14-3 for DESC cross reference numbers. Check data sheet for specifications on industrial and military temperature produced and surface mount.

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS						PACKAGES AVAILABLE	MIL/ IND TEMP	IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)			
SINGLE									
LF355A	2000	5	0.05	75	5	25†*	H, N8		JFET Inputs, Low I_B, No Phase Reversal
LF356A	2000	5	0.05	75	10	15†*	H, N8		
LM10B	2000	2†	20	120	—	50†	H, J8	M	On-Chip Reference Operates with +1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8		
LM10C	4000	5†	30	80	—	50†	H, J8, N8		
LM10CL	4000	5†	30	80	—	50†	H, J8, N8		
LM308A	500	5	7	60	0.1	30†	H, N8	M	Low Bias, Supply Current
LT318A	1000		250	200	50	42†	H, J8, N8	M	High Speed, 15MHz
LM318	10000		500	25	50	42†	H, J8, N8, S8	M	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	M	Low Noise, Low Offset Drift with Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	M	
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8, S8	M	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	M	
OP-15E	500	5	0.05	100	10	20†*	H, N8	M	Precision JFET Input, Low Bias Current, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	20†*	H, N8	M	
OP-15G	3000	15	0.2	50	5	20†*	H, N8	M	
OP-16E	500	5	0.05	100	18	20†*	H, N8	M	Precision JFET Input, High Speed, No Phase Reversal
OP-16F	1000	10	0.1	75	12	20†*	H, N8	M	
OP-16G	3000	15	0.2	50	9	20†*	H, N8	M	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	I	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	I	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	I	Very Low Noise, Stable for Gains ≥ 5
OP-37G	100	1.8	80	700	11	8.0	H, N8	I	
OP-97E	25	0.6	±0.1	300	0.1	30	H, N8	M	Low Power, Low I_B, Precision
DUAL									
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	M	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	M	
LT1013AC	150	2.0	20	1500	0.2	24†	H, J8	M	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	24†	H, J8, N8	M, I	
LT1013D	800	5.0	30	1200	0.2	24†	N8, S8		
LT1024AC	50	1.5	0.12	250	0.1	33	N	M	Low V_{OS}, Low Power, Matching Specs
LT1024C	100	2.0	0.20	180	0.1	33	N	M	
LTC1047C	10	0.01	0.02	1000	0.2†	0.8mVp-p**	N8, S		No External Capacitors Required Dual, Precision Auto Zeroed Op Amp
LTC1051C	5	0.05	0.05	1000	4†	0.4μVp-p**	J8, N8, S	M, I	
LT1057AC	450	7	0.05	150	10	26†	H, J8	M	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057ACN8	450	10	0.05	150	10	26†	N8		
LT1057C	800	12	0.075	100	8	26†	H, J8	M, I	
LT1057CN8	800	16	0.075	100	8	26†	N8, S8	I	
LT1078AC	70	2.0	8	250	0.07†	40	H, J8, N8	M	Micropower, Precision, Single Supply, Low Noise Dual
LT1078C	120	2.5	10	200	0.07†	29†	H, J8, N8, S8	M, I	
LT1112A	60	0.50	0.25	1000	0.16	15†	J8, N8, S8	M, I	Low Power, Precision, Matching Specs
LT1112C	75	0.75	0.28	800	0.16	15†	J8, N8, S8	M, I	
LT1113AC	1500	15	0.45	1200	2.5	17†	N8, J8, S8	M, I	Dual Low Noise, Precision JFET Input
LT1113C	1800	20	0.48	1000	2.5	17†	N8, J8, S8	M, I	
LT1124AC	70	1	55	2000	3	5.5	N	M, I	Dual Precision Op Amp, Low Noise, High Speed
LT1124C	100	1.5	70	1500	2.7	5.5	J, N, S	M, I	

† Typical spec * 100Hz noise ** DC to 1Hz noise **NOTE:** See page 14-3 for DESC cross reference numbers

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	MIL/ IND TEMP	
DUAL									
LT1126AC	70	1.0	20	2000	8	5.5	N8	M, I	Dual Precision Op Amp, Low Noise, High Speed
LT1126C	100	1.5	30	1500	8	5.5	J8, N8, S8	M, I	
LT1169A	1500	15	3	1200	2.4	17†	J8, N8, S8		Dual Low Noise, Picoampere Bias Current JFET Input Op Amp
LT1169C	1800	20	5	1000	2.4	17†	J8, N8, S8		
LT1178AC	70	2.2	5	140	0.013	75	H, J8, N8		17μA Max, Single Supply, Precision Dual
LT1178C	120	3.0	6	110	0.013	50†	H, J8, N8	I	
LT1211C	275	0.6	125	250	4	12.5	J8, N8, S8	M, I	Fast, Precise, Single Supply Op Amps. Industrial Temperature (−40°C to 85°C) Specs Included with Commercial Temperature Devices
LT1211AC	150	0.5	100	250	4	12.5	J8, N8, S8	M, I	
LT1213C	275	0.6	200	250	8.5	10	J8, N8, S8	M, I	
LT1213AC	150	0.5	160	250	8.5	10	J8, N8, S8	M, I	
LT1215C	450	1.0	600	150	30	15	J8, N8, S8		
LT1215AC	300	0.8	500	150	30	15	J8, N8, S8		
LT1413AC	150	2	15	400	0.2	24†	N8	I	Dual Single Supply Precision Op Amp Optimized for 5V and GND
LT1413C	280	2.5	18	350	0.2	24†	N8, S8	I	
LT1413S	380	2.5	18	350	0.2	24†	S8		
LT1457C	800	16	0.075	100	2	28	N8, S8		Dual Precision JFET Input Op Amp. C-Load Stable
LF412AC	1000	10	0.1	100	10	20†*	H, J8, N8	M	High Performance Dual JFET Input Op Amp
OP-215E	1000	10	0.1	150	10	20†*	H, J8, N8	M	
OP-215G	3000	20	0.2	50	8	20†*	H, J8, N8	M	
OP-227E	80	1.0	40	3000	1.7	6	J, N	M	Dual Matched OP-27
OP-227G	180	1.8	80	2000	1.7	9	J, N	M	
OP-237E	80	1.0	40	3000	10	6	J, N	M	Dual Matched OP-37
OP-237G	180	1.8	80	2000	10	9	J, N	M	
OP-270A	75	1	20	750	1.7	6.5	J	M	Dual Op Amp, Low Noise
OP-270C	250	3	60	350	1.7	3.6†	N, S	M	
QUAD									
LT1014AC	180	2.0	20	1500	0.2	24†	J	M	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	24†	J, N	M, I	
LT1014D	800	5.0	30	1200	0.2	24†	N, S		
LT1058AC	600	10	0.05	150	10	26†	J	M	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058C	1000	15	0.075	100	8	26†	J, N, S	M, I	
LT1079AC	120	2.0	8	250	0.07†	40	J, N	M	Micropower, Precision, Single Supply, Low Noise Quad
LT1079C	150	2.5	10	200	0.07†	29†	J, N, S	M, I	
LT1114AC	60	0.50	0.25	1000	0.16	15†	J8, N8, S8	M, I	Low Power, Precision, Matching Specs
LT1114C	75	0.75	0.28	800	0.16	15†	J8, N8, S8	M, I	
LT1125AC	90	1	20	2000	3	5.5	N	M	Precision Quad Op Amp, Low Noise, High Speed
LT1125C	140	1.5	30	1500	2.7	5.5	J, N, S	M, I	
LT1127AC	90	1.0	20	2000	8	5.5	N	M	
LT1127C	140	1.5	30	1500	8	5.5	N, J, S	M, I	
LT1179AC	100	2.2	5	140	0.013	75	J, N		17μA Max, Single Supply, Precision Quad
LT1179C	150	3.0	6	110	0.013	50†	J, N	I	
LT1212C	275	0.6	125	250	4	12.5	N, S	I	Fast, Precise, Single Supply Op Amps. Industrial Temperature (−40°C to 85°C) Specs Included with Commercial Temperature Devices
LT1214C	275	0.6	200	250	8.5	10	N, S	I	
LT1216C	450	1.0	600	150	30	15	N, S	I	
LTC1053C	5	0.05	0.05	1000	4†	0.4μVp-p**	N, S	I	Quad, Precision Auto Zeroed Op Amp. No External Capacitors Required
OP-470A	400	2	25	500	1.4	6.5	J	M	Quad Op Amp, Low Noise
OP-470C	1000	2†	60	400	1.4	6.5	N, S		

† Typical spec * 100Hz noise ** DC to 1Hz noise

NOTE: See page 14-3 for DESC cross reference numbers

High Speed Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	MIN SLEW RATE (V/µs)	TYP SETTLING TIME TO 0.1 % (µs)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (µV)	I_B MAX (nA)	PACKAGES AVAILABLE	MIL/ IND TEMP	
SINGLE									
LT1122AC	60	0.340* 0.540**	14	180	600	0.075	J8, N8	M	JFET Input. Faster and Better DC Specs Than OP-42. A and C Have Grades 100% Tested Settling Time
LT1122BC	60	0.350*	14	180	600	0.075	J8, N8	M	
LT1122CC	50	0.350* 0.590**	13	150	900	0.1	J8, N8, S8	M	
LT1122DC	50	0.360*	13	150	900	0.1	J8, N8, S8	M	
LT1187C	130	0.1***	50 (A_V = 2)		10000	2000	N8, S8		Low Power Video Difference Amplifier
LT1189C	175	1***	35 (A_V = 10)		3000	2000	N8, S8		
LT1190C	450†	0.1	50	3.5	10000	2500	J8, N8, S8	M	±5V Supply Color Video Op Amps
LT1191C	450†	0.1	90	6	5000	2500	J8, N8, S8	M	
LT1192C	450†	0.1	400 ($A_V \geq 5$)	16	2.5	2500	J8, N8, S8	M	
LT1193C	450†	0.1	70		12000	3500	J8, N8, S8	M	Color Video Differential Amplifier
LT1194C	450†	0.1	40		6000	3500	J8, N8, S8	M	
LT1195C	140	0.22***	50	0.5	8000	2000	J8, N8, S8		Low Power, High Speed
LT1200C	30	0.430	11.0	4	1000	1000	N8, S8		Low Supply Current Op Amp
LT1206C	600		50	0.6	15000	20000	N8, R, Y, S8		250mA Current Feedback Amplifier
LT1217C	100	280	10.0	3.2	3000	500	N8, S8		Low Power Current Feedback Amplifier
LT1220C	200	0.09	45	20	1000	300	N8		Ultra High Speed, Good DC Specs
LT1221C	200	0.09	150 ($A_V \geq 4$)	50	1000	300	N8		
LT1222C	200	0.09	500 ($A_V \geq 10$)	100	1000	300	N8		
LT1223C	800	0.075	100	3.2	3000	3000	J8, N8, S8	M	Current Feedback Amplifier
LT1224C	250	0.090	45	3.3	2000	8000	J8, N8, S8	M	High Speed, DC Precision, Can Drive Unlimited Capacitive Load While Remaining Stable
LT1225C	250	0.070	150 ($A_V \geq 5$)	12.5	1000	8000	J8, N8, S8	M	
LT1226C	250	0.075	1000 ($A_V \geq 25$)	50	1000	8000	J8, N8, S8	M	
LT1227C	500	0.050	140.0	0.6	10000	10000	J8, N8, S8	M	Current Feedback Amplifier
LT1228C	300	0.045	100	0.6	10000	10000	J8, N8, S8	M	Electronic DC Gain Control
LT1252C	250		100	0.56	15000	15000	N8, S8		Low Cost Video Amplifier
LT1354C	200	0.280	12	12	800	300	N8, S8		1mA, 12MHz, 400V/µs C-Load
LT1357C	300	0.220	25	20	600	500	N8, S8		2mA, 25MHz, 600V/µs C-Load
LT1360C	600	0.090	50	4.5	1000	1000	N8, S8		4mA, 50MHz, 800V/µs C-Load
LT1363C	750	0.080	70	4.5	1500	2000	N8, S8		6mA, 70MHz, 1000V/µs C-Load
DUAL									
LT1201C	30	330	12	4	2000	1000	N8, S8		1mA, 12MHz, 50V/µs Dual C-Load
LT1208C	250	0.090	45	3.3	3000	8000	N8, S8		45MHz, 450µs Dual C-Load
LT1211C	5	2.2	14	1200	550	120	N8, S8		14MHz, 7V/µs Single Supply Precision
LT1211A	5	2.2	14	1200	400	95	N8, S8		
LT1213C	10	1.1	28	1200	550	190	N8, S8		28MHz, 12V/µs, Single Supply Precision
LT1213A	10	1.1	28	1200	400	150	N8, S8		
LT1215C	40	0.480	23	1000	650	550	N8, S8		23MHz, 50V/µs, Single Supply Precision
LT1215 A	40	0.480	23	1000	500	500	N8, S8		
LT1229C	300	0.045	100	0.6	650	550	J8, N8, S8	M	Fast Slew Rate, Current Feedback Architecture
LT1253C	250		90	0.560	15000	15000	N8, S8		Low Cost Video Amplifier
LT1259C	900	0.075	130	0.71	10000	3000	N14, S14		Low Cost 130MHz Dual CFAs with Individual Shutdowns
LT1355C	200	0.023	12	12	800	300	N8, S8		1mA, 12MHz, 400V/µs Dual C-Load
LT1358C	300	0.220	25	20	600	500	N8, S8		2mA, 25MHz, 600V/µs Dual C-Load
LT1361C	600	0.090	50	4.5	1000	1000	N8, S8		4mA, 50MHz, 800V/µs Dual C-Load
LT1364C	750	0.080	70	4.5	1500	2000	N8, S8		6mA, 70MHz, 1000V/µs Dual C-Load

†Typical value *10V step, to 1mV at sum node. **Maximum value, 10V step, to 1mV at sum node. ***3V Step

NOTE: See page 14-3 for DESC cross reference numbers

High Speed Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	MIN SLEW RATE (V/µs)	TYP SETTLING TIME TO 0.1 % (µs)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (µV)	I_B MAX (nA)	PACKAGES AVAILABLE	MIL/ IND TEMP	
TRIPLE									
LT1260C	900	0.075	130	0.71	10000	3000	N16, S16		Low Cost Triple 130MHz CFAs with Individual Shutdowns
QUAD									
LT1202C	30	0.330	12	4	2000	1000	N14, S16		1mA, 12MHz, 50V/µs Quad C-Load
LT1209C	250	0.090	45	3.3	3000	8000	N14, S16		45MHz, 450V/µs Quad C-Load
LT1212C	5	2.2	14	1200	550	120	N14, S16		14MHz, 7V/µs Single Supply Precision
LT1214C	10	1.1	28	1200	550	190	N14, S16		28MHz, 12V/µs, Single Supply Precision
LT1216C	40	0.480	23	1000	650	550	N14, S16		23MHz, 50V/µs, Single Supply Precision
LT1230C	300	0.045	100	0.6	15000	10000	J, N, S		Fast Slew Rate, Current Feedback Architecture
LT1254C	250		90	0.560	15000	15000	N14, S14		Low Cost Video Amplifier
LT1356C	200	0.280	12	12	800	300	N14, S16		1mA, 12MHz, 400V/µs Quad C-Load
LT1359C	300	0.220	25	20	600	500	N14, S16		2mA, 25MHz, 600V/µs Quad C-Load
LT1362C	600	0.090	50	4.5	1000	1000	N14, S16		4mA, 50MHz, 800V/µs Quad C-Load
LT1365C	750	0.080	70	4.5	1500	2000	N14, S16		6mA, 70MHz, 1000V/µs Quad C-Load

†Typical value *10V step, to 1mV at sum node. **Maximum value, 10V step, to 1mV at sum node. ***3V Step

NOTE: See page 14-3 for DESC cross reference numbers

SECTION 2—AMPLIFIERS

PRECISION OPERATIONAL AMPLIFIERS

LT1028/LT1128, Ultra Low Noise Precision High Speed Op Amps 2-12
LT1112/LT1114, Dual/Quad Low Power Precision, Picoamp Input Op Amps 2-29
LT1113, Dual Low Noise, Precision, JFET Input Op Amps 2-40
LT1169, Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp 2-55
LT1178S8, 20μA Max, Dual SO-8 Package, Single Supply Precision Op Amp 2-67
LT1413, Single Supply, Dual Precision Op Amp 2-68
LT1457, Dual, Precision JFET Input Op Amp 2-76

Ultra Low Noise Precision High Speed Op Amps

FEATURES

- Voltage Noise
  - 1.1nV/√Hz Max. at 1kHz
  - 0.85nV/√Hz Typ. at 1kHz
  - 1.0nV/√Hz Typ. at 10Hz
  - $35nV_{P-P}$ Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product
  - LT1028: 50MHz Min.
  - LT1128: 13MHz Min.
- Slew Rate
  - LT1028: 11V/μs Min.
  - LT1128: 5V/μs Min.
- Offset Voltage: 40μV Max.
- Drift with Temperature: 0.8μV/°C Max.
- Voltage Gain: 7 Million Min.
- Available in 8-Pin SO Package

APPLICATIONS

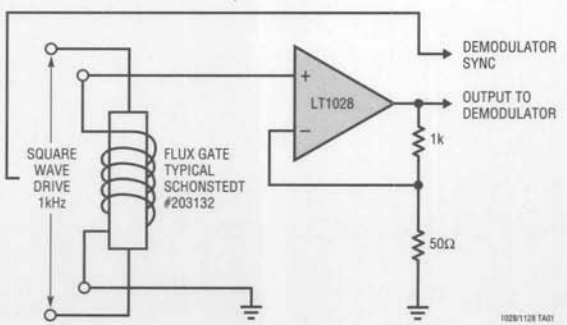
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplfiers

DESCRIPTION

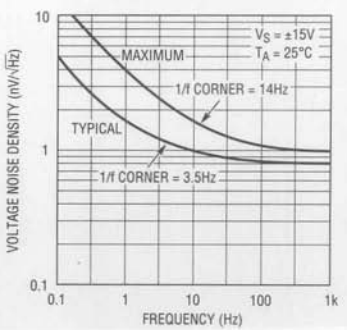
The LT1028(gain of –1 stable)/LT1128(gain of +1 stable) achieve a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for LT1028, 20MHz for LT1128), distortion-free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028/LT1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 25nA.

The LT1028/LT1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028/LT1128's contribution to total system noise will be negligible.

Flux Gate Amplifier



Voltage Noise vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- –55°C to 105°C ..... ±22V
- 105°C to 125°C ..... ±16V

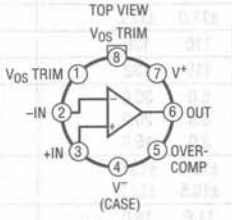
Differential Input Current (Note 8) ..... ±25mA
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite

Operating Temperature Range
- LT1028/LT1128AM, M ..... –55°C to 125°C
- LT1028/LT1128AC, C ..... –40°C to 85°C

Storage Temperature Range
- All Devices ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

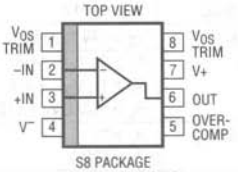


H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 175°C, θ_{JA} = 140°C/W, θ_{JC} = 40°C/W

ORDER PART NUMBER

LT1028AMH
LT1028MH
LT1028ACH
LT1028CH



S8 PACKAGE
8-LEAD PLASTIC SOIC

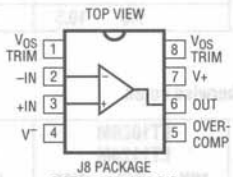
T_{JMAX} = 135°C, θ_{JA} = 140°C/W

ORDER PART NUMBER

LT1028CS8
LT1128CS8

S8 PART MARKING

1028
1128

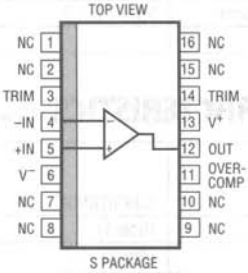


J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 165°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 130°C, θ_{JA} = 130°C/W (N8)

LT1028AMJ8
LT1028MJ8
LT1028ACJ8
LT1028CJ8
LT1028ACN8
LT1028CN8
LT1128AMJ8
LT1128MJ8
LT1128CJ8
LT1128ACN8
LT1128CN8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 140°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1028CS

NOTE: THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS.

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC LT1128AM/AC MIN	TYP	MAX	LT1028M/C LT1128M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		µV/Mo
I_{OS}	Input Offset Current	V_{CM} = 0V		12	50		18	100	nA
I_B	Input Bias Current	V_{CM} = 0V		±25	±90		±30	±180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nV_{P-P}

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM/AC LT1128AM/AC MIN	TYP	MAX	LT1028M/C LT1128M/C MIN	TYP	MAX	UNITS
	Input Noise Voltage Density	f_O = 10Hz (Note 4) f_O = 1000Hz, 100% tested			1.00 0.85	1.7 1.1		1.0 0.9	1.9 1.2	nV/√Hz nV/√Hz
I_n	Input Noise Current Density	f_O = 10Hz (Note 3 and 5) f_O = 1000Hz, 100% tested			4.7 1.0	10.0 1.6		4.7 1.0	12.0 1.8	pA/√Hz pA/√Hz
	Input Resistance Common Mode Differential Mode				 300 20			 300 20		 MΩ kΩ
	Input Capacitance				5			5		pF
	Input Voltage Range			±11.0	±12.2		±11.0	±12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$		114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$		117	133		110	132		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm 12V$ $R_L \geq 1k$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$		7.0 5.0 3.0	30.0 20.0 15.0		5.0 3.5 2.0	30.0 20.0 15.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$ $R_L \geq 600\Omega$		±12.3 ±11.0	±13.0 ±12.2		±12.0 ±10.5	±13.0 ±12.2		V V
SR	Slew Rate	$A_{VCL} = -1$ $A_{VCL} = -1$	LT1028 LT1128	11.0 5.0	15.0 6.0		11.0 4.5	15.0 6.0		V/μs V/μs
GBW	Gain-Bandwidth Product	f_O = 20kHz (Note 6) f_O = 200kHz (Note 6)	LT1028 LT1128	50 13	75 20		50 11	75 20		MHz MHz
Z_O	Open-Loop Output Impedance	$V_O = 0$, $I_O = 0$			80			80		Ω
I_S	Supply Current				7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM LT1128AM MIN	TYP	MAX	LT1028M LT1128M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	120		45	180	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note7)	●		0.2	0.8		0.25	1.0	μV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	●		25	90		30	180	nA
I_B	Input Bias Current	V_{CM} = 0V	●		±40	±150		±50	±300	nA
	Input Voltage Range		●	±10.3	±11.7		±10.3	±11.7		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 16V$	●	110	130		104	130		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm 10V$ $R_L \geq 1k$, $V_O = \pm 10V$	●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$	●	±10.3	±11.6		±10.3	±11.6		V
I_S	Supply Current		●		8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AC LT1128AC MIN	LT1028AC LT1128AC TYP	LT1028AC LT1128AC MAX	LT1028C LT1128C MIN	LT1028C LT1128C TYP	LT1028C LT1128C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		15	80		30	125	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note7)	●		0.1	0.8		0.2	1.0	µV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	65		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±30	±120		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	110	124		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	114	132		107	132		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \ge 2k$, $V_O = \pm 10V$ $R_L \ge 1k$, $V_O = \pm 10V$	●	5.0 4.0	25.0 18.0		3.0 2.5	25.0 18.0		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k$ $R_L \ge 600\Omega$ (Note 9)	●	±11.5 ±9.5	±12.7 ±11.0		±11.5 ±9.0	±12.7 ±10.5		V V
I_S	Supply Current		●		8.0	10.5		8.2	11.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS		LT1028AC LT1128AC MIN	LT1028AC LT1128AC TYP	LT1028AC LT1128AC MAX	LT1028C LT1128C MIN	LT1028C LT1128C TYP	LT1028C LT1128C MAX	UNITS
V_{OS}	Input Offset Voltage		●		20	95		35	150	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift		●		0.2	0.8		0.25	1.0	µV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		20	80		28	160	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±35	±140		±45	±280	nA
	Input Voltage Range		●	±10.4	±11.8		±10.4	±11.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	108	123		102	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	112	131		106	131		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \ge 2k$, $V_O = \pm 10V$ $R_L \ge 1k$, $V_O = \pm 10V$	●	4.0 3.0	20.0 14.0		2.5 2.0	20.0 14.0		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k$	●	±11.0	±12.5		±11.0	±12.5		V
I_S	Supply Current		●		8.5	11.0		8.7	12.5	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot with the exception of the S8 and S16 packages. Devices 100% tested at 10Hz are available on request.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 7: This parameter is not 100% tested.

Note 8: The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

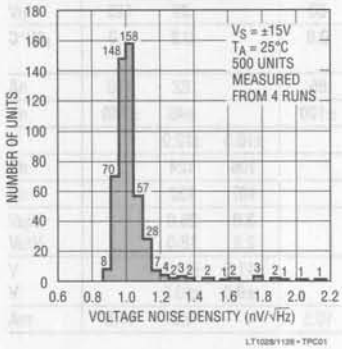
Note 9: This parameter guaranteed by design, fully warmed up at $T_A = 70°C$. It includes chip temperature increase due to supply and load currents.

Note 10: The LT1028/LT1128 are not tested and are not quality-assurance-sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and /or 125°C tests.

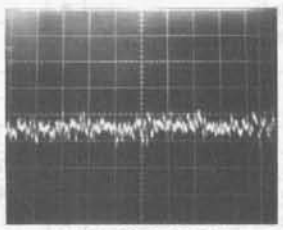
2

TYPICAL PERFORMANCE CHARACTERISTICS

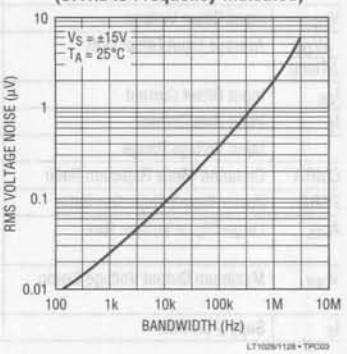
10Hz Voltage Noise Distribution



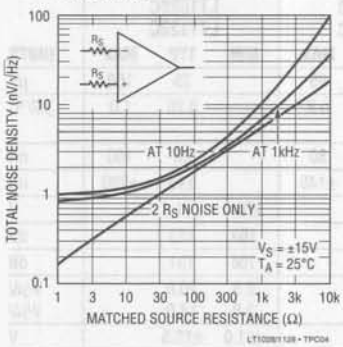
Wideband Noise, DC to 20kHz



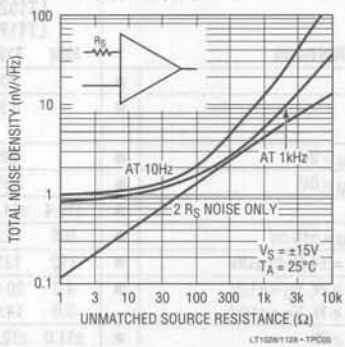
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



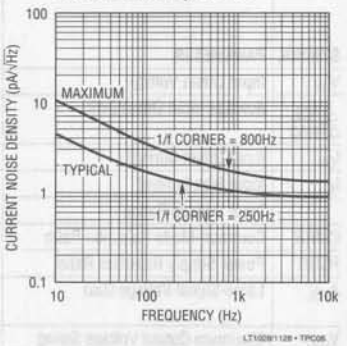
Total Noise vs Matched Source Resistance



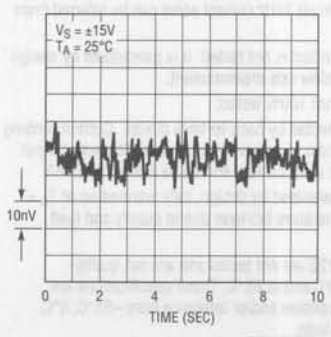
Total Noise vs Unmatched Source Resistance



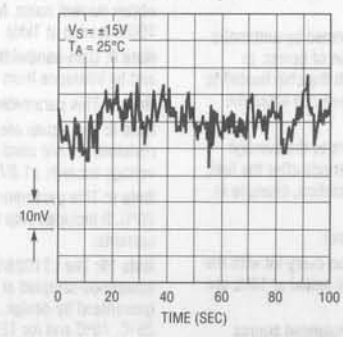
Current Noise Spectrum



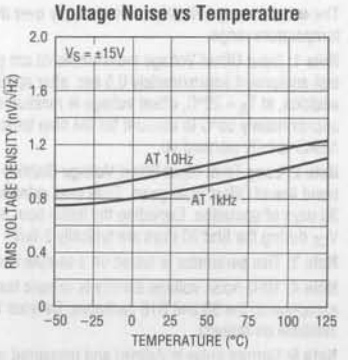
0.1Hz to 10Hz Voltage Noise



0.01Hz to 1Hz Voltage Noise

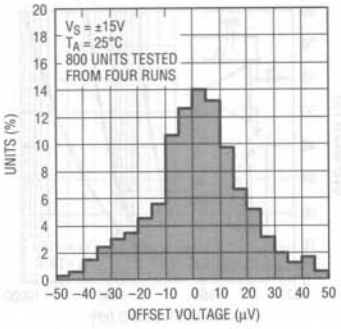


Voltage Noise vs Temperature

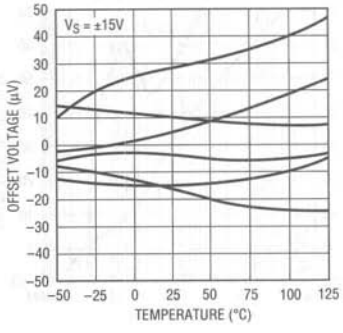


TYPICAL PERFORMANCE CHARACTERISTICS

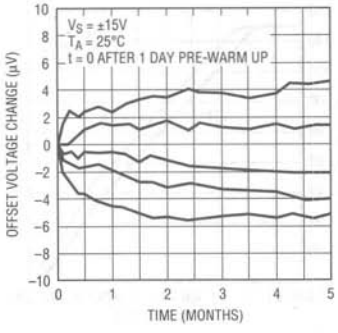
Distribution of Input Offset Voltage



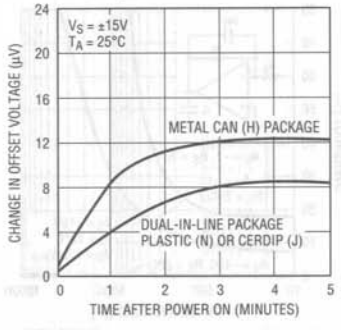
Offset Voltage Drift with Temperature of Representative Units



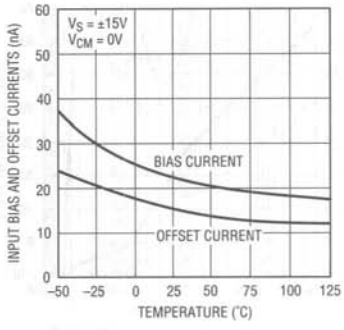
Long-Term Stability of Five Representative Units



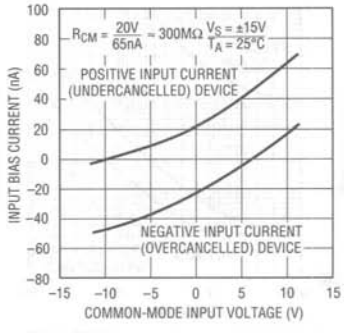
Warm-Up Drift



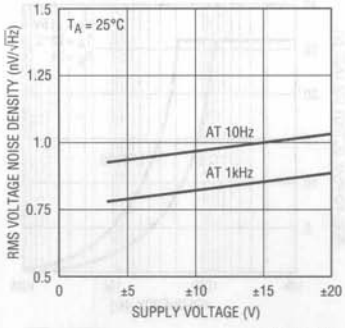
Input Bias and Offset Currents Over Temperature



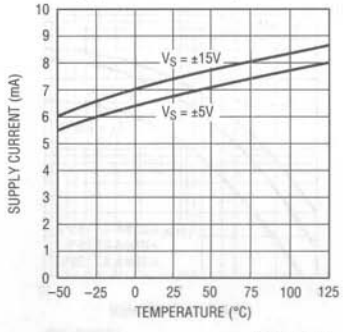
Bias Current Over the Common-Mode Range



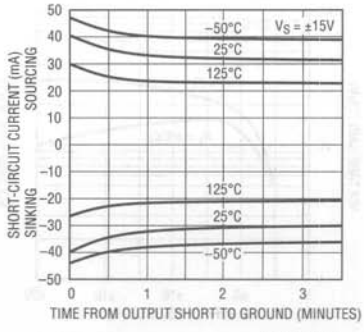
Voltage Noise vs Supply Voltage



Supply Current vs Temperature



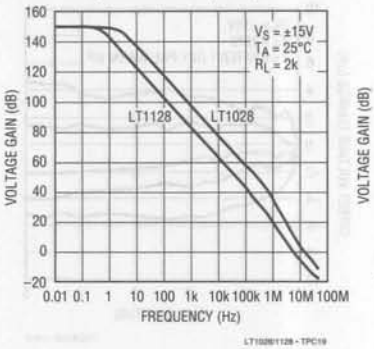
Output Short-Circuit Current vs Time



2

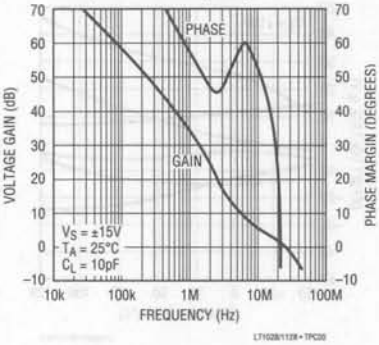
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain vs Frequency



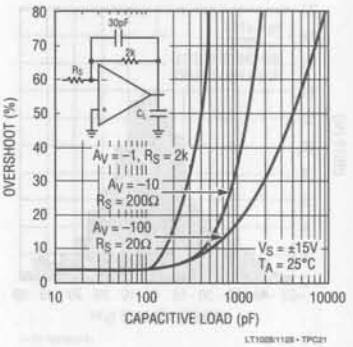
LT1028/1128 • TPC19

LT1028
Gain, Phase vs Frequency



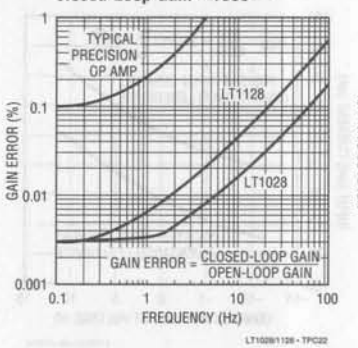
LT1028/1128 • TPC20

LT1028
Capacitance Load Handling



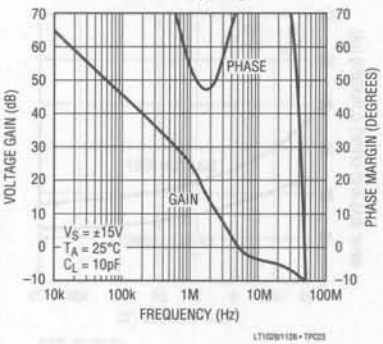
LT1028/1128 • TPC21

Gain Error vs Frequency
Closed-Loop Gain = 1000



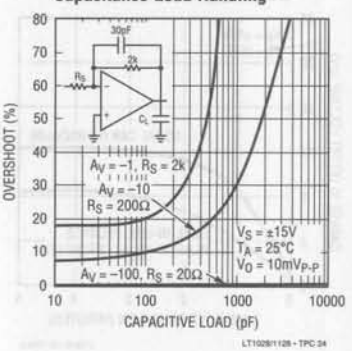
LT1028/1128 • TPC22

LT1128
Gain Phase vs Frequency



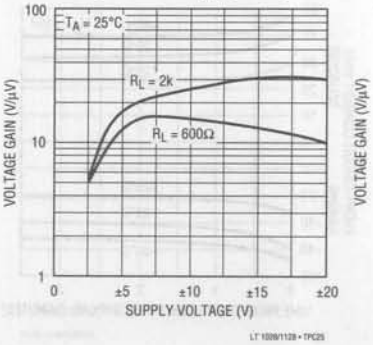
LT1028/1128 • TPC23

LT1128
Capacitance Load Handling



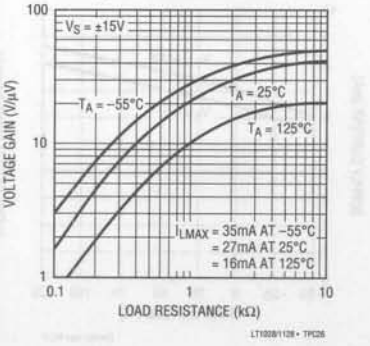
LT1028/1128 • TPC 24

Voltage Gain vs Supply Voltage



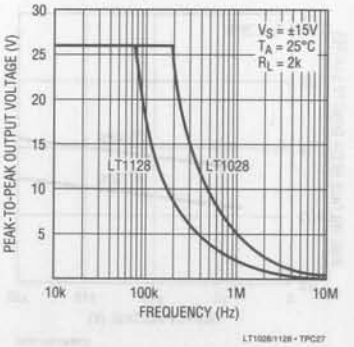
LT 1028/1128 • TPC25

Voltage Gain vs Load Resistance



LT1028/1128 • TPC26

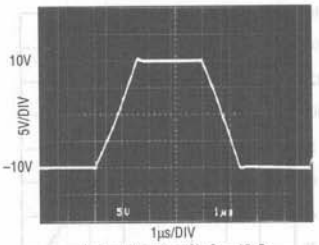
Maximum Undistorted Output
vs Frequency



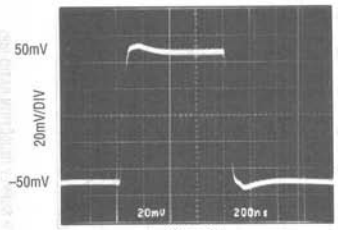
LT1028/1128 • TPC27

TYPICAL PERFORMANCE CHARACTERISTICS

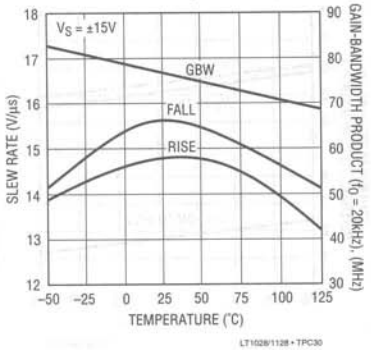
LT1028
Large-Signal Transient Response



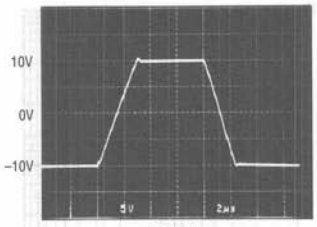
LT1028
Small-Signal Transient Response



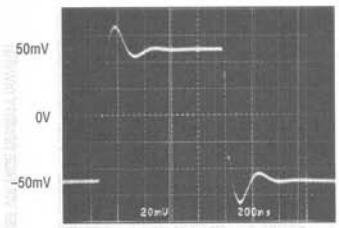
LT1028
Slew Rate, Gain-Bandwidth Product Over Temperature



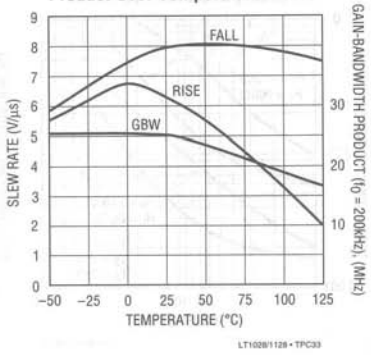
LT1128
Large-Signal Transient Response



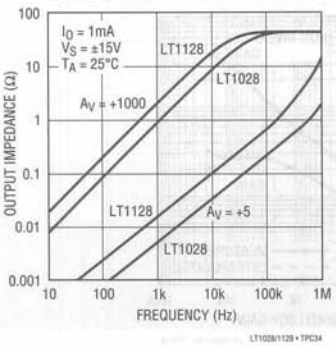
LT1128
Small-Signal Transient Response



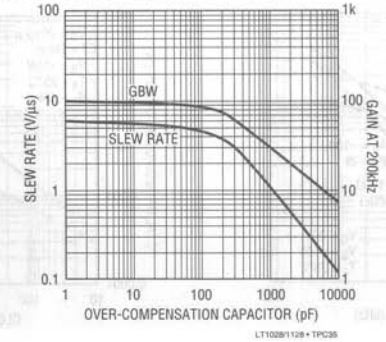
LT1128
Slew Rate, Gain-Bandwidth Product Over Temperature



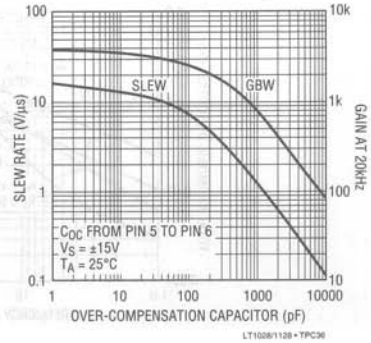
Closed-Loop Output Impedance



LT1128
Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor



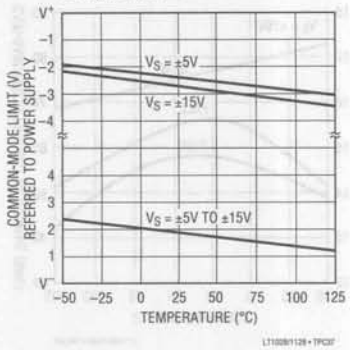
LT1028
Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor



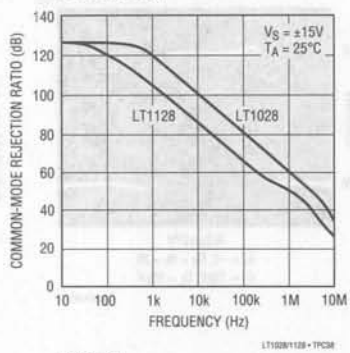
2

TYPICAL PERFORMANCE CHARACTERISTICS

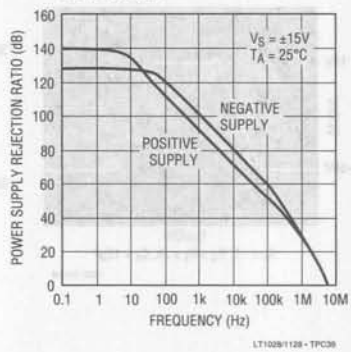
Common-Mode Limit Over Temperature



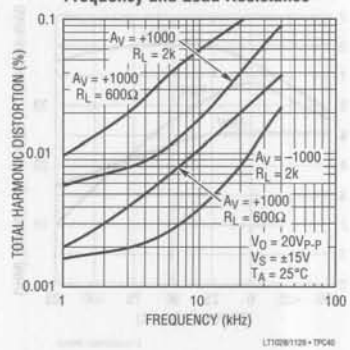
Common-Mode Rejection Ratio vs Frequency



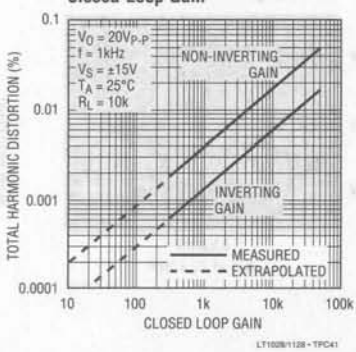
Power Supply Rejection Ratio vs Frequency



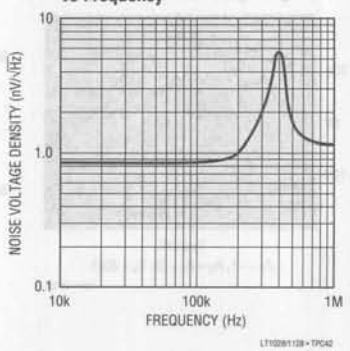
LT1028
Total Harmonic Distortion vs Frequency and Load Resistance



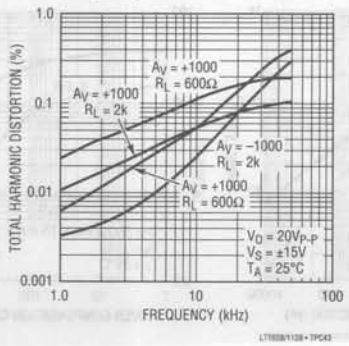
LT1028
Total Harmonic Distortion vs Closed-Loop Gain



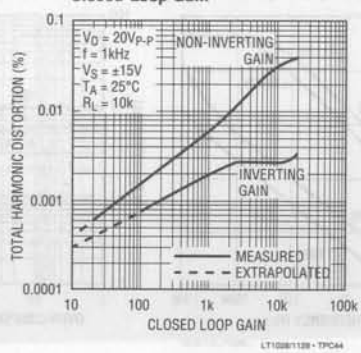
High Frequency Voltage Noise vs Frequency



LT1128
Total Harmonic Distortion vs Frequency and Load Resistance



LT1128
Total Harmonic Distortion vs Closed-Loop Gain



APPLICATIONS INFORMATION–NOISE

Voltage Noise vs Current Noise

The LT1028/LT1128's less than $1nV/\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028/LT1128's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (I_n) and resistor noise (r_n).

Total Noise vs Source Resistance

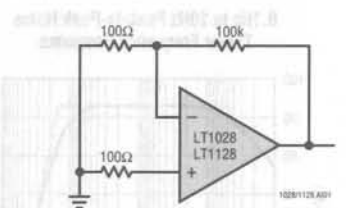
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (I_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs, and

$$r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}} \quad \text{in } nV/\sqrt{Hz} \text{ at } 25°C$$

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.



$R_{eq} = 100\Omega + 100\Omega \parallel 100k \approx 200\Omega$

$r_n = 0.13\sqrt{200} = 1.84nV/\sqrt{Hz}$

$e_n = 0.85nV/\sqrt{Hz}$

$I_n = 1.0pA/\sqrt{Hz}$

$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04nV/\sqrt{Hz}$

Output noise = $1000\ e_t = 2.04\mu V/\sqrt{Hz}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term, as in the example above, and the LT1028/LT1128's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20k, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1k because the resistor noise contribution is less. When $R_S > 1k$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028/LT1128 are the optimum amplifiers for noise performance, provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise, as the source resistance is increased beyond the LT1028/LT1128's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE(Ω) (Note 1)	BEST OP AMP AT LOW FREQ(10Hz)	BEST OP AMP WIDEBAND(1kHz)
0 to 400	LT1028/LT1128	LT1028/LT1128
400 to 4k	LT1007/1037	LT1028/LT1128
4k to 40k	LT1001	LT1007/1037
40k to 500k	LT1012	LT1001
500k to 5M	LT1012 or LT1055	LT1012
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., R_S = 1k means: 1k at each input, or 1k at one input and zero at the other.

APPLICATIONS INFORMATION–NOISE

Noise Testing – Voltage Noise

The LT1028/LT1128's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed-loop gain of 31 with a 60Ω source resistor and a 1.8k feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0nV/\sqrt{Hz}$. An LT1028/LT1128 with $0.85nV/\sqrt{Hz}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31nV/\sqrt{Hz}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8% to 10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028/LT1128 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028/LT1128 requires special test precautions:

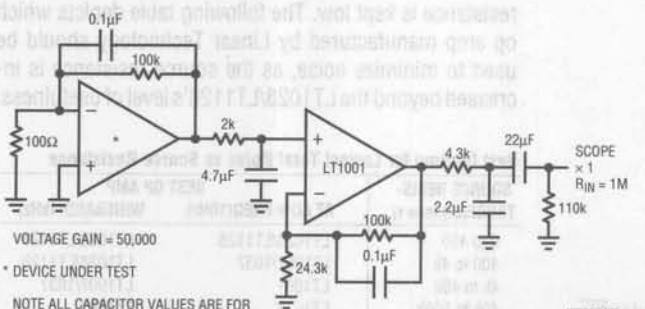
(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10μV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air current to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

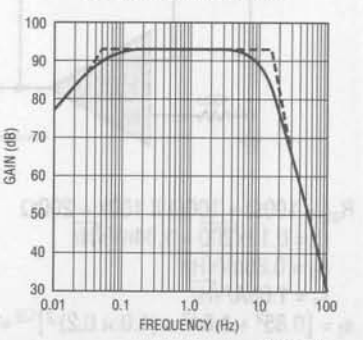
(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response

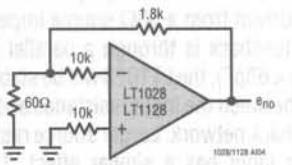


APPLICATIONS INFORMATION–NOISE

Noise Testing – Current Noise

Current noise density (I_n) is defined by the following formula, and can be measured in the circuit shown:

$$I_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$



If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

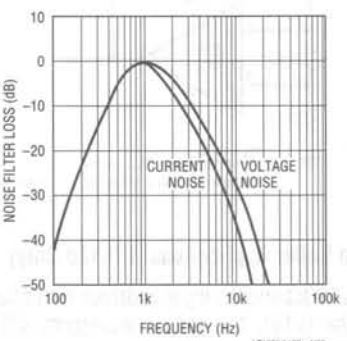
100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028/LT1128 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter



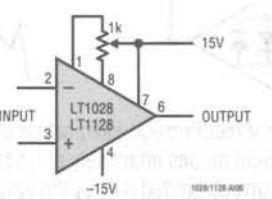
APPLICATIONS INFORMATION

General

The LT1028/LT1128 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028/LT1128 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028/LT1128 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other



than zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.

The adjustment range with a 1k pot is approximately ±1.1mV.

Offset Voltage and Drift

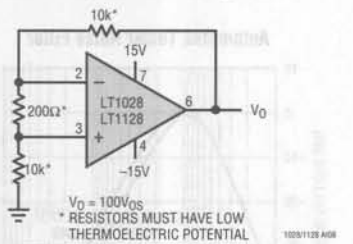
Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input

APPLICATIONS INFORMATION

terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

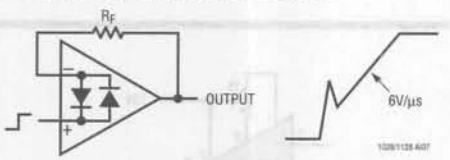
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028/LT1128.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



Unity-Gain Buffer Applications (LT1128 Only)

When $R_F \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.

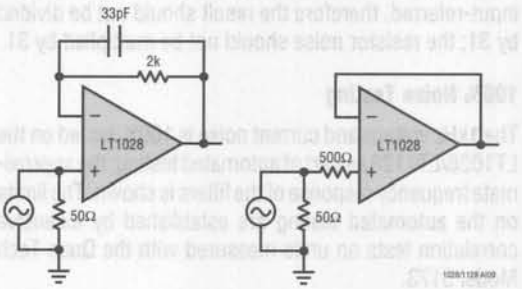


During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

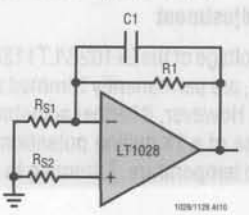
As with all operational amplifiers when $R_F > 2k$, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_F will eliminate this problem.

Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed-loop gains greater than +2 or –1 because phase margin is about 50° at an open-loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the noninverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_F < 68pF$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the noninverting input has a similar effect. The following voltage follower configurations are stable:



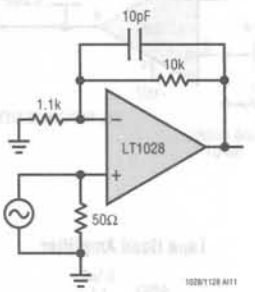
Another configuration which requires unity-gain stability is shown below. When C_F is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of R_{S2} will be minimal. When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} represents a heavy load on the output through the C_F short. When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1}. For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to R_{S2} is 40%.



APPLICATIONS INFORMATION

If C_F is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at gain of 10 (20dB). The following configuration has a high (≈70%) overshoot without the 10pF capacitor because of additional phase shift caused by the feedback resistor – input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.



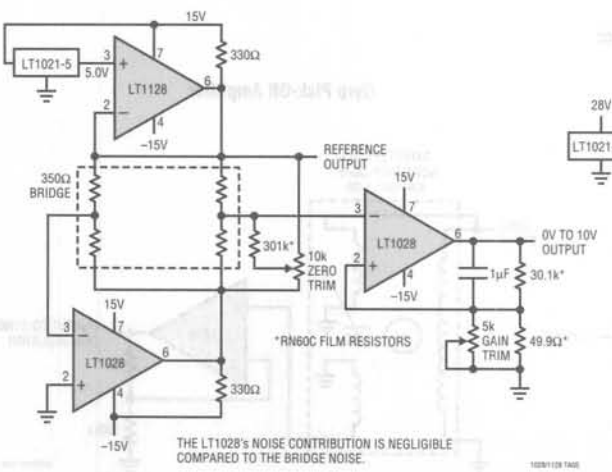
Over-Compensation

The LT1028/LT1128 are equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

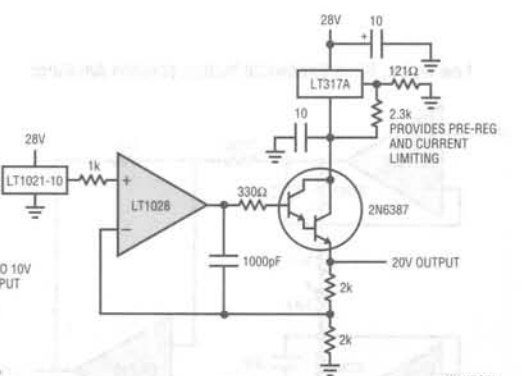
2

TYPICAL APPLICATION

Strain Gauge Signal Conditioner with Bridge Excitation

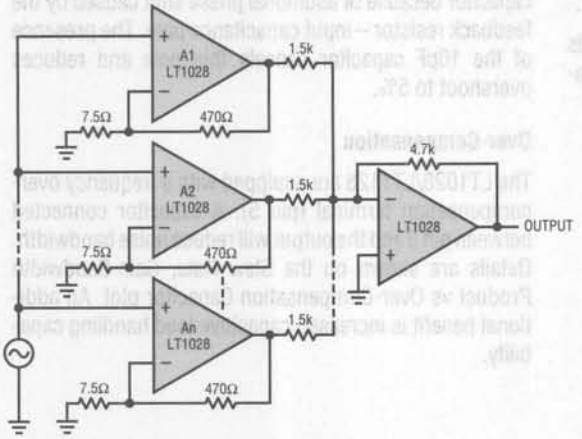


Low Noise Voltage Regulator



TYPICAL APPLICATION

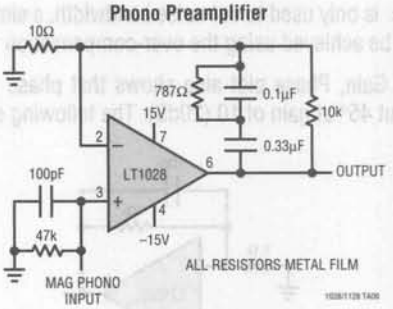
Paralleling Amplifiers to Reduce Voltage Noise



1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = 0.9nV/√Hz.
2. GAIN WITH n LT1028s IN PARALLEL = n × 200.
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 0.9nV/\sqrt{Hz}$.
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{0.9}{\sqrt{n}}$ nV/√Hz.
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES.
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz = $\frac{2\mu V}{\sqrt{5}} = 0.9\mu V$.

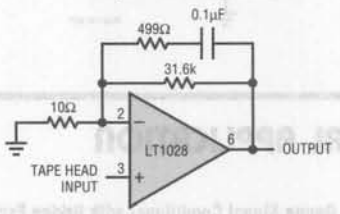
1028/1128 TA03

Phono Preamplifier



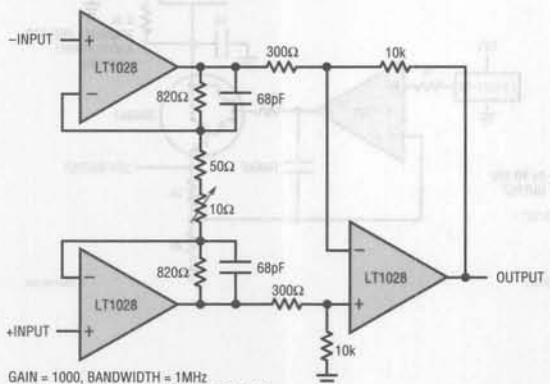
1028/1128 TA06

Tape Head Amplifier



1028/1128 TA07

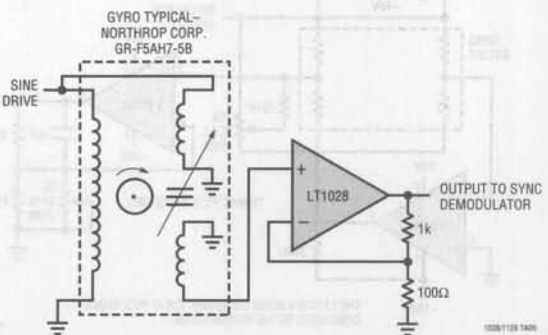
Low Noise, Wide Bandwidth Instrumentation Amplifier



GAIN = 1000, BANDWIDTH = 1MHz
INPUT REFERRED NOISE = 1.5nV/√Hz AT 1kHz
WIDEBAND NOISE –DC to 1MHz = $3\mu V_{RMS}$
IF BW LIMITED TO DC TO 100kHz = $0.55\mu V_{RMS}$

1028/1128 TA08

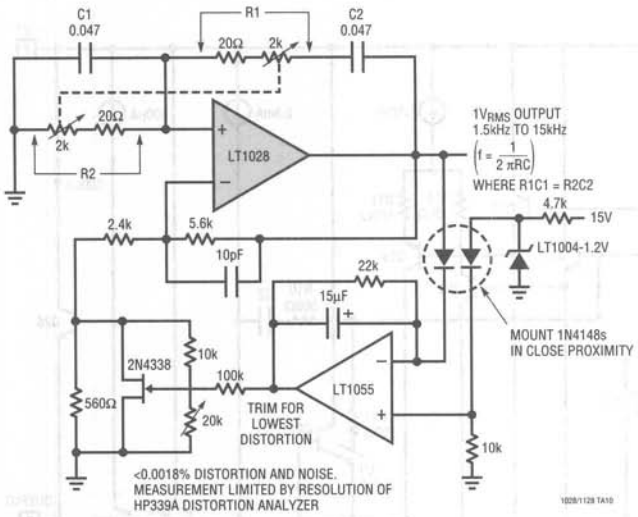
Gyro Pick-Off Amplifier



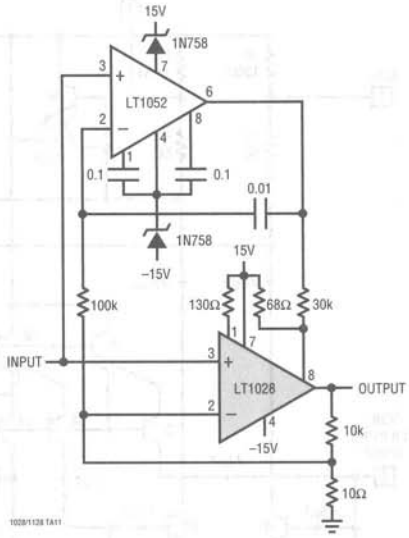
1028/1128 TA09

TYPICAL APPLICATION

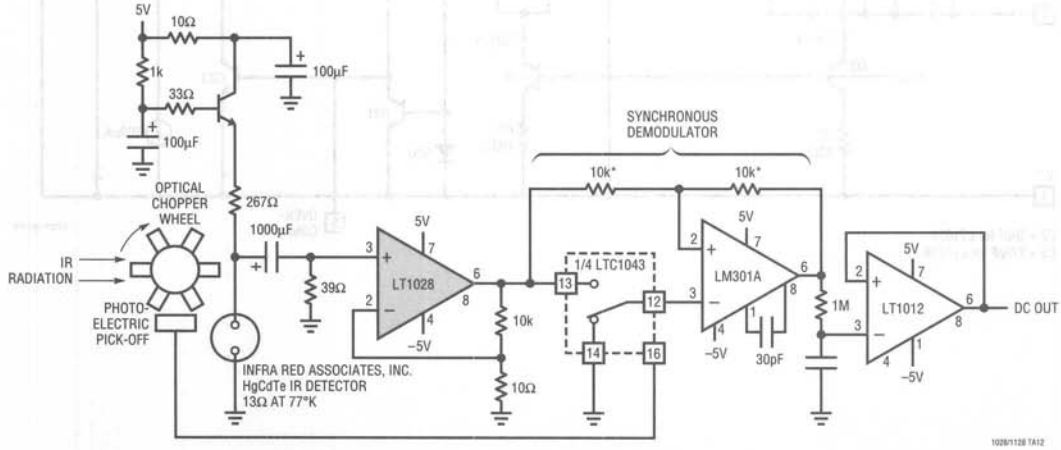
Super Low Distortion Variable Sine Wave Oscillator



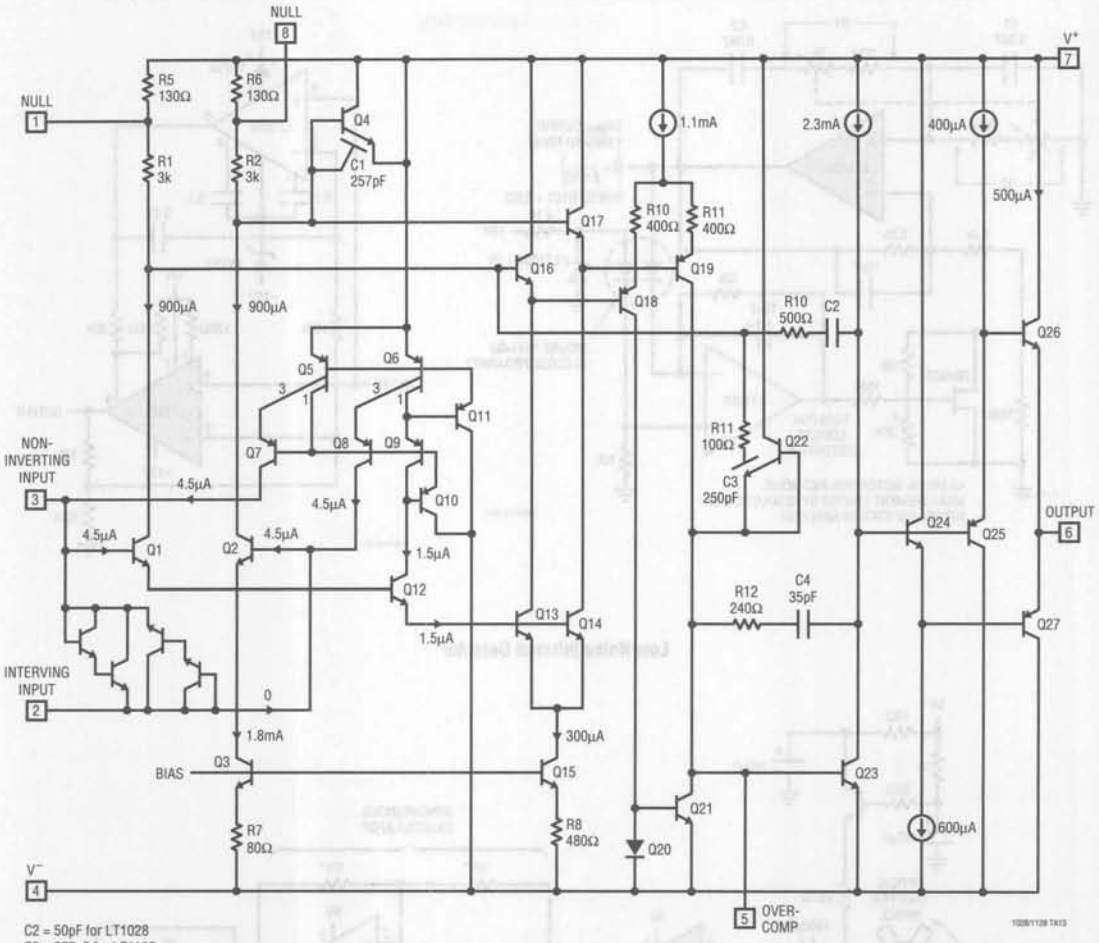
Chopper-Stabilized Amplifier



Low Noise Infrared Detector



SCHEMATIC DIAGRAM



Dual/Quad Low Power Precision, Picoamp Input Op Amps

FEATURES

- S8 Package – Standard Pinout
- Offset Voltage – Prime Grade: 60μV Max
- Offset Voltage – Low Cost Grade (Including Surface Mount Dual/Quad): 75μV Max
- Offset Voltage Drift: 0.5μV/°C Max
- Input Bias Current: 250pA Max
- 0.1Hz to 10Hz Noise: 0.3μV_{P-P}, 2.2pA_{P-P}
- Supply Current per Amplifier: 400μA Max
- CMRR: 120dB Min
- Voltage Gain: 1 Million Min
- Guaranteed Specs with ±1.0V Supplies
- Guaranteed Matching Specifications
- LT1114 in Narrow Surface Mount Package

APPLICATIONS

- Picoampere/Microvolt Instrumentation
- Two and Three Op Amp Instrumentation Amplifers
- Thermocouple and Bridge Amplifiers
- Low Frequency Active Filters
- Photo Current Amplifiers
- Battery-Powered Systems

DESCRIPTION

The LT1112 dual and LT1114 quad op amps achieve a new standard in combining low cost and outstanding precision specifications.

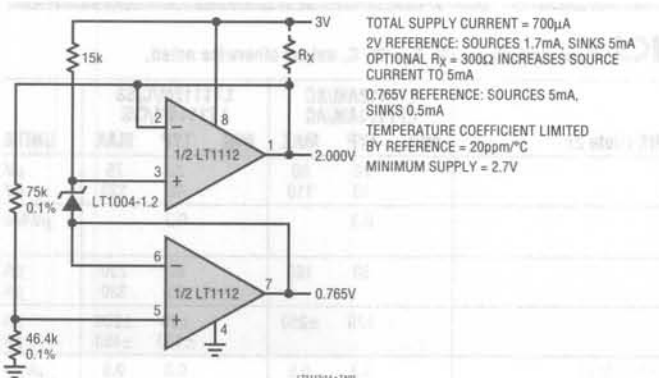
The performance of the selected prime grades matches or exceeds competitive devices. In the design of the LT1112/LT1114 however, particular emphasis has been placed on optimizing performance in the low cost plastic and SO packages. For example, the 75μV maximum offset voltage in these low cost packages is the lowest on any dual or quad non-chopper op amp.

The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as two and three op amp instrumentation amplifiers.

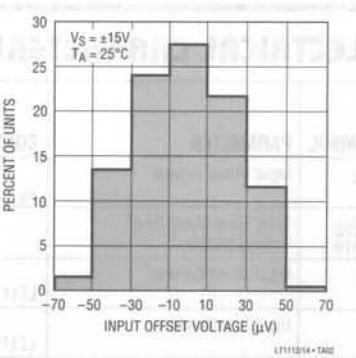
Another set of specifications is furnished at ±1V supplies. This, combined with the low 320μA supply current per amplifier, allows the LT1112/LT1114 to be powered by two nearly discharged AA cells.

Protected by U.S. Patents 4,575,685; 4,775,884 and 4,837,496

Dual Output, Buffered Reference (On Single 3V Supply)



Distribution of Input Offset Voltage (In All Packages)

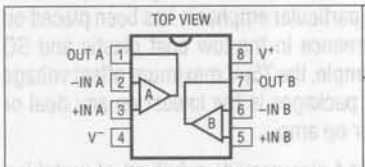


ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Equal to Supply Voltage) ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

Operating Temperature Range
LT1112AM/LT1112M
LT1114AM/LT1114M ..... −55°C to 125°C
LT1112AC/LT1112C/LT1112S8
LT1114AC/LT1114C/LT1114S ..... −40°C to 85°C

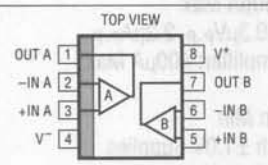
PACKAGE/ORDER INFORMATION



J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP
T_{JMAX} = 160°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 140°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER

LT1112AMJ8
LT1112MJ8
LT1112ACN8
LT1112CN8



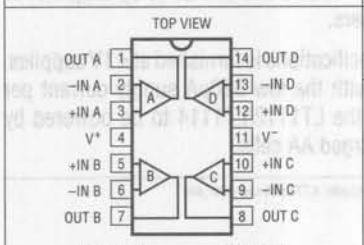
S8 PACKAGE 8-LEAD PLASTIC SO
T_{JMAX} = 140°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1112S8

S8 PART MARKING

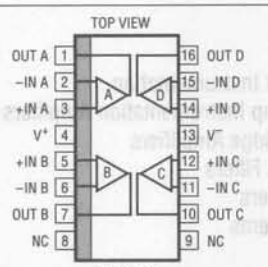
1112



J PACKAGE 14-LEAD CERAMIC DIP
N PACKAGE 14-LEAD PLASTIC DIP
T_{JMAX} = 160°C, θ_{JA} = 80°C/W (J)
T_{JMAX} = 140°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER

LT1114AMJ
LT1114MJ
LT1114ACN
LT1114CN



S PACKAGE 16-LEAD PLASTIC SO (NARROW)
T_{JMAX} = 140°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1114S

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1112AM/AC LT1114AM/AC MIN	TYP	MAX	LT1112M/C/S8 LT1114M/C/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			20	60		25	75	µV
		V_S = ±1.0V		40	110		45	130	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		µV/Mo
I_{OS}	Input Offset Current			50	180		60	230	pA
		LT1114S					75	330	pA
I_B	Input Bias Current			±70	±250		±80	±280	pA
		LT1114S					±100	±450	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 9)		0.3	0.9		0.3	0.9	μV_{P-P}

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1112AM/AC LT1114AM/AC MIN	TYP	MAX	LT1112M/C/S8 LT1114M/C/S MIN	TYP	MAX	UNITS
	Input Noise Voltage Density	$f_O = 10Hz$ (Note 9) $f_O = 1000Hz$ (Note 9)		16 14	28 18		16 14	28 18	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz		2.2			2.2		pA_{P-P}
	Input Noise Current Density	$f_O = 10Hz$ $f_O = 1000Hz$		0.030 0.008			0.030 0.008		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range		±13.5	±14.3		±13.5	±14.3		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm13.5V$	120	136		115	136		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.0V$ to $\pm20V$	116	126		114	126		dB
	Minimum Supply Voltage	(Note 4)	±1.0			±1.0			V
R_{IN}	Input Resistance Differential Mode Common Mode	(Note 3)	20	50 800		15	40 700		MΩ GΩ
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k\Omega$ $V_O = \pm10V$, $R_L = 2k\Omega$	1000 800	5000 1500		800 600	5000 1300		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±13.0 ±11.0	±14.0 ±12.4		±13.0 ±11.0	±14.0 ±12.4		V V
SR	Slew Rate		0.16	0.30		0.16	0.30		V/µs
GBW	Gain-Bandwidth Product	$f_O = 10kHz$	450	750		450	750		kHz
I_S	Supply Current per Amplifier 	 $V_S = \pm1.0V$		350 320	400 370		350 320	450 420	µA µA
	Channel Separation	$f_O = 10Hz$		150			150		dB
ΔV_{OS}	Offset Voltage Match	(Note 5)		35	100		40	130	µV
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6) 	 LT1114S		100	450		100 120	500 680	pA pA
ΔCMRR	Common-Mode Rejection Match	(Notes 5, 7)	117	136		113	136		dB
ΔPSRR	Power Supply Rejection Match	(Notes 5, 7)	114	130		112	130		dB

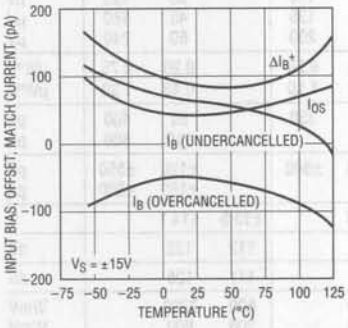
ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112AMJ8 LT1114AMJ MIN	TYP	MAX	LT1112MJ8 LT1114MJ MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage 	 $V_S = \pm1.2V$	● ●		35 60	120 220		45 70	150 260	µV µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 8)	●		0.15	0.5		0.20	0.75	µV/°C
I_{OS}	Input Offset Current		●		80	400		100	500	pA
I_B	Input Bias Current		●		±150	±600		±170	±700	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm13.5V$	●	116	130		111	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.2V$ to $\pm20V$	●	112	124		110	124		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k\Omega$ $V_O = \pm10V$, $R_L = 2k\Omega$	● ●	500 200	2500 600		400 170	2500 500		V/mV V/mV

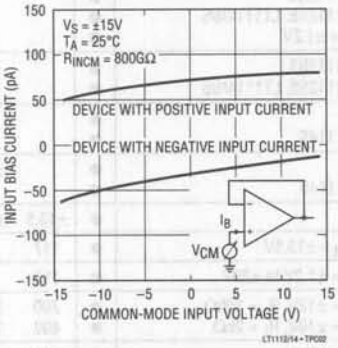
2

TYPICAL PERFORMANCE CHARACTERISTICS

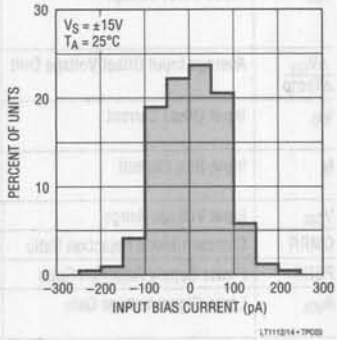
Input Bias and Offset Current, Noninverting Bias Current Match vs Temperature



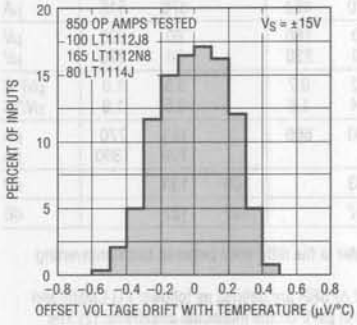
Input Bias Current Over Common-Mode Range



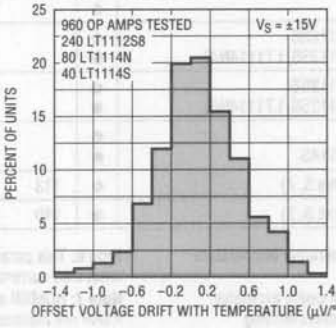
Distribution of Input Bias Current (In All Packages Except LT1114S)



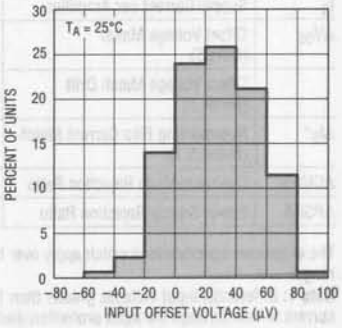
Drift with Temperature LT1112N8/J8, LT1114J



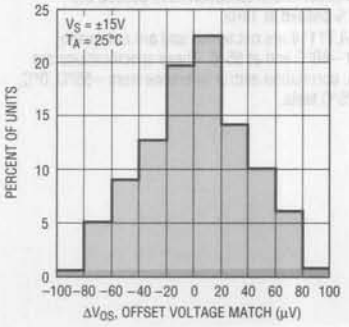
Drift with Temperature LT1112S8, LT1114N/S



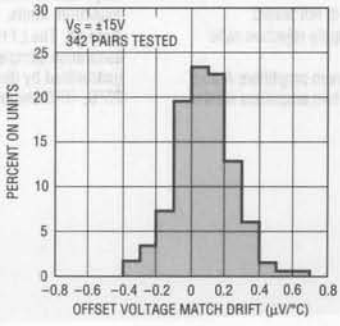
Distribution of Offset Voltage at V_S = ±1.0V (In All Packages)



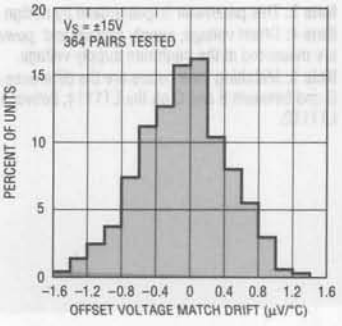
Distribution of Offset Voltage Match



Distribution of Offset Voltage Match Drift (LT1112J8, LT1112N8, LT1114J Packages)



Distribution of Offset Voltage Match Drift (LT1112S8, LT1114N, LT1114S Packages)



ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-40°C \le T_A \le 85°C$, (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112ACN8 LT1114ACN MIN	LT1112ACN8 LT1114ACN TYP	LT1112ACN8 LT1114ACN MAX	LT1112N8/S8 LT1114CN/S MIN	LT1112N8/S8 LT1114CN/S TYP	LT1112N8/S8 LT1114CN/S MAX	UNITS
V_{OS}	Input Offset Voltage	LT1112N8	●		30	110		35	135	µV
		LT1112S8, LT1114N/S	●		40	135		45	160	µV
		$V_S = \pm 1.2V$	●		55	200		60	240	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	LT1112N8	●		0.15	0.50		0.20	0.75	µV/°C
		LT1112S8, LT1114N/S	●		0.30	1.10		0.40	1.30	µV/°C
I_{OS}	Input Offset Current		●		70	330		85	400	pA
		LT1114S	●					110	600	pA
I_B	Input Bias Current		●		±110	±500		±120	±550	pA
		LT1114S	●					±150	±800	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	117	132		112	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	●	113	125		111	125		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k\Omega$	●	700	3300		600	3300		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$	●	400	1100		300	900		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.85		±13.0	±13.85		V
SR	Slew Rate		●	0.13	0.24		0.13	0.24		V/µs
I_S	Supply Current per Amplifier		●		370	450		370	510	µA
ΔV_{OS}	Offset Voltage Match (Note 5)	LT1112N8	●		50	180		60	225	µV
		LT1112S8, LT1114N/S	●		60	230		70	270	µV
	Offset Voltage Match Drift (Notes 5)	LT1112N8	●		0.2	0.7		0.3	1.0	µV/°C
		LT1112S8, LT1114N/S	●		0.4	1.6		0.5	1.9	µV/°C
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6)		●		140	660		155	770	pA
		LT1114S	●					190	1300	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	113	133		109	133		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	110	127		107	127		dB

The ● denotes specifications which apply over the operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1114s (or 100 LT1112s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Offset voltage, supply current and power supply rejection ratio are measured at the minimum supply voltage.

Note 5: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1114; between the two amplifiers on the LT1112.

Note 6: This parameter is the difference between two noninverting input bias currents.

Note 7: ΔCMRR and ΔPSRR are defined as follows: (1) CMRR and PSRR are measured in µV/V on the individual amplifiers. (2) The difference is calculated between the matching sides in µV/V. (3) The result is converted to dB.

Note 8: This parameter is not 100% tested.

Note 9: These parameters are not tested. More than 99% of the op amps tested during product characterization have passed the maximum limits. 100% passed at 1kHz.

Note 10: The LT1112/LT1114 are not tested and are not quality assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

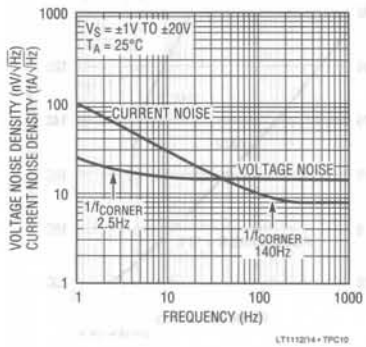
SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112AMJ8 LT1114AMJ MIN	TYP	MAX	LT1112MJ8 LT1114MJ MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.85		±13.0	±13.85		V
SR	Slew Rate		●	0.12	0.22		0.12	0.22		V/µs
I_S	Supply Current per Amplifier		●		380	460		380	530	µA
ΔV_{OS}	Offset Voltage Match	(Note 5)	●		55	200		70	240	µV
	Offset Voltage Match Drift	(Notes 5, 8)	●		0.2	0.7		0.3	1.0	µV/°C
ΔI_B^+	Noninverting Bias Current Match	(Notes 5, 6)	●		150	750		170	850	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	112	130		106	130		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	109	126		106	126		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

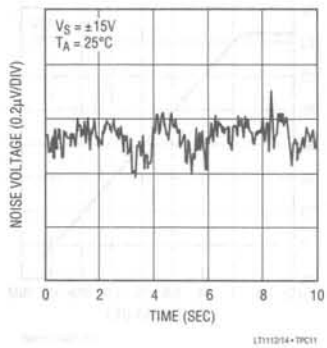
SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112N8/S8 LT1114CN/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1112N8	●		27	100		30	125	µV
		LT1112S8, LT1114N/S	●		35	125		45	150	µV
		$V_S = \pm 1.2V$	●		50	175		65	210	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift (Note 8)	LT1112N8	●		0.15	0.5		0.2	0.75	µV/°C
		LT1112S8, LT1114N/S	●		0.3	1.1		0.4	1.3	µV/°C
I_{OS}	Input Offset Current		●		60	220		70	290	pA
		LT1114S	●					90	420	pA
I_B	Input Bias Current		●		±80	±300		±90	±350	pA
		LT1114S	●					±115	±550	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.2		±13.5	±14.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	118	133		113	133		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	●	114	125		112	125		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k\Omega$	●	800	4000		650	4000		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$	●	500	1300		400	1000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.9		±13.0	±13.9		V
SR	Slew Rate		●	0.14	0.27		0.14	0.27		V/µs
I_S	Supply Current per Amplifier		●		370	440		370	500	µA
ΔV_{OS}	Offset Voltage Match (Note 5)	LT1112N8	●		45	170		55	210	µV
		LT1112S8, LT1114N/S	●		55	220		70	270	µV
	Offset Voltage Match Drift (Notes 5, 8)	LT1112N8	●		0.2	0.7		0.3	1.0	µV/°C
		LT1112S8, LT1114N/S	●		0.4	1.6		0.5	1.9	µV/°C
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6)		●		120	530		135	620	pA
		LT1114S	●					160	880	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	114	134		109	134		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	110	128		108	128		dB

TYPICAL PERFORMANCE CHARACTERISTICS

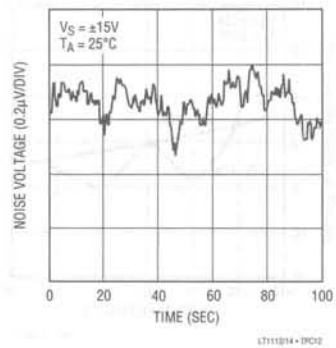
Noise Spectrum



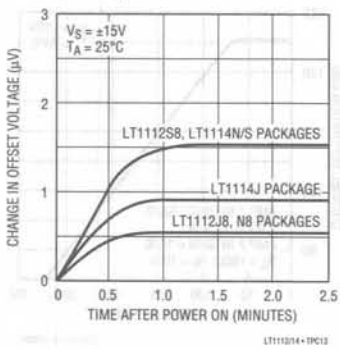
0.1Hz to 10Hz Noise



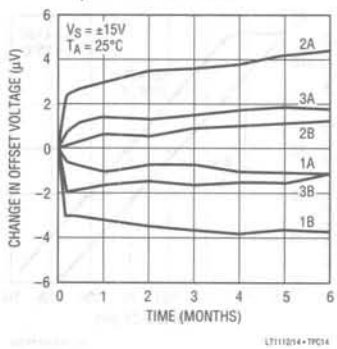
0.01Hz to 1Hz Noise



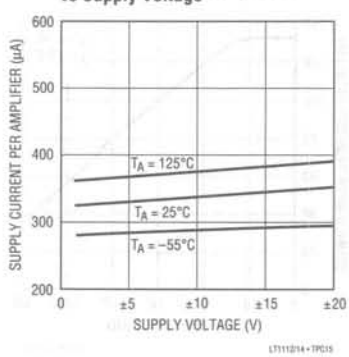
Warm-Up Drift



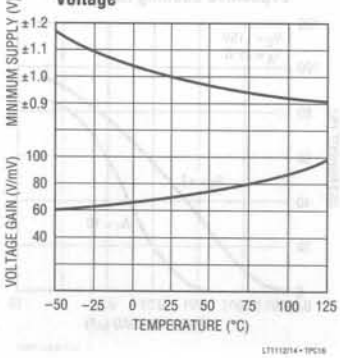
Long Term Stability of Three Representative Units



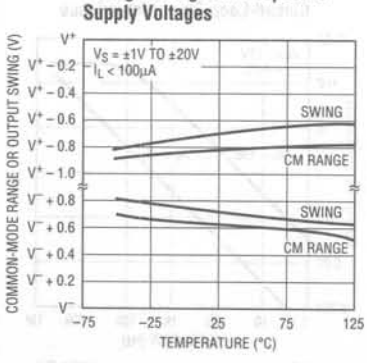
Supply Current per Amplifier vs Supply Voltage



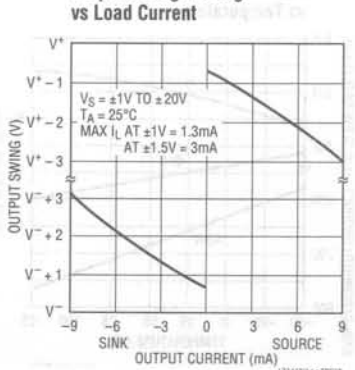
Minimum Supply Voltage vs Temp
Voltage Gain at Minimum Supply Voltage



Common-Mode Range and Voltage Swing with Respect to Supply Voltages



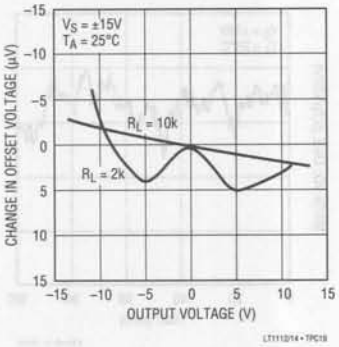
Output Voltage Swing vs Load Current



2

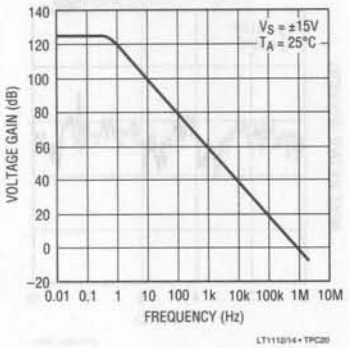
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain



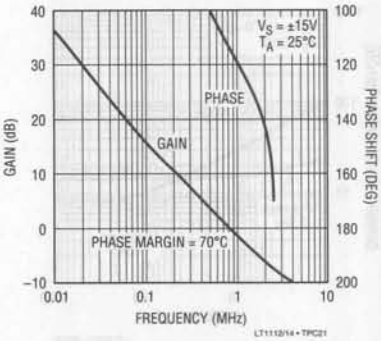
LT1112/14 • TPC19

Voltage Gain vs Frequency



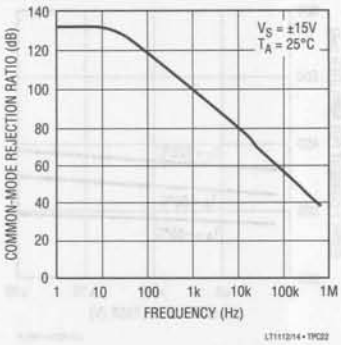
LT1112/14 • TPC20

Gain, Phase Shift vs Frequency



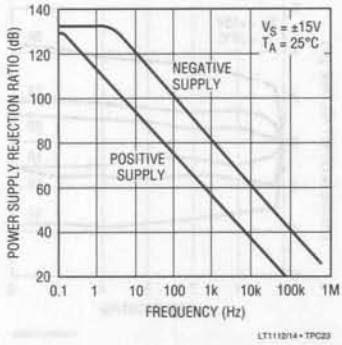
LT1112/14 • TPC21

Common-Mode Rejection vs Frequency



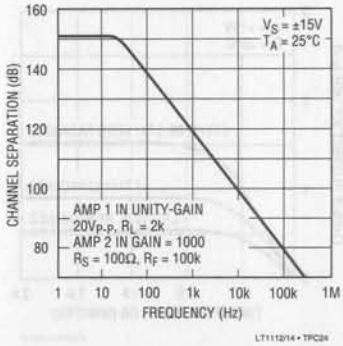
LT1112/14 • TPC22

Power Supply Rejection vs Frequency



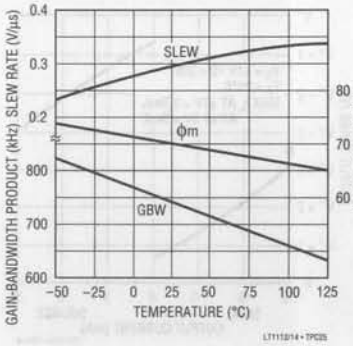
LT1112/14 • TPC23

Channel Separation vs Frequency



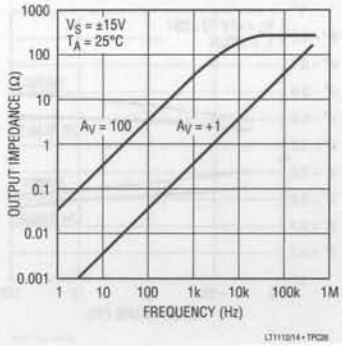
LT1112/14 • TPC24

Slew Rate, Gain-Bandwidth Product and Phase Margin vs Temperature



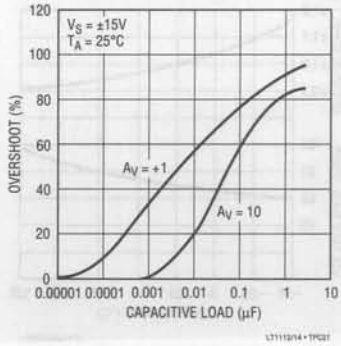
LT1112/14 • TPC25

Closed-Loop Output Impedance



LT1112/14 • TPC26

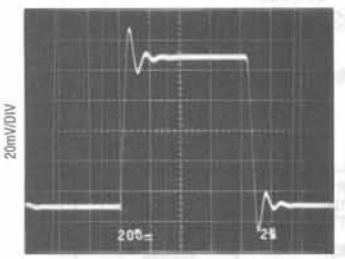
Capacitive Loading Handling



LT1112/14 • TPC27

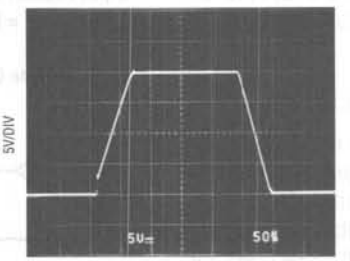
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response



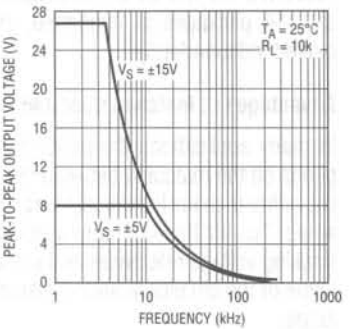
A_V = +1
C_L = 500pF
V_S = ±15V

Large-Signal Transient Response



A_V = +1
R_F = 10k
C_F = 100pF
V_S = ±15V

Undistorted Output Voltage vs Frequency



APPLICATIONS INFORMATION

The LT1112 dual and LT1114 quad in the plastic and ceramic DIP packages are pin compatible to and directly replace such precision op amps as the OP-200, OP-297, AD706 duals and OP-400, OP-497, AD704 quads with improved price/performance.

The LT1112 in the S8 surface mount package has the standard pin configuration, i.e., the same configuration as the plastic and ceramic DIP packages.

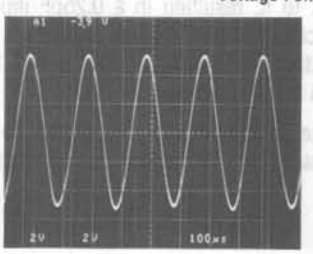
The LT1114 quad is offered in the narrow 16-pin surface mount package. All competitors are in the wide 16-pin package which occupies 1.8 times the area of the narrow package. The wide package is also 1.8 times thicker than the narrow package.

The inputs of the LT1112/1114 are protected with back-to-back diodes. In the voltage follower configuration, when the input is driven by a fast large-signal pulse (>1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection, will flow through the diodes.

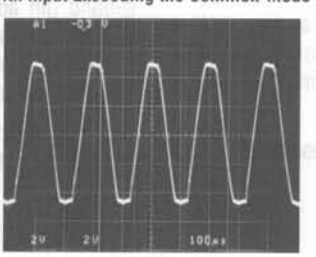
The use of a feedback resistor is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

The input voltage of the LT1112/1114 should never exceed the supply voltages by more than a diode drop. However, the example below shows that as the input voltage exceeds the common-mode range, the LT1112's output clips cleanly, without any glitches or phase reversal. The OP-297 exhibits phase reversal. The photos also illustrate that both the input and output ranges of the LT1112 are within

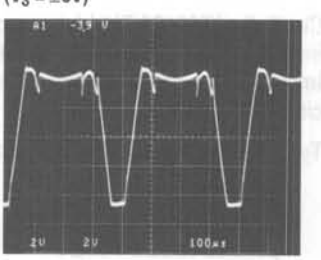
Voltage Follower with Input Exceeding the Common-Mode Range (V_S = ±5V)



INPUT: ±5.2V Sine Wave



LT1112 Output



OP-297 Output

APPLICATIONS INFORMATION

800mV of the supplies. The effect of input and output overdrive on the other amplifiers in the LT1112 or LT1114 packages is negligible, as each amplifier is biased independently.

Advantages of Matched Dual and Quad Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1112. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

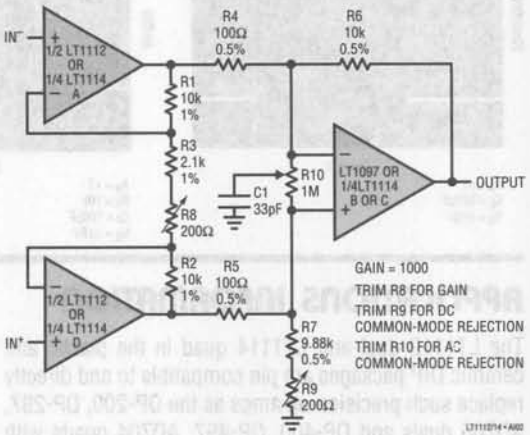
Assume $CMRR_A = +1\mu V/V$ or 120dB,
and $CMRR_B = +0.75\mu V/V$ or 122.5dB,
then $\Delta CMRR = 0.25\mu V/V$ or 132dB;
if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB,
then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly the LT1112/LT1114, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 35μV
Offset voltage drift = 0.3μV/°C
Input bias current = 80pA
Input offset current = 100pA
Input resistance = 800GΩ
Input noise = $0.42\mu V_{P-P}$

Three Op Amp Instrumentation Amplifier



When the instrumentation amplifier is used with high impedance sources, the LT1114 is recommended because its CMRR vs frequency performance is better than the LT1112's. For example, with two matched 1MΩ source resistors, CMRR at 100Hz is 100dB with the LT1114, 76dB with the LT1112.

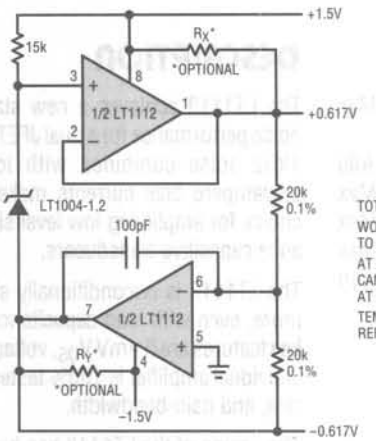
This difference is explained by the fact that capacitance between adjacent pins on an IC package is about 0.25pF (including package, socket and PC board trace capacitances).

On the dual op amp package, positive input A is next to the V^- pin (AC ground), while positive input B has no AC ground pin adjacent to it, resulting in a 0.25pF input capacitance mismatch. At 100Hz, 0.25pF represents a 6.4×10^9 input impedance mismatch, which is only 76dB higher than the 1MΩ source resistors.

On the quad package, all four inputs are adjacent to a power supply terminal–therefore, there is no mismatch.

TYPICAL APPLICATION

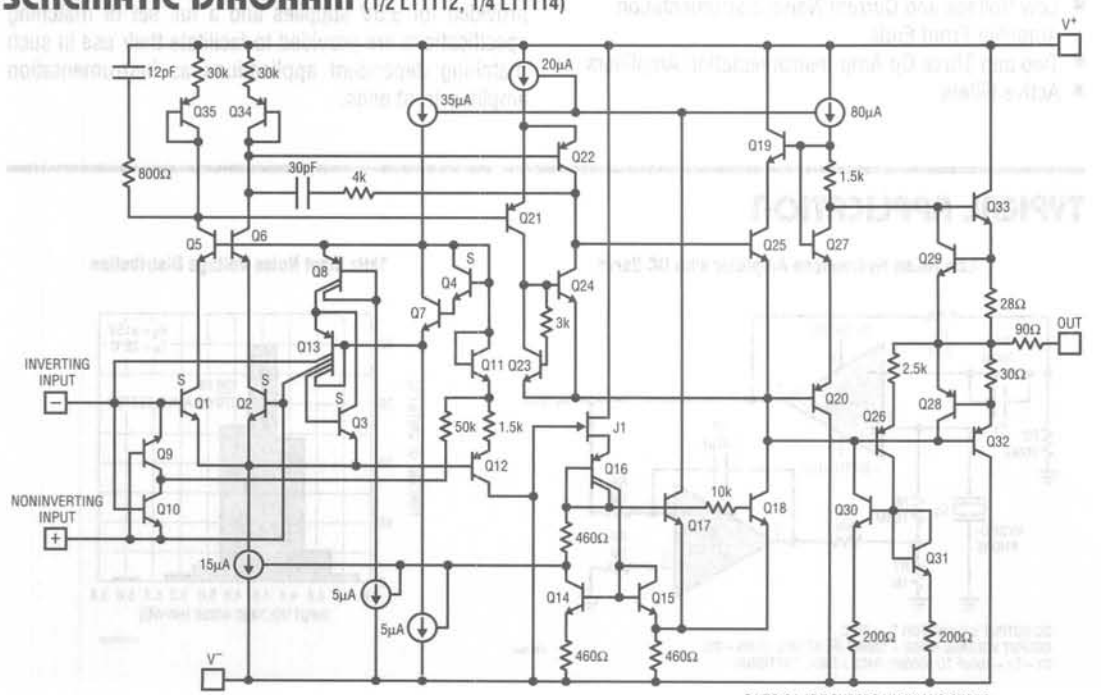
Dual Buffered ±0.617V Reference Powered by Two AA Batteries



TOTAL SUPPLY CURRENT = 700µA
WORKS WITH BATTERIES DISCHARGED TO ±1.3V
AT ±1.5V: MAXIMUM LOAD CURRENT = 800µA; CAN BE INCREASED WITH OPTIONAL R_X, R_Y;
AT $R_X = R_Y = 750\Omega$ LOAD CURRENT = 2mA
TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = 20ppm/°C

LT1112/14 • TA03

SCHEMATIC DIAGRAM (1/2 LT1112, 1/4 LT1114)



Q1 TO Q4 ARE SUPERGAIN TRANSISTORS

LT1112/14 • SD01

Dual Low Noise, Precision, JFET Input Op Amps

FEATURES

- 100% Tested Low Voltage Noise — 6nV/√Hz Max
- S8 Package Standard Pinout
- Voltage Gain — 1.2 Million Min
- Offset Voltage — 1.5mV Max
- Offset Voltage Drift — 15µV/°C Max
- Input Bias Current, Warmed Up — 450pA Max
- Gain-Bandwidth Product — 6.3MHz Typ
- Guaranteed Specifications with ±5V Supplies
- Guaranteed Matching Specifications

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

DESCRIPTION

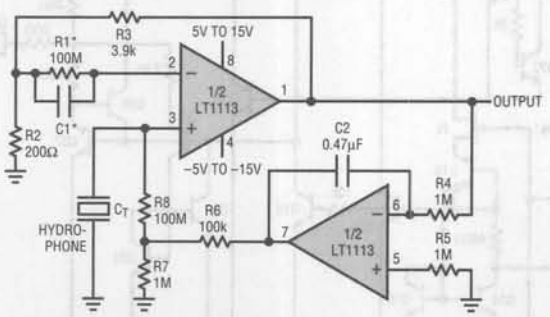
The LT1113 achieves a new standard of excellence in noise performance for a dual JFET op amp. The 4.5nV/√Hz 1kHz noise combined with low current noise and picoampere bias currents makes the LT1113 an ideal choice for amplifying low level signals from high impedance capacitive transducers.

The LT1113 is unconditionally stable for gains of 1 or more, even with load capacitances up to 1000pF. Other key features are 0.4mV V_{OS}, voltage gain of 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate, and gain-bandwidth.

The design of the LT1113 has been optimized to achieve true precision performance with an industry standard pinout in the S8 package. A set of specifications are provided for ±5V supplies and a full set of matching specifications are provided to facilitate their use in such matching dependent applications as instrumentation amplifier front ends.

TYPICAL APPLICATION

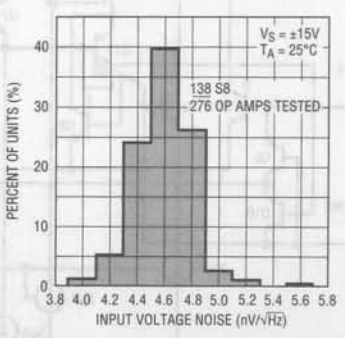
Low Noise Hydrophone Amplifier with DC Servo



DC OUTPUT ≤ 2.5mV FOR T_A < 70°C
OUTPUT VOLTAGE NOISE = 128nV/√Hz AT 1kHz (GAIN = 20)
C1 = C_T = 100pF TO 5000pF; R4C2 > R8C_T; *OPTIONAL

1113 TA01

1kHz Input Noise Voltage Distribution



1113 TA02

ABSOLUTE MAXIMUM RATINGS

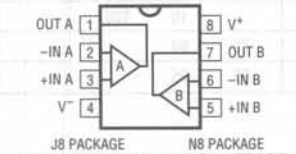
Supply Voltage
- –55°C to 105°C ..... ±20V
- 105°C to 125°C ..... ±16V

Differential Input Voltage ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Output Short Circuit Duration ..... 1 Minute

Operating Temperature Range
- LT1113AM/LT1113M ..... –55°C to 125°C
- LT1113AC/LT1113C ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

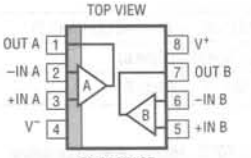
PACKAGE/ORDER INFORMATION



J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP

T_{JMAX} = 160°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 140°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LT1113AMJ8
LT1113MJ8
LT1113ACN8
LT1113CN8



S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 160°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1113CS8
S8 PART MARKING
1113

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1113AM/AC MIN	LT1113AM/AC TYP	LT1113AM/AC MAX	LT1113M/C MIN	LT1113M/C TYP	LT1113M/C MAX	UNITS
V_{OS}	Input Offset Voltage			0.40	1.5		0.50	1.8	mV
		V_S = ±5V		0.45	1.7		0.55	2.0	mV
I_{OS}	Input Offset Current	Warmed Up (Note 2)		30	100		35	150	pA
I_B	Input Bias Current	Warmed Up (Note 2)		300	450		320	480	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		17			17		$nV/\sqrt{Hz}$
		f_O = 1000Hz		4.5	6.0		4.5	6.0	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1000Hz (Note 3)		10			10		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance								
	Differential Mode			10^{11}			10^{11}		Ω
	Common Mode	V_{CM} = –10V to 8V		10^{11}			10^{11}		Ω
		V_{CM} = 8V to 11V		10^{10}			10^{10}		Ω
C_{IN}	Input Capacitance			14			14		pF
		V_S = ±5V		27			27		pF
V_{CM}	Input Voltage Range (Note 4)		13.0	13.5		13.0	13.5		V
			–10.5	–11.0		–10.5	–11.0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = –10V to 13V	85	98		82	95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	86	100		83	98		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k	1200	4800		1000	4500		V/mV
		V_O = ±10V, R_L = 1k	600	4000		500	3000		V/mV

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1113AM/AC MIN	LT1113AM/AC TYP	LT1113AM/AC MAX	LT1113M/C MIN	LT1113M/C TYP	LT1113M/C MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 10k$	±13.5	±13.8		±13.0	±13.8		V
		$R_L = 1k$	±12.0	±13.0		±11.5	±13.0		V
SR	Slew Rate	$R_L \geq 2k$ (Note 6)	2.5	4.2		2.5	4.2		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	4.5	6.3		4.5	6.3		MHz
	Channel Separation	$f_O = 10Hz$, $V_O = \pm 10V$, $R_L = 1k$		130			126		dB
I_S	Supply Current per Amplifier			5.3	6.25		5.3	6.50	mA
		$V_S = \pm 5V$		5.3	6.20		5.3	6.45	mA
ΔV_{OS}	Offset Voltage Match			0.8	2.5		0.8	3.3	mV
ΔI_B^+	Noninverting Bias Current Match	Warmed Up (Note 2)		10	80		10	120	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	81	94		78	94		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	82	95		80	95		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1113AC MIN	LT1113AC TYP	LT1113AC MAX	LT1113C MIN	LT1113C TYP	LT1113C MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.6	2.1		0.7	2.5	mV
		$V_S = \pm 5V$	●		0.7	2.3		0.8	2.7	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		7	15		8	20	µV/°C
I_{OS}	Input Offset Current		●		50	350		55	450	pA
I_B	Input Bias Current		●		600	1200		700	1600	pA
V_{CM}	Input Voltage Range		●	12.9	13.4		12.9	13.4		V
			●	−10.0	−10.8		−10.0	−10.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -10V$ to 12.9V	●	81	97		79	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	83	99		81	97		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	900	3600		800	3400		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	500	2600		400	2400		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±13.2	±13.5		±12.7	±13.5		V
		$R_L = 1k$	●	±11.7	±12.7		±11.3	±12.7		V
SR	Slew Rate	$R_L \geq 2k$ (Note 6)	●	2.3	4.0		1.9	4.0		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	3.6	5.1		3.6	5.1		MHz
I_S	Supply Current per Amplifier		●		5.3	6.35		5.3	6.55	mA
		$V_S = \pm 5V$	●		5.3	6.30		5.3	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		0.9	3.5		0.9	4.5	mV
ΔI_B^+	Noninverting Bias Current Match		●		30	300		35	400	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	●	76	93		74	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	79	93		77	93		dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 7)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1113AC MIN	LT1113AC TYP	LT1113AC MAX	LT1113C MIN	LT1113C TYP	LT1113C MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.7	2.4		0.8	2.8	mV
		$V_S = \pm 5V$	●		0.8	2.6		0.9	3.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		7	15		8	20	µV/°C
I_{OS}	Input Offset Current		●		80	700		90	1000	pA
I_B	Input Bias Current		●		1750	3000		1800	5000	pA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	−10.0	−10.5		−10.0	−10.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -10V$ to 12.6V	●	80	96		78	93		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	81	98		79	96		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	850	3300		750	3000		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	400	2200		300	2000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±13.0	±12.5		±12.5	±12.5		V
		$R_L = 1k$	●	±11.5	±12.0		±11.0	±12.0		V
SR	Slew Rate	$R_L \ge 2k$	●	2.2	3.8		1.8	3.8		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	3.3	4.8		3.3	4.8		MHz
I_S	Supply Current per Amplifier		●		5.30	6.35		5.30	6.55	mA
		$V_S = \pm 5V$	●		5.25	6.30		5.25	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.0	4.4		1.0	5.1	mV
ΔI_B^+	Noninverting Bias Current Match		●		50	600		55	900	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	●	76	93		73	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	77	92		75	92		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1113AM MIN	LT1113AM TYP	LT1113AM MAX	LT1113M MIN	LT1113M TYP	LT1113M MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.8	2.7		0.9	3.3	mV
		$V_S = \pm 5V$	●		0.8	2.8		0.9	3.4	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		5	12		8	15	µV/°C
I_{OS}	Input Offset Current		●		0.8	15		1.0	25	nA
I_B	Input Bias Current		●		25	50		27	70	nA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	−10.0	−10.4		−10.0	−10.4		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -10V$ to 12.6V	●	79	95		77	92		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	80	97		78	95		dB

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ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1113AM MIN	LT1113AM TYP	LT1113AM MAX	LT1113M MIN	LT1113M TYP	LT1113M MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	800	2700		700	2500		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	400	1500		300	1000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±13.0	±12.5		±12.5	±12.5		V
		$R_L = 1k$	●	±11.5	±12.0		±11.0	±12.0		V
SR	Slew Rate	$R_L \ge 2k$ (Note 6)	●	2.1	3.6		1.8	3.6		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	2.5	3.8		2.5	3.8		MHz
I_S	Supply Current Per Amplifier		●		5.30	6.35		5.30	6.55	mA
		$V_S = \pm 5V$	●		5.25	6.30		5.25	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.0	5.0		1.0	5.5	mV
ΔI_B^+	Noninverting Bias Current Match		●		1.8	12		2.0	20	nA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	●	75	92		73	92		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	76	91		74	91		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1113s (200 op amps) typically 120 op amps will be better than the indicated specification.

Note 2: Warmed-up I_B and I_{OS} readings are extrapolated to a chip temperature of 50°C from 25°C measurements and 50°C characterization data.

Note 3: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 4: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade), to 2.8mV (C grade).

Note 5: This parameter is not 100% tested.

Note 6: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

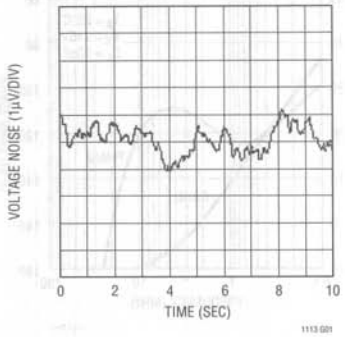
Note 7: The LT1113 is not tested and not quality assurance sampled at 85°C and at −40°C. These specifications are guaranteed by design, correlation and/or inference from −55°C, 0°C, 25°C, 70°C and/or 125°C tests.

Note 8: ΔCMRR and ΔPSRR are defined as follows:
(1) CMRR and PSRR are measured in µV/V on the individual amplifiers.
(2) The difference is calculated between the matching sides in µV/V.
(3) The result is converted to dB.

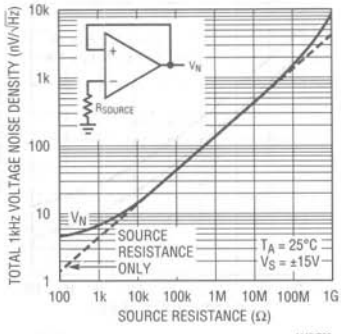
Note 9: The LT1113 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

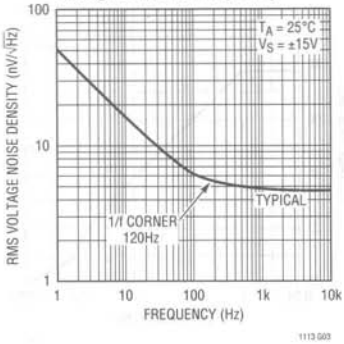
0.1Hz to 10Hz Voltage Noise



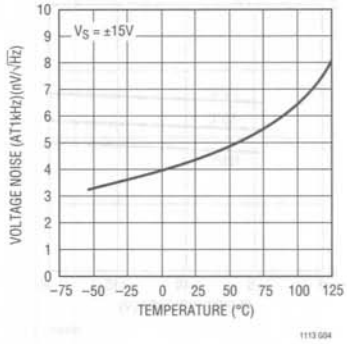
1kHz Output Voltage Noise Density vs Source Resistance



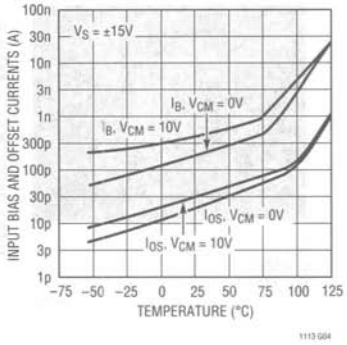
Voltage Noise vs Frequency



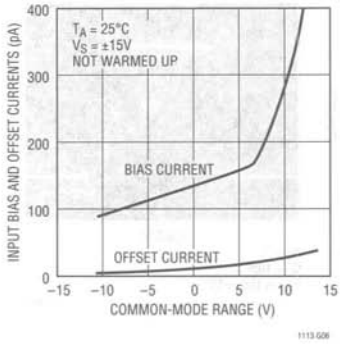
Voltage Noise vs Chip Temperature



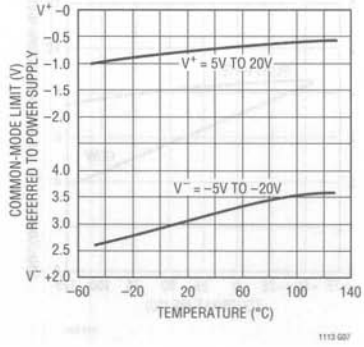
Input Bias and Offset Currents vs Chip Temperature



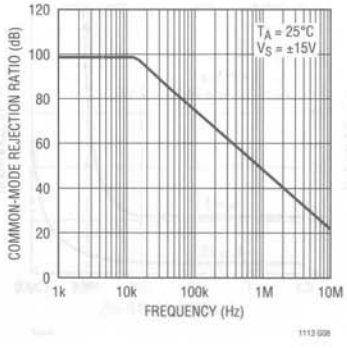
Input Bias and Offset Currents Over the Common-Mode Range



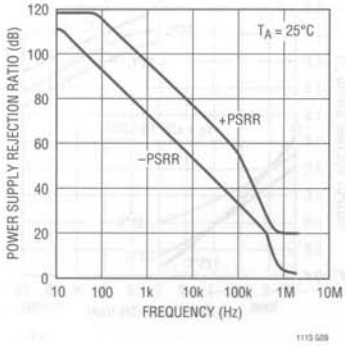
Common-Mode Limit vs Temperature



Common-Mode Rejection Ratio vs Frequency



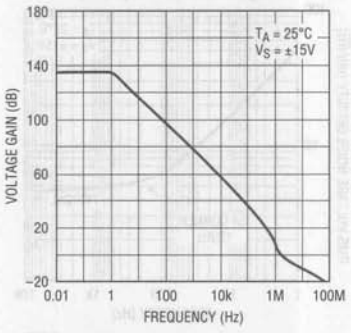
Power Supply Rejection Ratio vs Frequency



2

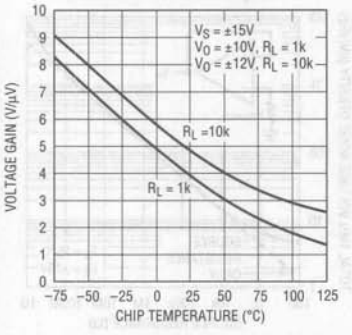
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain vs Frequency



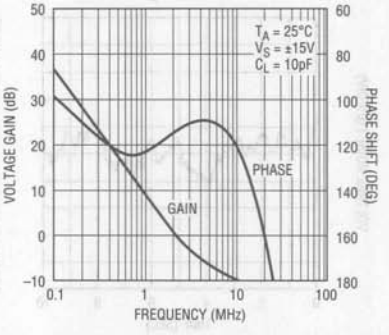
1113 G10

Voltage Gain vs Chip Temperature



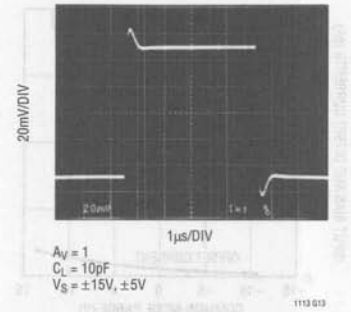
1113 G11

Gain and Phase Shift vs Frequency



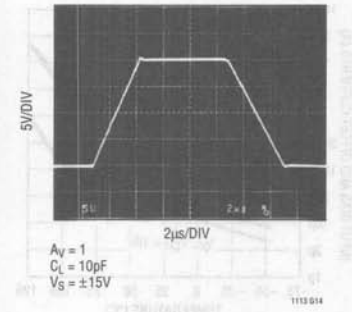
1113 G12

Small-Signal Transient Response



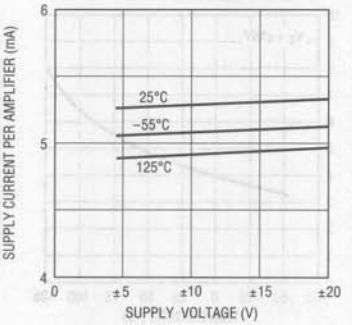
1113 G13

Large-Signal Transient Response



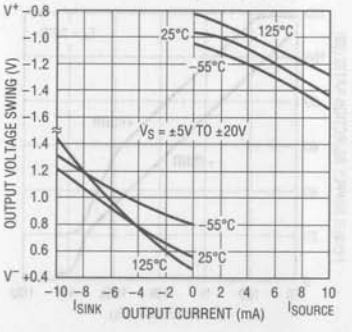
1113 G14

Supply Current vs Supply Voltage



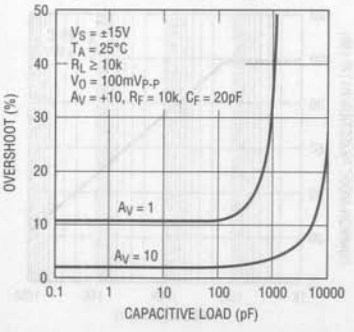
1113 G15

Output Voltage Swing vs Load Current



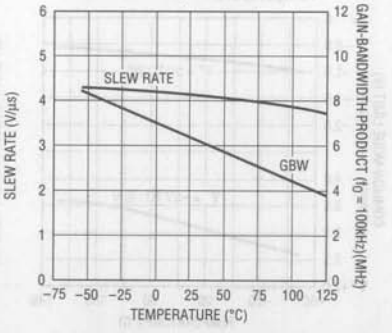
1113 G16

Capacitive Load Handling



1113 G17

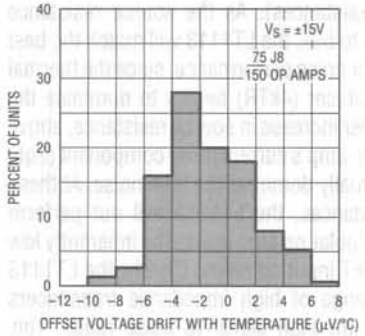
Slew Rate and Gain-Bandwidth Product vs Temperature



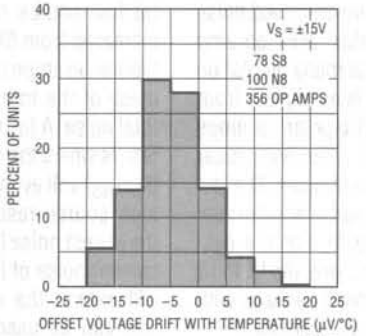
1113 G18

TYPICAL PERFORMANCE CHARACTERISTICS

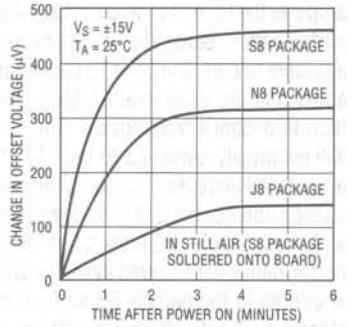
Distribution of Offset Voltage Drift with Temperature (J8)



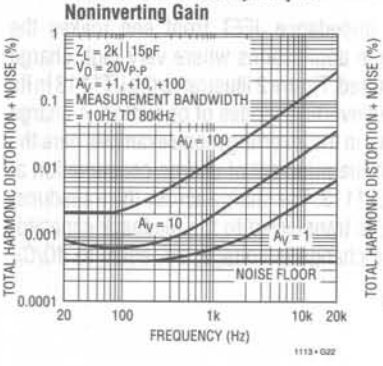
Distribution of Offset Voltage Drift with Temperature (N8, S8)



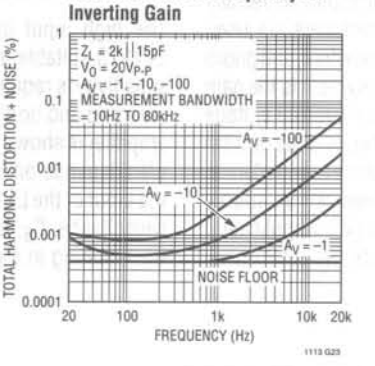
Warm-Up Drift



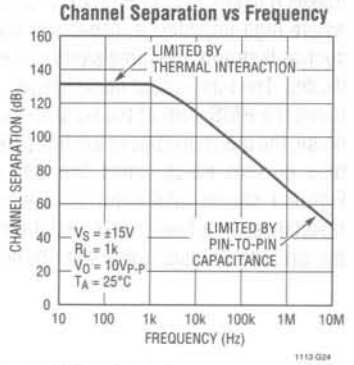
THD and Noise vs Frequency for Noninverting Gain



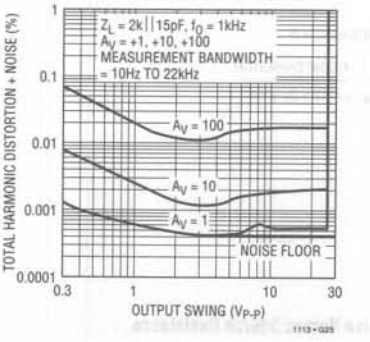
THD and Noise vs Frequency for Inverting Gain



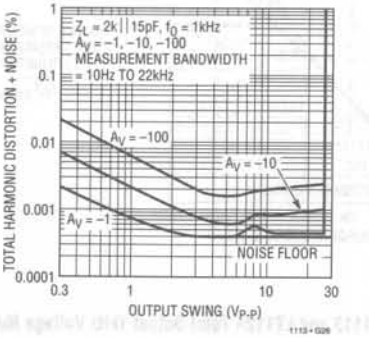
Channel Separation vs Frequency



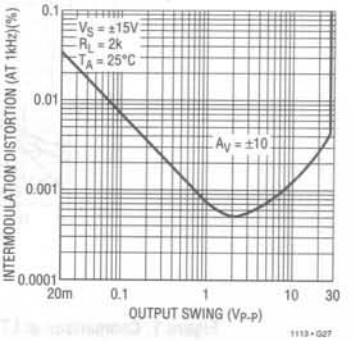
THD and Noise vs Output Amplitude for Noninverting Gain



THD and Noise vs Output Amplitude for Inverting Gain



CCIF IMD Test (Equal Amplitude Tones at 13kHz, 14kHz)*



* See LT1115 data sheet for definition of CCIF testing.

APPLICATIONS INFORMATION

The LT1113 dual in the plastic and ceramic DIP packages are pin compatible to and directly replace such JFET op amps as the OPA2111 and OPA2604 with improved noise performance. Being the lowest noise dual JFET op amp available to date, the LT1113 can replace many bipolar op amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps will eventually loose out to the LT1113 when transducer impedance increases due to higher current noise. The low voltage noise of the LT1113 allows it to surpass every dual and most single JFET op amps available. For the best performance versus area available anywhere, the LT1113 is offered in the narrow S8 surface mount package with standard pinout and no degradation in performance.

The low voltage and current noise offered by the LT1113 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers, and photo diodes. The total output noise in such a system is the gain times the RMS sum of the op amp input referred voltage noise, the thermal noise of the transducer, and the op amp bias current noise times the transducer impedance. Figure 1 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1113 will beat out any dual JFET op amp, only the lowest noise bipolar op amps have the edge (at low source resistances). As the source resistance increases from 5k to 50k, the LT1113 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_B R_{TRANS}$) will eventually dominate the total noise. At these high source resistances, the LT1113 will out perform the lowest noise bipolar op amp due to the inherently low current noise of FET input op amps. Clearly, the LT1113 will extend the range of high impedance transducers that can be used for high signal to noise ratios. This makes the LT1113 the best choice for high impedance, capacitive transducers.

The high input impedance JFET front end makes the LT1113 suitable in applications where very high charge sensitivity is required. Figure 2 illustrates the LT1113 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; here the gain depends on the principal of charge conservation at the input of the LT1113. The charge across the transducer capacitance, C_S, is transferred to the feedback capacitor C_F, resulting in a change in voltage, dV, equal to dQ/C_F.

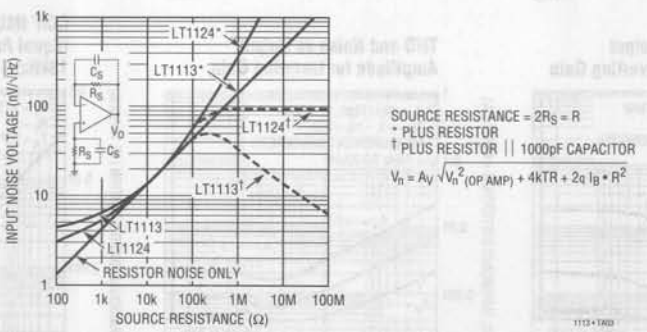


Figure 1. Comparison of LT1113 and LT1124 Total Output 1kHz Voltage Noise Versus Source Resistance

APPLICATIONS INFORMATION

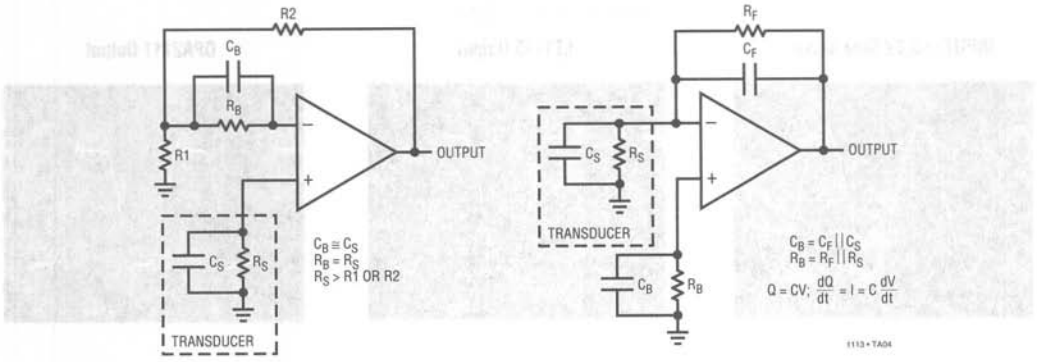


Figure 2. Noninverting and Inverting Gain Configurations

The gain therefore is 1 + C_F/C_S. For unity gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1113 and R_F should equal R_S. In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance; this voltage is then buffered by the LT1113 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors over increasing temperature, especially with transducer resistances of up to 100MΩ or more. The optimum value for R_S is determined by equating the thermal noise ($4kTR_S$) to the current noise times R_S, ($2qI_B$) R_S, resulting in $R_B = 2V_T/I_B$. A parallel capacitor, C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

The LT1113 can be operated from ±5V supplies for lower power dissipation resulting in lower I_B and noise at the expense of reduced dynamic range. To illustrate this benefit, let's take the following example:

An LT1113CS8 operates at an ambient temperature of 25°C with ±15V supplies, dissipating 318mW of power (typical supply current = 10.6mA for the dual). The S8 package has a θ_{JA} of 190°C/W, which results in a die temperature increase of 60.4°C or a room temperature die operating temperature of 85.4°C. At ±5V supplies, the die temperature increases by only one third of the previous amount or 20.1°C resulting in a typical die operating temperature of only 45.1°C. A 40 degree reduction of die temperature is achieved at the expense of a 20V reduction in dynamic range. If no DC correction resistor is used at the input, the input referred offset will be the input bias current at the operating die temperature times the transducer resistance (refer to Input Bias and Offset Currents vs Chip Temperature graph in Typical Performance Characteristics section). A 100mV input V_{OS} is the result of a 1nA I_B(at 85°C) dropped across a 100MΩ transducer resistance; at ±5V supplies, the input offset is only 28mV (I_B at 45°C is 280pA). Careful selection of a DC correction resistor (R_B) will reduce the IR errors due to I_B by an order of magnitude. A further reduction of IR errors can be

APPLICATIONS INFORMATION

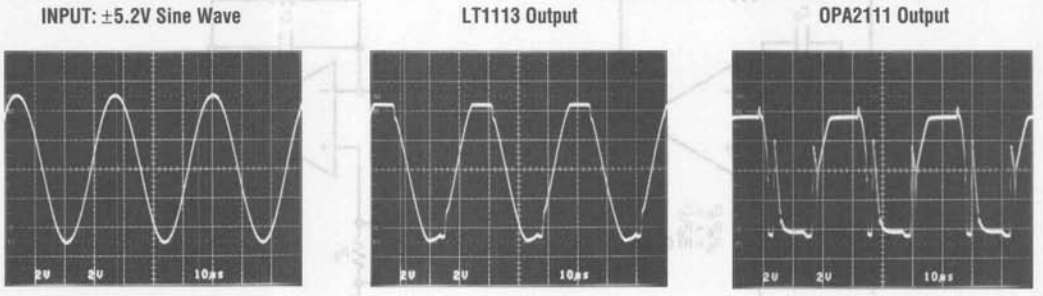


Figure 3. Voltage Follower with Input Exceeding the Common-Mode Range (V_S = ±5V)

achieved by using a DC servo circuit shown in the applications section of this data sheet. The DC servo has the advantage of reducing a wide range of IR errors to the millivolt level over a wide temperature variation. The preservation of dynamic range is especially important when reduced supplies are used, since input bias currents can exceed the nanoamp level for die temperatures over 85°C.

To take full advantage of a wide input common-mode range, the LT1113 was designed to eliminate phase reversal. Referring to the photographs shown in Figure 3, the LT1113 is shown operating in the follower mode (A_V = +1) at ±5V supplies with the input swinging ±5.2V. The output of the LT1113 clips cleanly and recovers with no phase reversal, unlike the competition as shown by the last photograph. This has the benefit of preventing lock-up in servo systems and minimizing distortion components. The effect of input and output overdrive on one amplifier has no effect on the other, as each amplifier is biased independently.

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration in Figure 4 illustrates these concepts. Output offset is a function of the difference between the two halves of the LT1113. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and bias current. Input bias current will be the average of the two noninverting input currents (I_{B+}). The difference between these two currents (ΔI_{B+}) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

APPLICATIONS INFORMATION

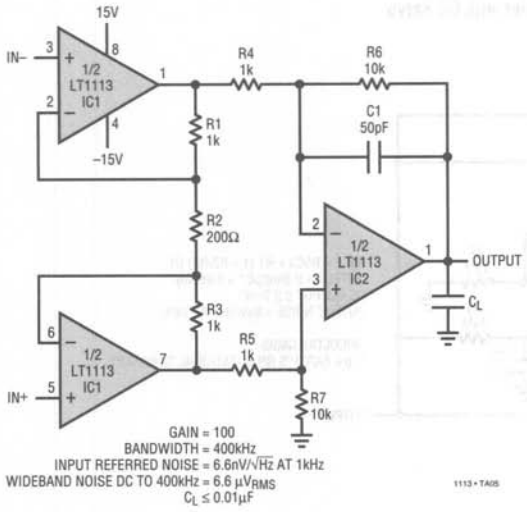


Figure 4. Three Op Amp Instrumentation Amplifier

The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A$ = +50μV/V or 86dB,

and $CMRR_B$ = + 39μV/V or 88dB,

then ΔCMRR = 11μV/V or 99dB;

if $CMRR_B$ = -39μV/V which is still 88dB,

then ΔCMRR = 89μV/V or 81dB

Clearly the LT1113, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 0.8mV

Input bias current = 320pA

Input offset current = 10pA

Input resistance = $10^{11}\Omega$

Input noise = $3.4\mu V_{P-P}$

High Speed Operation

The low noise performance of the LT1113 was achieved by making the input JFET differential pair large to maximize the first stage gain. Increasing the JFET geometry also increases the parasitic gate capacitance, which if left unchecked, can result in increased overshoot and ringing. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S,C_S), and the amplifier input capacitance (C_{IN} = 27pF). In closed loop gain configurations and with R_S and R_F in the kilohm range (Figure 5), this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

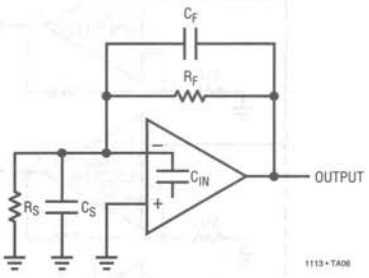
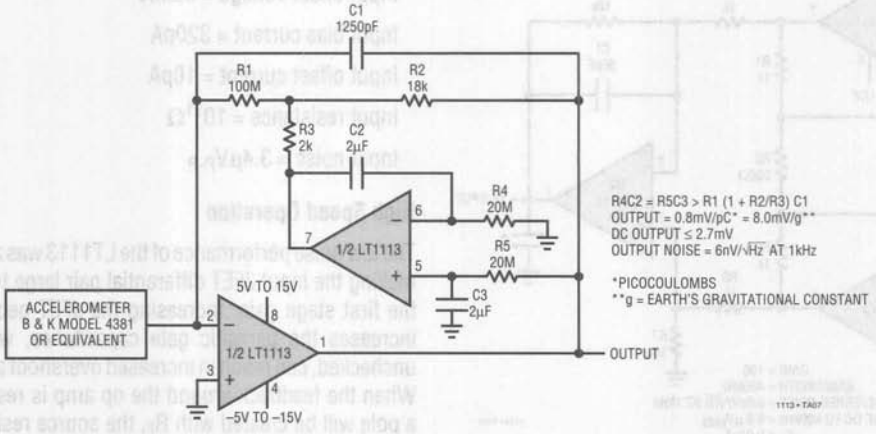


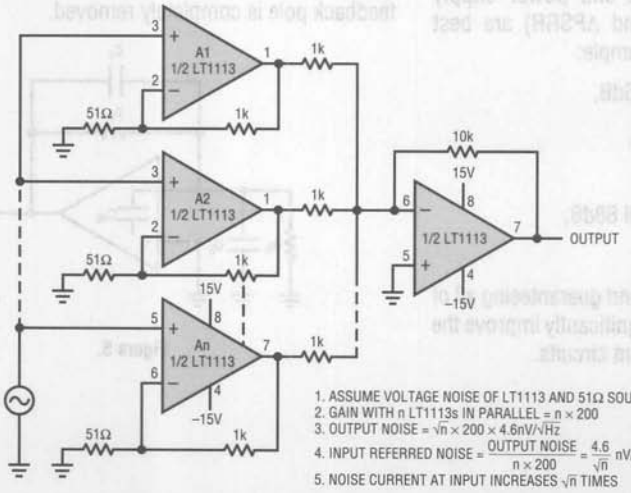
Figure 5.

TYPICAL APPLICATIONS

Accelerometer Amplifier with DC Servo



Paralleling Amplifiers to Reduce Voltage Noise

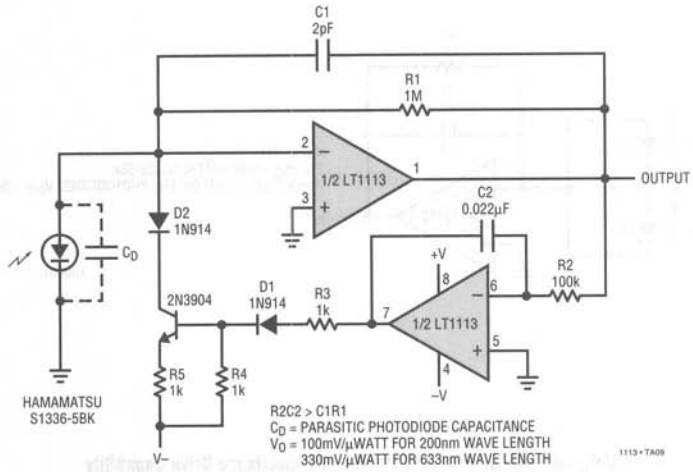


1. ASSUME VOLTAGE NOISE OF LT1113 AND 51Ω SOURCE RESISTOR = 4.6nV/√Hz
2. GAIN WITH n LT1113s IN PARALLEL = n × 200
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 4.6\text{nV}/\sqrt{\text{Hz}}$
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{4.6}{\sqrt{n}}\ \text{nV}/\sqrt{\text{Hz}}$
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES

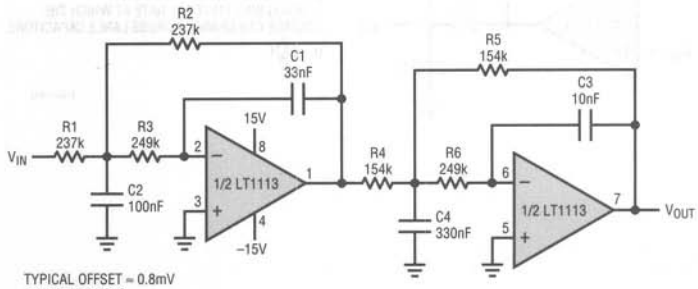
1113 • TA08

TYPICAL APPLICATIONS

Low Noise Light Sensor with DC Servo

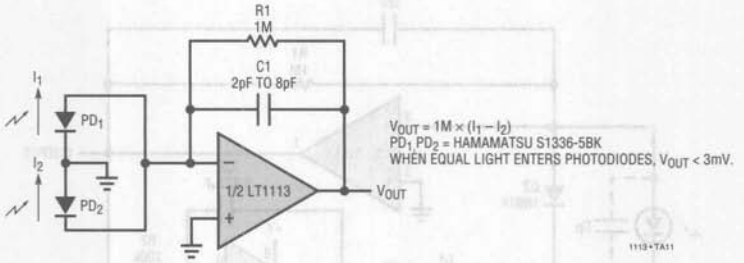


10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)

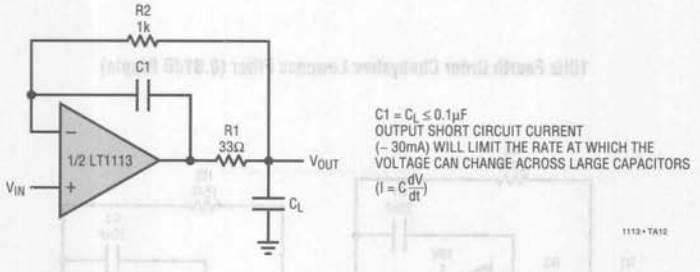


TYPICAL APPLICATIONS

Light Balance Detection Circuit



Unity Gain Buffer with Extended Load Capacitance Drive Capability



Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp

FEATURES

- **Input Bias Current, Warmed Up: 10pA Max**
- **100% Tested Low Voltage Noise: 8nV/√Hz Max**
- Very Low Input Capacitance: 1.5pF
- Voltage Gain: 1.2 Million Min
- Offset Voltage: 1.5mV Max
- Input Resistance: $10^{13}\Omega$
- Gain-Bandwidth Product: 5.3MHz Typ
- Guaranteed Specifications with ±5V Supplies
- Guaranteed Matching Specifications

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

DESCRIPTION

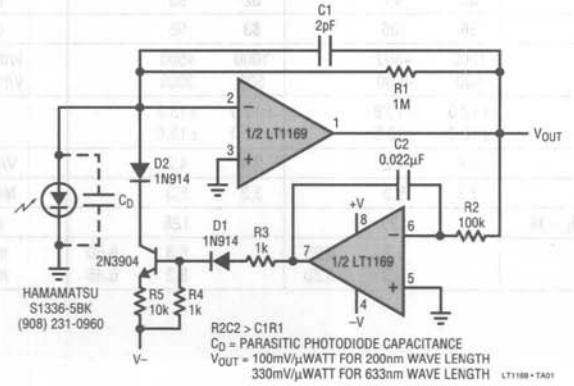
The LT1169 achieves a new standard of excellence in noise performance for a dual JFET op amp. For the first time low voltage noise (6nV/√Hz) is simultaneously offered with extremely low current noise (0.8fA/√Hz), providing the lowest total noise for high impedance transducer applications. Unlike most JFET op amps, the very low input bias current (3pA Typ) is maintained over the entire common-mode range which results in an extremely high input resistance ($10^{13}\Omega$). When combined with a very low input capacitance (1.5pF) an extremely high input impedance results making the LT1169 the first choice for amplifying low level signals from high impedance transducers. The low input capacitance also assures high gain linearity when buffering AC signals from high impedance transducers.

The LT1169 is unconditionally stable for gains of 1 or more, even with 1000pF capacitive loads. Other key features are 0.5mV V_{OS} and a voltage gain over 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate (4.2V/µs), and gain-bandwidth product (5.3MHz).

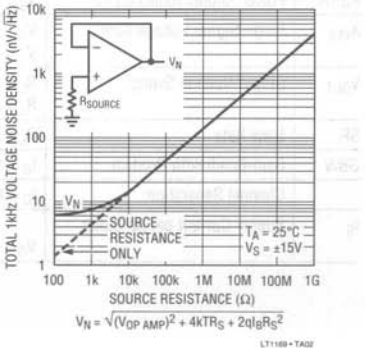
A full set of matching specifications are provided for precision instrumentation amplifier front ends. Specifications at ±5V supply operation are also provided. For an even lower voltage noise please see the LT1113 data sheet.

TYPICAL APPLICATION

Low Noise Light Sensor with DC Servo



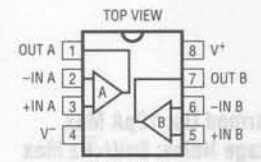
1kHz Output Voltage Noise Density vs Source Resistance



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
−55°C to 105°C ..... ±20V
105°C to 125°C ..... ±16V
Differential Input Voltage ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 80°C/W

ORDER PART NUMBER
LT1169ACN8
LT1169CN8

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1169A MIN	LT1169A TYP	LT1169A MAX	LT1169 MIN	LT1169 TYP	LT1169 MAX	UNITS
V_{OS}	Input Offset Voltage			0.50	1.5		0.60	2.0	mV
		V_S = ±5V		0.55	1.7		0.65	2.2	mV
I_{OS}	Input Offset Current	Warmed Up (Note 2)		1.5	7		2.5	15	pA
		T_J = 25°C (Note 5)		0.5	2		0.7	4	pA
I_B	Input Bias Current	Warmed Up (Note 2)		3	10		4.0	20	pA
		T_J = 25°C (Note 5)		1	3		1.5	5	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		17			17		$nV/\sqrt{Hz}$
		f_O = 1000Hz		6	8		6	8	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1kHz (Note 3)		0.8			1		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential Mode			10^{14}			10^{14}		Ω
	Common Mode	V_{CM} = −10V to 13V		10^{13}			10^{13}		Ω
C_{IN}	Input Capacitance			1.5			1.5		pF
		V_S = ±5V		2.0			2.0		pF
V_{CM}	Input Voltage Range (Note 4)		13.0	13.5		13.0	13.5		V
			−10.5	−11.0		−10.5	−11.0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −10V to 13V	85	98		82	95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	86	100		83	98		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k	1200	4800		1000	4500		V/mV
		V_O = ±10V, R_L = 1k	600	4000		500	3000		V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k	±13.0	±13.8		±13.0	±13.8		V
		R_L = 1k	±12.0	±13.0		±12.0	±13.0		V
SR	Slew Rate	$R_L \geq$ 2k (Note 6)	2.4	4.2		2.4	4.2		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	3.3	5.3		3.3	5.3		MHz
	Channel Separation	f_O = 10Hz, V_O = ±10V, R_L = 1k		130			126		dB
I_S	Supply Current per Amplifier			5.3	6.25		5.3	6.50	mA
		V_S = ±5V		5.3	6.20		5.3	6.45	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1169A MIN	LT1169A TYP	LT1169A MAX	LT1169 MIN	LT1169 TYP	LT1169 MAX	UNITS
ΔV_{OS}	Offset Voltage Match			0.8	2.7		0.8	3.5	mV
ΔI_B^+	Noninverting Bias Current Match	Warmed Up (Note 2)		2	8		3	20	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	81	94		78	94		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	82	95		80	95		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, (Note 9), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1169A MIN	LT1169A TYP	LT1169A MAX	LT1169 MIN	LT1169 TYP	LT1169 MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.6	2.9		0.7	3.2	mV
		$V_S = \pm 5V$	●		0.7	3.1		0.8	3.4	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		15	40		20	50	µV/°C
I_{OS}	Input Offset Current		●		8	40		10	50	pA
I_B	Input Bias Current		●		100	200		180	400	pA
V_{CM}	Input Voltage Range		●	12.9	13.4		12.9	13.4		V
			●	−10.0	−10.8		−10.0	−10.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -10V$ to 12.9V	●	81	97		79	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	83	99		81	97		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	900	3600		800	3400		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	500	2600		400	2400		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±12.5	±13.5		±12.5	±13.5		V
		$R_L = 1k$	●	±11.5	±12.7		±11.5	±12.7		V
SR	Slew Rate	$R_L \ge 2k$ (Note 6)	●	2.3	4		1.9	4		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	3	4.2		3	4.2		MHz
I_S	Supply Current per Amplifier		●		5.3	6.35		5.3	6.55	mA
		$V_S = \pm 5V$	●		5.3	6.30		5.3	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1	4		1.5	5	mV
ΔI_B^+	Noninverting Bias Current Match		●		3.5	35		5.5	50	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	●	76	93		74	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	79	93		77	93		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, (Note 7), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1169A MIN	LT1169A TYP	LT1169A MAX	LT1169 MIN	LT1169 TYP	LT1169 MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.7	3.5		0.8	3.8	mV
		$V_S = \pm 5V$	●		0.8	3.7		0.9	4.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		15	40		20	50	µV/°C
I_{OS}	Input Offset Current		●		20	100		30	200	pA
I_B	Input Bias Current		●		280	600		320	1200	pA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	−10.0	−10.5		−10.0	−10.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -10V$ to 12.6V	●	80	96		78	93		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	81	98		79	96		dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, (Note 7), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1169A MIN	LT1169A TYP	LT1169A MAX	LT1169 MIN	LT1169 TYP	LT1169 MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	850	3300		750	3000		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	400	2200		300	2000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±12.5	±12.5		±12.5	±12.5		V
		$R_L = 1k$	●	±11.3	±12.0		±11.3	±12.0		V
SR	Slew Rate	$R_L \ge 2k$	●	2.2	3.8		1.8	3.8		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	2.7	4		2.7	4		MHz
I_S	Supply Current per Amplifier		●		5.30	6.35		5.30	6.55	mA
		$V_S = \pm 5V$	●		5.25	6.30		5.25	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.6	5		1.8	6	mV
ΔI_B^+	Noninverting Bias Current Match		●		8	80		10	180	pA
ΔCMRR	Common-Mode Rejection Match	(Note 8)	●	76	93		73	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	77	92		75	92		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1169s (200 op amps) typically 120 op amps will be better than the indicated specification.

Note 2: I_B and I_{OS} readings are extrapolated to a warmed-up temperature from 25°C measurements and 45°C characterization data.

Note 3: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 4: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade), to 2.8mV (C grade).

Note 5: This parameter is not 100% tested.

Note 6: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

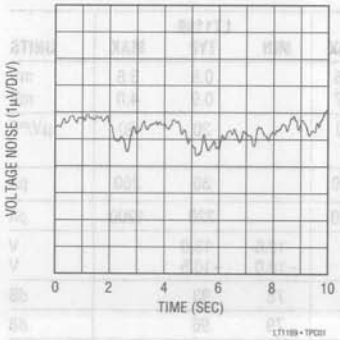
Note 7: The LT1169 is not tested and not quality assurance sampled at 85°C and at −40°C. These specifications are guaranteed by design, correlation and/or inference from −55°C, 25°C, and/or 125°C characterization and 0°C, 70°C tests.

Note 8: ΔCMRR and ΔPSRR are defined as follows:
(1) CMRR and PSRR are measured in µV/V on the individual amplifiers.
(2) The difference is calculated between the matching sides in µV/V.
(3) The result is converted to dB.

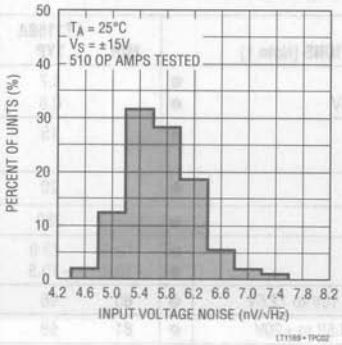
Note 9: The LT1169 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

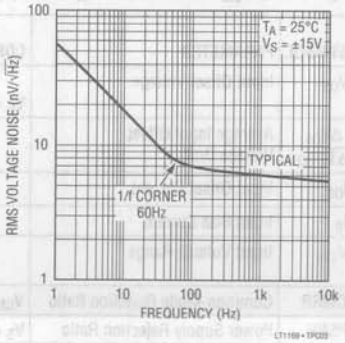
0.1Hz to 10Hz Voltage Noise



1kHz Input Noise Voltage Distribution

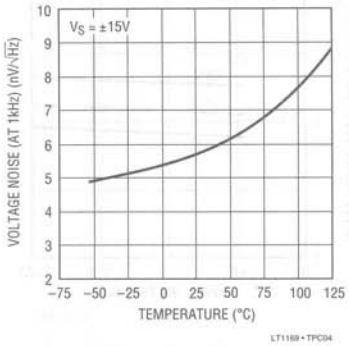


Voltage Noise vs Frequency

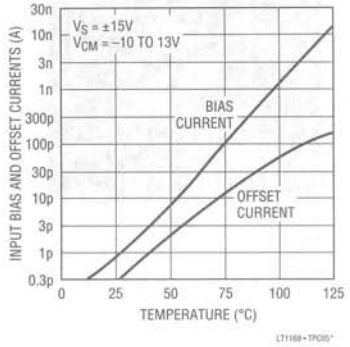


TYPICAL PERFORMANCE CHARACTERISTICS

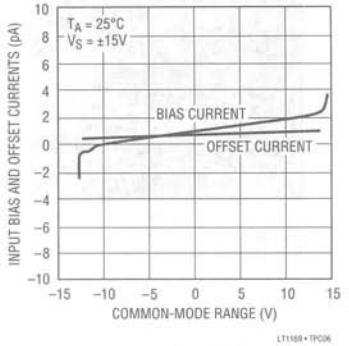
Voltage Noise vs Chip Temperature



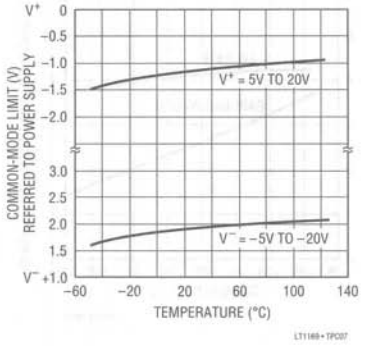
Input Bias and Offset Currents vs Chip Temperature



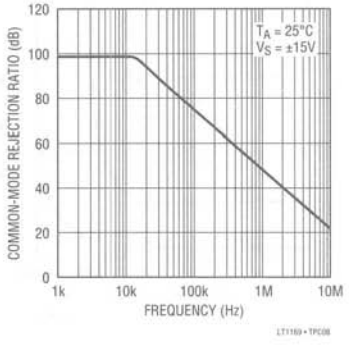
Input Bias and Offset Currents Over the Common-Mode Range



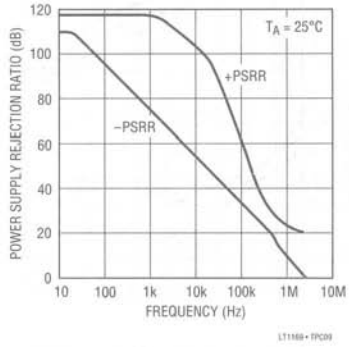
Common-Mode Limit vs Temperature



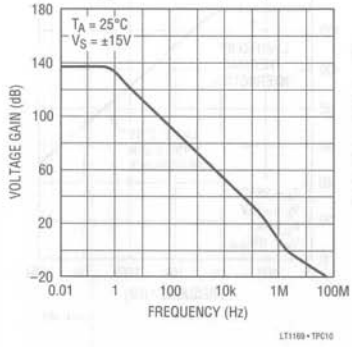
Common-Mode Rejection Ratio vs Frequency



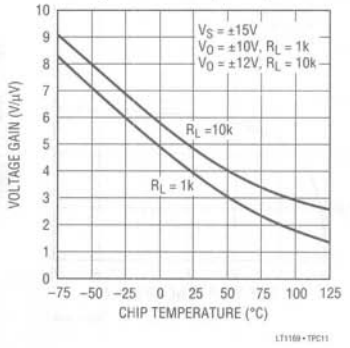
Power Supply Rejection Ratio vs Frequency



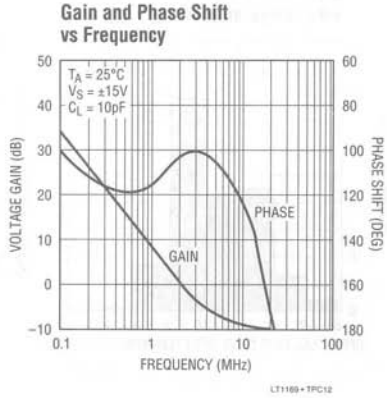
Voltage Gain vs Frequency



Voltage Gain vs Chip Temperature



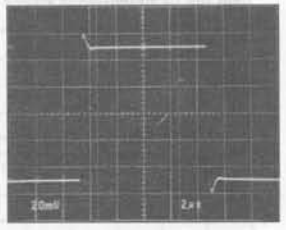
Gain and Phase Shift vs Frequency



2

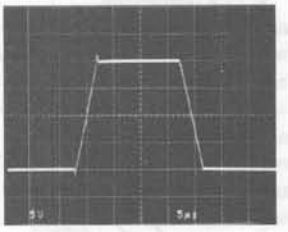
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response



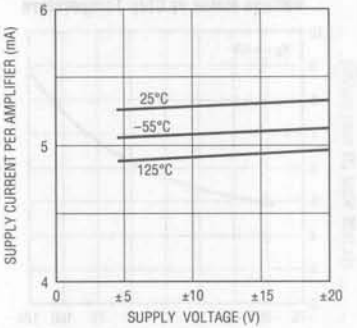
$A_V = 1$
$C_L = 10pF$
$V_S = \pm15V, \pm5V$
2µs/DIV

Large-Signal Transient Response

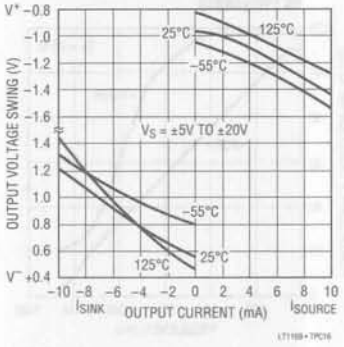


$A_V = 1$
$C_L = 10pF$
$V_S = \pm15V$
5µs/DIV

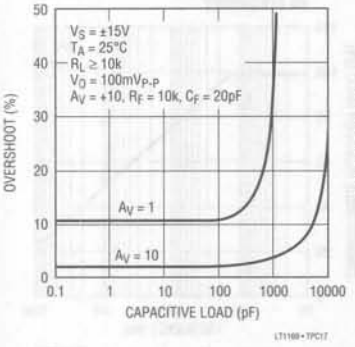
Supply Current vs Supply Voltage



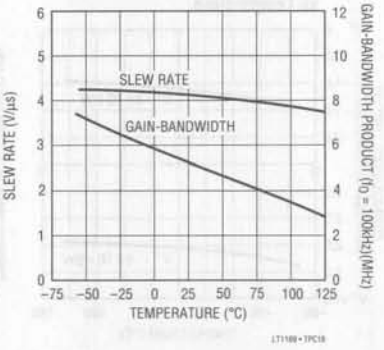
Output Voltage Swing vs Load Current



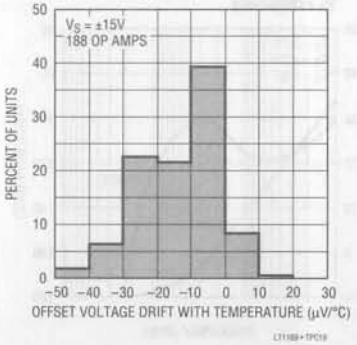
Capacitive Load Handling



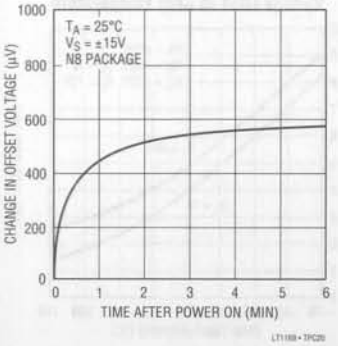
Slew Rate and Gain-Bandwidth Product vs Temperature



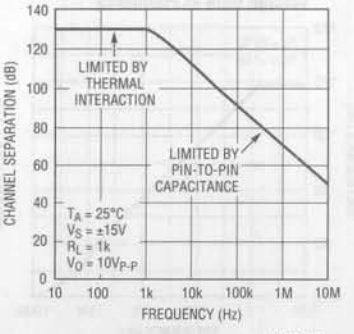
Distribution of Offset Voltage Drift with Temperature



Warm-Up Drift

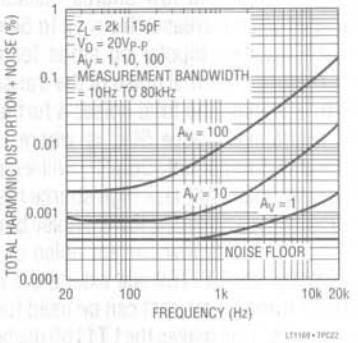


Channel Separation vs Frequency

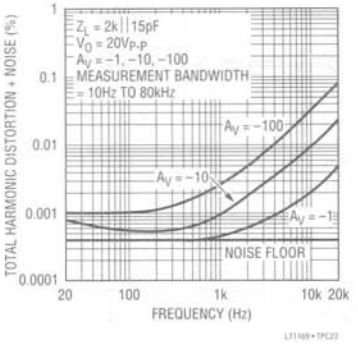


TYPICAL PERFORMANCE CHARACTERISTICS

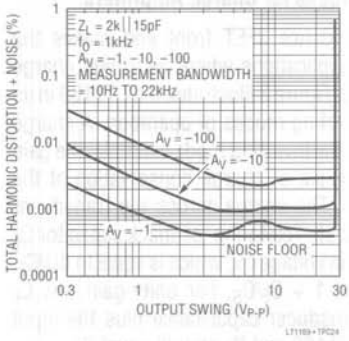
THD and Noise vs Frequency for Noninverting Gain



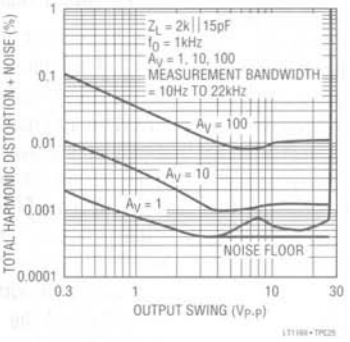
THD and Noise vs Frequency for Inverting Gain



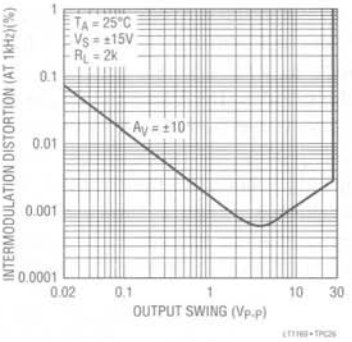
THD and Noise vs Output Amplitude for Inverting Gain



THD and Noise vs Output Amplitude for Noninverting Gain



CCIF IMD Test (Equal Amplitude Tones at 13kHz, 14kHz)*



*SEE LT1115 DATA SHEET FOR DEFINITION OF CCIF TESTING

APPLICATIONS INFORMATION

LT1169 vs the Competition

With improved noise performance, the LT1169 dual in the plastic DIP directly replaces such JFET op amps as the OPA2111, OPA2604, OP215, and the AD822. The combination of low current and voltage noise of the LT1169 allows it to surpass most dual and single JFET op amps. The LT1169 can replace many of the lowest noise bipolar amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps will eventually lose out to the LT1169 when transducer impedance increases due to higher current noise.

The extremely high input impedance ($10^{13}\Omega$) assures that the input bias current is almost constant over the entire common-mode range. Figure 1 shows how the LT1169 stands up to the competition. Unlike the competition, as the input voltage is swept across the entire common-mode range the input bias current of the LT1169 hardly changes. As a result the current noise does not degrade. This makes the LT1169 the best choice in applications where an amplifier has to buffer signals from a high impedance transducer.

APPLICATIONS INFORMATION

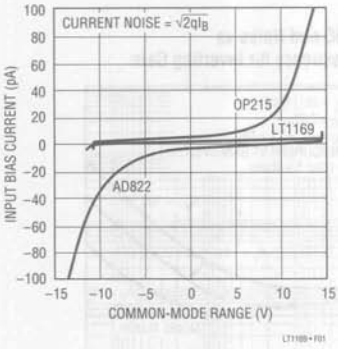


Figure 1. Comparison of LT1169, OP215, and AD822 Input Bias Current vs Common-Mode Range

Amplifying Signals from High Impedance Transducers

The low voltage and current noise offered by the LT1169 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers, and photodiodes. The total output noise in such a system is the gain times the RMS sum of the op amp's input referred voltage noise, the thermal noise of the transducer, and the op amp's input bias current noise times the transducer impedance. Figure 2 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate

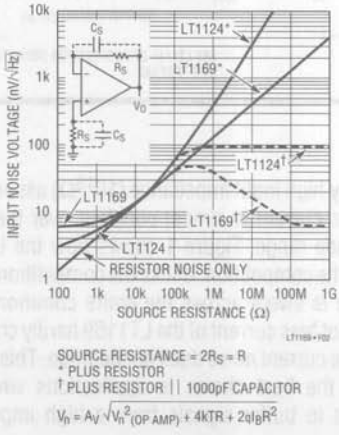


Figure 2. Comparison of LT1169 and LT1124 Total Output 1kHz Voltage Noise vs Source Resistance

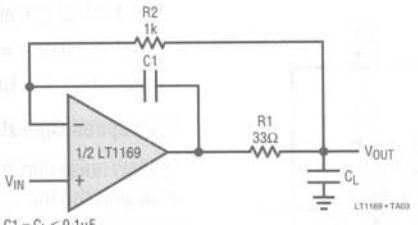
the total noise. This means the LT1169 is superior to most dual JFET op amps. Only the lowest noise bipolar op amps have the advantage at low source resistances. As the source resistance increases from 5k to 50k, the LT1169 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_BR^2$) will eventually dominate the total noise. At these high source resistances, the LT1169 will out perform the lowest noise bipolar op amps due to the inherently low current noise of FET input op amps. Clearly, the LT1169 will extend the range of high impedance transducers that can be used for high signal-to-noise ratios. This makes the LT1169 the best choice for high impedance, capacitive transducers.

Optimization Techniques for Charge Amplifiers

The high input impedance JFET front end makes the LT1169 suitable in applications where very high charge sensitivity is required. Figure 3 illustrates the LT1169 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; the gain depends on the principal of charge conservation at the input of the LT1169. The charge across the transducer capacitance C_S is transferred to the feedback capacitor C_F resulting in a change in voltage dV, which is equal to dQ/C_F. The gain therefore is $1 + C_F/C_S$. For unity-gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1169 and R_F should equal R_S.

In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance, C_S. This voltage is then buffered by the LT1169 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors over increasing temperature, especially with transducer resistances of up to 1000MΩ or more. The optimum value for R_B is determined by equating the thermal noise ($4kTR_S$) to the current noise ($2qI_B$) times R_S^2. Solving for R_S results in $R_B = R_S = 2V_T/I_B$. A parallel

APPLICATIONS INFORMATION



$C1 = C_L \leq 0.1\mu F$
OUTPUT SHORT CIRCUIT CURRENT (– 30mA) WILL LIMIT THE RATE AT WHICH THE VOLTAGE CAN CHANGE ACROSS LARGE CAPACITORS
$\left(I = C\frac{dV}{dt}\right)$

Figure 3. Inverting and Noninverting Gain Configurations

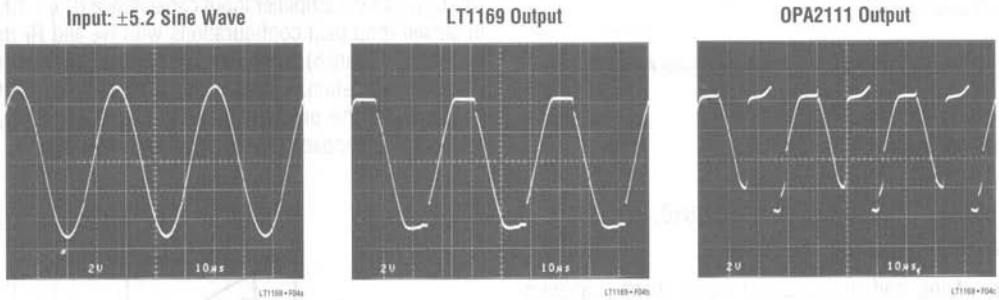


Figure 4. Voltage Follower with Input Exceeding the Common-Mode Range ($V_S = \pm 5V$)

capacitor C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

To take full advantage of a wide input common-mode range, the LT1169 was designed to eliminate phase reversal. Referring to the photographs in Figure 4, the LT1169 is shown operating in the follower mode ($A_V = 1$) at ±5V supplies with the input swinging ±5.2V. The output of the LT1169 clips cleanly and recovers with no phase reversal, unlike the competition as shown by the last photograph. This has the benefit of preventing lockup in servo systems and minimizing distortion components. The effect of input and output overdrive on one amplifier has no effect on the other, as each amplifier is biased independently.

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration in Figure 5 illustrates these concepts. Output offset is a function of the difference between the two halves of the LT1169. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and bias current. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

APPLICATIONS INFORMATION

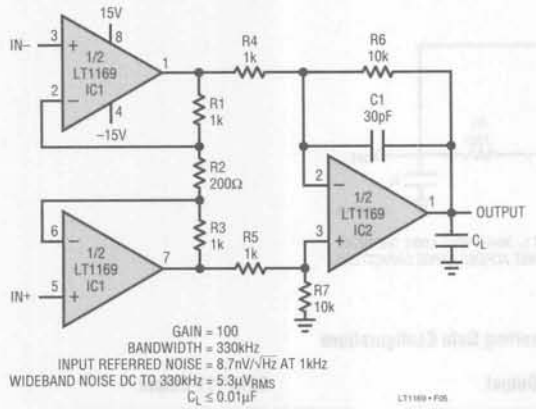


Figure 5. Three Op Amp Instrumentation Amplifier

Assume $CMRR_A = 50\mu V/V$ or 86dB,
and $CMRR_B = 39\mu V/V$ or 88dB,
then $\Delta CMRR = 11\mu V/V$ or 99dB;
if $CMRR_B = -39\mu V/V$ which is still 88dB,
then $\Delta CMRR = 89\mu V/V$ or 81dB

By specifying and guaranteeing all of these matching parameters, the LT1169 can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 0.8mV
Input bias current = 4pA
Input offset current = 3pA
Input resistance = $10^{13}\Omega$
Input noise = $3.4\mu V_{P-P}$

High Speed Operation

The low noise performance of the LT1169 was achieved by enlarging the input JFET differential pair to maximize the first stage gain. Enlarging the JFET geometry also increases the parasitic gate capacitance, which if left unchecked, can result in increased overshoot and ringing. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S,C_S), and the amplifier input capacitance (C_{IN} = 1.5pF). In closed-loop gain configurations with R_S and R_F in the MΩ range (Figure 6), this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

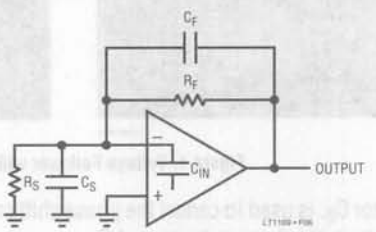
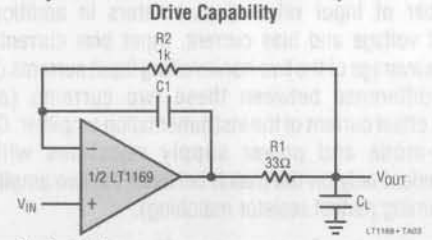


Figure 6.

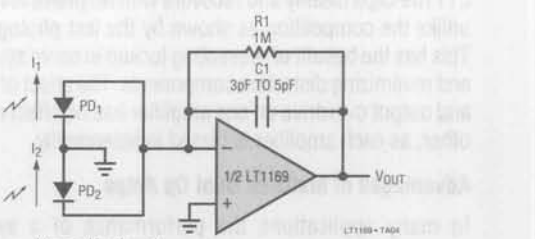
TYPICAL APPLICATIONS

Unity-Gain Buffer with Extended Load Capacitance Drive Capability



$C1 = C_L \leq 0.1\mu F$
OUTPUT SHORT CIRCUIT CURRENT (~ 30mA) WILL LIMIT THE RATE AT WHICH THE VOLTAGE CAN CHANGE ACROSS LARGE CAPACITORS ($I = C\frac{dV}{dt}$)

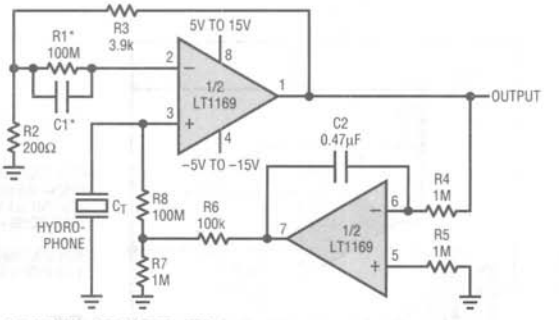
Light Balance Detection Circuit



$V_{OUT} = 1M \times (I_1 - I_2)$
PD_1 PD_2 = HAMAMATSU S1336-5BK
WHEN EQUAL LIGHT ENTERS PHOTODIODES, $V_{OUT} < 3mV$.

TYPICAL APPLICATIONS

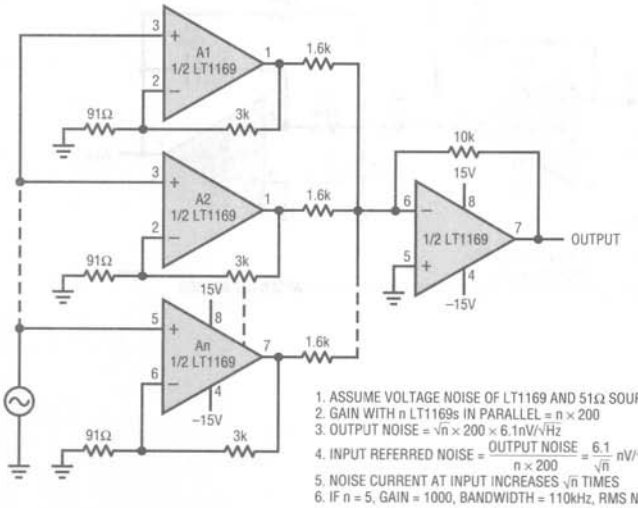
Low Noise Hydrophone Amplifier with DC Servo



DC OUTPUT ≤ 2.5mV FOR T_A < 70°C
OUTPUT VOLTAGE NOISE = 128nV/√Hz AT 1kHz (GAIN = 20)
C1 ≈ C_T ≈ 100pF TO 5000pF; R4C2 > R8C_T; *OPTIONAL

LT1169 • TA05

Paralleling Amplifiers to Reduce Voltage Noise

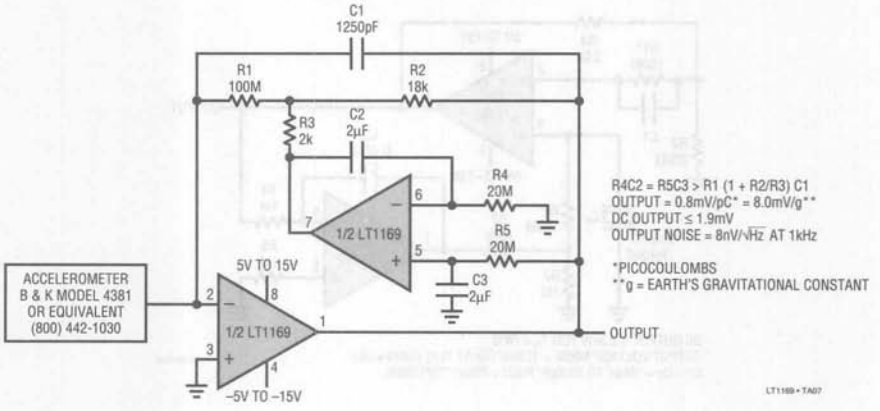


1. ASSUME VOLTAGE NOISE OF LT1169 AND 51Ω SOURCE RESISTOR = 6.1nV/√Hz
2. GAIN WITH n LT1169s IN PARALLEL = n × 200
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 6.1nV/\sqrt{Hz}$
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{6.1}{\sqrt{n}}$ nV/√Hz
5. NOISE CURRENT AT INPUT INCREASES √n TIMES
6. IF n = 5, GAIN = 1000, BANDWIDTH = 110kHz, RMS NOISE, DC TO 1MHz = $\frac{2.1\mu V}{\sqrt{5}} = 1.0\mu V$

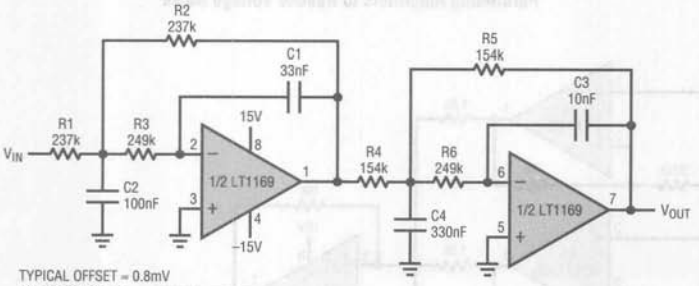
LT1169 • TA06

TYPICAL APPLICATIONS

Accelerometer Amplifier with DC Servo



10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)

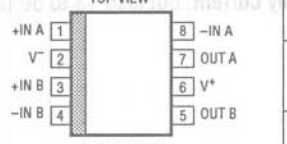


20μA Max, Dual SO-8 Package, Single Supply Precision Op Amp

FEATURES

- 8-Pin SO Package
- 20μA Max Supply Current per Amplifier
- 180μV Max Offset Voltage
- 350pA Max Offset Current
- $0.9\mu V_{P-P}$, 0.1Hz to 10Hz Voltage Noise
- $1.5pA_{P-P}$, 0.1Hz to 10Hz Current Noise
- 0.6μV/°C Offset Voltage Drift
- Single Supply Operation:
  - Input Voltage Range Includes Ground
  - Output Swings to Ground While Sinking Current
  - No Pull-Down Resistors Are Needed
- Output Sources and Sinks 5mA Load Current

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LT1178S8
PART MARKING
1178

Please note that the LT1178S8 surface mount pinout differs from that of the LT1178 standard plastic or ceramic dual-in-line packages.

Consult factory for Industrial and Military grade parts.

DESCRIPTION

The LT1178S8 is a micropower dual op amp in the surface mount 8-pin package. It is optimized for single supply operation at 5V. Specifications are also provided at ±15V supplies.

The extremely low supply current is combined with true precision specifications: offset voltage is 60μV, offset current is 50pA. Both offset parameters have low drift with temperature. The $1.5pA_{P-P}$ current noise and picoampere offset current permit the use of megohm level source resistors without introducing serious errors. Voltage noise at $0.9\mu V_{P-P}$ is remarkably low considering the low supply current.

The LT1178S8 can be operated from a single supply as low as one lithium cell or two Ni-Cad batteries. The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current—no power consuming pull-down resistors are needed.

For applications where three times higher supply current is acceptable, the micropower LT1077 single, LT1078 dual and LT1079 quad are recommended. The LT1077/LT1078/LT1079 have significantly higher bandwidth, slew rate; lower voltage noise and better output drive capability.

2

ELECTRICAL CHARACTERISTICS

For electrical specifications not listed below, refer to the standard LT1178C data sheet with the changes noted on this page.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V	T_A = 25°C		60	180	μV
		V_S = 5V, 0V	0°C ≤ T_A ≤ 70°C		85	350	μV
		V_S = ±15V	T_A = 25°C		120	350	μV
		V_S = ±15V	0°C ≤ T_A ≤ 70°C		150	540	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 1)	V_S = 5V, 0V	0°C ≤ T_A ≤ 70°C		0.6	3.5	μV/°C
		V_S = ±15V	0°C ≤ T_A ≤ 70°C		0.7	3.8	μV/°C

Note 1: Not 100% production tested.

Single Supply, Dual Precision Op Amp

FEATURES

Single Supply Operation:

- Input Goes Below Ground
- Output Swings to Ground Sinking Current
- No Pull-Down Resistors Needed
- Phase Reversal Protection

At 5V, 0V Low Cost Grade Specifications:

- 280µV Max Offset Voltage
- 380µV Max in S8 Package
- 0.8nA Max Offset Current
- 480µA Max Supply Current per Amplifier
- 0.5µV/°C Drift
- 1.4 Million Voltage Gain
- 950kHz Gain-Bandwidth Product
- 0.55µV$_{P-P}$, 0.1Hz to 10Hz Noise

APPLICATIONS

- Single Supply Systems
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters
- Battery-Powered Systems
- Strain Gauge and Bridge Amplifiers

DESCRIPTION

The LT1413 is a low cost, upgraded version of Linear Technology's industry standard LT1013 dual, single supply op amp. The LT1413 is optimized for single 5V applications, although ±15V specifications are also provided for completeness.

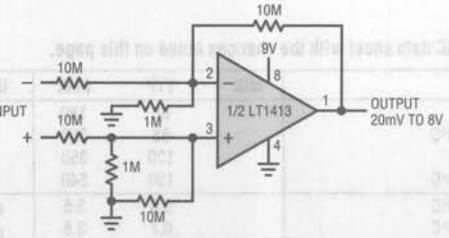
In the design of the LT1413, particular emphasis has been placed on low cost plastic and SO-8 package performance: 60µV offset voltage, 0.1nA offset current, in excess of 10mA output current at 330µA supply current and 140dB channel separation are some of the specifications achieved.

Other dual, single supply amplifiers are available to complement the LT1413 family: the micropower LT1078's supply current is 10 times lower with a 4.5 fold speed performance degradation compared to the LT1413. Conversely, the LT1211, LT1213 and LT1215 duals have 4 to 14 times higher supply current, but also 13 to 50 times higher speed.

Protected by U.S. Patent 4,775,884.

TYPICAL APPLICATION

+90V, –3V Common-Mode Range Difference Amplifier (A_V = 1)

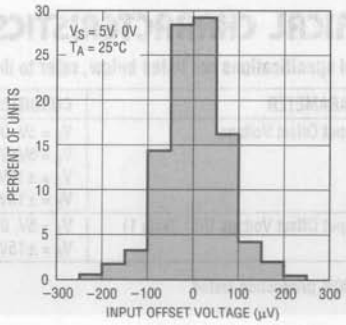


OUTPUT OFFSET = 1.5mV
(INPUT REFERRED = 125µV)
INPUT RESISTANCE = 11M
BANDWIDTH = 80kHz

(THE 0.1nA TYPICAL OFFSET CURRENT PERMITS THE USE OF 1MΩ RESISTORS)

LT1413 • TA03

Distribution of Input Offset Voltage (In Plastic DIP, N8 Package)



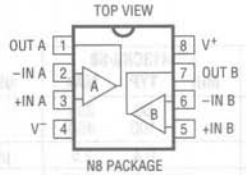
LT1413 • TA01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage .....
  Equal to Positive Supply Voltage
  5V Below Negative Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

Note: When the input voltage exceeds the maximum ratings, the input current should be limited to 10mA.

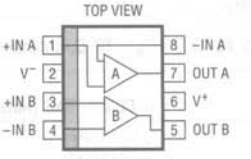
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1413ACN8
LT1413CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-LEAD DIP PIN LOCATIONS. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE CONFIGURATION.

T_{JMAX} = 105°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LT1413S8
S8 PART MARKING
1413

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8 LT1413S8		50	150		60 80	280 380	µV µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability			0.4			0.5		µV/Mo
I_{OS}	Input Offset Current			0.1	0.7		0.1	0.8	nA
I_B	Input Bias Current			9	15		9	18	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.55	1.1		0.55		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz (Note 2) f_O = 1000Hz (Note 2)		24 23	38 30		24 23		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz		2.8			2.8		pA_{P-P}
	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		0.07 0.02			0.07 0.02		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance Differential Mode Common Mode	(Note 3)	 300	 500 3		 250	 500 3		 MΩ GΩ
	Input Voltage Range		3.65 0	3.8 −0.3		3.65 0	3.8 −0.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.65V	90	101		88	101		dB
PSRR	Power Supply Rejection Ratio	V_S = 3.2V to 12V	102	118		100	118		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 4V, No Load V_O = 0.05V to 3.5V, R_L = 2k	400 300	1400 1000		350 250	1400 1000		V/mV V/mV

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
	Maximum Output Voltage Swing	Output Low, No Load		15	25		15	25	mV
		Output Low, 600Ω to GND		5	10		5	10	mV
		Output Low, I_{SINK} = 1mA		220	350		220	350	mV
		Output High, No Load	4.1	4.4		4.1	4.4		V
		Output High, 600Ω to GND	3.4	4.0		3.4	4.0		V
SR	Slew Rate	A_V = 1	0.2	0.3		0.2	0.3		V/µs
GBW	Gain-Bandwidth Product	$f_O \leq$ 100kHz (Note 4)	600	950		600	950		kHz
I_S	Supply Current per Amplifier			330	450		330	480	µA
	Channel Separation	ΔV_{IN} = 3V, R_L = 2k (Note 5)	125	140		123	140		dB
	Minimum Supply Voltage	(Note 6)		2.85	3.0		2.85	3.0	V

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8	●		65	240		80	390	µV
		LT1413S8	●					100	490	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.3	2.0		0.4	2.5	µV/°C
I_{OS}	Input Offset Current		●		0.1	1.0		0.1	1.2	nA
I_B	Input Bias Current		●		10	20		10	23	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.6V	●	88	100		85	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 3.45V to 12V	●	100	117		97	117		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.07V to 3.9V, No Load	●	300	1100		300	1100		V/mV
		V_O = 0.07V to 3.2V, R_L = 2k	●	200	800		200	800		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		18	32		18	32	mV
		Output Low, I_{SINK} = 1mA	●		270	430		270	430	mV
		Output High, No Load	●	4.0	4.3		4.0	4.3		V
		Output High, 600Ω to GND	●	3.3	3.9		3.2	3.9		V
I_S	Supply Current per Amplifier		●		350	500		350	530	µA

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, −40°C ≤ T_A ≤ 85°C (Note 7)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8	●		70	300		85	470	µV
		LT1413S8	●					110	570	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		0.3	2.2		0.4	2.8	µV/°C
I_{OS}	Input Offset Current		●		0.2	1.4		0.2	1.7	nA
I_B	Input Bias Current		●		11	25		11	30	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.4V	●	85	99		82	99		dB
PSRR	Power Supply Rejection Ratio	V_S = 3.9V to 12V	●	98	116		94	116		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.08V to 3.8V, No Load	●	220	1000		220	1000		V/mV
		V_O = 0.08V to 3.0V, R_L = 2k	●	150	700		150	700		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		20	38		20	38	mV
		Output Low, I_{SINK} = 1mA	●		300	480		300	480	mV
		Output High, No Load	●	3.9	4.2		3.9	4.2		V
		Output High, 600Ω to GND	●	3.1	3.8		3.0	3.8		V
I_S	Supply Current per Amplifier		●		360	550		360	580	µA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8 LT1413S8		75	280		90 110	480 580	µV µV
I_{OS}	Input Offset Current			0.1	0.7		0.1	0.8	nA
I_B	Input Bias Current			8	15		8	18	nA
	Input Voltage Range		13.5 −15.0	13.8 −15.3		13.5 −15.0	13.8 −15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13.5V, -15V$	100	117		97	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120		100	117		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	1500	5000		1200	4000		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L = 2k$	±13	±14		±12.5	±14		V
SR	Slew Rate		0.2	0.4		0.2	0.4		V/µs
I_S	Supply Current per Amplifier			350	500		350	550	µA

$V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8 LT1413S8	● ●		95	390		110 130	620 720	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.4	2.5		0.5	3.0	µV/°C
I_{OS}	Input Offset Current		●		0.1	1.0		0.1	1.2	nA
I_B	Input Bias Current		●		9	20		9	23	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	1000	4000		700	3000		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	98	116		94	113		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	101	119		97	116		dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9		±12.0	±13.9		V
I_S	Supply Current per Amplifier		●		360	550		360	600	µA

$V_S = \pm 15V$, $-40°C \le T_A \le 85°C$ (Note 7)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1413ACN8 MIN	LT1413ACN8 TYP	LT1413ACN8 MAX	LT1413CN8/S8 MIN	LT1413CN8/S8 TYP	LT1413CN8/S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1413N8 LT1413S8	● ●		100	460		120 140	700 800	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		0.4	2.8		0.5	3.3	µV/°C
I_{OS}	Input Offset Current		●		0.2	1.4		0.2	1.7	nA
I_B	Input Bias Current		●		10	25		10	30	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	800	3000		500	2400		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	97	115		92	112		dB
PSRR	Power Supply Rejection Ratio	$V_S \pm 2V$ to $\pm 18V$	●	100	118		95	115		dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12.2	±13.8		±11.8	±13.8		V
I_S	Supply Current per Amplifier		●		370	580		370	630	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1413s typically 120 op amps will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only. All noise parameters are tested with $V_S = \pm 2.5V$, $V_O = 0V$.

Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Gain-Bandwidth Product is not tested. It is inferred from the slew rate measurement.

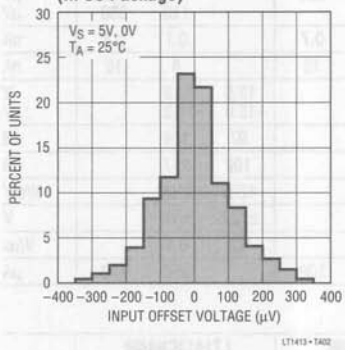
Note 5: This parameter is not 100% tested.

Note 6: At the minimum supply voltage, the offset voltage changes less than 200µV compared to its value at 5V, 0V.

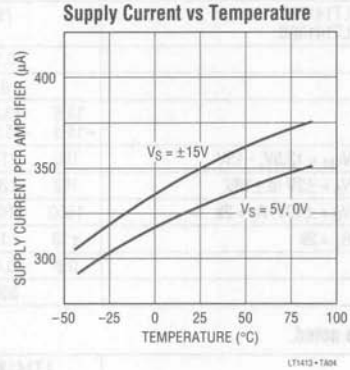
Note 7: The LT1413 is not tested and is not quality-assurance sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from 0°C, 25°C and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

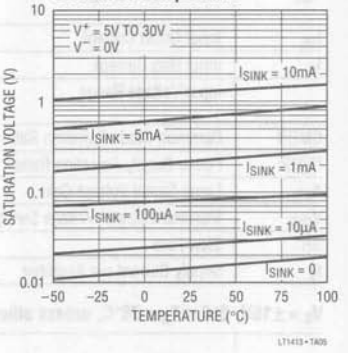
Distribution of Input Offset Voltage (In S8 Package)



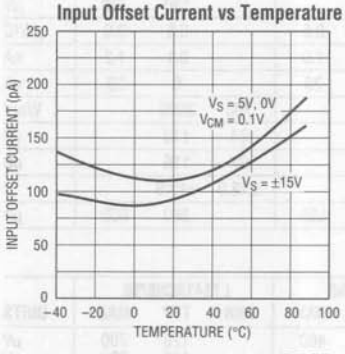
Supply Current vs Temperature



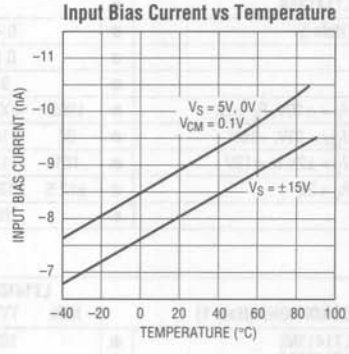
Output Saturation vs Sink Current vs Temperature



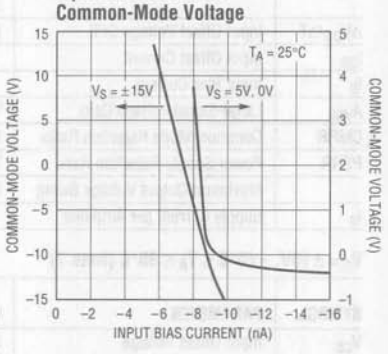
Input Offset Current vs Temperature



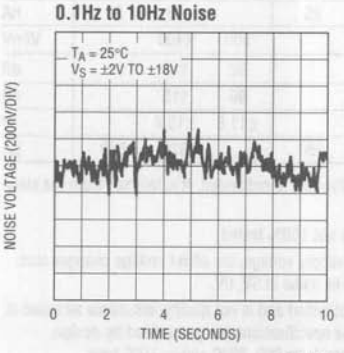
Input Bias Current vs Temperature



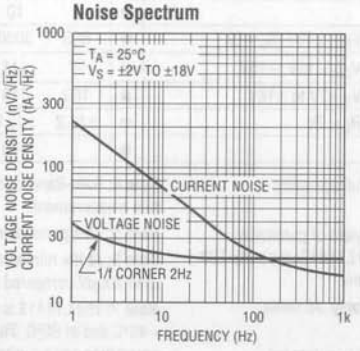
Input Bias Current vs Common-Mode Voltage



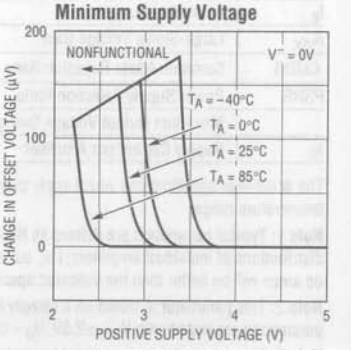
0.1Hz to 10Hz Noise



Noise Spectrum

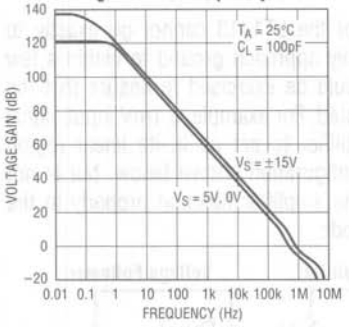


Minimum Supply Voltage

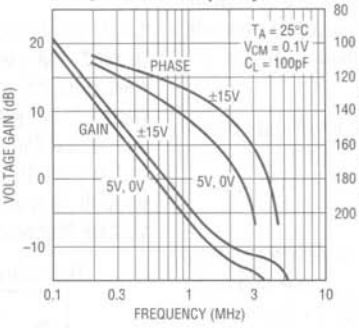


TYPICAL PERFORMANCE CHARACTERISTICS

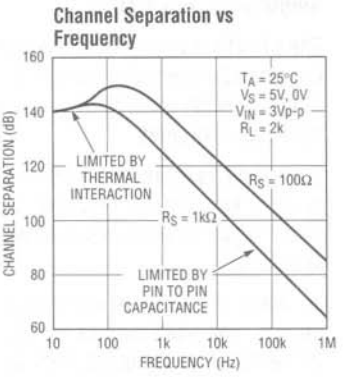
Voltage Gain vs Frequency



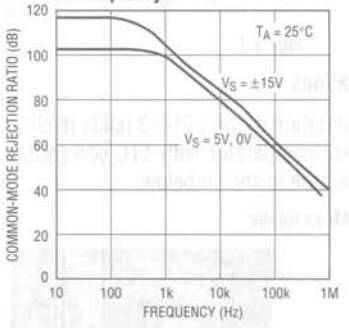
Gain, Phase vs Frequency



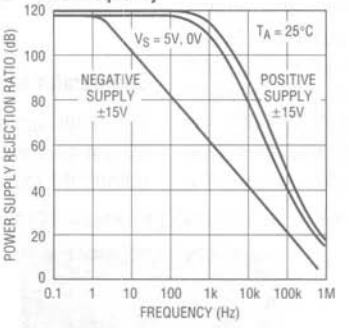
Channel Separation vs Frequency



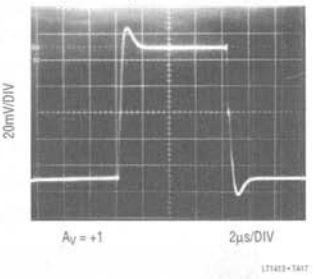
Common-Mode Rejection Ratio vs Frequency



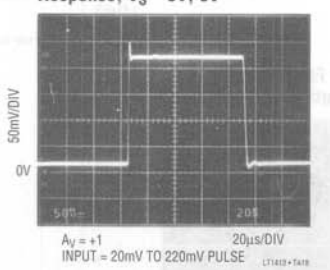
Power Supply Rejection Ratio vs Frequency



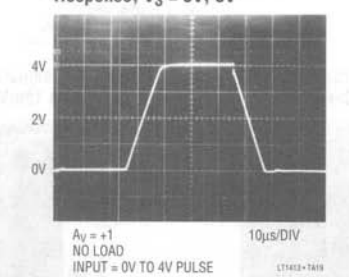
Small Signal Transient Response, V_S = ±15V



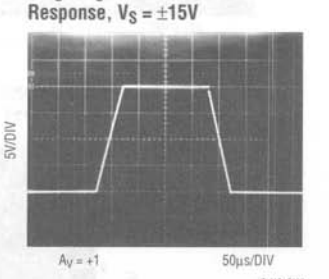
Small Signal Transient Response, V_S = 5V, 0V



Large Signal Transient Response, V_S = 5V, 0V



Large Signal Transient Response, V_S = ±15V



2

APPLICATIONS INFORMATION

Single Supply Operation

The LT1413 is fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground.

If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-21 and OP-221.

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1413, the 400Ω resistors, in series with the input (see Schematic Diagram), protect the devices even when the input is 5V below ground.

b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1413 outputs do not reverse, as illustrated below, even when the inputs are at –1.5V. Keep the output of the other amplifier out of negative saturation for the phase reversal protection to function properly.

Since the output of the LT1413 cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage-follower mode.

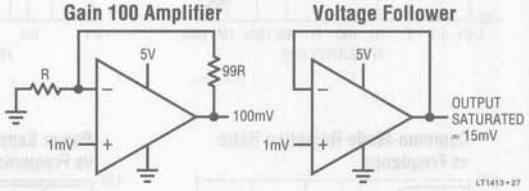
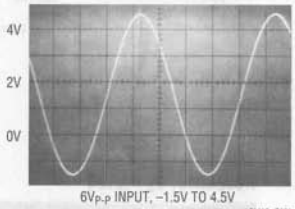


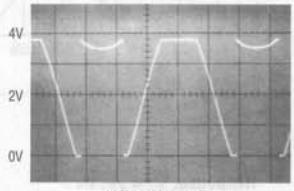
Figure 1.

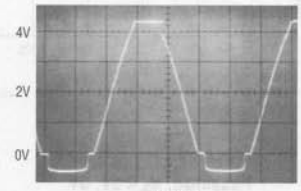
Comparator Applications

The single supply operation of the LT1413 lends itself to its use as a precision comparator with TTL compatible output; the response time is shown below.

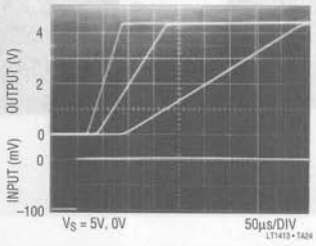
Voltage Follower with Input Exceeding the Negative Common-Mode Range



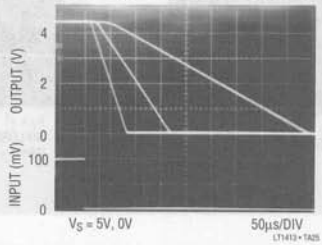




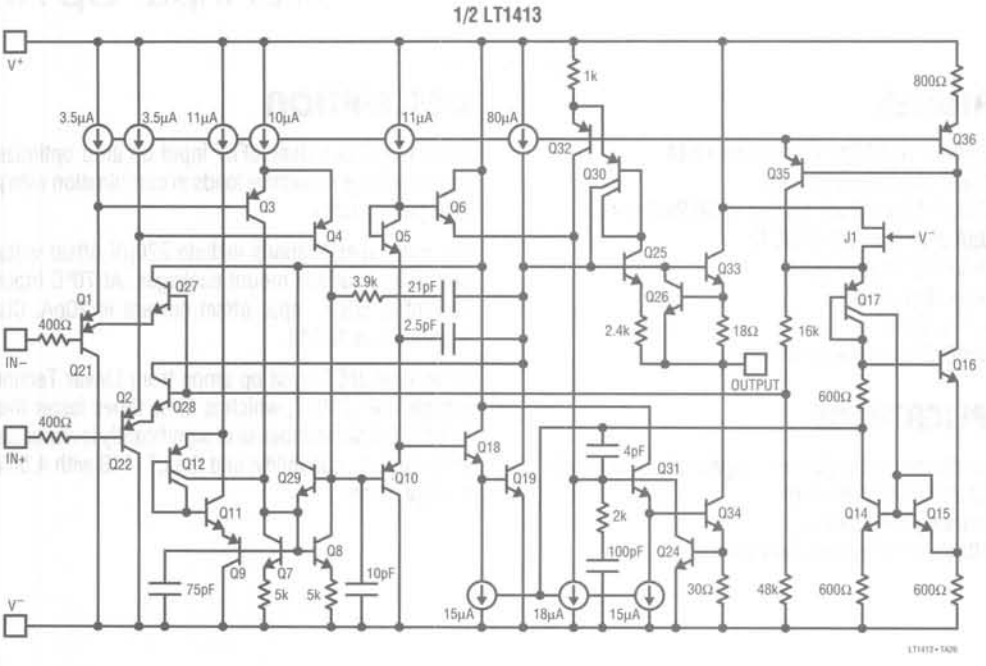
Comparator Rise Response Time 10mV, 5mV, 2mV Overdrives



Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



SIMPLIFIED SCHEMATIC



2

Dual, Precision JFET Input Op Amp

FEATURES

- **Handles 10,000pF Capacitive Load**
- 450μV Max Offset Voltage
- 1200μV Max Offset Voltage in S8 Package
- **50pA Bias Current at 70°C**
- 13nV/√Hz Voltage Noise
- 4V/μs Slew Rate
- 4μV/°C Drift
- 130dB Channel Separation

APPLICATIONS

- Sample-and-Hold (Drives Large Hold Capacitors)
- A/D and D/A Converters
- Photodiode Amplifiers
- Voltage-to-Frequency Converters

DESCRIPTION

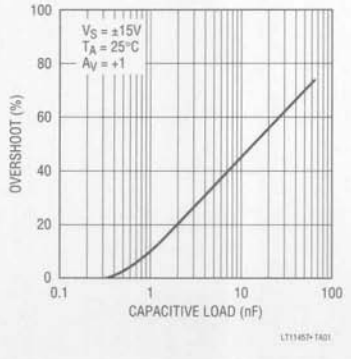
The LT1457 is a dual, JFET input op amp optimized for handling large capacitive loads in combination with precision performance.

Precision specifications include 220μV offset voltage in plastic and surface mount packages. At 70°C input bias current is 50pA, input offset current is 20pA. Channel separation is 130dB.

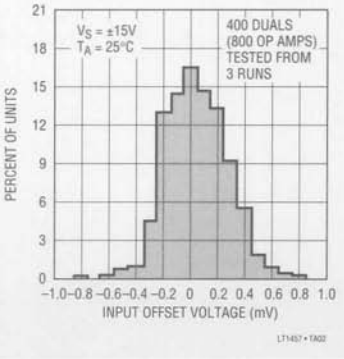
Other dual JFET input op amps from Linear Technology include the LT1057, which is three times faster than the LT1457 but at the expense of significantly lower capacitive load handling capability; and the LT1113 with 4.5nV/√Hz voltage noise.

TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



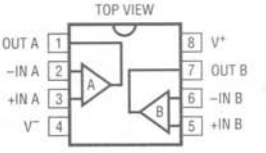
Input Offset Voltage Distribution S8 Package



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... Equal to Supply Voltages
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

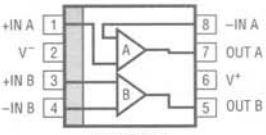
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 115°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1457ACN8
LT1457CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-LEAD DIP PIN LOCATIONS. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE CONFIGURATION.

T_{JMAX} = 130°C, θ_{JA} = 190°C/W

LT1457S8

S8 PART MARKING

1457

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C LT1457S8		150	450		200 220	800 1200	µV µV
I_{OS}	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
I_B	Input Bias Current	Fully Warmed Up		±5	±50		±7	±75	pA
	Input Resistance-Differential -Common-Mode	 V_{CM} = –11V to 8V V_{CM} = 8V to 11V		10^{12} 10^{12} 10^{11}			10^{12} 10^{12} 10^{11}		Ω Ω Ω
	Input Capacitance			4			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.0			2.1		μV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1kHz (Note 2)		26 13	 22		28 14	 24	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 3)		1.5	4		1.8	6	fA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 2k V_O = ±10V, R_L = 1k	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		±10.5	14.3 –11.5		±10.5	14.3 –11.5		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10.5V	86	100		82	98		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	88	103		86	102		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13		±12	±13		V
SR	Slew Rate		2	4		2	4		V/µs

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
GBW	Gain-Bandwidth Product	(Note 5)	1.0	1.7		1.0	1.7		MHz
I_S	Supply Current Per Amplifier			1.8	3.0		1.8	3.0	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm10V$		132			130		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C	●		250	900		330	1500	µV
		LT1457S8	●					400	1900	µV
	Average Temperature Coefficient of Input Offset Voltage (Note 4)		●		3	10		4	16	µV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70°C$			18	150		20	250	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70°C$			±50	±250		±60	±350	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm10V$, $R_L = 2k$	●	70	220		50	200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.4V$	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●	87	102		84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.8		±12	±12.8		V
I_S	Supply Current Per Amplifier		●			3.2			3.2	mA
		$T_A = 70°C$			1.7			1.7		mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C	●		350	1100		400	1800	µV
		LT1457S8	●					500	2300	µV
	Average Temperature Coefficient of Input Offset Voltage		●		3	10		4	16	µV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 85°C$			0.1	0.5		0.1	0.6	nA
I_B	Input Bias Current	Warmed Up, $T_A = 85°C$			±0.2	±0.7		±0.2	±0.9	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm10V$, $R_L = 2k$	●	40	120		30	110		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.4V$	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm17V$	●	86	100		83	98		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.7		±12	±12.6		V
I_S	Supply Current Per Amplifier	$T_A = -40°C$				3.8			3.8	mA
		$T_A = 85°C$			1.7			1.7		mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1457s (200 op amps) typically 120 will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_b)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

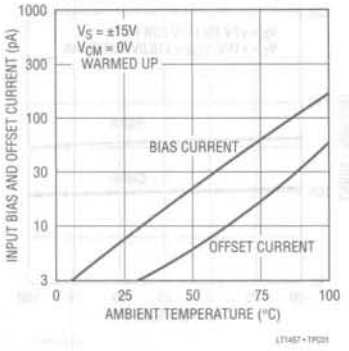
Note 4: This parameter is not 100% tested.

Note 5: Gain-Bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

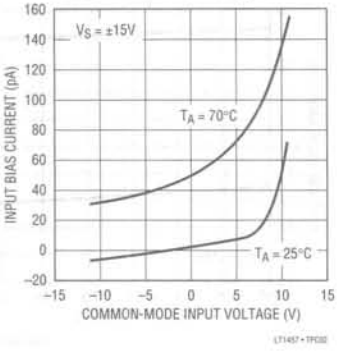
Note 6: The LT1457 is not tested and not quality-assurance-sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

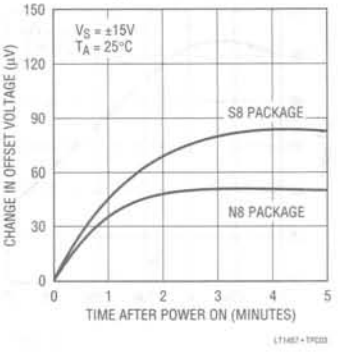
Input Bias and Offset Current vs Temperature



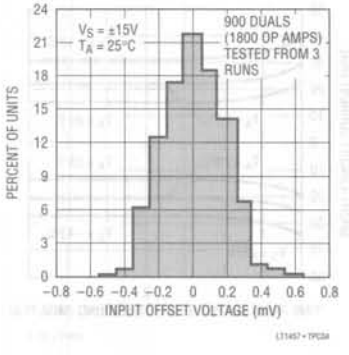
Input Bias Current Over the Common-Mode Range



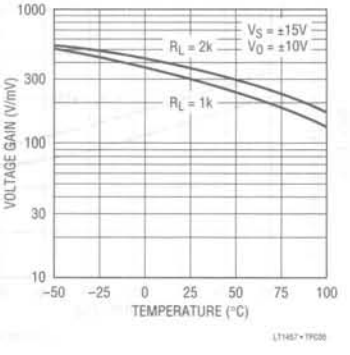
Warm-Up Drift



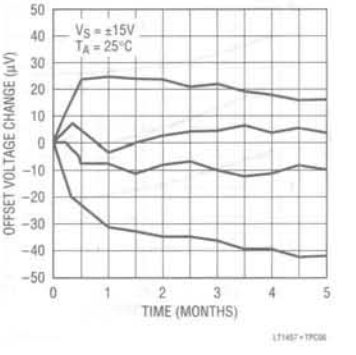
Input Offset Voltage Distribution N8 Package



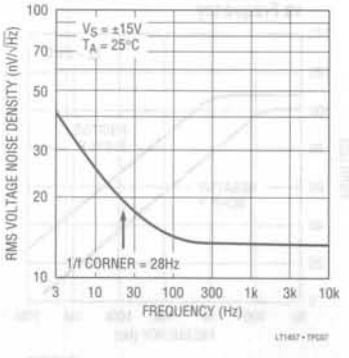
Voltage Gain vs Temperature



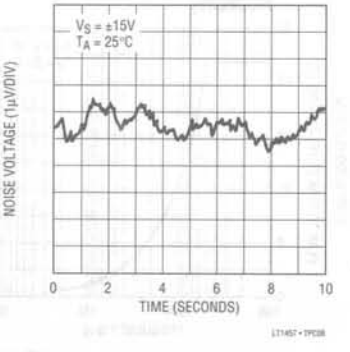
Long Term Drift of Representative Units



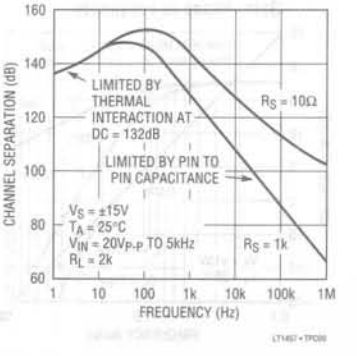
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise



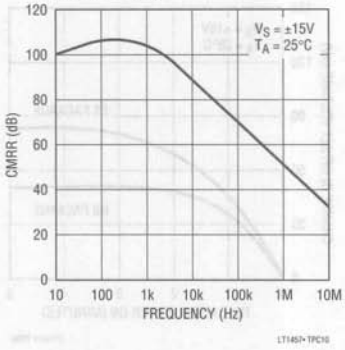
Channel Separation vs Frequency



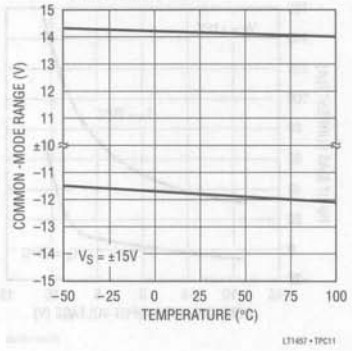
2

TYPICAL PERFORMANCE CHARACTERISTICS

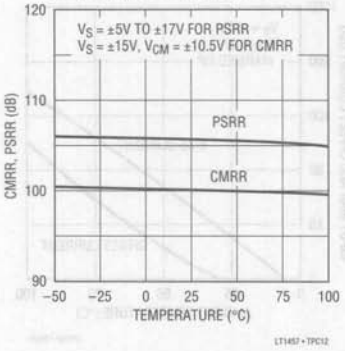
Common-Mode Rejection Ratio vs Frequency



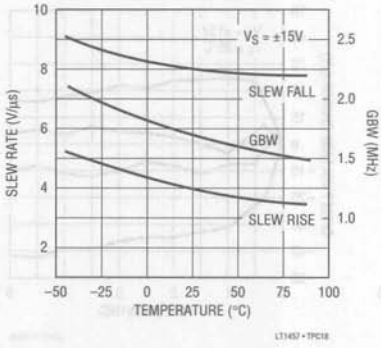
Common-Mode Range vs Temperature



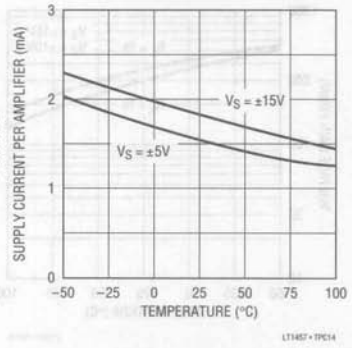
Common-Mode and Power Supply Rejections vs Temperature



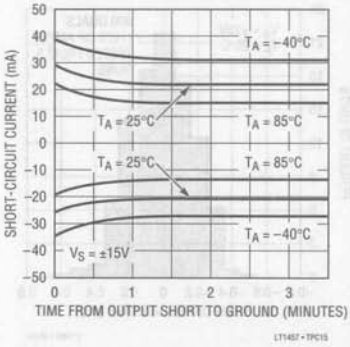
Slew Rate, Gain-Bandwidth Product vs Temperature



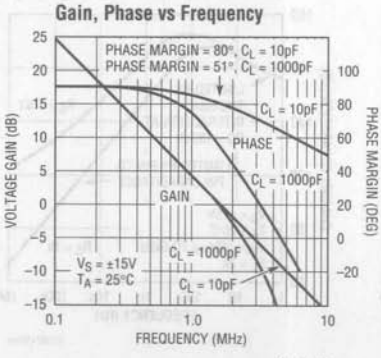
Supply Current vs Temperature



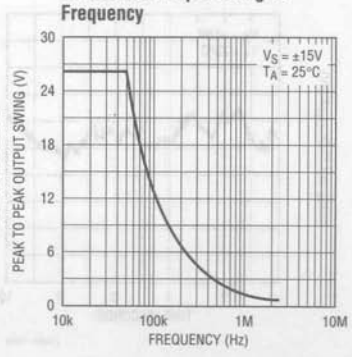
Short-Circuit Current vs Time (One Output Shorted to Ground)



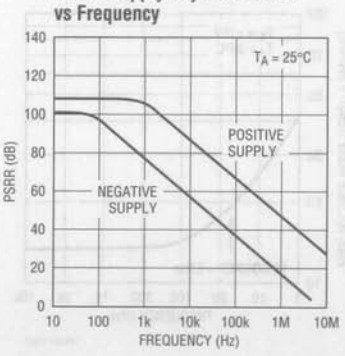
Gain, Phase vs Frequency



Undistorted Output Swing vs Frequency

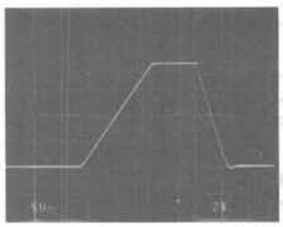


Power Supply Rejection Ratio vs Frequency

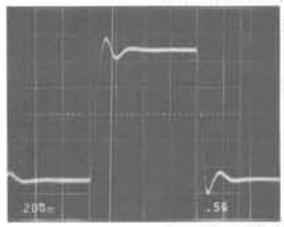


TYPICAL PERFORMANCE CHARACTERISTICS

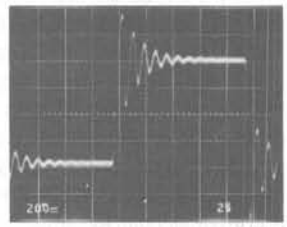
Large-Signal Response
$A_V = 1$, $C_L = 100pF$



Small-Signal Response
$A_V = 1$, $C_L = 1000pF$



Small-Signal Response
$A_V = 1$, $C_L = 10,000pF$

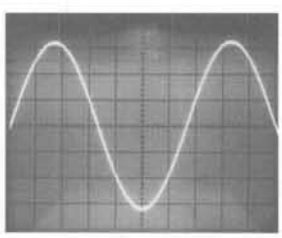


APPLICATIONS INFORMATION

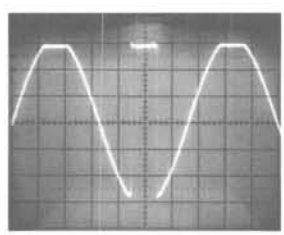
Phase Reversal Protection

Most industry standard JFET input single, dual, and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, and TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below –12V with ±15V supplies). The photos show a ±16V sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1457 (C).

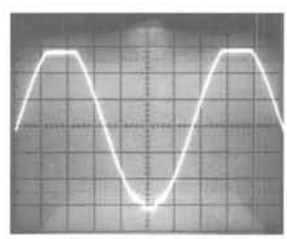
The phase reversal of photo (B) can cause lock-up in servo systems. The LT1457 does not phase-reverse due to a unique phase reversal protection circuit.



(A) ±16V Sine Wave Input



(B) LF412A Output



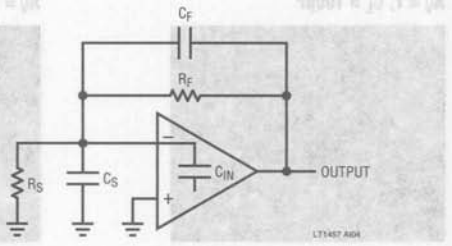
(C) LT1457 Output

All Photos 5V/Div Vertical Scale, 50μs/Div Horizontal Scale

APPLICATIONS INFORMATION

High Speed Operation

When the feedback around the op amp is resisitive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation on high speed amplifiers. Because the LT1457's phase margin is very high, this problem is minimal. However, a small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.



SECTION 2—AMPLIFIERS

HIGH SPEED AMPLIFIERS

LT1122, Fast Settling, JFET Input Operational Amplifier 2-84
LT1187, Low Power Video Difference Amplifier 2-92
LT1189, Low Power Video Difference Amplifier 2-104
LT1195, Low Power, High Speed Operational Amplifier 2-116
LT1201/LT1202, Dual and Quad 1mA, 12MHz, 50V/μs Op Amps 2-127
LT1206, 250mA/60MHz Current Feedback Amplifier 2-137
LT1208/LT1209, Dual and Quad 45MHz, 400V/μs Op Amps 2-150
LT1211/LT1212, 14MHz, 7V/μs, Single Supply Dual and Quad Precision Op Amps 2-160
LT1213/LT1214, 28MHz, 12V/μs, Single Supply Dual and Quad Precision Op Amps 2-176
LT1215/LT1216, 23MHz, 50V/μs, Single Supply Dual and Quad Precision Op Amps 2-192
LT1227, 140MHz Video Current Feedback Amplifier 2-208
LT1251/LT1256, 40MHz Video Fader and DC Gain Controlled Amplifier 2-219
LT1252, Low Cost Video Amplifier 2-242
LT1253/LT1254, Low Cost Dual and Quad Video Amplifiers 2-249
LT1259/LT1260, Low Cost Dual and Triple 130MHz Current Feedback Amplifiers with Shutdown 2-256
LT1354, 12MHz, 400V/μs Op Amp 2-267
LT1355/LT1356, Dual and Quad 12MHz, 400V/μs Op Amps 2-278
LT1357, 25MHz, 600V/μs Op Amp 2-289
LT1358/LT1359, Dual and Quad 25MHz, 600V/μs Op Amps 2-300
LT1360, 50MHz, 800V/μs Op Amp 2-311
LT1361/LT1362, Dual and Quad 50MHz, 800V/μs Op Amps 2-322
LT1363, 70MHz, 1000V/μs Op Amp 2-333
LT1364/LT1365, Dual and Quad 70MHz, 1000V/μs Op Amps 2-344

Fast Settling, JFET Input Operational Amplifier

FEATURES

- 100% Tested Settling Time to 1mV at Sum Node, 10V Step Tested with Fixed Feedback Capacitor — 340ns Typ, 540ns Max
- Slew Rate — 60V/µs Min
- Gain Bandwidth Product — 14MHz
- Power Bandwidth (20Vp-p) — 1.2 MHz
- Unity Gain Stable; Phase Margin — 60°
- Input Offset Voltage — 600µV Max
- Input Bias Current — 25°C: 75pA Max; 70°C: 600pA Max
- Input Offset Current — 25°C: 40pA Max; 70°C: 150pA Max
- Low Distortion

APPLICATIONS

- Fast 12-Bit D/A Output Amplifiers
- High Speed Buffers
- Fast Sample and Hold Amplifiers
- High Speed Integrators
- Voltage to Frequency Converters
- Active Filters
- Log Amplifiers
- Peak Detectors

DESCRIPTION

The LT1122 JFET input operational amplifier combines high speed and precision performance.

A unique poly-gate JFET process minimizes gate series resistance and gate-to-drain capacitance, facilitating wide bandwidth performance, without degrading JFET transistor matching.

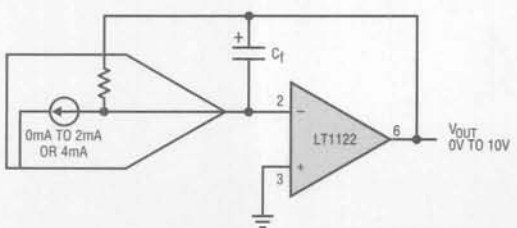
It slews at 80V/µs and settles in 340ns. The LT1122 is internally compensated to be unity gain stable, yet it has a bandwidth of 14MHz at a supply current of only 7mA. Its speed makes the LT1122 an ideal choice for fast settling 12-bit data conversion and acquisition systems.

The LT1122 offset voltage of 120µV, and voltage gain of 500,000 also support the 12-bit accurate applications.

The input bias current of 10pA and offset current of 4pA combined with its speed allow the LT1122 to be used in such applications as high speed sample and hold amplifiers, peak detectors, and integrators.

TYPICAL APPLICATION

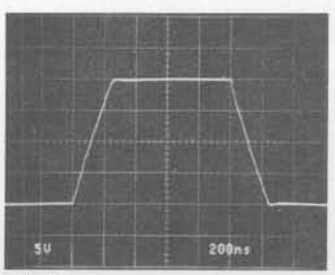
12-Bit Voltage Output D/A Converter



12-BIT CURRENT OUTPUT D/A CONVERTER
C_f = 5pF TO 17pF
(DEPENDING ON D/A CONVERTER USED)

LT1122•TA01

Large-Signal Response



200ns/DIV
AV = −1

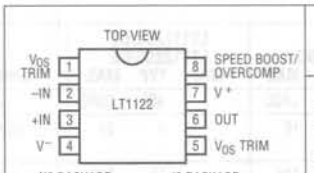
1122 TA07

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Operating Temperature Range
LT1122AM/BM/CM/DM ..... –55°C to 125°C
LT1122AC/BC/CC/DC/CS/DS ..... –40°C to 85°C
Storage Temperature Range
All Devices ..... –65°C to 150°C

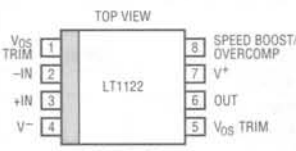
PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PLASTIC DIP
J8 PACKAGE 8-LEAD HERMETIC DIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J8)

ORDER PART NUMBER	
LT1122AMJ8	LT1122CCJ8
LT1122BMJ8	LT1122DCJ8
LT1122CMJ8	LT1122ACN8
LT1122DMJ8	LT1122BCN8
LT1122ACJ8	LT1122CCN8
LT1122BCJ8	LT1122DCN8



S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1122CS8
LT1122DS8
PART MARKING
1122C
1122D

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM LT1122AC/BC MIN	TYP	MAX	LT1122CM/DM LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			120	600		130	900	µV
I_{OS}	Input Offset Current			4	40		5	50	pA
I_B	Input Bias Current			10	75		12	100	pA
	Input Resistance								
	Differential			10^{12}			10^{12}		Ω
	Common Mode	V_{CM} = –10V to +8V		10^{12}			10^{12}		Ω
		V_{CM} = +8V to +11V		10^{11}			10^{11}		Ω
	Input Capacitance			4			4		pF
S_R	Slew Rate	A_V = –1	60	80		50	75		V/µs
	Settling Time (Note 2)	+10V to 0V, –10V to 0V							
		100% Tested: A and C Grades to 1mV at Sum Node		340	540		350	590	ns
		B and D Grades to 1mV at Sum Node		350			360		ns
		All Grades to 0.5mV at Sum Node		450			470		ns
GBW	Gain Bandwidth Product			14			13		MHz
	Power Bandwidth	V_{OUT} = 20Vp-p		1.2			1.1		MHz
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	180	500		150	450		V/mV
		V_{OUT} = ±10V, R_L = 600Ω	130	250		110	220		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	83	99		80	98		dB
	Input Voltage Range	(Note 3)	±10.5	±11		±10.5	±11		V
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V	86	103		82	101		dB
	Input Noise Voltage	0.1Hz to 10Hz		3.0			3.3		μV_{P-P}
	Input Noise Voltage Density	f_O = 100Hz		25			27		$nV/\sqrt{Hz}$
		f_O = 10kHz		14			15		$nV/\sqrt{Hz}$
	Input Noise Current Density	f_O = 100Hz, f_O = 10kHz		2			2		$fA/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM LT1122AC/BC MIN	TYP	MAX	LT1122CM/DM LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	±12	±12.5		±12	±12.5		V
		$R_L = 600\Omega$	±11.5	±12		±11.5	±12		V
I_S	Supply Current			7.5	10		7.8	11	mA
	Minimum Supply voltage	(Note 4)		±5			±5		V
	Offset Adjustment Range	$R_{POT} \geq 10k$, Wiper to V+		±4	±10		±4	±10	mV

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1122AC/BC MIN	TYP	MAX	LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		350	1400		400	2000	µV
	Average Temperature Coefficient of Input Offset Voltage		●		5	18		6	25	µV/°C
I_{OS}	Input Offset Current		●		12	150		15	200	pA
I_B	Input Bias Current		●		80	600		90	800	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	120	380		100	340		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	82	98		78	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	84	101		80	99		dB
	Input Voltage Range		●	±10	±10.8		±10	±10.8		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.5	±12.4		±11.5	±12.4		V
S_R	Slew Rate	$A_V = -1$	●	50	70		40	65		V/µs

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1122AM/BM MIN	TYP	MAX	LT1122CM/DM MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		650	2400		800	3400	µV
	Average Temperature Coefficient of Input Offset Voltage		●		6	18		7	25	µV/°C
I_{OS}	Input Offset Current		●		0.5	6		0.6	9	nA
I_B	Input Bias Current		●		6	25		7	35	nA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	70	230		60	200		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	80	97		76	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	83	100		78	98		dB
	Input Voltage Range		●	±10	±10.5		±10	±10.5		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.3	±12.1		±11.3	±12.1		V
S_R	Slew Rate	$A_V = -1$	●	45	60		35	55		V/µs

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: The LT1122 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed up chip temperature can be 10°C to 50°C higher than the ambient temperature.

Note 2: Settling time is 100% tested for A and C grades using the settling time test circuit shown. This test is not included in quality assurance sample testing.

Note 3: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 4mV (A, B grades), to 5.7mV (C, D grades).

Note 4: Minimum supply voltage is tested by measuring offset voltage to 7mV maximum at ±5V supplies.

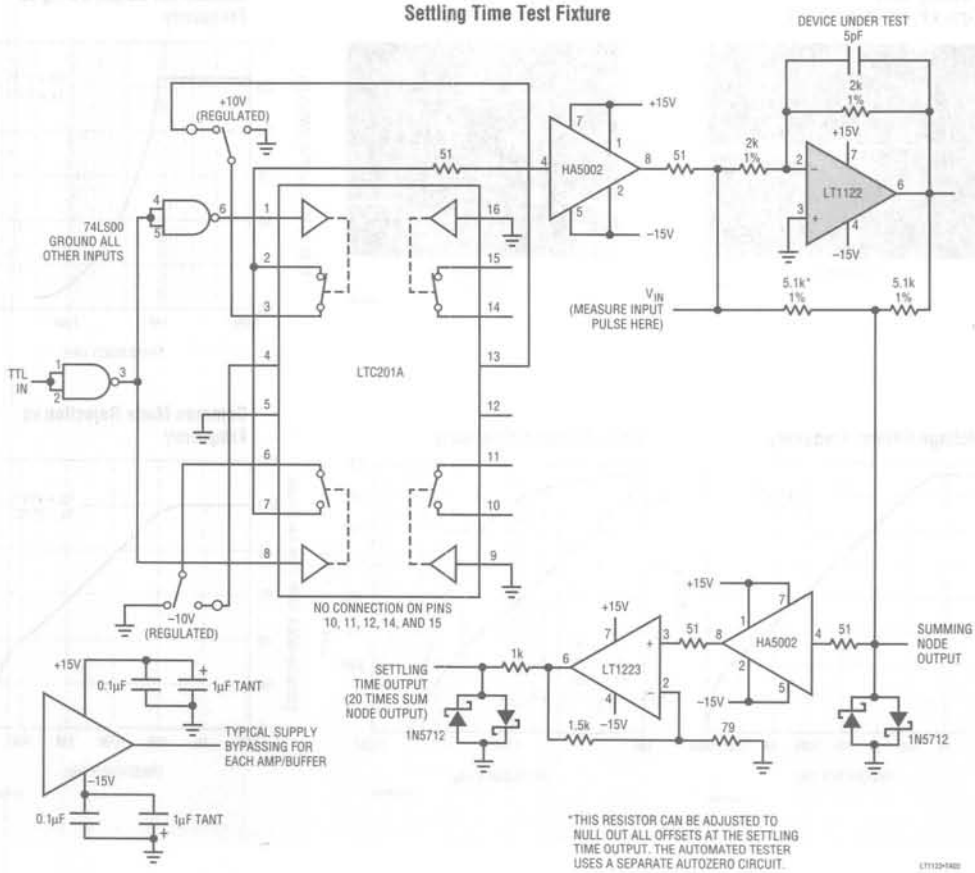
Note 5: The LT1122 is not tested and not quality-assurance-sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 5)

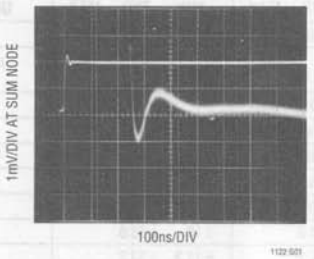
SYMBOL	PARAMETER	CONDITIONS		LT1122AC/BC MIN	LT1122AC/BC TYP	LT1122AC/BC MAX	LT1122CC/DC LT1122CS/DS MIN	LT1122CC/DC LT1122CS/DS TYP	LT1122CC/DC LT1122CS/DS MAX	UNITS
V_{OS}	Input Offset Voltage		●		450	1900		500	2700	µV
	Average Temperature Coefficient of Input Offset Voltage		●		6	20		7	28	µV/°C
I_{OS}	Input Offset Current		●		30	600		40	900	pA
I_B	Input Bias Current		●		230	2000		260	2700	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	●	95	340		80	300		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	80	98		76	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	83	100		78	98		dB
	Input Voltage Range		●	±10	±10.6		±10	±10.6		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.3	±12.2		±11.3	±12.2		V
S_R	Slew Rate	$A_V = -1$	●	45	65		35	60		V/µs

Settling Time Test Fixture

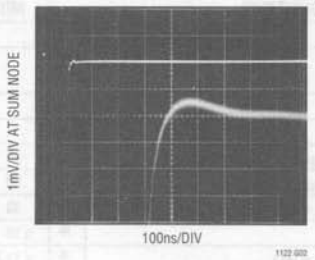


TYPICAL PERFORMANCE CHARACTERISTICS

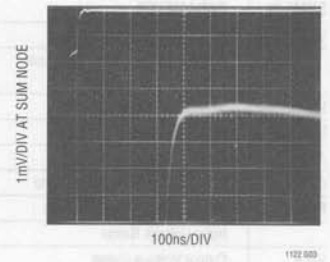
Settling Time (Input From –10V to 0V)



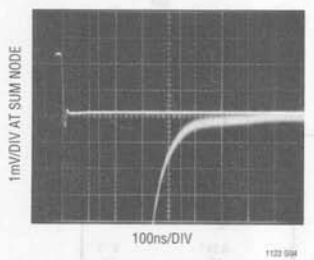
Settling Time (Input From +10V to 0V)



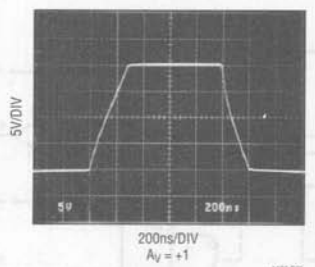
Settling Time (Input From 0V to +10V)



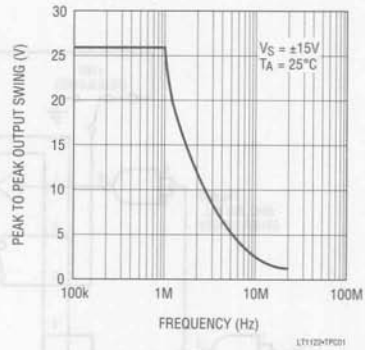
Settling Time (Input From 0V to –10V)



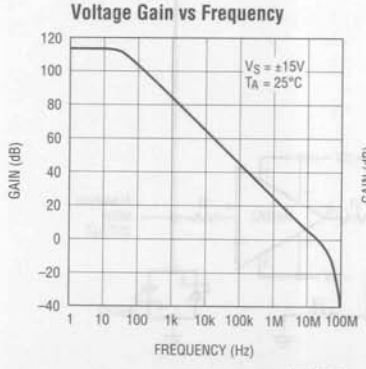
Large Signal Response



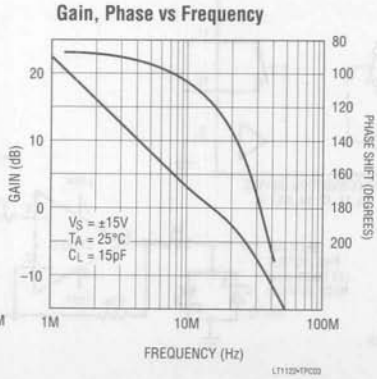
Undistorted Output Swing vs Frequency



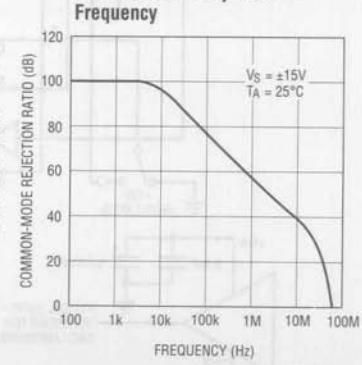
Voltage Gain vs Frequency



Gain, Phase vs Frequency

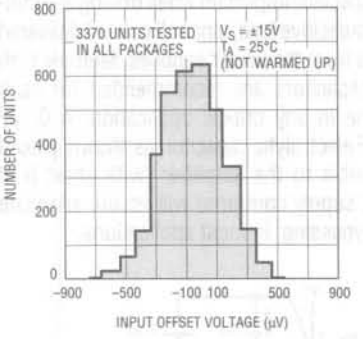


Common Mode Rejection vs Frequency

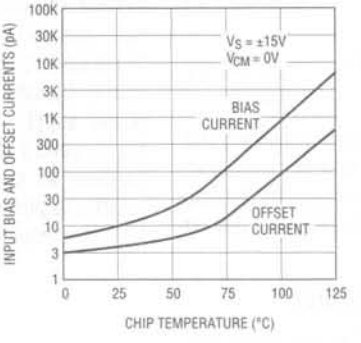


TYPICAL PERFORMANCE CHARACTERISTICS

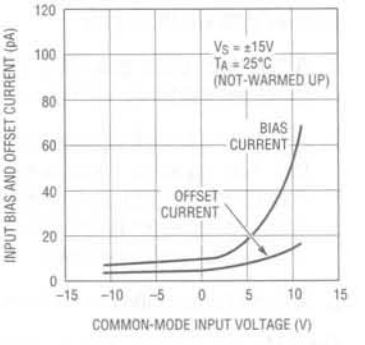
Distribution of Input Offset Voltage



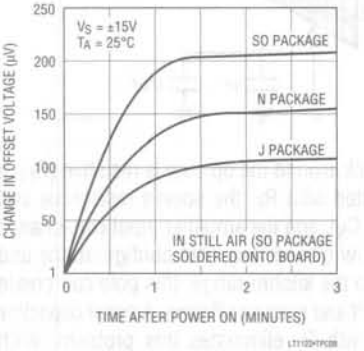
Input Bias and Offset Currents Over Temperature



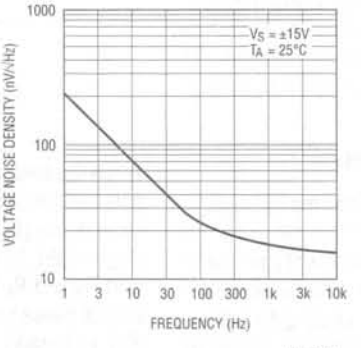
Bias and Offset Currents Over The Common-Mode Range



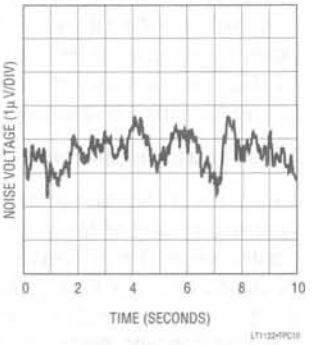
Warm-up Drift



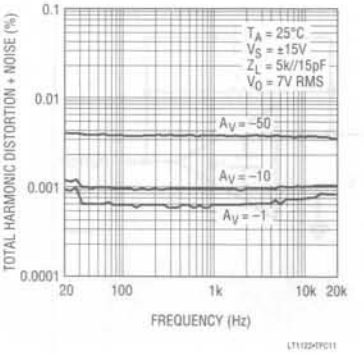
Noise Spectrum



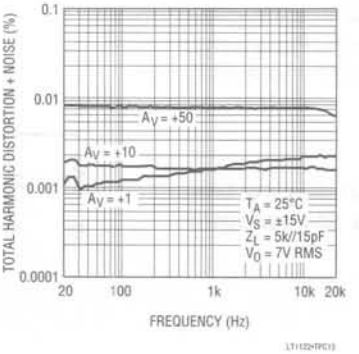
0.1Hz to 10Hz Noise



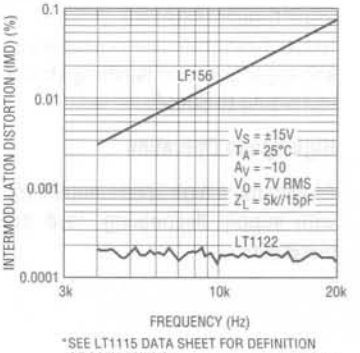
Total Harmonic Distortion + Noise vs Frequency Inverting Gain



Total Harmonic Distortion + Noise vs Frequency Non-Inverting Gain



Intermodulation Distortion (CCIF Method) vs Frequency LT1122 and LF156*



*SEE LT1115 DATA SHEET FOR DEFINITION OF CCIF TESTING

2

APPLICATIONS INFORMATION

Settling Time Measurements

Settling time test circuits shown on some competitive devices' data sheets require:

1. A "flat top" pulse generator. Unfortunately, flat top pulse generators are not commercially available.
2. A variable feedback capacitor around the device under test. This capacitor varies over a four to one range. Presumably, as each op amp is measured for settling time, the capacitor is fine tuned to optimize settling time for that particular device.
3. A small inductor load to optimize settling.

The LT1122's settling time is 100% tested in the test circuit shown. No "flat top" pulse generator is required. The test circuit can be readily constructed, using commercially available ICs. Of course, standard high frequency board construction techniques should be followed. All LT1122s are measured with a constant feedback capacitor. No fine tuning is required.

Speed Boost/Overcompensation Terminal

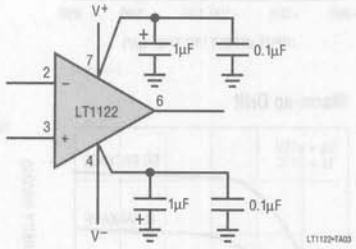
Pin 8 of the LT1122 can be used to change the input stage operating current of the device. Shorting pin 8 to the positive supply (Pin 7) increases slew rate and bandwidth by about 25%, but at the expense of a reduction in phase margin by approximately 18 degrees. Unity gain capacitive load handling decreases from typically 500pF to 100pF.

Conversely, connecting a 15k resistor from pin 8 to ground pulls 1mA out of pin 8 (with $V^+ = 15V$). This reduces slew rate and bandwidth by 25%. Phase margin and capacitive load handling improve; the latter typically increasing to 800pF.

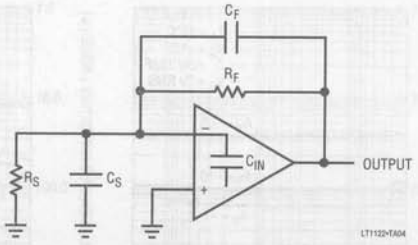
High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

The power supply connections to the LT1122 must maintain a low impedance to ground over a bandwidth of 20MHz. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1µF ceramic and a 1µF electrolytic capacitor, as shown, placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications.

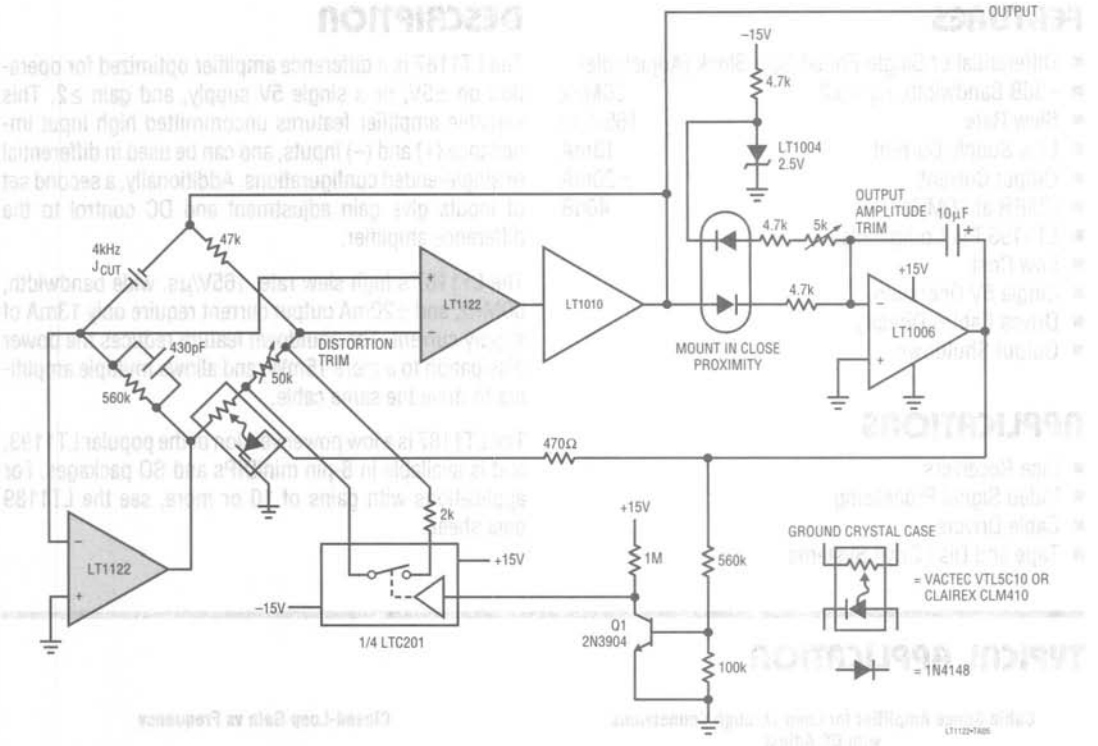


When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S (C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.

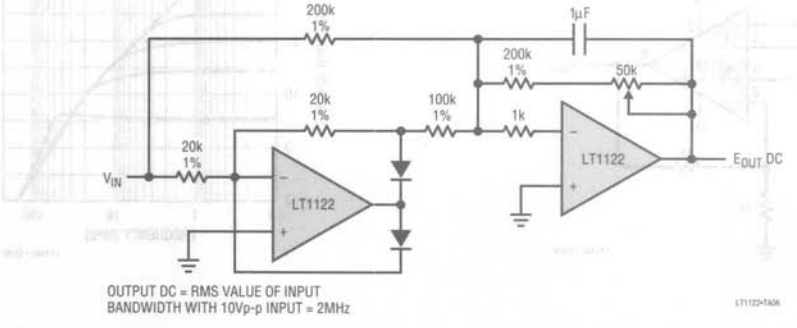


TYPICAL APPLICATIONS

Quartz Stabilized Oscillator With 9ppm Distortion



Wide-Band, Filtered, Full Wave Rectifier



LINEAR TECHNOLOGY

LT1187

Low Power Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- –3dB Bandwidth, $A_V = \pm 2$ 50MHz
- Slew Rate 165V/µs
- Low Supply Current 13mA
- Output Current ±20mA
- CMRR at 10MHz 40dB
- LT1193 Pin Compatible
- Low Cost
- Single 5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Tape and Disc Drive Systems

DESCRIPTION

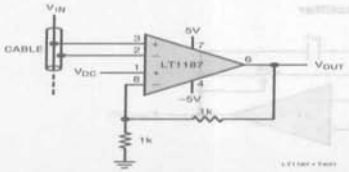
The LT1187 is a difference amplifier optimized for operation on ±5V, or a single 5V supply, and gain ≥2. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the difference amplifier.

The LT1187's high slew rate, 165V/µs, wide bandwidth, 50MHz, and ±20mA output current require only 13mA of supply current. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

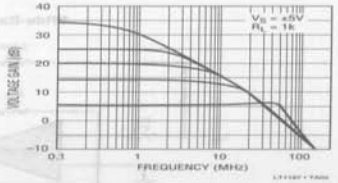
The LT1187 is a low power version of the popular LT1193, and is available in 8-pin miniDIPs and SO packages. For applications with gains of 10 or more, see the LT1189 data sheet.

TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



Closed-Loop Gain vs Frequency

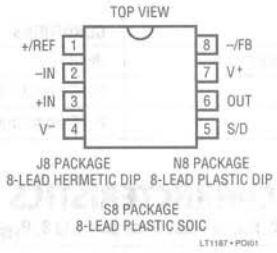


LINEAR TECHNOLOGY

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1187M ..... −55°C to 150°C
LT1187C ..... 0°C to 70°C
Junction Temperature (Note 2)
Plastic Package (CN8,CS8) ..... 150°C
Ceramic Package (CJ8,MJ8) ..... 175°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1187CJ8 LT1187CN8 LT1187CS8 LT1187MJ8
S8 PART MARKING
1187

Consult factory for Industrial grade parts.

2

±5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, $R_L = R_{FB1} + R_{FB2}$ = 1k, $C_L \leq$ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	10	mV
		SOIC Package		2.0	11	mV
I_{OS}	Input Offset Current	Either Input		0.2	1.0	µA
I_B	Input Bias Current	Either Input		±0.5	±2.0	µA
e_n	Input Noise Voltage	f_O = 10kHz		65		nV/√Hz
i_n	Input Noise Current	f_O = 10kHz		1.5		pA/√Hz
R_{IN}	Input Resistance	Differential		100		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 5)		±380		mV
	Input Voltage Range		−2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −2.5V to 3.5V	70	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	70	85		dB
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k, A_V = 50	±3.8	±4.0		V
		V_S = ±8V, R_L = 1k, A_V = 50	±6.7	±7.0		
		V_S = ±8V, R_L = 300Ω, A_V = 50, (Note 3)	±6.4	±6.8		
G_E	Gain Error	V_O = ±1V, A_V = 10, R_L = 1k		0.2	1.0	%
SR	Slew Rate	(Note 6, 10)	100	165		V/µs
FPBW	Full Power Bandwidth	V_O = $1V_{P-P}$, (Note 7)		53		MHz
BW	Small Signal Bandwidth	A_V = 10		5.7		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = ±1.5V, 20% to 80% (Note 10)	150	230	325	ns
t_{PD}	Propagation Delay	R_L= 1k, V_O = ±125mV, 50% to 50%		26		ns
	Overshoot	V_O = ±50mV		0		%
t_S	Settling Time	3V Step, 0.1%, (Note 8)		100		ns
Diff A_V	Differential Gain	R_L = 1k, A_V = 4, (Note 9)		0.6		%
Diff Ph	Differential Phase	R_L = 1k, A_V = 4, (Note 9)		0.8		DEG_{P-P}
I_S	Supply Current			13	16	mA
	Shutdown Supply Current	Pin 5 at V^-		0.8	1.5	mA

±5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M/C MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA
t_{ON}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		500		ns
t_{OFF}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		600		ns

5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1187M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)			2.0	10	mV
		SOIC Package			2.0	12	mV
I_{OS}	Input Offset Current	Either Input			0.2	1.0	µA
I_B	Input Bias Current	Either Input			±0.5	±2.0	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to $3.5V$		70	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground (Note 3)	V_{OUT} High	3.6	4.0		V
			V_{OUT} Low		0.15	0.4	
SR	Slew Rate	$V_O = 1.5V$ to $3.5V$			130		V/µs
BW	Small-Signal Bandwidth	$A_V = 10$			5.3		MHz
I_S	Supply Current				12	15	mA
	Shutdown Supply Current	Pin 5 at V^-			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

±5V ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq 125°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	15	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			8.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		−2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to $3.5V$	70	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm8V$	60	85		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.8		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		0.2	1.2	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

±5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187C MIN	LT1187C TYP	LT1187C MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	12	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			9.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	70	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	65	85		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.8		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		0.2	1.0	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, (Note 3)

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1187C MIN	LT1187C TYP	LT1187C MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4) SOIC Package			2.0 2.0	12.0 13.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift				9.0		µV/°C
I_{OS}	Input Offset Current	Either Input			0.2	1.5	µA
I_B	Input Bias Current	Either Input			±0.5	±3.5	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		70	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground	V_{OUT} High	3.5	4.0		V
		(Note 3)	V_{OUT} Low		0.15	0.4	
I_S	Supply Current				12	16	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted continuously.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1187MJ8,LT1187CJ8: $T_J = T_A + (P_D \times 100°C/W)$
LT1187CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1187CS8: $T_J = T_A + (P_D \times 150°C/W)$

Note 3: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 300\Omega$ is specified, then an additional 430Ω is added to the output such that ($R_{FB1} + R_{FB2}$) in parallel with 430Ω is $R_L = 300\Omega$.

Note 4: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 5: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 6: Slew rate is measured between ±0.5V on the output, with a V_{IN} step of ±0.75V, $A_V = 3$ and $R_L = 1k$.

Note 7: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

Note 8: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

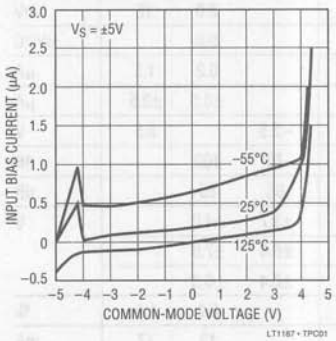
Note 9: NTSC (3.58MHz).

Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J8 and N8 suffix) and are sample tested on every lot of the SO packaged parts (S8 suffix).

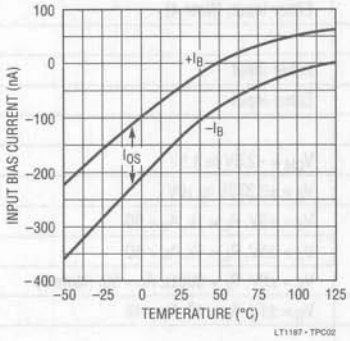
Note 11: See Application section for shutdown at elevated temperatures. Do not operate shutdown above $T_J > 125°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

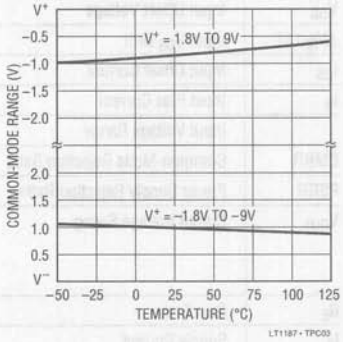
Input Bias Current vs Common-Mode Voltage



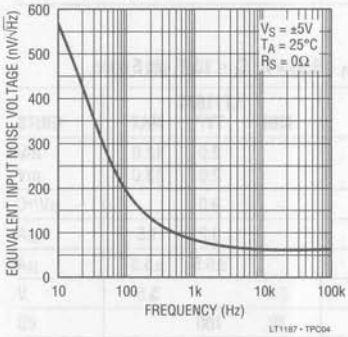
Input Bias Current vs Temperature



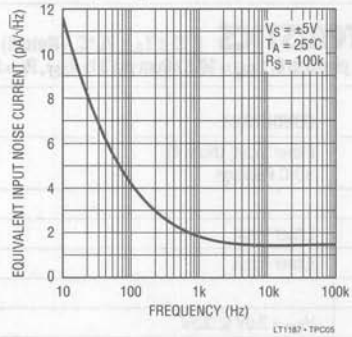
Common-Mode Voltage vs Temperature



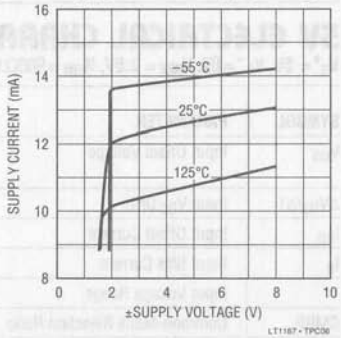
Equivalent Input Noise Voltage vs Frequency



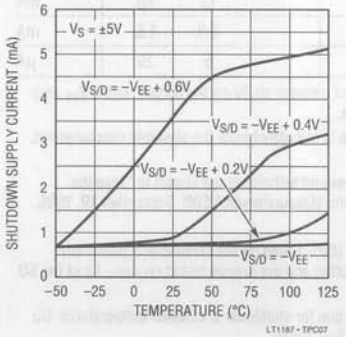
Equivalent Input Noise Current vs Frequency



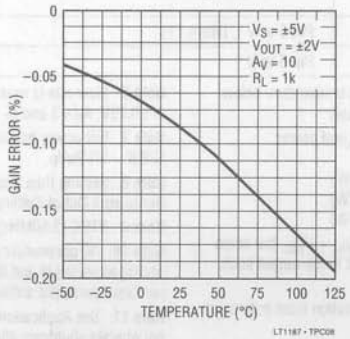
Supply Current vs Supply Voltage



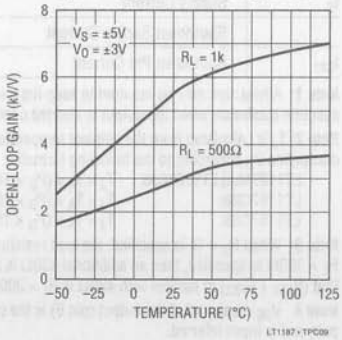
Shutdown Supply Current vs Temperature



Gain Error vs Temperature

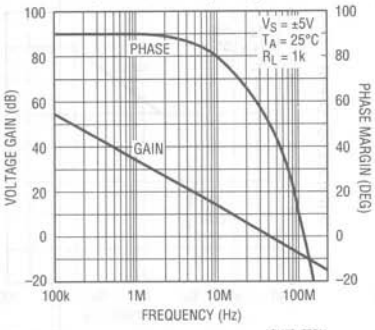


Open-Loop Gain vs Temperature



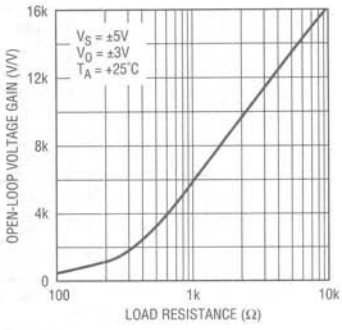
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency

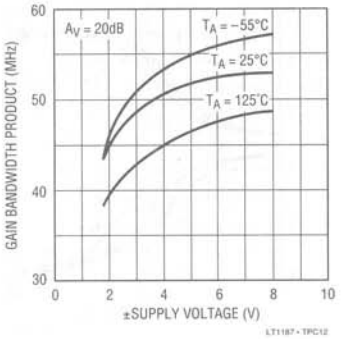


LT1187 • TPC11

Open-Loop Voltage Gain vs Load Resistance

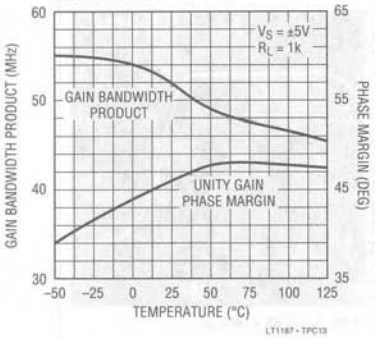


Gain Bandwidth Product vs Supply Voltage



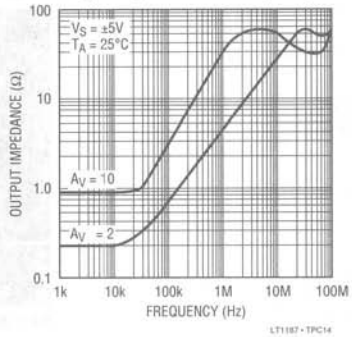
LT1187 • TPC12

Gain Bandwidth Product and Unity Gain Phase Margin vs Temperature



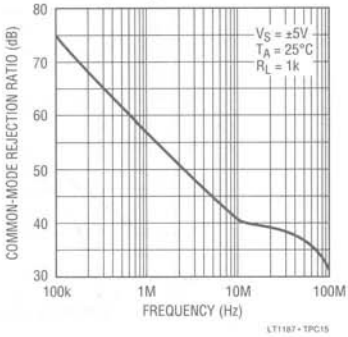
LT1187 • TPC13

Output Impedance vs Frequency



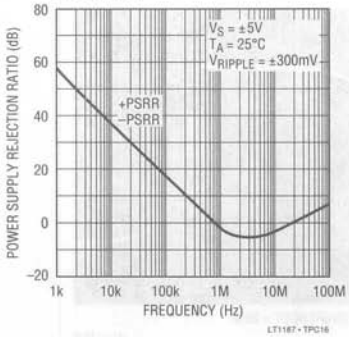
LT1187 • TPC14

Common-Mode Rejection Ratio vs Frequency



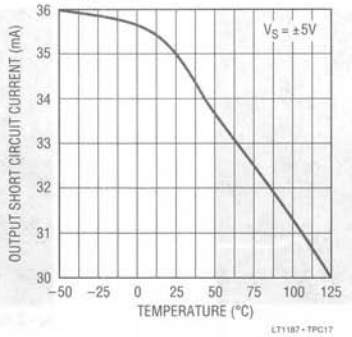
LT1187 • TPC15

Power Supply Rejection Ratio vs Frequency



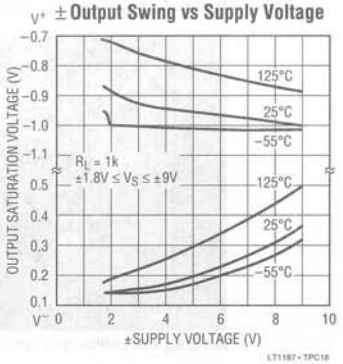
LT1187 • TPC16

Output Short Circuit Current vs Temperature



LT1187 • TPC17

± Output Swing vs Supply Voltage

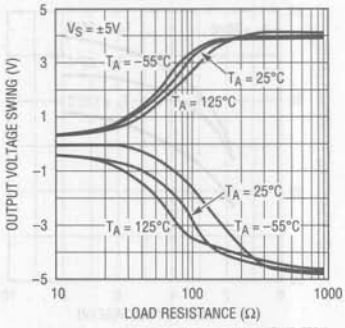


LT1187 • TPC18

2

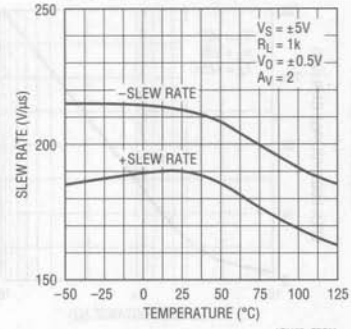
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



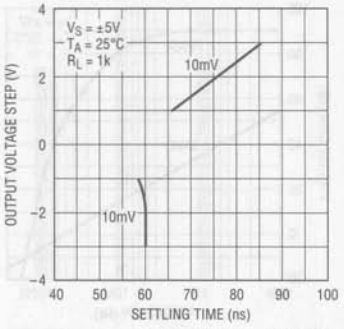
LT1187 • TPC19

Slew Rate vs Temperature



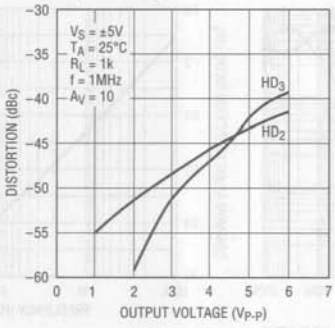
LT1187 • TPC20

Output Voltage Step vs Settling Time, A_V = 2



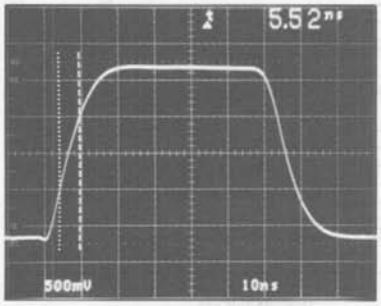
LT1187 • TPC21

Harmonic Distortion vs Output Voltage



LT1187 • TPC22

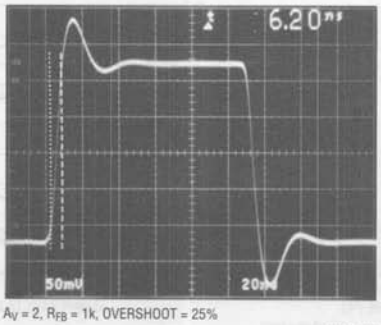
Large-Signal Transient Response



INPUT IN LIMITING, A_V = 3, SR = 180V/µs

LT1187 • TPC23

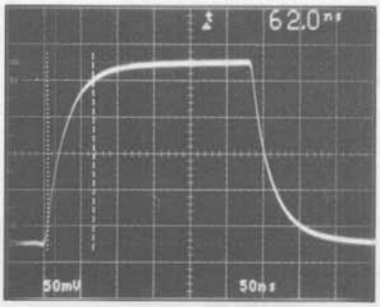
Small-Signal Transient Response



A_V = 2, R_{FB} = 1k, OVERSHOOT = 25%

LT1187 • TPC24

Small-Signal Transient Response



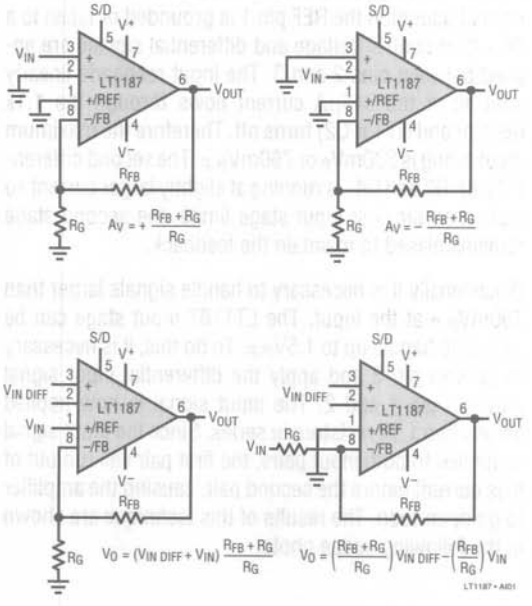
A_V = 2, R_{FB} = 1k, OVERSHOOT = 25%

LT1187 • TPC25

APPLICATIONS INFORMATION

The primary use of the LT1187 is in converting high speed differential signals to a single-ended output. The LT1187 video difference amplifier has two uncommitted high input impedance (+) and (–) inputs. The amplifier has another set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust and DC control to the difference amplifier. The voltage gain of the LT1187 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 2 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/REF (pin 1). The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±0.38V.



Power Supply Bypassing

The LT1187 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. In applications requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended.

Calculating the Output Offset Voltage

Both input stages contribute to the output offset voltage at pin 6. The feedback correction forces balance in the input stages by introducing an Input V_{OS} at pin 8. The complete expression for the output offset voltage is:

$$V_{OUT} = (V_{OS} + I_{OS}(R_S) + I_B(R_{REF})) \times (R_{FB}+R_G)/R_G + I_B(R_{FB})$$

R_S represents the input source resistance, typically 75Ω, and R_{REF} represents the finite source impedance from the DC reference voltage, for V_{REF} grounded, $R_{REF} = 0\Omega$. The I_{OS} is normally a small contributor and the expression simplifies to:

$$V_{OUT} = V_{OS}(R_{FB}+R_G)/R_G + I_B(R_{FB})$$

If R_{FB} is limited to 1k the last term of the equation contributes only 2mV, since I_B is less than 2µA.

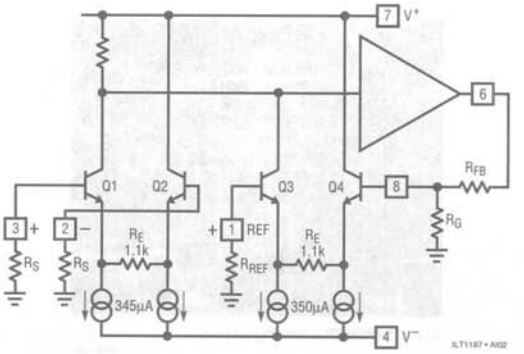


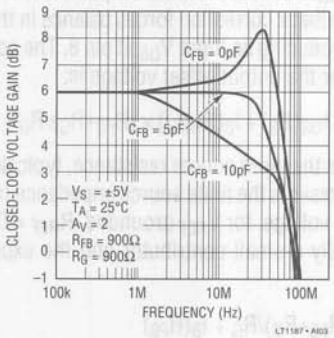
Figure 1. Simplified Input Stage Schematic

APPLICATIONS INFORMATION

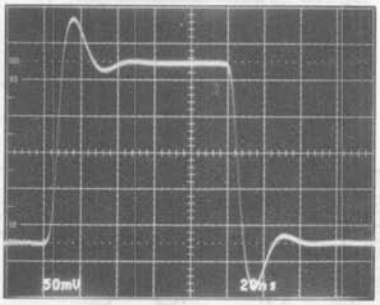
Operating with Low Closed-Loop Gains

The LT1187 has been optimized for closed-loop gains of 2 or greater. For a closed-loop gain of 2 the response peaks about 2dB. Peaking can be eliminated by placing a capacitor across the feedback resistor, (feedback zero). This peaking shows up as time domain overshoot of about 25%.

Closed-Loop Voltage Gain vs Frequency



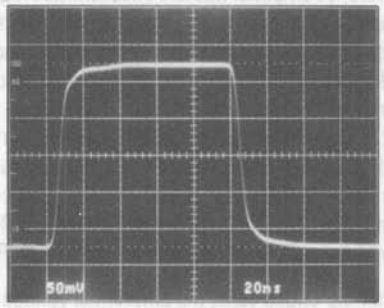
Small-Signal Transient Response



A_V = 2, OVERSHOOT = 25%, $R_{FB} = R_G$ = 1k

LT1187 • A04

Small-Signal Transient Response



A_V = 2, WITH 8pF FEEDBACK CAPACITOR

LT1187 • A05

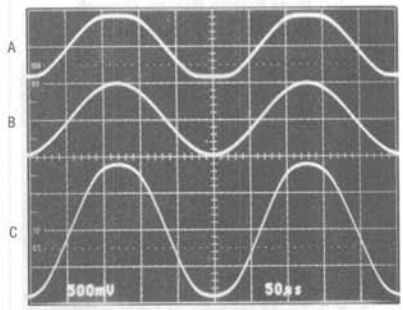
Extending the Input Range

Figure 1 shows a simplified schematic of the LT1187. In normal operation the REF pin 1 is grounded or taken to a DC offset control voltage and differential signals are applied between pins 2 and 3. The input responds linearly until all of the 345µA current flows through the 1.1k resistor and Q1 (or Q2) turns off. Therefore the maximum input swing is 380mV$_P$ or 760mV$_{P-P}$. The second differential pair, Q3 and Q4, is running at slightly larger current so that when the first input stage limits, the second stage remains biased to maintain the feedback.

Occasionally it is necessary to handle signals larger than 760mV$_{P-P}$ at the input. The LT1187 input stage can be tricked to handle up to 1.5V$_{P-P}$. To do this, it is necessary to ground pin 3 and apply the differential input signal between pin 1 and 2. The input signal is now applied across two 1.1k resistors in series. Since the input signal is applied to both input pairs, the first pair will run out of bias current before the second pair, causing the amplifier to go open-loop. The results of this technique are shown in the following scope photo.

APPLICATIONS INFORMATION

LT1187 in Unity Gain



(A) STANDARD INPUTS, PINS 2 TO 3, V_{IN} = 1.0V_{P-P}
(B) EXTENDED INPUTS, PINS 2 TO 2, V_{IN} = 1.0V_{P-P}
(C) EXTENDED INPUTS, PINS 1 TO 2, V_{IN} = 2.0V_{P-P}

LT1187 • A06

Using the Shutdown Feature

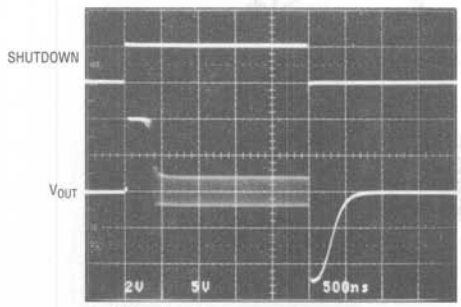
The LT1187 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 20k in parallel with the feedback resistors. For MUX applications, the amplifiers may be configured inverting, noninverting, or differential. When the output is loaded with as little 1k from the amplifier's feedback resistors, the amplifier shuts off in 600ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperature it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

Send Color Video Over Twisted-Pair

With an LT1187 it is possible to send and receive color composite video signals more than 1000 feet on a low cost twisted-pair. A bidirectional "video bus" consists of the LT1195 op amp and the LT1187 video difference amplifier. A pair of LT1195s at TRANSMIT 1, is used to generate differential signals to drive the line which is back-terminated in its characteristic impedance. The LT1187, twisted-pair receiver, converts signals from differential to single-ended. Topology of the LT1187 provides for cable compensation at the amplifier's feedback node as shown. In this case, 1000 feet of twisted-pair is compensated with 1000pF and 50Ω to boost the 3dB bandwidth of the system from 750kHz to 4MHz. This bandwidth is adequate to pass a 3.58MHz chroma subcarrier, and the 4.5MHz sound subcarrier. Attenuation in the cable can be compensated by lowering the gain set resistor R_G. At TRANSMIT 2, another pair of LT1195s serve the dual function to provide cable termination via low output impedance, and generate differential signals for TRANSMIT 2. Cable termination is made up of a 15Ω and 33Ω attenuator to reduce the differential input signal to the LT1187. Maximum input signal for the LT1187 is 760mV_{P-P}.

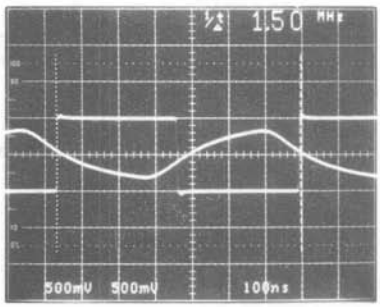
1MHz Sine Wave Gated Off with Shutdown Pin



A_V = 2, R_{FB} = R_G = 1k

LT1187 • A07

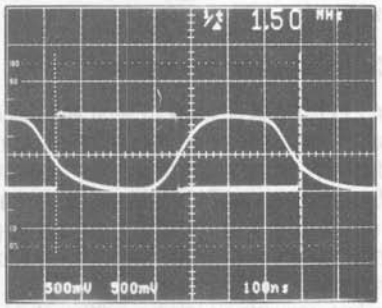
1.5MHz Square Wave Input and Unequalized Response Through 1000 Feet of Twisted-Pair



LT1187 • A08

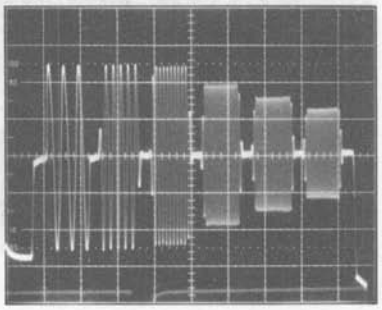
APPLICATIONS INFORMATION

1.5MHz Square Wave Input and Equalized Response Through 1000 Feet of Twisted-Pair



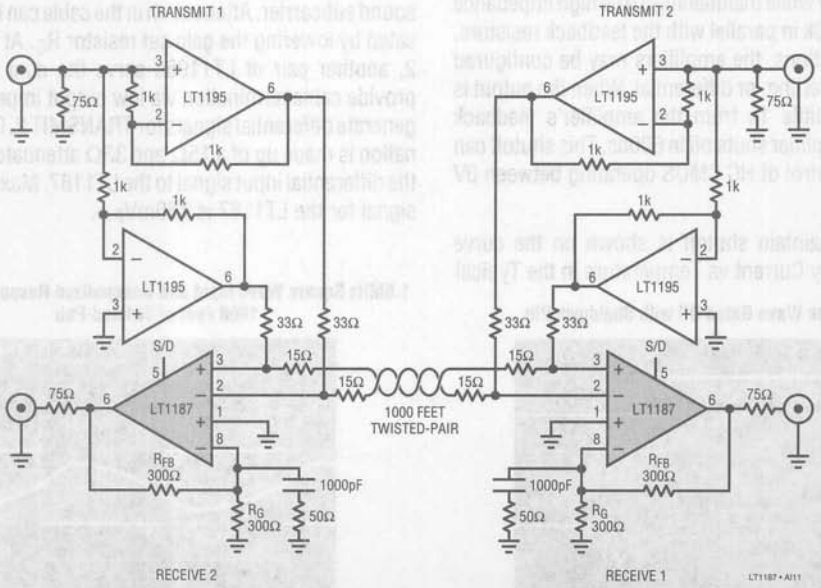
LT1187 • AI09

Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair

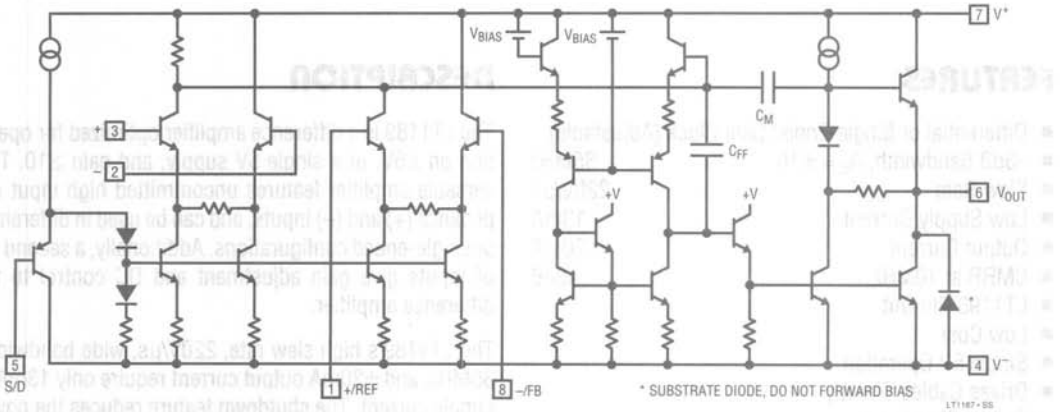


LT1187 • AI10

Bidirectional Video Bus



SIMPLIFIED SCHEMATIC



2

Low Power Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- –3dB Bandwidth, $A_V = \pm 10$ 35MHz
- Slew Rate 220V/µs
- Low Supply Current 13mA
- Output Current ±20mA
- CMRR at 10MHz 48dB
- LT1193 Pin Out
- Low Cost
- Single 5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Tape and Disc Drive Systems

DESCRIPTION

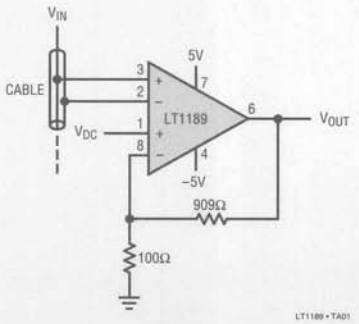
The LT1189 is a difference amplifier optimized for operation on ±5V, or a single 5V supply, and gain ≥10. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the difference amplifier.

The LT1189's high slew rate, 220V/µs, wide bandwidth, 35MHz, and ±20mA output current require only 13mA of supply current. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

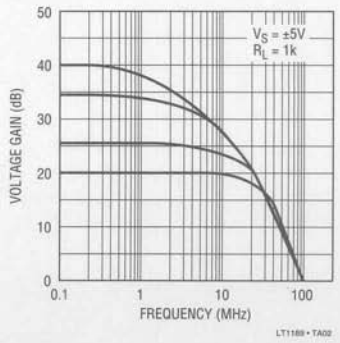
The LT1189 is a low power, gain of 10 stable version of the popular LT1193, and is available in 8-pin miniDIPs and SO packages. For lower gain applications see the LT1187 data sheet.

TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



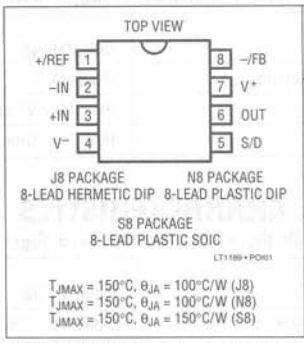
Closed-Loop Gain vs Frequency



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1189M ..... −55°C to 150°C
LT1189C ..... 0°C to 70°C
Junction Temperature (Note 2)
Plastic Package (CN8,CS8) ..... 150°C
Ceramic Package (CJ8,MJ8) ..... 175°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1189CJ8 LT1189CN8 LT1189CS8 LT1189MJ8
S8 PART MARKING
1189

Consult factory for Industrial grade parts.

2

±5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, $R_L = R_{FB1} + R_{FB2}$ = 1k, $C_L \leq$ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		1.0	3.0	mV
		SOIC Package		1.0	4.0	mV
I_{OS}	Input Offset Current	Either Input		0.2	1.0	µA
I_B	Input Bias Current	Either Input		±0.5	±2.0	µA
e_n	Input Noise Voltage	f_O = 10kHz		30		nV/√Hz
i_n	Input Noise Current	f_O = 10kHz		1.25		pA/√Hz
R_{IN}	Input Resistance	Differential		30		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 5)		±170		mV
	Input Voltage Range		−2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −2.5V to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	75	90		dB
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k, A_V = 50	±3.8	±4.0		V
		V_S = ±8V, R_L = 1k, A_V = 50	±6.7	±7.0		
		V_S = ±8V, R_L = 300Ω, A_V = 50, (Note 3)	±6.4	±6.8		
G_E	Gain Error	V_O = ±1.0V, A_V = 10		1.0	3.5	%
SR	Slew Rate	(Note 6, 10)	150	220		V/µs
FPBW	Full Power Bandwidth	V_O = $2V_{P-P}$, (Note 7)		35		MHz
BW	Small Signal Bandwidth	A_V = 10		35		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = ±1.5V, 20% to 80% (Note 10)	35	50	75	ns
t_{PD}	Propagation Delay	R_L = 1k, V_O = ±125mV, 50% to 50%		12		ns
	Overshoot	V_O = ±50mV		10		%
t_S	Settling Time	3V Step, 0.1%, (Note 8)		1		µs
Diff A_V	Differential Gain	R_L = 1k, A_V = 10, (Note 9)		0.6		%
Diff Ph	Differential Phase	R_L = 1k, A_V = 10, (Note 9)		0.75		DEG_{P-P}
I_S	Supply Current			13	16	mA
	Shutdown Supply Current	Pin 5 at V^-		0.8	1.5	mA

±5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M/C MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		500		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		600		ns

5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1189M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)			1.0	3.0	mV
		SOIC Package			1.0	5.0	mV
I_{OS}	Input Offset Current	Either Input			0.2	1.0	µA
I_B	Input Bias Current	Either Input			±0.5	±2.0	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		80	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground (Note 3)	V_{OUT} High	3.6	4.0		V
			V_{OUT} Low		0.15	0.4	
SR	Slew Rate	$V_O = 1.5V$ to 3.5V			175		V/µs
BW	Small-Signal Bandwidth	$A_V = 10$			30		MHz
I_S	Supply Current				12	15	mA
	Shutdown Supply Current	Pin 5 at V^-			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

±5V ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq 125°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		1.0	7.5	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			10		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	65	90		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.6		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		1.0	6.0	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

±5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	Either Input SOIC Package		1.0 1.0	3.0 6.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			5.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	70	90		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.6		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		1.0	3.5	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, (Note 3)

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1189C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage, (Note 4)	Either Input			1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift				5.0		µV/°C
I_{OS}	Input Offset Current	Either Input			0.2	1.5	µA
I_B	Input Bias Current	Either Input			±0.5	±3.5	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		80	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground	V_{OUT} High	3.5	4.0		V
		(Note 3)	V_{OUT} Low		0.15	0.4	
I_S	Supply Current				12	16	mA
	Shutdown Supply Current	Pin 5 at V, (Note 11)			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted continuously.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1189MJ8, LT1189CJ8: $T_J = T_A + (P_D \times 100°C/W)$
LT1189CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1189CS8: $T_J = T_A + (P_D \times 150°C/W)$

Note 3: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 300\Omega$ is specified, then an additional 430Ω is added to the output such that ($R_{FB1} + R_{FB2}$) in parallel with 430Ω is $R_L = 300\Omega$.

Note 4: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 5: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 6: Slew rate is measured between ±1V on the output, with a V_{IN} step of ±0.5V, $A_V = 10$ and $R_L = 1k$.

Note 7: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

Note 8: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

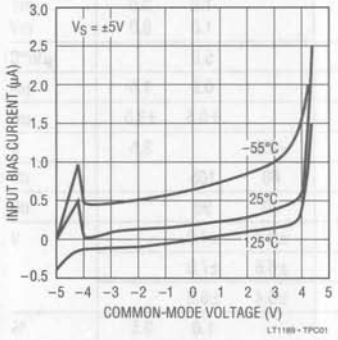
Note 9: NTSC (3.58MHz).

Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J8 and N8 suffix) and are sample tested on every lot of the SO packaged parts (S8 suffix).

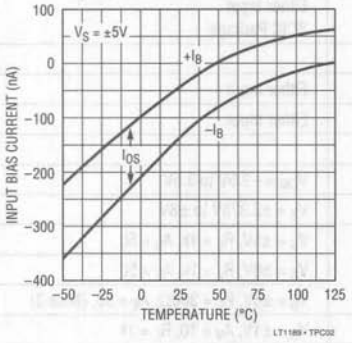
Note 11: See Application section for shutdown at elevated temperatures. Do not operate shutdown above $T_J > 125°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

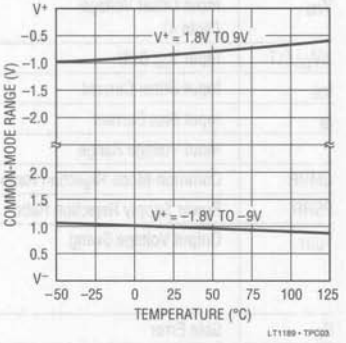
Input Bias Current vs Common-Mode Voltage



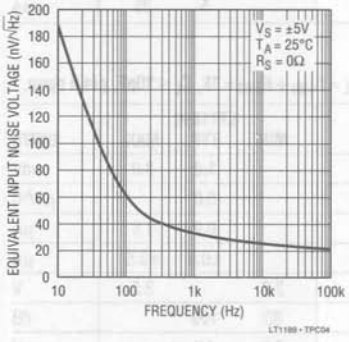
Input Bias Current vs Temperature



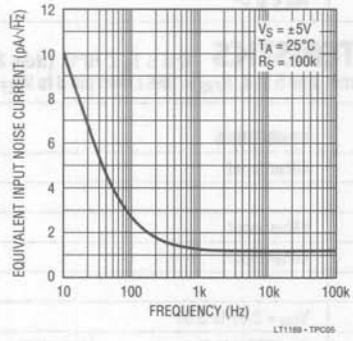
Common-Mode Voltage vs Temperature



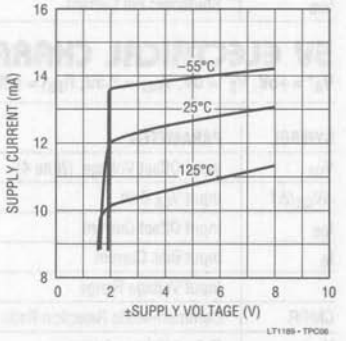
Equivalent Input Noise Voltage vs Frequency



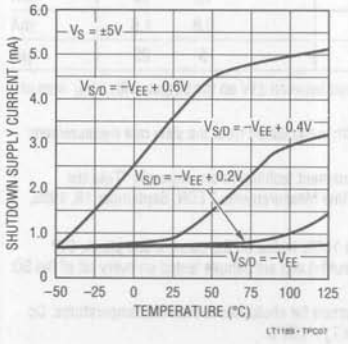
Equivalent Input Noise Current vs Frequency



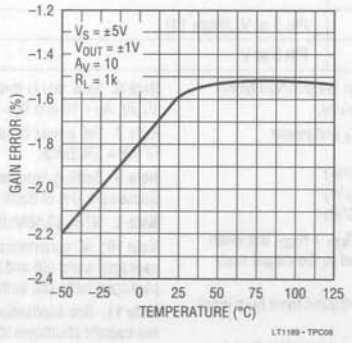
Supply Current vs Supply Voltage



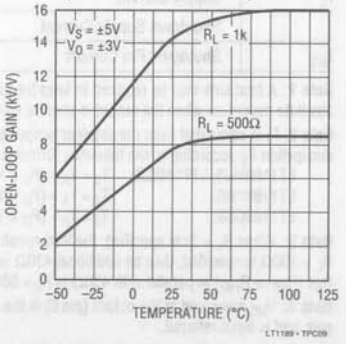
Shutdown Supply Current vs Temperature



Gain Error vs Temperature

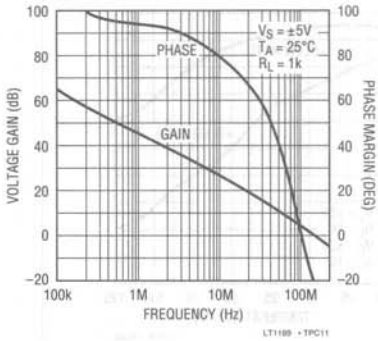


Open-Loop Gain vs Temperature

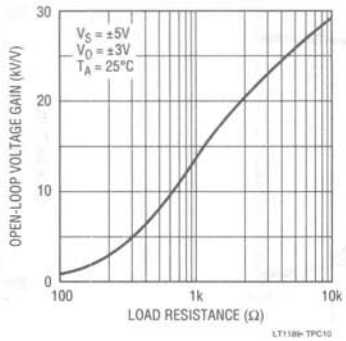


TYPICAL PERFORMANCE CHARACTERISTICS

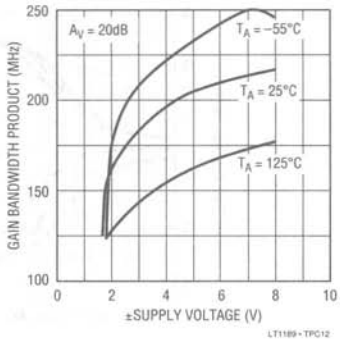
Gain, Phase vs Frequency



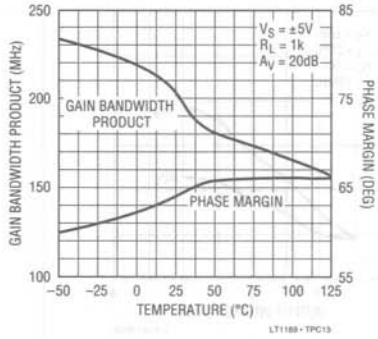
Open-Loop Voltage Gain vs Load Resistance



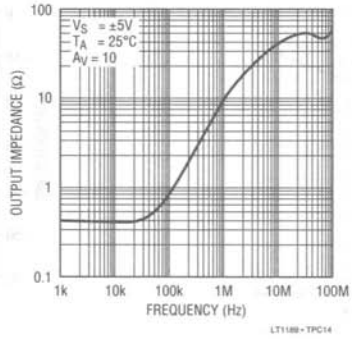
Gain Bandwidth Product vs Supply Voltage



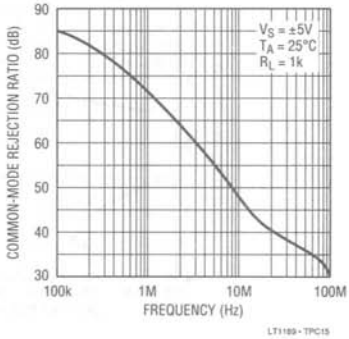
Gain Bandwidth Product and Phase Margin vs Temperature



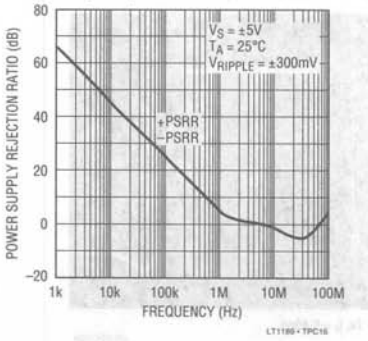
Output Impedance vs Frequency



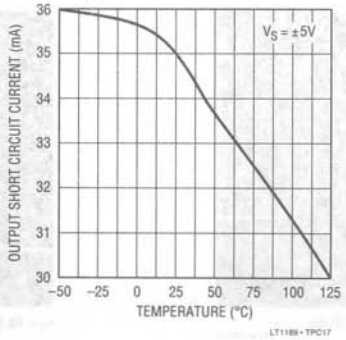
Common-Mode Rejection Ratio vs Frequency



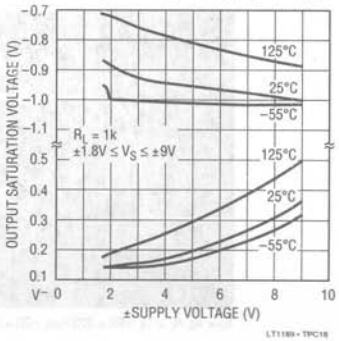
Power Supply Rejection Ratio vs Frequency



Output Short Circuit Current vs Temperature

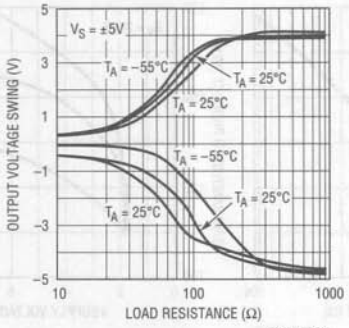


± Output Swing vs Supply Voltage



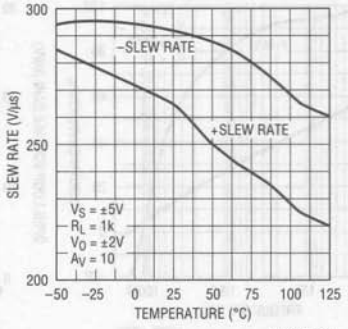
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



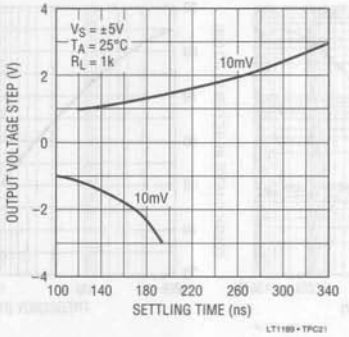
LT1189 • TPC19

Slew Rate vs Temperature



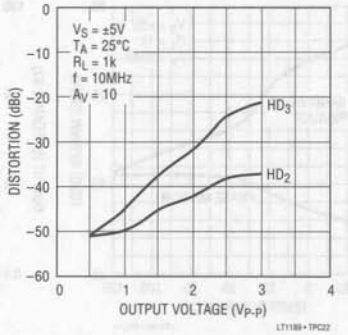
LT1189 • TPC20

Output Voltage Step vs Settling Time, A_V = 10



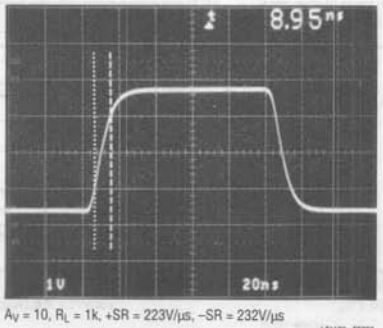
LT1189 • TPC21

Harmonic Distortion vs Output Level



LT1189 • TPC22

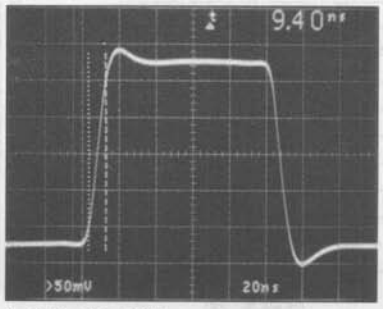
Large-Signal Transient Reponse



A_V = 10, R_L = 1k, +SR = 223V/µs, –SR = 232V/µs

LT1189 • TPC23

Small-Signal Transient Reponse



A_V = 10, R_L = 1k, t_r = 9.40ns

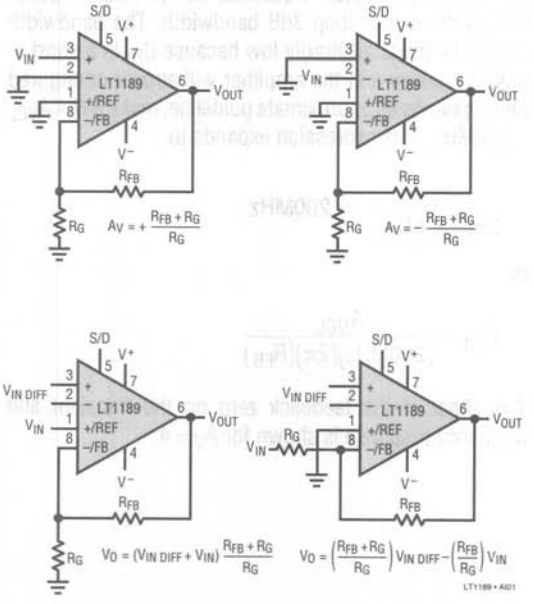
LT1189 • TPC24

LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

The primary use of the LT1189 is in converting high speed differential signals to a single-ended output. The LT1189 video difference amplifier has two uncommitted high input impedance (+) and (–) inputs. The amplifier has another set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust, and DC control to the differential amplifier. The voltage gain of the LT1189 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 10 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/REF (pin 1). The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±170mV.



Power Supply Bypassing

The LT1189 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. In applications requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended.

Calculating the Output Offset Voltage

Both input stages contribute to the output offset voltage at pin 6. The feedback correction forces balance in the input stages by introducing an Input V_{OS} at pin 8. The complete expression for the output offset voltage is:

$$V_{OUT} = (V_{OS} + I_{OS}(R_S) + I_B(R_{REF})) \times (R_{FB} + R_G)/R_G + I_B(R_{FB})$$

R_S represents the input source resistance, typically 75Ω, and R_{REF} represents finite source impedance from the DC reference voltage, for V_{REF} grounded, R_{REF} = 0Ω the I_{OS} is normally a small contributor and the expression simplifies to:

$$V_{OUT} = V_{OS}(R_{FB} + R_G)/R_G + I_B(R_{FB})$$

If R_{FB} is limited to 1k, the last term of the equation contributes only 2mV since I_B is less than 2µA.

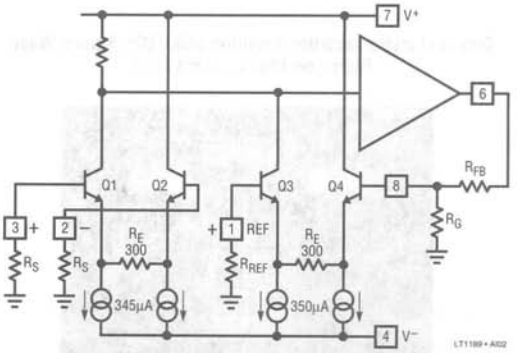


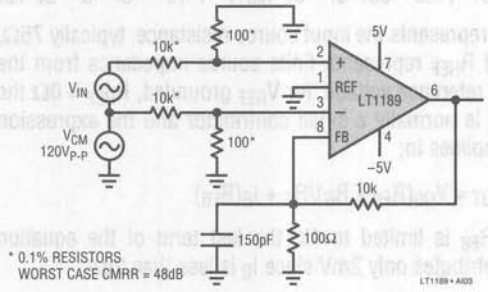
Figure 1. Simplified Input Stage Schematic

APPLICATIONS INFORMATION

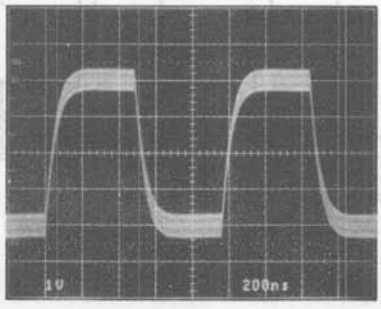
Instrumentation Amplifier Rejects High Voltage

Instrumentation amplifiers are often used to process slowly varying outputs from transducers. With the LT1189 it is easy to make an instrumentation amplifier that can respond to rapidly varying signals. Attenuation resistors in front of the LT1189 allow very large common-mode signals to be rejected while maintaining good frequency response. The input common-mode and differential-mode signals are reduced by 100:1, while the closed-loop gain is set to be 100, thereby maintaining unity-gain input to output. The unique topology allows for frequency response boost by adding 150pF to pin 8 as shown.

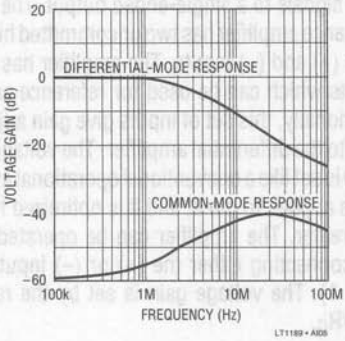
3.5MHz Instrumentation Amplifier Rejects 120V_{P-P}



Output of Instrumentation Amplifier with 1MHz Square Wave Riding on 120V_{P-P} at the Input



High Voltage Instrumentation Amplifier Response



Operating with Low Closed-Loop Gain

The LT1189 has been optimized for closed-loop gains of 10 or greater. The amplifier can be operated at much lower closed-loop gains with the aid of a capacitor C_{FB} across the feedback resistor, (feedback zero). This capacitor lowers the closed-loop 3dB bandwidth. The bandwidth cannot be made arbitrarily low because C_{FB} is a short at high frequency and the amplifier will appear configured unity-gain. As an approximate guideline, make $BW \times A_{VCL}$ = 200MHz. This expression expands to:

$$\frac{A_{VCL}}{2\pi(R_{FB})(C_{FB})} = 200MHz$$

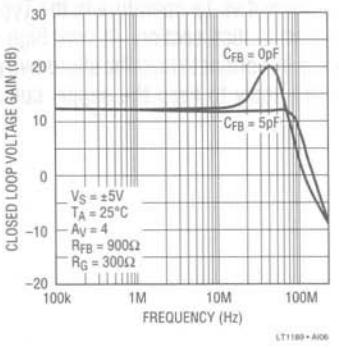
or:

$$C_{FB} = \frac{A_{VCL}}{(200MHz)(2\pi)(R_{FB})}$$

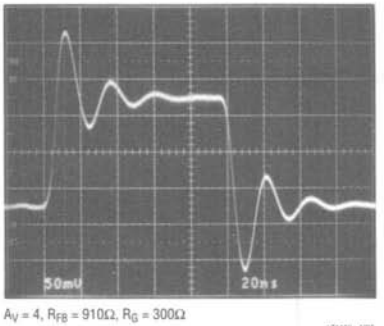
The effect of the feedback zero on the transient and frequency response is shown for A_V = 4.

APPLICATIONS INFORMATION

Closed-Loop Voltage Gain vs Frequency



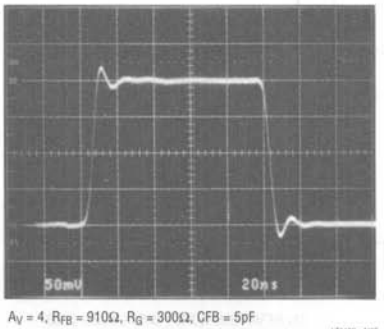
Small-Signal Transient Response



A_V = 4, R_{FB} = 910Ω, R_G = 300Ω

LT1189 • AI07

Small-Signal Transient Response



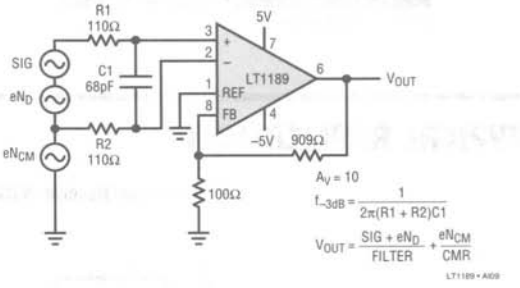
A_V = 4, R_{FB} = 910Ω, R_G = 300Ω, CFB = 5pF

LT1189 • AI08

Reducing the Closed-Loop Bandwidth

Although it is possible to reduce the closed-loop bandwidth by using a feedback zero, instability can occur if the bandwidth is made too low. An alternate technique is to do differential filtering at the input of the amplifier. This technique filters the differential input signal, and the differential noise, but does not filter common-mode noise. Common-mode noise is rejected by the LT1189's CMRR.

10MHz Bandwidth Limited Amplifier

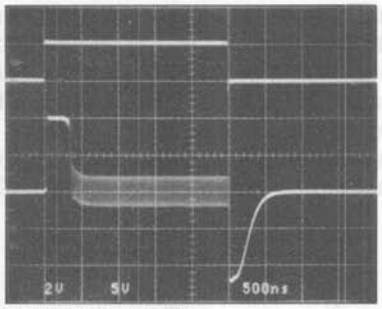


Using the Shutdown Feature

The LT1189 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of about 20kΩ in parallel with the feedback resistors. For MUX applications, the amplifiers may be configured inverting, non-inverting, or differential. When the output is loaded with as little as 1kΩ from the amplifier's feedback resistors, the amplifier shuts off in 600ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

APPLICATIONS INFORMATION

1MHz Sine Wave Gated Off with Shutdown Pin



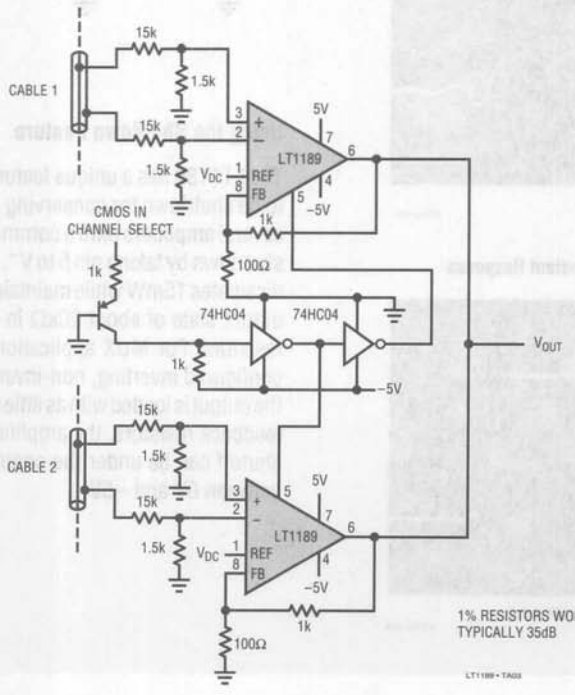
A_V = 10, R_{FB} = 900Ω, R_G = 100Ω

LT1189 • AI10

The ability to maintain shutoff is shown on the curve Shut down Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperature it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

TYPICAL APPLICATION

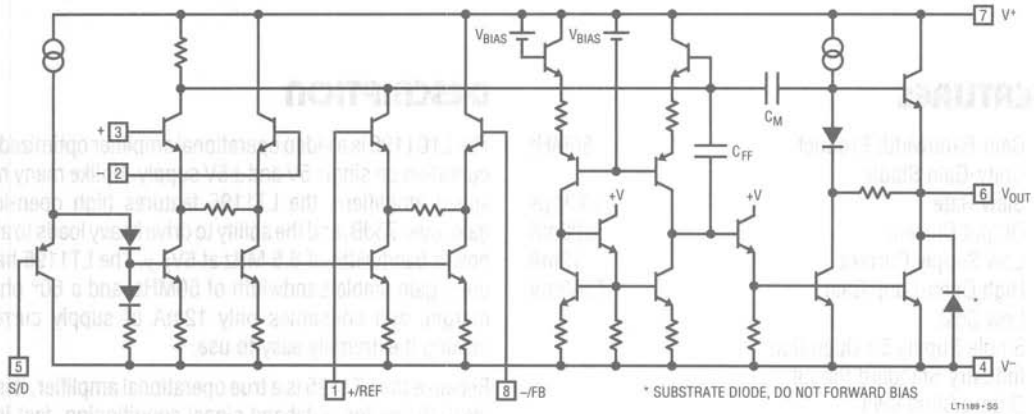
Differential Receiver MUX for Power Down Applications



1% RESISTORS WORST CASE CMRR = 28dB
TYPICALLY 35dB

LT1189 • TA03

SIMPLIFIED SCHEMATIC



2

Low Power, High Speed Operational Amplifier

FEATURES

- Gain-Bandwidth Product 50MHz
- Unity-Gain Stable
- Slew Rate 165V/µs
- Output Current ±20mA
- Low Supply Current 12mA
- High Open-Loop Gain 7.5V/mV
- Low Cost
- Single Supply 5V Operation
- Industry Standard Pinout
- Output Shutdown

APPLICATIONS

- Video Cable Drivers
- Video Signal Processing
- Fast Peak Detectors
- Fast Integrators
- Video Cable Drivers
- Pulse Amplifiers

DESCRIPTION

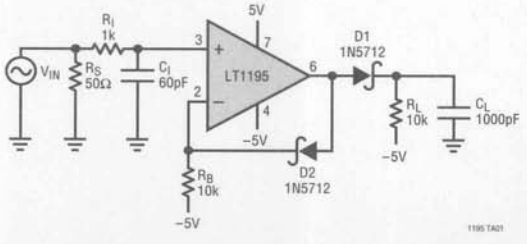
The LTC1195 is a video operational amplifier optimized for operation on single 5V and ±5V supply. Unlike many high speed amplifiers, the LT1195 features high open-loop gain, over 75dB, and the ability to drive heavy loads to a full power bandwidth of 8.5 MHz at $6V_{P-P}$. The LT1195 has a unity-gain stable bandwidth of 50MHz, and a 60° phase margin, and consumes only 12mA of supply current, making it extremely easy to use.

Because the LT1195 is a true operational amplifier, it is an ideal choice for wideband signal conditioning, fast integrators, peak detectors, active filters, and applications requiring speed, accuracy, and low cost.

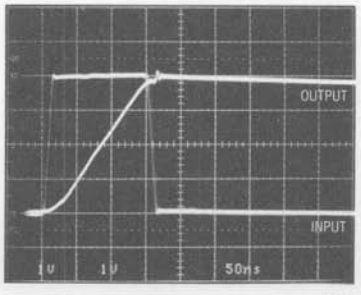
The LT1195 is a low power version of the popular LT1190, and is available in 8-pin miniDIPs and SO packages with standard pinouts. The normally unused pin 5 is used for a shutdown feature that shuts off the output and reduces power dissipation to a mere 15mW.

TYPICAL APPLICATION

Fast Pulse Detector



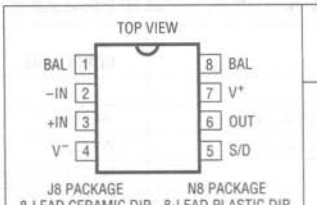
Pulse Detector Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1195M ..... –55°C to 125°C
LT1195C ..... 0°C to 70°C
Junction Temperature (Note 2)
Plastic Package (CN8, CS8) ..... 150°C
Ceramic Package (CJ8, MJ8) ..... 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1195MJ8 LT1195CJ8 LT1195CN8 LT1195CS8
S8 PART MARKING
1195

Consult factory for Industrial grade parts.

2

±5V ELECTRICAL CHARACTERISTICS T_A = 25°C

V_S = ±5V, $C_L \leq$ 10pF, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1195M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	J8, N8 Package		3.0	8.0	mV
		S8 Package		3.0	10.0	mV
I_{OS}	Input Offset Current			0.2	1.0	µA
I_B	Input Bias Current			±0.5	±2.0	µA
e_n	Input Noise Voltage	f_O = 10kHz		70		nV√Hz
i_n	Input Noise Current	f_O = 10kHz		2.0		pA√Hz
R_{IN}	Input Resistance Differential Mode			230		kΩ
	Input Resistance Common Mode			20		MΩ
C_{IN}	Input Capacitance	A_V = 1		2.2		pF
	Input Voltage Range	(Note 3)	–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = –2.5 to 3.5V	60	85		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	60	85		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 1k, V_{OUT} = ±3V	2.0	7.5		V/mV
		R_L = 150Ω, V_{OUT} = ±3V	0.5	1.5		V/mV
		V_S = ±8V, R_L = 1k, V_{OUT} = ±5V		11.0		V/mV
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k	±3.8	±4.0		V
		V_S = ±8V, R_L = 1k	±6.7	±7.0		V
SR	Slew Rate	A_V = –1, R_L = 1k, (Note 4, 9)	110	165		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $6V_{P-P}$, (Note 5)		8.75		MHz
GBW	Gain-Bandwidth Product			50		MHz
t_{r1}, t_{f1}	Rise Time, Fall Time	A_V = 50, V_{OUT} = ±1.5V, 20% to 80%, (Note 9)	125	170	250	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	A_V = 1, V_{OUT} = ±125mV, 10% to 90%		3.4		ns
t_{PD}	Propagation Delay	A_V = 1, V_{OUT} = ±125mV, 50% to 50%		2.5		ns
	Overshoot	A_V = 1, V_{OUT} = ±125mV		22		%
t_S	Settling Time	3V Step, 0.1%, (Note 6)		220		ns
Diff A_V	Differential Gain	R_L = 150Ω, A_V = 2, (Note 7)		1.25		%
Diff Ph	Differential Phase	R_L = 150Ω, A_V = 2, (Note 7)		0.86		DEG_{P-P}

±5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$

$V_S = \pm5V$, $C_L \leq 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1195M/C MIN	TYP	MAX	UNITS
I_S	Supply Current			12	16	mA
	Shutdown Supply Current	Pin 5 at V^-		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA
t_{ON}	Turn-On Time	Pin 5 from V^- to Ground, R_L = 1k		160		ns
t_{OFF}	Turn-Off Time	Pin 5 from Ground to V^-, R_L = 1k		700		ns

5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{CM} = 2.5V$, $C_L \leq 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1195M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	J8, N8 Package			3.0	9.0	mV
		S8 Package			3.0	11.0	mV
I_{OS}	Input Offset Current				0.2	1.0	µA
I_B	Input Bias Current				±0.5	±2.0	µA
	Input Voltage Range	(Note 3)		2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 2V to 3.5V		60	85		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 150Ω to Ground, V_O = 1V to 3V		0.5	3.0		V/mV
V_{OUT}	Output Voltage Swing	R_L = 150Ω to Ground	V_{OUT} High	3.5	3.8		V
			V_{OUT} Low		0.25	0.4	V
SR	Slew Rate	$A_V = -1$, V_{OUT} = 1V to 3V			140		V/µs
GBW	Gain-Bandwidth Product				45		MHz
I_S	Supply Current				11	15	mA
	Shutdown Supply Current	Pin 5 at V^-			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

±5V ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq 125°C$, (Note 10)

$V_S = \pm5V$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1195M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			3.0	15.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			17		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	2.0	µA
I_B	Input Bias Current	Either Input		±0.5	±2.5	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	55	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	55	80		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 1k, $V_{OUT} = \pm3V$	1.50	5.0		V/mV
		R_L = 150Ω, $V_{OUT} = \pm3V$	0.25	0.8		V/mV
V_{OUT}	Output Voltage Swing	R_L = 1k	±3.7	±3.9		V
I_S	Supply Current			12	18	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 8)		0.8	2.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

±5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$

V_S = ±5V, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1195C MIN	LT1195C TYP	LT1195C MAX	UNITS
V_{OS}	Input Offset Voltage	J8, N8 Package S8 Package		3.0 3.0	10.0 15.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			12		µV/°C
I_{OS}	Input Offset Current			0.2	1.7	µA
I_B	Input Bias Current			±0.5	±2.5	µA
CMRR	Common-Mode Rejection Ratio	V_{CM} = −2.5V to 3.5V	60	85		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±5V	60	90		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 1k , V_{OUT} = ±3V R_L = 150Ω , V_{OUT} = ±3V	2.0 0.3	7.5 1.5		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 1k	±3.7	±3.9		V
I_S	Supply Current			12	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 8)		0.9	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

5V ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$

V_S^+ = 5V, V_S^- = 0V, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1195C MIN	LT1195C TYP	LT1195C MAX	UNITS
V_{OS}	Input Offset Voltage	J8, N8 Package S8 Package			1.0 1.0	10.0 15.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift				15		µV/°C
I_{OS}	Input Offset Current	Either Input			0.2	1.7	µA
I_B	Input Bias Current	Either Input			±0.5	±2.5	µA
	Input Voltage Range	(Note 3)		2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 2V to 3.5V		60	85		dB
V_{OUT}	Output Voltage Swing	R_L = 150Ω to Ground	V_{OUT} High	3.5	3.75		V
			V_{OUT} Low		0.15	0.4	V
I_S	Supply Current				12	16	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 8)			0.9	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted continuously.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1195MJ8, LT1195CJ8: $T_J = T_A + (P_D \times 100°C/W)$
LT1195CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1195CS8: $T_J = T_A + (P_D \times 150°C/W)$

Note 3: Exceeding the input common-mode range may cause the output to invert.

Note 4: Slew rate is measured between ±1V on the output, with a ±3V input step.

Note 5: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 6: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

Note 7: NTSC (3.58MHz). For R_L = 1k, Diff A_V = 0.3%, Diff Ph = 0.35°.

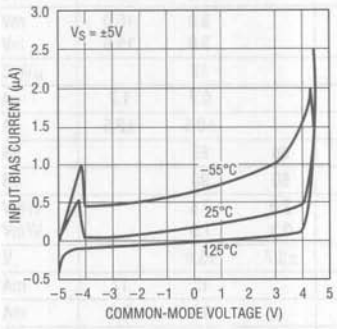
Note 8: See Applications Information section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

Note 9: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J8 and N8 suffix) and are sample tested on every lot of the SO packaged parts (S8 suffix).

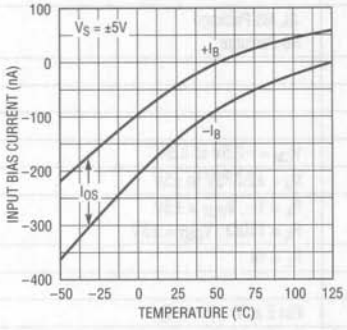
Note 10: Do not operate at $A_V < 2$ for $T_A < 0°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

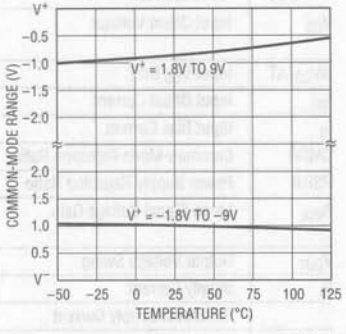
Input Bias Current vs Common-Mode Voltage



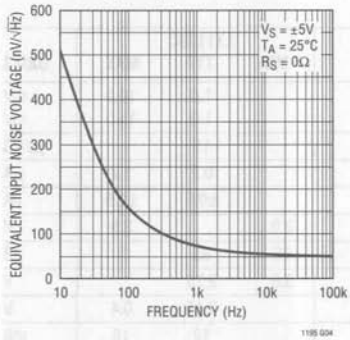
Input Bias Current vs Temperature



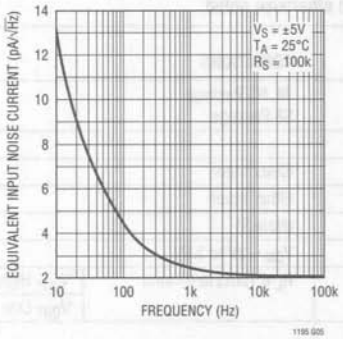
Common-Mode Voltage vs Temperature



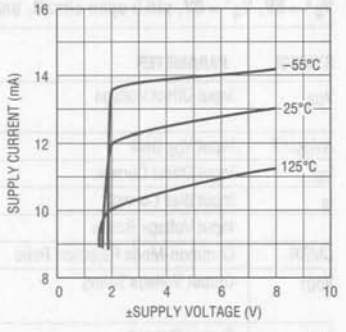
Equivalent Input Noise Voltage vs Frequency



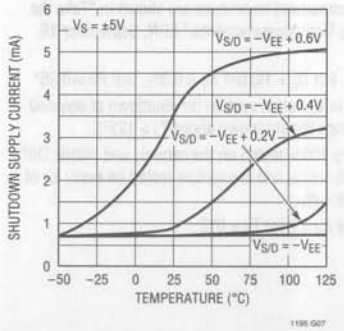
Equivalent Input Noise Current vs Frequency



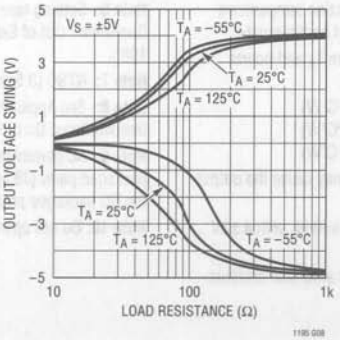
Supply Current vs Supply Voltage



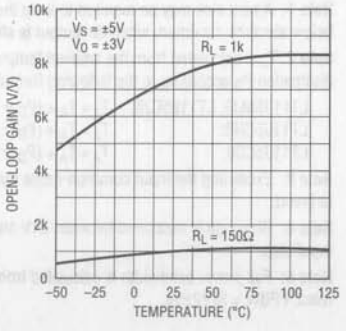
Shutdown Supply Current vs Temperature



Output Voltage Swing vs Load Resistance

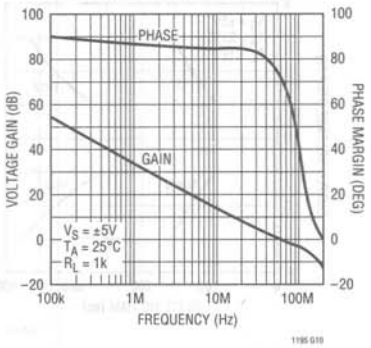


Open-Loop Gain vs Temperature

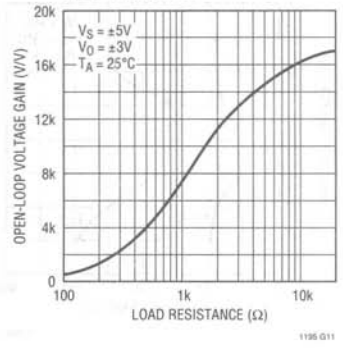


TYPICAL PERFORMANCE CHARACTERISTICS

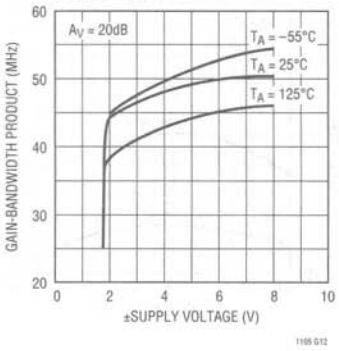
Gain and Phase vs Frequency



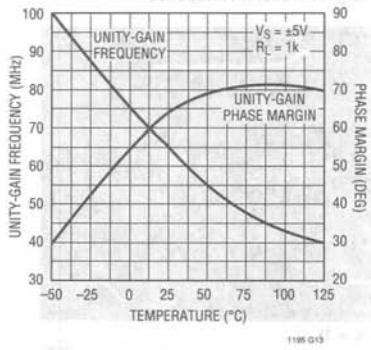
Open-Loop Voltage Gain vs Load Resistance



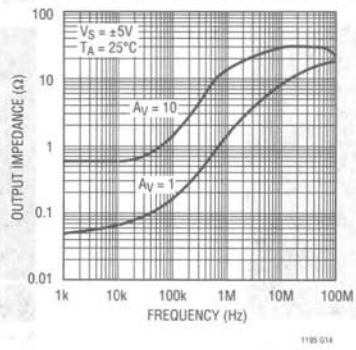
Gain Bandwidth Product vs Supply Voltage



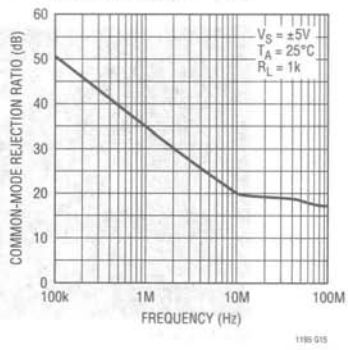
Unity-Gain Frequency and Phase Margin vs Temperature



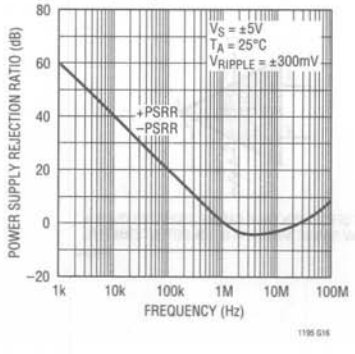
Output Impedance vs Frequency



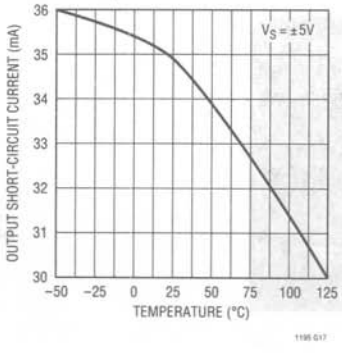
Common-Mode Rejection Ratio vs Frequency



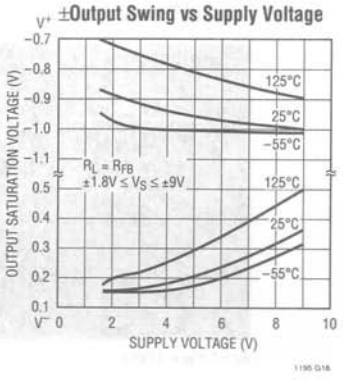
Power Supply Rejection Ratio vs Frequency



Output Short-Circuit Current vs Temperature



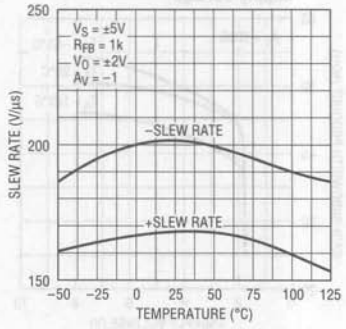
±Output Swing vs Supply Voltage



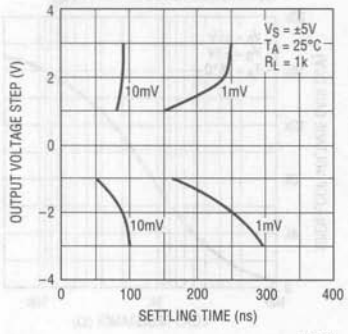
2

TYPICAL PERFORMANCE CHARACTERISTICS

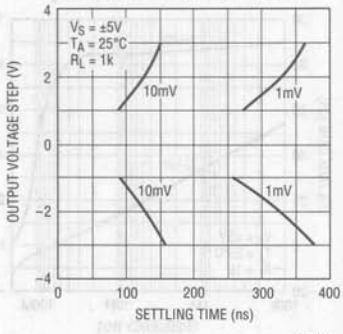
Slew Rate vs Temperature



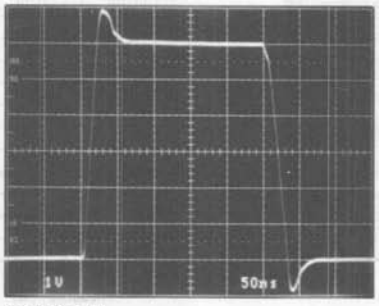
Output Voltage Step vs Settling Time, $A_V = -1$



Output Voltage Step vs Settling Time, $A_V = 1$



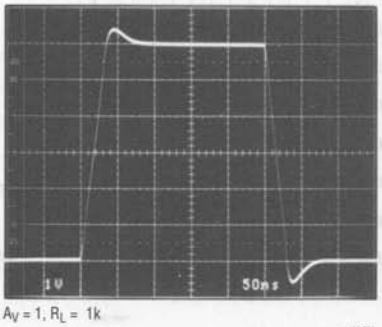
Large-Signal Transient Response



$A_V = 1$, $R_L = 1k$

1195 G22

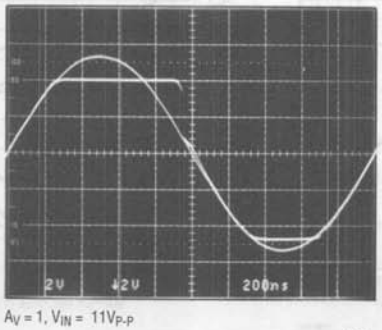
Large-Signal Transient Response



$A_V = 1$, $R_L = 1k$

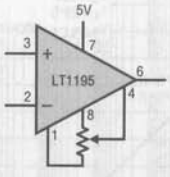
1195 G23

Overload Recovery



$A_V = 1$, $V_{IN} = 11V_{P-P}$

1195 G24



INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±150mV RANGE WITH A 1k to 10k POTENTIOMETER.

1195 G25

APPLICATIONS INFORMATION

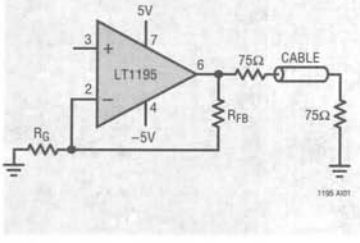
Power Supply Bypassing

The LT1195 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 0.5 inches from the ampifier is all that is required. In applications requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended.

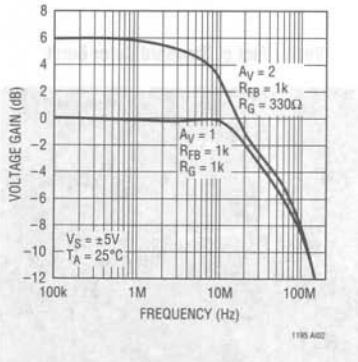
Cable Terminations

The LT1195 operational amplifier has been optimized as a low cost video cable driver. The ±20mA guaranteed output current enables the LT1195 to easily deliver $6V_{P-P}$ into 150Ω, while operating on ±5V supplies.

Double-Terminated Cable Driver



Cable Driver Voltage Gain vs Frequency

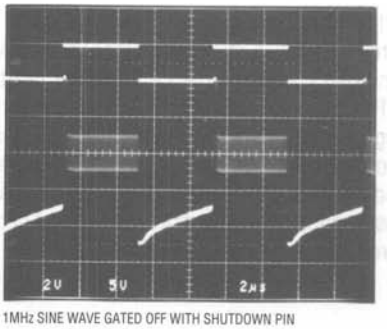


When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. this can be compensated for by taking a gain of 2, or 6dB in the amplifier.

Using the Shutdown Feature

The LT1195 has a unique feature that allows the amplifier to be shut down for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15k in parallel with the feedback resistors. The amplifiers must be used in a noninverting configuration for MUX applications. In inverting configurations the input signal is fed to the output through the feedback components. The following scope photos show that with very high R_L, the output is truly high impedance; the output slowly decays toward ground. Additionally, when the output is loaded with as little as 1k the amplifier shuts off in 700ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN
A_V = 1, R_L = SCOPE PROBE
1195 A03

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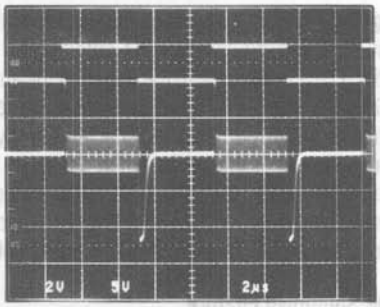
APPLICATIONS INFORMATION

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN
A_V = 1, R_L = 1k

1195 A04

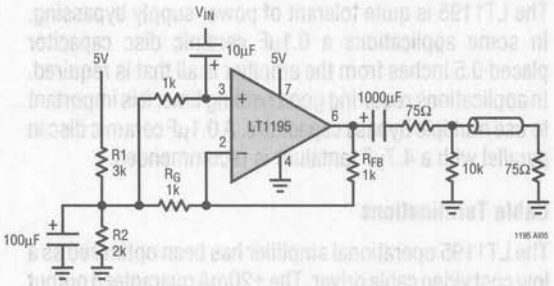
Detecting Pulses

The front page shows a circuit for detecting very fast pulses. In this open-loop design, the detector diode is D1 and a level shifting or compensating diode is D2. A load resistor R_L is connected to –5V, and an identical bias resistor R_B is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. A very fast pulse will exceed the amplifier slew rate and cause a long overload recovery time. Some amount of dV/dt limiting on the input can help this overload condition, however too much will delay the response. Also shown is the response to a $4V_{P-P}$ input that is 150ns wide. The maximum output slew rate in the photo is 30V/µs. This rate is set by the 30mA current limit driving 1000pF.

Operation on Single 5V Supply

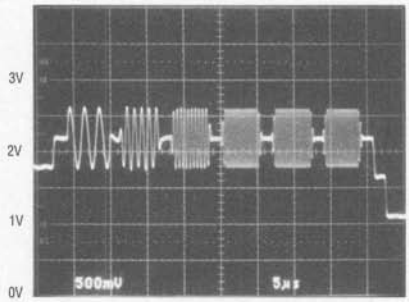
The LT1195 has been optimized for a single 5V supply. This circuit amplifies standard composite video ($1V_{P-P}$ including sync) by 2 and drives a double-terminated 75Ω cable. Resistors R1 and R2 bias the amplifier at 2V, allowing the sync pulses to stay within the common-mode range of the amplifier. Large coupling capacitors are required to pass the low frequency sidebands of the composite signal. A multiburst response and vector plot standard color burst are shown.

Single 5V Video Amplifier



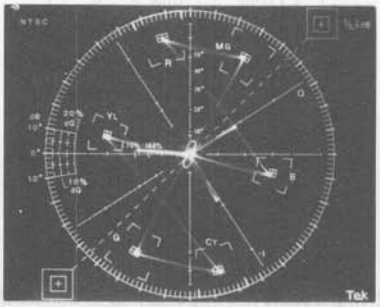
1195 A05

Video Multiburst at Pin 6 of Amplifier



1195 A06

Vector Plot of Standard Color Burst



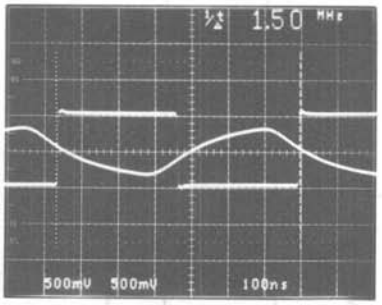
1195 A07

APPLICATIONS INFORMATION

Send Color Video Over Twisted-Pair

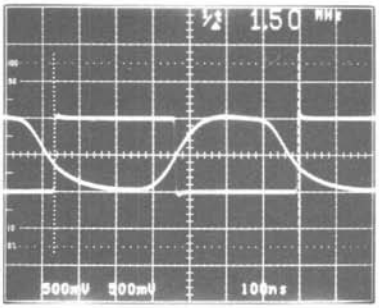
With an LT1195 it is possible to send and receive color composite video signals more than 1000 feet on a low cost twisted-pair. A bidirectional "video bus" consists of the LT1195 op amp and the LT1187 video difference amplifier. A pair of LT1195s at TRANSMIT 1, is used to generate differential signals to drive the line which is back-terminated in its characteristic impedance. The LT1187, twisted-pair receiver, converts signals from differentials to single-ended. Topology of the LT1187 provides for cable compensation at the amplifier's feedback node as shown. In this case, 1000 feet of twisted-pair is compensated with 1000pF and 50Ω to boost the 3dB bandwidth of the system from 750kHz to 4MHz. This bandwidth is adequate to pass a 3.58MHz chrome subcarrier, and the 4.5MHz sound subcarrier. Attenuation in the cable can be compensated by lowering the gain set resistor R_G. At TRANSMIT 2, another pair of LT1195s serve the dual function to provide cable termination via low output impedance, and generate differential signals for TRANSMIT 2. Cable termination is made up of 15Ω and 33Ω attentuator to reduce the differential input signal to the LT1187. Maximum input signal for the LT1187 is 760mV$_{P-P}$.

1.5MHz Square Wave Input and Unequalized Response Through 1000 Feet of Twisted-Pair



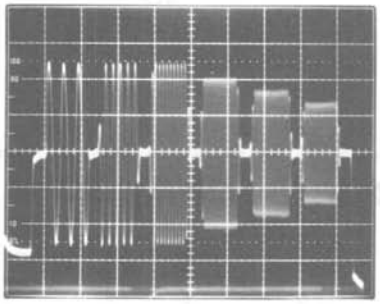
1195 A108

1.5MHz Square Wave Input and Equalized Response Through 1000 Feet of Twisted-Pair



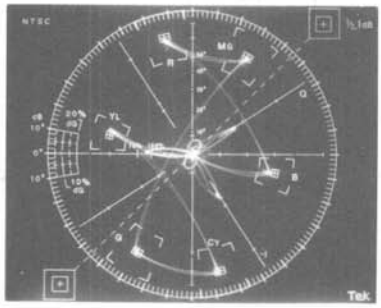
1195 A109

Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair



1195 A110

Vector Plot of Standard Color Burst Through 1000 Feet of Twisted-Pair

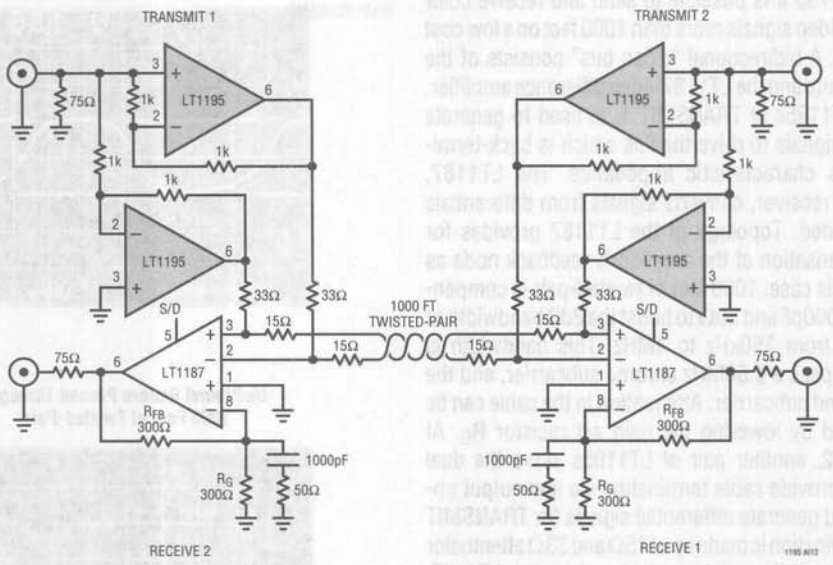


1195 A111

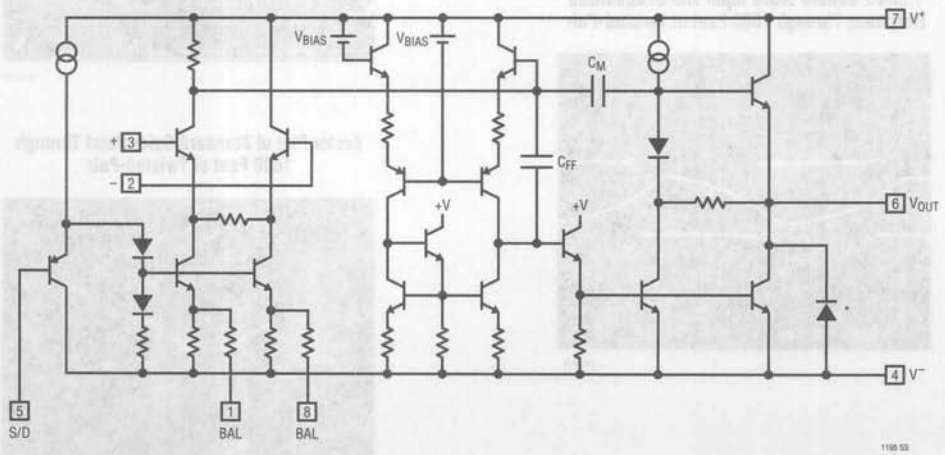
2

APPLICATIONS INFORMATION

Bidirectional Video Bus



SIMPLIFIED SCHEMATIC



* SUBSTRATE DIODE, DO NOT FORWARD BIAS

Dual and Quad 1mA, 12MHz, 50V/µs Op Amps

FEATURES

- **1mA Supply Current per Amplifier**
- 50V/µs Slew Rate
- 12MHz Gain-Bandwidth
- Unity-Gain Stable
- 330ns Settling Time to 0.1%, 10V Step
- 6V/mV DC Gain, R_L = 2kΩ
- 2mV Maximum Input Offset Voltage
- 100nA Maximum Input Offset Current
- 1µA Maximum Input Bias Current
- ±12V Minimum Output Swing into 2kΩ
- Wide Supply Range: ±2.5V to ±15V
- Drives Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

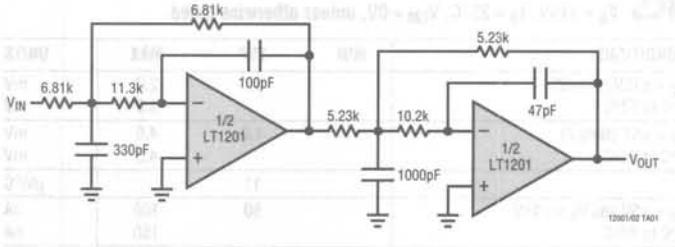
The LT1201/LT1202 are dual and quad low power, high speed operational amplifiers with excellent DC performance. The LT1201/LT1202 feature much lower supply current than devices with comparable bandwidth and slew rate. Each amplifier is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. Each output is capable of driving a 2kΩ load to ±12V with ±15V supplies and a 500Ω load to ±3V on ±5V supplies. The amplifiers are also capable of driving large capacitive loads which make them useful in buffer or cable driver applications.

The LT1201/LT1202 are members of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

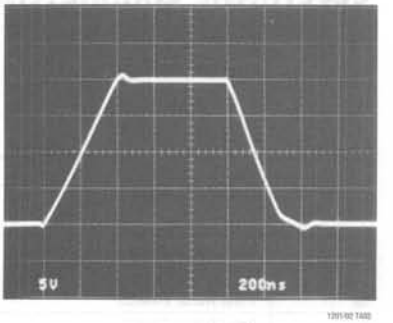
2

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



Inverter Pulse Response

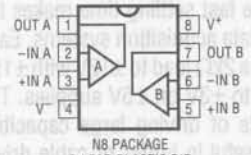


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
LT1201C/LT1202C ..... −40°C to 85°C
Specified Temperature Range (Note 5)
LT1201C/LT1202C ..... 0°C to 70°C
Maximum Junction Temperature
Plastic Package ..... 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



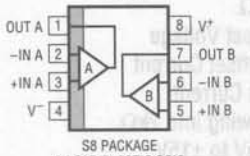
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1201CN8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

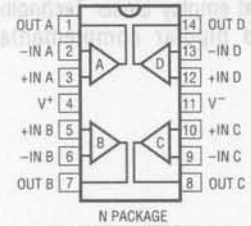
ORDER PART NUMBER

LT1201CS8

S8 PART MARKING

1201

TOP VIEW



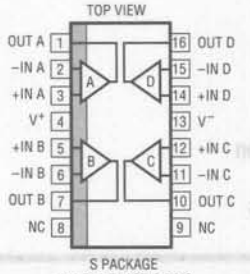
N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1202CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1202CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = ±15V (Note 2)		0.7	2.0	mV
		0°C to 70°C			3.0	mV
		V_S = ±5V (Note 2)		1.0	4.0	mV
		0°C to 70°C			4.5	mV
	Input V_{OS} Drift			11		µV/°C
I_{OS}	Input Offset Current	V_S = ±5V and V_S = ±15V		50	100	nA
		0°C to 70°C			150	nA
I_B	Input Bias Current	V_S = ±5V and V_S = ±15V		0.5	1.0	µA
		0°C to 70°C			1.2	µA
e_n	Input Noise Voltage	f = 10kHz		30		nV/√Hz
i_n	Input Noise Current	f = 10kHz		0.6		pA/√Hz

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	$V_{CM} = \pm12V$ Differential	48	90 500		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$; $V_S = \pm5V$, $V_{CM} = \pm2.5V$ 0°C to 70°C	92 90	100		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$ 0°C to 70°C	80 80	90		dB dB
	Input Voltage Range$^+$	$V_S = \pm15V$ $V_S = \pm5V$	12.0 2.5	14 4		V V
	Input Voltage Range$^-$	$V_S = \pm15V$ $V_S = \pm5V$		−13 −3	−12.0 −2.5	V V
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 5k$ 0°C to 70°C	4.0 3.5	8		V/mV V/mV
		$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 2k$ 0°C to 70°C	3.0 2.5	6		V/mV V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 2k$ 0°C to 70°C	2.5 2.0	5		V/mV V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 1k$ 0°C to 70°C	2.0 1.6	4		V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 2k$, 0°C to 70°C $V_S = \pm5V$, $R_L = 500\Omega$, 0°C to 70°C	12.0 3.0	13.8 4.0		±V ±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$, 0°C to 70°C $V_S = \pm5V$, $V_{OUT} = \pm3V$, 0°C to 70°C	6 6	12 12		mA mA
SR	Slew Rate	$V_S = \pm15V$, $A_{VCL} = -2$ (Note 3) 0°C to 70°C	30 27	50		V/µs V/µs
		$V_S = \pm5V$, $A_{VCL} = -2$ (Note 3) 0°C to 70°C	20 18	33		V/µs V/µs
	Full Power Bandwidth	$V_S = \pm15V$, 10V Peak (Note 4) $V_S = \pm5V$, 3V Peak (Note 4)		0.8 1.7		MHz MHz
GBW	Gain-Bandwidth	$V_S = \pm15V$, f = 0.1MHz $V_S = \pm5V$, f = 0.1MHz		12 9		MHz MHz
t_r, t_f	Rise Time, Fall Time	$V_S = \pm15V$, $A_{VCL} = 1$, 10% to 90%, 0.1V $V_S = \pm5V$, $A_{VCL} = 1$, 10% to 90%, 0.1V		18 23		ns ns
	Overshoot	$V_S = \pm15V$, $A_{VCL} = 1$, 0.1V $V_S = \pm5V$, $A_{VCL} = 1$, 0.1V		25 20		% %
	Propagation Delay	$V_S = \pm15V$, 50% V_{IN} to 50%V_{OUT} $V_S = \pm5V$, 50% V_{IN} to 50%V_{OUT}		18 23		ns ns
t_s	Settling Time	$V_S = \pm15V$, 10V Step, 0.1%, $A_{VCL} = 1$ $V_S = \pm5V$, 5V Step, 0.1%, $A_{VCL} = 1$		330 300		ns ns
R_O	Output Resistance	$A_{VCL} = 1$, f = 0.1MHz		1.1		Ω
	Crosstalk	$V_{OUT} = \pm10V$, $R_L = 2k$		−110	−100	dB
I_S	Supply Current	Each Amplifier, $V_S = \pm5V$ and $V_S = \pm15V$ 0°C to 70°C		1	1.4 1.6	mA mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested with automated test equipment and is exclusive of warm-up drift.

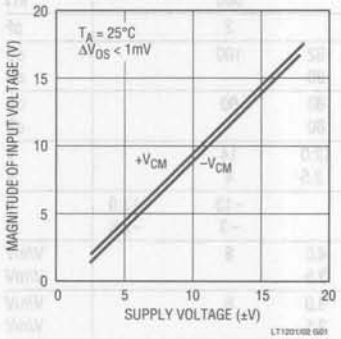
Note 3: Slew rate is measured in a gain of −2. For ±15V supplies measure between ±10V on the output with ±6V on the input. For ±5V supplies measure between ±2V on the output with ±1.75V on the input.

Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

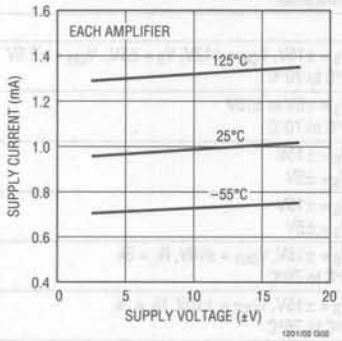
Note 5: Commercial grade parts are designed to operate over the temperature range of −40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over −40°C to 85°C are available on special request. Consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

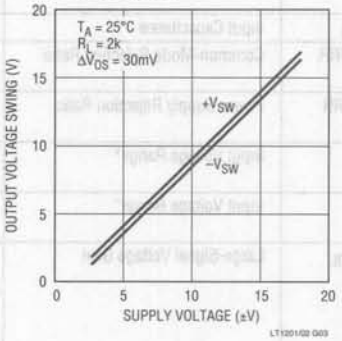
Input Common-Mode Range vs Supply Voltage



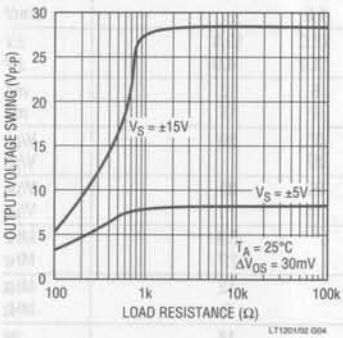
Supply Current vs Supply Voltage



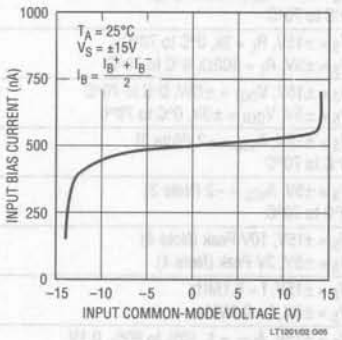
Output Voltage Swing vs Supply Voltage



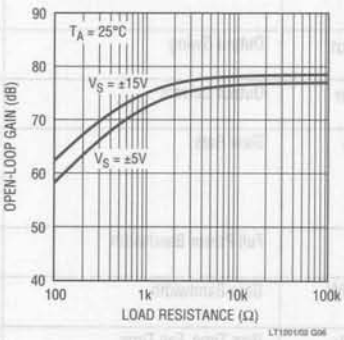
Output Voltage Swing vs Resistive Load



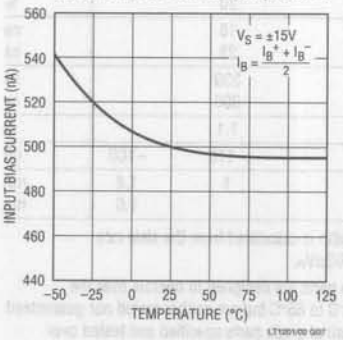
Input Bias Current vs Input Common-Mode Voltage



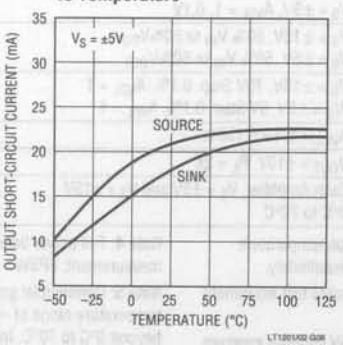
Open-Loop Gain vs Resistive Load



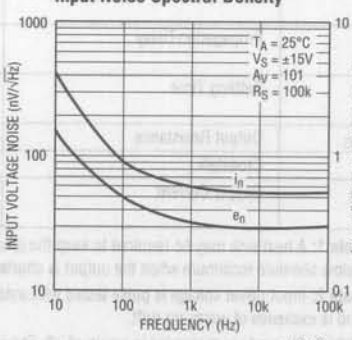
Input Bias Current vs Temperature



Output Short-Circuit Current vs Temperature



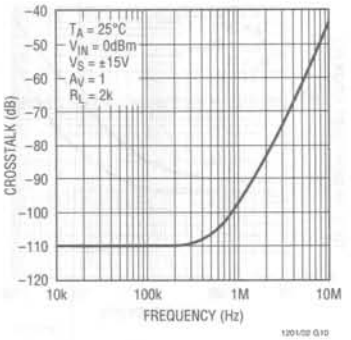
Input Noise Spectral Density



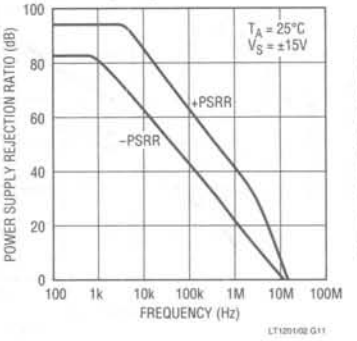
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

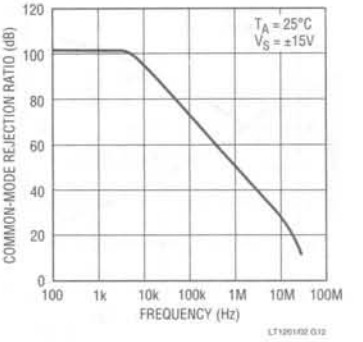
Crosstalk vs Frequency



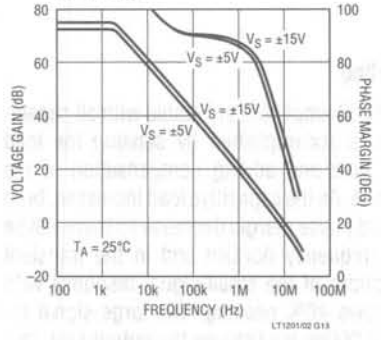
Power Supply Rejection Ratio vs Frequency



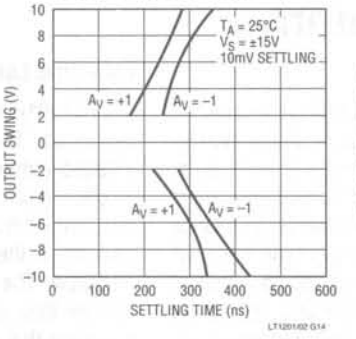
Common-Mode Rejection Ratio vs Frequency



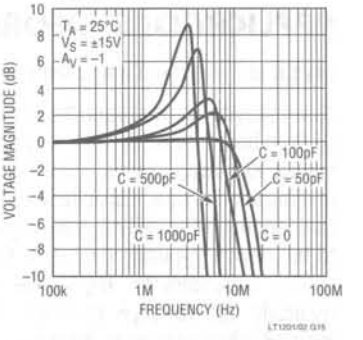
Voltage Gain and Phase vs Frequency



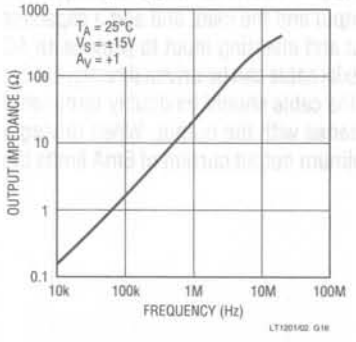
Output Swing vs Settling Time



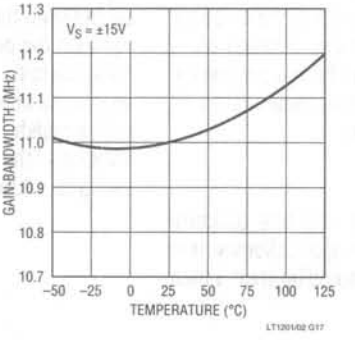
Frequency Response vs Capacitive Load



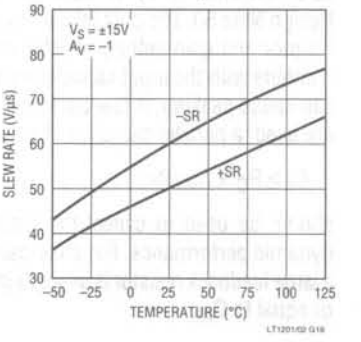
Closed-Loop Output Impedance vs Frequency



Gain-Bandwidth vs Temperature



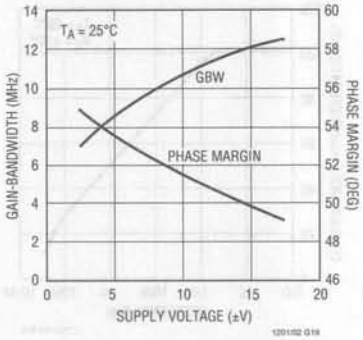
Slew Rate vs Temperature



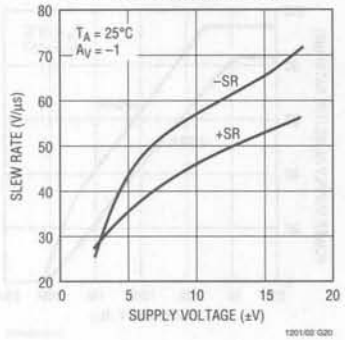
2

TYPICAL PERFORMANCE CHARACTERISTICS

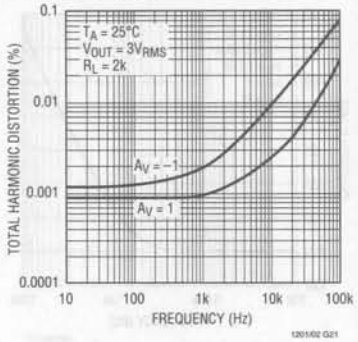
Gain-Bandwidth and Phase Margin vs Supply Voltage



Slew Rate vs Supply Voltage



Total Harmonic Distortion vs Frequency



APPLICATIONS INFORMATION

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF) and low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of value:

$$C_F \geq R_G \times C_{IN}/R_F$$

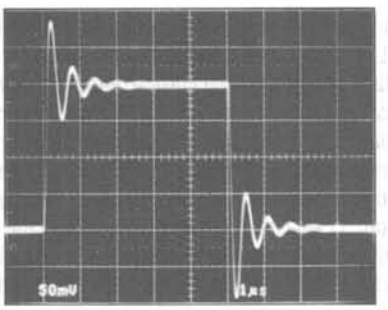
should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1201/LT1202 amplifiers are stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small-signal response with 1000pF load shows 40% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current. To reduce peaking with capacitive loads, insert a small decoupling resistor between the output and the load, and add a capacitor between the output and inverting input to provide an AC feedback path. Coaxial cable can be driven directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output. When driving a 150Ω load the minimum output current of 6mA limits the swing to ±0.9V.

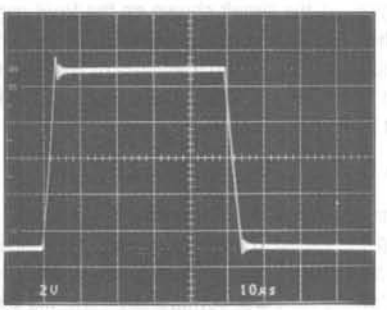
APPLICATIONS INFORMATION

Small-Signal Capacitive Loading



$A_V = -1$
$C_L = 1000pF$

Large-Signal Capacitive Loading



$A_V = 1$
$C_L = 10,000pF$

Input Considerations

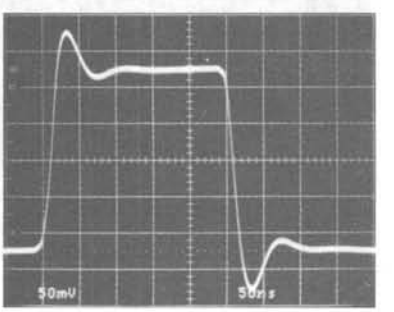
Resistors in series with the inputs are recommended for the LT1201/LT1202 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

Transient Response

The LT1201/LT1202 gain-bandwidth is 12MHz when measured at 100kHz. The actual frequency response in unity-gain is considerably higher than 12MHz due to peaking caused by a second pole beyond the unity-gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity-gain small-signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

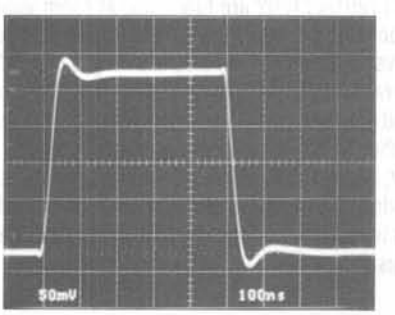
The large-signal response in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common-mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1201/LT1202 so that the falling edge slew rate is balanced.

Small-Signal Transient Response



$A_V = 1$

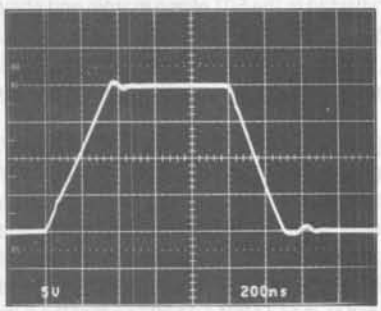
Small-Signal Transient Response



$A_V = -1$

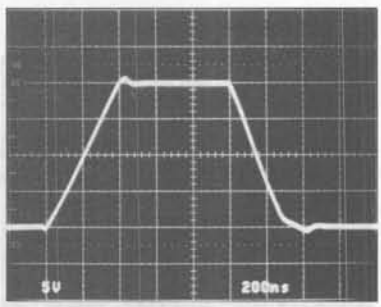
APPLICATIONS INFORMATION

Large-Signal Transient Response



$A_V = 1$

Large-Signal Transient Response



$A_V = -1$

Low Voltage Operation

The LT1201/LT1202 are functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions at room temperature the typical input common-mode range is 2.2V to –1.5V, and a 1MHz, $2.5V_{P-P}$ sine wave can be accurately reproduced. With 5V total supply voltage the gain-bandwidth is reduced to 7MHz and the slew rate is reduced to 20V/µs.

DAC Current-to-Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1201/LT1202 make them well suited for current-to-voltage conversion after current output D/A converters. A typical application with a DAC-08 type converter (full-scale output of 2mA) uses a 5k feedback resistor. A 12pF compensation capacitor across the feedback resistor is used to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1201/LT1202 and DAC settles to less than 40mV (1LSB) in 500ns for a 0V to 10V step or for a 10V to 0V step.

Active Filters

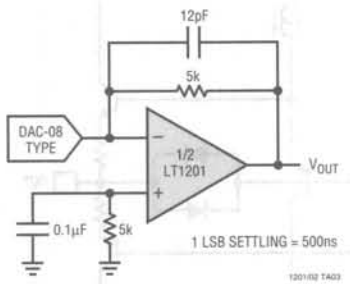
The LT1201/LT1202 are well suited to active filter applications such as the circuit shown on the front page of the data sheet. This particular example is a 4-pole Butterworth lowpass filter with a cutoff frequency of 100kHz. In choosing an amplifier for filter applications a good rule of thumb is:

$$f_0 \times Q < GBW/20$$

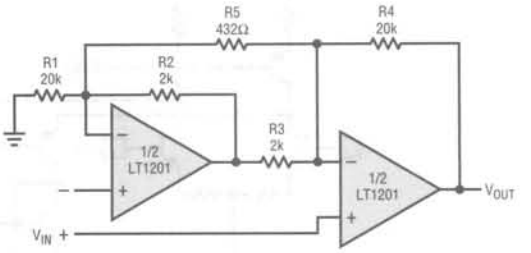
For our example the first section has Q = 0.54 and the second section has Q = 1.31, so the amplifier easily meets the gain-bandwidth requirement of 2.6MHz for f_0 = 100kHz. This multiple feedback configuration and the Sallen-Key configuration (as shown in the Typical Applications section) are the most commonly used topologies. The multiple feedback configuration has an advantage over the noninverting Sallen-Key configuration in many cases because the amplifier does not see a frequency varying common-mode voltage and high frequency output impedance is not critical. The result is better frequency performance beyond f_0 (for our particular example the stopband performance is dramatically better above 1MHz). Advantages of the Sallen-Key topology over the multiple feedback topology include: better gain accuracy, better DC accuracy, and unity-gain filters can be implemented more easily.

TYPICAL APPLICATIONS

DAC Current-to-Voltage Converter



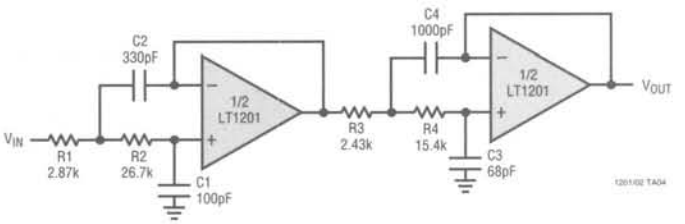
Instrumentation Amplifier



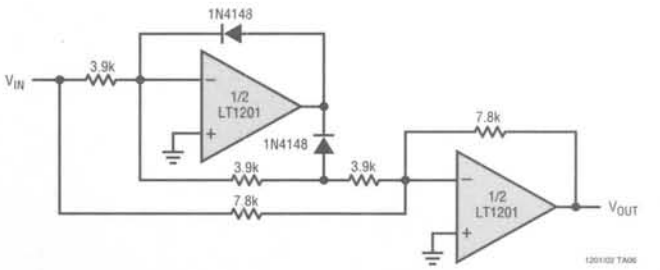
$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 120kHz

100kHz 4th Order Butterworth Filter (Sallen-Key)

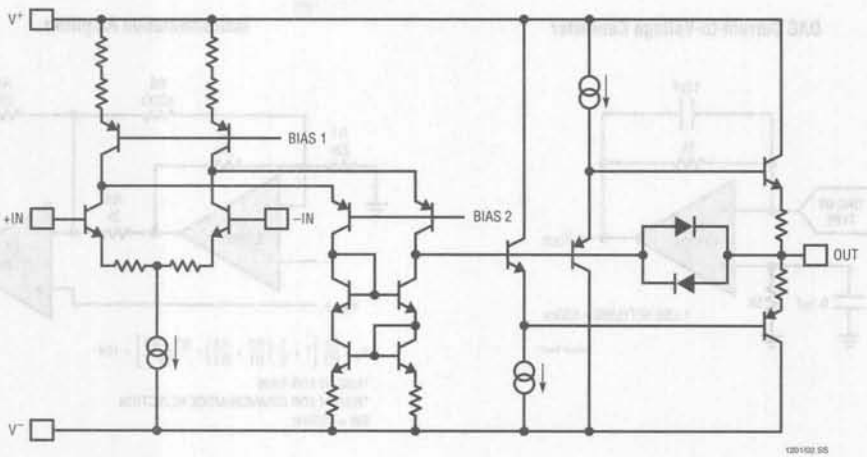


Full-Wave Rectifier



2

SIMPLIFIED SCHEMATIC One amplifier shown.



250mA/60MHz Current Feedback Amplifier

FEATURES

- **250mA Minimum Output Drive Current**
- 60MHz Bandwidth, $A_V = 2$, $R_L = 100\Omega$
- 900V/µs Slew Rate, $A_V = 2$, $R_L = 50\Omega$
- 0.02% Differential Gain, $A_V = 2$, $R_L = 30\Omega$
- 0.17° Differential Phase, $A_V = 2$, $R_L = 30\Omega$
- High Input Impedance, 10MΩ
- Wide Supply Range, ±5V to ±15V
- Shutdown Mode: $I_S < 200\mu A$
- Adjustable Supply Current
- Stable with $C_L = 10{,}000pF$

APPLICATIONS

- Video Amplifiers
- Cable Drivers
- RGB Amplifiers
- Test Equipment Amplifiers
- Buffers

DESCRIPTION

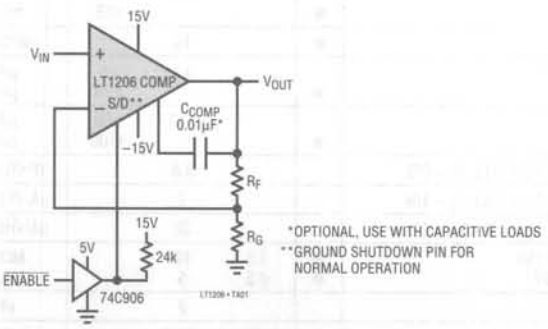
The LT1206 is a current feedback amplifier with high output current drive capability and excellent video characteristics. The LT1206 is stable with large capacitive loads, and can easily supply the large currents required by the capacitive loading. A shutdown feature switches the device into a high impedance, low current mode, reducing dissipation when the device is not in use. For lower bandwidth applications, the supply current can be reduced with a single external resistor. The low differential gain and phase, wide bandwidth, and the 250mA minimum output current drive make the LT1206 well suited to drive multiple cables in video systems.

The LT1206 is manufactured on Linear Technology's proprietary complementary bipolar process.

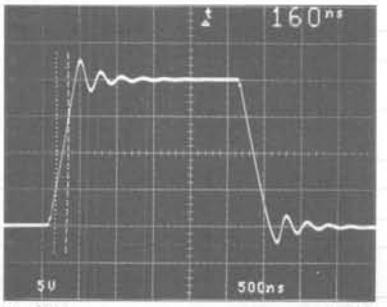
2

TYPICAL APPLICATIONS

Noninverting Amplifier with Shutdown



Large-Signal Response, $C_L = 10{,}000pF$

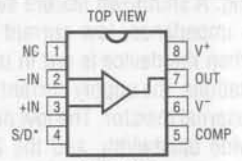


$V_S = \pm 15V$
$R_L = \infty$
$R_F = R_G = 3k$

ABSOLUTE MAXIMUM RATINGS

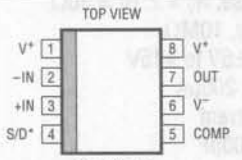
Supply Voltage ..... ±18V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range (Note 2) ..... 0°C to 70°C
Operating Temperature Range
LT1206C ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



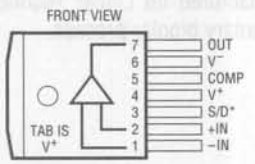
N8 PACKAGE
8-LEAD PLASTIC DIP
θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1206CN8**



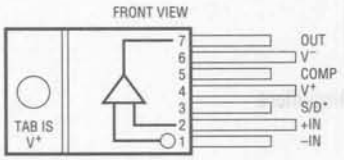
S8 PACKAGE
8-LEAD PLASTIC SO
θ_{JA} = 60°C/W

ORDER PART NUMBER
LT1206CS8**
PART MARKING
1206



R PACKAGE
7-LEAD PLASTIC DD
θ_{JA} = 30°C/W

ORDER PART NUMBER
LT1206CR**



Y PACKAGE
7-LEAD TO-220
θ_{JC} = 5°C/W

ORDER PART NUMBER
LT1206CY**

*Ground shutdown pin for normal operation **See Note 2
Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, $V_{S/D}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN}^+	Noninverting Input Current	T_A = 25°C			±2	±5	µA
			●			±20	µA
I_{IN}^-	Inverting Input Current	T_A = 25°C			±10	±60	µA
			●			±100	µA
e_n	Input Noise Voltage Density	f = 10kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			3.6		nV/√Hz
$+i_n$	Input Noise Current Density	f = 10kHz, R_F = 1k, R_G = 10Ω, R_S = 10k			2		pA/√Hz
$-i_n$	Input Noise Current Density	f = 10kHz, R_F = 1k, R_G = 10Ω, R_S = 10k			30		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±12V, V_S = ±15V	●	1.5	10		MΩ
		V_{IN} = ±2V, V_S = ±5V	●	0.5	5		MΩ
C_{IN}	Input Capacitance	V_S = ±15V			2		pF
	Input Voltage Range	V_S = ±15V	●	±12	±13.5		V
		V_S = ±5V	●	±2	±3.5		V

ELECTRICAL CHARACTERISTICS $V_{CM} = 0, \pm 5V \le V_S \le \pm 15V$, pulse tested, $V_{S/D} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 12V$	●	55	62		dB
		$V_S = \pm 5V$, $V_{CM} = \pm 2V$	●	50	60		dB
	Inverting Input Current Common-Mode Rejection	$V_S = \pm 15V$, $V_{CM} = \pm 12V$	●		0.1	10	μA/V
		$V_S = \pm 5V$, $V_{CM} = \pm 2V$	●		0.1	10	μA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	60	77		dB
	Noninverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		30	500	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		0.7	5	μA/V
A_V	Large-Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 50\Omega$	●	55	71		dB
		$V_S = \pm 5V$, $V_{OUT} = \pm 2V$, $R_L = 25\Omega$	●	55	68		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 50\Omega$	●	100	260		kΩ
		$V_S = \pm 5V$, $V_{OUT} = \pm 2V$, $R_L = 25\Omega$	●	75	200		kΩ
V_{OUT}	Maximum Output Voltage Swing	$V_S = \pm 15V$, $R_L = 50\Omega$, $T_A = 25°C$		±11.5	±12.5		V
			●	±10.0			V
		$V_S = \pm 5V$, $R_L = 25\Omega$, $T_A = 25°C$		±2.5	±3.0		V
			●	±2.0			V
I_{OUT}	Maximum Output Current	$R_L = 1\Omega$	●	250	500	1200	mA
I_S	Supply Current	$V_S = \pm 15V$, $V_{S/D} = 0V$, $T_A = 25°C$			20	30	mA
			●			35	mA
	Supply Current, $R_{S/D} = 51k$ (Note 3)	$V_S = \pm 15V$, $T_A = 25°C$			12	17	mA
	Positive Supply Current, Shutdown	$V_S = \pm 15V$, $V_{S/D} = 15V$	●			200	μA
	Output Leakage Current, Shutdown	$V_S = \pm 15V$, $V_{S/D} = 15V$	●			10	μA
SR	Slew Rate (Note 4)	$A_V = 2$, $T_A = 25°C$		400	900		V/μs
	Differential Gain (Note 5)	$V_S = \pm 15V$, $R_F = 560\Omega$, $R_G = 560\Omega$, $R_L = 30\Omega$			0.02		%
	Differential Phase (Note 5)	$V_S = \pm 15V$, $R_F = 560\Omega$, $R_G = 560\Omega$, $R_L = 30\Omega$			0.17		DEG
BW	Small-Signal Bandwidth	$V_S = \pm 15V$, Peaking ≤ 0.5dB $R_F = R_G = 620\Omega$, $R_L = 100\Omega$			60		MHz
		$V_S = \pm 15V$, Peaking ≤ 0.5dB $R_F = R_G = 649\Omega$, $R_L = 50\Omega$			52		MHz
		$V_S = \pm 15V$, Peaking ≤ 0.5dB $R_F = R_G = 698\Omega$, $R_L = 30\Omega$			43		MHz
		$V_S = \pm 15V$, Peaking ≤ 0.5dB $R_F = R_G = 825\Omega$, $R_L = 10\Omega$			27		MHz

The ● denotes specifications which apply for $0°C \le T_A \le 70°C$.

Note 1: Applies to short circuits to ground only. A short circuit between the output and either supply may permanently damage the part when operated on supplies greater than ±10V.

Note 2: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts tested over –40°C to 85°C are available on special request. Consult factory.

Note 3: $R_{S/D}$ is connected between the shutdown pin and ground.

Note 4: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with $R_F = 1.5k$, $R_G = 1.5k$ and $R_L = 400\Omega$.

Note 5: NTSC composite video with an output level of 2V.

SMALL-SIGNAL BANDWIDTH

I_S = 20mA Typical, Peaking ≤ 0.1dB

A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±5V, R_{SD} = 0Ω					
−1	150	562	562	48	21.4
	30	649	649	34	17
	10	732	732	22	12.5
1	150	619	–	54	22.3
	30	715	–	36	17.5
	10	806	–	22.4	11.5
2	150	576	576	48	20.7
	30	649	649	35	18.1
	10	750	750	22.4	11.7
10	150	442	48.7	40	19.2
	30	511	56.2	31	16.5
	10	649	71.5	20	10.2

A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±15V, R_{SD} = 0Ω					
−1	150	681	681	50	19.2
	30	768	768	35	17
	10	887	887	24	12.3
1	150	768	–	66	22.4
	30	909	–	37	17.5
	10	1k	–	23	12
2	150	665	665	55	23
	30	787	787	36	18.5
	10	931	931	22.5	11.8
10	150	487	536	44	20.7
	30	590	64.9	33	17.5
	10	768	84.5	20.7	10.8

I_S = 10mA Typical, Peaking ≤ 0.1dB

A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±5V, R_{SD} = 10.2k					
−1	150	576	576	35	17
	30	681	681	25	12.5
	10	750	750	16.4	8.7
1	150	665	–	37	17.5
	30	768	–	25	12.6
	10	845	–	16.5	8.2
2	150	590	590	35	16.8
	30	681	681	25	13.4
	10	768	768	16.2	8.1
10	150	301	33.2	31	15.6
	30	392	43.2	23	11.9
	10	499	54.9	15	7.8

A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±15V, R_{SD} = 60.4k					
−1	150	634	634	41	19.1
	30	768	768	26.5	14
	10	866	866	17	9.4
1	150	768	–	44	18.8
	30	909	–	28	14.4
	10	1k	–	16.8	8.3
2	150	649	649	40	18.5
	30	787	787	27	14.1
	10	931	931	16.5	8.1
10	150	301	33.2	33	15.6
	30	402	44.2	25	13.3
	10	590	64.9	15.3	7.4

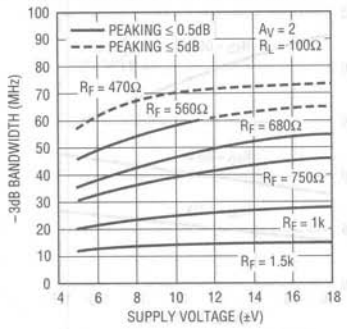
I_S = 5mA Typical, Peaking ≤ 0.1dB

A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±5V, R_{SD} = 22.1k					
−1	150	604	604	21	10.5
	30	715	715	14.6	7.4
	10	681	681	10.5	6.0
1	150	768	–	20	9.6
	30	866	–	14.1	6.7
	10	825	–	9.8	5.1
2	150	634	634	20	9.6
	30	750	750	14.1	7.2
	10	732	732	9.6	5.1
10	150	100	11.1	16.2	5.8
	30	100	11.1	13.4	7.0
	10	100	11.1	9.5	4.7

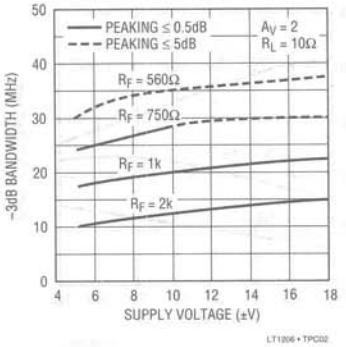
A_V	R_L	R_F	R_G	−3dB BW (MHz)	−0.1dB BW (MHz)
V_S = ±15V, R_{SD} = 121k					
−1	150	619	619	25	12.5
	30	787	787	15.8	8.5
	10	825	825	10.5	5.4
1	150	845	–	23	10.6
	30	1k	–	15.3	7.6
	10	1k	–	10	5.2
2	150	681	681	23	10.2
	30	845	845	15	7.7
	10	866	866	10	5.4
10	150	100	11.1	15.9	4.5
	30	100	11.1	13.6	6
	10	100	11.1	9.6	4.5

TYPICAL PERFORMANCE CHARACTERISTICS

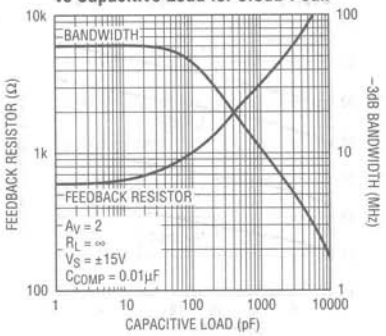
Bandwidth vs Supply Voltage



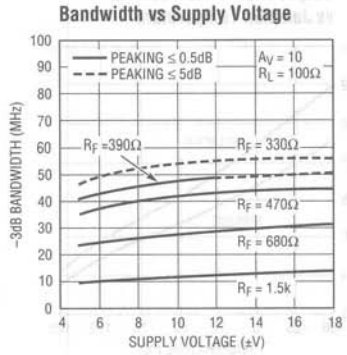
Bandwidth vs Supply Voltage



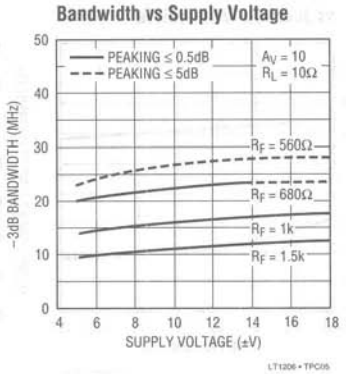
Bandwidth and Feedback Resistance vs Capacitive Load for 0.5dB Peak



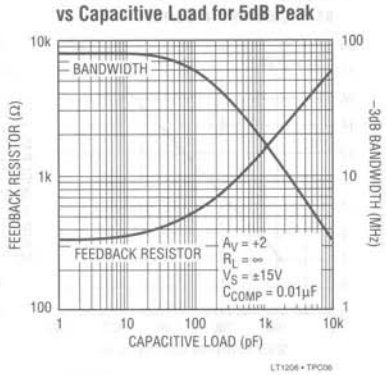
Bandwidth vs Supply Voltage



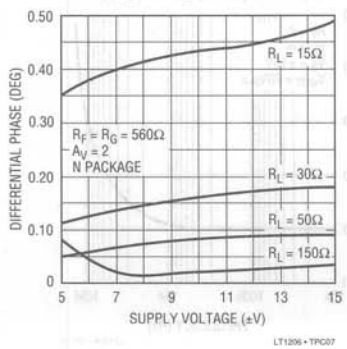
Bandwidth vs Supply Voltage



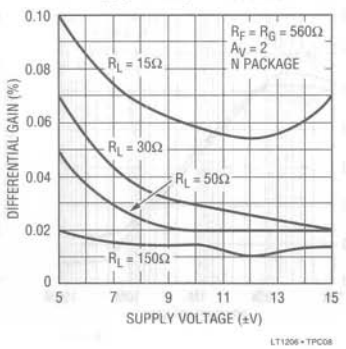
Bandwidth and Feedback Resistance vs Capacitive Load for 5dB Peak



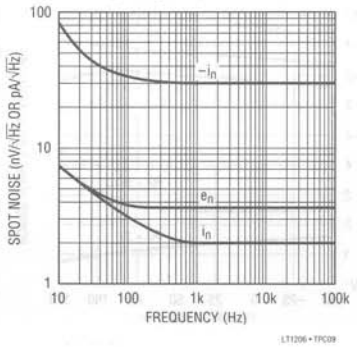
Differential Phase vs Supply Voltage



Differential Gain vs Supply Voltage



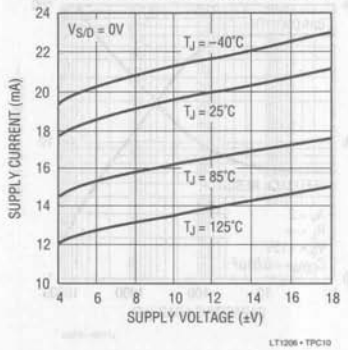
Spot Noise Voltage and Current vs Frequency



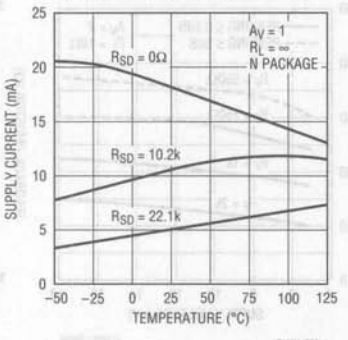
2

TYPICAL PERFORMANCE CHARACTERISTICS

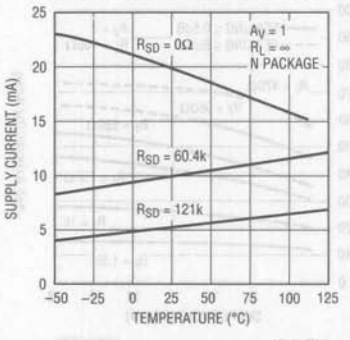
Supply Current vs Supply Voltage



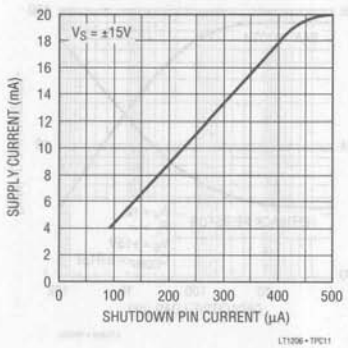
Supply Current vs Ambient Temperature, V_S = ±5V



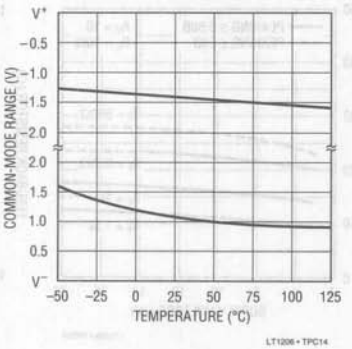
Supply Current vs Ambient Temperature, V_S = ±15V



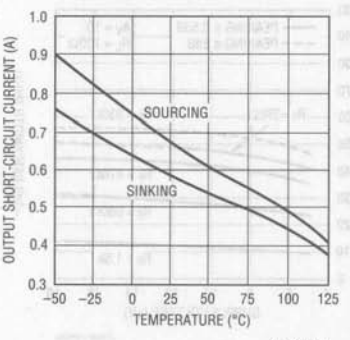
Supply Current vs Shutdown Pin Current



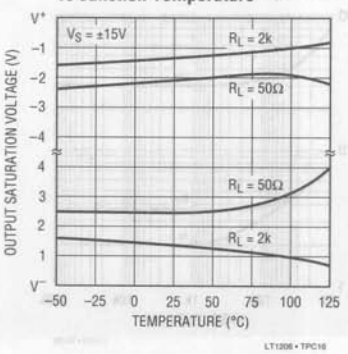
Input Common-Mode Limit vs Junction Temperature



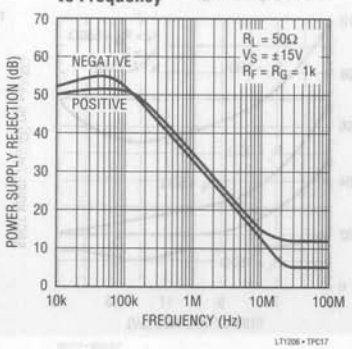
Output Short-Circuit Current vs Junction Temperature



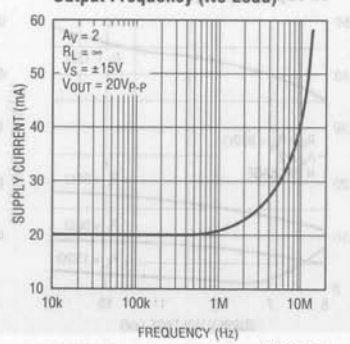
Output Saturation Voltage vs Junction Temperature



Power Supply Rejection Ratio vs Frequency

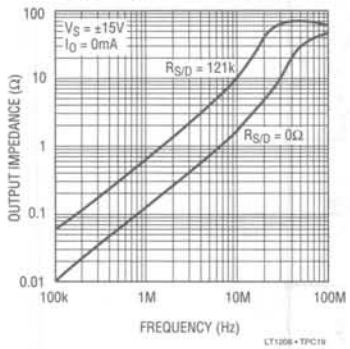


Supply Current vs Large Signal Output Frequency (No Load)

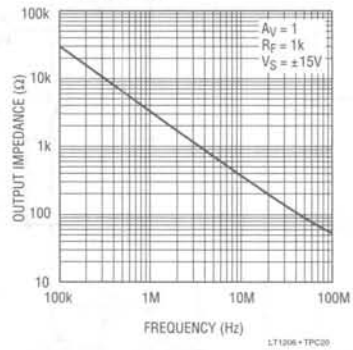


TYPICAL PERFORMANCE CHARACTERISTICS

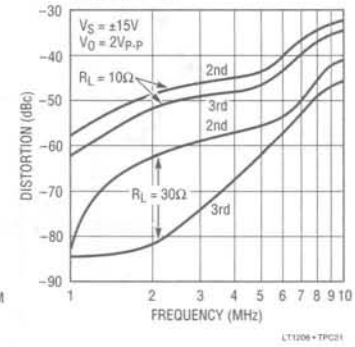
Output Impedance vs Frequency



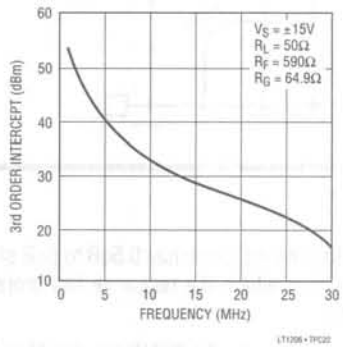
Output Impedance in Shutdown vs Frequency



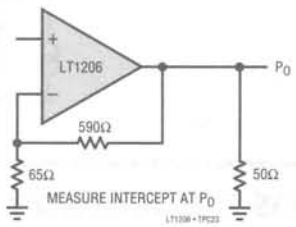
2nd and 3rd Harmonic Distortion vs Frequency



3rd Order Intercept vs Frequency

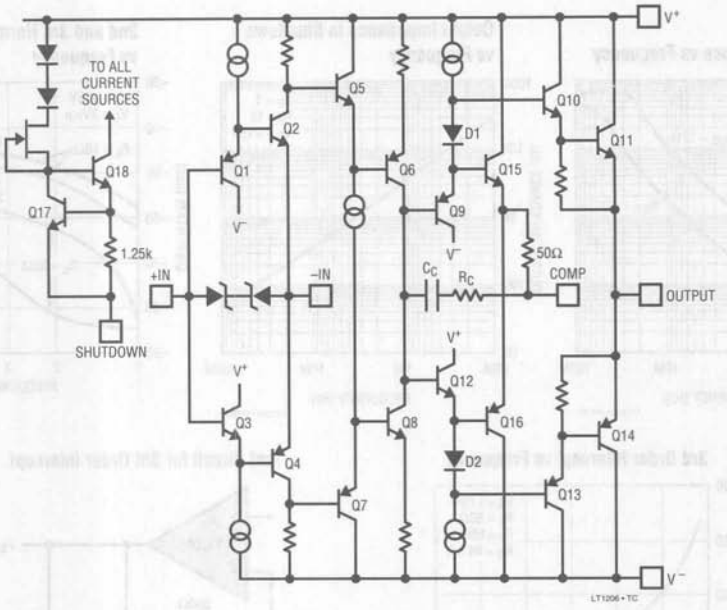


Test Circuit for 3rd Order Intercept



2

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

The LT1206 is a current feedback amplifier with high output current drive capability. The device is stable with large capacitive loads and can easily supply the high currents required by capacitive loads. The amplifier will drive low impedance loads such as cables with excellent linearity at high frequencies.

Feedback Resistor Selection

The optimum value for the feedback resistors is a function of the operating conditions of the device, the load impedance and the desired flatness of response. The Typical AC Performance tables give the values which result in the highest 0.1dB and 0.5dB bandwidths for various resistive loads and operating conditions. If this level of flatness is not required, a higher bandwidth can be obtained by use of a lower feedback resistor. The characteristic curves of Bandwidth vs Supply Voltage indicate feedback resistors for peaking up to 5dB. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

For resistive loads, the COMP pin should be left open (see section on capacitive loads).

Capacitive Loads

The LT1206 includes an optional compensation network for driving capacitive loads. This network eliminates most of the output stage peaking associated with capacitive loads, allowing the frequency response to be flattened. Figure 1 shows the effect of the network on a 200pF load. Without the optional compensation, there is a 5dB peak at 40MHz caused by the effect of the capacitance on the output stage. Adding a 0.01μF bypass capacitor between the output and the COMP pins connects the compensation and completely eliminates the peaking. A lower value feedback resistor can now be used, resulting in a response

APPLICATIONS INFORMATION

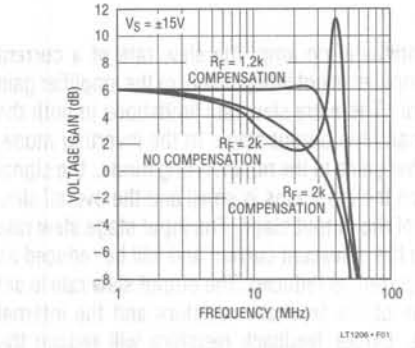


Figure 1.

which is flat to 0.35dB to 30MHz. The network has the greatest effect for C_L in the range of 0pF to 1000pF. The graph of Maximum Capacitive Load vs Feedback Resistor can be used to select the appropriate value of feedback resistor. The values shown are for 0.5dB and 5dB peaking at a gain of 2 with no resistive load. This is a worst case condition, as the amplifier is more stable at higher gains and with some resistive load in parallel with the capacitance. Also shown is the –3dB bandwidth with the suggested feedback resistor vs the load capacitance.

Although the optional compensation works well with capacitive loads, it simply reduces the bandwidth when it is connected with resistive loads. For instance, with a 30Ω load, the bandwidth drops from 55MHz to 35MHz when the compensation is connected. Hence, the compensation was made optional. To disconnect the optional compensation, leave the COMP pin open.

Shutdown/Current Set

If the shutdown feature is not used, the SHUTDOWN pin must be connected to ground or V^-.

The shutdown pin can be used to either turn off the biasing for the amplifier, reducing the quiescent current to less than 200µA, or to control the quiescent current in normal operation.

The total bias current in the LT1206 is controlled by the current flowing out of the shutdown pin. When the shutdown pin is open or driven to the positive supply, the part is shut down. In the shutdown mode, the output looks like a 40pF capacitor and the supply current is typically 100µA. The shutdown pin is referenced to the positive supply through an internal bias circuit (see the simplified schematic). An easy way to force shutdown is to use open drain (collector) logic. The circuit shown in Figure 2 uses a 74C904 buffer to interface between 5V logic and the LT1206. The switching time between the active and shutdown states is less than 1µs. A 24k pull-up resistor speeds up the turn-off time and insures that the LT1206 is completely turned off. Because the pin is referenced to the positive supply, the logic used should have a breakdown voltage of greater than the positive supply voltage. No other circuitry is necessary as the internal circuit limits the shutdown pin current to about 500µA. Figure 3 shows the resulting waveforms.

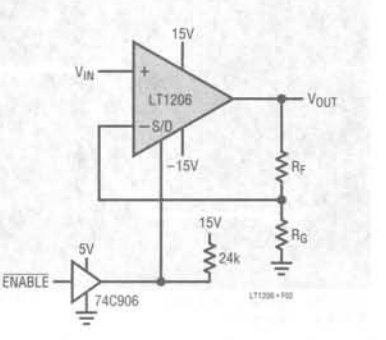


Figure 2. Shutdown Interface

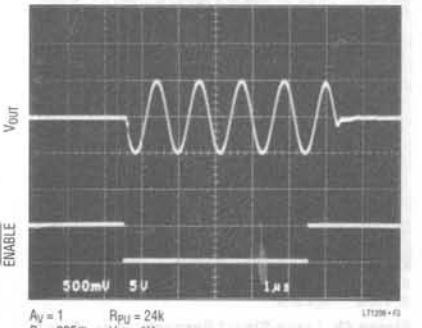
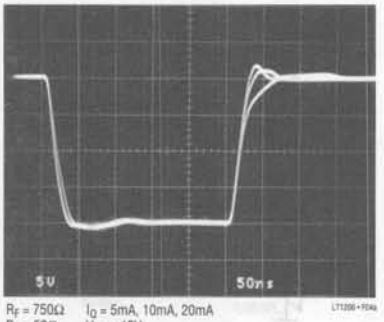


Figure 3. Shutdown Operation

APPLICATIONS INFORMATION

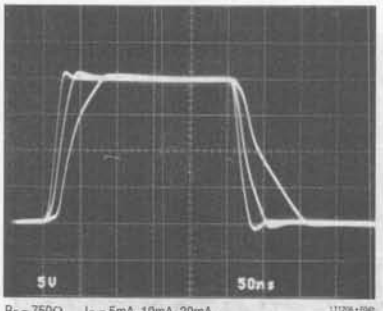
For applications where the full bandwidth of the amplifier is not required, the quiescent current of the device may be reduced by connecting a resistor from the shutdown pin to ground. The quiescent current will be approximately 40 times the current in the shutdown pin. The voltage across the resistor in this condition is $V^+ - 3V_{BE}$. For example, a 60k resistor will set the quiescent supply current to 10mA with $V_S = \pm 15V$.

The photos (Figures 4a and 4b) show the effect of reducing the quiescent supply current on the large-signal response. The quiescent current can be reduced to 5mA in the inverting configuration without much change in response. In noninverting mode, however, the slew rate is reduced as the quiescent current is reduced.



$R_F = 750\Omega$ $I_Q = 5mA, 10mA, 20mA$
$R_L = 50\Omega$ $V_S = \pm 15V$

Figure 4a. Large-Signal Response vs I_Q, $A_V = -1$

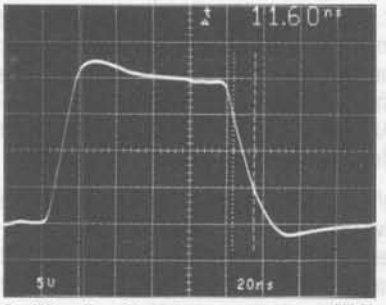


$R_F = 750\Omega$ $I_Q = 5mA, 10mA, 20mA$
$R_L = 50\Omega$ $V_S = \pm 15V$

Figure 4b. Large-Signal Response vs I_Q, $A_V = 2$

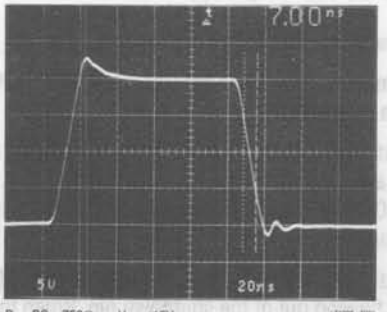
Slew Rate

Unlike a traditional op amp, the slew rate of a current feedback amplifier is not independent of the amplifier gain configuration. There are slew rate limitations in both the input stage and the output stage. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude on the input pins is small and the overall slew rate is that of the output stage. The input stage slew rate is related to the quiescent current and will be reduced as the supply current is reduced. The output slew rate is set by the value of the feedback resistors and the internal capacitance. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced. The photos (Figures 5a, 5b and 5c) show the large-signal response of the LT1206 for various gain configurations. The slew rate varies from 860V/µs for a gain of 1, to 1400V/µs for a gain of –1.



$R_F = 825\Omega$ $V_S = \pm 15V$
$R_L = 50\Omega$

Figure 5a. Large-Signal Response, $A_V = 1$



$R_F = RG = 750\Omega$ $V_S = \pm 15V$
$R_L = 50\Omega$

Figure 5b. Large-Signal Response, $A_V = -1$

APPLICATIONS INFORMATION

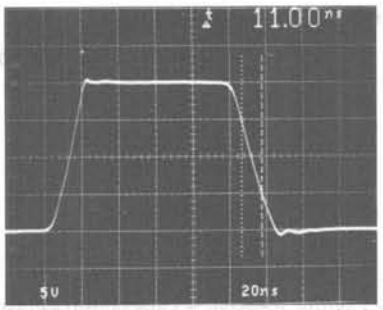


Figure 5c. Large-Signal Response, A_V = 2

When the LT1206 is used to drive capacitive loads, the available output current can limit the overall slew rate. In the fastest configuration, the LT1206 is capable of a slew rate of over 1V/ns. The current required to slew a capacitor at this rate is 1mA per picofarad of capacitance, so 10,000pF would require 10A! The photo (Figure 6) shows the large signal behavior with C_L = 10,000pF. The slew rate is about 60V/µs, determined by the current limit of 600mA.

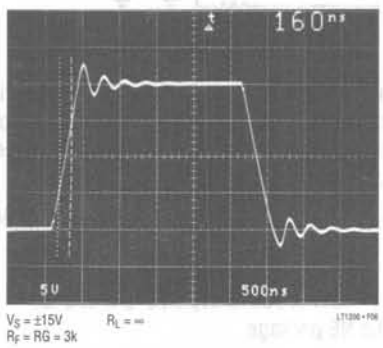


Figure 6. Large-Signal Response, C_L = 10,000pF

Differential Input Signal Swing

The differential input swing is limited to about ±6V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect; however, in the shutdown mode the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage. To allow for some margin, it is recommended that the input signal be less than ±5V when the device is shut down.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier.

Power Supplies

The LT1206 will operate from single or split supplies from ±5V (10V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 500µV per volt of supply mismatch. The inverting bias current can change as much as 5µA per volt of supply mismatch, though typically the change is less than 0.5µA per volt.

Thermal Considerations

The LT1206 contains a thermal shutdown feature which protects against excessive internal (junction) temperature. If the junction temperature of the device exceeds the protection threshold, the device will begin cycling between normal operation and an off state. The cycling is not harmful to the part. The thermal cycling occurs at a slow rate, typically 10ms to several seconds, which depends on the power dissipation and the thermal time constants of the package and heat sinking. Raising the ambient temperature until the device begins thermal shutdown gives a good indication of how much margin there is in the thermal design.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PCB material can be very effective at transmitting heat between the pad area attached to the tab of the device, and a ground or

APPLICATIONS INFORMATION

power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PCB material is high, the length/area ratio of the thermal resistance between the layer is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by the device.

Tables 1 and 2 list thermal resistance for each package. For the TO-220 package, thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different board sizes and copper areas are listed for each surface mount package. All measurements were taken in still air on 3/32" FR-4 board with 1oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape.

Table 1. R Package, 7-Lead DD

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	25°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	27°C/W
125 sq. mm	2500 sq. mm	2500 sq. mm	35°C/W

*Tab of device attached to topside copper

Table 2. S8 Package, 8-Lead Plastic SOIC

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	60°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	62°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	65°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	69°C/W
100 sq. mm	1000 sq. mm	2500 sq. mm	73°C/W
100 sq. mm	225 sq. mm	2500 sq. mm	80°C/W
100 sq. mm	100 sq. mm	2500 sq. mm	83°C/W

*Pins 1 and 8 attached to topside copper

Y Package, 7-Lead TO-220
Thermal Resistance (Junction-to-Case) = 5°C/W

N8 Package, 8-Lead DIP
Thermal Resistance (Junction-to-Ambient) = 100°C/W

Calculating Junction Temperature

The junction temperature can be calculated from the equation:

$$T_J = (P_D \times \theta_{JA}) + T_A$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Device Dissipation
θ_{JA} = Thermal Resistance (Junction-to Ambient)

As an example, calculate the junction temperature for the circuit in Figure 7 for the N8, S8, and R packages assuming a 70°C ambient temperature.

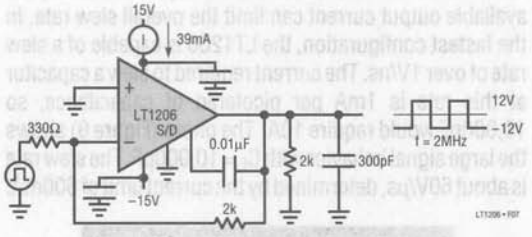


Figure 7. Thermal Calculation Example

The device dissipation can be found by measuring the supply currents, calculating the total dissipation, and then subtracting the dissipation in the load and feedback network.

$$P_D = (39mA \times 30V) - (12V)^2/(2k||2k) = 1.03W$$

Then:

$T_J = (1.03W \times 100°C/W) + 70°C = 173°C$
for the N8 package

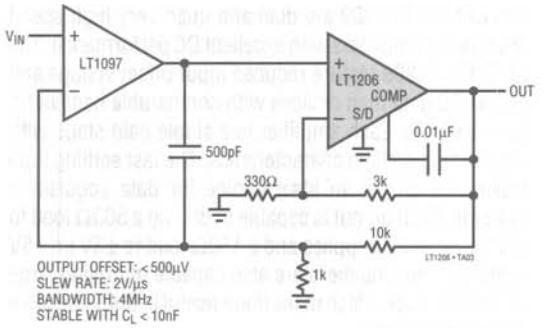
$T_J = (1.03W \times 65°C/W) \times + 70°C = 137°C$
for the S8 with 225 sq. mm topside heat sinking

$T_J = (1.03W \times 35°C/W) \times + 70°C = 106°C$
for the R package with 100 sq. mm topside heat sinking

Since the Maximum Junction Temperature is 150°C, the N8 package is clearly unacceptable. Both the S8 and R packages are usable.

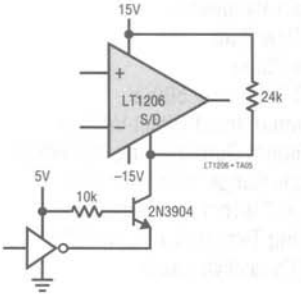
TYPICAL APPLICATIONS

Precision ×10 Hi Current Amplifier

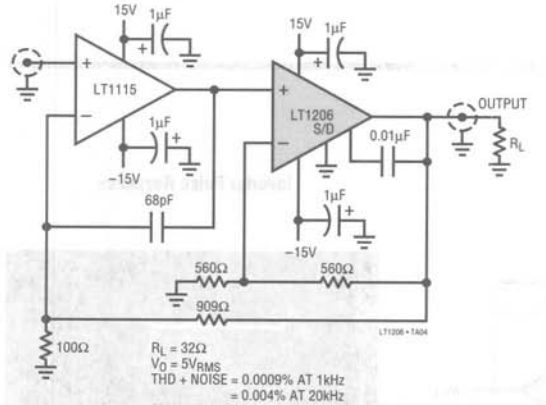


OUTPUT OFFSET: < 500µV
SLEW RATE: 2V/µs
BANDWIDTH: 4MHz
STABLE WITH C_L < 10nF

CMOS Logic to Shutdown Interface

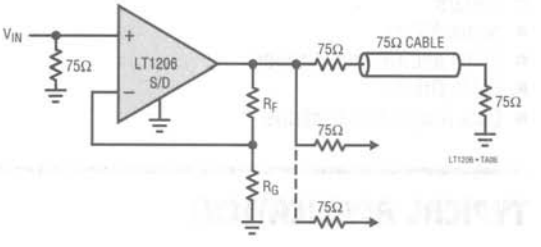


Low Noise ×10 Buffered Line Driver

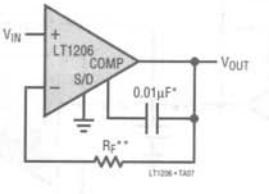


R_L = 32Ω
V_O = $5V_{RMS}$
THD + NOISE = 0.0009% AT 1kHz
= 0.004% AT 20kHz
SMALL SIGNAL 0.1dB BANDWIDTH = 600kHz

Distribution Amplifier



Buffer A_V = 1



*OPTIONAL, USE WITH CAPACITIVE LOADS
**VALUE OF R_F DEPENDS ON SUPPLY VOLTAGE AND LOADING. SELECT FROM TYPICAL AC PERFORMANCE TABLE OR DETERMINE EMPIRICALLY

2

Dual and Quad 45MHz, 400V/µs Op Amps

FEATURES

- 45MHz Gain-Bandwidth
- 400V/µs Slew Rate
- Unity-Gain Stable
- 7V/mV DC Gain, R_L = 500Ω
- 3mV Maximum Input Offset Voltage
- ±12V Minimum Output Swing into 500Ω
- Wide Supply Range: ±2.5V to ±15V
- 7mA Supply Current per Amplifier
- 90ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

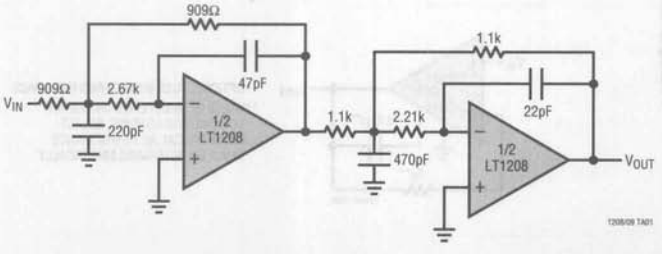
DESCRIPTION

The LT1208/LT1209 are dual and quad very high speed operational amplifiers with excellent DC performance. The LT1208/LT1209 feature reduced input offset voltage and higher DC gain than devices with comparable bandwidth and slew rate. Each amplifier is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. Each output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are also capable of driving large capacitive loads which make them useful in buffer or cable driver applications.

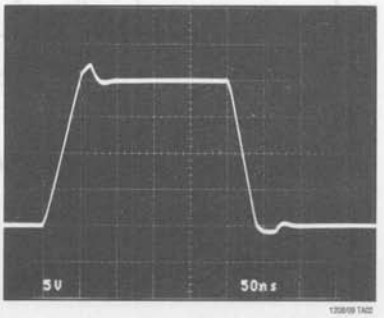
The LT1208/LT1209 are members of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

TYPICAL APPLICATION

1MHz, 4th Order Butterworth Filter



Inverter Pulse Response

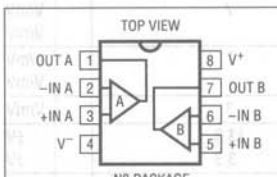


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
LT1208C/LT1209C ..... –40°C to 85°C

Maximum Junction Temperature
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

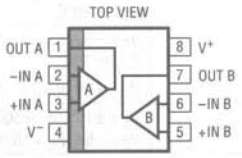


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1208CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

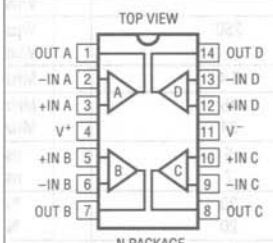
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1208CS8

S8 PART MARKING

1208

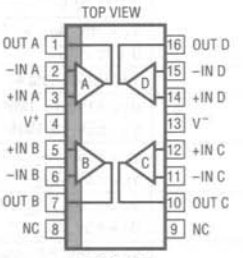


N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1209CN



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1209CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, R_L = 1k, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = ±5V (Note 2)			0.5	3.0	mV
		0°C to 70°C	●			4.0	mV
		V_S = ±15V (Note 2)			1.0	5.0	mV
		0°C to 70°C	●			6.0	mV
	Input V_{OS} Drift				25		µV/°C
I_{OS}	Input Offset Current	V_S = ±5V and V_S = ±15V			100	400	nA
		0°C to 70°C	●			600	nA
I_B	Input Bias Current	V_S = ±5V and V_S = ±15V			4	8	µA
		0°C to 70°C	●			9	µA
e_n	Input Noise Voltage	f = 10kHz			22		nV/√Hz
i_n	Input Noise Current	f = 10kHz			1.1		pA/√Hz

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 1k$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$		12	40		MΩ
		Differential			250		kΩ
C_{IN}	Input Capacitance				2		pF
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 12V$; $V_S = \pm 5V$,		86	98		dB
		$V_{CM} = \pm 2.5V$, 0°C to 70°C	●	83			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$		76	84		dB
		0°C to 70°C	●	75			dB
	Input Voltage Range	$V_S = \pm 15V$		±12	±13		V
		$V_S = \pm 5V$		±2.5	±3		V
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 500\Omega$		3.3	7		V/mV
		0°C to 70°C	●	2.5			V/mV
		$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$		2.5	7		V/mV
		0°C to 70°C	●	2.0			V/mV
		$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$			3		V/mV
V_{OUT}	Output Swing	$V_S = \pm 15V$, $R_L = 500\Omega$, 0°C to 70°C	●	12.0	13.3		±V
		$V_S = \pm 5V$, $R_L = 150\Omega$, 0°C to 70°C	●	3.0	3.3		±V
I_{OUT}	Output Current	$V_S = \pm 15V$, $V_{OUT} = \pm 12V$, 0°C to 70°C	●	24	40		mA
		$V_S = \pm 5V$, $V_{OUT} = \pm 3V$, 0°C to 70°C	●	20	40		mA
SR	Slew Rate	$V_S = \pm 15V$, $A_{VCL} = -2$, (Note 3)		250	400		V/µs
		0°C to 70°C	●	200			V/µs
		$V_S = \pm 5V$, $A_{VCL} = -2$, (Note 3)		150	250		V/µs
		0°C to 70°C	●	130			V/µs
	Full Power Bandwidth	10V Peak, (Note 4)			6.4		MHz
GBW	Gain-Bandwidth	$V_S = \pm 15V$, f = 1MHz			45		MHz
		$V_S = \pm 5V$, f = 1MHz			34		MHz
t_r, t_f	Rise Time, Fall Time	$V_S = \pm 15V$, $A_{VCL} = 1$, 10% to 90%, 0.1V			5		ns
		$V_S = \pm 5V$, $A_{VCL} = 1$, 10% to 90%, 0.1V			7		ns
	Overshoot	$V_S = \pm 15V$, $A_{VCL} = 1$, 0.1V			30		%
		$V_S = \pm 5V$, $A_{VCL} = 1$, 0.1V			20		%
	Propagation Delay	$V_S = \pm 15V$, 50% V_{IN} to 50%V_{OUT}			5		ns
		$V_S = \pm 5V$, 50% V_{IN} to 50%V_{OUT}			7		ns
t_s	Settling Time	$V_S = \pm 15V$, 10V Step, $V_S = \pm 5V$,			90		ns
		5V Step, 0.1%					
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$			1.30		%
		f = 3.58MHz, $R_L = 1k$			0.09		%
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$			1.8		Deg
		f = 3.58MHz, $R_L = 1k$			0.1		Deg
R_O	Output Resistance	$A_{VCL} = 1$, f = 1MHz			2.5		Ω
	Crosstalk	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$			−100	−94	dB
I_S	Supply Current	Each Amplifier, $V_S = \pm 5V$ and $V_S = \pm 15V$			7	9	mA
		0°C to 70°C	●			10.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

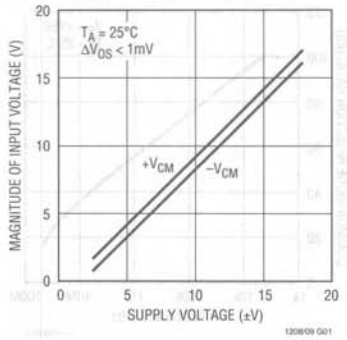
Note 2: Input offset voltage is tested with automated test equipment and is exclusive of warm-up drift.

Note 3: Slew rate is measured in a gain of −2. For ±15V supplies measure between ±10V on the output with ±6V on the input. For ±5V supplies measure between ±2V on the output with ±1.75V on the input.

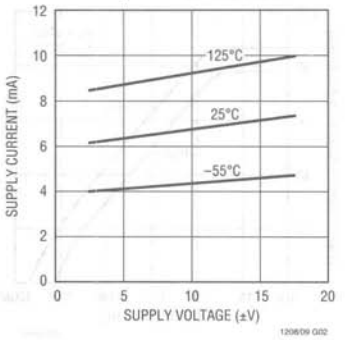
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

TYPICAL PERFORMANCE CHARACTERISTICS

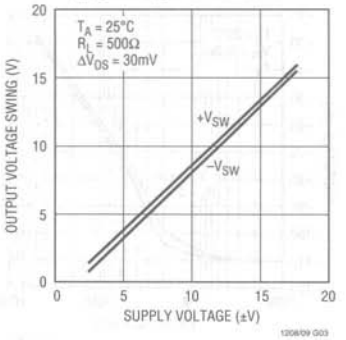
Input Common-Mode Range vs Supply Voltage



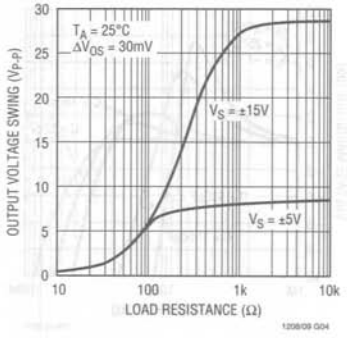
Supply Current vs Supply Voltage and Temperature



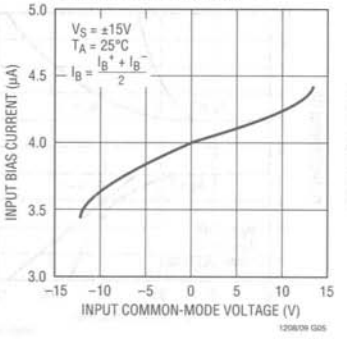
Output Voltage Swing vs Supply Voltage



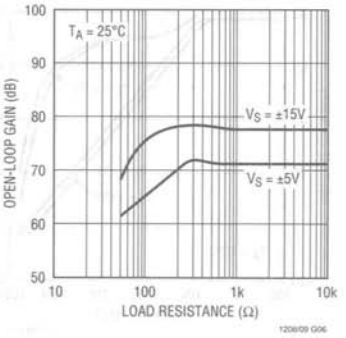
Output Voltage Swing vs Resistive Load



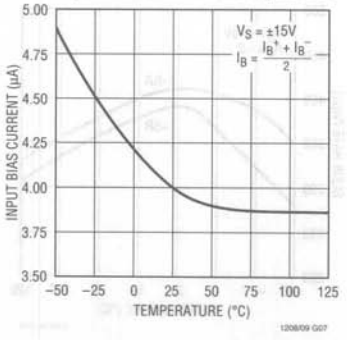
Input Bias Current vs Input Common-Mode Voltage



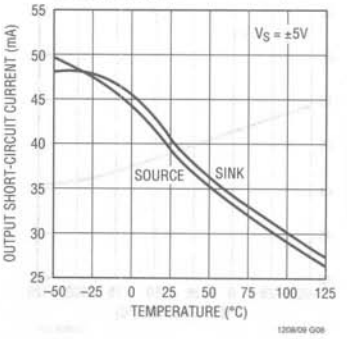
Open-Loop Gain vs Resistive Load



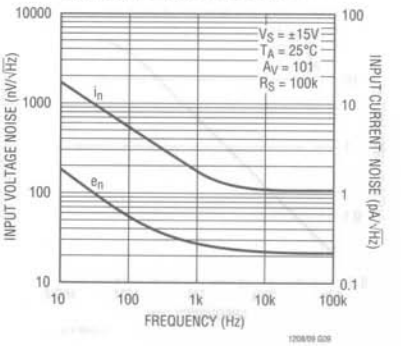
Input Bias Current vs Temperature



Output Short-Circuit Current vs Temperature



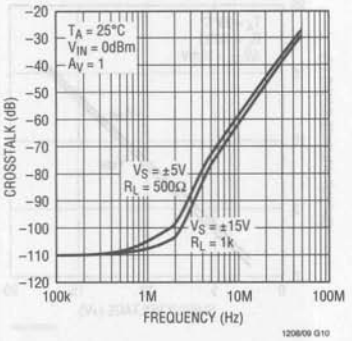
Input Noise Spectral Density



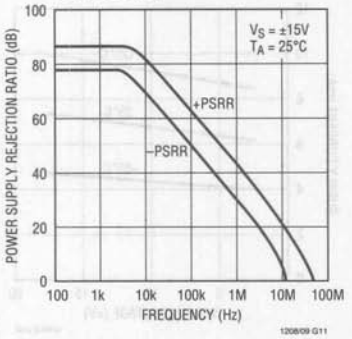
2

TYPICAL PERFORMANCE CHARACTERISTICS

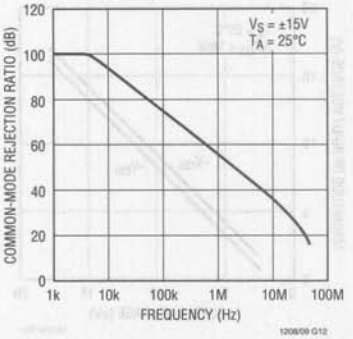
Crosstalk vs Frequency



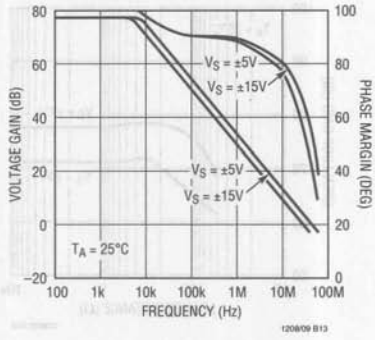
Power Supply Rejection Ratio vs Frequency



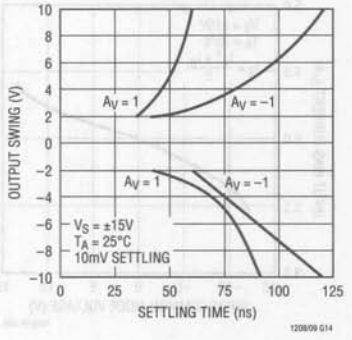
Common-Mode Rejection Ratio vs Frequency



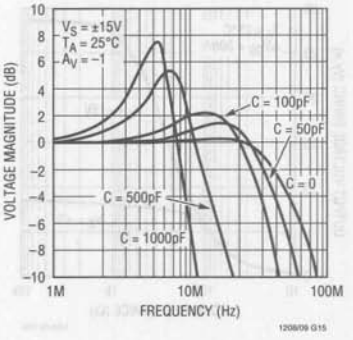
Voltage Gain and Phase vs Frequency



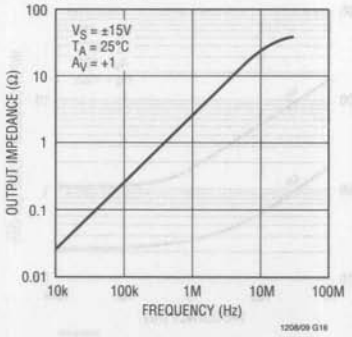
Output Swing vs Settling Time



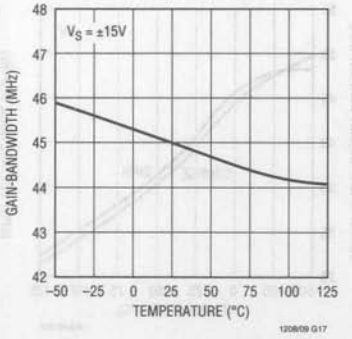
Frequency Response vs Capacitive Load



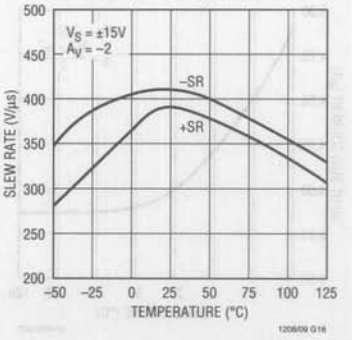
Closed-Loop Output Impedance vs Frequency



Gain-Bandwidth vs Temperature

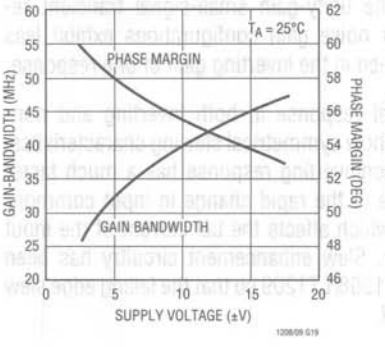


Slew Rate vs Temperature

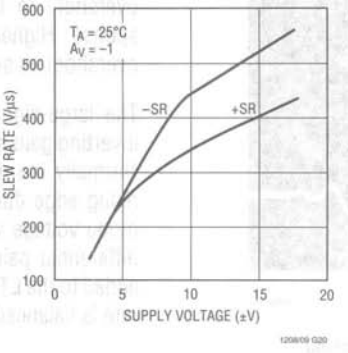


TYPICAL PERFORMANCE CHARACTERISTICS

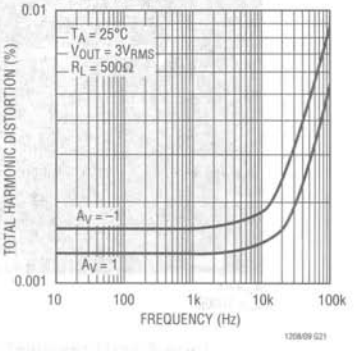
Gain-Bandwidth and Phase Margin vs Supply Voltage



Slew Rate vs Supply Voltage



Total Harmonic Distortion vs Frequency



2

APPLICATIONS INFORMATION

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F \geq R_G \times C_{IN}/R_F$$

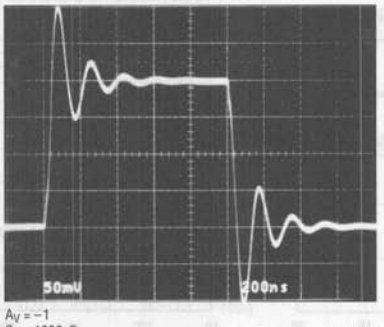
should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1208/LT1209 amplifiers are stable with capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small-signal response with 1000pF load shows 50% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current. To reduce peaking with capacitive loads, insert a small decoupling resistor between the output and the load, and add a capacitor between the output and inverting input to provide an AC feedback path. Coaxial cable can be driven directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

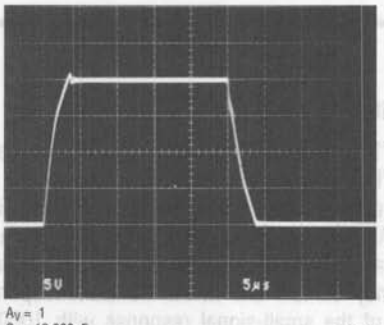
APPLICATIONS INFORMATION

Small-Signal Capacitive Loading



$A_V = -1$
$C_L = 1000pF$

Large-Signal Capacitive Loading



$A_V = 1$
$C_L = 10,000pF$

Input Considerations

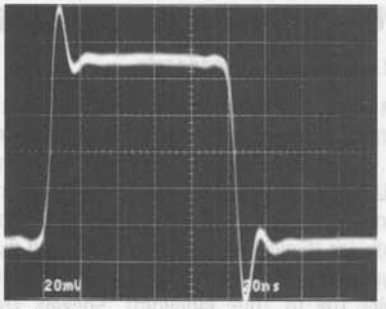
Resistors in series with the inputs are recommended for the LT1208/LT1209 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

Transient Response

The LT1208/LT1209 gain-bandwidth is 45MHz when measured at 100kHz. The actual frequency response in unity-gain is considerably higher than 45MHz due to peaking caused by a second pole beyond the unity-gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity-gain small-signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

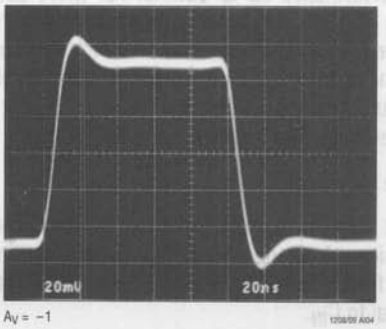
The large-signal response in both inverting and noninverting gain show symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common-mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1208/LT1209 so that the falling edge slew rate is balanced.

Small-Signal Transient Response



$A_V = 1$

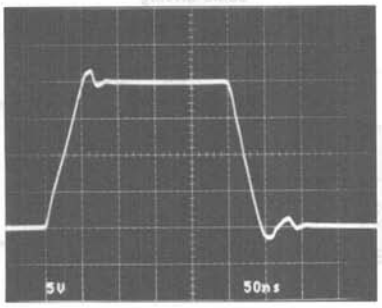
Small-Signal Transient Response



$A_V = -1$

APPLICATIONS INFORMATION

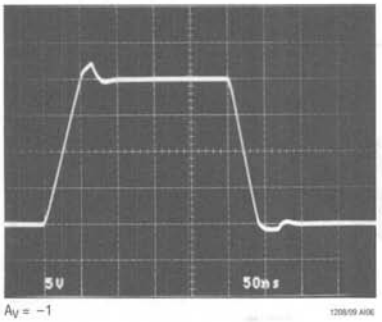
Large-Signal Transient Response



$A_V = 1$

1208/09 A05

Large-Signal Transient Response



$A_V = -1$

1208/09 A06

Low Voltage Operation

The LT1208/LT1209 are functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions, at room temperature, the typical input common-mode range is 1.9V to –1.3V (for a V_{OS} change of 1mV), and a 5MHz, $2V_{P-P}$ sine wave can be faithfully reproduced. With 5V total supply voltage the gain-bandwidth is reduced to 26MHz and the slew rate is reduced to 135V/µs.

Power Dissipation

The LT1208/LT1209 combine high speed and large output current drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions.

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1208CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1208CS8: $T_J = T_A + (P_D \times 150°C/W)$
LT1209CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1209CS: $T_J = T_A + (P_D \times 100°C/W)$

Maximum power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage).

For each amplifier P_{DMAX} is as follows:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + \frac{(0.5V^+)^2}{R_L}$$

Example: LT1208 in S8 at 70°C, $V_S = \pm 10V$, $R_L = 500\Omega$

$$P_{DMAX} = (20V)(10.5mA) + \frac{(5V)^2}{500\Omega} = 260mW$$

$$T_J = 70°C + (2 \times 260mW)(150°C/W) = 148°C$$

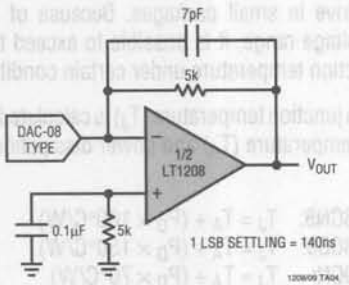
DAC Current-to-Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1208/LT1209 make them well-suited for current-to-voltage conversion after current output D/A converters. A typical application with a DAC-08 type converter (full-scale output of 2mA) uses a 5k feedback resistor. A 7pF compensation capacitor across the feedback resistor is used to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1208/LT1209 and DAC settles to less than 40mV (1LSB) in 140ns for a 10V step.

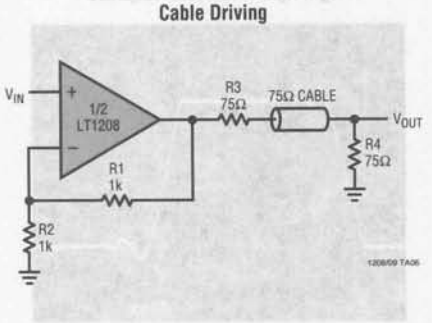
2

TYPICAL APPLICATIONS

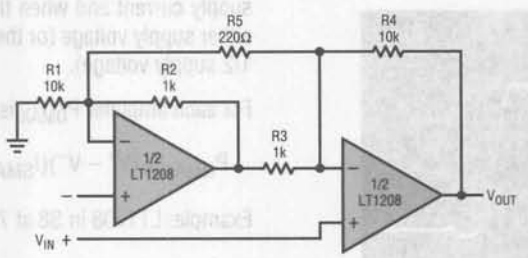
DAC Current-to-Voltage Converter



Cable Driving



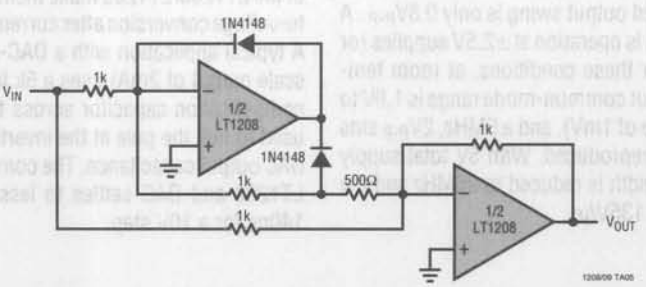
Instrumentation Amplifier



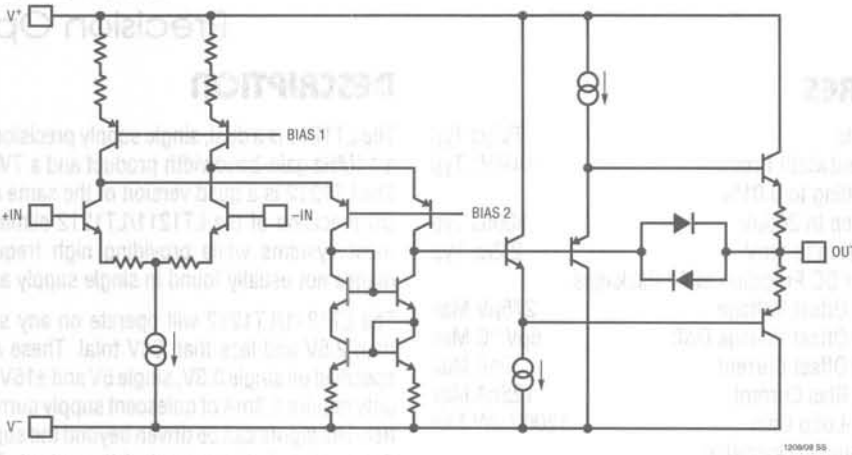
$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 430kHz

Full-Wave Rectifier



SIMPLIFIED SCHEMATIC



14MHz, 7V/µs, Single Supply Dual and Quad Precision Op Amps

FEATURES

- Slew Rate 7V/µs Typ
- Gain-Bandwidth Product 14MHz Typ
- Fast Settling to 0.01%
  - 2V Step to 200µV 900ns Typ
  - 10V Step to 1mV 2.2µs Typ
- Excellent DC Precision in All Packages
  - Input Offset Voltage 275µV Max
  - Input Offset Voltage Drift 6µV/°C Max
  - Input Offset Current 30nA Max
  - Input Bias Current 125nA Max
  - Open-Loop Gain 1200V/mV Min
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground While Sinking Current
- Low Input Noise Voltage 12nV/√Hz Typ
- Low Input Noise Current 0.2pA/√Hz Typ
- Specified on 3.3V, 5V and ±15V
- Large Output Drive Current 20mA Min
- Low Supply Current per Amplifier 1.8mA Max
- Dual in 8-Pin DIP and SO8
- Quad in 14-Pin DIP and NARROW SO16

Note: For applications requiring higher slew rate, see the LT1213/LT1214 and LT1215/LT1216 data sheets.

DESCRIPTION

The LT1211 is a dual, single supply precision op amp with a 14MHz gain-bandwidth product and a 7V/µs slew rate. The LT1212 is a quad version of the same amplifier. The DC precision of the LT1211/LT1212 eliminates trims in most systems while providing high frequency performance not usually found in single supply amplifiers.

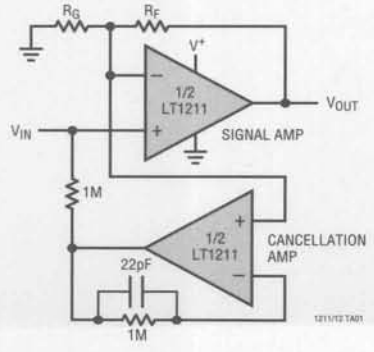
The LT1211/LT1212 will operate on any supply greater than 2.5V and less than 36V total. These amplifiers are specified on single 3.3V, single 5V and ±15V supplies, and only require 1.3mA of quiescent supply current per amplifier. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The minimum output drive is 20mA, ideal for driving low impedance loads.

APPLICATIONS

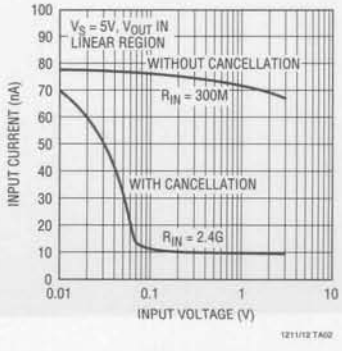
- 2.5V Full-Scale 12-Bit Systems $V_{OS} \leq 0.45LSB$
- 10V Full-Scale 16-Bit Systems $V_{OS} \leq 1.8LSB$
- Active Filters
- Photo Diode Amplifiers
- DAC Current-to-Voltage Amplifiers
- Battery-Powered Systems

TYPICAL APPLICATION

Input Bias Current Cancellation



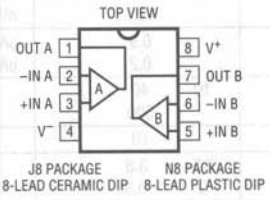
Input Current vs Input Voltage



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1211C/LT1212C ..... −40°C to 85°C
LT1211M ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Junction Temperature (Note 2)
Plastic Package (N8, S8, N, S) ..... 150°C
Ceramic Package (J8) ..... 175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

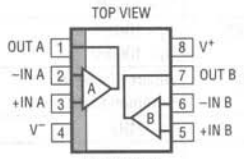


J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER

LT1211CN8
LT1211ACN8
LT1211MJ8
LT1211AMJ8



S8 PACKAGE 8-LEAD PLASTIC SOIC

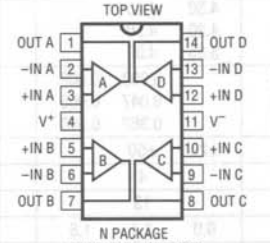
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1211CS8

S8 PART MARKING

1211

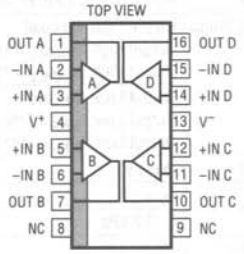


N PACKAGE 14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1212CN



S PACKAGE 16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1212CS

Consult factory for Industrial grade parts.

AVAILABLE OPTIONS

				PACKAGE		
NUMBER OF OP AMPS	T_A RANGE	MAX V_{OS} (25°C)	MAX TC V_{OS} ($\Delta V_{OS}/\Delta T$)	CERAMIC (J)	PLASTIC DIP (N)	SURFACE MOUNT (S)
Two (Dual)	−40°C to 85°C	150µV	1.5µV/°C		LT1211ACN8	
		275µV	3µV/°C		LT1211CN8	
		275µV	6µV/°C			LT1211CS8
Two (Dual)	−55°C to 125°C	150µV	1.5µV/°C	LT1211AMJ8		
		275µV	3µV/°C	LT1211MJ8		
Four (Quad)	−40°C to 85°C	275µV	6µV/°C		LT1212CN	LT1212CS

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AC LT1211AM MIN	LT1211AC LT1211AM TYP	LT1211AC LT1211AM MAX	LT1211C/LT1211M LT1212C MIN	LT1211C/LT1211M LT1212C TYP	LT1211C/LT1211M LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			75	150		100	275	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability			0.5			0.6		µV/Mo
I_{OS}	Input Offset Current			5	20		5	30	nA
I_B	Input Bias Current			50	100		60	125	nA
	Input Noise Voltage	0.1Hz to 10Hz		250			250		nV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz		12.5 12.0			12.5 12.0		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		0.9 0.2			0.9 0.2		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance (Note 3)	Differential Mode Common Mode	10	40 500		10	40 500		MΩ MΩ
	Input Capacitance	f = 1MHz		10			10		pF
	Input Voltage Range		3.5 0	3.8 −0.3		3.5 0	3.8 −0.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	90	105		86	102		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	90	115		87	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	250	560		250	560		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 15mA	4.30 4.20 3.85	4.40 4.30 4.00		4.30 4.20 3.85	4.40 4.30 4.00		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 15mA		0.003 0.047 0.362	0.006 0.065 0.500		0.003 0.047 0.362	0.006 0.065 0.500	V V V
I_O	Maximum Output Current	(Note 9)	±20	±50		±20	±50		mA
SR	Slew Rate	A_V = −2		4			4		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz		13			13		MHz
I_S	Supply Current per Amplifier		0.9	1.3	1.8	0.9	1.3	1.8	mA
	Minimum Supply Voltage	Single Supply		2.2	2.5		2.2	2.5	V
	Full Power Bandwidth	A_V = 1, V_O = $2.5V_{P-P}$		300			300		kHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, V_O = 100mV		45			45		ns
OS	Overshoot	A_V = 1, V_O = 100mV		25			25		%
t_{PD}	Propagation Delay	A_V = 1, V_O = 100mV		36			36		ns
t_S	Settling Time	0.01%, A_V = 1, ΔV_O = 2V		900			900		ns
	Open-Loop Output Resistance	I_O = 0mA, f = 5MHz		75			75		Ω
THD	Total Harmonic Distortion	A_V = 1, V_O = $1V_{RMS}$, 20Hz to 20kHz		0.001			0.001		%

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AC MIN	LT1211AC TYP	LT1211AC MAX	LT1211C/LT1212C MIN	LT1211C/LT1212C TYP	LT1211C/LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			100	175		150	375	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			5	25		10	35	nA
I_B	Input Bias Current			60	110		70	135	nA
	Input Voltage Range		3.4 0.1	3.5 −0.1		3.4 0.1	3.5 −0.1		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.1V to 3.4V	89	105		85	102		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	89	114		86	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	150	430		150	430		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.20	4.33		4.20	4.33		V
		Output High, I_{SOURCE} = 1mA	4.10	4.23		4.10	4.23		V
		Output High, I_{SOURCE} = 10mA	3.90	4.03		3.90	4.03		V
		Output Low, No Load		0.004	0.007		0.004	0.007	V
		Output Low, I_{SINK} = 1mA		0.052	0.070		0.052	0.070	V
		Output Low, I_{SINK} = 10mA		0.290	0.400		0.290	0.400	V
I_S	Supply Current per Amplifier		0.8	1.4	2.1	0.8	1.4	2.1	mA

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1211AC MIN	LT1211AC TYP	LT1211AC MAX	LT1211C/LT1212C MIN	LT1211C/LT1212C TYP	LT1211C/LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			120	200		175	500	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	30		20	50	nA
I_B	Input Bias Current			70	120		80	145	nA
	Input Voltage Range		3.1 0.2	3.2 0		3.1 0.2	3.2 0		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.2V to 3.1V	88	104		84	101		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	88	113		85	109		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	100	390		100	390		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.15	4.25		4.15	4.25		V
		Output High, I_{SOURCE} = 1mA	4.00	4.16		4.00	4.16		V
		Output High, I_{SOURCE} = 10mA	3.80	3.96		3.80	3.96		V
		Output Low, No Load		0.005	0.008		0.005	0.008	V
		Output Low, I_{SINK} = 1mA		0.053	0.075		0.053	0.075	V
		Output Low, I_{SINK} = 10mA		0.300	0.420		0.300	0.420	V
I_S	Supply Current per Amplifier		0.7	1.5	2.2	0.7	1.5	2.2	mA

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AM MIN	LT1211AM TYP	LT1211AM MAX	LT1211M MIN	LT1211M TYP	LT1211M MAX	UNITS
V_{OS}	Input Offset Voltage			140	250		200	500	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			0.7	1.5		1	3	µV/°C
I_{OS}	Input Offset Current			15	40		25	75	nA
I_B	Input Bias Current			75	130		85	160	nA
	Input Voltage Range		3.1 0.4	3.2 0.2		3.1 0.4	3.2 0.2		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.4V to 3.1V	87	104		81	101		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	87	113		84	109		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	100	250		100	250		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 10mA	4.10 3.95 3.70	4.20 4.10 3.90		4.10 3.95 3.70	4.20 4.10 3.90		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 10mA		0.007 0.060 0.350	0.010 0.085 0.500		0.007 0.060 0.350	0.010 0.085 0.500	mV mV mV
I_S	Supply Current per Amplifier		0.5	1.7	2.5	0.5	1.7	2.5	mA

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AC LT1211AM MIN	LT1211AC LT1211AM TYP	LT1211AC LT1211AM MAX	LT1211C/LT1211M LT1212C MIN	LT1211C/LT1211M LT1212C TYP	LT1211C/LT1211M LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			125	400		150	550	µV
I_{OS}	Input Offset Current			5	20		5	30	nA
I_B	Input Bias Current			45	95		50	120	nA
	Input Voltage Range		13.5 −15.0	13.8 −15.3		13.5 −15.0	13.8 −15.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −15V to 13.5V	90	105		86	102		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	90	113		87	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1200	5000		1200	5000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 15mA	13.8	14.0		13.8	14.0		V
		Output Low, I_{SINK} = 15mA	−14.4	−14.6		−14.4	−14.6		V
I_O	Maximum Output Current	(Note 9)	±20	±50		±20	±50		mA
SR	Slew Rate	A_V = −2 (Note 6)	5	7		5	7		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz	8	14		8	14		MHz
I_S	Supply Current per Amplifier		0.9	1.8	2.5	0.9	1.8	2.5	mA
	Channel Separation	V_O = ±10V, R_L = 2k	128	140		128	140		dB
	Minimum Supply Voltage	Equal Split Supplies		±1.2	±2.0		±1.2	±2.0	V
	Full Power Bandwidth	A_V = 1, V_O = $20V_{P-P}$		60			60		kHz
	Settling Time	0.01%, A_V = 1, ΔV_O = 10V		2.2			2.2		µs

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AC MIN	LT1211AC TYP	LT1211AC MAX	LT1211C/LT1212C MIN	LT1211C/LT1212C TYP	LT1211C/LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			150	425		200	650	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	20		10	35	nA
I_B	Input Bias Current			55	100		60	125	nA
	Input Voltage Range		13.4 −14.9	13.5 −15.1		13.4 −14.9	13.5 −15.1		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.9V to 13.4V	89	104		85	101		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	89	112		86	108		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1000	3500		1000	3500		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 10mA	13.8	14.0		13.8	14.0		V
		Output Low, I_{SINK} = 10mA	−14.5	−14.7		−14.5	−14.7		V
I_S	Supply Current per Amplifier		0.8	2.1	2.9	0.8	2.1	2.9	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1211AC MIN	LT1211AC TYP	LT1211AC MAX	LT1211C/LT1212C MIN	LT1211C/LT1212C TYP	LT1211C/LT1212C MAX	UNITS
V_{OS}	Input Offset Voltage			175	450		250	700	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	25		10	40	nA
I_B	Input Bias Current			55	100		60	130	nA
	Input Voltage Range		13.1 −14.8	13.2 −15.0		13.1 −14.8	13.2 −15.0		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.8V to 13.1V	88	103		84	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	88	111		85	107		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1000	3000		1000	3000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 10mA	13.7	13.9		13.7	13.9		V
		Output Low, I_{SINK} = 10mA	−14.5	−14.7		−14.5	−14.7		V
I_S	Supply Current per Amplifier		0.7	2.2	3.0	0.7	2.2	3.0	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1211AM MIN	LT1211AM TYP	LT1211AM MAX	LT1211M MIN	LT1211M TYP	LT1211M MAX	UNITS
V_{OS}	Input Offset Voltage			200	500		300	800	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			0.7	1.5		1	3	µV/°C
I_{OS}	Input Offset Current			10	40		10	60	nA
I_B	Input Bias Current			55	110		60	140	nA
	Input Voltage Range		13.1 −14.6	13.2 −14.8		13.1 −14.6	13.2 −14.8		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.6V to 13.1V	87	103		81	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V	87	111		84	107		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	800	1500		800	1500		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 10mA	13.6	13.8		13.6	13.8		V
		Output Low, I_{SINK} = 10mA	−14.3	−14.5		−14.3	−14.5		V
I_S	Supply Current per Amplifier		0.5	2.3	3.4	0.5	2.3	3.4	mA

3.3V ELECTRICAL CHARACTERISTICS

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted. (Note 7)

			LT1211AC LT1211AM			LT1211C/LT1211M LT1212C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			75	150		100	275	µV
	Input Voltage Range (Note 8)		1.8	2.1		1.8	2.1		V
			0	−0.3		0	−0.3		V
	Maximum Output Voltage Swing	Output High, No Load	2.60	2.70		2.60	2.70		V
		Output High, I_{SOURCE} = 1mA	2.50	2.60		2.50	2.60		V
		Output High, I_{SOURCE} = 15mA	2.15	2.30		2.15	2.30		V
		Output Low, No Load		0.003	0.006		0.003	0.006	V
		Output Low, I_{SINK} = 1mA		0.047	0.065		0.047	0.065	V
		Output Low, I_{SINK} = 15mA		0.362	0.500		0.362	0.500	V
I_O	Maximum Output Current		±20	±50		±20	±50		mA

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted. (Note 7)

			LT1211AC			LT1211C/LT1212C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			100	175		150	375	µV
	Input Voltage Range (Note 8)		1.7	1.4		1.7	1.8		V
			0.1	−0.1		0.1	−0.1		V
	Maximum Output Voltage Swing	Output High, No Load	2.50	2.63		2.50	2.63		V
		Output High, I_{SOURCE} = 1mA	2.40	2.53		2.40	2.53		V
		Output High, I_{SOURCE} = 10mA	2.20	2.33		2.20	2.33		V
		Output Low, No Load		0.004	0.007		0.004	0.007	V
		Output Low, I_{SINK} = 1mA		0.052	0.070		0.052	0.070	V
		Output Low, I_{SINK} = 10mA		0.290	0.400		0.290	0.400	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5, 7)

			LT1211AC			LT1211C/LT1212C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			120	200		175	500	µV
	Input Voltage Range (Note 8)		1.4	1.5		1.4	1.5		V
			0.2	0		0.2	0		V
	Maximum Output Voltage Swing	Output High, No Load	2.45	2.55		2.45	2.55		V
		Output High, I_{SOURCE} = 1mA	2.30	2.46		2.30	2.46		V
		Output High, I_{SOURCE} = 10mA	2.10	2.26		2.10	2.26		V
		Output Low, No Load		0.005	0.008		0.005	0.008	V
		Output Low, I_{SINK} = 1mA		0.053	0.075		0.053	0.075	V
		Output Low, I_{SINK} = 10mA		0.300	0.420		0.300	0.420	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted. (Note 7)

			LT1211AM			LT1211M			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			130	250		200	500	µV
	Input Voltage Range (Note 8)		1.4	1.5		1.4	1.5		V
			0.4	0.2		0.4	0.2		V
	Maximum Output Voltage Swing	Output High, No Load	2.40	2.50		2.40	2.50		V
		Output High, I_{SOURCE} = 1mA	2.25	2.40		2.25	2.40		V
		Output High, I_{SOURCE} = 10mA	2.00	2.20		2.00	2.20		V
		Output Low, No Load		0.007	0.010		0.007	0.010	V
		Output Low, I_{SINK} = 1mA		0.060	0.085		0.060	0.085	V
		Output Low, I_{SINK} = 10mA		0.350	0.500		0.350	0.500	V

ELECTRICAL CHARACTERISTICS

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1211MJ8, LT1211AMJ8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1211CN8, LT1211ACN8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1211CS8:	$T_J = T_A + (P_D \times 150°C/W)$
LT1212CN:	$T_J = T_A + (P_D \times 70°C/W)$
LT1212CS:	$T_J = T_A + (P_D \times 100°C/W)$

Note 3: This parameter is not 100% tested.

Note 4: Guaranteed by correlation to 3.3V and ±15V tests.

Note 5: The LT1211/LT1212 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

Note 6: Slew rate is measured between ±8.5V on an output swing of ±10V on ±15V supplies.

Note 7: Most LT1211/LT1212 electrical characteristics change very little with supply voltage. See the 5V tables for characteristics not listed in the 3.3V table.

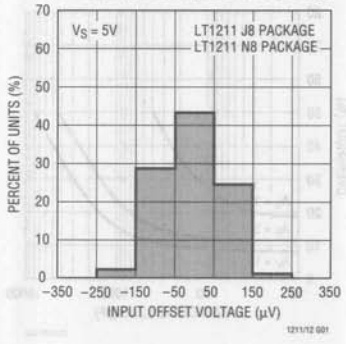
Note 8: Guaranteed by correlation to 5V and ±15V tests.

Note 9: Guaranteed by correlation to 3.3V tests.

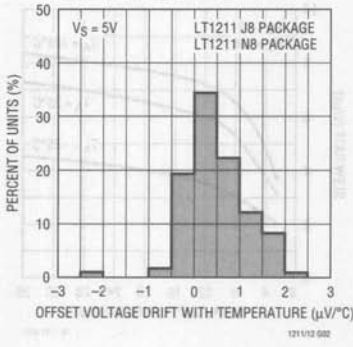
TYPICAL PERFORMANCE CHARACTERISTICS

2

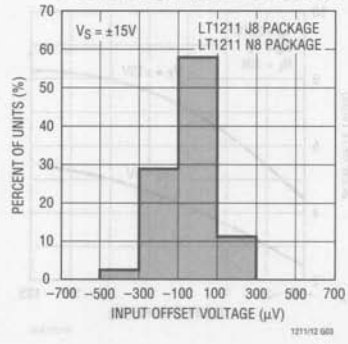
Distribution of Input Offset Voltage



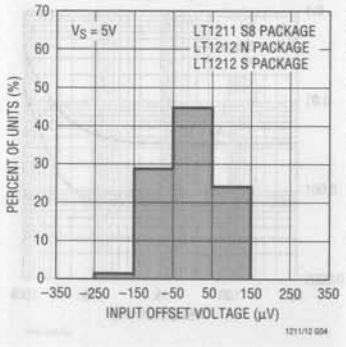
Distribution of Offset Voltage Drift with Temperature



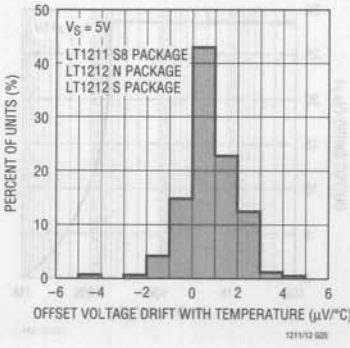
Distribution of Input Offset Voltage



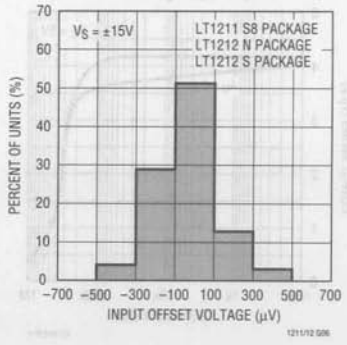
Distribution of Input Offset Voltage



Distribution of Offset Voltage Drift with Temperature

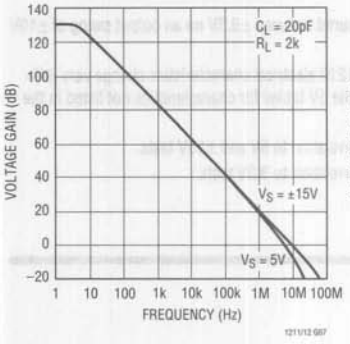


Distribution of Input Offset Voltage

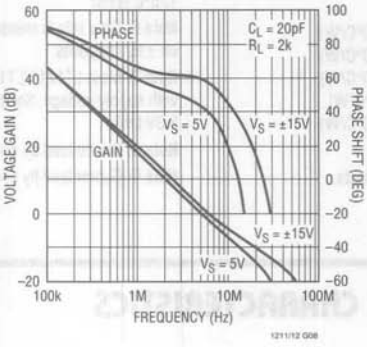


TYPICAL PERFORMANCE CHARACTERISTICS

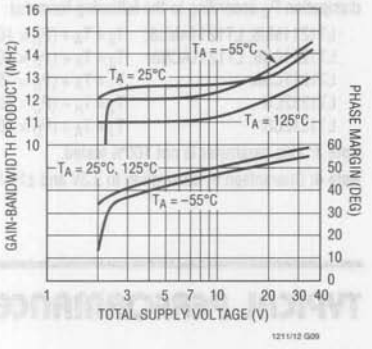
Voltage Gain vs Frequency



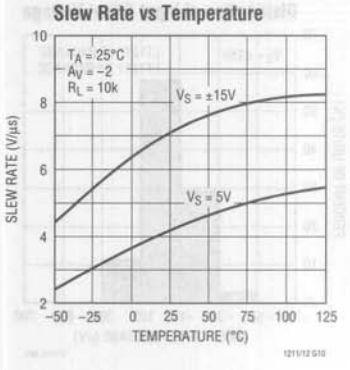
Voltage Gain, Phase vs Frequency



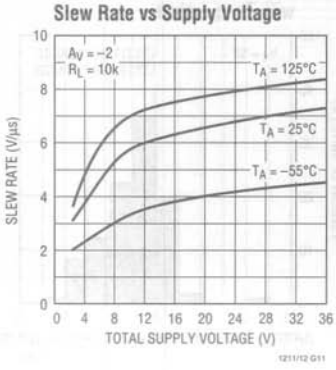
Gain-Bandwidth Product, Phase Margin vs Supply Voltage



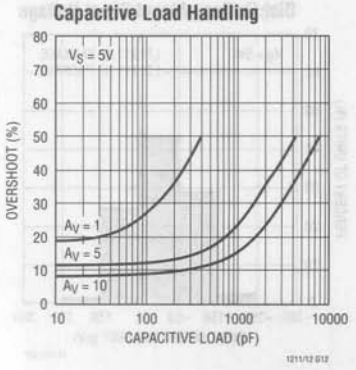
Slew Rate vs Temperature



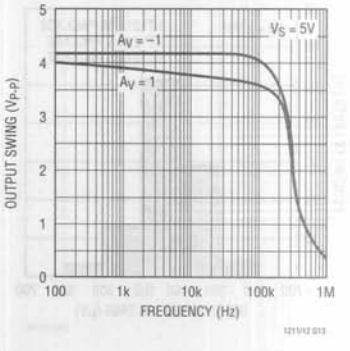
Slew Rate vs Supply Voltage



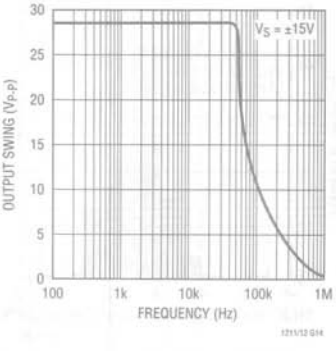
Capacitive Load Handling



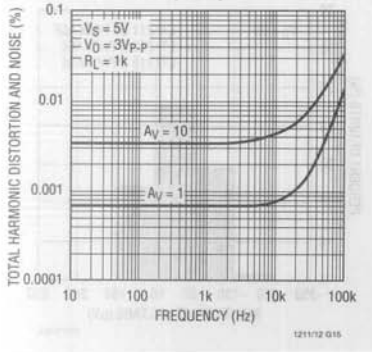
Undistorted Output Swing vs Frequency, V_S = 5V



Undistorted Output Swing vs Frequency, V_S = ±15V

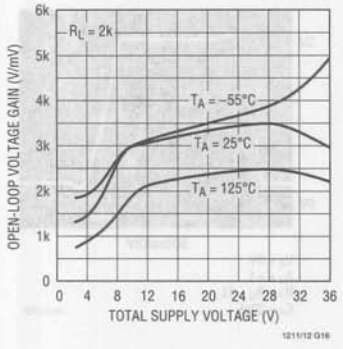


Total Harmonic Distortion and Noise vs Frequency

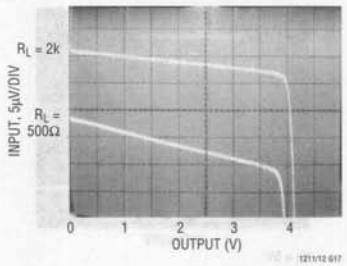


TYPICAL PERFORMANCE CHARACTERISTICS

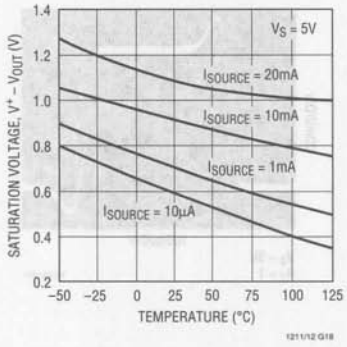
Open-Loop Voltage Gain vs Supply Voltage



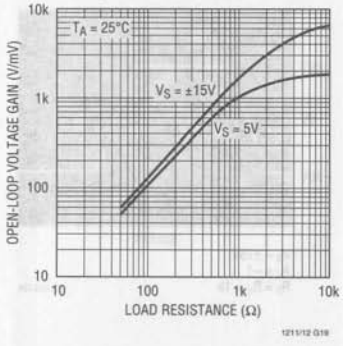
Open-Loop Gain, V_S = 5V



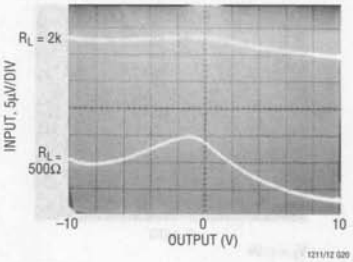
Positive Output Saturation Voltage vs Temperature



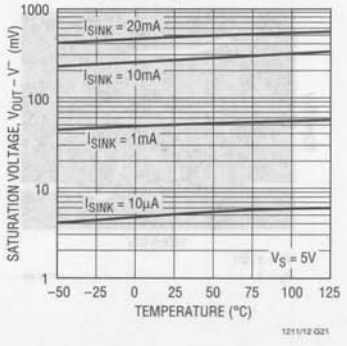
Voltage Gain vs Load Resistance



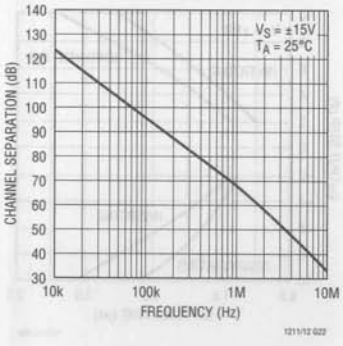
Open-Loop Gain, V_S = ±15V



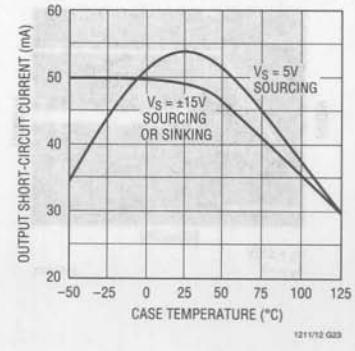
Negative Output Saturation Voltage vs Temperature



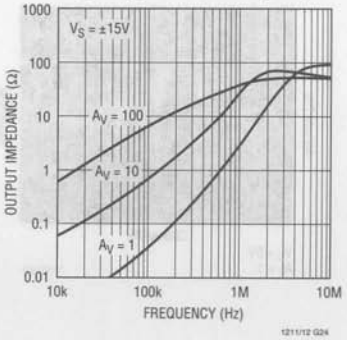
Channel Separation vs Frequency



Output Short-Circuit Current vs Temperature



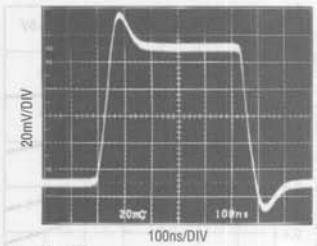
Output Impedance vs Frequency



2

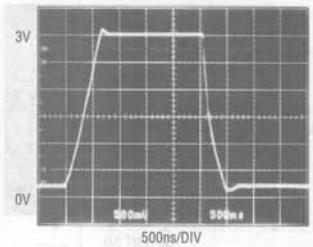
TYPICAL PERFORMANCE CHARACTERISTICS

5V Small-Signal Response



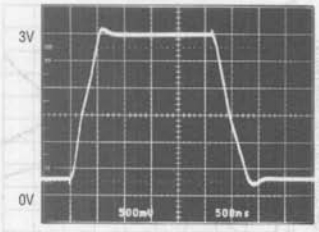
V_S = 5V
A_V = 1

5V Large-Signal Response



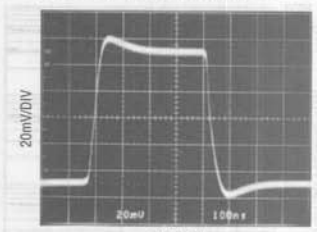
V_S = 5V
A_V = 1

5V Large-Signal Response



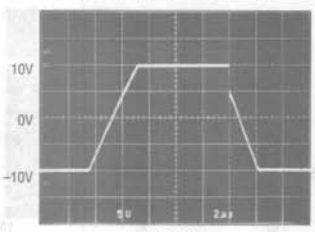
V_S = 5V
A_V = −1
R_F = R_G = 1k
C_F = 20pF

±15V Small-Signal Response



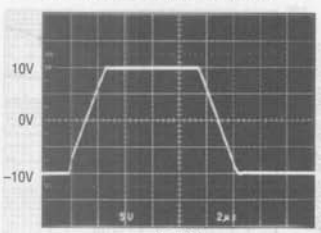
V_S = ±15V
A_V = 1

±15V Large-Signal Response



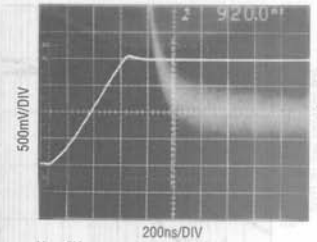
V_S = ±15V
A_V = 1

±15V Large-Signal Response



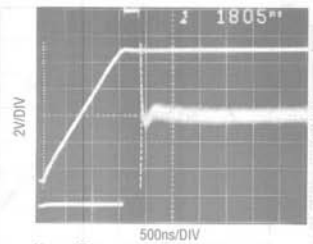
V_S = ±15V
A_V = −1
R_F = R_G = 1k

5V Settling



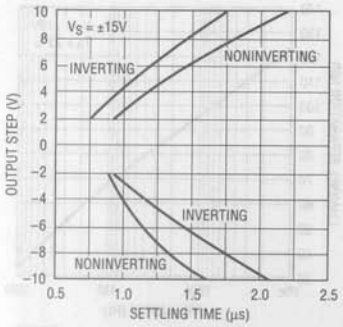
V_S = 5V
A_V = 1

±15V Settling



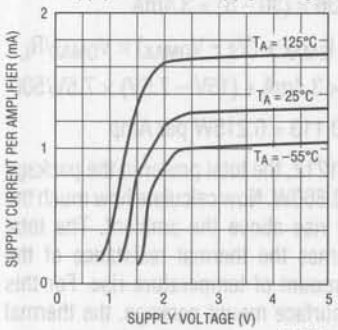
V_S = ±15V
A_V = −1

Settling Time to 0.01% vs Output Step

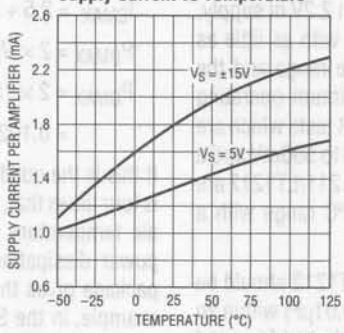


TYPICAL PERFORMANCE CHARACTERISTICS

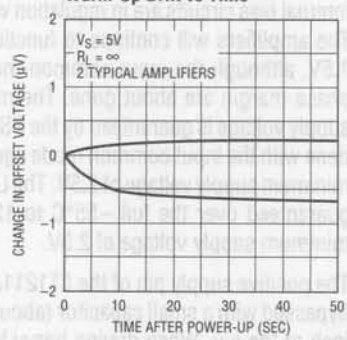
Supply Current vs Supply Voltage



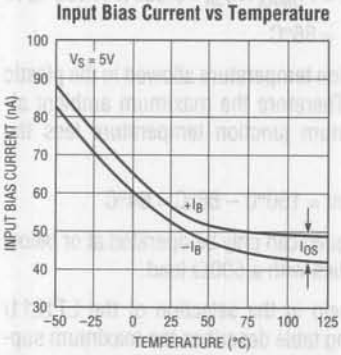
Supply Current vs Temperature



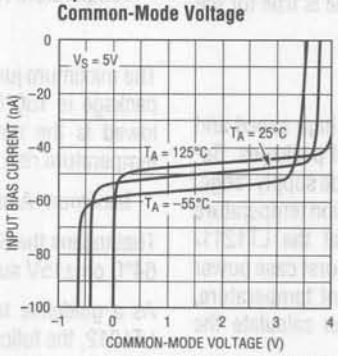
Warm-Up Drift vs Time



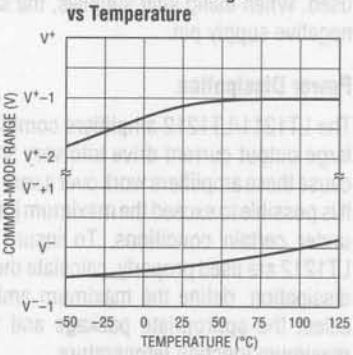
Input Bias Current vs Temperature



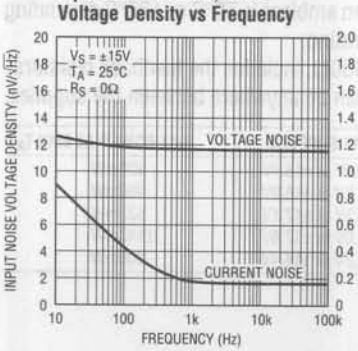
Input Bias Current vs Common-Mode Voltage



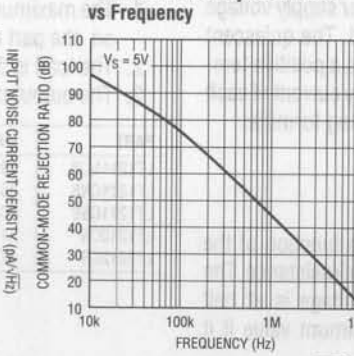
Common-Mode Range vs Temperature



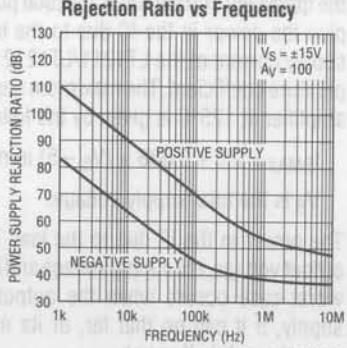
Input Noise Current, Noise Voltage Density vs Frequency



Common-Mode Rejection Ratio vs Frequency



Input Referred Power Supply Rejection Ratio vs Frequency



2

APPLICATIONS INFORMATION

Supply Voltage

The LT1211/LT1212 op amps are fully functional and all internal bias circuits are in regulation with 2.2V of supply. The amplifiers will continue to function with as little as 1.5V, although the input common-mode range and the phase margin are about gone. The minimum operating supply voltage is guaranteed by the PSRR tests which are done with the input common mode equal to 500mV and a minimum supply voltage of 2.5V. The LT1211/LT1212 are guaranteed over the full –55°C to 125°C range with a minimum supply voltage of 2.5V.

The positive supply pin of the LT1211/LT1212 should be bypassed with a small capacitor (about 0.01μF) within an inch of the pin. When driving heavy loads and for good settling time, an additional 4.7μF capacitor should be used. When using split supplies, the same is true for the negative supply pin.

Power Dissipation

The LT1211/LT1212 amplifiers combine high speed and large output current drive into very small packages. Because these amplifiers work over a very wide supply range, it is possible to exceed the maximum junction temperature under certain conditions. To insure that the LT1211/LT1212 are used properly, calculate the worst case power dissipation, define the maximum ambient temperature, select the appropriate package and then calculate the maximum junction temperature.

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1211/LT1212 has a positive temperature coefficient. The maximum supply current of each amplifier at 125°C is given by the following formula:

$$I_{SMAX} = 2.5 + 0.036 \times (V_S - 5) \text{ in mA}$$

V_S is the total supply voltage.

The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, calculate the worst case power dissipation while operating on ±15V supplies and driving a 500Ω load.

$$I_{SMAX} = 2.5 + 0.036 \times (30 - 5) = 3.4\text{mA}$$

$$P_{DMAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OMAX}) \times V_{OMAX}/R_L$$

$$P_{DMAX} = 2 \times 15\text{V} \times 3.4\text{mA} + (15\text{V} - 7.5\text{V}) \times 7.5\text{V}/500$$

$$= 0.102 + 0.113 = 0.215\text{W per Amp}$$

If this is the quad LT1212, the total power in the package is four times that, or 0.860W. Now calculate how much the die temperature will rise above the ambient. The total power dissipation times the thermal resistance of the package gives the amount of temperature rise. For this example, in the SO surface mount package, the thermal resistance is 100°C/W junction-to-ambient in still air.

$$\text{Temperature Rise} = P_{DMAX} \times \theta_{JA} = 0.860\text{W} \times 100°\text{C/W}$$

$$= 86°\text{C}$$

The maximum junction temperature allowed in the plastic package is 150°C. Therefore the maximum ambient allowed is the maximum junction temperature less the temperature rise.

$$\text{Maximum Ambient} = 150°\text{C} - 86°\text{C} = 64°\text{C}$$

That means the SO quad can only be operated at or below 64°C on ±15V supplies with a 500Ω load.

As a guideline to help in the selection of the LT1211/LT1212, the following table describes the maximum supply voltage that can be used with each part based on the following assumptions:

1. The maximum ambient is 70°C or 125°C depending on the part rating.
2. The load is 500Ω, includes the feedback resistors.
3. The output can be anywhere between the supplies.

PART	MAX SUPPLIES	MAX POWER AT MAX T_A
LT1211MJ8	19.5V or ±16.4V	500mW
LT1211CN8	25.2V or ±18.0V	800mW
LT1211CS8	20.3V or ±17.1V	533mW
LT1212CN	21.0V or ±17.8V	1143mW
LT1212CS	17.3V or ±14.4V	800mW

APPLICATIONS INFORMATION

Inputs

Typically, at room temperature, the inputs of the LT1211/LT1212 can common mode 400mV below ground (V^-) and to within 1.2V of the positive supply with the amplifier still functional. However the input bias current and offset voltage will shift as shown in the characteristic curves. For full precision performance, the common-mode range should be limited between ground (V^-) and 1.5V below the positive supply.

When either of the inputs is taken below ground (V^-) by more than about 700mV, that input bias current will increase dramatically. The current is limited by internal 100Ω resistors between the input pins and diodes to each supply. The output will remain low (no phase reversal) for inputs 1.3V below ground (V^-). If the output does not have to sink current, such as in a single supply system with a 1k load to ground, there is no phase reversal for inputs up to 8V below ground.

There are no clamps across the inputs of the LT1211/LT1212 and therefore each input can be forced to any voltage between the supplies. The input current will remain constant at about 60nA over most of this range. When an input gets closer than 1.5V to the positive supply, that input current will gradually decrease to zero until the input goes above the supply, then it will increase due to the previously mentioned diodes. If the inverting input is held more positive than the noninverting input by 200mV or more, while at the same time the noninverting input is within 300mV of ground (V^-), then the supply current will increase by 1mA and the noninverting input current will increase to about 10μA. This should be kept in mind in comparator applications where the inverting input stays above ground (V^-) and the noninverting input is at or near ground (V^-).

Output

The output of the LT1211/LT1212 will swing to within 0.60V of the positive supply with no load. The open-loop output resistance, when the output is driven hard into the positive rail, is about 100Ω as the output starts to source current; this resistance drops to about 25Ω as the current increases. Therefore when the output sources 1mA, the output will swing to within 0.7V of the positive supply. While sourcing 20mA, it is within 1.1V of the positive supply.

The output of the LT1211/LT1212 will swing to within 3mV of the negative supply while sinking zero current. Thus, in a typical single supply application with the load going to ground, the output will go to within 3mV of ground. The open-loop output resistance when the output is driven hard into the negative rail is about 44Ω at low currents and reduces to about 24Ω at high currents. Therefore, when the output sinks 1mA, the output is about 42mV above the negative supply and while sinking 20mA, it is about 480mV above it.

The output of the LT1211/LT1212 has reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited currents will flow. If the current is transient and limited to several hundred mA, no damage will occur.

Feedback Components

Because the input currents of the LT1211/LT1212 are less than 125nA, it is possible to use high value feedback resistors to set the gain. However, care must be taken to insure that the pole that is formed by the feedback resistors and the input capacitance does not degrade the stability of the amplifier. For example, if a single supply, noninverting gain of two is set with two 20k resistors, the LT1211/LT1212 will probably oscillate. This is because the amplifier goes open-loop at 3MHz (6dB of gain) and has 50° of phase margin. The feedback resistors and the 10pF input capacitance generate a pole at 1.6MHz that introduces 63° of phase shift at 3MHz! The solution is simple; use lower value resistors or add a feedback capacitor of 10pF or more.

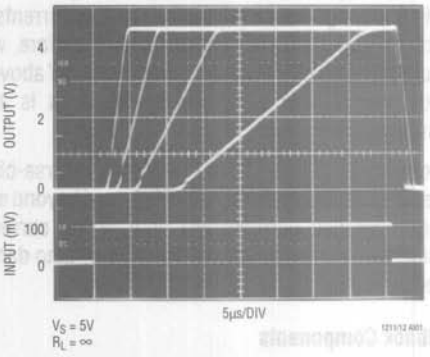
APPLICATIONS INFORMATION

Comparator Applications

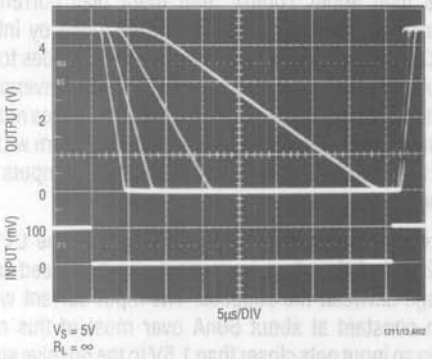
Sometimes it is desirable to use an op amp as a comparator. When operating the LT1211/LT1212 on a single 3.3V or 5V supply, the output interfaces directly with most TTL and CMOS logic.

The response time of the LT1211/LT1212 is a strong function of the amount of input overdrive as shown in the following photos. These amplifiers are unity-gain stable op amps and not fast comparators, therefore, the logic being driven may oscillate due to the long transition time. The output can be speeded up by adding 20mV or more of hysteresis (positive feedback), but the offset is then a function of the input direction.

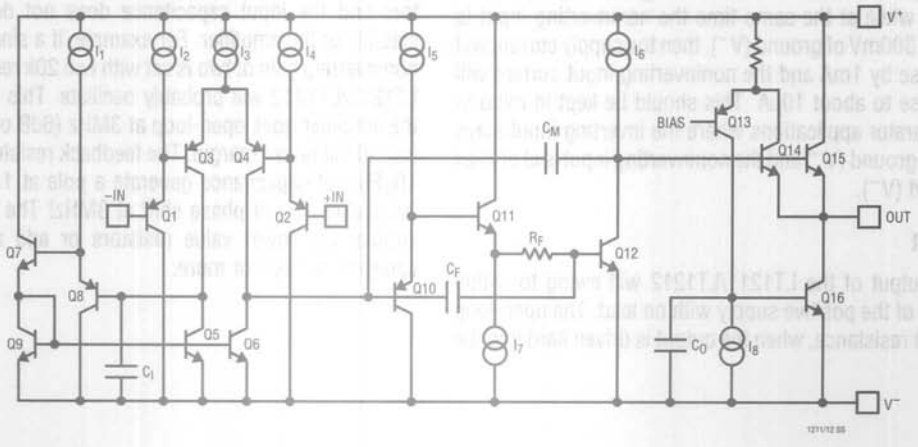
LT1211 Comparator Response (+)
20mV, 10mV, 5mV, 2mV Overdrives



LT1211 Comparator Response (–)
20mV, 10mV, 5mV, 2mV Overdrives

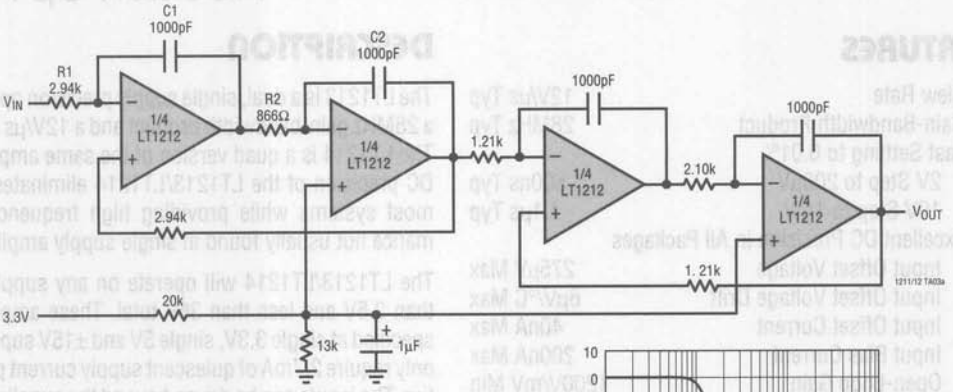


SIMPLIFIED SCHEMATIC



TYPICAL APPLICATIONS

Single Supply, 100kHz, 4th Order Butterworth Lowpass Filter



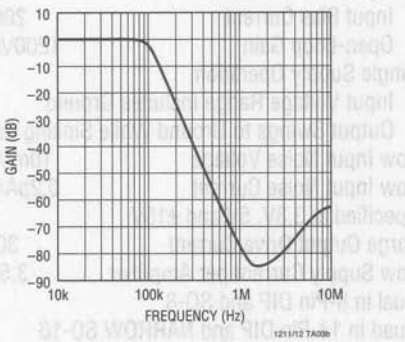
12-BIT ACCURATE SIGNAL RANGE FROM 6mV TO 1.8V ON 3.3V SINGLE SUPPLY.
MAXIMUM OUTPUT OFFSET ERROR IS 676µV.

FOR EACH 2ND ORDER SECTION:

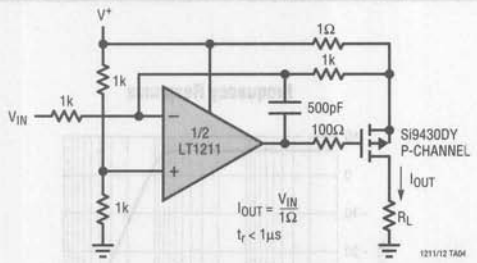
$$W_O^2 = \frac{1}{C1C2R1R2}$$

$$R1 = \frac{1}{W_O QC1}$$

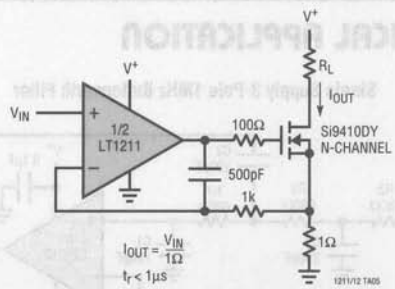
$$R2 = \frac{Q}{W_O C2}$$



1A Voltage-Controlled Current Source



1A Voltage-Controlled Current Sink



28MHz, 12V/µs, Single Supply Dual and Quad Precision Op Amps

FEATURES

- Slew Rate 12V/µs Typ
- Gain-Bandwidth Product 28MHz Typ
- Fast Settling to 0.01%
  - 2V Step to 200µV 500ns Typ
  - 10V Step to 1mV 1.1µs Typ
- Excellent DC Precision in All Packages
  - Input Offset Voltage 275µV Max
  - Input Offset Voltage Drift 6µV/°C Max
  - Input Offset Current 40nA Max
  - Input Bias Current 200nA Max
  - Open-Loop Gain 1200V/mV Min
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground While Sinking Current
- Low Input Noise Voltage 10nV/√Hz Typ
- Low Input Noise Current 0.2pA/√Hz Typ
- Specified at 3.3V, 5V and ±15V
- Large Output Drive Current 30mA Min
- Low Supply Current per Amplifier 3.5mA Max
- Dual in 8-Pin DIP and SO-8
- Quad in 14-Pin DIP and NARROW SO-16

Note: For applications requiring higher slew rate, see the LT1215/LT1216 data sheet. For lower power and lower slew rate, see the LT1211/LT1212 data sheet.

DESCRIPTION

The LT1213 is a dual, single supply precision op amp with a 28MHz gain-bandwidth product and a 12V/µs slew rate. The LT1214 is a quad version of the same amplifier. The DC precision of the LT1213/LT1214 eliminates trims in most systems while providing high frequency performance not usually found in single supply amplifiers.

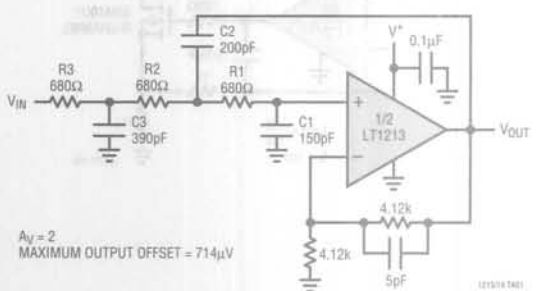
The LT1213/LT1214 will operate on any supply greater than 2.5V and less than 36V total. These amplifiers are specified at single 3.3V, single 5V and ±15V supplies, and only require 2.7mA of quiescent supply current per amplifier. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The minimum output drive is 30mA, ideal for driving low impedance loads.

APPLICATIONS

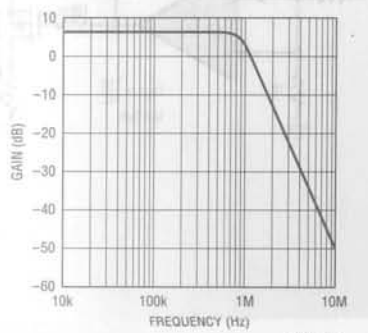
- 2.5V Full-Scale 12-Bit Systems $V_{OS} \leq 0.45LSB$
- 10V Full-Scale 16-Bit Systems $V_{OS} \leq 1.8LSB$
- Active Filters
- Photodiode Amplifiers
- DAC Current-to-Voltage Amplifiers
- Battery-Powered Systems

TYPICAL APPLICATION

Single Supply 3-Pole 1MHz Butterworth Filter



Frequency Response

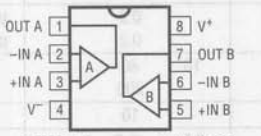


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1213C/LT1214C ..... –40°C to 85°C
LT1213M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 2)
Plastic Package (N8, S8, N, S) ..... 150°C
Ceramic Package (J8) ..... 175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



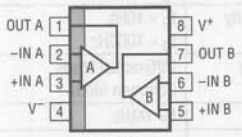
J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER

LT1213CN8
LT1213ACN8
LT1213MJ8
LT1213AMJ8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

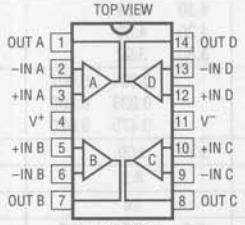
ORDER PART NUMBER

LT1213CS8

S8 PART MARKING

1213

TOP VIEW



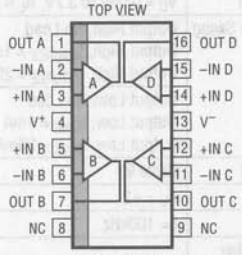
N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1214CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1214CS

Consult factory for Industrial grade parts.

AVAILABLE OPTIONS

NUMBER OF OP AMPS	T_A RANGE	MAX V_{OS} (25°C)	MAX TC V_{OS} ($\Delta V_{OS}/\Delta T$)	PACKAGE		
				CERAMIC DIP (J)	PLASTIC DIP (N)	SURFACE MOUNT (S)
Two (Dual)	–40°C to 85°C	150µV	1.5µV/°C		LT1213ACN8	
		275µV	3µV/°C		LT1213CN8	
		275µV	6µV/°C			LT1213CS8
Two (Dual)	–55°C to 125°C	150µV	1.5µV/°C	LT1213AMJ8		
		275µV	3µV/°C	LT1213MJ8		
Four (Quad)	–40°C to 85°C	275µV	6µV/°C		LT1214CN	LT1214CS

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AC LT1213AM MIN	LT1213AC LT1213AM TYP	LT1213AC LT1213AM MAX	LT1213C/LT1213M LT1214C MIN	LT1213C/LT1213M LT1214C TYP	LT1213C/LT1213M LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			75	150		100	275	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability			0.5			0.6		µV/Mo
I_{OS}	Input Offset Current			5	30		5	40	nA
I_B	Input Bias Current			80	160		100	200	nA
	Input Noise Voltage	0.1Hz to 10Hz		200			200		nV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz		10 10			10 10		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		0.9 0.2			0.9 0.2		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance (Note 3)	Differential Mode Common Mode	10	40 200		10	40 200		MΩ MΩ
	Input Capacitance	f = 1MHz		10			10		pF
	Input Voltage Range		3.5 0	3.8 −0.3		3.5 0	3.8 −0.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	90	105		86	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	93	116		90	116		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	250	850		250	850		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 20mA	4.30 4.20 3.80	4.39 4.30 3.92		4.30 4.20 3.80	4.39 4.30 3.92		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 20mA		0.004 0.033 0.475	0.007 0.050 0.620		0.004 0.033 0.475	0.007 0.050 0.620	V V V
I_O	Maximum Output Current	(Note 9)	±30	±50		±30	±50		mA
SR	Slew Rate	A_V = −2		8.5			8.5		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz		26			26		MHz
I_S	Supply Current per Amplifier		2.0	2.7	3.8	2.0	2.7	3.8	mA
	Minimum Supply Voltage	Single Supply, V_{CM} = 0V		2.2	2.5		2.2	2.5	V
	Full Power Bandwidth	A_V = 1, V_O = $2.5V_{P-P}$		1.0			1.0		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, V_O = 100mV		24			24		ns
OS	Overshoot	A_V = 1, V_O = 100mV		30			30		%
t_{PD}	Propagation Delay	A_V = 1, V_O = 100mV		17			17		ns
t_S	Settling Time	0.01%, A_V = 1, ΔV_O = 2V		500			500		ns
	Open-Loop Output Resistance	I_O = 0mA, f = 10MHz		50			50		Ω
THD	Total Harmonic Distortion	A_V = 1, V_O = $1V_{RMS}$, 20Hz to 20kHz		0.001			0.001		%

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			100	175		150	375	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	45		10	55	nA
I_B	Input Bias Current			90	190		110	230	nA
	Input Voltage Range		3.4	3.5		3.4	3.5		V
			0.1	−0.1		0.1	−0.1		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.1V to 3.4V	89	105		85	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	92	114		89	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	200	580		200	580		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.20	4.33		4.20	4.33		V
		Output High, I_{SOURCE} = 1mA	4.10	4.25		4.10	4.25		V
		Output High, I_{SOURCE} = 15mA	3.84	3.96		3.84	3.96		V
		Output Low, No Load		0.005	0.008		0.005	0.008	V
		Output Low, I_{SINK} = 1mA		0.036	0.055		0.036	0.055	V
		Output Low, I_{SINK} = 15mA		0.370	0.530		0.370	0.530	V
I_S	Supply Current per Amplifier		1.8	2.9	4.0	1.8	2.9	4.0	mA

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			120	200		175	500	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			15	50		20	75	nA
I_B	Input Bias Current			100	200		120	250	nA
	Input Voltage Range		3.1	3.2		3.1	3.2		V
			0.2	0		0.2	0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.2V to 3.1V	88	104		84	104		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	91	113		88	113		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	200	510		200	510		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.15	4.25		4.15	4.25		V
		Output High, I_{SOURCE} = 1mA	4.00	4.16		4.00	4.16		V
		Output High, I_{SOURCE} = 15mA	3.72	3.89		3.72	3.89		V
		Output Low, No Load		0.006	0.009		0.006	0.009	V
		Output Low, I_{SINK} = 1mA		0.037	0.060		0.037	0.060	V
		Output Low, I_{SINK} = 15mA		0.380	0.550		0.380	0.550	V
I_S	Supply Current per Amplifier		1.5	2.9	4.0	1.5	2.9	4.0	mA

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AM MIN	LT1213AM TYP	LT1213AM MAX	LT1213M MIN	LT1213M TYP	LT1213M MAX	UNITS
V_{OS}	Input Offset Voltage			140	250		200	500	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			0.7	1.5		1.0	3.0	µV/°C
I_{OS}	Input Offset Current			20	70		25	100	nA
I_B	Input Bias Current			105	210		125	275	nA
	Input Voltage Range		3.1 0.4	3.2 0.2		3.1 0.4	3.2 0.2		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.4V to 3.1V	87	104		83	104		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	90	113		87	113		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	150	300		150	300		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 15mA	4.05 3.90 3.60	4.20 4.10 3.80		4.05 3.90 3.60	4.20 4.10 3.80		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 15mA		0.007 0.040 0.400	0.012 0.070 0.750		0.007 0.040 0.400	0.012 0.070 0.750	mV mV mV
I_S	Supply Current per Amplifier		1.3	3.0	4.2	1.3	3.0	4.2	mA

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AC LT1213AM MIN	LT1213AC LT1213AM TYP	LT1213AC LT1213AM MAX	LT1213C/LT1213M LT1214C MIN	LT1213C/LT1213M LT1214C TYP	LT1213C/LT1213M LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			125	400		150	550	µV
I_{OS}	Input Offset Current			5	30		5	40	nA
I_B	Input Bias Current			70	150		90	190	nA
	Input Voltage Range		13.5 −15.0	13.8 −15.3		13.5 −15.0	13.8 −15.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −15V to 13.5V	90	107		86	107		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	93	116		90	116		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1200	4000		1200	4000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 20mA	13.7	13.9		13.7	13.9		V
		Output Low, I_{SINK} = 20mA	−14.3	−14.5		−14.3	−14.5		V
I_O	Maximum Output Current	(Note 9)	±30	±50		±30	±50		mA
SR	Slew Rate	A_V = −2 (Note 6)	10	12		10	12		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz	15	28		15	28		MHz
I_S	Supply Current per Amplifier		2.0	3.4	4.7	2.0	3.4	4.7	mA
	Channel Separation	V_O = ±10V, R_L = 2k	128	140		128	140		dB
	Minimum Supply Voltage	Equal Split Supplies		±1.2	±2.0		±1.2	±2.0	V
	Full-Power Bandwidth	A_V = 1, V_O = $20V_{P-P}$		150			150		kHz
	Settling Time	0.01%, A_V = 1, ΔV_O = 10V		1.1			1.1		µs

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			150	425		200	650	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	35		10	45	nA
I_B	Input Bias Current			90	160		95	200	nA
	Input Voltage Range		13.4 −14.9	13.5 −15.1		13.4 −14.9	13.5 −15.1		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.9V to 13.4V	89	105		85	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	92	115		89	115		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1000	4000		1000	4000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 15mA	13.8	14.0		13.8	14.0		V
		Output Low, I_{SINK} = 15mA	−14.4	−14.6		−14.4	−14.6		V
I_S	Supply Current per Amplifier		1.8	3.7	5.0	1.8	3.7	5.0	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			175	450		250	700	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		0.7	1.5		1	3	µV/°C
		14-Pin DIP, SOIC Package					2	6	µV/°C
I_{OS}	Input Offset Current			10	40		20	75	nA
I_B	Input Bias Current			95	180		105	220	nA
	Input Voltage Range		13.1 −14.8	13.2 −15.0		13.1 −14.8	13.2 −15.0		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.8V to 13.1V	88	104		84	104		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	91	114		88	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1000	4000		1000	4000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 15mA	13.7	13.9		13.7	13.9		V
		Output Low, I_{SINK} = 15mA	−14.4	−14.6		−14.4	−14.6		V
I_S	Supply Current per Amplifier		1.5	3.7	5.1	1.5	3.7	5.1	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1213AM MIN	LT1213AM TYP	LT1213AM MAX	LT1213M MIN	LT1213M TYP	LT1213M MAX	UNITS
V_{OS}	Input Offset Voltage			200	500		300	800	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			0.7	1.5		1	3	µV/°C
I_{OS}	Input Offset Current			15	60		25	90	nA
I_B	Input Bias Current			100	200		110	250	nA
	Input Voltage Range		13.1 −14.6	13.2 −14.8		13.1 −14.6	13.2 −14.8		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.6V to 13.1V	87	104		83	104		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V	90	114		87	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	800	1100		800	1100		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 15mA	13.6	13.8		13.6	13.8		V
		Output Low, I_{SINK} = 15mA	−14.2	−14.5		−14.2	−14.5		V
I_S	Supply Current per Amplifier		1.3	4.0	5.4	1.3	4.0	5.4	mA

2

3.3V ELECTRICAL CHARACTERISTICS

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted. (Note 7)

SYMBOL	PARAMETER	CONDITIONS	LT1213AC LT1213AM MIN	LT1213AC LT1213AM TYP	LT1213AC LT1213AM MAX	LT1213C/LT1213M LT1214C MIN	LT1213C/LT1213M LT1214C TYP	LT1213C/LT1213M LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			75	150		100	275	µV
	Input Voltage Range (Note 8)		1.8	2.1		1.8	2.1		V
			0	−0.3		0	−0.3		V
	Maximum Output Voltage Swing	Output High, No Load	2.60	2.69		2.60	2.69		V
		Output High, I_{SOURCE} = 1mA	2.50	2.60		2.50	2.60		V
		Output High, I_{SOURCE} = 20mA	2.10	2.22		2.10	2.22		V
		Output Low, No Load		0.004	0.007		0.004	0.007	V
		Output Low, I_{SINK} = 1mA		0.033	0.050		0.033	0.050	V
		Output Low, I_{SINK} = 20mA		0.475	0.620		0.475	0.620	V
I_O	Maximum Output Current		±30	±50		±30	±50		mA

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted. (Note 7)

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			100	175		150	375	µV
	Input Voltage Range (Note 8)		1.7	1.8		1.7	1.8		V
			0.1	−0.1		0.1	−0.1		V
	Maximum Output Voltage Swing	Output High, No Load	2.50	2.63		2.50	2.63		V
		Output High, I_{SOURCE} = 1mA	2.40	2.55		2.40	2.55		V
		Output High, I_{SOURCE} = 15mA	2.14	2.26		2.14	2.26		V
		Output Low, No Load		0.005	0.008		0.005	0.008	V
		Output Low, I_{SINK} = 1mA		0.037	0.055		0.037	0.055	V
		Output Low, I_{SINK} = 15mA		0.400	0.530		0.400	0.530	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5, 7)

SYMBOL	PARAMETER	CONDITIONS	LT1213AC MIN	LT1213AC TYP	LT1213AC MAX	LT1213C/LT1214C MIN	LT1213C/LT1214C TYP	LT1213C/LT1214C MAX	UNITS
V_{OS}	Input Offset Voltage			120	200		175	500	µV
	Input Voltage Range (Note 8)		1.4	1.5		1.4	1.5		V
			0.2	0		0.2	0		V
	Maximum Output Voltage Swing	Output High, No Load	2.45	2.55		2.45	2.55		V
		Output High, I_{SOURCE} = 1mA	2.30	2.46		2.30	2.46		V
		Output High, I_{SOURCE} = 15mA	2.02	2.19		2.02	2.19		V
		Output Low, No Load		0.006	0.009		0.006	0.009	V
		Output Low, I_{SINK} = 1mA		0.040	0.060		0.040	0.060	V
		Output Low, I_{SINK} = 15mA		0.410	0.550		0.410	0.550	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted. (Note 7)

SYMBOL	PARAMETER	CONDITIONS	LT1213AM MIN	LT1213AM TYP	LT1213AM MAX	LT1213M MIN	LT1213M TYP	LT1213M MAX	UNITS
V_{OS}	Input Offset Voltage			130	250		200	500	µV
	Input Voltage Range (Note 8)		1.4	1.5		1.4	1.5		V
			0.4	0.2		0.4	0.2		V
	Maximum Output Voltage Swing	Output High, No Load	2.35	2.50		2.35	2.50		V
		Output High, I_{SOURCE} = 1mA	2.20	2.40		2.20	2.40		V
		Output High, I_{SOURCE} = 15mA	1.90	2.10		1.90	2.10		V
		Output Low, No Load		0.007	0.012		0.007	0.012	V
		Output Low, I_{SINK} = 1mA		0.040	0.070		0.040	0.070	V
		Output Low, I_{SINK} = 15mA		0.500	0.750		0.500	0.750	V

ELECTRICAL CHARACTERISTICS

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1213MJ8, LT1213AMJ8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1213CN8, LT1213ACN8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1213CS8:	$T_J = T_A + (P_D \times 150°C/W)$
LT1214CN:	$T_J = T_A + (P_D \times 70°C/W)$
LT1214CS:	$T_J = T_A + (P_D \times 100°C/W)$

Note 3: This parameter is not 100% tested.

Note 4: Guaranteed by correlation to 3.3V and ±15V tests.

Note 5: The LT1213/LT1214 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

Note 6: Slew rate is measured between ±8.5V on an output swing of ±10V on ±15V supplies.

Note 7: Most LT1213/LT1214 electrical characteristics change very little with supply voltage. See the 5V tables for characteristics not listed in the 3.3V table.

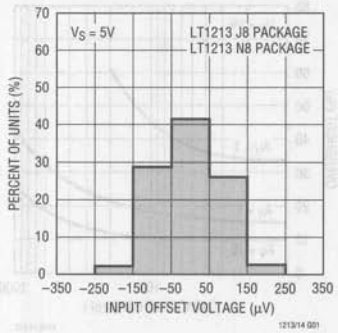
Note 8: Guaranteed by correlation to 5V and ±15V tests.

Note 9: Guaranteed by correlation to 3.3V tests.

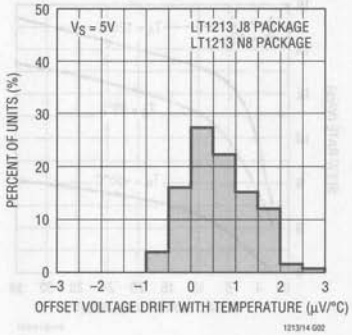
TYPICAL PERFORMANCE CHARACTERISTICS

2

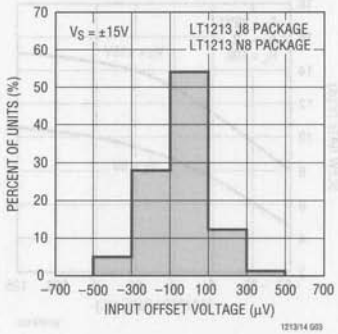
Distribution of Input Offset Voltage



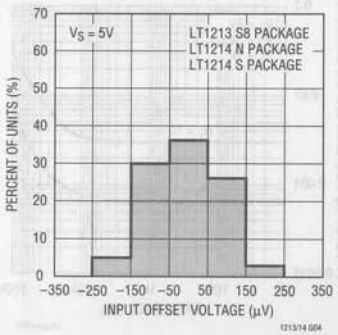
Distribution of Offset Voltage Drift with Temperature



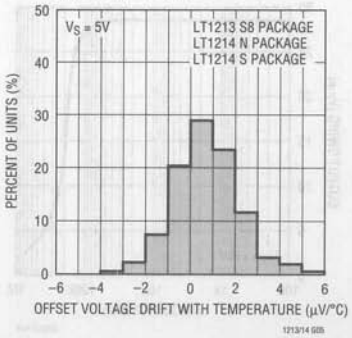
Distribution of Input Offset Voltage



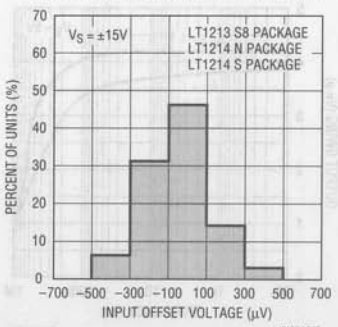
Distribution of Input Offset Voltage



Distribution of Offset Voltage Drift with Temperature

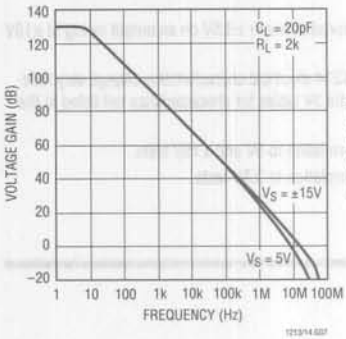


Distribution of Input Offset Voltage

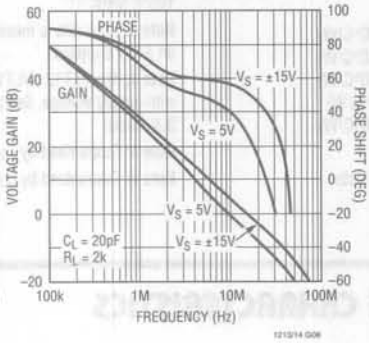


TYPICAL PERFORMANCE CHARACTERISTICS

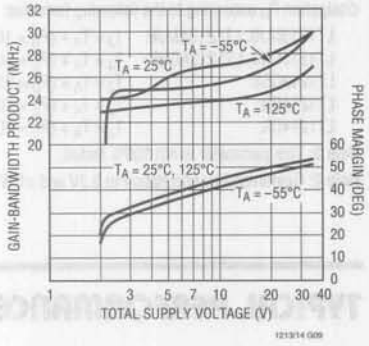
Voltage Gain vs Frequency



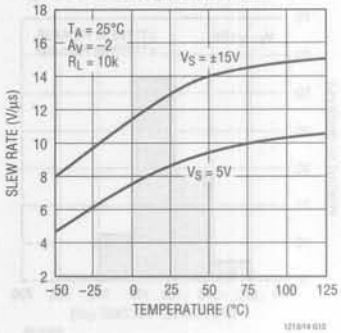
Voltage Gain, Phase vs Frequency



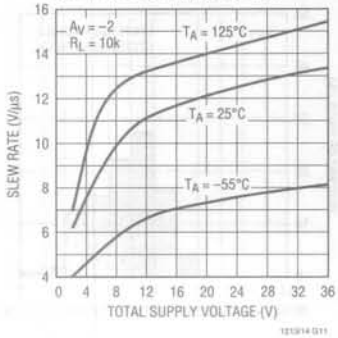
Gain-Bandwidth Product, Phase Margin vs Supply Voltage



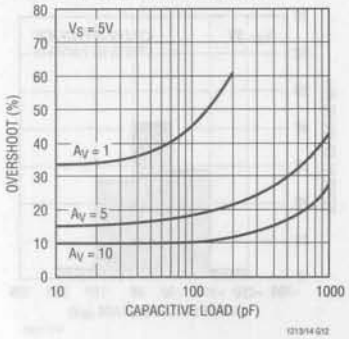
Slew Rate vs Temperature



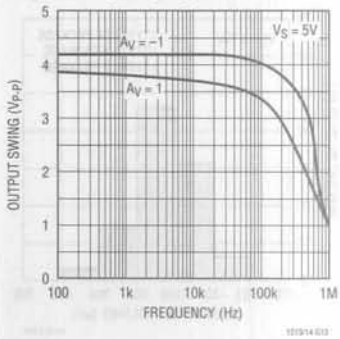
Slew Rate vs Supply Voltage



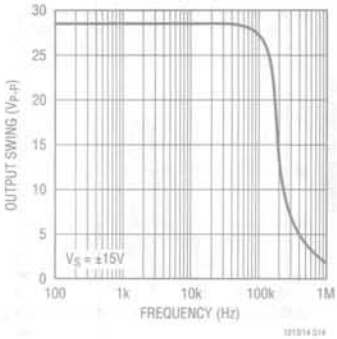
Capacitive Load Handling



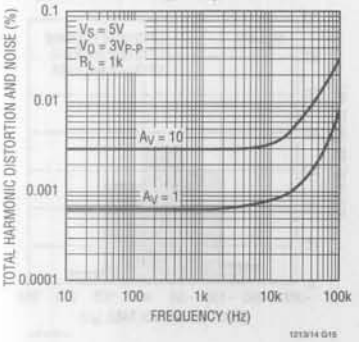
Undistorted Output Swing vs Frequency, V_S = 5V



Undistorted Output Swing vs Frequency, V_S = ±15V

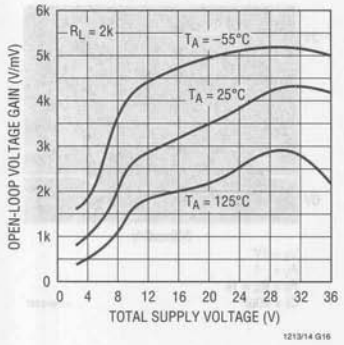


Total Harmonic Distortion and Noise vs Frequency

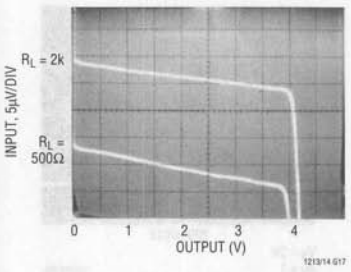


TYPICAL PERFORMANCE CHARACTERISTICS

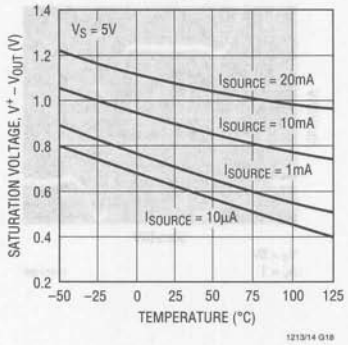
Open-Loop Voltage Gain vs Supply Voltage



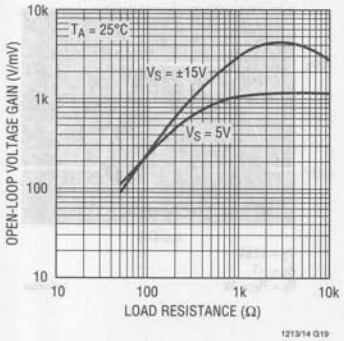
Open-Loop Gain, V_S = 5V



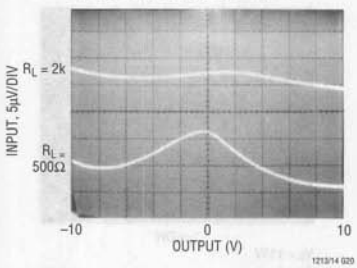
Positive Output Saturation Voltage vs Temperature



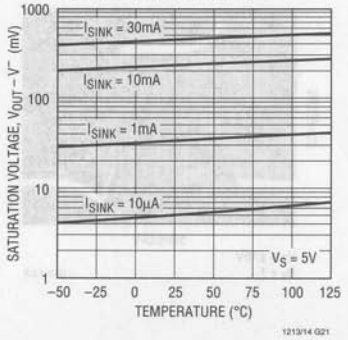
Voltage Gain vs Load Resistance



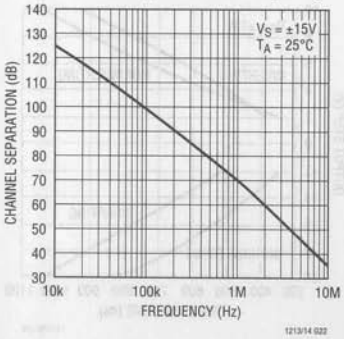
Open-Loop Gain, V_S = ±15V



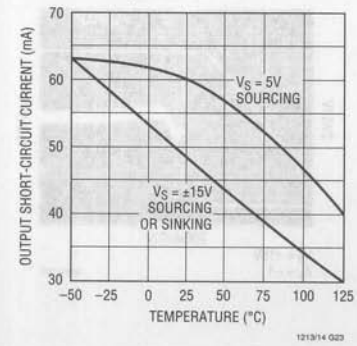
Negative Output Saturation Voltage vs Temperature



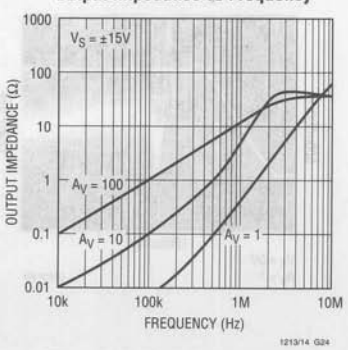
Channel Separation vs Frequency



Output Short-Circuit Current vs Temperature



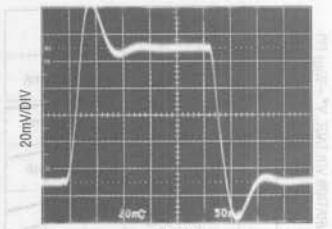
Output Impedance vs Frequency



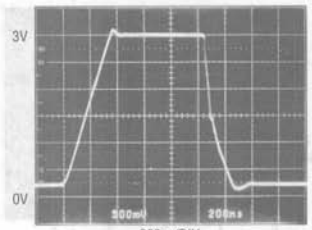
2

TYPICAL PERFORMANCE CHARACTERISTICS

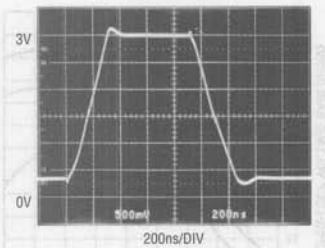
5V Small-Signal Response



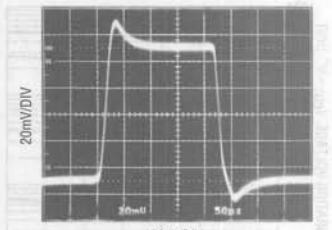
5V Large-Signal Response



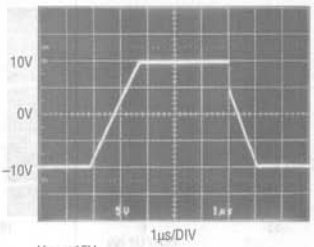
5V Large-Signal Response



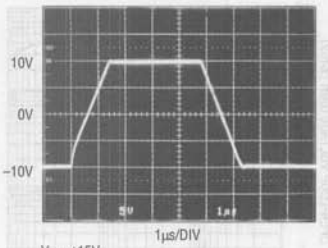
±15V Small-Signal Response



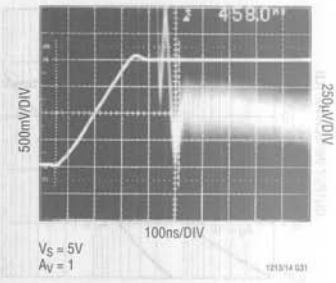
±15V Large-Signal Response



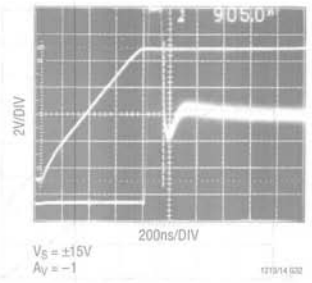
±15V Large-Signal Response



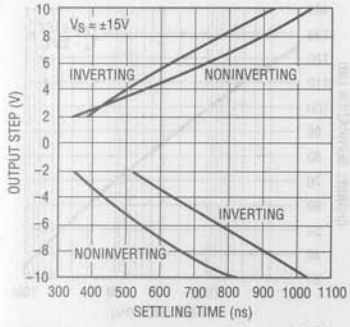
5V Settling



±15V Settling

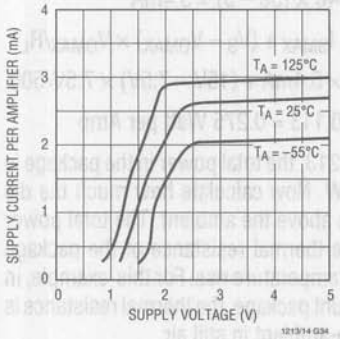


Settling Time to 0.01% vs Output Step

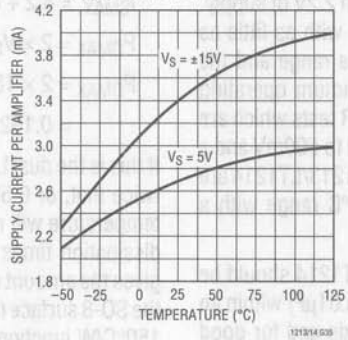


TYPICAL PERFORMANCE CHARACTERISTICS

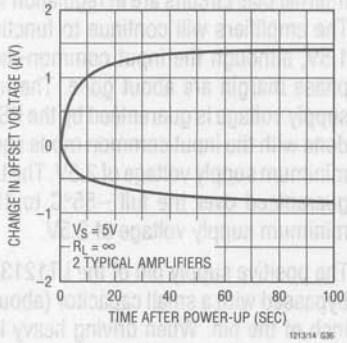
Supply Current vs Supply Votage



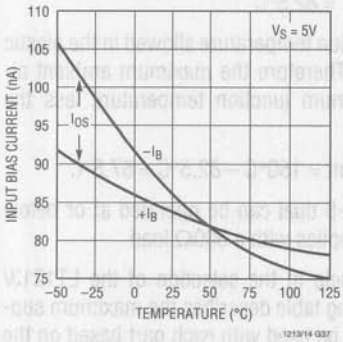
Supply Current vs Temperature



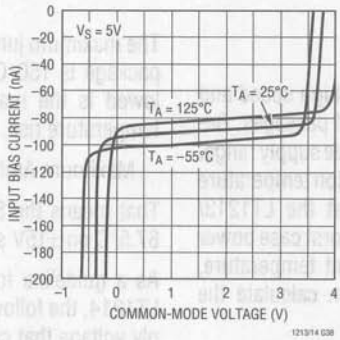
Warm-Up Drift vs Time



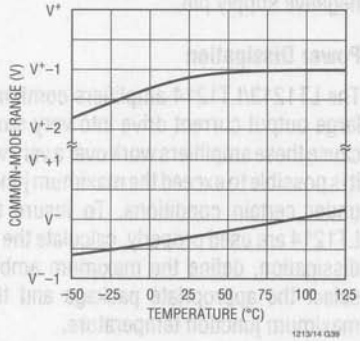
Input Bias Current vs Temperature



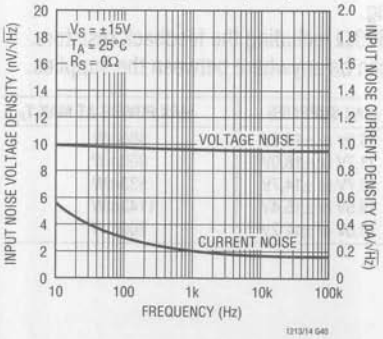
Input Bias Current vs Common-Mode Voltage



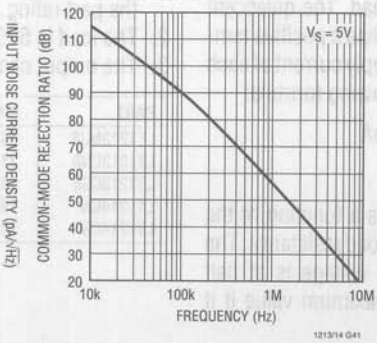
Common-Mode Range vs Temperature



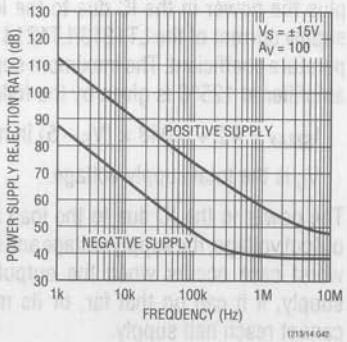
Input Noise Current, Noise Voltage Density vs Frequency



Common-Mode Rejection Ratio vs Frequency



Input Referred Power Supply Rejection Ratio vs Frequency



2

APPLICATIONS INFORMATION

Supply Voltage

The LT1213/LT1214 op amps are fully functional and all internal bias circuits are in regulation with 2.2V of supply. The amplifiers will continue to function with as little as 1.5V, although the input common-mode range and the phase margin are about gone. The minimum operating supply voltage is guaranteed by the PSRR tests which are done with the input common mode equal to 500mV and a minimum supply voltage of 2.5V. The LT1213/LT1214 are guaranteed over the full –55°C to 125°C range with a minimum supply voltage of 2.5V.

The positive supply pin of the LT1213/LT1214 should be bypassed with a small capacitor (about 0.01μF) within an inch of the pin. When driving heavy loads and for good settling time, an additional 4.7μF capacitor should be used. When using split supplies, the same is true for the negative supply pin.

Power Dissipation

The LT1213/LT1214 amplifiers combine high speed and large output current drive into very small packages. Because these amplifiers work over a very wide supply range, it is possible to exceed the maximum junction temperature under certain conditions. To insure that the LT1213/LT1214 are used properly, calculate the worst case power dissipation, define the maximum ambient temperature, select the appropriate package and then calculate the maximum junction temperature.

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1213/LT1214 has a positive temperature coefficient. The maximum supply current of each amplifier at 125°C is given by the following formula:

$$I_{SMAX} = 4.2 + 0.048 \times (V_S - 5) \text{ in mA}$$

V_S is the total supply voltage.

The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, calculate the worst case power dissipation while operating on ±15V supplies and driving a 500Ω load.

$$I_{SMAX} = 4.2 + 0.048 \times (30 - 5) = 5.4\text{mA}$$

$$P_{DMAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OMAX}) \times V_{OMAX}/R_L$$

$$P_{DMAX} = 2 \times 15\text{V} \times 5.4\text{mA} + (15\text{V} - 7.5\text{V}) \times 7.5\text{V}/500$$

$$= 0.162 + 0.113 = 0.275 \text{ Watt per Amp}$$

If this is the dual LT1213, the total power in the package is twice that, or 0.550W. Now calculate how much the die temperature will rise above the ambient. The total power dissipation times the thermal resistance of the package gives the amount of temperature rise. For this example, in the SO-8 surface mount package, the thermal resistance is 150°C/W junction-to-ambient in still air.

$$\text{Temperature Rise} = P_{DMAX} \times \theta_{JA} = 0.550\text{W} \times 150°\text{C/W}$$

$$= 82.5°\text{C}$$

The maximum junction temperature allowed in the plastic package is 150°C. Therefore the maximum ambient allowed is the maximum junction temperature less the temperature rise.

$$\text{Maximum Ambient} = 150°\text{C} - 82.5°\text{C} = 67.5°\text{C}$$

That means the SO-8 dual can be operated at or below 67.5°C on ±15V supplies with a 500Ω load.

As a guideline to help in the selection of the LT1213/LT1214, the following table describes the maximum supply voltage that can be used with each part based on the following assumptions:

1. The maximum ambient is 70°C or 125°C depending on the part rating.
2. The load is 500Ω including the feedback resistors.
3. The output can be anywhere between the supplies.

PART	MAX SUPPLIES	MAX POWER AT MAX T_A
LT1213MJ8	18.0V or ±14.1V	500mW
LT1213CN8	23.7V or ±18.0V	800mW
LT1213CS8	18.7V or ±14.7V	533mW
LT1214CN	19.5V or ±15.4V	1143mW
LT1214CS	15.8V or ±12.2V	800mW

APPLICATIONS INFORMATION

Inputs

Typically at room temperature, the inputs of the LT1213/LT1214 can common mode 400mV below ground (V^-) and to within 1.2V of the positive supply with the amplifier still functional. However, the input bias current and offset voltage will shift as shown in the characteristic curves. For full precision performance, the common-mode range should be limited between ground (V^-) and 1.5V below the positive supply.

When either of the inputs is taken below ground (V^-) by more than about 700mV, that input current will increase dramatically. The current is limited by internal 100Ω resistors between the input pins and diodes to each supply. The output will remain low (no phase reversal) for inputs 1.3V below ground (V^-). If the output does not have to sink current, such as in a single supply system with a 1k load to ground, there is no phase reversal for inputs up to 8V below ground.

There are no clamps across the inputs of the LT1213/LT1214 and therefore each input can be forced to any voltage between the supplies. The input current will remain constant at about 100nA over most of this range. When an input gets closer than 1.5V to the positive supply, that input current will gradually decrease to zero until the input goes above the supply, then it will increase due to the previously mentioned diodes. If the inverting input is held more positive than the noninverting input by 200mV or more, while at the same time the noninverting input is within 300mV of ground (V^-), then the supply current will increase by 2mA and the noninverting input current will increase to about 10μA. This should be kept in mind in comparator applications where the inverting input stays above ground (V^-) and the noninverting input is at or near ground (V^-).

Output

The output of the LT1213/LT1214 will swing to within 0.61V of the positive supply with no load. The open-loop output resistance, when the output is driven hard into the positive rail, is about 100Ω as the output starts to source current; this resistance drops to about 20Ω as the current increases. Therefore when the output sources 1mA, the output will swing to within 0.7V of the positive supply. While sourcing 30mA, it is within 1.25V of the positive supply.

The output of the LT1213/LT1214 will swing to within 4mV of the negative supply while sinking zero current. Thus, in a typical single supply application with the load going to ground, the output will go to within 4mV of ground. The open-loop output resistance when the output is driven hard into the negative rail is about 29Ω at low currents and reduces to about 23Ω at high currents. Therefore when the output sinks 1mA, the output is about 33mV above the negative supply and while sinking 30mA, it is about 690mV above it.

The output of the LT1213/LT1214 has reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited currents will flow. If the current is transient and limited to several hundred mA, no damage will occur.

Feedback Components

Because the input currents of the LT1213/LT1214 are less than 200nA, it is possible to use high value feedback resistors to set the gain. However, care must be taken to insure that the pole that is formed by the feedback resistors and the input capacitance does not degrade the stability of the amplifier. For example, if a single supply, noninverting gain of two is set with two 10k resistors, the LT1213/LT1214 will probably oscillate. This is because the amplifier goes open-loop at 6MHz (6dB of gain) and has 45° of phase margin. The feedback resistors and the 10pF input capacitance generate a pole at 3MHz that introduces 63° of phase shift at 6MHz! The solution is simple, lower the values of the resistors or add a feedback capacitor of 10pF or more.

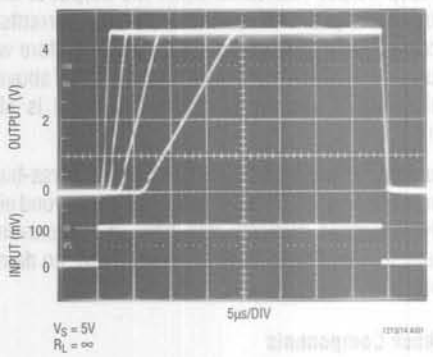
APPLICATIONS INFORMATION

Comparator Applications

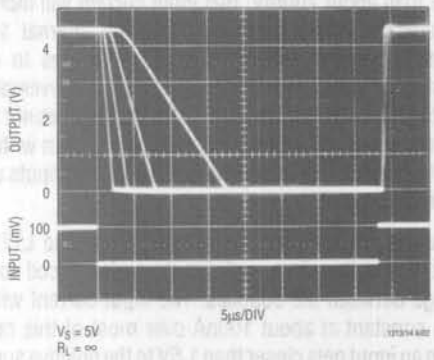
Sometimes it is desirable to use an op amp as a comparator. When operating the LT1213/LT1214 on a single 3.3V or 5V supply, the output interfaces directly with most TTL and CMOS logic.

The response time of the LT1213/LT1214 is a strong function of the amount of input overdrive as shown in the following photos. These amplifiers are unity-gain stable op amps and not fast comparators, therefore, the logic being driven may oscillate due to the long transition time. The output can be speeded up by adding 20mV or more of hysteresis (positive feedback), but the offset is then a function of the input direction.

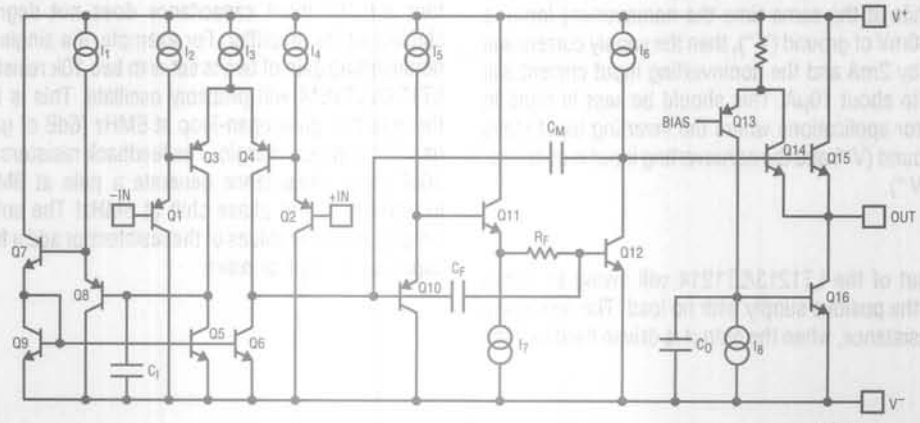
LT1213 Comparator Response (+)
20mV, 10mV, 5mV, 2mV Overdrives



LT1213 Comparator Response (–)
20mV, 10mV, 5mV, 2mV Overdrives

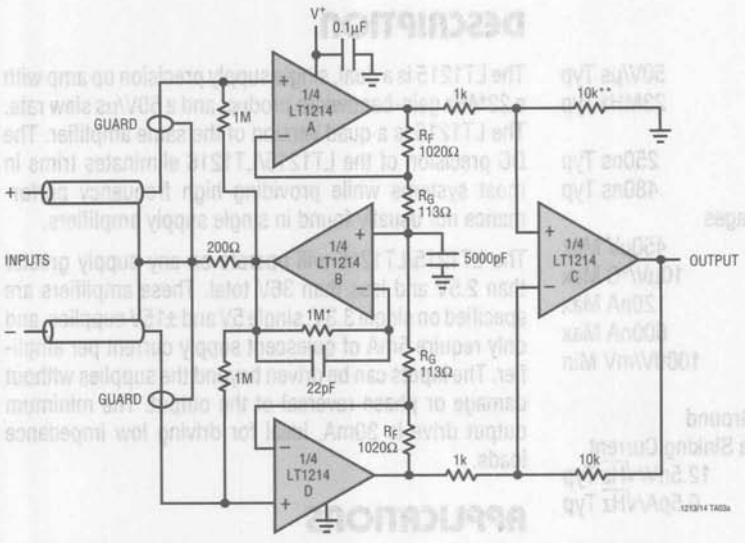


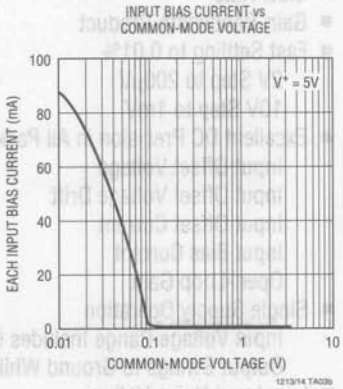
SIMPLIFIED SCHEMATIC



TYPICAL APPLICATIONS

Instrumentation Amplifier with Guard/Shield Driver and Input Bias Current Cancellation



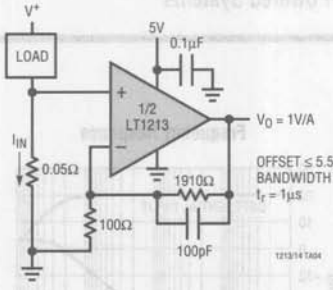


COMMON MODE R_{IN} = 3G
DIFFERENTIAL R_{IN} = 2M
BANDWIDTH = 2MHz
t_r = 170ms

$$GAIN = 10\left(1 + \frac{R_F}{R_G}\right) = 100$$

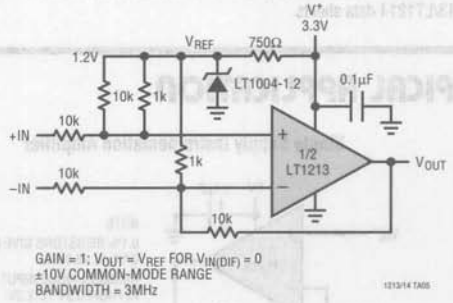
* TRIM FOR INPUT BIAS CURRENT
** TRIM FOR CMRR

Ground Current Sense Amplifier



OFFSET ≤ 5.5mA
BANDWIDTH = 500kHz
t_r = 1µs

Difference Amplifier with Wide Input Common-Mode Range



GAIN = 1; $V_{OUT} = V_{REF}$ FOR $V_{IN(DIF)} = 0$
±10V COMMON-MODE RANGE
BANDWIDTH = 3MHz

23MHz, 50V/µs, Single Supply Dual and Quad Precision Op Amps

FEATURES

- Slew Rate 50V/µs Typ
- Gain-Bandwidth Product 23MHz Typ
- Fast Settling to 0.01%
  - 2V Step to 200µV 250ns Typ
  - 10V Step to 1mV 480ns Typ
- Excellent DC Precision in All Packages
  - Input Offset Voltage 450µV Max
  - Input Offset Voltage Drift 10µV/°C Max
  - Input Offset Current 120nA Max
  - Input Bias Current 600nA Max
  - Open-Loop Gain 1000V/mV Min
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground While Sinking Current
- Low Input Noise Voltage 12.5nV/√Hz Typ
- Low Input Noise Current 0.5pA/√Hz Typ
- Specified on 3.3V, 5V and ±15V
- Large Output Drive Current 30mA Min
- Low Supply Current per Amplifier 6.6mA Max
- Dual in 8-Pin DIP and SO8
- Quad in 14-Pin DIP and NARROW SO16

Note: For applications requiring less slew rate, see the LT1211/LT1212 and LT1213/LT1214 data sheets.

DESCRIPTION

The LT1215 is a dual, single supply precision op amp with a 23MHz gain-bandwidth product and a 50V/µs slew rate. The LT1216 is a quad version of the same amplifier. The DC precision of the LT1215/LT1216 eliminates trims in most systems while providing high frequency performance not usually found in single supply amplifiers.

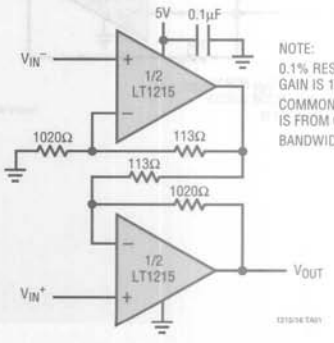
The LT1215/LT1216 will operate on any supply greater than 2.5V and less than 36V total. These amplifiers are specified on single 3.3V, single 5V and ±15V supplies, and only require 5mA of quiescent supply current per amplifier. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The minimum output drive is 30mA, ideal for driving low impedance loads.

APPLICATIONS

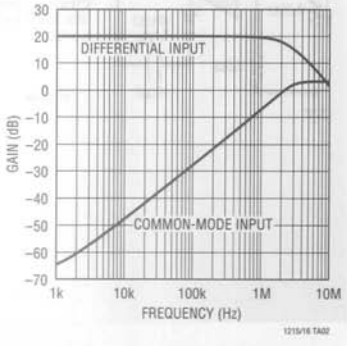
- 2.5V Full-Scale 12-Bit Systems $V_{OS} \leq 0.75$ LSB
- 10V Full-Scale 16-Bit Systems $V_{OS} \leq 3$ LSB
- Active Filters
- Photo Diode Amplifiers
- DAC Current to Voltage Amplifiers
- Battery-Powered Systems

TYPICAL APPLICATION

Single Supply Instrumentation Amplifier



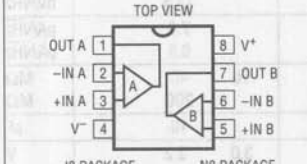
Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1215C/LT1216C ..... −40°C to 85°C
LT1215M ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Junction Temperature (Note 2)
Plastic Package (CN8, CS8, CN, CS) ..... 150°C
Ceramic Package (MJ8) ..... 175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

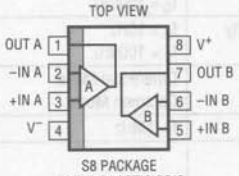


J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER

LT1215CN8
LT1215ACN8
LT1215MJ8
LT1215AMJ8



S8 PACKAGE
8-LEAD PLASTIC SOIC

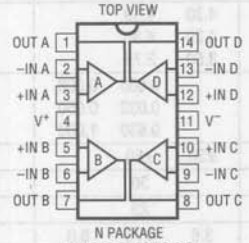
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1215CS8

S8 PART MARKING

1215

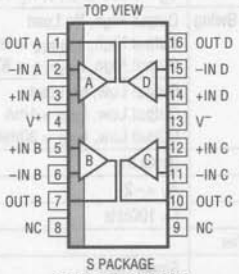


N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1216CN



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1216CS

Consult factory for Industrial grade parts.

AVAILABLE OPTIONS

NUMBER OF OP AMPS	T_A RANGE	MAX V_{OS} (25°C)	MAX TC V_{OS} ($\Delta V_{OS}/\Delta T$)	PACKAGE CERAMIC (J)	PACKAGE PLASTIC DIP (N)	PACKAGE SURFACE MOUNT (S)
Two (Dual)	−40°C to 85°C	300µV	2.5µV/°C		LT1215ACN8	
		450µV	5µV/°C		LT1215CN8	
		450µV	10µV/°C			LT1215CS8
Two (Dual)	−55°C to 125°C	300µV	2.5µV/°C	LT1215AMJ8		
		450µV	5µV/°C	LT1215MJ8		
Four (Quad)	−40°C to 85°C	450µV	10µV/°C		LT1216CN	LT1216CS

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AC LT1215AM MIN	LT1215AC LT1215AM TYP	LT1215AC LT1215AM MAX	LT1215C/LT1215M LT1216C MIN	LT1215C/LT1215M LT1216C TYP	LT1215C/LT1215M LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			125	300		150	450	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability			0.8			1.0		µV/Mo
I_{OS}	Input Offset Current			35	80		35	120	nA
I_B	Input Bias Current			420	500		420	600	nA
	Input Noise Voltage	0.1Hz to 10Hz		400			400		nV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz		15.0 12.5			15.0 12.5		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		7.0 0.5			7.0 0.5		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance (Note 3)	Differential Mode Common Mode	10	40 200		10	40 200		MΩ MΩ
	Input Capacitance	f = 1MHz		10			10		pF
	Input Voltage Range		3.0 0	3.2 −0.2		3.0 0	3.2 −0.2		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3V	90	108		86	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12.5V	96	115		93	115		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	150	600		150	600		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 30mA	4.30 4.20 3.60	4.39 4.30 3.75		4.30 4.20 3.60	4.39 4.30 3.75		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 30mA		0.005 0.030 0.630	0.008 0.050 1.000		0.005 0.030 0.630	0.008 0.050 1.000	V V V
I_O	Maximum Output Current	(Note 9)	±30	±50		±30	±50		mA
SR	Slew Rate	A_V = −2		30			30		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz		23			23		MHz
I_S	Supply Current Per Amplifier		3.6	4.75	6.6	3.6	4.75	6.6	mA
	Minimum Supply Voltage	Single Supply		2.2	2.5		2.2	2.5	V
	Full Power Bandwidth	A_V = 1, V_O = $2.5V_{P-P}$		2.6			2.6		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, V_O = 100mV		16			16		ns
OS	Overshoot	A_V = 1, V_O = 100mV		25			25		%
t_{PD}	Propagation Delay	A_V = 1, V_O = 100mV		13			13		ns
t_S	Settling Time	0.01%, A_V = 1, ΔV_O = 2V		250			250		ns
	Open-Loop Output Resistance	I_O = 0mA, f = 10MHz		40			40		Ω
THD	Total Harmonic Distortion	A_V = 1, V_O = $1V_{RMS}$, 20Hz to 20kHz		0.001			0.001		%

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AC MIN	LT1215AC TYP	LT1215AC MAX	LT1215C/LT1216C MIN	LT1215C/LT1216C TYP	LT1215C/LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			200	350		250	550	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		1	2.5		2	5	µV/°C
		14-Pin DIP, SOIC Package					3	10	µV/°C
I_{OS}	Input Offset Current			35	100		35	140	nA
I_B	Input Bias Current			450	530		450	630	nA
	Input Voltage Range		2.9	3.1		2.9	3.1		V
			0.1	−0.1		0.1	−0.1		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.1V to 2.9V	89	108		85	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.6V to 12.5V	95	114		92	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	100	600		100	600		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.20	4.33		4.20	4.33		V
		Output High, I_{SOURCE} = 1mA	4.10	4.24		4.10	4.24		V
		Output High, I_{SOURCE} = 20mA	3.70	3.89		3.70	3.89		V
		Output Low, No Load		0.006	0.009		0.006	0.009	V
		Output Low, I_{SINK} = 1mA		0.035	0.055		0.035	0.055	V
		Output Low, I_{SINK} = 20mA		0.500	0.725		0.500	0.725	V
I_S	Supply Current Per Amplifier		3.3	5.2	7.5	3.3	5.2	7.5	mA

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1215AC MIN	LT1215AC TYP	LT1215AC MAX	LT1215C/LT1216C MIN	LT1215C/LT1216C TYP	LT1215C/LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			200	400		250	600	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		1	2.5		2	5	µV/°C
		14-Pin DIP, SOIC Package					3	10	µV/°C
I_{OS}	Input Offset Current			35	110		35	150	nA
I_B	Input Bias Current			450	550		450	650	nA
	Input Voltage Range		2.8	3.0		2.8	3.0		V
			0.2	0		0.2	0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.2V to 2.8V	88	108		84	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 12.5V	94	114		91	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	100	600		100	600		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load	4.10	4.30		4.10	4.30		V
		Output High, I_{SOURCE} = 1mA	4.00	4.16		4.00	4.16		V
		Output High, I_{SOURCE} = 20mA	3.60	3.82		3.60	3.82		V
		Output Low, No Load		0.006	0.010		0.006	0.010	V
		Output Low, I_{SINK} = 1mA		0.035	0.060		0.035	0.060	V
		Output Low, I_{SINK} = 20mA		0.500	0.750		0.500	0.750	V
I_S	Supply Current Per Amplifier		2.9	5.3	7.6	2.9	5.3	7.6	mA

5V ELECTRICAL CHARACTERISTICS

V_S = 5V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AM MIN	LT1215AM TYP	LT1215AM MAX	LT1215M MIN	LT1215M TYP	LT1215M MAX	UNITS
V_{OS}	Input Offset Voltage			250	450		350	750	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			1	2.5		2	5	µV/°C
I_{OS}	Input Offset Current			35	150		35	200	nA
I_B	Input Bias Current			450	600		450	700	nA
	Input Voltage Range		2.8 0.4	3.0 0.2		2.8 0.4	3.0 0.2		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.4V to 2.8V	87	108		82	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 12.5V	93	114		90	114		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.05V to 3.7V, R_L = 500Ω	50	100		50	100		V/mV
	Maximum Output Voltage Swing (Note 4)	Output High, No Load Output High, I_{SOURCE} = 1mA Output High, I_{SOURCE} = 20mA	4.00 3.90 3.50	4.20 4.10 3.80		4.00 3.90 3.50	4.20 4.10 3.80		V V V
		Output Low, No Load Output Low, I_{SINK} = 1mA Output Low, I_{SINK} = 20mA		0.007 0.040 0.700	0.012 0.070 1.000		0.007 0.040 0.700	0.012 0.070 1.000	mV mV mV
I_S	Supply Current Per Amplifier		2.3	5.5	8.4	2.3	5.5	8.4	mA

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AC LT1215AM MIN	LT1215AC LT1215AM TYP	LT1215AC LT1215AM MAX	LT1215C/LT1215M LT1216C MIN	LT1215C/LT1215M LT1216C TYP	LT1215C/LT1215M LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			225	500		250	650	µV
I_{OS}	Input Offset Current			30	80		30	110	nA
I_B	Input Bias Current			360	500		360	550	nA
	Input Voltage Range		13.0 −15.0	13.2 −15.2		13.0 −15.0	13.2 −15.2		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −15V to 13V	90	108		86	108		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	96	110		93	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	1000	3500		1000	3500		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 30mA	13.5	13.75		13.5	13.75		V
		Output Low, I_{SINK} = 30mA	−14	−14.4		−14	−14.4		V
I_O	Maximum Output Current	(Note 9)	±30	±50		±30	±50		mA
SR	Slew Rate	A_V = −2 (Note 6)	40	50		40	50		V/µs
GBW	Gain-Bandwidth Product	f = 100kHz	15	23		15	23		MHz
I_S	Supply Current Per Amplifier		3.6	5.7	8	3.6	5.7	8	mA
	Channel Separation	V_O = ±10V, R_L = 2k	128	140		128	140		dB
	Minimum Supply Voltage	Equal Split Supplies		±1.7	±2		±1.7	±2	V
	Full-Power Bandwidth	A_V = 1, V_O = $20V_{P-P}$		750			750		kHz
	Settling Time	0.01%, A_V = 1, ΔV_O = 10V		480			480		ns

±15V ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AC MIN	LT1215AC TYP	LT1215AC MAX	LT1215C/LT1216C MIN	LT1215C/LT1216C TYP	LT1215C/LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			325	550		400	750	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		1	2.5		2	5	µV/°C
		14-Pin DIP, SOIC Package					3	10	µV/°C
I_{OS}	Input Offset Current			30	100		30	130	nA
I_B	Input Bias Current			360	530		360	580	nA
	Input Voltage Range		12.9 −14.9	13.1 −15.1		12.9 −14.9	13.1 −15.1		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.9V to 12.9V	89	108		85	108		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.1V to ±18V	95	110		92	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	800	3000		800	3000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 20mA	13.7	13.9		13.7	13.9		V
		Output Low, I_{SINK} = 20mA	−14.2	−14.5		−14.2	−14.5		V
I_S	Supply Current Per Amplifier		3.3	6.3	9.2	3.3	6.3	9.2	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LT1215AC MIN	LT1215AC TYP	LT1215AC MAX	LT1215C/LT1216C MIN	LT1215C/LT1216C TYP	LT1215C/LT1216C MAX	UNITS
V_{OS}	Input Offset Voltage			325	600		400	800	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)	8-Pin DIP Package		1	2.5		2	5	µV/°C
		14-Pin DIP, SOIC Package					3	10	µV/°C
I_{OS}	Input Offset Current			30	110		30	140	nA
I_B	Input Bias Current			360	550		360	600	nA
	Input Voltage Range		12.8 −14.8	13.0 −15.0		12.8 −14.8	13.0 −15.0		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.8V to 12.8V	88	108		84	108		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.2V to ±18V	94	110		91	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	800	2500		800	2500		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 20mA	13.6	13.8		13.6	13.8		V
		Output Low, I_{SINK} = 20mA	−14.1	−14.5		−14.1	−14.5		V
I_S	Supply Current Per Amplifier		2.9	6.5	9.5	2.9	6.5	9.5	mA

V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1215AM MIN	LT1215AM TYP	LT1215AM MAX	LT1215M MIN	LT1215M TYP	LT1215M MAX	UNITS
V_{OS}	Input Offset Voltage			350	650		500	950	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 3)			1	2.5		2	5	µV/°C
I_{OS}	Input Offset Current			30	150		30	200	nA
I_B	Input Bias Current			360	600		360	700	nA
	Input Voltage Range		12.8 −14.6	13.0 −14.8		12.8 −14.6	13.0 −14.8		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −14.6V to 12.8V	87	108		82	108		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.2V to ±15V	93	110		90	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0V to ±10V, R_L = 2k	500	2000		500	2000		V/mV
	Maximum Output Voltage Swing	Output High, I_{SOURCE} = 20mA	13.4	13.8		13.4	13.8		V
		Output Low, I_{SINK} = 20mA	−14	−14.5		−14	−14.5		V
I_S	Supply Current Per Amplifier		2.3	7	10.3	2.3	7	10.3	mA

3.3V ELECTRICAL CHARACTERISTICS

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 25°C, unless otherwise noted. (Note 7)

			LT1215AC LT1215AM			LT1215C/LT1215M LT1216C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			125	300		150	450	µV
	Input Voltage Range (Note 8)		1.3	1.5		1.3	1.5		V
			0	−0.2		0	−0.2		V
	Maximum Output Voltage Swing	Output High, No Load	2.60	2.69		2.60	2.69		V
		Output High, I_{SOURCE} = 1mA	2.50	2.60		2.50	2.60		V
		Output High, I_{SOURCE} = 30mA	1.90	2.05		1.90	2.05		V
		Output Low, No Load		0.005	0.008		0.005	0.008	V
		Output Low, I_{SINK} = 1mA		0.035	0.050		0.035	0.050	V
		Output Low, I_{SINK} = 30mA		0.700	1.000		0.700	1.000	V
I_O	Maximum Output Current		±30	±50		±30	±50		mA

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted. (Note 7)

			LT1215AC			LT1215C/LT1216C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			200	350		250	550	µV
	Input Voltage Range (Note 8)		1.2	1.4		1.2	1.4		V
			0.1	−0.1		0.1	−0.1		V
	Maximum Output Voltage Swing	Output High, No Load	2.50	2.63		2.50	2.63		V
		Output High, I_{SOURCE} = 1mA	2.40	2.54		2.40	2.54		V
		Output High, I_{SOURCE} = 20mA	2.00	2.19		2.00	2.19		V
		Output Low, No Load		0.006	0.009		0.006	0.009	V
		Output Low, I_{SINK} = 1mA		0.035	0.055		0.035	0.055	V
		Output Low, I_{SINK} = 20mA		0.500	0.725		0.500	0.725	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 5, 7)

			LT1215AC			LT1215C/LT1216C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			200	400		250	600	µV
	Input Voltage Range (Note 8)		1.1	1.3		1.1	1.3		V
			0.2	0		0.2	0		V
	Maximum Output Voltage Swing	Output High, No Load	2.40	2.50		2.40	2.50		V
		Output High, I_{SOURCE} = 1mA	2.30	2.46		2.30	2.46		V
		Output High, I_{SOURCE} = 20mA	1.90	2.12		1.90	2.12		V
		Output Low, No Load		0.006	0.010		0.006	0.010	V
		Output Low, I_{SINK} = 1mA		0.035	0.060		0.035	0.060	V
		Output Low, I_{SINK} = 20mA		0.500	0.750		0.500	0.750	V

V_S = 3.3V, V_{CM} = 0.5V, V_{OUT} = 0.5V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted. (Note 7)

			LT1215AM			LT1215M			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			250	450		350	750	µV
	Input Voltage Range (Note 8)		1.1	1.3		1.1	1.3		V
			0.4	0.2		0.4	0.2		V
	Maximum Output Voltage Swing	Output High, No Load	2.30	2.50		2.30	2.50		V
		Output High, I_{SOURCE} = 1mA	2.20	2.40		2.20	2.40		V
		Output High, I_{SOURCE} = 20mA	1.80	2.10		1.80	2.10		V
		Output Low, No Load		0.007	0.012		0.007	0.012	V
		Output Low, I_{SINK} = 1mA		0.040	0.070		0.040	0.070	V
		Output Low, I_{SINK} = 20mA		0.700	1.000		0.700	1.000	V

ELECTRICAL CHARACTERISTICS

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1215MJ8, LT1215AMJ8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1215CN8, LT1215ACN8:	$T_J = T_A + (P_D \times 100°C/W)$
LT1215CS8:	$T_J = T_A + (P_D \times 150°C/W)$
LT1216CN:	$T_J = T_A + (P_D \times 70°C/W)$
LT1216CS:	$T_J = T_A + (P_D \times 100°C/W)$

Note 3: This parameter is not 100% tested.

Note 4: Guaranteed by correlation to 3.3V and ±15V tests.

Note 5: The LT1215/LT1216 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

Note 6: Slew rate is measured between ±8.5V on an output swing of ±10V on ±15V supplies.

Note 7: Most LT1215/LT1216 electrical characteristics change very little with supply voltage. See the 5V tables for characteristics not listed in the 3.3V table.

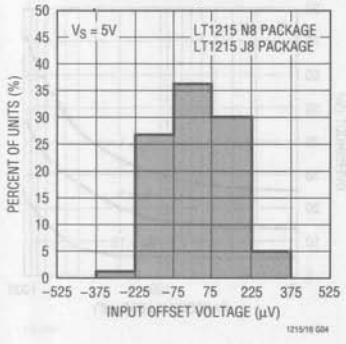
Note 8: Guaranteed by correlation to 5V and ±15V tests.

Note 9: Guaranteed by correlation to 3.3V tests.

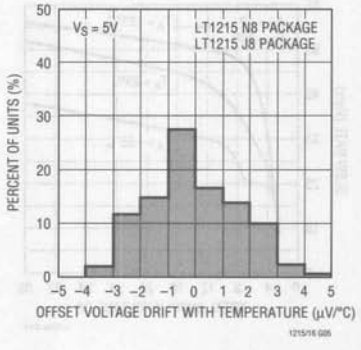
TYPICAL PERFORMANCE CHARACTERISTICS

2

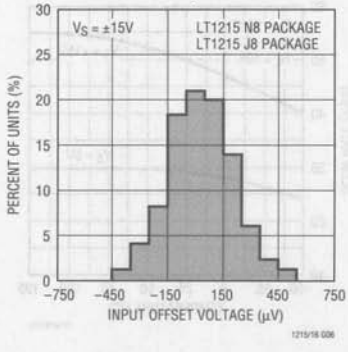
Distribution of Input Offset Voltage



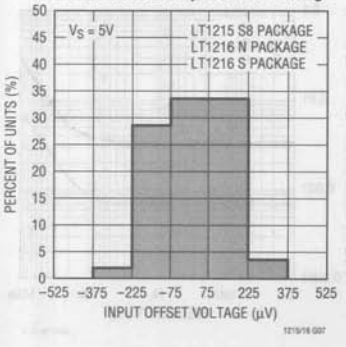
Distribution of Offset Voltage Drift with Temperature



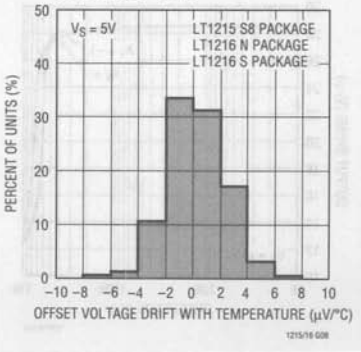
Distribution of Input Offset Voltage



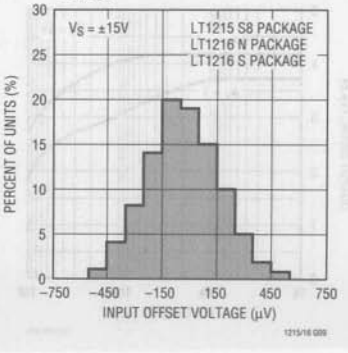
Distribution of Input Offset Voltage



Distribution of Offset Voltage Drift with Temperature



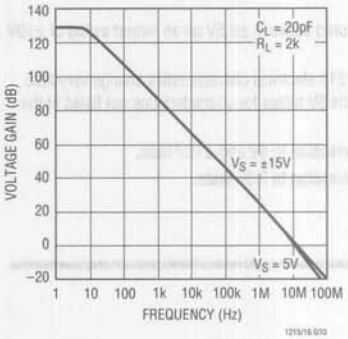
Distribution of Input Offset Voltage



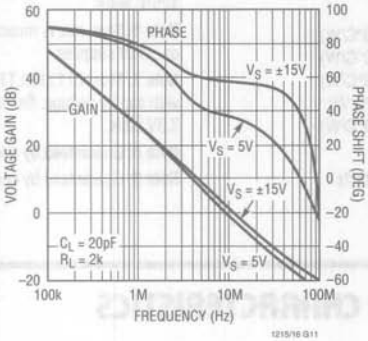
LT1215/LT1216

TYPICAL PERFORMANCE CHARACTERISTICS

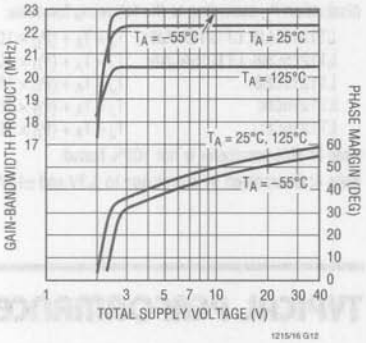
Voltage Gain vs Frequency



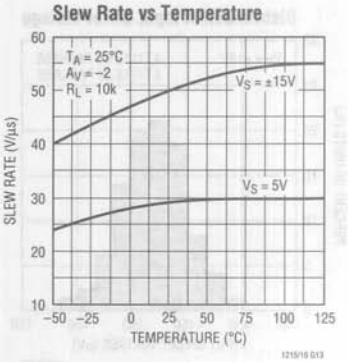
Voltage Gain, Phase vs Frequency



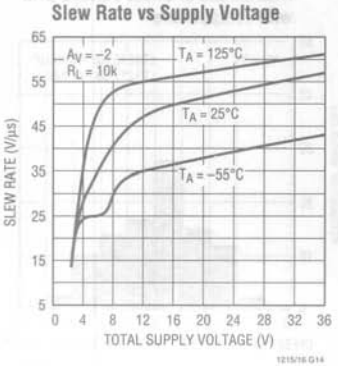
Gain-Bandwidth Product, Phase Margin vs Supply Voltage



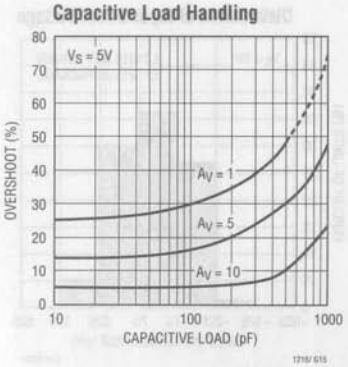
Slew Rate vs Temperature



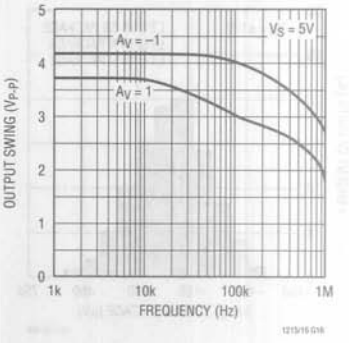
Slew Rate vs Supply Voltage



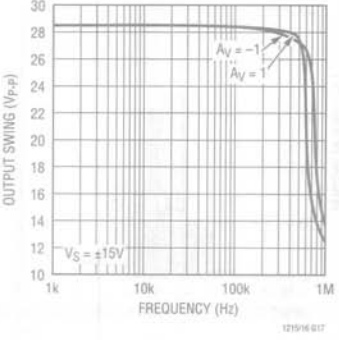
Capacitive Load Handling



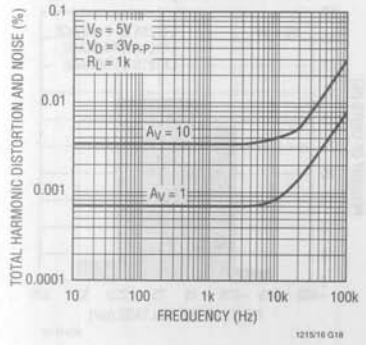
Undistorted Output Swing vs Frequency, V_S = 5V



Undistorted Output Swing vs Frequency, V_S = ±15V

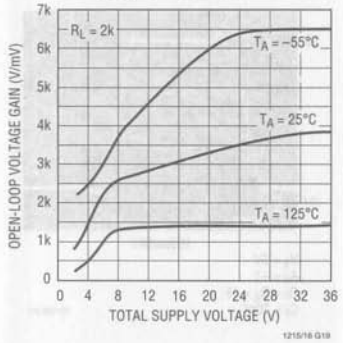


Total Harmonic Distortion and Noise vs Frequency

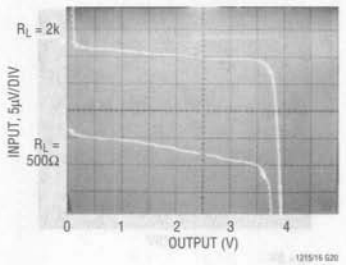


TYPICAL PERFORMANCE CHARACTERISTICS

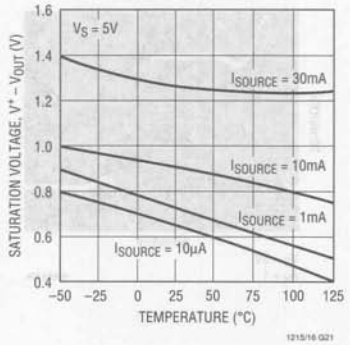
Open-Loop Voltage Gain vs Supply Voltage



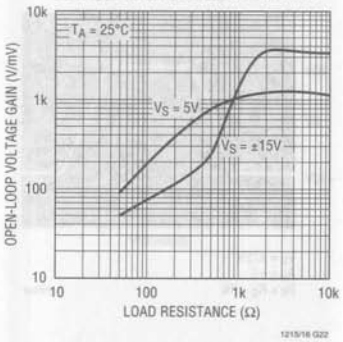
Open-Loop Gain, V_S = 5V



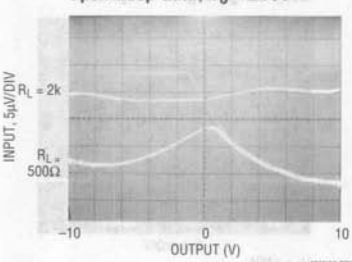
Positive Output Saturation Voltage vs Temperature



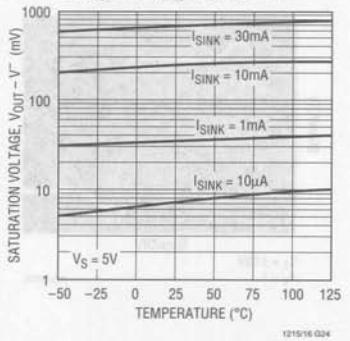
Voltage Gain vs Load Resistance



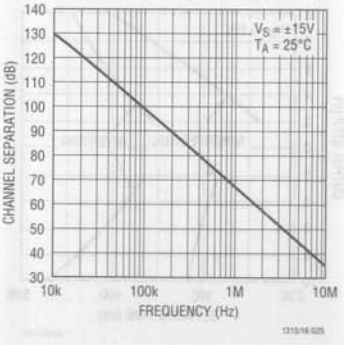
Open-Loop Gain, V_S = ±15V



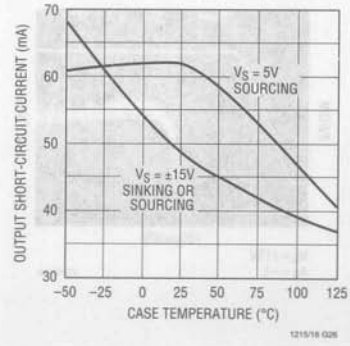
Negative Output Saturation Voltage vs Temperature



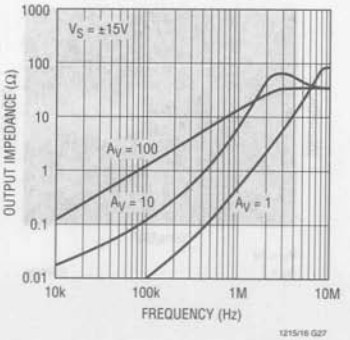
Channel Separation vs Frequency



Output Short-Circuit Current vs Temperature



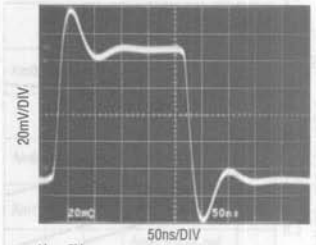
Output Impedance vs Frequency



2

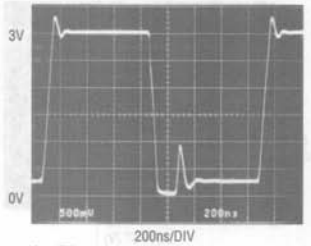
TYPICAL PERFORMANCE CHARACTERISTICS

5V Small-Signal Response



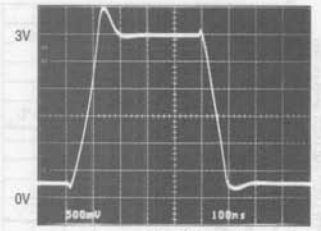
$V_S = 5V$
$A_V = 1$

5V Large-Signal Response



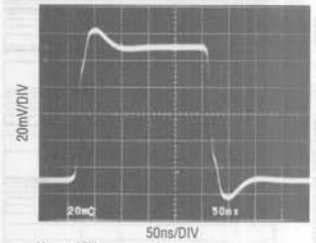
$V_S = 5V$
$A_V = 1$

5V Large-Signal Response



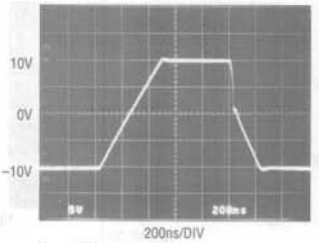
$V_S = 5V$
$A_V = -1$
$R_F = R_G = 1k$
$C_F = 20pF$

±15V Small-Signal Response



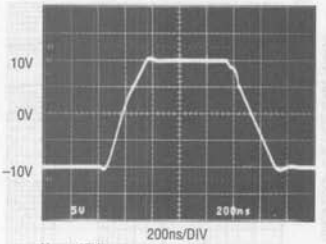
$V_S = \pm 15V$
$A_V = 1$

±15V Large-Signal Response



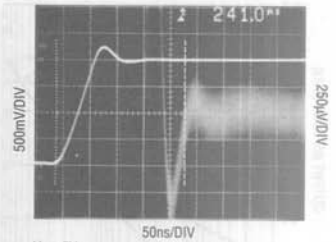
$V_S = \pm 15V$
$A_V = 1$

±15V Large-Signal Response



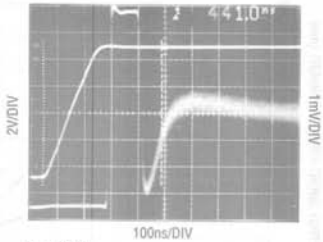
$V_S = \pm 15V$
$A_V = -1$
$R_F = R_G = 1k$

5V Settling



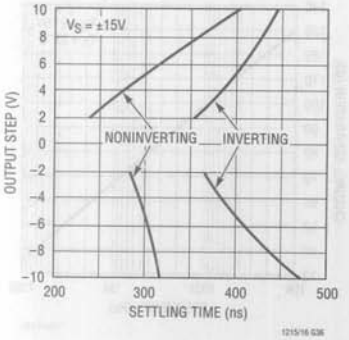
$V_S = 5V$
$A_V = 1$

±15V Settling



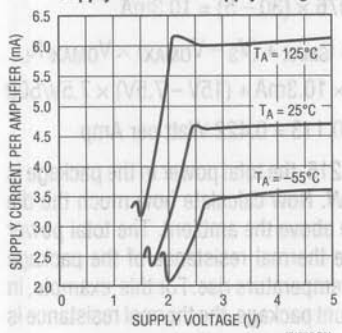
$V_S = \pm 15V$
$A_V = -1$

Settling Time to 0.01% vs Output Step

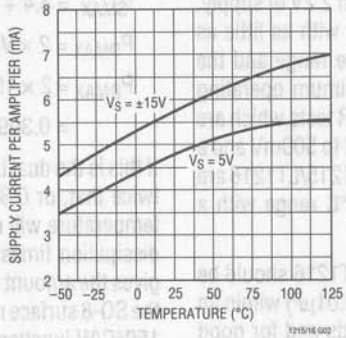


TYPICAL PERFORMANCE CHARACTERISTICS

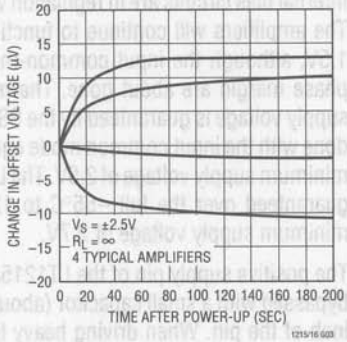
Supply Current vs Supply Votage



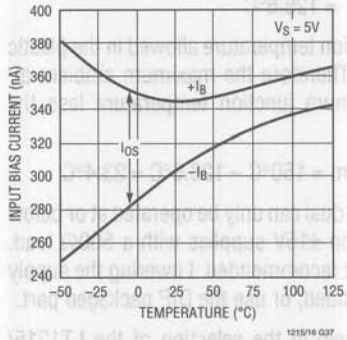
Supply Current vs Temperature



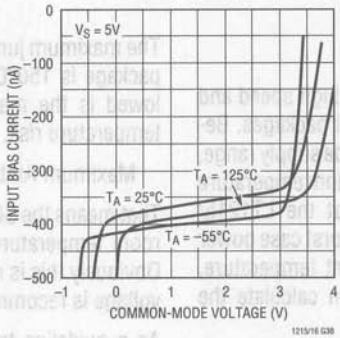
Warm-Up Drift vs Time



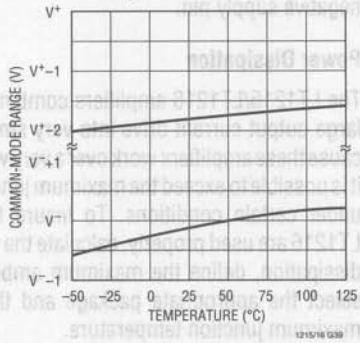
Input Bias Current vs Temperature



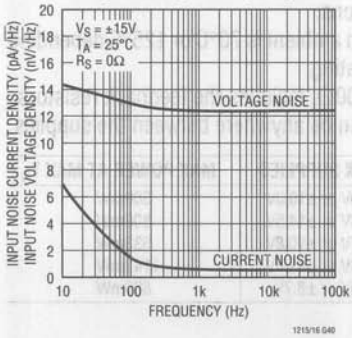
Input Bias Current vs Common-Mode Voltage



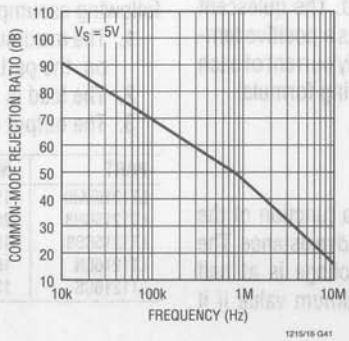
Common-Mode Range vs Temperature



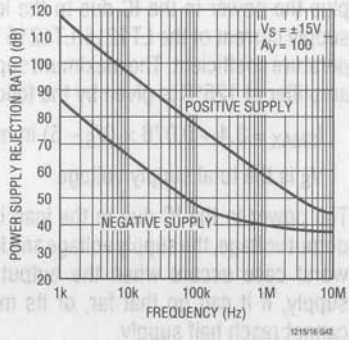
Input Noise Current, Noise Voltage Density vs Frequency



Common-Mode Rejection Ratio vs Frequency



Input Referred Power Supply Rejection Ratio vs Frequency



2

APPLICATIONS INFORMATION

Supply Voltage

The LT1215/LT1216 op amps are fully functional and all internal bias circuits are in regulation with 2.2V of supply. The amplifiers will continue to function with as little as 1.5V, although the input common-mode range and the phase margin are about gone. The minimum operating supply voltage is guaranteed by the PSRR tests which are done with the input common mode equal to 500mV and a minimum supply voltage of 2.5V. The LT1215/LT1216 are guaranteed over the full –55°C to 125°C range with a minimum supply voltage of 2.7V.

The positive supply pin of the LT1215/LT1216 should be bypassed with a small capacitor (about 0.01μF) within an inch of the pin. When driving heavy loads and for good settling time, an additional 4.7μF capacitor should be used. When using split supplies, the same is true for the negative supply pin.

Power Dissipation

The LT1215/LT1216 amplifiers combine high speed and large output current drive into very small packages. Because these amplifiers work over a very wide supply range, it is possible to exceed the maximum junction temperature under certain conditions. To insure that the LT1215/LT1216 are used properly, calculate the worst case power dissipation, define the maximum ambient temperature, select the appropriate package and then calculate the maximum junction temperature.

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1215/LT1216 has a positive temperature coefficient. The maximum supply current of each amplifier at 125°C is given by the following formula:

$$I_{SMAX} = 8.4 + 0.076 \times (V_S - 5) \text{ in mA}$$

V_S is the total supply voltage.

The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, calculate the worst case power dissipation while operating on ±15V supplies and driving a 500Ω load.

$$I_{SMAX} = 8.4 + 0.076 \times (30 - 5) = 10.3\text{mA}$$

$$P_{DMAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OMAX}) \times V_{OMAX}/R_L$$

$$P_{DMAX} = 2 \times 15\text{V} \times 10.3\text{mA} + (15\text{V} - 7.5\text{V}) \times 7.5\text{V}/500$$

$$= 0.309 + 0.113 = 0.422 \text{ Watt per Amp}$$

If this is the dual LT1215, the total power in the package is twice that, or 0.844W. Now calculate how much the die temperature will rise above the ambient. The total power dissipation times the thermal resistance of the package gives the amount of temperature rise. For this example, in the SO-8 surface mount package, the thermal resistance is 150°C/W junction-to-ambient in still air.

$$\text{Temperature Rise} = P_{DMAX} \times \theta_{JA} = 0.844\text{W} \times 150°\text{C/W}$$

$$= 126.6°\text{C}$$

The maximum junction temperature allowed in the plastic package is 150°C. Therefore the maximum ambient allowed is the maximum junction temperature less the temperature rise.

$$\text{Maximum Ambient} = 150°\text{C} - 126.6°\text{C} = 23.4°\text{C}$$

That means the SO8 dual can only be operated at or below room temperature on ±15V supplies with a 500Ω load. Obviously this is not recommended. Lowering the supply voltage is recommended, or use the DIP packaged part.

As a guideline to help in the selection of the LT1215/LT1216, the following table describes the maximum supply voltage that can be used with each part based on the following assumptions:

1. The maximum ambient is 70°C or 125°C depending on the part rating.
2. The load is 500Ω, includes the feedback resistors.
3. The output can be anywhere between the supplies.

PART	MAX SUPPLIES	MAX POWER AT MAX T_A
LT1215MJ8	15.0V or ±10.3V	500mW
LT1215CN8	20.3V or ±14.5V	800mW
LT1215CS8	15.7V or ±10.8V	533mW
LT1216CN	16.4V or ±11.4V	1143mW
LT1216CS	13.0V or ±8.7V	800mW

APPLICATIONS INFORMATION

Inputs

Typically at room temperature, the inputs of the LT1215/LT1216 can common mode 400mV below ground (V^-) and to within 1.5V of the positive supply with the amplifier still functional. However the input bias current and offset voltage will shift as shown in the characteristic curves. For full precision performance, the common-mode range should be limited between ground (V^-) and 2V below the positive supply.

When either of the inputs is taken below ground (V^-) by more than about 700mV, that input current will increase dramatically. The current is limited by internal 100Ω resistors between the input pins and diodes to each supply. The output will remain low (no phase reversal) for inputs 1.3V below ground (V^-). If the output does not have to sink current, such as in a single supply system with a 1k load to ground, there is no phase reversal for inputs up to 8V below ground.

There are no clamps across the inputs of the LT1215/LT1216 and therefore each input can be forced to any voltage between the supplies. The input current will remain constant at about 360nA over most of this range. When an input gets closer than 2V to the positive supply, that input current will gradually decrease to zero until the input goes above the supply, then it will increase due to the previously mentioned diodes. If the inverting input is held more positive than the noninverting input by 200mV or more, while at the same time the noninverting input is within 300mV of ground (V^-), then the supply current will increase by 5mA and the noninverting input current will increase to about 100μA. This should be kept in mind in comparator applications where the inverting input stays above ground (V^-) and the noninverting input does not.

Output

The output of the LT1215/LT1216 will swing to within 0.61V of the positive supply with no load. The open-loop output resistance, when the output is driven hard into the positive rail, is about 100Ω as the output starts to source current; this resistance drops to about 20Ω as the current increases. Therefore when the output sources 1mA, the output will swing to within 0.7V of the positive supply. While sourcing 30mA, it is within 1.25V of the positive supply.

The output of the LT1215/LT1216 will swing to within 5mV of the negative supply while sinking zero current. Thus, in a typical single supply application with the load going to ground, the output will go to within 5mV of ground. The open-loop output resistance when the output is driven hard into the negative rail is about 25Ω at low currents and reduces to about 21Ω at high currents. Therefore when the output sinks 1mA, the output is about 30mV above the negative supply and while sinking 30mA, it is about 630mV above it.

The output of the LT1215/LT1216 has reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited currents will flow. If the current is transient and limited to several hundred mA, no damage will occur.

Feedback Components

Because the input currents of the LT1215/LT1216 are less than 600nA, it is possible to use high value feedback resistors to set the gain. However, care must be taken to insure that the pole that is formed by the feedback resistors and the input capacitance does not degrade the stability of the amplifier. For example, if a single supply, noninverting gain of two is set with two 10k resistors, the LT1215/LT1216 will probably oscillate. This is because the amplifier goes open-loop at 7MHz (6dB of gain) and has 50° of phase margin. The feedback resistors and the 10pF input capacitance generate a pole at 3MHz that introduces 67° of phase shift at 7MHz! The solution is simple, lower the values of the resistors or add a feedback capacitor of 10pF or more.

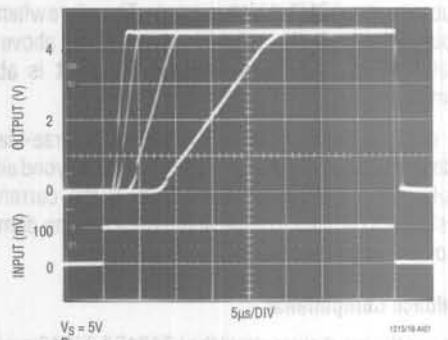
APPLICATIONS INFORMATION

Comparator Applications

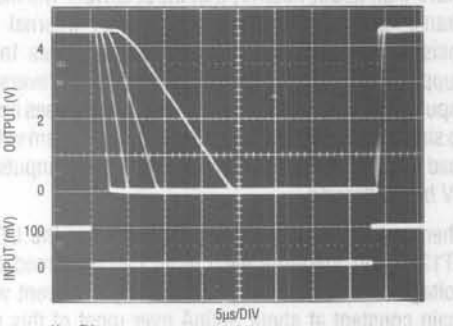
Sometimes it is desirable to use an op amp as a comparator. When operating the LT1215/LT1216 on a single 3.3V or 5V supply, the output interfaces directly with most TTL and CMOS logic.

The response time of the LT1215/LT1216 is a strong function of the amount of input overdrive as shown in the following photos. These amplifiers are unity-gain stable op amps and not fast comparators, therefore, the logic being driven may oscillate due to the long transition time. The output can be speeded up by adding 20mV or more of hysteresis (positive feedback), but the offset is then a function of the input direction.

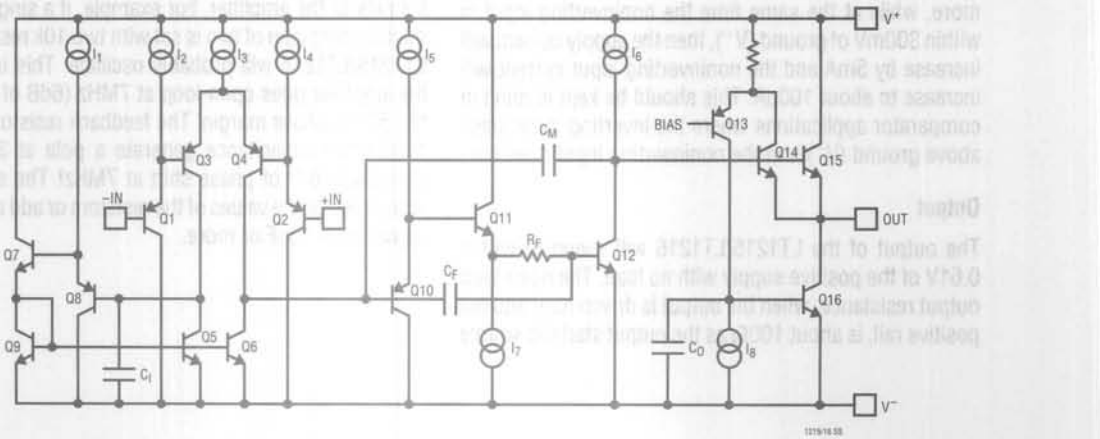
LT1215 Comparator Response (+)
20mV, 10mV, 5mV, 2mV Overdrives



LT1215 Comparator Response (–)
20mV, 10mV, 5mV, 2mV Overdrives

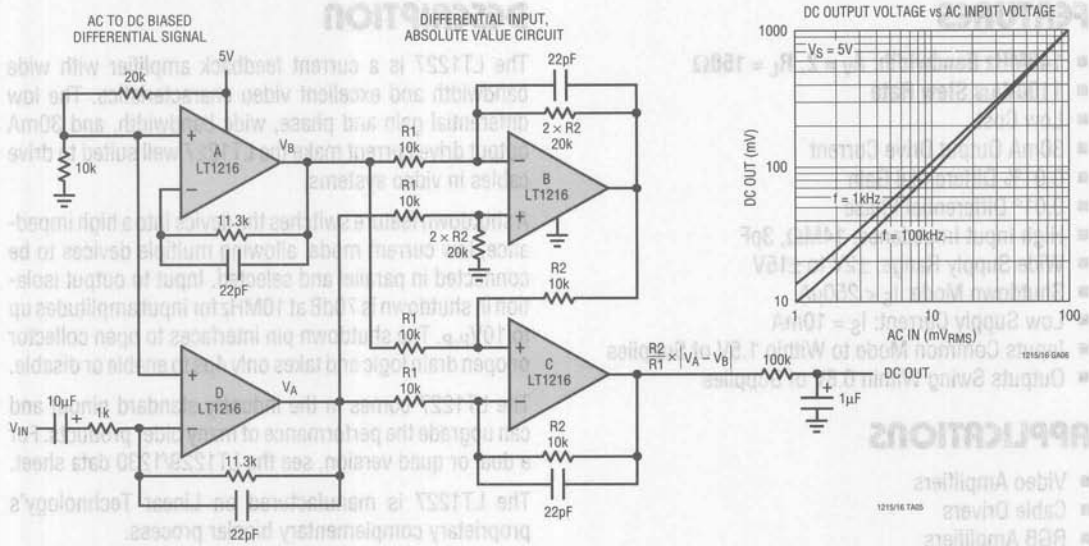


SIMPLIFIED SCHEMATIC

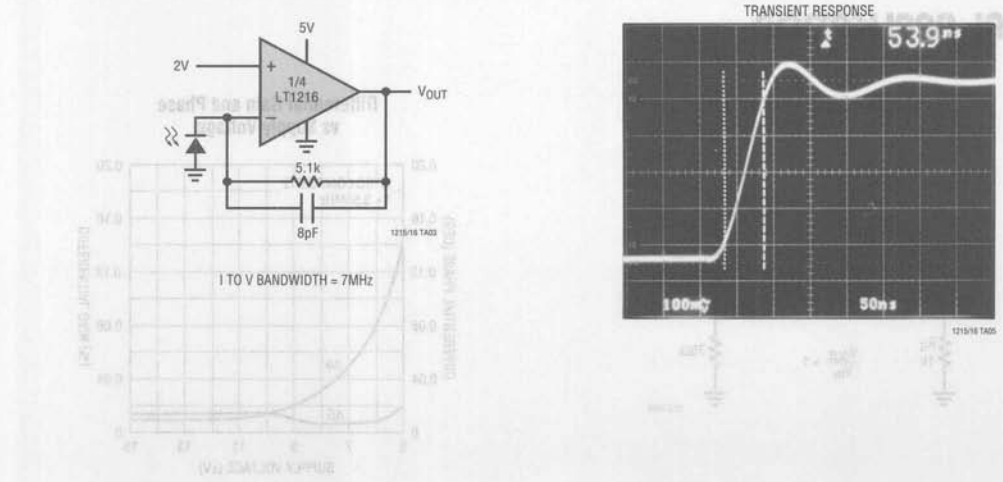


TYPICAL APPLICATIONS

Single Supply, AC Coupled Input, RMS Calibrated, Average Detector



LT1216 Photo Diode Amplifier



140MHz Video Current Feedback Amplifier

FEATURES

- **140MHz Bandwidth: $A_V = 2$, $R_L = 150\Omega$**
- **1100V/μs Slew Rate**
- Low Cost
- 30mA Output Drive Current
- 0.01% Differential Gain
- 0.01° Differential Phase
- High Input Impedance: 14MΩ, 3pF
- Wide Supply Range: ±2V to ±15V
- Shutdown Mode: $I_S < 250\mu A$
- Low Supply Current: $I_S = 10mA$
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies

APPLICATIONS

- Video Amplifiers
- Cable Drivers
- RGB Amplifiers
- Test Equipment Amplifiers
- 50Ω Buffers for Driving Mixers

DESCRIPTION

The LT1227 is a current feedback amplifier with wide bandwidth and excellent video characteristics. The low differential gain and phase, wide bandwidth, and 30mA output drive current make the LT1227 well suited to drive cables in video systems.

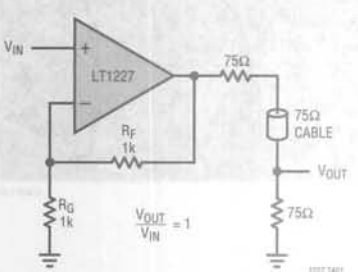
A shutdown feature switches the device into a high impedance, low current mode, allowing multiple devices to be connected in parallel and selected. Input to output isolation in shutdown is 70dB at 10MHz for input amplitudes up to $10V_{P-P}$. The shutdown pin interfaces to open collector or open drain logic and takes only 4μs to enable or disable.

The LT1227 comes in the industry standard pinout and can upgrade the performance of many older products. For a dual or quad version, see the LT1229/1230 data sheet.

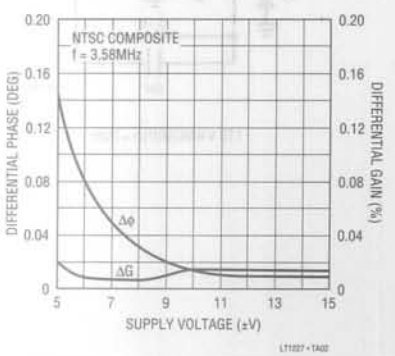
The LT1227 is manufactured on Linear Technology's proprietary complementary bipolar process.

TYPICAL APPLICATION

Video Cable Driver



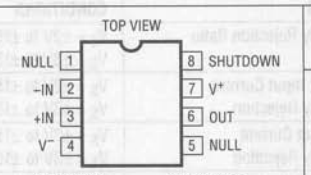
Differential Gain and Phase vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

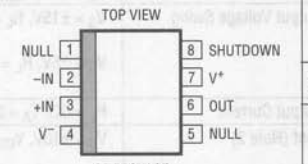
Supply Voltage ..... ±18V
Input Current ..... ±15mA
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1227C ..... 0°C to 70°C
LT1227M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature
Plastic Package ..... 150°C
Ceramic Package ..... 175°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1227MJ8 LT1227CN8
LT1227CS8
S8 PART MARKING
1227

Consult factory for Industrial grade parts.

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ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN+}	Noninverting Input Current	T_A = 25°C			±0.3	±3	µA
			●			±10	µA
I_{IN-}	Inverting Input Current	T_A = 25°C			±10	±60	µA
			●			±100	µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			3.2		nV/√Hz
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.7		pA/√Hz
$-i_n$	Inverting Input Noise Current Density	f = 1kHz			32		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±13V, V_S = ±15V	●	1.5	14		MΩ
		V_{IN} = ±3V, V_S = ±5V	●	1.5	11		MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range	V_S = ±15V, T_A = 25°C		±13	±13.5		V
			●	±12			V
		V_S = ±5V, T_A = 25°C		±3	±3.5		V
			●	±2			V
CMRR	Common-Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C		55	62		dB
		V_S = ±15V, V_{CM} = ±12V	●	55			dB
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C		55	61		dB
		V_S = ±5V, V_{CM} = ±2V	●	55			dB
	Inverting Input Current Common-Mode Rejection	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C			3.5	10	µA/V
		V_S = ±15V, V_{CM} = ±12V	●			10	µA/V
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C			4.5	10	µA/V
		V_S = ±5V, V_{CM} = ±2V	●			10	µA/V

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V, T_A = 25°C		60	80		dB
		V_S = ±3V to ±15V	●	60			dB
	Noninverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			2	50	nA/V
		V_S = ±3V to ±15V	●			50	nA/V
	Inverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			0.25	5	µA/V
		V_S = ±3V to ±15V	●			5	µA/V
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	55	72		dB
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	55	72		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN^-}$	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	100	270		kΩ
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	100	240		kΩ
V_{OUT}	Maximum Output Voltage Swing	V_S = ±15V, R_L = 400Ω, T_A = 25°C		±12	±13.5		V
			●	±10			V
		V_S = ±5V, R_L = 150Ω, T_A = 25°C		±3	±3.7		V
			●	±2.5			V
I_{OUT}	Maximum Output Current	R_L = 0Ω, T_A = 25°C		30	60		mA
I_S	Supply Current (Note 2)	V_S = ±15V, V_{OUT} = 0V, T_A = 25°C			10	15.0	mA
			●			17.5	mA
	Positive Supply Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V, T_A = 25°C			120	300	µA
			●			500	µA
I_8	Shutdown Pin Current (Note 3)	V_S = ±15V	●			300	µA
	Output Leakage Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V, T_A = 25°C				10	µA
SR	Slew Rate (Notes 4 and 5)	T_A = 25°C		500	1100		V/µs
t_r, t_f	Rise and Fall Time, V_{OUT} = 1V_{P-P}	V_S = ±5V, R_F = 1k, R_G = 1k, R_L = 150Ω			8.7		ns
BW	Small-Signal Bandwidth	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			140		MHz
t_r, t_f	Small-Signal Rise and Fall Time	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			3.3		ns
	Propagation Delay	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			3.4		ns
	Small-Signal Overshoot	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			5		%
t_S	Settling Time	0.1%, V_{OUT} = 10V, R_F = 1k, R_G = 1k, R_L = 1k			50		ns
	Differential Gain (Note 6)	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			0.014		%
		V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 1k			0.010		%
	Differential Phase (Note 6)	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			0.010		DEG
		V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 1k			0.013		DEG

The ● denotes specifications which apply over the operating temperature range.

Note 1: A heat sink may be required depending on the power supply voltage.

Note 2: The supply current of the LT1227 has a negative temperature coefficient. For more information, see Typical Performance Characteristics curves.

Note 3: Ramp pin 8 voltage down from 15V while measuring I_S. When I_S drops to less than 0.5mA, measure pin 8 current.

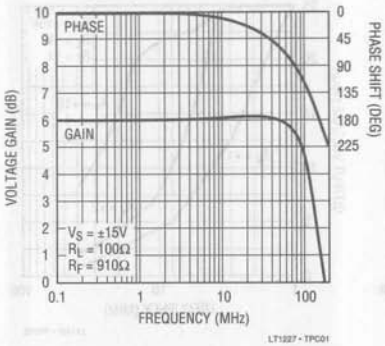
Note 4: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with R_F = 2k, R_G = 220Ω and R_L = 400Ω.

Note 5: AC parameters are 100% tested on the ceramic and plastic DIP package parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

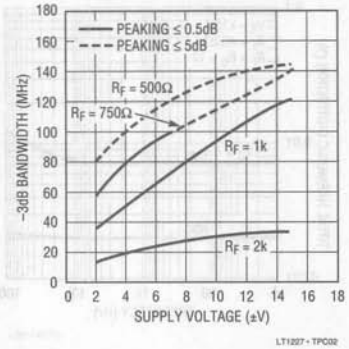
Note 6: NTSC composite video with an output level of 2V.

TYPICAL PERFORMANCE CHARACTERISTICS

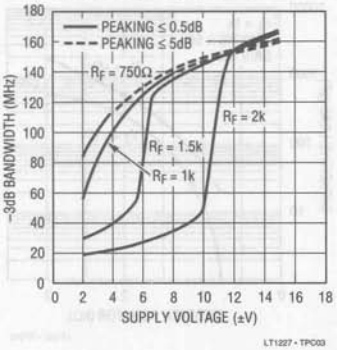
Voltage Gain and Phase vs Frequency, Gain = 6dB



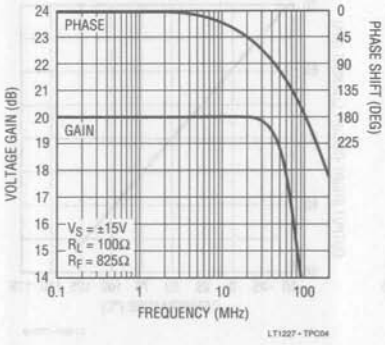
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 100Ω



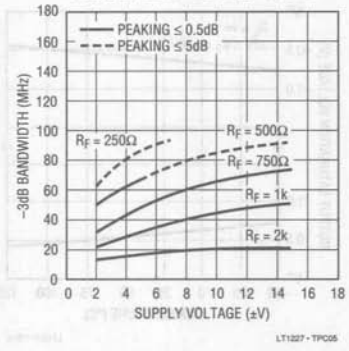
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 1k



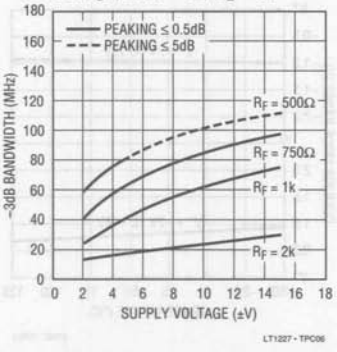
Voltage Gain and Phase vs Frequency, Gain = 20dB



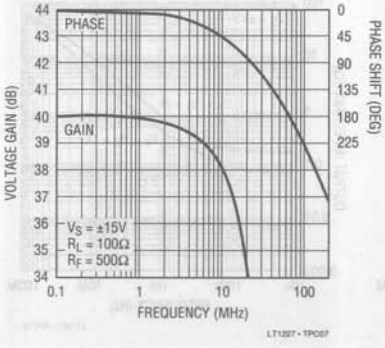
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 100Ω



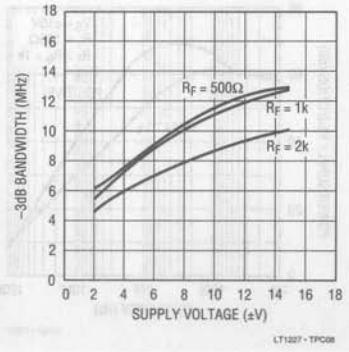
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 1k



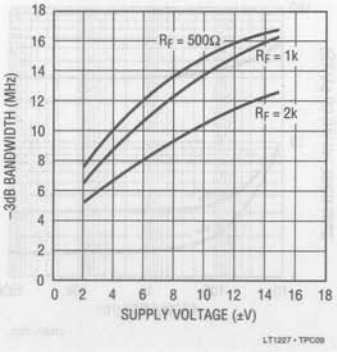
Voltage Gain and Phase vs Frequency, Gain = 40dB



–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 100Ω



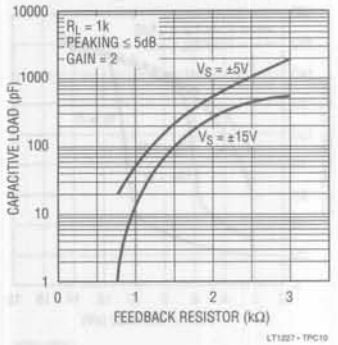
–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 1k



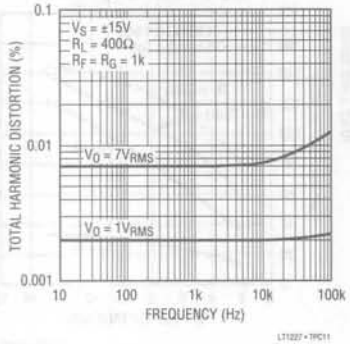
2

TYPICAL PERFORMANCE CHARACTERISTICS

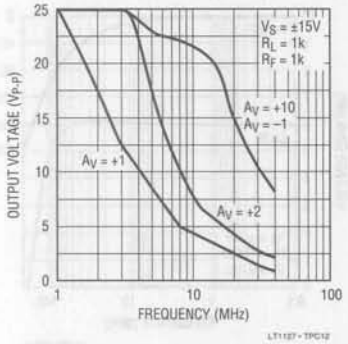
Maximum Capacitive Load vs Feedback Resistor



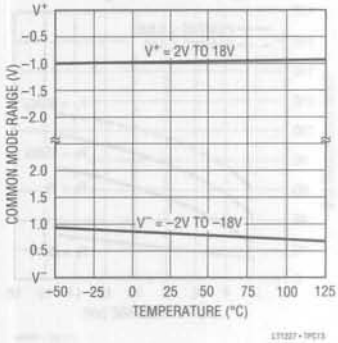
Total Harmonic Distortion vs Frequency



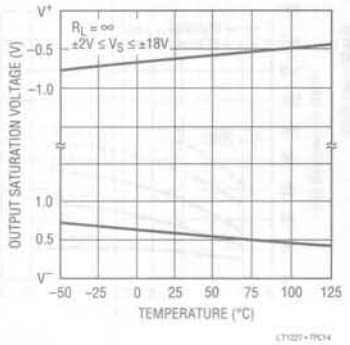
Maximum Undistorted Output vs Frequency



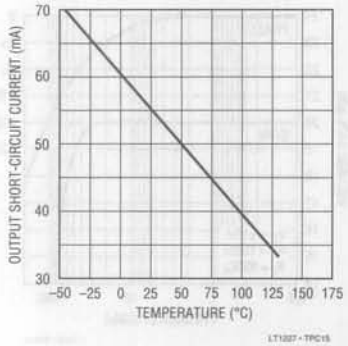
Input Common Mode Limit vs Temperature



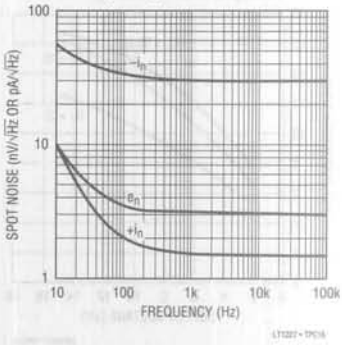
Output Saturation Voltage vs Temperature



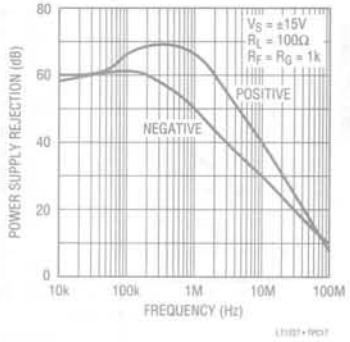
Output Short-Circuit Current vs Junction Temperature



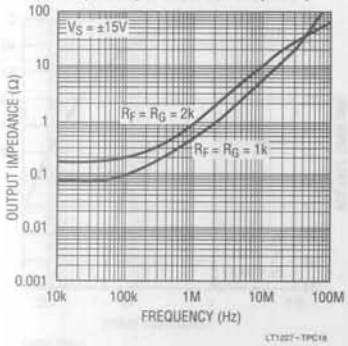
Spot Noise Voltage and Current vs Frequency



Power Supply Rejection vs Frequency

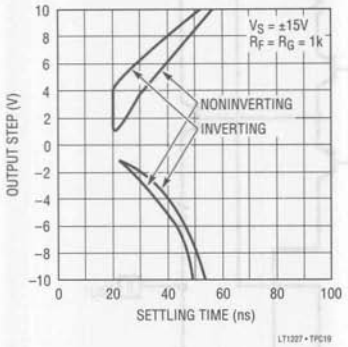


Output Impedance vs Frequency

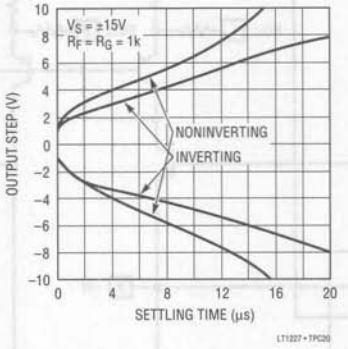


TYPICAL PERFORMANCE CHARACTERISTICS

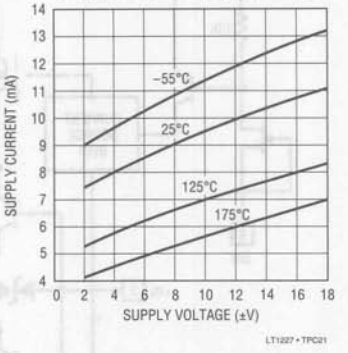
Settling Time to 10mV vs Output Step



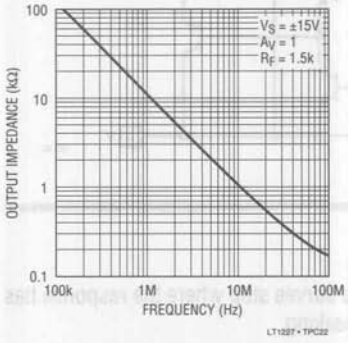
Settling Time to 1mV vs Output Step



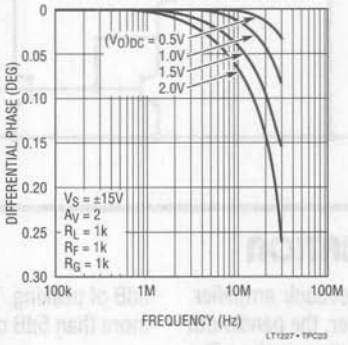
Supply Current vs Supply Voltage



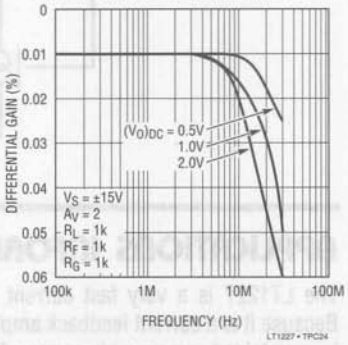
Output Impedance in Shutdown vs Frequency



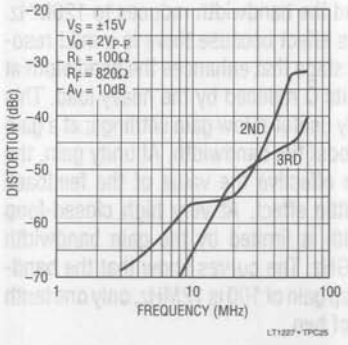
Differential Phase vs Frequency



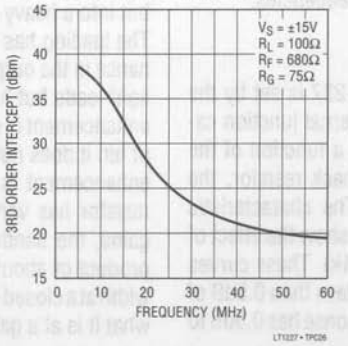
Differential Gain vs Frequency



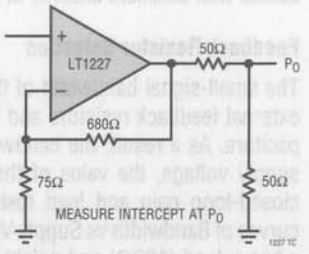
2nd and 3rd Harmonic Distortion vs Frequency



3rd Order Intercept vs Frequency

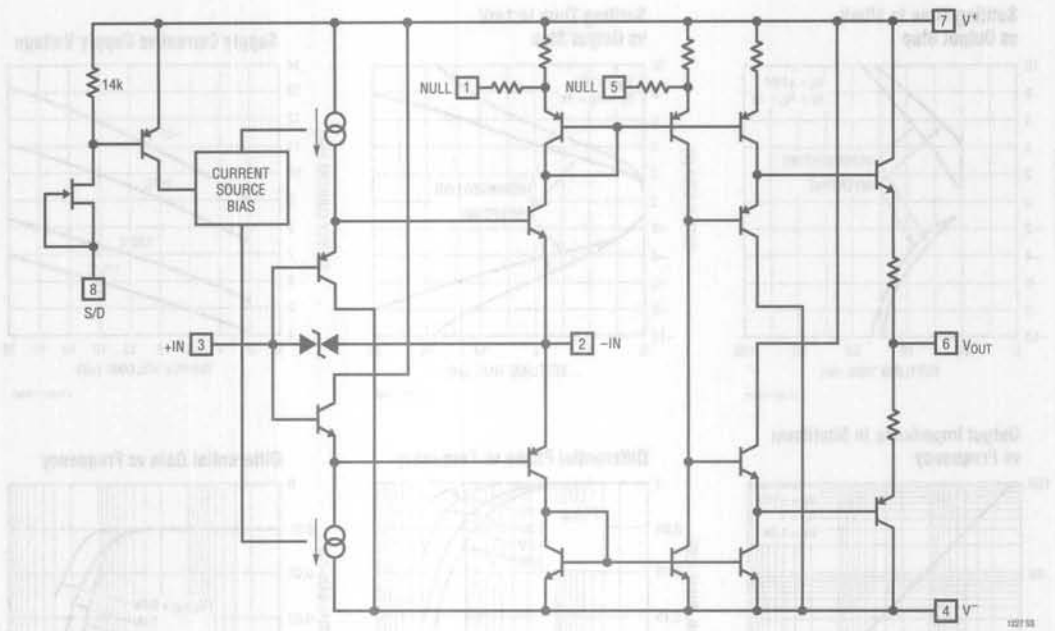


Test Circuit for 3rd Order Intercept



2

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

The LT1227 is a very fast current feedback amplifier. Because it is a current feedback amplifier, the bandwidth is maintained over a wide range of voltage gains. The amplifier is designed to drive low impedance loads such as cables with excellent linearity at high frequencies.

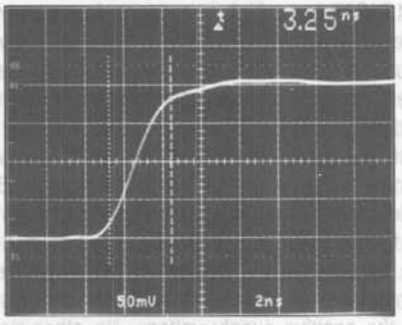
Feedback Resistor Selection

The small-signal bandwidth of the LT1227 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and load resistor. The characteristic curves of Bandwidth vs Supply Voltage show the effect of a heavy load (100Ω) and a light load (1k). These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

At a gain of two, on ±15V supplies with a 1k feedback resistor, the bandwidth into a light load is over 140MHz, but into a heavy load the bandwidth reduces to 120MHz. The loading has this effect because there is a mild resonance in the output stage that enhances the bandwidth at light loads but has its Q reduced by the heavy load. This enhancement is only useful at low gain settlings; at a gain of ten it does not boost the bandwidth. At unity gain, the enhancement is so effective the value of the feedback resistor has very little effect. At very high closed-loop gains, the bandwidth is limited by the gain bandwidth product of about 1GHz. The curves show that the bandwidth at a closed-loop gain of 100 is 12MHz, only one tenth what it is at a gain of two.

APPLICATIONS INFORMATION

Small-Signal Rise Time, A_V = +2



R_F = 1k, R_G= 1k, R_L = 100Ω

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier.

Capacitive Loads

The LT1227 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1k load at a gain of 2. This is a worst case condition, the amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present and the disadvantage that the gain is a function of the load resistance.

Power Supplies

The LT1227 will operate from single or split supplies from ±2V (4V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 500μV per volt of supply mismatch. The inverting bias current can change as much as 5.0μA per volt of supply mismatch, though typically the change is less than 0.5μA per volt.

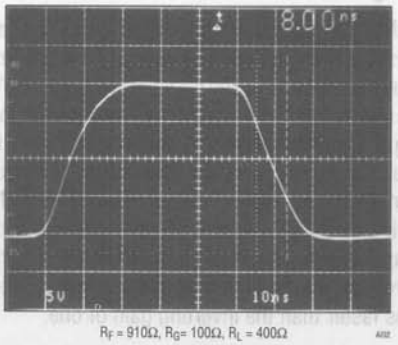
Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way slew rate is in a traditional op amp. This is because both the input stage and the output stage have slew rate limitations. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than ten in the noninverting mode, the overall slew rate is limited by the input stage.

The input stage slew rate of the LT1227 is approximately 125V/μs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and the internal capacitances. At a gain of ten with a 1k feedback resistor and ±15V supplies, the output slew rate is typically 1100V/μs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

The graph of Maximum Undistorted Output vs Frequency relates the slew rate limitations to sinusoidal inputs for various gain configurations.

Large-Signal Transient Response, A_V = +10

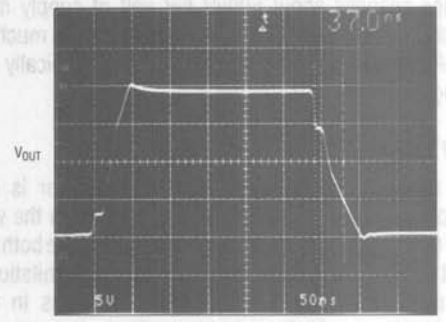


R_F = 910Ω, R_G= 100Ω, R_L = 400Ω

2

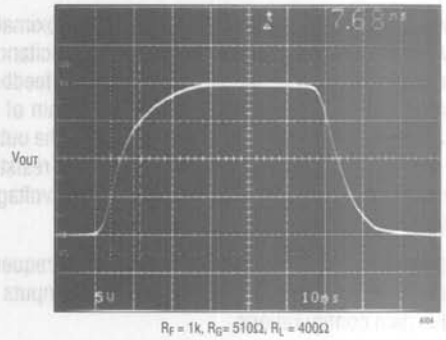
APPLICATIONS INFORMATION

Large-Signal Transient Response, $A_V = +2$



$R_F = 1k$, $R_G = 1k$, $R_L = 400\Omega$

Large-Signal Transient Response, $A_V = -2$



$R_F = 1k$, $R_G = 510\Omega$, $R_L = 400\Omega$

Settling Time

The characteristic curves show that the LT1227 amplifier settles to within 10mV of final value in 40ns to 55ns for any output step up to 10V. The curve of settling to 1mV of final value shows that there is a slower thermal contribution up to 20µs. The thermal settling component comes from the output and the input stage. The output contributes just under 1mV per volt of output change and the input contributes 300µV per volt of input change. Fortunately the input thermal tends to cancel the output thermal. For this reason the noninverting gain of two configuration settles faster than the inverting gain of one.

Shutdown

The LT1227 has a high impedance, low supply current mode which is controlled by pin 8. In the shutdown mode, the output looks like a 12pF capacitor and the supply current drops to approximately the pin 8 current. The shutdown pin is referenced to the positive supply through an internal pullup circuit (see the simplified schematic). Pulling a current of greater than 50µA from pin 8 will put the device into the shutdown mode. An easy way to force shutdown is to ground pin 8, using open drain (collector) logic. Because the pin is referenced to the positive supply, the logic used should have a breakdown voltage of greater than the positive supply voltage. No other circuitry is necessary as an internal JFET limits the pin 8 current to about 100µA. When pin 8 is open, the LT1227 operates normally.

Differential Input Signal Swing

The differential input swing is limited to about ±6V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect; however, in the shutdown mode, the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage. To allow for some margin, it is recommended that the input signal be less than ±5V when the device is shutdown.

Offset Adjust

Pins 1 and 5 are provided for offset nulling. A small current to V^+ or ground will compensate for DC offsets in the device. The pins are referenced to the positive supply (see the simplified schematic) and should be left open if unused. The offset adjust pins act primarily on the inverting input bias current. A 10k pot connected to pins 1 and 5 with the wiper connected to V^+ will null out the bias current, but will not affect the offset voltage much. Since the output offset is

$$V_O \cong A_V \bullet V_{OS} + (I_{IN^-}) \bullet R_F$$

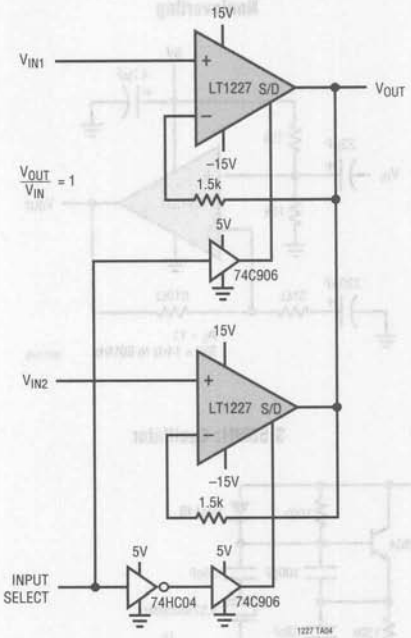
at higher gains ($A_V > 5$), the V_{OS} term will dominate. To null out the V_{OS} term, use a 10k pot between pins 1 and 5 with a 150k resistor from the wiper to ground for 15V split supplies, 47k for 5V split supplies.

TYPICAL APPLICATIONS

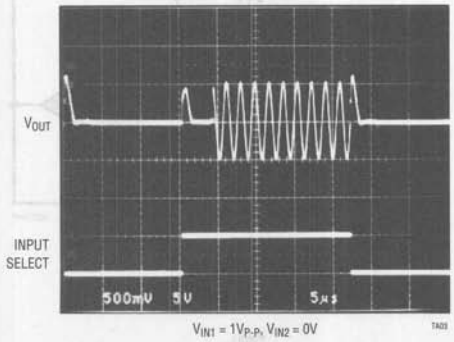
MUX Amplifier

The shutdown function can be effectively used to construct a MUX amplifier. A two-channel version is shown, but more inputs could be added with suitable logic. By configuring each amplifier as a unity-gain follower, there is no loading by the feedback network when the amplifier is off. The open drains of the 74C906 buffers are used to interface the 5V logic to the shutdown pin. Feedthrough from the unselected input to the output is –70dB at 10MHz. The differential voltage between MUX inputs V_{IN1} and V_{IN2} appears across the inputs of the shutdown device, this voltage should be less than ±5V to avoid turning on the clamp diodes discussed previously. If the inputs are sinusoidal having a zero DC level, this implies that the amplitude of each input should be less than $5V_{P-P}$. The output impedance of the off amplifier remains high until the output level exceeds approximately $6V_{P-P}$ at 10MHz, this sets the maximum usable output level. Switching time between inputs is about 4µs without an external pullup. Adding a 10k pullup resistor from each shutdown pin to V^+ will reduce the switching time to 2µs but will increase the positive supply current in shutdown by 1.5mA.

MUX Amplifier

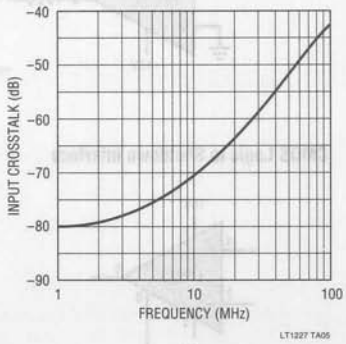


MUX Output



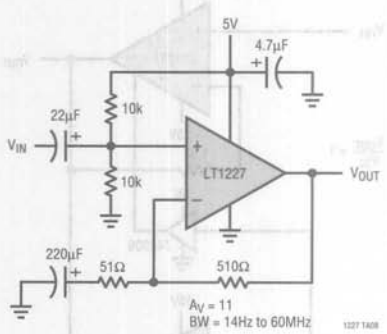
$V_{IN1} = 1V_{P-P}$, $V_{IN2} = 0V$

MUX Input Crosstalk vs Frequency

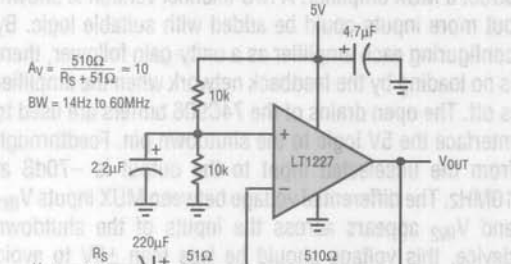


TYPICAL APPLICATIONS

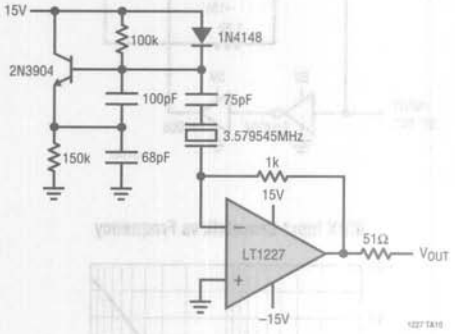
Single Supply AC-Coupled Amplifier Noninverting



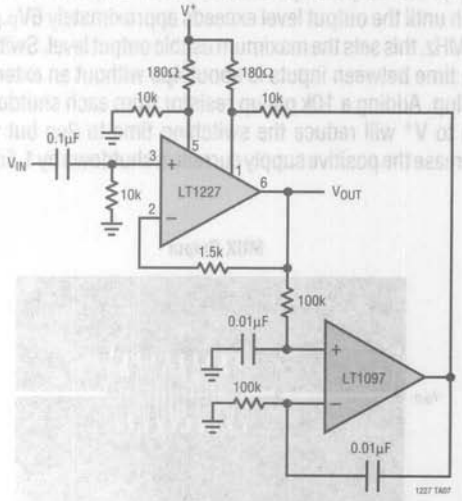
Single Supply AC-Coupled Amplifier Inverting



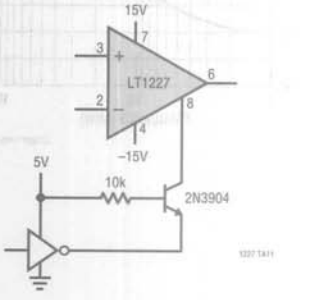
3.58MHz Oscillator



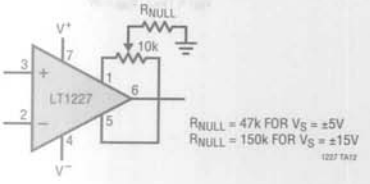
Buffer with DC Nulling Loop



CMOS Logic to Shutdown Interface



Optional Offset Nulling circuit



40MHz Video Fader and DC Gain Controlled Amplifier

FEATURES

- **Accurate Linear Gain Control: ±1% Typ, ±3% Max**
- **Constant Gain with Temperature**
- Wide Bandwidth: 40MHz
- High Slew Rate: 300V/µs
- Fast Control Path: 10MHz
- Low Control Feedthrough: 2.5mV
- High Output Current: 40mA
- Low Output Noise
  45nV/√Hz at A_V = 1
  270nV/√Hz at A_V = 100
- Low Distortion: 0.01%
- Wide Supply Range: ±2.5V to ±15V
- Low Supply Current: 13mA
- Low Differential Gain and Phase: 0.02%, 0.02°

APPLICATIONS

- Composite Video Gain Control
- RGB, YUV Video Gain Control
- Video Faders, Keyers
- Gamma Correction Amplifiers
- Audio Gain Control, Faders
- Multipliers, Modulators
- Electronically Tunable Filters

DESCRIPTION

The LT1251/LT1256 are two-input, one-output, 40MHz current feedback amplifiers with a linear control circuit that sets the amount each input contributes to the output. These parts make excellent electronically controlled variable gain amplifiers, filters, mixers and faders. The only external components required are the power supply bypass capacitors and the feedback resistors. Both parts operate on supplies from ±2.5V (or single 5V) to ±15V (or single 30V).

Absolute gain accuracy is trimmed at wafer sort to minimize part-to-part variations. The circuit is completely temperature compensated.

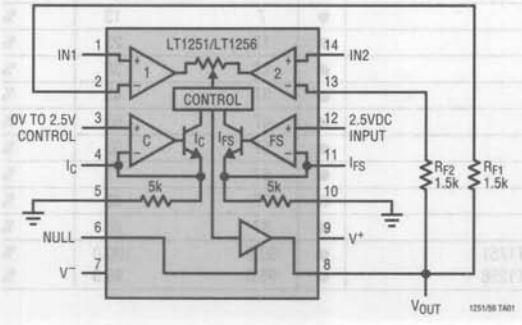
The LT1251 includes circuitry that eliminates the need for accurate control signals around zero and full scale. For control signals of less than 2% or greater than 98%, the LT1251 sets one input completely off and the other completely on. This is ideal for fader applications because it eliminates off-channel feedthrough due to offset or gain errors in the control signals.

The LT1256 does not have this on/off feature and operates linearly over the complete control range. The LT1256 is recommended for applications requiring more than 20dB of linear control range.

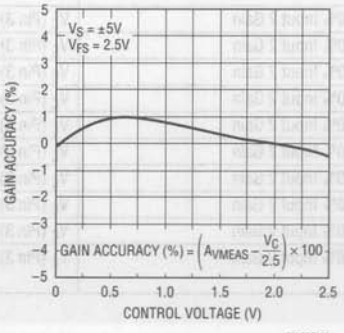
2

TYPICAL APPLICATION

Two-Input Video Fader



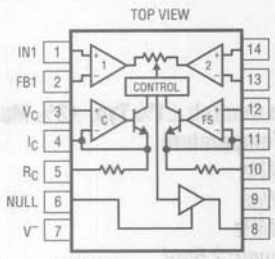
LT1256
Gain Accuracy vs Control Voltage



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Input Voltage on Pins 3,4,5,10,11,12 ..... V^- to V^+
Output Short Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range (Note 2) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
14-LEAD PLASTIC DIP

S PACKAGE
14-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER

LT1251CN
LT1251CS
LT1256CN
LT1256CS
(Note 2)

Consult factory for Industrial and Military grade parts.

SIGNAL AMPLIFIER AC CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{IN} = 1V_{RMS}, f = 1kHz, A_{VMAX} = 1, R_{F1} = R_{F2} = 1.5k, V_{FS} = 2.5V, I_C = I_{FS} = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
2%IN1	2% Input 1 Gain	V_C (Pin 3) = 0.05V	LT1251	●	0		0.1	%
			LT1256	●	0.1		5.0	%
10%IN1	10% Input 1 Gain	V_C (Pin 3) = 0.25V		●	7		13	%
20%IN1	20% Input 1 Gain	V_C (Pin 3) = 0.50V		●	17		23	%
30%IN1	30% Input 1 Gain	V_C (Pin 3) = 0.75V		●	27		33	%
40%IN1	40% Input 1 Gain	V_C (Pin 3) = 1.00V		●	37		43	%
50%IN1	50% Input 1 Gain	V_C (Pin 3) = 1.25V		●	47		53	%
60%IN1	60% Input 1 Gain	V_C (Pin 3) = 1.50V		●	57		63	%
70%IN1	70% Input 1 Gain	V_C (Pin 3) = 1.75V		●	67		73	%
80%IN1	80% Input 1 Gain	V_C (Pin 3) = 2.00V		●	77		83	%
90%IN1	90% Input 1 Gain	V_C (Pin 3) = 2.25V		●	87		93	%
98%IN1	98% Input 1 Gain	V_C (Pin 3) = 2.45V	LT1251	●	99.9		100.0	%
			LT1256	●	95.0		99.9	%
2%IN2	2% Input 2 Gain	V_C (Pin 3) = 2.45V	LT1251	●	0		0.1	%
			LT1256	●	0.1		5.0	%
10%IN2	10% Input 2 Gain	V_C (Pin 3) = 2.25V		●	7		13	%
20%IN2	20% Input 2 Gain	V_C (Pin 3) = 2.00V		●	17		23	%
30%IN2	30% Input 2 Gain	V_C (Pin 3) = 1.75V		●	27		33	%
40%IN2	40% Input 2 Gain	V_C (Pin 3) = 1.50V		●	37		43	%
50%IN2	50% Input 2 Gain	V_C (Pin 3) = 1.25V		●	47		53	%
60%IN2	60% Input 2 Gain	V_C (Pin 3) = 1.00V		●	57		63	%
70%IN2	70% Input 2 Gain	V_C (Pin 3) = 0.75V		●	67		73	%
80%IN2	80% Input 2 Gain	V_C (Pin 3) = 0.50V		●	77		83	%
90%IN2	90% Input 2 Gain	V_C (Pin 3) = 0.25V		●	87		93	%
98%IN2	98% Input 2 Gain	V_C (Pin 3) = 0.05V	LT1251	●	99.9		100.0	%
			LT1256	●	95.0		99.9	%

SIGNAL AMPLIFIER AC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{IN} = 1V_{RMS}$, f = 1kHz, $A_{VMAX} = 1$, $R_{F1} = R_{F2} = 1.5k$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Supply Rejection	$V_C = 1.25V$, $V_S = \pm 5V$ to $\pm 15V$	●		0.03	0.10	%/V
	External Resistor Gain 50% Input 1	Pins 5,10 = Open, External 5k Resistors from Pins 4,11 to Ground, $V_C = 1.25V$	●	45		55	%
SR	Slew Rate	$V_{IN} = \pm 2.5V$, V_O at $\pm 2V$, $R_L = 150\Omega$	●	150	300		V/µs
	Control Feedthrough	$V_C = 1.25VDC + 2.5V_{P-P}$ at 1kHz			2.5		mV_{P-P}
	Full Power Bandwidth	$V_O = 1V_{RMS}$			20		MHz
BW	Small-Signal Bandwidth	$V_S = \pm 5V$ $V_S = \pm 15V$			30 40		MHz MHz
	Differential Gain (Notes 4,5)	Control = 0% or 100% Control = 25% or 75%			0.02 0.90		% %
	Differential Phase (Notes 4,5)	Control = 0% or 100% Control = 25% or 75%			0.02 0.55		DEG DEG
THD	Total Harmonic Distortion	Gain = 100% Gain = 50% Gain = 10%			0.002 0.015 0.4		% % %
t_r, t_f	Rise Time, Fall Time	10% to 90%, $V_O = 100mV$			11		ns
OS	Overshoot	$V_O = 100mV$			3		%
t_{PD}	Propagation Delay	$V_O = 100mV$			10		ns
t_S	Settling Time	0.1%, $\Delta V_O = 2V$			65		ns

SIGNAL AMPLIFIER DC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{CM} = 0V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input Difference Between Inputs	● ●	 −3	2 1	5 3	mV mV
	Input Offset Voltage Drift				10		µV/°C
I_{IN}^+	Noninverting Input Bias Current	Either Input	●	−2.5	0.5	2.5	µA
I_{IN}^-	Inverting Input Bias Current	Either Input Difference Between Inputs	● ●	−30 −1	10 0.5	30 1	µA µA
	Inverting Input Bias Current Null Change	Null (Pin 6) Open to V^-	●	−280	−170	−60	µA
e_n	Input Noise Voltage Density	f = 1kHz			2.7		$nV/\sqrt{Hz}$
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.5		$pA/\sqrt{Hz}$
$-i_n$	Inverting Input Noise Current Density	f = 1kHz			29		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Either Noninverting Input	●	5	17		MΩ
C_{IN}	Input Capacitance	Either Noninverting Input	●		1.5		pF
	Input Voltage Range	$V_S = \pm 5V$ $V_S = 5V$	● ●	±3 2	±3.2	 3	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to 3V $V_S = 5V$, $V_{CM} = 2V$ to 3V, $V_O = 2.5V$	● ●	55 50	61 57		dB dB
	Inverting Input Current Common-Mode Rejection	$V_{CM} = -3V$ to 3V $V_S = 5V$, $V_{CM} = 2V$ to 3V, $V_O = 2.5V$	● ●		0.07 0.17	0.25 0.70	µA/V µA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	70	76		dB
	Noninverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		30	100	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		30	200	nA/V

2

SIGNAL AMPLIFIER DC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{CM} = 0V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_O = -3V$ to $3V$, $R_L = 150\Omega$	●	83	93		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$V_O = -3V$ to $3V$, $R_L = 150\Omega$	●	1.0	1.8		MΩ
V_{OUT}	Maximum Output Voltage Swing	No Load	●	±4.0	±4.2		V
		$R_L = 150\Omega$	●	±3.0	±3.5		V
		$V_S = \pm 15V$, No Load	●	±14.0	±14.2		V
		$V_S = 5V$, $V_{CM} = 2.5V$, (Note 6)	●	1.2		3.8	V
I_O	Maximum Output Current	$V_S = \pm 5V$	●	±30	±40		mA
		$V_S = 5V$, $V_{CM} = V_O = 2.5V$	●	±20	±30		mA
I_S	Supply Current	$V_C = V_{FS} = 2.5V$	●	10.0	13.5	17.0	mA
		$V_C = V_{FS} = 1.25V$	●	5.0	7.5	9.5	mA
		$V_C = V_{FS} = 0V$	●	0.8	1.3	1.8	mA
		$V_C = V_{FS} = 2.5V$, $V_S = \pm 15V$	●	10.0	14.5	18.5	mA
		$V_C = V_{FS} = 0V$, $V_S = \pm 15V$	●	0.8	1.4	2.0	mA

CONTROL AND FULL SCALE AMPLIFIER CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Amplifier Input Offset Voltage	Pin 4 to Pin 3	●		5	15	mV
	Full Scale Amplifier Input Offset Voltage	Pin 11 to Pin 12	●		5	15	mV
	Control Amplifier Input Resistance		●	25	100		MΩ
	Full Scale Amplifier Input Resistance		●	25	100		MΩ
	Control Amplifier Input Bias Current		●	−750	−300		nA
	Full Scale Amplifier Input Bias Current		●	−750	−300		nA
R_C	Internal Control Resistor	$T_A = 25°C$		3.75	5	6.25	kΩ
R_{FS}	Internal Full Scale Resistor	$T_A = 25°C$		4	5	6	kΩ
	Resistor Temperature Coefficient				0.2		%/°C
	Control Path Bandwidth	Small Signal, $V_C = 100mV$, (Note 7)			10		MHz
	Control Path Rise and Fall Time	Small Signal, $V_C = 100mV$, (Note 7)			35		ns
	Control Path Transition Time	0% to 100%			150		ns
	Control Path Propagation Delay	Small Signal, $\Delta V_C = 100mV$			50		ns
		V_C from 0% or 100%			90		ns

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: A heat sink may be required depending on the power supply voltage.

Note 2: Commercial grade parts are designed to operate over the temperature range of −40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over −40°C to 85°C are available on special request. Consult factory.

Note 3: T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formulas:

LT1251CN/LT1256CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1251CS/LT1256CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 4: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Five identical amplifier stages were cascaded giving an effective resolution of 0.02% and 0.02°.

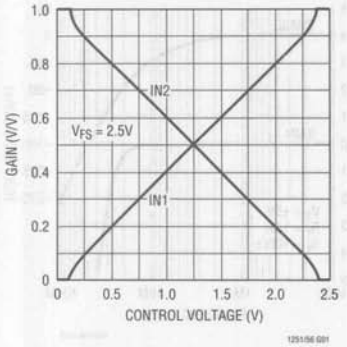
Note 5: Differential gain and phase are best when the control is set at 0% or 100%. See the Typical Performance Characteristics curves.

Note 6: Tested with $R_L = 150\Omega$ to 2.5V to simulate an AC coupled load.

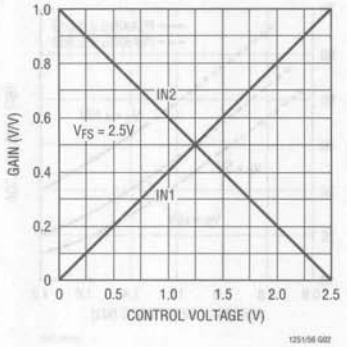
Note 7: Small-signal control path response is measured driving R_C (pin 5) to eliminate peaking caused by stray capacitance on pin 4.

TYPICAL PERFORMANCE CHARACTERISTICS

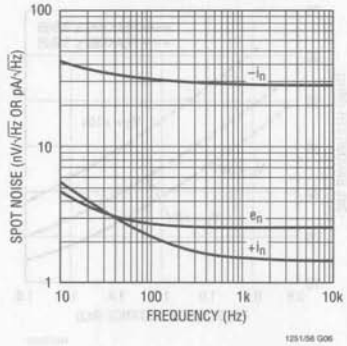
LT1251
Gain vs Control Voltage



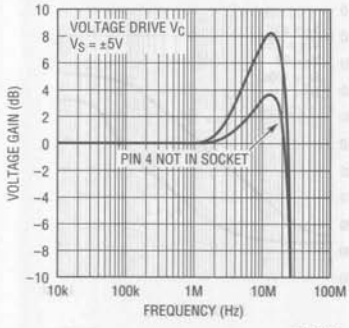
LT1256
Gain vs Control Voltage



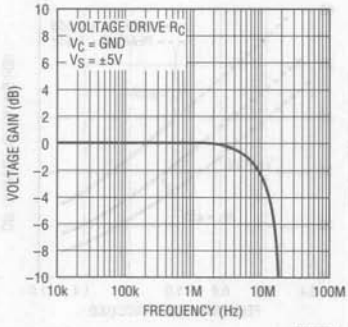
Spot Input Noise Voltage and Current vs Frequency



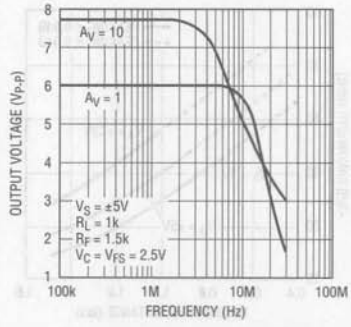
LT1251/LT1256
Control Path Bandwidth



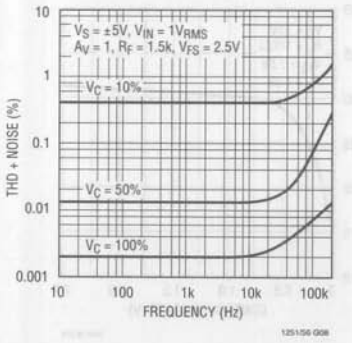
LT1251/LT1256
Control Path Bandwidth



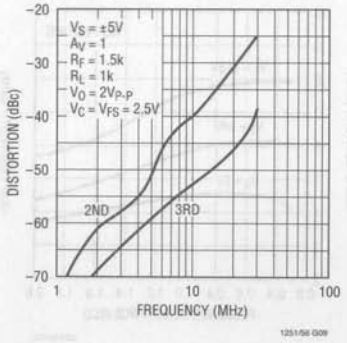
Undistorted Output Voltage vs Frequency



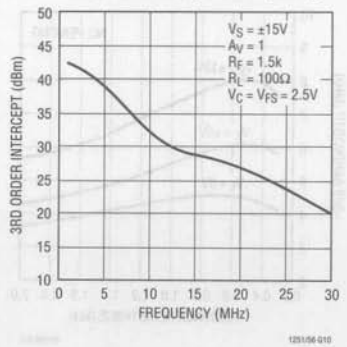
THD Plus Noise vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



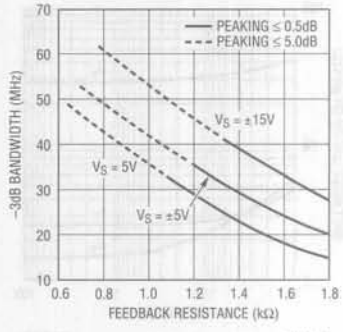
3rd Order Intercept vs Frequency



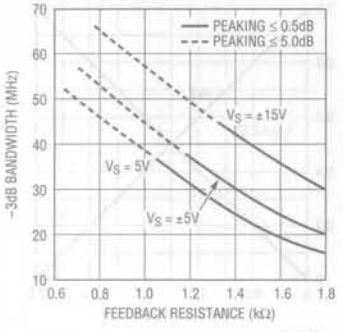
2

TYPICAL PERFORMANCE CHARACTERISTICS

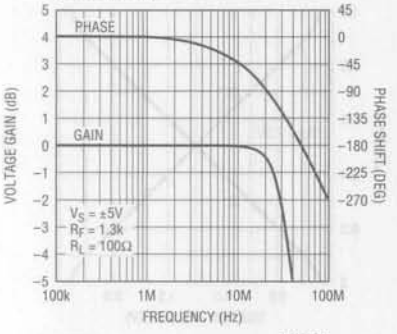
Bandwidth vs Feedback Resistance, $A_V = 1$, $R_L = 100\Omega$



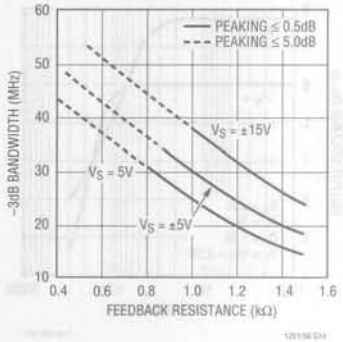
Bandwidth vs Feedback Resistance, $A_V = 1$, $R_L = 1k$



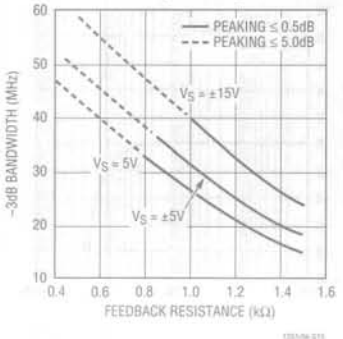
Voltage Gain and Phase vs Frequency



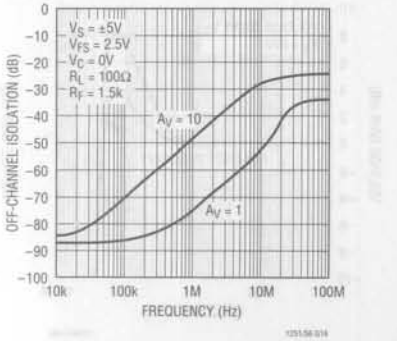
Bandwidth vs Feedback Resistance, $A_V = 10$, $R_L = 100\Omega$



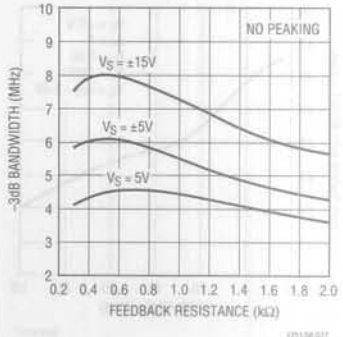
Bandwidth vs Feedback Resistance, $A_V = 10$, $R_L = 1k$



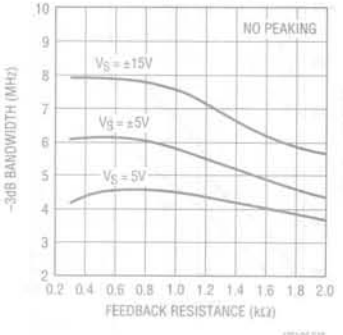
Off-Channel Isolation vs Frequency



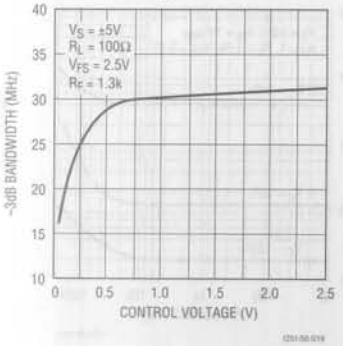
Bandwidth vs Feedback Resistance, $A_V = 100$, $R_L = 100\Omega$



Bandwidth vs Feedback Resistance, $A_V = 100$, $R_L = 1k$

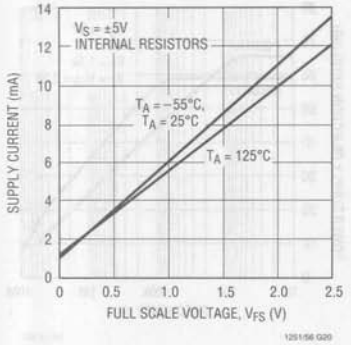


–3dB Bandwidth vs Control Voltage

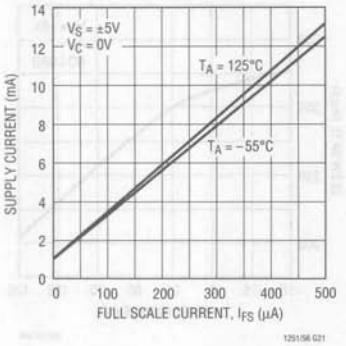


TYPICAL PERFORMANCE CHARACTERISTICS

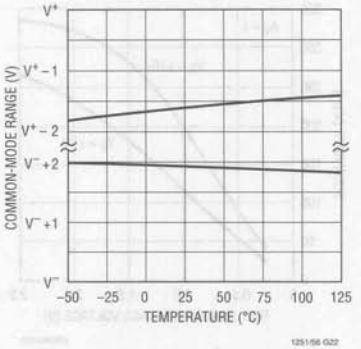
Supply Current vs Full Scale Voltage



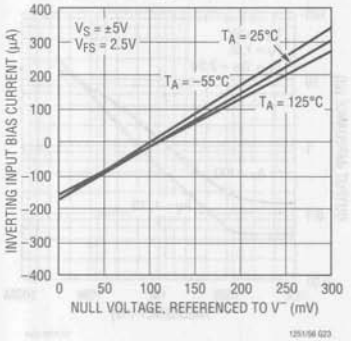
Supply Current vs Full Scale Current



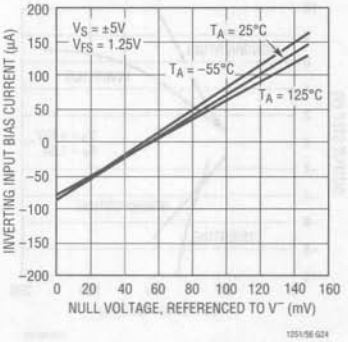
Input Common-Mode Range vs Temperature



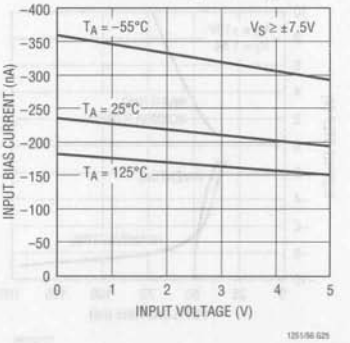
Inverting Input Bias Current vs Null Voltage



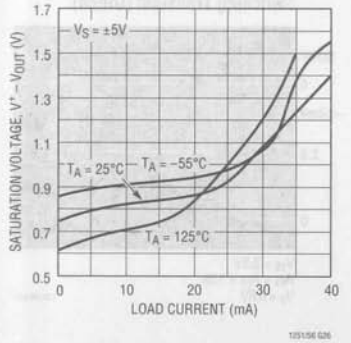
Inverting Input Bias Current vs Null Voltage



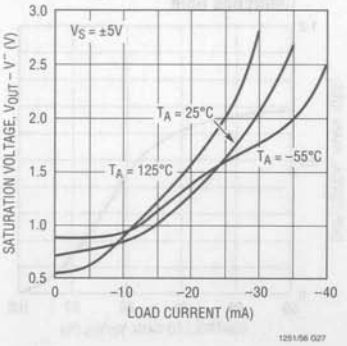
Control and Full Scale Amp Input Bias Current vs Input Voltage



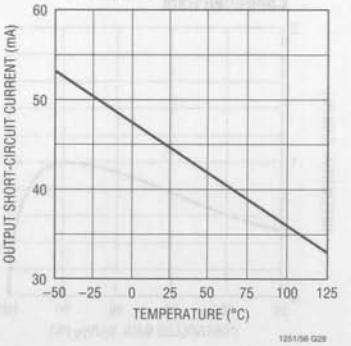
Positive Output Saturation Voltage vs Load Current



Negative Output Saturation Voltage vs Load Current



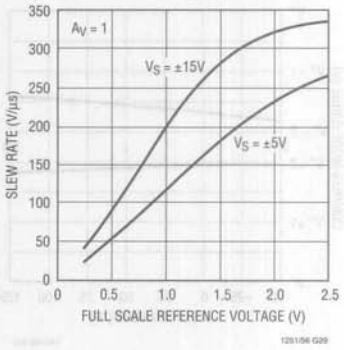
Output Short-Circuit Current vs Temperature



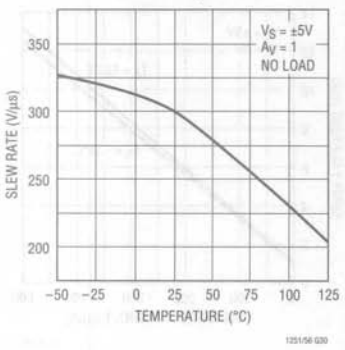
2

TYPICAL PERFORMANCE CHARACTERISTICS

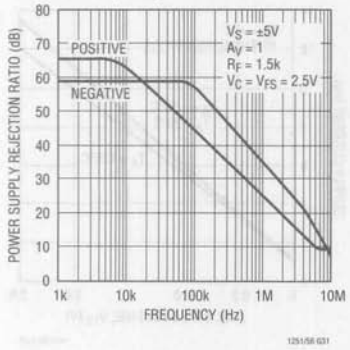
Slew Rate vs Full Scale Reference Voltage



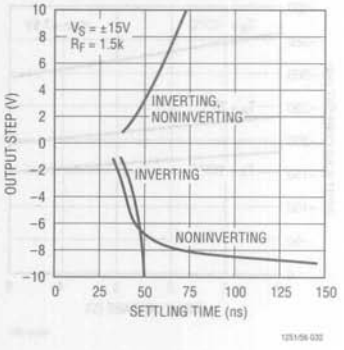
Slew Rate vs Temperature



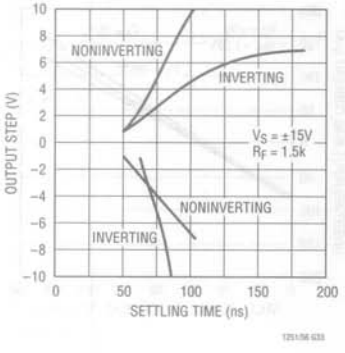
Power Supply Rejection Ratio vs Frequency



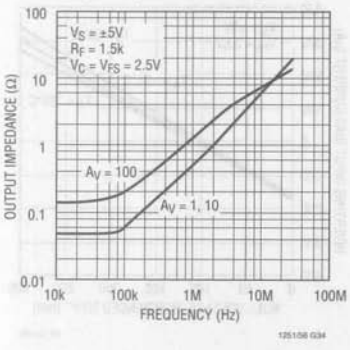
Settling Time to 10mV vs Output Step



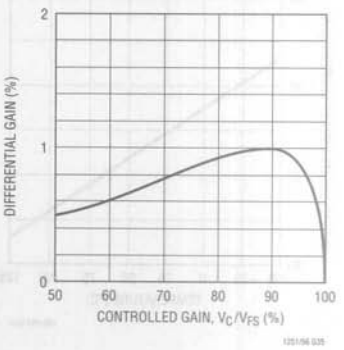
Settling Time to 1mV vs Output Step



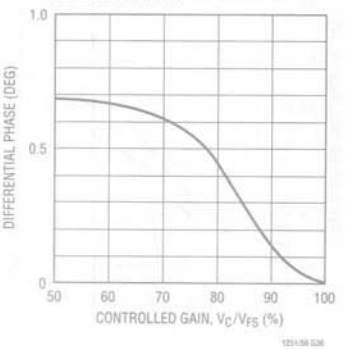
Output Impedance vs Frequency



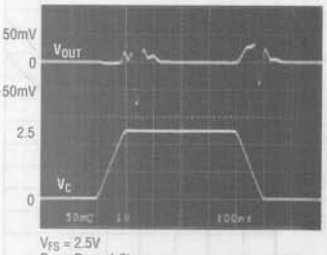
Differential Gain vs Controlled Gain



Differential Phase vs Controlled Gain

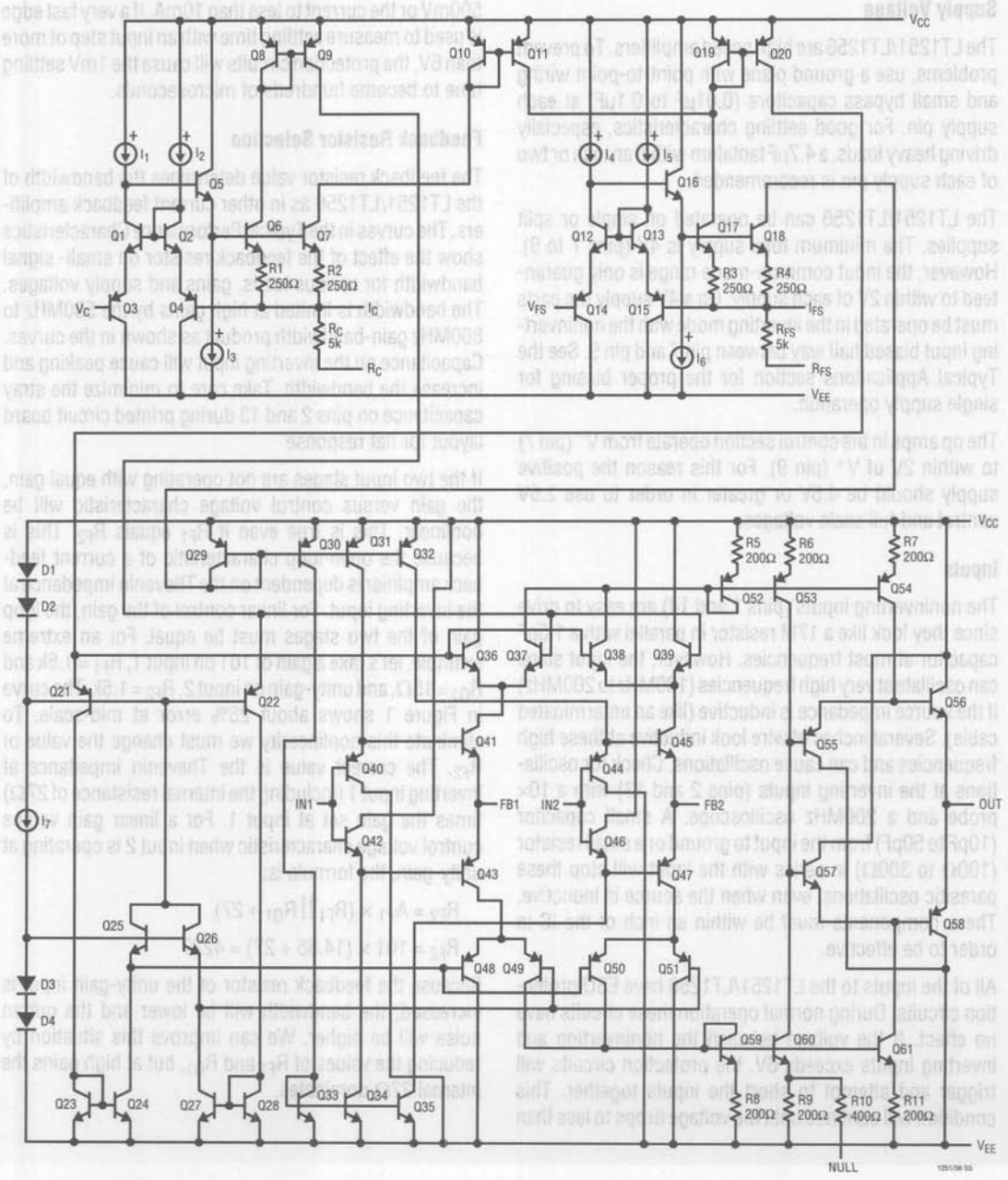


LT1251 Switching Transient (Glitch)



LINEAR TECHNOLOGY

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

Supply Voltage

The LT1251/LT1256 are high speed amplifiers. To prevent problems, use a ground plane with point-to-point wiring and small bypass capacitors (0.01μF to 0.1μF) at each supply pin. For good settling characteristics, especially driving heavy loads, a 4.7μF tantalum within an inch or two of each supply pin is recommended.

The LT1251/LT1256 can be operated on single or split supplies. The minimum total supply is 4V (pins 7 to 9). However, the input common-mode range is only guaranteed to within 2V of each supply. On a 4V supply the parts must be operated in the inverting mode with the noninverting input biased half way between pin 7 and pin 9. See the Typical Applications section for the proper biasing for single supply operation.

The op amps in the control section operate from V^- (pin 7) to within 2V of V^+ (pin 9). For this reason the positive supply should be 4.5V or greater in order to use 2.5V control and full scale voltages.

Inputs

The noninverting inputs (pins 1 and 14) are easy to drive since they look like a 17M resistor in parallel with a 1.5pF capacitor at most frequencies. However, the input stage can oscillate at very high frequencies (100MHz to 200MHz) if the source impedance is inductive (like an unterminated cable). Several inches of wire look inductive at these high frequencies and can cause oscillations. Check for oscillations at the inverting inputs (pins 2 and 13) with a 10× probe and a 200MHz oscilloscope. A small capacitor (10pF to 50pF) from the input to ground or a small resistor (100Ω to 300Ω) in series with the input will stop these parasitic oscillations, even when the source is inductive. These components must be within an inch of the IC in order to be effective.

All of the inputs to the LT1251/LT1256 have ESD protection circuits. During normal operation these circuits have no effect. If the voltage between the noninverting and inverting inputs exceeds 6V, the protection circuits will trigger and attempt to short the inputs together. This condition will continue until the voltage drops to less than 500mV or the current to less than 10mA. If a very fast edge is used to measure settling time with an input step of more than 6V, the protection circuits will cause the 1mV settling time to become hundreds of microseconds.

Feedback Resistor Selection

The feedback resistor value determines the bandwidth of the LT1251/LT1256 as in other current feedback amplifiers. The curves in the Typical Performance Characteristics show the effect of the feedback resistor on small- signal bandwidth for various loads, gains and supply voltages. The bandwidth is limited at high gains by the 500MHz to 800MHz gain-bandwidth product as shown in the curves. Capacitance on the inverting input will cause peaking and increase the bandwidth. Take care to minimize the stray capacitance on pins 2 and 13 during printed circuit board layout for flat response.

If the two input stages are not operating with equal gain, the gain versus control voltage characteristic will be nonlinear. This is true even if R_{F1} equals R_{F2}. This is because the open-loop characteristic of a current feedback amplifier is dependent on the Thevenin impedance at the inverting input. For linear control of the gain, the loop gain of the two stages must be equal. For an extreme example, let's take a gain of 101 on input 1, R_{F1} = 1.5k and R_{G1} = 15Ω, and unity-gain on input 2, R_{F2} = 1.5k. The curve in Figure 1 shows about 25% error at mid-scale. To eliminate this nonlinearity we must change the value of R_{F2}. The correct value is the Thevenin impedance at inverting input 1 (including the internal resistance of 27Ω) times the gain set at input 1. For a linear gain versus control voltage characteristic when input 2 is operating at unity-gain, the formula is:

$$R_{F2} = A_{V1} \times (R_{F1} \,||\, R_{G1} + 27)$$

$$R_{F2} = 101 \times (14.85 + 27) = 4227$$

Because the feedback resistor of the unity-gain input is increased, the bandwidth will be lower and the output noise will be higher. We can improve this situation by reducing the values of R_{F1} and R_{G1}, but at high gains the internal 27Ω dominates.

APPLICATIONS INFORMATION

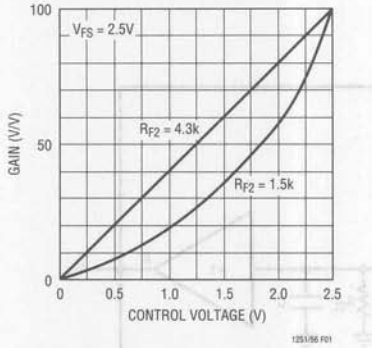


Figure 1. Linear Gain Control from 0 to 101

Capacitive Loads

Increasing the value of the feedback resistor reduces the bandwidth and open-loop gain of the LT1251/LT1256; therefore, the pole introduced by a capacitive load can be overcome. If there is little or no resistive load in parallel with the load capacitance, the output stage will resonate, peak and possibly oscillate. With a resistive load of 150Ω, any capacitive load can be accommodated by increasing the feedback resistor. If the capacitive load cannot be paralleled with a DC load of 150Ω, a network of 200pF in series with 100Ω should be placed from the output to ground. Then the feedback resistor should be selected for best response.

The Null Pin

Pin 6 can be used to adjust the gain of an internal current mirror to change the output offset. The open circuit voltage at pin 6 is set by the full scale current I_{FS} flowing through 200Ω to the negative supply. Therefore, the null pin sits 100mV above the negative supply with V_{FS} equal to 2.5V. Any op amp whose output swings within a few millivolts of the negative supply can drive the null pin. The AM modulator application shows an LT1077 driving the null pin to eliminate the output DC offset voltage.

Crosstalk

The amount of signal from the off input that appears at the output is a function of frequency and the circuit topology. The nature of a current feedback input stage is to force the voltage at the inverting input to be equal to the voltage at the noninverting input. This is independent of feedback and forced by a buffer amplifier between the inputs. When the LT1251/LT1256 are operating noninverting, the off input signal is present at the inverting input. Since one end of the feedback resistor is connected to this input, the off signal is only a feedback resistor away from the output. The amount of unwanted signal at the output is determined by the size of the feedback resistor and the output impedance of the LT1251/LT1256. The output impedance rises with increasing frequency resulting in more crosstalk at higher frequencies. Additionally, the current that flows in the inverting input is diverted to the supplies within the chip and some of this signal will also show up at the output. With a 1.5k feedback resistor, the crosstalk is down about 86dB at low frequencies and rises to –78dB at 1MHz and on to –60dB at 6MHz. The curves show the details.

Distortion

When only one input is contributing to the output (V_C = 0% or 100%) the LT1251/LT1256 have very low distortion. As the control reduces the output, the distortion will increase. The amount of increase is a function of the current that flows in the inverting input. Larger input signals generate more distortion. Using a larger feedback resistor will reduce the distortion at the expense of higher output noise.

APPLICATIONS INFORMATION

Signal Path Description

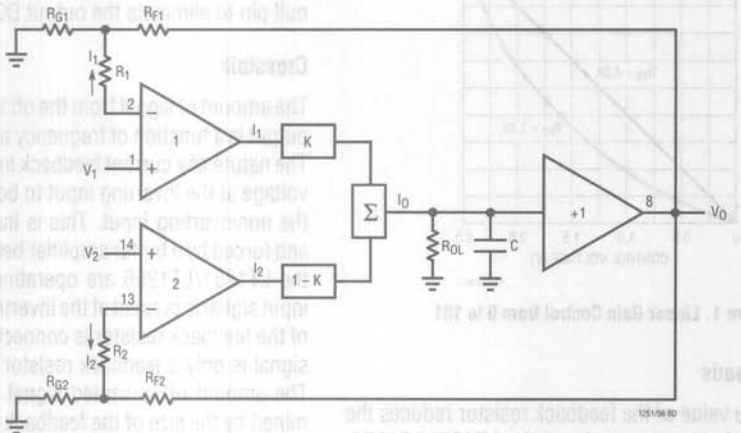


Figure 2. Signal Path Block Diagram

Figure 2 is the basic block diagram of the LT1251/LT1256 signal path with external resistors R_{G1}, R_{F1}, R_{G2} and R_{F2}. Both input stages are operating as noninverting amplifiers with two input signals V_1 and V_2.

Each input stage has a unity-gain buffer from the noninverting input to the inverting input. Therefore, the inverting input is at the same voltage as the noninverting input. R_1 and R_2 represent the internal output resistances of these buffers, approximately 27Ω.

K is a constant determined by the control circuit, and can be any value between 0 and 1. The control circuit is described in a later section.

By inspection of the diagram:

$$I_1 = \frac{V_1}{R_1 + \frac{(R_{G1})(R_{F1})}{R_{G1}+R_{F1}}} - \frac{V_0}{R_{F1} + R_1\left(\frac{R_{F1}}{R_{G1}} + 1\right)}$$

$$I_2 = \frac{V_2}{R_2 + \frac{(R_{G2})(R_{F2})}{R_{G2}+R_{F2}}} - \frac{V_0}{R_{F2} + R_2\left(\frac{R_{F2}}{R_{G2}} + 1\right)}$$

$$I_O = KI_1 + (1-K)I_2$$

$$V_O = I_O\left(\frac{R_{OL}}{(1 + sR_{OL}C)}\right)$$

Substituting and rearranging gives:

$$V_O = \frac{\dfrac{KV_1}{R_1 + \frac{(R_{G1})(R_{F1})}{R_{G1}+R_{F1}}} + \dfrac{(1-K)V_2}{R_2 + \frac{(R_{G2})(R_{F2})}{R_{G2}+R_{F2}}}}{\dfrac{1 + sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1} + R_1\left(\frac{R_{F1}}{R_{G1}} + 1\right)} + \dfrac{(1-K)}{R_{F2} + R_2\left(\frac{R_{F2}}{R_{G2}} + 1\right)}}$$

General Equation for the Noninverting Amplifier Case

APPLICATIONS INFORMATION

In low gain applications, R_1 and R_2 are small compared to the feedback resistors and therefore we can simplify the equation to:

$$V_O = \frac{\dfrac{KV_1}{(R_{G1})(R_{F1})} + \dfrac{(1-K)V_2}{(R_{G2})(R_{F2})}}{\dfrac{1+sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1}} + \dfrac{(1-K)}{R_{F2}}}$$

Note that the denominator causes a gain error due to the open-loop gain (typically 0.1% for frequencies below 20kHz) and for mismatches in R_{F1} and R_{F2}. A 1% mismatch in the feedback resistors results in a 0.25% error at K = 0.5.

If we set $R_{F1} = R_{F2}$ and assume $R_{OL} >> R_{F1}$ (a 0.1% error at low frequencies) the above equation simplifies to:

$$V_O = KV_1A_{V1} + (1-K)V_2A_{V2}$$

$$\text{where } A_{V1} = 1 + \frac{R_{F1}}{R_{G1}} \text{ and } A_{V2} = 1 + \frac{R_{F2}}{R_{G2}}$$

This shows that the output fades linearly from input 2, times its gain, to input 1, times its gain, as K goes from 0 to 1.

If only one input is used (for example, V_1) and pin 14 is grounded, then the gain is proportional to K.

$$\frac{V_O}{V_1} = KA_{V1}$$

Similarly for the inverting case where the noninverting inputs are grounded and the input voltages V_1 and V_2 drive the normally grounded ends of R_{G1} and R_{G2}, we get:

$$V_O = -\frac{\dfrac{KV_1}{R_{G1} + R_1\left(\dfrac{R_{G1}}{R_{F1}} + 1\right)} + \dfrac{(1-K)V_2}{R_{G2} + R_2\left(\dfrac{R_{G2}}{R_{F2}} + 1\right)}}{\dfrac{1+sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1} + R_1\left(\dfrac{R_{F1}}{R_{G1}} + 1\right)} + \dfrac{(1-K)}{R_{F2} + R_2\left(\dfrac{R_{F2}}{R_{G2}} + 1\right)}}$$

General Equation for the Inverting Amplifier Case

Note that the denominator is the same as the noninverting case. In low gain applications, R_1 and R_2 are small compared to the feedback resistors and therefore we can simplify the equation to:

$$V_O = -\frac{\dfrac{KV_1}{R_{G1}} + \dfrac{(1-K)V_2}{R_{G2}}}{\dfrac{1+sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1}} + \dfrac{(1-K)}{R_{F2}}}$$

Again if we set $R_{F1} = R_{F2}$ and assume $R_{OL} >> R_{F1}$ (a 0.1% error at low frequencies) the above equation simplifies to:

$$V_O = -\left[KV_1A_{V1} + (1-K)V_2A_{V2}\right]$$

$$\text{where } A_{V1} = \frac{R_{F1}}{R_{G1}} \text{ and } A_{V2} = \frac{R_{F2}}{R_{G2}}$$

The four-resistor difference amplifier yields the same result as the inverting amplifier case, and the common-mode rejection is independent of K.

2

APPLICATIONS INFORMATION

Control Circuit Description

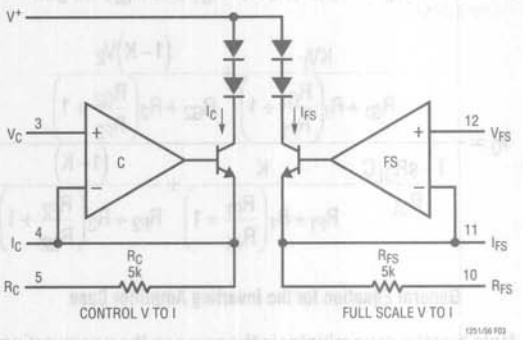


Figure 3. Control Circuit Block Diagram

The control section of the LT1251/LT1256 consists of two identical voltage-to-current converters (V-to-I); each V-to-I contains an op amp, an NPN transistor and a resistor. The converter on the right generates a *full scale* current I_{FS} and the one on the left generates a *control* current I_C. The ratio I_C/I_{FS} is called K. K goes from a minimum of zero (when I_C is zero) to a maximum of one (when I_C is equal to, or greater than, I_{FS}). K determines the gain from each signal input to the output.

The op amp in each V-to-I drives the transistor until the voltage at the inverting input is the same as the voltage at the noninverting input. If the open end of the resistor (pin 5 or 10) is grounded, the voltage across the resistor is the same as the voltage at the noninverting input. The emitter current is therefore equal to the input voltage V_C divided by the resistor value R_C. The collector current is essentially the same as the emitter current and it is the ratio of the two collector currents that sets the gain.

The LT1251/LT1256 are tested with pins 5 and 10 grounded and a full scale voltage of 2.5V applied to V_{FS} (pin 12). This sets I_{FS} at approximately 500μA; the control voltage V_C is applied to pin 3. When the control voltage is negative or zero, I_C is zero and K is zero. When V_C is 2.5V or greater, I_C is equal to or greater than I_{FS} and K is one. The gain of channel one goes from 0% to 100% as V_C goes from zero to 2.5V. The gain of channel two goes the opposite way, from 100% down to 0%. The worst case error in K (the gain) is ±3% as detailed in the electrical tables. By using a 2.5V full scale voltage and the internal resistors, no additional errors need be accounted for.

In the LT1256, K changes linearly with I_C. To insure that K is zero, V_C must be negative 15mV or more to overcome the worst case control op amp offset. Similarly to insure that K is 100%, V_C must be 3% larger than V_{FS} based on the guaranteed gain accuracy.

To eliminate the overdrive requirement, the LT1251 has internal circuitry that senses when the control current is at about 5% and sets K to 0%. Similarly, at about 95% it sets K to 100%. The LT1251 guarantees that a 2% (50mV) input gives zero and 98% (2.45V) gives 100%.

The operating currents of the LT1251/LT1256 are derived from I_{FS} and therefore the quiescent current is a function of V_{FS} and R_{FS}. The electrical tables show the supply current for three values of V_{FS} including zero. An approximate formula for the supply current is:

$$I_S = 1mA + (24 \times I_{FS}) + (V_S/20k)$$

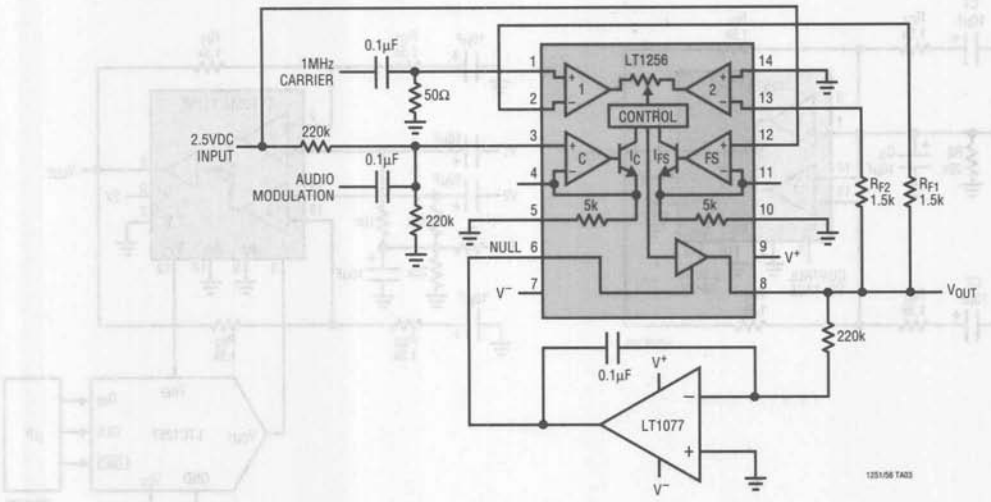
where V_S is the total supply voltage between pins 9 and 7. By reducing I_{FS} the supply current can be reduced, however the slew rate and bandwidth will also be reduced as indicated in the characteristic curves. Using the internal resistors (5k) with V_{FS} equal to 2.5V results in I_{FS} equal to 500μA; there is no reason to use a larger value of I_{FS}.

The inverting inputs of the V-to-I converters are available so that external resistors can be used instead of the internal ones. For example, if a 10V full scale voltage is desired, an external pair of 20k resistors should be used to set I_{FS} to 500μA. The positive supply voltage must be 2.5V greater than the maximum V_C and/or V_{FS} to keep the transistors from saturating. Do not use the internal resistors with external resistors because the internal resistors have a large positive temperature coefficient (0.2%/°C) that will cause gain errors.

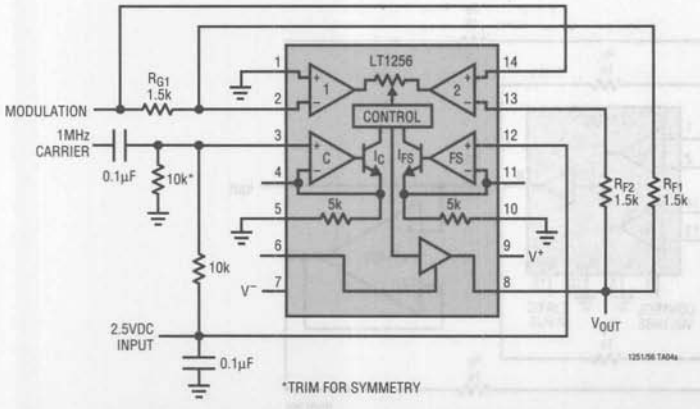
If the control voltage is applied to the free end of resistor R_C (pin 5) and the V_C input (pin 3) is grounded, the polarity of the control voltage must be inverted. Therefore, K will be 0% for zero input and 100% for –2.5V input, assuming V_{FS} equals 2.5V. With pin 3 grounded, pin 4 is a virtual ground; this is convenient for summing several negative going control signals.

TYPICAL APPLICATIONS

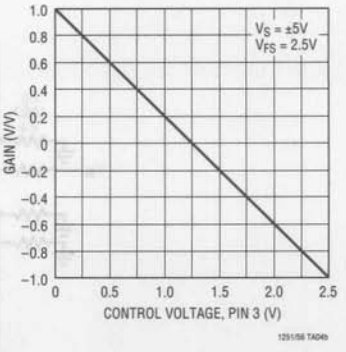
AM Modulator with DC Output Nulling Circuit



Four-Quadrant Multiplier as a Double-Sideband Suppressed-Carrier Modulator



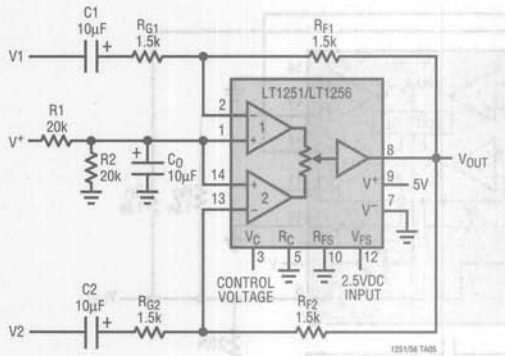
Modulation Gain vs Control Voltage



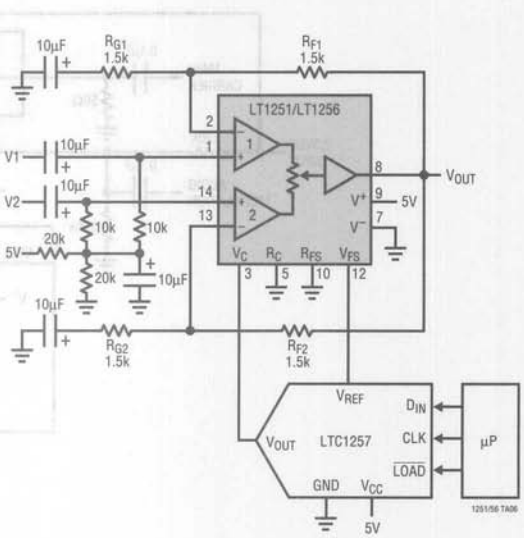
2

TYPICAL APPLICATIONS

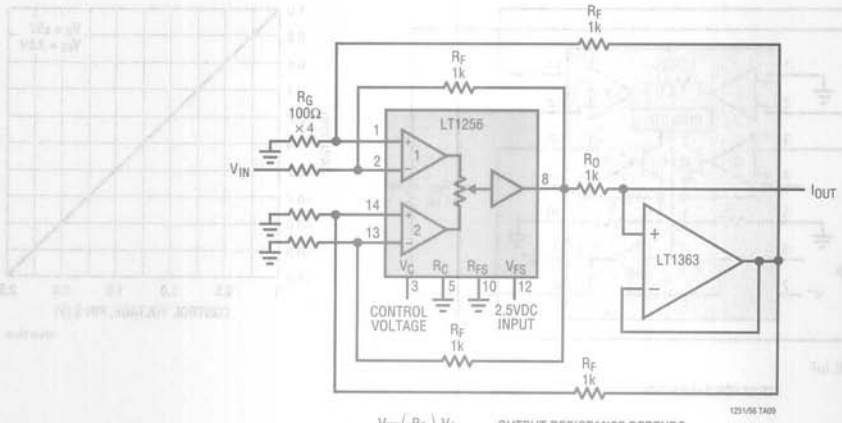
Single Supply Inverting AC Amplifier



Single Supply Noninverting AC Amplifier with Digital Gain Control



Controlled Gain, Voltage-to-Current Converter (Current Source)

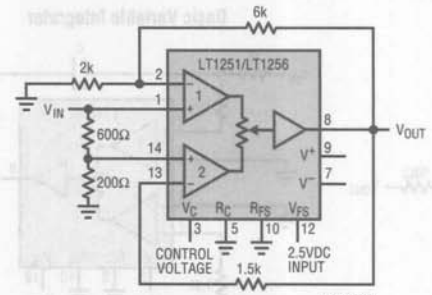


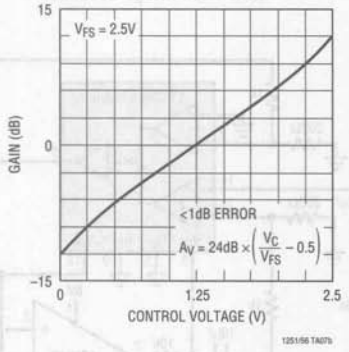
$$I_{OUT} = \frac{V_{IN}}{R_O}\left(\frac{R_F}{R_G}\right)\frac{V_C}{V_{FS}}$$

OUTPUT RESISTANCE DEPENDS ON MATCHING OF RESISTORS

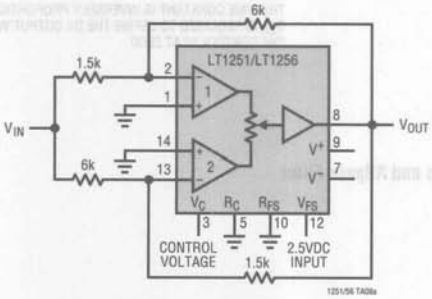
TYPICAL APPLICATIONS

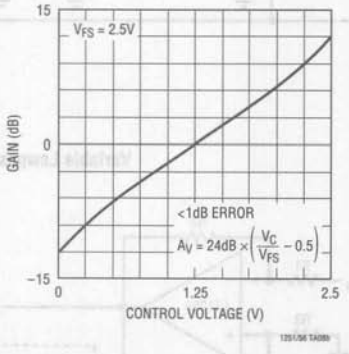
Logarithmic Gain Control (Noninverting)



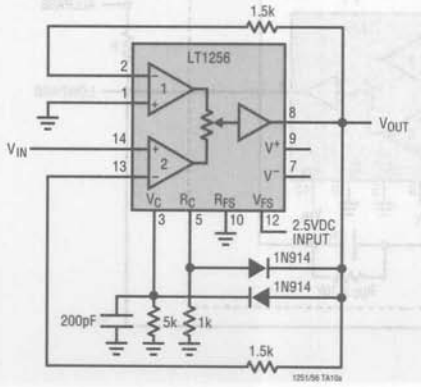


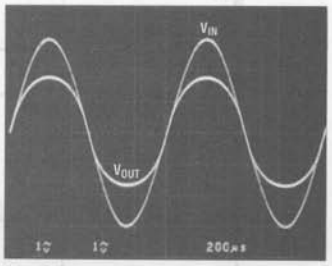
Logarithmic Gain Control (Inverting)





Soft Clipper





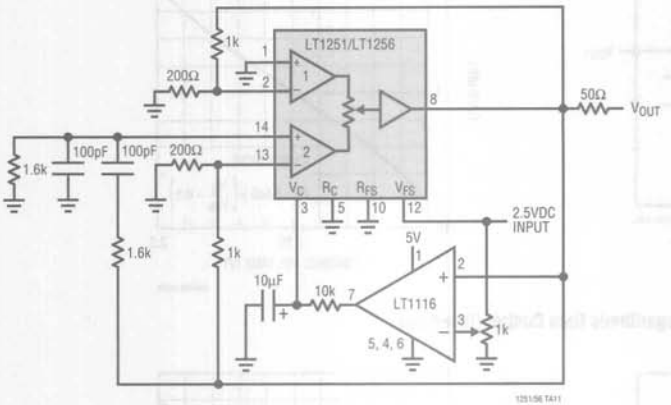
VFS = 2.5V
VS = ±5V
f = 1kHz

1251/56 TA10b

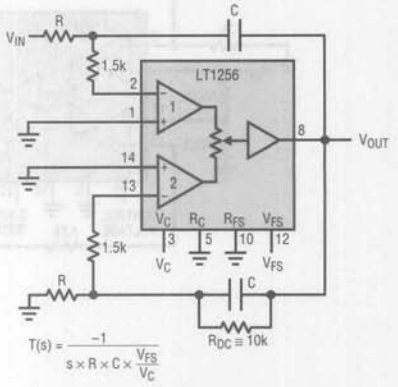
2

TYPICAL APPLICATIONS

1MHz Wien Bridge Oscillator



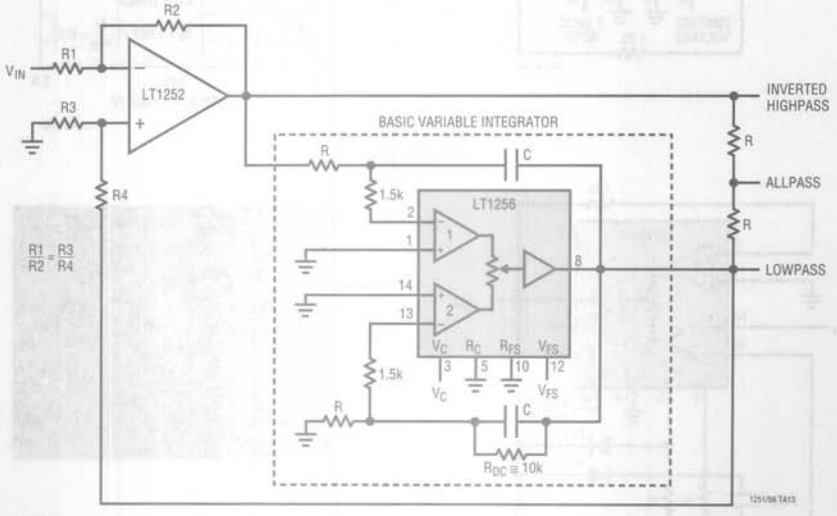
Basic Variable Integrator



THE TIME CONSTANT IS INVERSELY PROPORTIONAL TO V_C. R_{DC} IS REQUIRED TO DEFINE THE DC OUTPUT WHEN THE CONTROL IS AT ZERO.

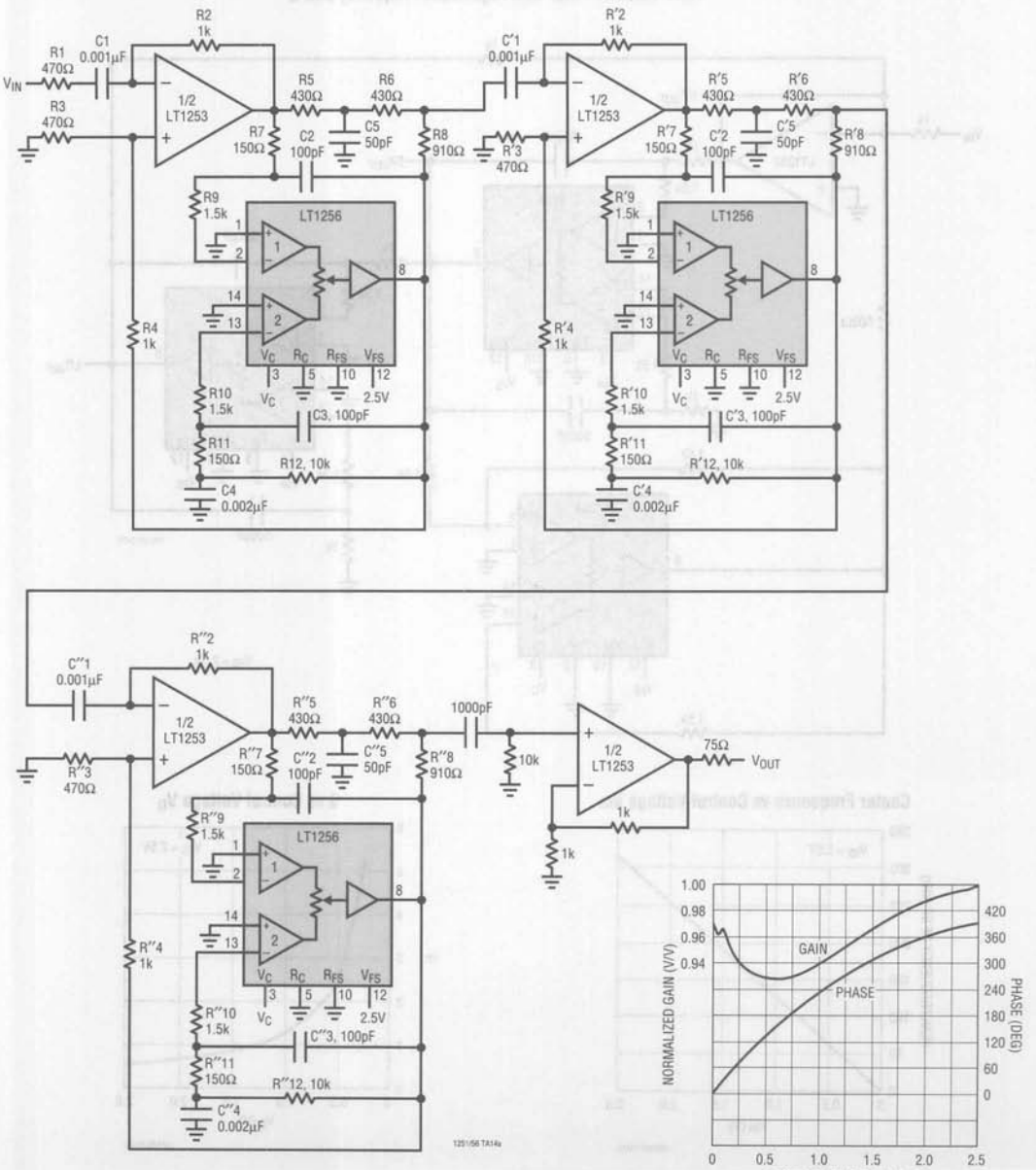
1251/56 TA12

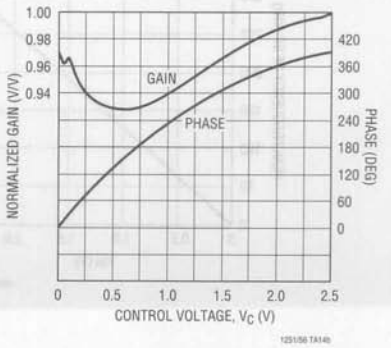
Variable Lowpass, Highpass and Allpass Filter



TYPICAL APPLICATIONS

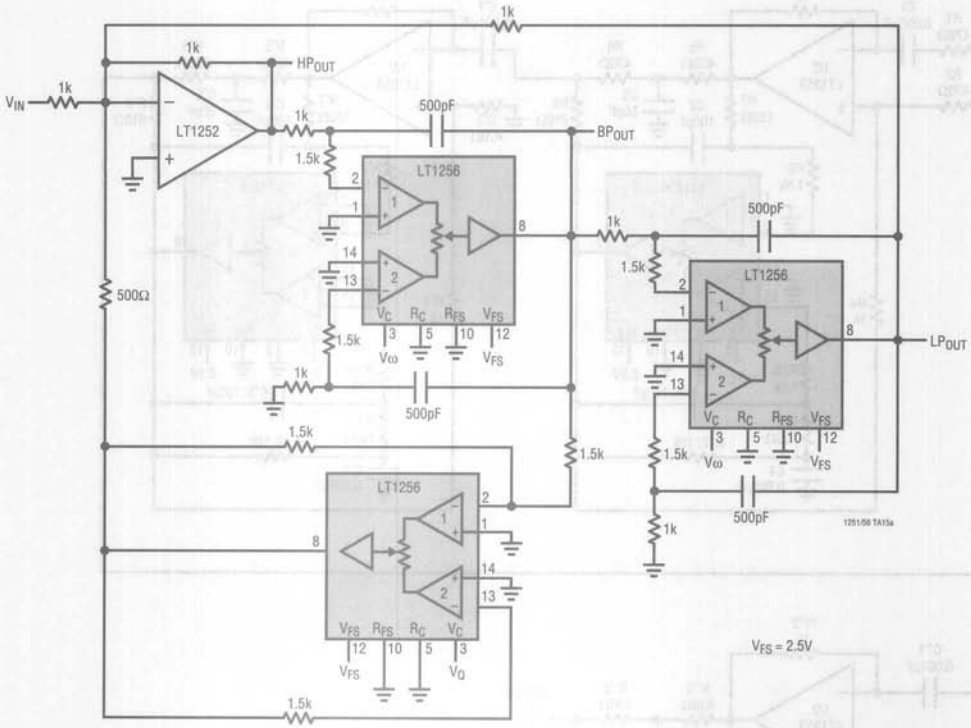
3.58MHz Phase Shifter



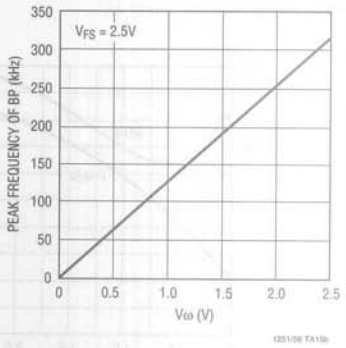


TYPICAL APPLICATIONS

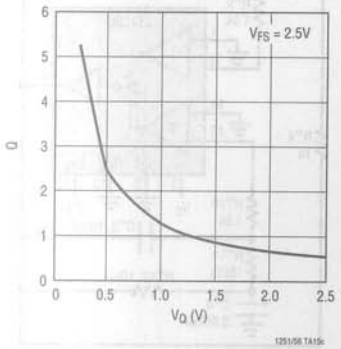
State Variable Filter with Adjustable Frequency and Q



Center Frequency vs Control Voltage Vω



Q vs Control Voltage V_Q



MACROMODEL

For PSpice™

```
*
* Linear Technology LT1251/LT1256 VIDEO FADER MACROMODEL
* Written: 3-11-1994 BY WILLIAM H. GROSS.
*
* Connections: as per datasheet pinout
*1=first noninverting input
*2=first inverting input
*3=control voltage input
*4=control current input
*5=control resistor, RC
*6=null input
*7=positive supply
*8=output
*9=negative supply
*10=full scale resistor, RFS
*11=full scale current input
*12=full scale voltage input
*13=second inverting input
*14=second noninverting input
*
.SUBCKT LT1251 1 2 3 4 5 6 7 8 9 10 11 12 13 14
*
*first input stage
IB1       1      0      500NA
RI1       1      0      17MEG
C1        1      0      1.5PF
E1       2A      0      VALUE={LIMIT (V(1), V(8N)+0.4, V(8P)-0.4)+V(EN)/30}
VOS1     2A     2B      2.5MV
R1       2B      2      27
C2        2      0      1PF
*
*second input stage
IB2      14      0      450NA
RI2      14      0      17MEG
C14      14      0      1.5PF
E2      13A      0      VALUE={LIMIT (V(14), V(8N)+0.4, V(8P)-0.4)+V(EN)/30}
VOS2    13A     13B     1.5MV
R2      13B     13      27
C13     13      0       1PF
*
*control amp
IBC       3      0      -300NA
RIC       3      0      100MEG
C3        3      0      1PF
R3        3     3A      1600
CBWC     3A      0      10PF
EC       3B      0      3A     0     1.0
VOSC     3B      4      5MV
C4        4      0      1PF
RC        4      5      5K
C5        5      0      1PF
*
```

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MACROMODEL

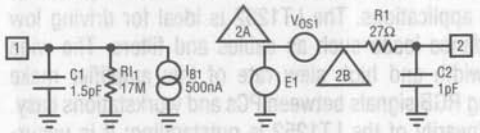
```
*full scale amp
IBFS     12      0      -300NA
RIFS     12      0      100MEG
C12      12      0      1PF
R12      12     12A     1600
CBWFS    12A     0      10PF
EFS      12B     0      12A    0     1.0
VOSFS    12B     11     -5MV
C11      11      0      1PF
RFS      11      10     5K
C10      10      0      1PF
*
*generating K
*** the next two lines are for the LT1251
EK K 0 TABLE {I(VOSC)/I(VOSFS)}=  (-100,0)    (0.04,0)    (0.1,0.11)
+                                 (0.9,0.907) (0.95,1.0)  (100,1.0)
*** the next two lines are for the LT1256
*EK K 0 TABLE {I(VOSC)/I(VOSFS)}= (-100,0)    (0,0)       (0.2,0.21)
*+                                (0.9,0.9)   (1.0,1.0)   (100,1.0)
RDUMMY   K       0      1MEG
RNOISE1  EN      0      200K
RNOISE2  EN      0      200K
*generates 40.7nV/rtHz
*
*null circuit
GNULL     9      6A     VALUE={I(VOSFS)}
RN1      6A      9      200
VNULL    6A      6B     0.0V
RN2      6B      6      400
C6        6      9      1PF
*
*output stage
E6       8A      0
+VALUE={1.8MEG*(I(VOS1)*V(K)+I(VOS2)*(1-V(K))-I(VNULL)+0.10UA+0.0007*V(EN))}
RG       8A      8B     1.8MEG
CG       8B      0      3.4PF
E8       8C      0      8B     0     1.0
V8       8C      8D     0.0V
R8       8D      8      11
*
*output swing and current limit
DP       8B      8P     D1
VDP      8P      7      -1.4V
DN       8N      8B     D1
VDN      8N      9      1.4V
.MODEL   D1      D
GCL      8B      0      TABLE {I(V8)}=(-1,-1)(-0.04,0)(0.04,0)(1,1)
*
*supply current
GQ        7      9      VALUE={1MA+24*I(VOSFS)+(V(7)-V(9))/20K}
GCC       7      0      TABLE {I(V8)}=(-1,0)(0,0)(1,1)
GEE       9      0      TABLE {I(V8)}=(-1,-1)(0,0)(1,0)
*
.ENDS LT1251
```

MACROMODEL

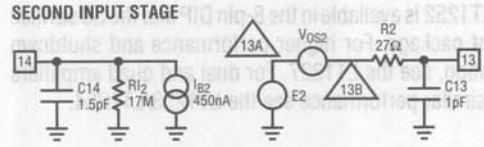
LT1251/LT1256 Macro Model for PSpice

PIN # IN □ NODE # IN △

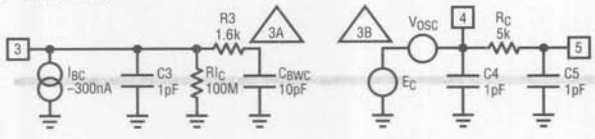
FIRST INPUT STAGE



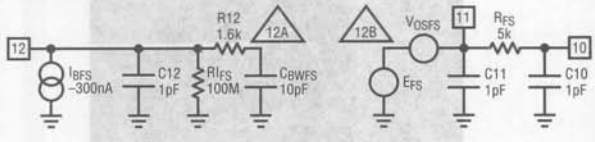
SECOND INPUT STAGE



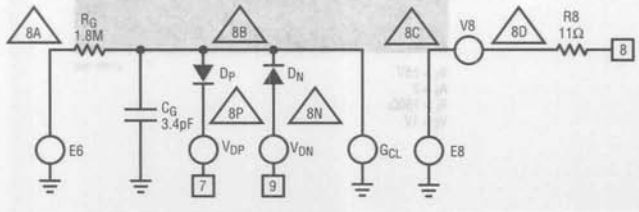
CONTROL AMP



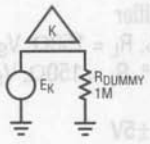
FULL SCALE AMP



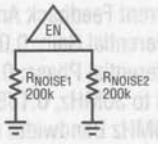
OUTPUT STAGE AND VOLTAGE SWING/CURRENT LIMIT



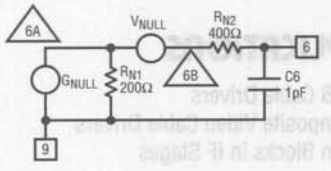
K GENERATOR



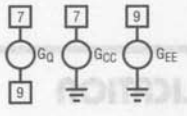
NOISE GENERATOR



NULL CIRCUIT



SUPPLY CURRENTS



1251/56 MM

2

Low Cost Video Amplifier

FEATURES

- Low Cost
- Current Feedback Amplifier
- Differential Gain: 0.01%, $R_L = 150\Omega$, $V_S = \pm 5V$
- Differential Phase: 0.09°, $R_L = 150\Omega$, $V_S = \pm 5V$
- Flat to 30MHz, 0.1dB
- 100MHz Bandwidth on ±5V
- Wide Supply Range: ±2V(4V) to ±14V(28V)
- Low Power: 85mW at ±5V

APPLICATIONS

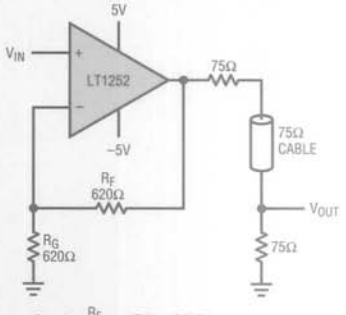
- RGB Cable Drivers
- Composite Video Cable Drivers
- Gain Blocks in IF Stages

DESCRIPTION

The LT1252 is low cost current feedback amplifier for video applications. The LT1252 is ideal for driving low impedance loads such as cables and filters. The wide bandwidth and high slew rate of this amplifier make driving RGB signals between PCs and workstations easy. The linearity of the LT1252 is outstanding; it is unsurpassed for driving composite video.

The LT1252 is available in the 8-pin DIP and the S8 surface mount package. For higher performance and shutdown operation, see the LT1227. For dual and quad amplifiers with similar performance see the LT1253/LT1254.

TYPICAL APPLICATION

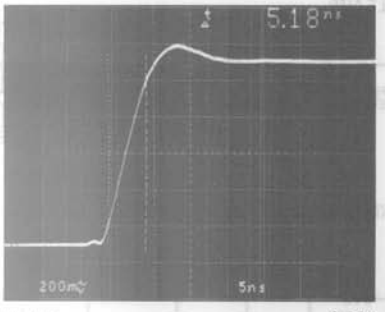


$A_V = 1 + \frac{R_F}{R_G}$ BW = 100MHz

AT AMPLIFIER OUTPUT.
6dB LESS AT V_{OUT}.

LT1252 • TA01

Transient Response



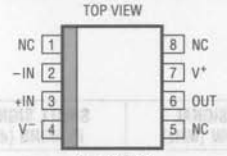
$V_S = \pm 5V$
$A_V = 2$
$R_L = 150\Omega$
$V_O = 1V$

LT1252 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 28V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 2) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

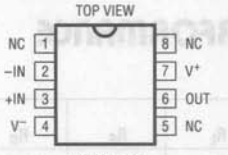
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1252CS8
S8 PART MARKING
1252



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1252CN8

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V to ±12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			5	15	mV
$+I_B$	Noninverting Bias Current			1	15	µA
$-I_B$	Inverting Bias Current			20	100	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = ±5V, V_O = ±2V, R_L = 150Ω	560	1500		V/V
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±12V	60	70		dB
CMRR	Common-Mode Rejection Ratio	V_S = ±5V, V_{CM} = ±2V	55	65		dB
V_{OUT}	Maximum Output Voltage Swing	V_S = ±12V, R_L = 500Ω V_S = ±5V, R_L = 150Ω	±7.0 ±2.5	±10.5 ±3.7		V V
I_{OUT}	Maximum Output Current		30	55		mA
I_S	Supply Current			8.5	18	mA
R_{IN}	Input Resistance		1	10		MΩ
C_{IN}	Input Capacitance			3		pF
	Power Supply Range Dual Single		±2 4		±12 24	V V
SR	Input Slew Rate	A_V = 1		125		V/µs
	Output Slew Rate	A_V = 2		250		V/µs

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_S = \pm5V$ to $\pm12V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Small-Signal Rise Time	$V_S = \pm12V$, $A_V = 2$		3.5		ns
	Rise and Fall Time	$V_S = \pm5V$, $A_V = 2$, $V_{OUT} = 1V_{P-P}$		5.2		ns
t_p	Propagation Delay	$V_S = \pm5V$, $A_V = 2$		3.5		ns

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1252CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1252CS8: $T_J = T_A + (P_D \times 150°C/W)$

TYPICAL AC PERFORMANCE

BANDWIDTH

V_S	A_V	R_L	R_F	R_G	SMALL SIGNAL −3dB BW (MHz)	SMALL SIGNAL −0.1dB BW (MHz)	SMALL SIGNAL PEAKING (dB)
±12	1	150	2370	None	282	45	1.9
±12	−1	1000	1100	1100	58	17	0.1
±12	−1	150	909	909	73	34	0.1
±12	2	1000	1210	1210	253	20	0.1
±12	2	150	909	909	142	38	0.1
±12	5	1000	1000	249	73	25	0.1
±12	5	150	866	215	75	31	0.1
±12	10	1000	909	100	67	26	0.1
±12	10	150	768	84.5	69	32	0.1
±5	1	1000	2210	None	260	10	2.4
±5	1	150	1300	None	232	50	0.8
±5	−1	1000	1000	1000	50	11	0.1
±5	−1	150	732	732	69	34	0.1
±5	2	1000	909	909	133	24	0.1
±5	2	150	787	787	100	30	0.1
±5	5	1000	825	205	62	21	0.1
±5	5	150	698	174	66	30	0.1
±5	10	1000	750	82.5	58	22	0.1
±5	10	150	619	68.1	60	30	0.1

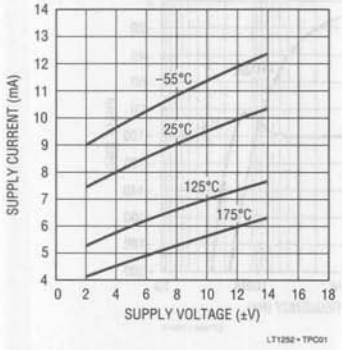
NTSC VIDEO (Note 1)

V_S	A_V	R_L	R_F	R_G	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE
±12	2	1000	1000	1000	0.02%	0.02°
±12	2	150	1000	1000	0.03%	0.04°
±5	2	1000	1000	1000	0.02%	0.08°
±5	2	150	1000	1000	0.01%	0.09°

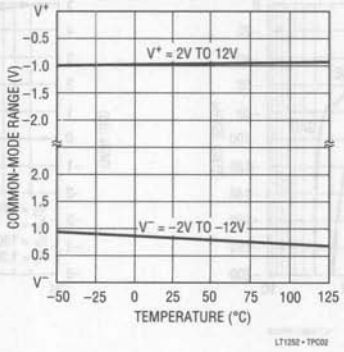
Note 1: Differential Gain and Phase are measured using a Tektronix TSG 120 YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Ten identical amplifier stages were cascaded giving an effective resolution of 0.01% and 0.01°.

TYPICAL PERFORMANCE CHARACTERISTICS

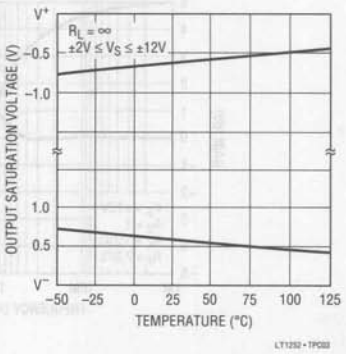
Supply Current vs Supply Voltage



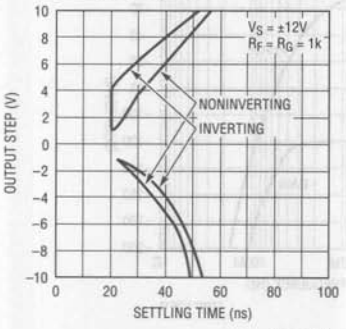
Input Common-Mode Limit vs Temperature



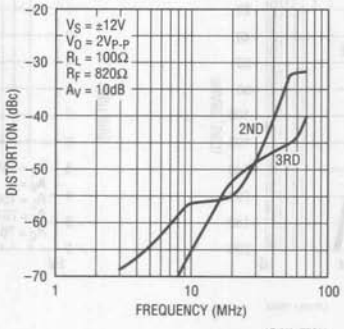
Output Saturation Voltage vs Temperature



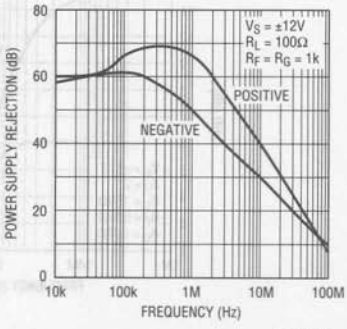
Settling Time to 10mV vs Output Step



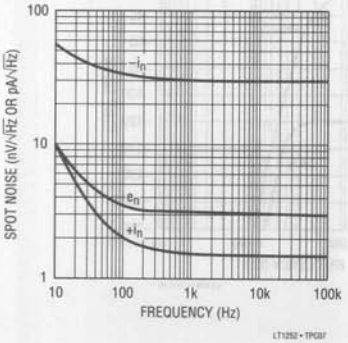
2nd and 3rd Harmonic Distortion vs Frequency



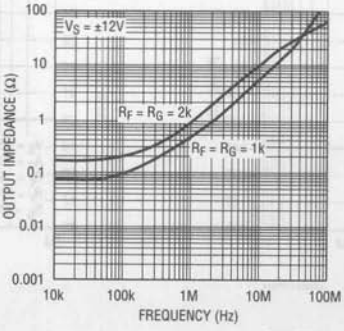
Power Supply Rejection vs Frequency



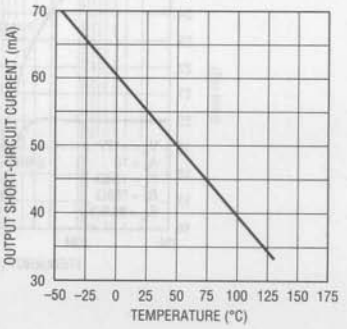
Spot Noise Voltage and Current vs Frequency



Output Impedance vs Frequency



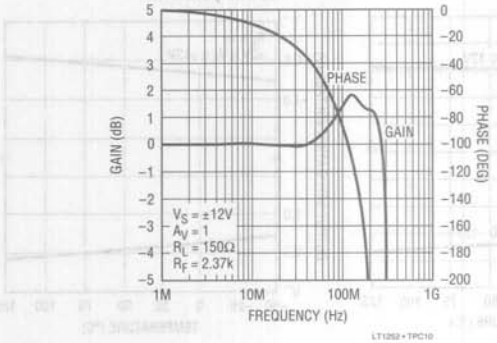
Output Short-Circuit Current vs Junction Temperature



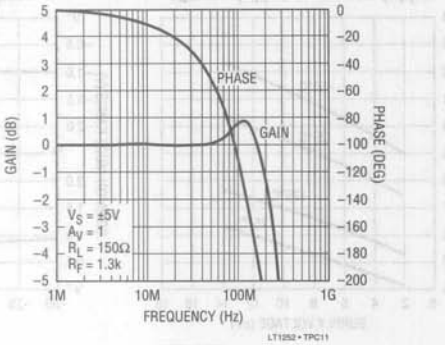
2

TYPICAL PERFORMANCE CHARACTERISTICS

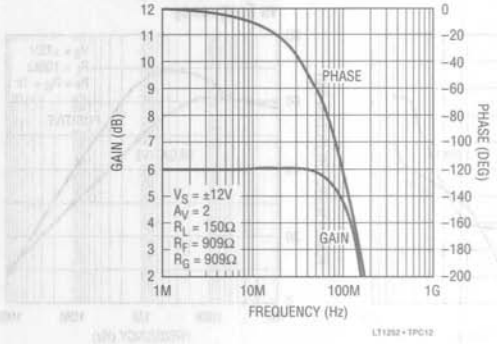
±12V Frequency Response



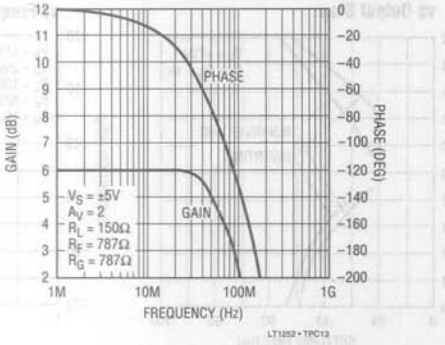
±5V Frequency Response



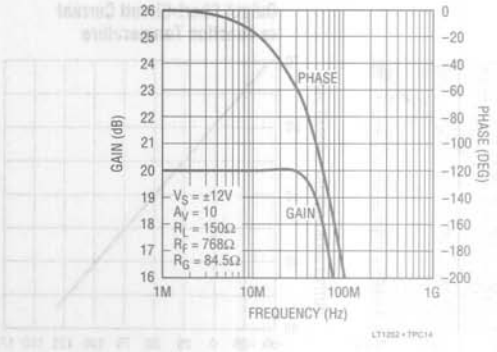
±12V Frequency Response



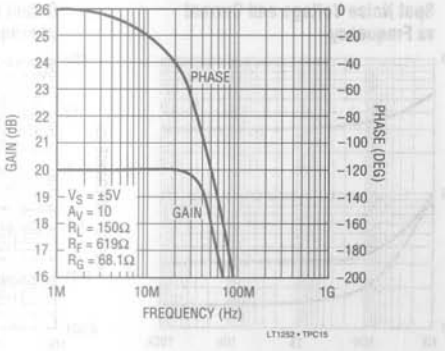
±5V Frequency Response



±12V Frequency Response

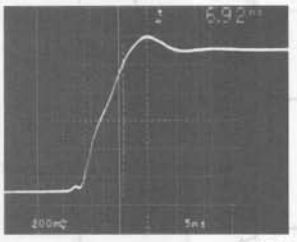


±5V Frequency Response



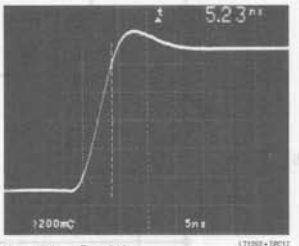
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



$V_S = \pm 5V$
$A_V = 1$
$R_L = 150\Omega$
$R_F = 619\Omega$
$V_O = 1V$

Transient Response

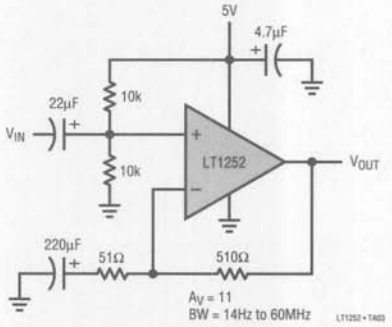


$V_S = \pm 5V$ $R_F = 619\Omega$
$A_V = 10$ $R_G = 68.1\Omega$
$R_L = 150\Omega$ $V_O = 1.5V$

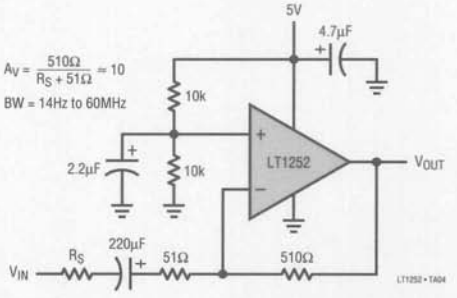
2

TYPICAL APPLICATIONS

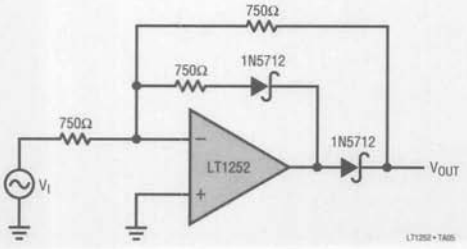
Single Supply AC-Coupled Amplifier Noninverting



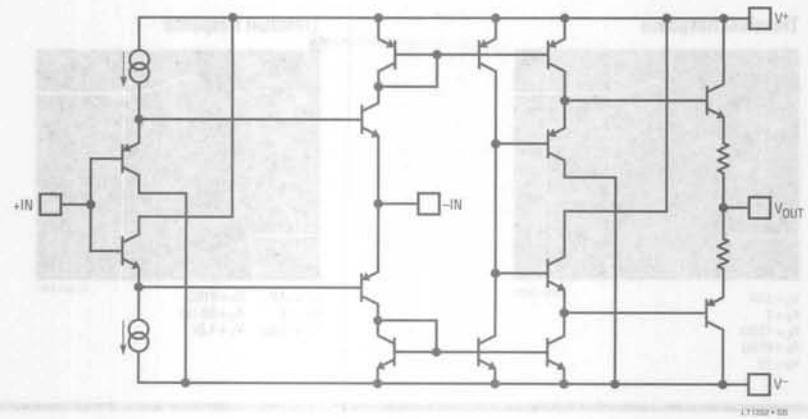
Single Supply AC-Coupled Amplifier Inverting



Half Wave Rectifier



SIMPLIFIED SCHEMATIC



Low Cost Dual and Quad Video Amplifiers

FEATURES

- Low Cost
- Current Feedback Amplifiers
- Differential Gain: 0.03%, $R_L = 150\Omega$, $V_S = \pm 5V$
- Differential Phase: 0.28°, $R_L = 150\Omega$, $V_S = \pm 5V$
- Flat to 30MHz, 0.1dB
- 90MHz Bandwidth on ±5V
- Wide Supply Range: ±2V(4V) to ±14V(28V)
- Low Power: 60mW per Amplifier at ±5V

APPLICATIONS

- RGB Cable Drivers
- Composite Video Cable Drivers
- Gain Blocks in IF Stages

DESCRIPTION

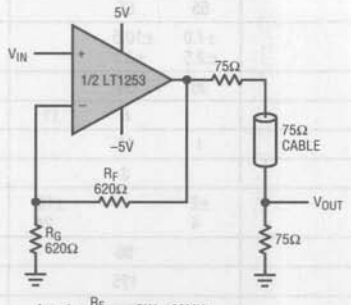
The LT1253 is a low cost dual current feedback amplifier for video applications. The LT1254 is a quad version of the LT1253. The amplifiers are completely isolated except for the power supply pins and therefore have excellent isolation, over 94dB at 5MHz. Dual and quad amplifiers significantly reduce costs compared with singles; the number of insertions is reduced and fewer supply bypass capacitors are required. In addition, these duals and quads cost less per amplifier than single video amplifiers.

The LT1253/LT1254 amplifiers are ideal for driving low impedance loads such as cables and filters. The wide bandwidth and high slew rate of these amplifiers make driving RGB signals between PCs and workstations easy. The excellent linearity of these amplifiers makes them ideal for composite video.

The LT1253 is available in 8-pin DIPs and the S8 surface mount package. The LT1254 is available in 14-pin DIPs and the S14 surface mount package. Both parts have the industry standard dual and quad op amp pin out. For higher performance, see the LT1229/LT1230.

2

TYPICAL APPLICATION

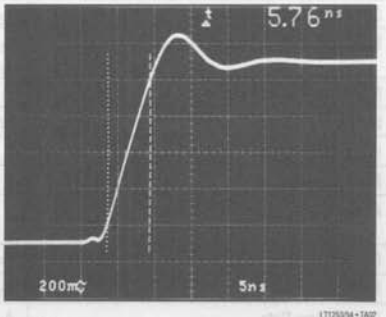


$A_V = 1 + \frac{R_F}{R_G}$ BW = 90MHz

AT AMPLIFIER OUTPUT.
6dB LESS AT V_{OUT}.

LT1253/54 • TA01

Transient Response



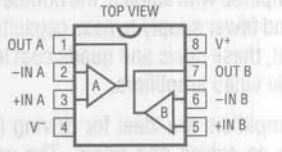
LT1253/54 • TA02

$V_S = \pm 5V$
$A_V = 2$
$R_L = 150\Omega$
$V_O = 1V$

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 28V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1253C, LT1254C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 2) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

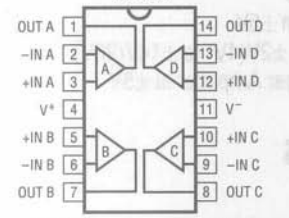
PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LT1253CN8 LT1253CS8
S8 PART MARKING
1253



N PACKAGE 14-LEAD PLASTIC DIP
S PACKAGE 14-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LT1254CN LT1254CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V to ±12V, unless otherwise noted.

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			5	15	mV
$+I_B$	Noninverting Bias Current			1	15	µA
$-I_B$	Inverting Bias Current			20	100	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = ±5V, V_O = ±2V, R_L = 150Ω	560	1500		V/V
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±12V	60	70		dB
CMRR	Common-Mode Rejection Ratio	V_S = ±5V, V_{CM} = ±2V	55	65		dB
V_{OUT}	Maximum Output Voltage Swing	V_S = ±12V, R_L = 500Ω V_S = ±5V, R_L = 150Ω	±7.0 ±2.5	±10.5 ±3.7		V V
I_{OUT}	Maximum Output Current		30	55		mA
I_S	Supply Current	Per Amplifier		6	11	mA
R_{IN}	Input Resistance		1	10		MΩ
C_{IN}	Input Capacitance			3		pF
	Power Supply Range Dual Single		±2 4		±12 24	V V
	Channel Separation	f = 10MHz		88		dB
SR	Input Slew Rate	A_V = 1		125		V/µs
	Output Slew Rate	A_V = 2		250		V/µs

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V to ±12V, unless otherwise noted.

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Small-Signal Rise Time	V_S = ±12V, A_V = 2		3.5		ns
	Rise and Fall Time	V_S = ±5V, A_V = 2, V_{OUT} = 1V_{P-P}		5.8		ns
t_p	Propagation Delay	V_S = ±5V, A_V = 2		3.5		ns

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1253CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1253CS8: $T_J = T_A + (P_D \times 150°C/W)$
LT1254CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1254CS: $T_J = T_A + (P_D \times 100°C/W)$

TYPICAL AC PERFORMANCE

BANDWIDTH

V_S	A_V	R_L	R_F	R_G	Small Signal −3dB BW (MHz)	Small Signal −0.1dB BW (MHz)	Small Signal Peaking (dB)
±12	1	1000	1100	None	270	51	3.4
±12	1	150	1000	None	204	48	1.3
±12	−1	1000	750	150	110	59	0.1
±12	−1	150	768	768	89	50	0.1
±12	2	1000	715	715	179	76	0.3
±12	2	150	715	715	117	62	0
±12	5	1000	680	180	106	42	0
±12	5	150	680	180	90	47	0
±12	10	1000	620	68.1	89	49	0.1
±12	10	150	620	68.1	80	46	0.1
±5	1	1000	787	None	218	53	1.5
±5	1	150	787	None	158	91	0.1
±5	−1	1000	715	715	76	28	0.1
±5	−1	150	715	715	70	30	0.1
±5	2	1000	620	620	117	58	0.1
±5	2	150	620	620	92	52	0.1
±5	5	1000	620	150	82	36	0
±5	5	150	620	150	72	34	0
±5	10	1000	562	61.9	70	35	0
±5	10	150	562	61.9	65	28	0

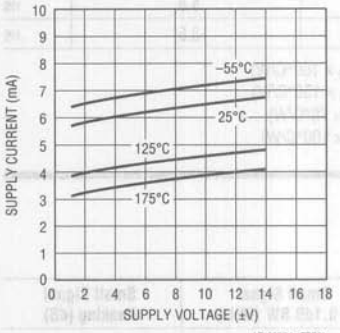
NTSC VIDEO (Note 1)

V_S	A_V	R_L	R_F	R_G	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE
±12	2	1000	750	750	0.01%	0.03°
±12	2	150	750	750	0.01%	0.12°
±5	2	1000	750	750	0.03%	0.18°
±5	2	150	750	750	0.03%	0.28°

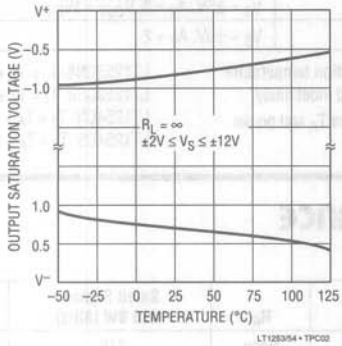
Note 1: Differential Gain and Phase are measured using a Tektronix TSG 120 YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Ten identical amplifier stages were cascaded giving an effective resolution of 0.01% and 0.01°.

TYPICAL PERFORMANCE CHARACTERISTICS

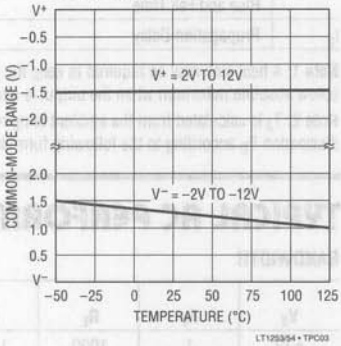
Supply Current vs Supply Voltage



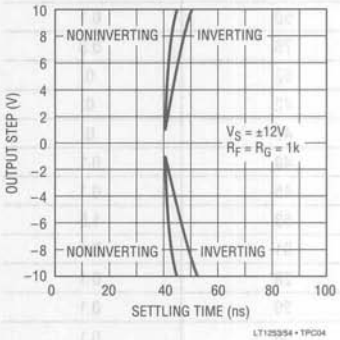
Output Saturation Voltage vs Temperature



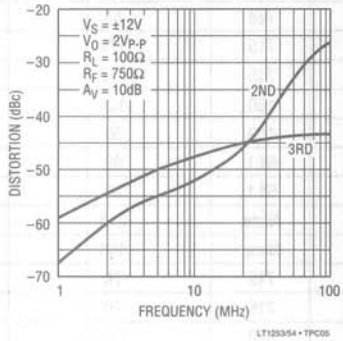
Input Common-Mode Limit vs Temperature



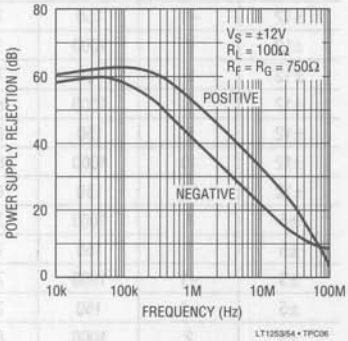
Settling Time to 10mV vs Output Step



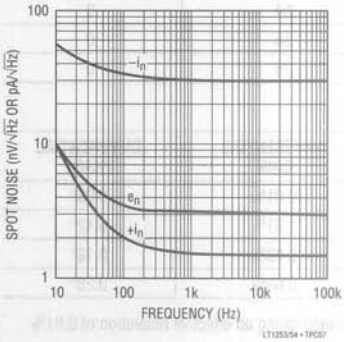
2nd and 3rd Harmonic Distortion vs Frequency



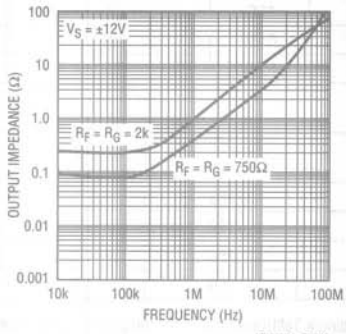
Power Supply Rejection vs Frequency



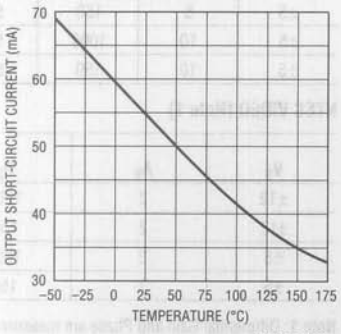
Spot Noise Voltage and Current vs Frequency



Output Impedance vs Frequency

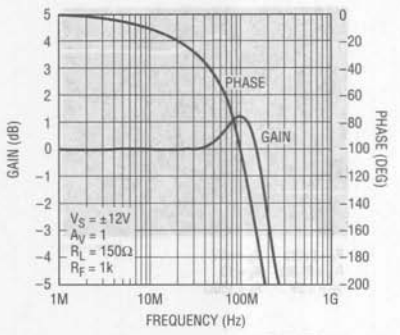


Output Short-Circuit Current vs Temperature

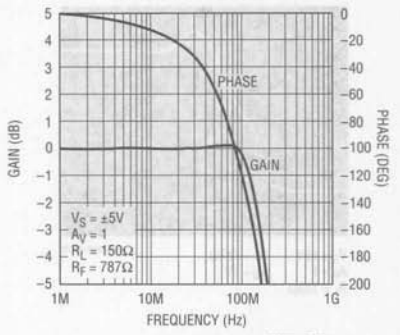


TYPICAL PERFORMANCE CHARACTERISTICS

±12V Frequency Response

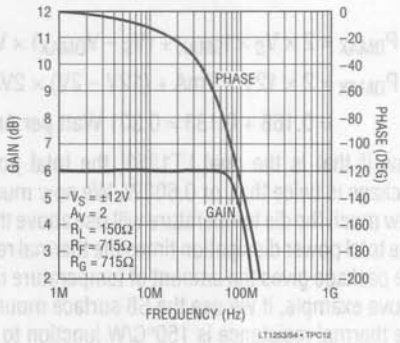


±5V Frequency Response

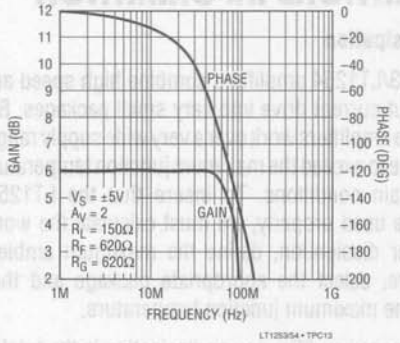


2

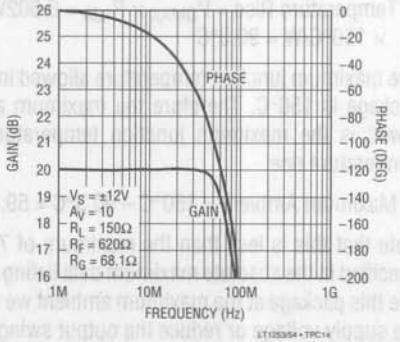
±12V Frequency Response



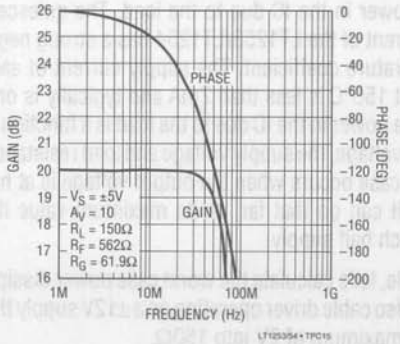
±5V Frequency Response



±12V Frequency Response

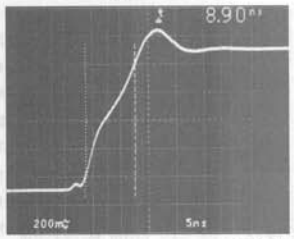


±5V Frequency Response



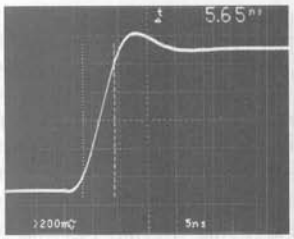
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



$V_S = \pm 5V$ $R_F = 787\Omega$
$A_V = 1$ $V_O = 1V$
$R_L = 150\Omega$

Transient Response



$R_F = 562\Omega$ $V_S = \pm 5V$
$R_G = 61.9\Omega$ $A_V = 10$
$V_O = 1.5V$ $R_L = 150\Omega$

APPLICATIONS INFORMATION

Power Dissipation

The LT1253/LT1254 amplifiers combine high speed and large output current drive into very small packages. Because these amplifiers work over a very wide supply range, it is possible to exceed the maximum junction temperature under certain conditions. To insure that the LT1253/LT1254 are used properly, we must calculate the worst case power dissipation, define the maximum ambient temperature, select the appropriate package and then calculate the maximum junction temperature.

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1253/LT1254 has a strong negative temperature coefficient. The supply current of each amplifier at 150°C is less than 7mA and typically is only 4.5mA. The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, let's calculate the worst case power dissipation in a video cable driver operating on a ±12V supply that delivers a maximum of 2V into 150Ω.

$$P_{DMAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OMAX}) \times V_{OMAX}/R_L$$

$$P_{DMAX} = 2 \times 12V \times 7mA + (12V - 2V) \times 2V/150$$

$$= 0.168 + 0.133 = 0.301 \text{ Watt per Amp}$$

Now if that is the dual LT1253, the total power in the package is twice that, or 0.602W. We now must calculate how much the die temperature will rise above the ambient. The total power dissipation times the thermal resistance of the package gives the amount of temperature rise. For the above example, if we use the S8 surface mount package, the thermal resistance is 150°C/W junction to ambient in still air.

$$\text{Temperature Rise} = P_{DMAX} \times R_{\theta JA} = 0.602W \times 150°C/W = 90.3°C$$

The maximum junction temperature allowed in the plastic package is 150°C. Therefore the maximum ambient allowed is the maximum junction temperature less the temperature rise.

$$\text{Maximum Ambient} = 150°C - 90.3°C = 59.7°C$$

Note that this is less than the maximum of 70°C that is specified in the absolute maximum data listing. In order to use this package at the maximum ambient we must lower the supply voltage or reduce the output swing.

APPLICATIONS INFORMATION

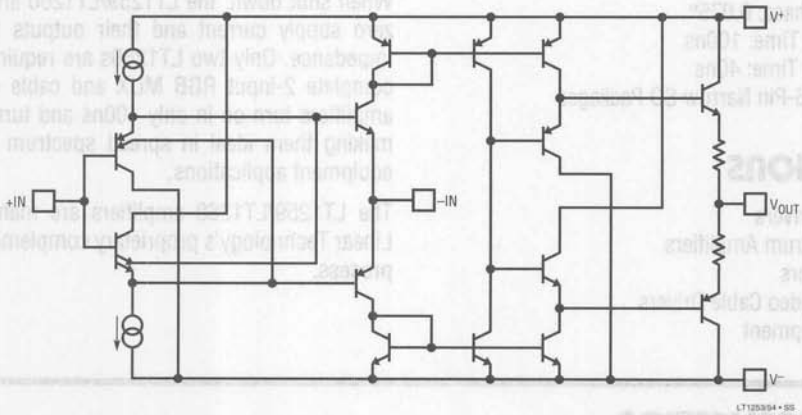
As a guideline to help in the selection of the LT1253/LT1254, the following table describes the maximum supply voltage that can be used with each part based on the following assumptions:

1. The maximum ambient is 70°C.
2. The load is a double-terminated video cable, 150Ω.
3. The maximum output voltage is 2V (peak or DC).

		MAX POWER at MAX T_A
LT1253CN8	$V_S < \pm 14$ (Abs Max)	0.800W
LT1253CS8	$V_S < \pm 10.6$	0.533W
LT1254CN	$V_S < \pm 11.4$	1.143W
LT1254CS	$V_S < \pm 7.6$	0.727W

SIMPLIFIED SCHEMATIC

One Amplifier



2

Low Cost Dual and Triple 130MHz Current Feedback Amplifiers with Shutdown

FEATURES

- **90MHz Bandwidth on ±5V**
- **0.1dB Gain Flatness >30MHz**
- **Completely Off in Shutdown, 0μA Supply Current**
- High Slew Rate: 1600V/μs
- Wide Supply Range: ±2V(4V) to ±15V(30V)
- 60mA Output Current
- Low Supply Current: 5mA/Amplifier
- Differential Gain: 0.016%
- Differential Phase: 0.075°
- Fast Turn-On Time: 100ns
- Fast Turn-Off Time: 40ns
- 14-Pin and 16-Pin Narrow SO Packages

APPLICATIONS

- RGB Cable Drivers
- Spread Spectrum Amplifiers
- MUX Amplifiers
- Composite Video Cable Drivers
- Portable Equipment

DESCRIPTION

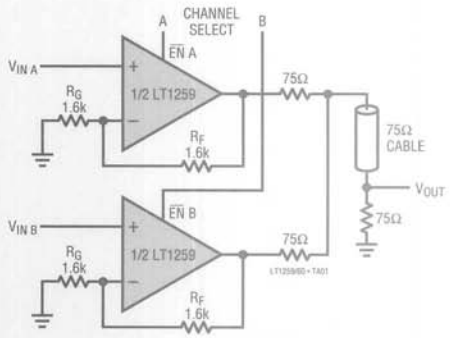
The LT1259 contains two independent 130MHz current feedback amplifiers, each with a shutdown pin. These amplifiers are designed for excellent linearity while driving cables and other low impedance loads. The LT1260 is a triple version especially suited to RGB video applications. These amplifiers operate on all supplies from single 5V to ±15V and draw only 5mA per amplifier when active.

When shut down, the LT1259/LT1260 amplifiers draw zero supply current and their outputs become high impedance. Only two LT1260s are required to make a complete 2-input RGB MUX and cable driver. These amplifiers turn on in only 100ns and turn off in 40ns, making them ideal in spread spectrum and portable equipment applications.

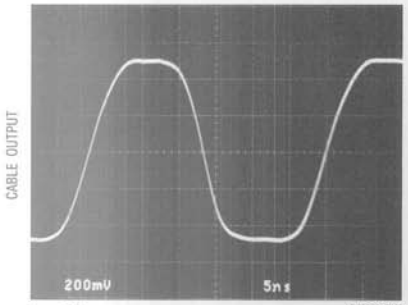
The LT1259/LT1260 amplifiers are manufactured on Linear Technology's proprietary complementary bipolar process.

TYPICAL APPLICATION

2-Input Video MUX Cable Driver



Square Wave Response

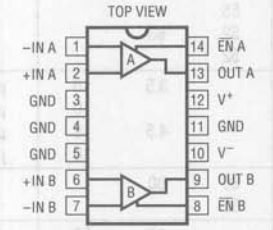


R_L = 150Ω
f = 30MHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range (Note 2) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 4) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

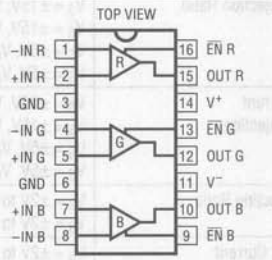


N PACKAGE 14-LEAD PLASTIC DIP
S PACKAGE 14-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LT1259CN*
LT1259CS*



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER

LT1260CN*
LT1260CS*

*See Notes 2 and 3.
Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, each amplifier V_{CM} = 0V, ±5V ≤ V_S ≤ ±15V, $\overline{EN}$ pins = 0V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			2	10	mV
			●			12	mV
	Input Offset Voltage Drift		●		15		µV/°C
I_{IN}^+	Noninverting Input Current	T_A = 25°C			0.5	3	µA
			●			6	µA
I_{IN}^-	Inverting Input Current	T_A = 25°C			8	60	µA
			●			70	µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			3.6		nV/√Hz
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.3		pA/√Hz
$-i_n$	Inverting Input Noise Current Density	f = 1kHz			45		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±13V, V_S = ±15V	●	2	17		MΩ
		V_{IN} = ±3V, V_S = ±5V	●	2	25		MΩ
C_{IN}	Input Capacitance	Enabled			2		pF
		Disabled			4		pF
C_{OUT}	Output Capacitance	Disabled			4.4		pF

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, each amplifier $V_{CM} = 0V$, $\pm 5V \le V_S \le \pm 15V$, $\overline{EN}$ pins = 0V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	$V_S = \pm 15V$, $T_A = 25°C$		±13	±13.5		V
			●	±12			V
		$V_S = \pm 5V$, $T_A = 25°C$		±3	±3.5		V
			●	±2			V
V_{OUT}	Maximum Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1k$	●	±12.0	±14.0		V
		$V_S = \pm 5V$, $R_L = 150\Omega$, $T_A = 25°C$		±3.0	±3.7		V
			●	±2.5			V
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 13V$, $T_A = 25°C$		55	69		dB
		$V_S = \pm 15V$, $V_{CM} = \pm 12V$	●	55			dB
		$V_S = \pm 5V$, $V_{CM} = \pm 3V$, $T_A = 25°C$		52	63		dB
		$V_S = \pm 5V$, $V_{CM} = \pm 2V$	●	52			dB
	Inverting Input Current Common-Mode Rejection	$V_S = \pm 15V$, $V_{CM} = \pm 13V$, $T_A = 25°C$			3.5	10	µA/V
		$V_S = \pm 15V$, $V_{CM} = \pm 12V$	●			10	µA/V
		$V_S = \pm 5V$, $V_{CM} = \pm 3V$, $T_A = 25°C$			4.5	10	µA/V
		$V_S = \pm 5V$, $V_{CM} = \pm 2V$	●			10	µA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-, $T_A = 25°C$		60	80		dB
		$V_S = \pm 3V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-	●	60			dB
	Noninverting Input Current Power Supply Rejection	$V_S = \pm 2V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-, $T_A = 25°C$			15	50	nA/V
		$V_S = \pm 3V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-	●			60	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 2V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-, $T_A = 25°C$			0.1	5	µA/V
		$V_S = \pm 3V$ to $\pm 15V$, $\overline{EN}$ Pins at V^-	●			5	µA/V
A_V	Large-Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 1k$	●	57	72		dB
		$V_S = \pm 5V$, $V_{OUT} = \pm 2V$, $R_L = 150\Omega$	●	57	69		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 1k$	●	120	300		kΩ
		$V_S = \pm 5V$, $V_{OUT} = \pm 2V$, $R_L = 150\Omega$	●	100	200		kΩ
I_{OUT}	Maximum Output Current	$R_L = 0\Omega$, $T_A = 25°C$		30	60		mA
I_S	Supply Current per Amplifier (Note 5)	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = 25°C$			5.0	7.5	mA
			●			7.9	mA
		$V_S = \pm 5V$, $V_{OUT} = 0V$, $T_A = 25°C$			4.5	6.7	mA
	Disable Supply Current per Amplifier	$V_S = \pm 15V$, $\overline{EN}$ Pin Voltage = 14.5V, $R_L = 150\Omega$	●		3	16.7	µA
		$V_S = \pm 15V$, Sink 1µA From $\overline{EN}$ Pin	●		1	2.7	µA
	Enable Pin Current	$V_S = \pm 15V$, $\overline{EN}$ Pin Voltage = 0V, $T_A = 25°C$			60	100	µA
			●			150	µA
SR	Slew Rate (Note 6)	$T_A = 25°C$		900	1600		V/µs
t_{ON}	Turn-On Delay Time (Note 7)	$A_V = 10$, $T_A = 25°C$			100	200	ns
t_{OFF}	Turn-Off Delay Time (Note 7)	$A_V = 10$, $T_A = 25°C$			40	150	ns
t_r, t_f	Small-Signal Rise and Fall Time	$V_S = \pm 12V$, $R_F = R_G = 1.5k$, $R_L = 150\Omega$			4.2		ns
	Propagation Delay	$V_S = \pm 12V$, $R_F = R_G = 1.5k$, $R_L = 150\Omega$			4.7		ns
	Small-Signal Overshoot	$V_S = \pm 12V$, $R_F = R_G = 1.5k$, $R_L = 150\Omega$			5		%
t_S	Settling Time	0.1%, $V_{OUT} = 10V$, $R_F = R_G = 1.5k$, $R_L = 1k$			75		ns
	Differential Gain (Note 8)	$V_S = \pm 12V$, $R_F = R_G = 1.5k$, $R_L = 150\Omega$			0.016		%
	Differential Phase (Note 8)	$V_S = \pm 12V$, $R_F = R_G = 1.5k$, $R_L = 150\Omega$			0.075		DEG

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: A heat sink may be required depending on the power supply voltage and how many amplifiers have their outputs short circuited.

Note 2: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

ELECTRICAL CHARACTERISTICS

Note 3: Ground pins are not internally connected. For best performance, connect to ground.

Note 4: T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formulas:

LT1259CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1259CS: $T_J = T_A + (P_D \times 110°C/W)$
LT1260CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1260CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 5: The supply current of the LT1259/LT1260 has a negative temperature coefficient. See Typical Performance Characteristics.

Note 6: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with R_F = 1k, R_G = 110Ω and R_L = 1k.

Note 7: Turn-on delay time is measured while operating on ±5V supplies with R_F = 1k, R_G = 110Ω and R_L = 150Ω. The t_{ON} is measured from control input to appearance of 0.5V at the output, for V_{IN} = 0.1V. Likewise, turn-off delay time is measured from control input to appearance of 0.5V on the output for V_{IN} = 0.1V.

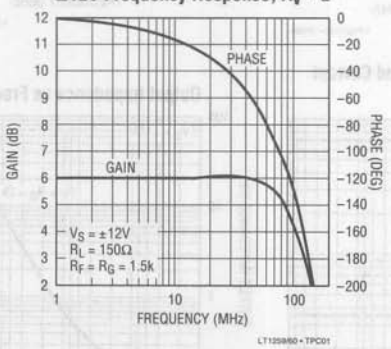
Note 8: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Six identical amplifier stages were cascaded giving an effective resolution of 0.016% and 0.016°.

TYPICAL AC PERFORMANCE

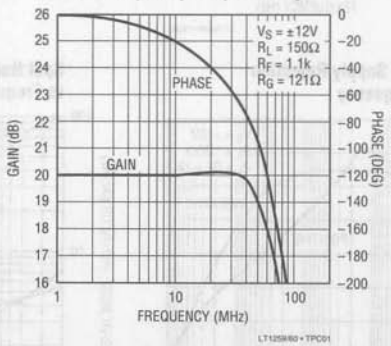
V_S (V)	A_V	R_L (Ω)	R_F (Ω)	R_G (Ω)	SMALL SIGNAL −3dB BW (MHz)	SMALL SIGNAL 0.1dB BW (MHz)	SMALL SIGNAL PEAKING (dB)
±12	2	150	1.5k	1.5k	130	53	0.1
±5	2	150	1.1k	1.1k	93	40	0
±12	10	150	1.1k	121	69	20	0.13
±5	10	150	825	90.9	61	16	0

TYPICAL PERFORMANCE CHARACTERISTICS

±12V Frequency Response, A_V = 2

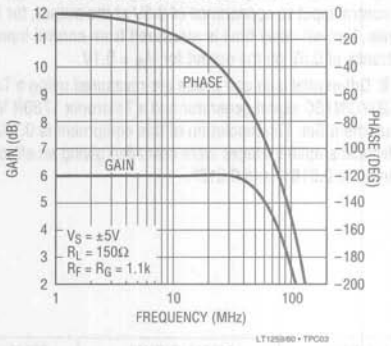


±12V Frequency Response, A_V = 10



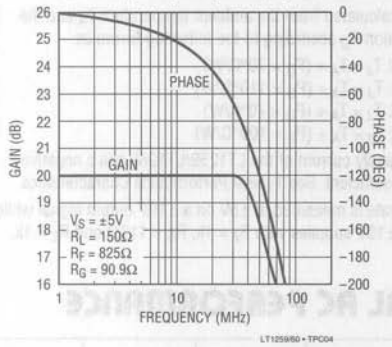
TYPICAL PERFORMANCE CHARACTERISTICS

±5V Frequency Response, $A_V = 2$



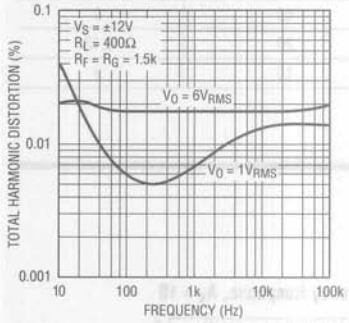
LT1259/60 • TPC03

±5V Frequency Response, $A_V = 10$



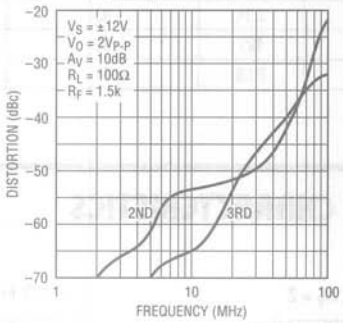
LT1259/60 • TPC04

Total Harmonic Distortion vs Frequency



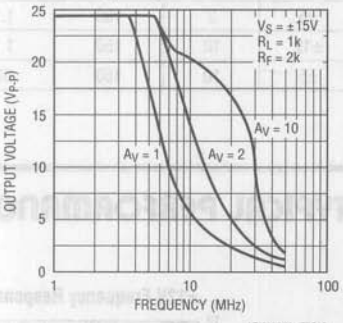
LT1259/60 • TPC05

2nd and 3rd Harmonic Distortion vs Frequency



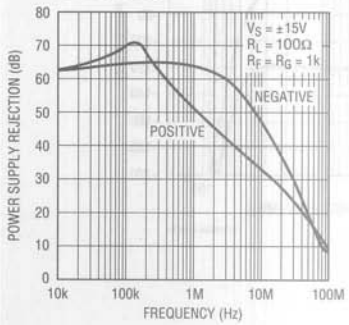
LT1259/60 • TPC06

Maximum Undistorted Output vs Frequency



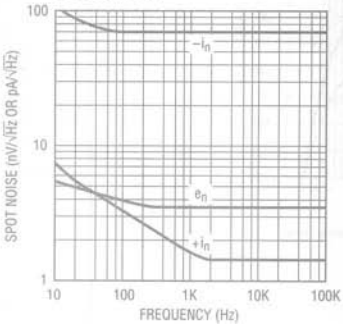
LT1259/60 • TPC07

Power Supply Rejection vs Frequency



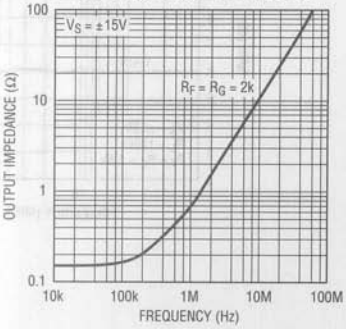
LT1259/60 • TPC08

Spot Noise Voltage and Current vs Frequency



LT1259/60 • TPC09

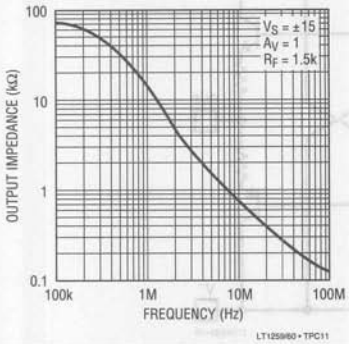
Output Impedance vs Frequency



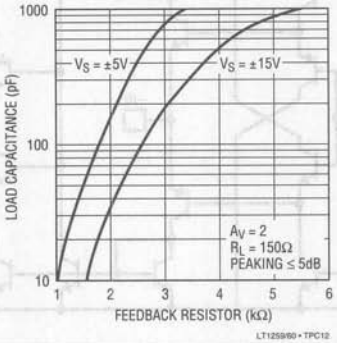
LT1259/60 • TPC10

TYPICAL PERFORMANCE CHARACTERISTICS

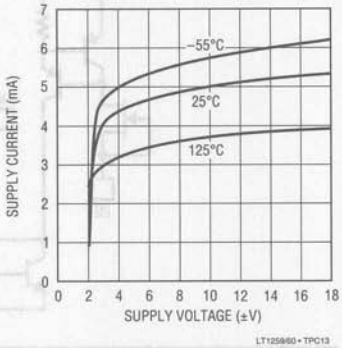
Output Impedance in Shutdown vs Frequency



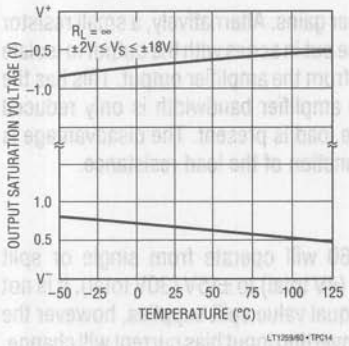
Maximum Capacitive Load vs Feedback Resistor



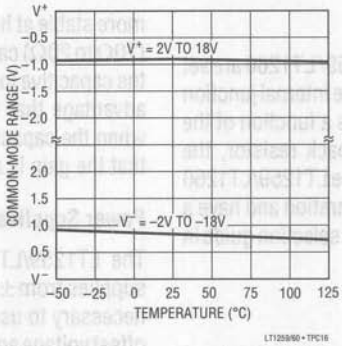
Supply Current vs Supply Voltage



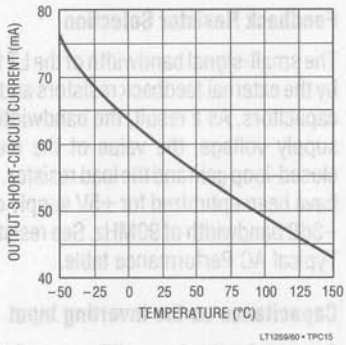
Output Saturation Voltage vs Temperature



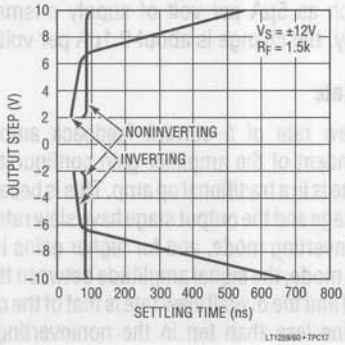
Input Common-Mode Limit vs Temperature



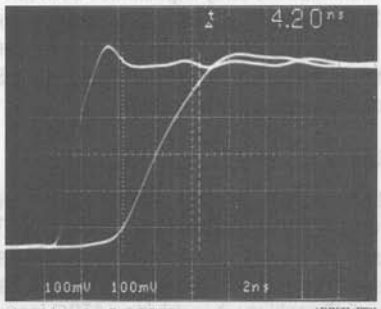
Output Short-Circuit Current vs Junction Temperature



Settling Time to 10mV vs Output Step

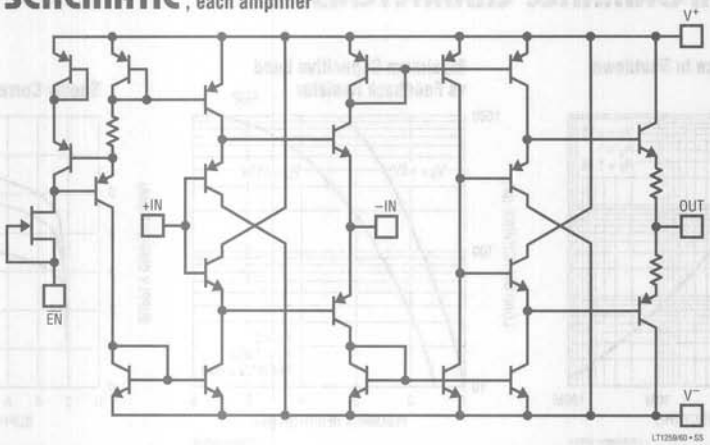


Small-Signal Rise Time



V_S = ±15V R_F = R_G = 1.6k
A_V = 2 R_L = 150Ω

SIMPLIFIED SCHEMATIC, each amplifier



APPLICATIONS INFORMATION

Feedback Resistor Selection

The small-signal bandwidth of the LT1259/ LT1260 are set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and the load resistor. The LT1259/LT1260 have been optimized for ±5V supply operation and have a –3dB bandwidth of 90MHz. See resistor selection guide in Typical AC Performance table.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response). See the section on Demo Board Information.

Capacitive Loads

The LT1259/LT1260 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for ≤5dB peaking when driving a 150Ω load at a gain of 2. This is a worst case condition. The amplifier is more stable at higher gains. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present. The disadvantage is that the gain is a function of the load resistance.

Power Supplies

The LT1259/LT1260 will operate from single or split supplies from ±2V (4V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 500μV per volt of supply mismatch. The inverting bias current can change as much as 5μA per volt of supply mismatch though typically, the change is about 0.1μA per volt.

Slew Rate

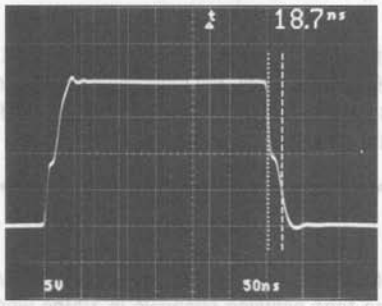
The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way slew rate is in a traditional op amp. This is because both the input stage and the output stage have slew rate limitations. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than ten in the noninverting mode, the overall slew rate is limited by the input stage.

APPLICATIONS INFORMATION

The input slew rate of the LT1259/LT1260 is approximately 270V/µs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and internal capacitances. At a gain of 10 with at 1k feedback resistor and ±15V supplies, the output slew rate is typically 1600V/µs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

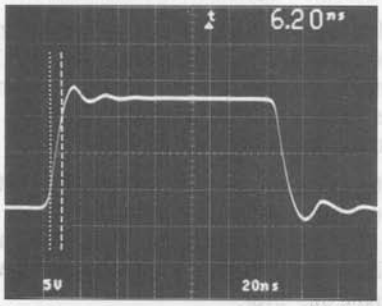
The graph of Maximum Undistorted Output vs Frequency relates the slew rate limitations to sinusoidal input for various gains.

Large-Signal Transient Response, $A_V = 2$



$V_S = \pm 15V$ $R_L = 400\Omega$
$R_F = R_G = 1.6k$

Large-Signal Transient Response, $A_V = 10$

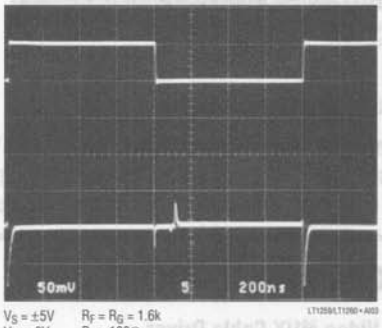


$V_S = \pm 15V$ $R_G = 110\Omega$
$R_F = 1k$ $R_L = 400\Omega$

Enable/Disable

The LT1259/LT1260 amplifiers have a unique high impedance, zero supply current mode which is controlled by independent $\overline{EN}$ pins. When disabled, an amplifier output looks like a 4.4pF capacitor in parallel with a 75k resistor, excluding feedback resistor effects. These amplifiers are designed to operate with open drain logic: the $\overline{EN}$ pins have internal pullups and the amplifiers draw zero current when these pins are high. To activate an amplifier, its $\overline{EN}$ pin is pulled to ground (or at least 2V below the positive supply). The enable pin current is approximately 60µA when activated. Input referred switching transients with no input signal applied are only 35mV positive and 80mV negative with $R_L = 100\Omega$.

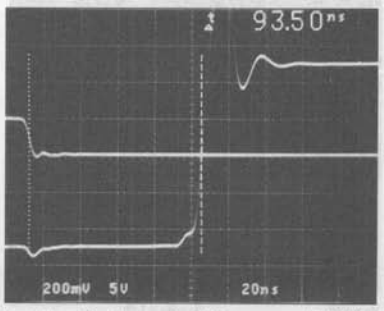
Output Switching Transient



$V_S = \pm 5V$ $R_F = R_G = 1.6k$
$V_{IN} = 0V$ $R_L = 100\Omega$

The enable/disable times are very fast when driven from standard 5V logic. The amplifier enables in about 100ns (50% point to 50% point) while operating on ±5V supplies. Likewise the disable time is approximately 40ns (50% point to 50% point) or 75ns to 90% of the final value. The output decay time is set by the output capacitance and load resistor.

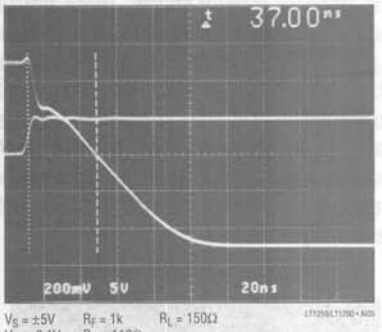
Amplifier Enable Time, $A_V = 10$



$V_S = \pm 5V$ $R_F = 1k$ $R_L = 150\Omega$
$V_{IN} = 0.1V$ $R_G = 110\Omega$

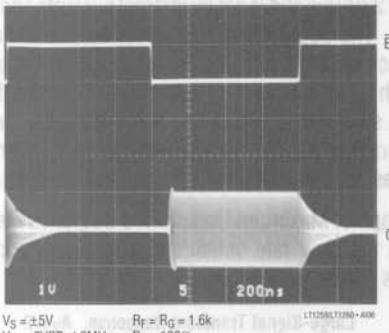
APPLICATIONS INFORMATION

Amplifier Disable Time, $A_V = 10$



$V_S = \pm 5V$ $R_F = 1k$ $R_L = 150\Omega$
$V_{IN} = 0.1V$ $R_G = 110\Omega$

Amplifier Enable/Disable Time, $A_V = 2$



$V_S = \pm 5V$ $R_F = R_G = 1.6k$
$V_{IN} = 2VPP$ at 2MHz $R_L = 100\Omega$

Differential Input Signal Swing

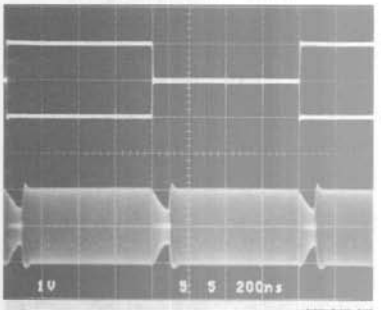
The differential input swing is limited to about ±6V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect. In the disabled mode however, the differential swing can be the same as the input swing, and the clamp voltage will set the maximum allowable input voltage.

TYPICAL APPLICATIONS

2-Input Video MUX Cable Driver

The application on the first page shows a low cost, 2-input video MUX cable driver. The scope photo displays the cable output of a 30MHz square wave driving 150Ω. In this circuit the active amplifier is loaded by R_F and R_G of the disabled amplifier, but in this case it only causes a 1.2% gain error. The gain error can be eliminated by configuring each amplifier as a unity-gain follower. The switching time between channels is 100ns when both $\overline{EN}$ A and $\overline{EN}$ B are driven.

2-Input Video MUX Switching Response



$V_S = \pm 5V$ $R_F = R_G = 1.6k$
$V_{IN\,A} = V_{IN\,2} = 2VPP$ at 2MHz $R_L = 100\Omega$

2-Input RGB MUX Cable Driver Demonstration Board

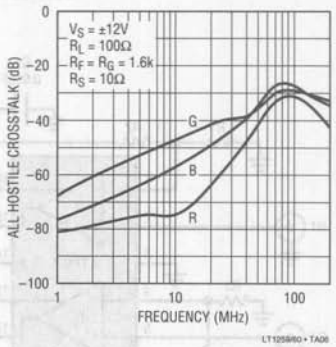
A complete 2-input RGB MUX has been fabricated on PC Demo Board #039A. The board incorporates two LT1260s with outputs summed through 75Ω back termination resistors as shown in the schematic. There are several things to note about Demo Board #039A:

1. The feedback resistors of the disabled LT1260 load the enabled amplifier and cause a small (1% to 2%) gain error depending on the values of R_F and R_G. Configure the amplifiers as unity-gain followers to eliminate this error.
2. The feedback node has minimum trace length connecting R_F and R_G to minimize stray capacitance.
3. Ground plane is pulled away from R_F and R_G on both sides of the board to minimize stray capacitance.

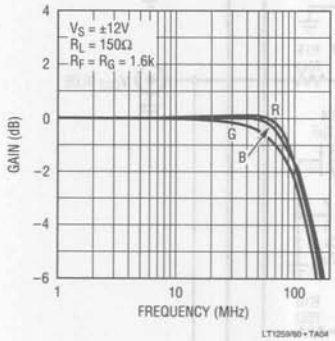
TYPICAL APPLICATIONS

4. Capacitors C1 and C6 are optional and only needed to reduce overshoot when $\overline{EN}$ 1 or $\overline{EN}$ 2 are activated with a long inductive ground wire.
5. The R, G and B amplifiers have slightly different frequency responses due to different output trace routing to R_F (between pins 3 and 4). All amplifiers have slightly less bandwidth in PCB #039 than when measured alone as shown in the Typical AC Performance table.
6. Part-to-part variation can change the peaking by ±0.25dB.

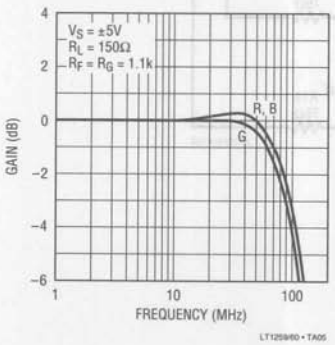
RGB Demo Board All Hostile Crosstalk



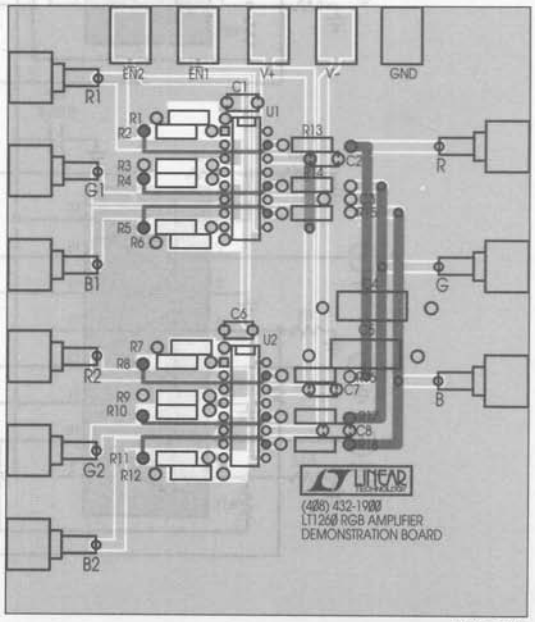
RGB Demo Board Gain vs Frequency



RGB Demo Board Gain vs Frequency



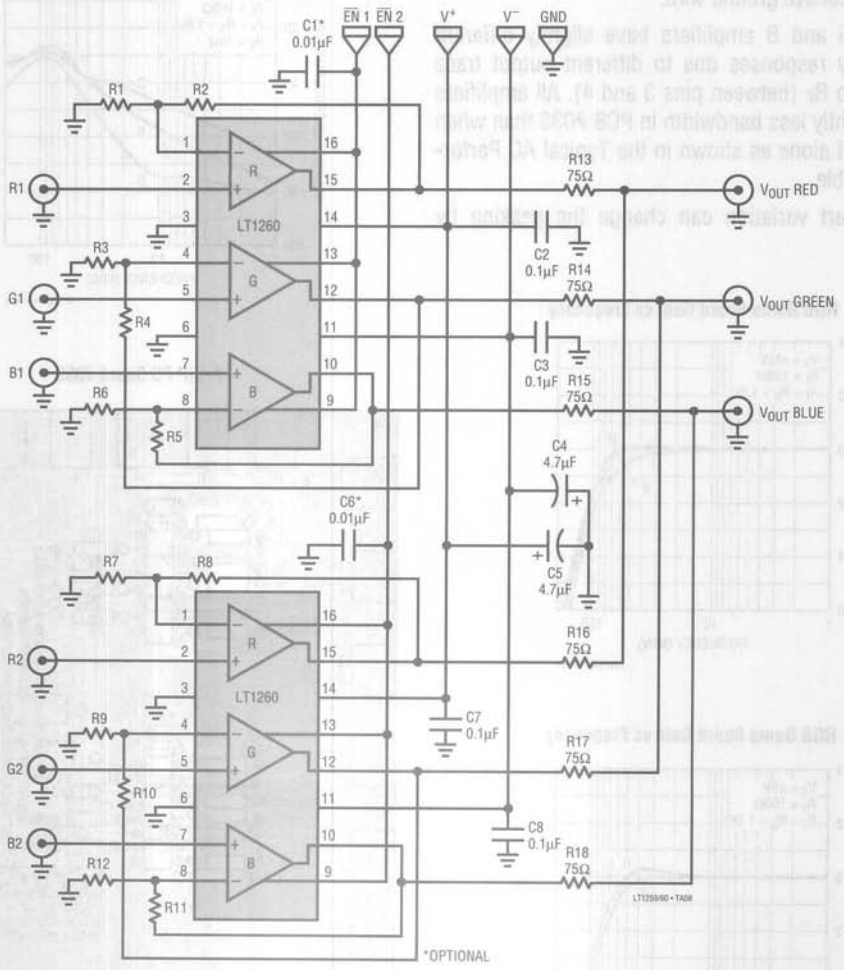
P-DIP PC Board #039



LT1259/60 • TA07

TYPICAL APPLICATIONS

Demonstration PC Board Schematic #039



12MHz, 400V/µs Op Amp

FEATURES

- **12MHz Gain-Bandwidth**
- **400V/µs Slew Rate**
- **1.25mA Maximum Supply Current**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 10nV/√Hz Input Noise Voltage
- 800µV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 70nA Maximum Input Offset Current
- 12V/mV Minimum DC Gain, R_L=1k
- 230ns Settling Time to 0.1%, 10V Step
- 280ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

The LT1354 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1354 has much lower supply current, lower input offset voltage, lower input bias current, and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

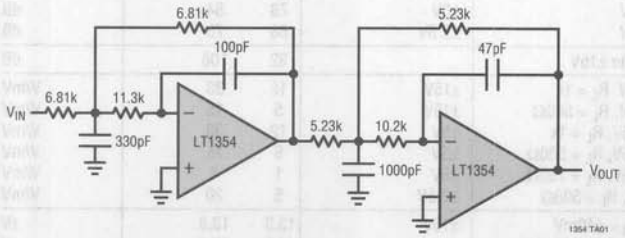
The LT1354 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1354 see the LT1355/LT1356 data sheet. For higher bandwidth devices with higher supply current see the LT1357 through LT1365 data sheets. Singles, duals, and quads of each amplifier are available.

C-Load is a trademark of Linear Technology Corporation

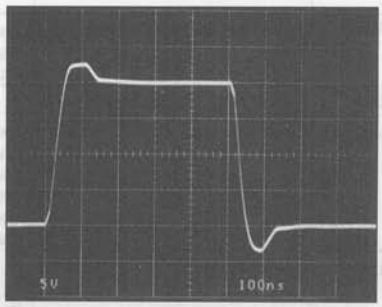
2

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



A_V = –1 Large-Signal Response



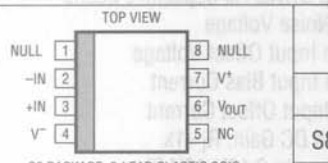
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

N8 PACKAGE, 8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1354CN8



S8 PACKAGE, 8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1354CS8
S8 PART MARKING
1354

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.3	0.8	mV
			±5V		0.3	0.8	mV
			±2.5V		0.4	1.0	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		20	70	nA
I_B	Input Bias Current		±2.5V to ±15V		80	300	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		10		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.6		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	70	160		MΩ
		Differential	±15V		11		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range $^+$		±15V	12.0	13.4		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.1		V
	Input Voltage Range $^-$		±15V		–13.2	–12.0	V
			±5V		–3.4	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	83	97		dB
		V_{CM} = ±2.5V	±5V	78	84		dB
		V_{CM} = ±0.5V	±2.5V	68	75		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	12	36		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	5	15		V/mV
		V_{OUT} = ±2.5V, R_L = 1k	±5V	12	36		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	5	15		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1	4		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	5	20		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.3	13.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	12.5	13.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.0	3.3		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = \pm12.5V$	±15V		25	30		mA
		$V_{OUT} = \pm3V$	±5V		20	25		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V		30	42		mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V		200	400		V/µs
			±5V		70	120		V/µs
	Full Power Bandwidth	10V Peak, (Note 3)	±15V			6.4		MHz
		3V Peak, (Note 3)	±5V			6.4		MHz
GBW	Gain-Bandwidth	f = 200kHz, R_L = 2k	±15V		9.0	12.0		MHz
			±5V		7.5	10.5		MHz
			±2.5V			9.0		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V			14		ns
			±5V			17		ns
	Overshoot	$A_V = 1$, 0.1V	±15V			20		%
			±5V			18		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V			16		ns
			±5V			19		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V			230		ns
		10V Step, 0.01%, $A_V = -1$	±15V			280		ns
		5V Step, 0.1%, $A_V = -1$	±5V			240		ns
		5V Step, 0.01%, $A_V = -1$	±5V			380		ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, R_L = 1k	±15V			2.2		%
			±5V			2.1		%
	Differential Phase	f = 3.58MHz, $A_V = 2$, R_L = 1k	±15V			3.1		Deg
			±5V			3.1		Deg
R_O	Output Resistance	$A_V = 1$, f = 100kHz	±15V			0.7		Ω
I_S	Supply Current		±15V			1.0	1.25	mA
			±5V			0.9	1.20	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.0	mV
			±5V	●			1.0	mV
			±2.5V	●			1.2	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			100	nA
I_B	Input Bias Current		±2.5V to ±15V	●			450	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	81			dB
		$V_{CM} = \pm2.5V$	±5V	●	77			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, R_L = 1k	±15V	●	10.0			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	3.3			V/mV
		$V_{OUT} = \pm2.5V$, R_L = 1k	±5V	●	10.0			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	3.3			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	3.3			V/mV

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	±15V	●	13.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	2.8			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12V$	±15V	●	24.0			mA
		$V_{OUT} = \pm 2.8V$	±5V	●	18.7			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	150			V/µs
			±5V	●	60			V/µs
GBW	Gain-Bandwidth	$f = 200kHz$, $R_L = 2k$	±15V	●	7.5			MHz
			±5V	●	6.0			MHz
I_S	Supply Current		±15V	●			1.45	mA
			±5V	●			1.40	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.5	mV
			±5V	●			1.5	mV
			±2.5V	●			1.7	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			200	nA
I_B	Input Bias Current		±2.5V to ±15V	●			550	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$	±15V	●	80			dB
		$V_{CM} = \pm 2.5V$	±5V	●	76			dB
		$V_{CM} = \pm 0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L = 1k$	±15V	●	7.0			V/mV
		$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	±15V	●	1.7			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 1k$	±5V	●	7.0			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	±5V	●	1.7			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	±5V	●	0.4			V/mV
		$V_{OUT} = \pm 1V$, $R_L = 500\Omega$	±2.5V	●	1.7			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	11.5			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	2.6			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 11.5V$	±15V	●	23.0			mA
		$V_{OUT} = \pm 2.6V$	±5V	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	23			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	120			V/µs
			±5V	●	50			V/µs

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
GBW	Gain-Bandwith	f = 200kHz, R_L = 2k	±15V	●	7.0			MHz
			±5V	●	5.5			MHz
I_S	Supply Current		±15V	●			1.50	mA
			±5V	●			1.45	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 3: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

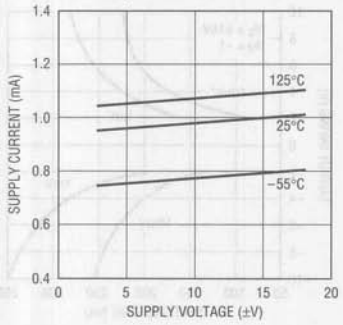
Note 4: This parameter is not 100% tested.

Note 5: The LT1354 is not tested and is not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

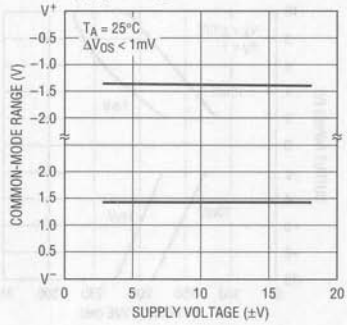
TYPICAL PERFORMANCE CHARACTERISTICS

2

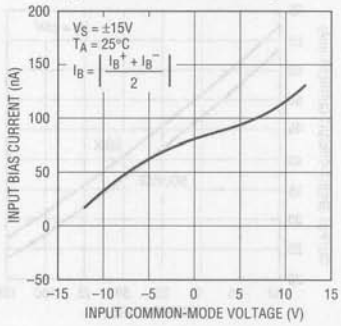
Supply Current vs Supply Voltage and Temperature



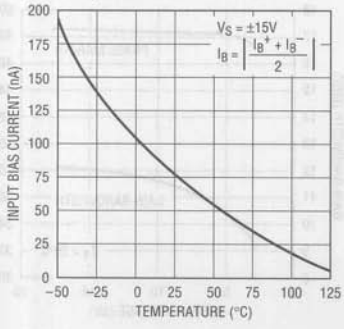
Input Common-Mode Range vs Supply Voltage



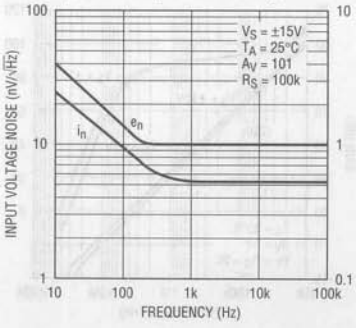
Input Bias Current vs Input Common-Mode Voltage



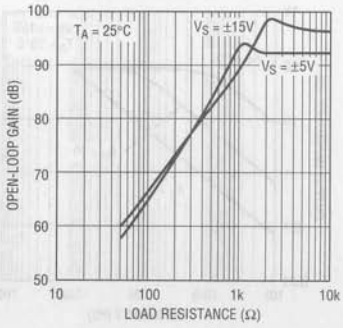
Input Bias Current vs Temperature



Input Noise Spectral Density

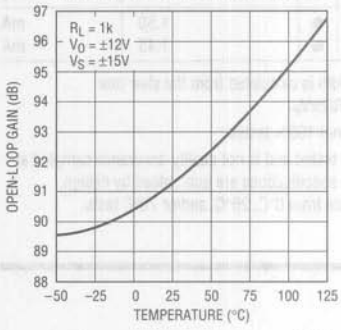


Open-Loop Gain vs Resistive Load

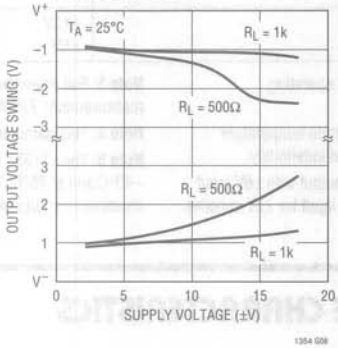


TYPICAL PERFORMANCE CHARACTERISTICS

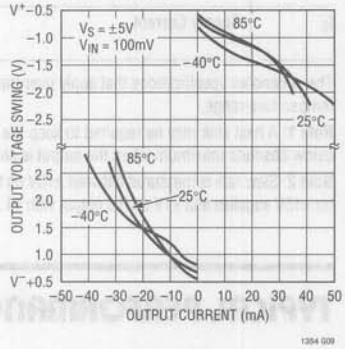
Open-Loop Gain vs Temperature



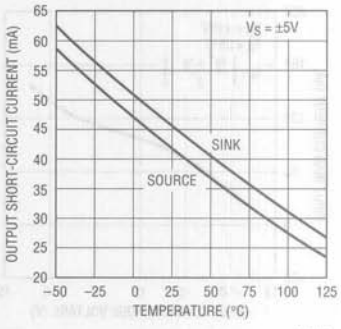
Output Voltage Swing vs Supply Voltage



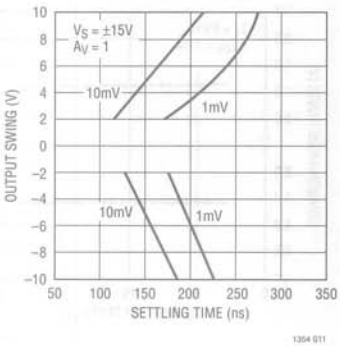
Output Voltage Swing vs Load Current



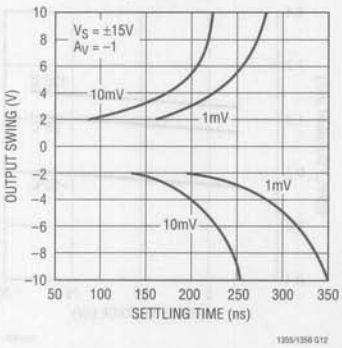
Output Short-Circuit Current vs Temperature



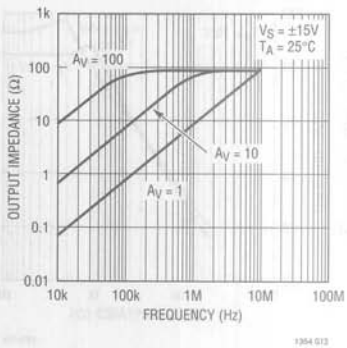
Settling Time vs Output Step (Noninverting)



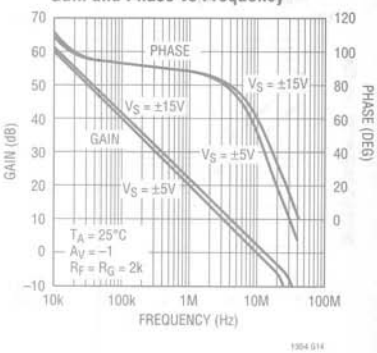
Settling Time vs Output Step (Inverting)



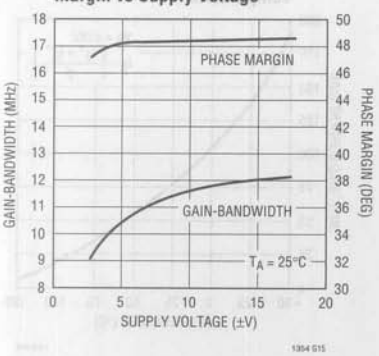
Output Impedance vs Frequency



Gain and Phase vs Frequency

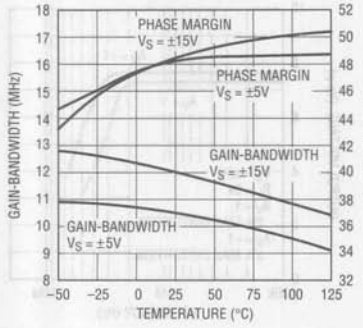


Gain-Bandwidth and Phase Margin vs Supply Voltage

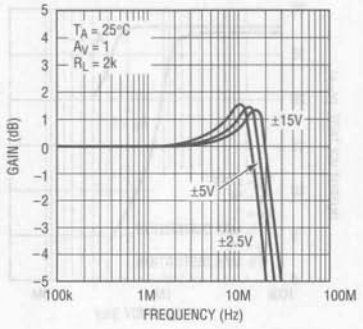


TYPICAL PERFORMANCE CHARACTERISTICS

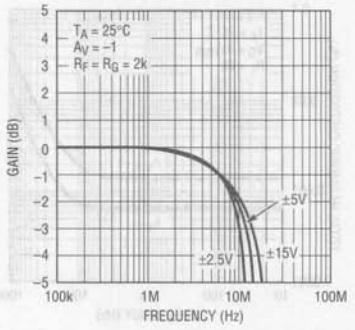
Gain-Bandwidth and Phase Margin vs Temperature



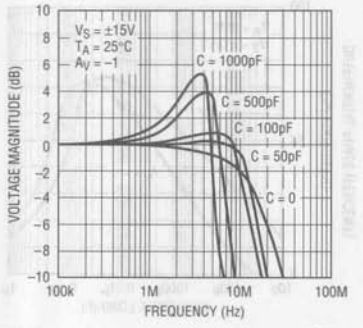
Frequency Response vs Supply Voltage (A_V = 1)



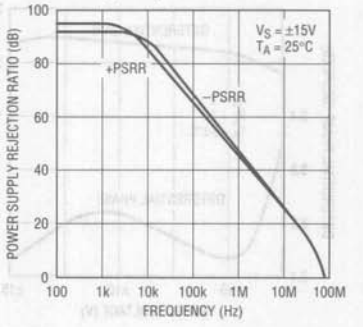
Frequency Response vs Supply Voltage (A_V = –1)



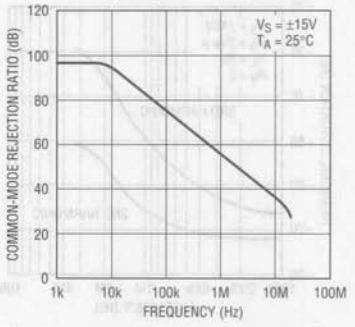
Frequency Response vs Capacitive Load



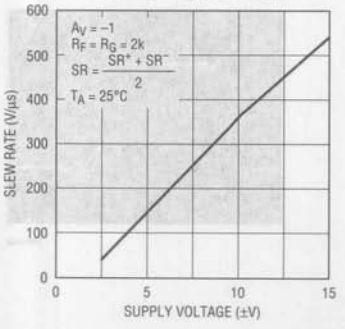
Power Supply Rejection Ratio vs Frequency



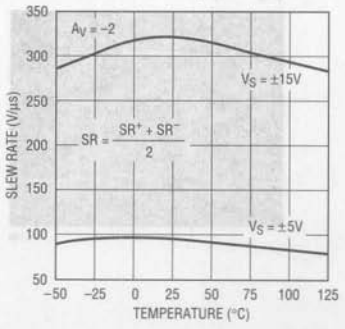
Common-Mode Rejection Ratio vs Frequency



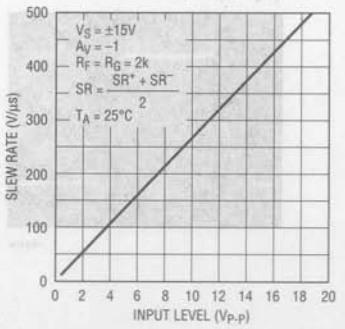
Slew Rate vs Supply Voltage



Slew Rate vs Temperature



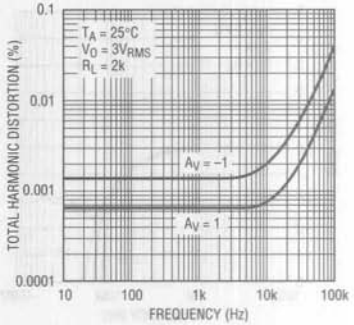
Slew Rate vs Input Level



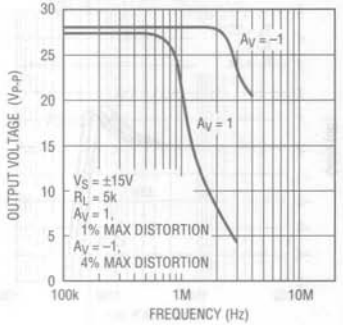
2

TYPICAL PERFORMANCE CHARACTERISTICS

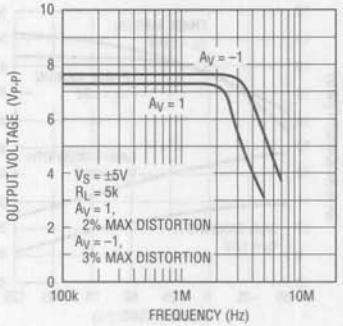
Total Harmonic Distortion vs Frequency



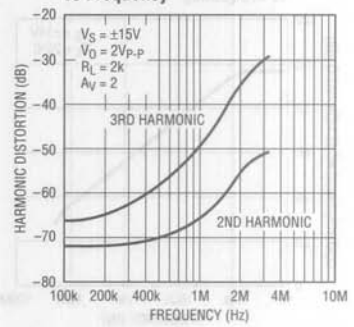
Undistorted Output Swing vs Frequency (±15V)



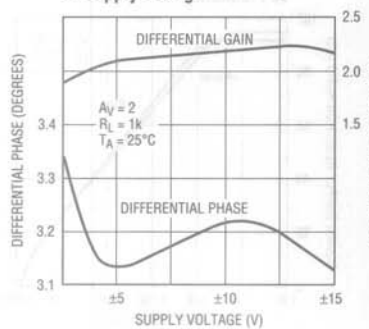
Undistorted Output Swing vs Frequency (±5V)



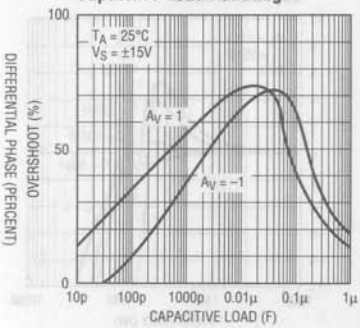
2nd and 3rd Harmonic Distortion vs Frequency



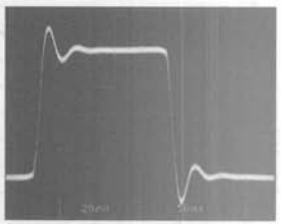
Differential Gain and Phase vs Supply Voltage



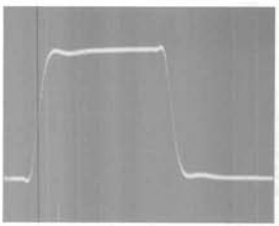
Capacitive Load Handling



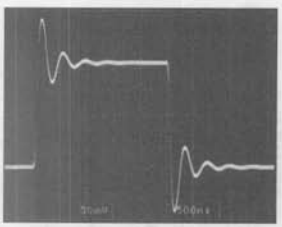
Small-Signal Transient (A_V = 1)



Small-Signal Transient (A_V = –1)

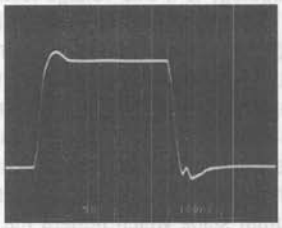


Small-Signal Transient (A_V = –1, C_L = 1000pF)

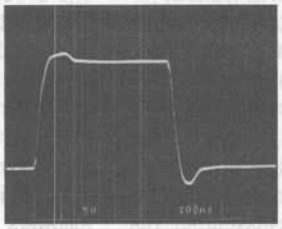


TYPICAL PERFORMANCE CHARACTERISTICS

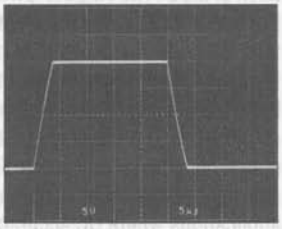
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



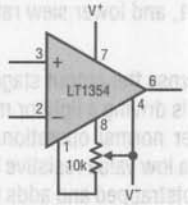
Large-Signal Transient ($A_V = 1$, $C_L = 10{,}000pF$)



APPLICATIONS INFORMATION

The LT1354 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1354 is shown below.

Offset Nulling



Layout and Passive Components

The LT1354 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1354 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 1000pF load shows 43% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited to 5V/µs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1354 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Power Dissipation

The LT1354 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1354CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1354CS8: $T_J = T_A + (P_D \times 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1354CS8 at 70°C, $V_S = \pm 15V$, $R_L = 100\Omega$ (Note: the minimum short-circuit current at 70°C is 24mA, so the output swing is guaranteed only to 2.4V with 100Ω.)

$$P_{DMAX} = (30V)(1.45mA) + (15V-2.4V)(24mA) = 346mW$$

$$T_{JMAX} = 70°C + (346mW)(190°C/W) = 136°C$$

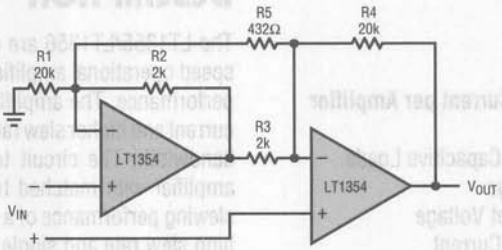
Circuit Operation

The LT1354 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive an 800Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1354 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

TYPICAL APPLICATIONS

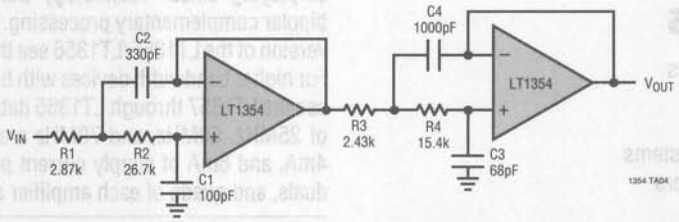
Instrumentation Amplifier



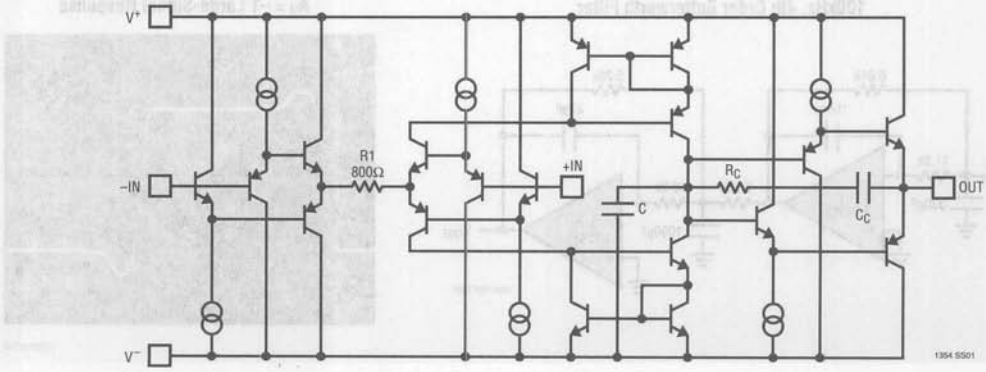
$$A_V = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 120kHz

100kHz, 4th Order Butterworth Filter (Sallen-Key)



SIMPLIFIED SCHEMATIC



Dual and Quad 12MHz, 400V/µs Op Amps

FEATURES

- **12MHz Gain-Bandwidth**
- **400V/µs Slew Rate**
- **1.25mA Maximum Supply Current per Amplifier**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 10nV/√Hz Input Noise Voltage
- 800µV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 70nA Maximum Input Offset Current
- 12V/mV Minimum DC Gain, R_L=1k
- 230ns Settling Time to 0.1%, 10V Step
- 280ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

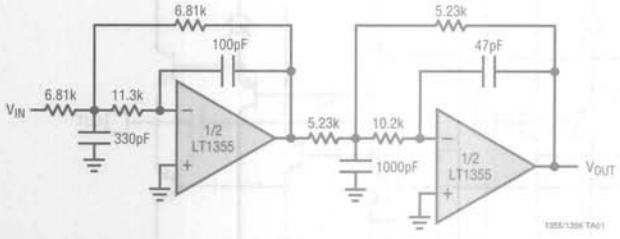
The LT1355/LT1356 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

The LT1355/LT1356 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1355/LT1356 see the LT1354 data sheet. For higher bandwidth devices with higher supply currents see the LT1357 through LT1365 data sheets. Bandwidths of 25MHz, 50MHz, and 70MHz are available with 2mA, 4mA, and 6mA of supply current per amplifier. Singles, duals, and quads of each amplifier are available.

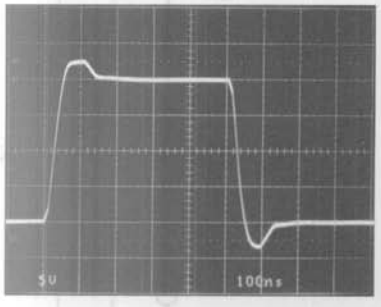
C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



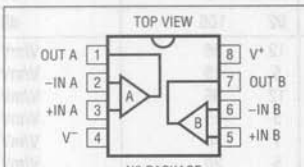
A_V = –1 Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

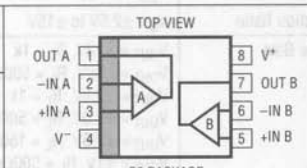
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



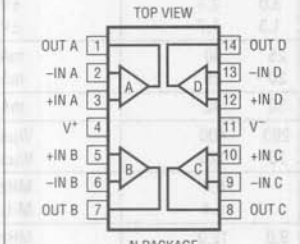
N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1355CN8



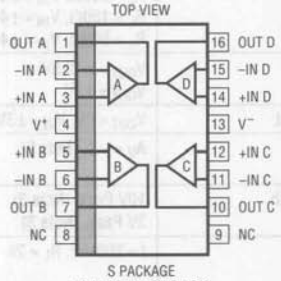
S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1355CS8
S8 PART MARKING
1355



N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1356CN



S PACKAGE
16-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1356CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.3	0.8	mV
			±5V		0.3	0.8	mV
			±2.5V		0.4	1.0	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		20	70	nA
I_B	Input Bias Current		±2.5V to ±15V		80	300	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		10		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.6		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	70	160		MΩ
	Input Resistance	Differential	±15V		11		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range +		±15V	12.0	13.4		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.1		V
	Input Voltage Range −		±15V		−13.2	−12.0	V
			±5V		−3.4	−2.5	V
			±2.5V		−0.9	−0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	83	97		dB
		V_{CM} = ±2.5V	±5V	78	84		dB
		V_{CM} = ±0.5V	±2.5V	68	75		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	12	36		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	5	15		V/mV
		V_{OUT} = ±2.5V, R_L = 1k	±5V	12	36		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	5	15		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1	4		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	5	20		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.3	13.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	12.5	13.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.0	3.3		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	V_{OUT} = ±12.5V	±15V	25	30		mA
		V_{OUT} = ±3V	±5V	20	25		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	30	42		mA
SR	Slew Rate	A_V = −2, (Note 2)	±15V	200	400		V/µs
			±5V	70	120		V/µs
	Full Power Bandwidth	10V Peak, (Note 3)	±15V		6.4		MHz
		3V Peak, (Note 3)	±5V		6.4		MHz
GBW	Gain-Bandwidth	f = 200kHz, R_L = 2k	±15V	9.0	12.0		MHz
			±5V	7.5	10.5		MHz
			±2.5V		9.0		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10%-90%, 0.1V	±15V		14		ns
			±5V		17		ns
	Overshoot	A_V = 1, 0.1V	±15V		20		%
			±5V		18		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		16		ns
			±5V		19		ns
t_s	Settling Time	10V Step, 0.1%, A_V = −1	±15V		230		ns
		10V Step, 0.01%, A_V = −1	±15V		280		ns
		5V Step, 0.1%, A_V = −1	±5V		240		ns
		5V Step, 0.01%, A_V = −1	±5V		380		ns
	Differential Gain	f = 3.58MHz, A_V = 2, R_L = 1k	±15V		2.2		%
			±5V		2.1		%
	Differential Phase	f = 3.58MHz, A_V = 2, R_L = 1k	±15V		3.1		Deg
			±5V		3.1		Deg
R_O	Output Resistance	A_V = 1, f = 100kHz	±15V		0.7		Ω
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		1.0	1.25	mA
		Each Amplifier	±5V		0.9	1.20	mA

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.0	mV
			±5V	●			1.0	mV
			±2.5V	●			1.2	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			100	nA
I_B	Input Bias Current		±2.5V to ±15V	●			450	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	81			dB
		$V_{CM} = ±2.5V$	±5V	●	77			dB
		$V_{CM} = ±0.5V$	±2.5V	●	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$	±15V	●	10.0			V/mV
		$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	3.3			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 1k$	±5V	●	10.0			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 500Ω$	±5V	●	3.3			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 150Ω$	±5V	●	0.6			V/mV
		$V_{OUT} = ±1V$, $R_L = 500Ω$	±2.5V	●	3.3			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$	±15V	●	13.2			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±15V	●	12.0			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±5V	●	3.4			±V
		$R_L = 150Ω$, $V_{IN} = ±40mV$	±5V	●	2.8			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = ±12V$	±15V	●	24.0			mA
		$V_{OUT} = ±2.8V$	±5V	●	18.7			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	150			V/µs
			±5V	●	60			V/µs
GBW	Gain-Bandwidth	f = 200kHz, $R_L = 2k$	±15V	●	7.5			MHz
			±5V	●	6.0			MHz
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			1.45	mA
		Each Amplifier	±5V	●			1.40	mA

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.5	mV
			±5V	●			1.5	mV
			±2.5V	●			1.7	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			200	nA
I_B	Input Bias Current		±2.5V to ±15V	●			550	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	80			dB
		$V_{CM} = ±2.5V$	±5V	●	76			dB
		$V_{CM} = ±0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	90			dB

2

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	7.0			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	1.7			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	●	7.0			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	1.7			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.4			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	1.7			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	11.5			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	2.6			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm11.5V$	±15V	●	23.0			mA
		$V_{OUT} = \pm2.6V$	±5V	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	23			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	120			V/µs
			±5V	●	50			V/µs
GBW	Gain-Bandwidth	f = 200kHz, $R_L = 2k$	±15V	●	7.0			MHz
			±5V	●	5.5			MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			1.50	mA
		Each Amplifier	±5V	●			1.45	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

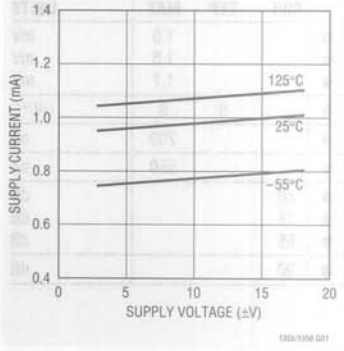
Note 3: Full power bandwidth is calculated from the slew rate measurement: $FPBW = (SR)/2\pi V_P$.

Note 4: This parameter is not 100% tested.

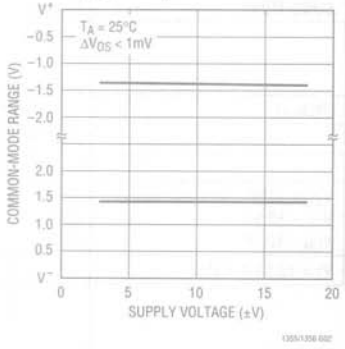
Note 5: The LT1355/LT1356 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

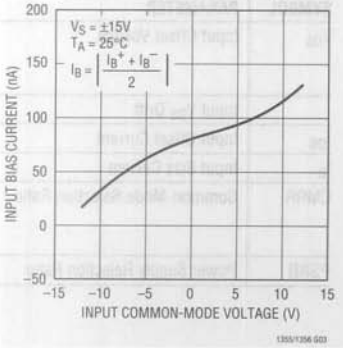
Supply Current vs Supply Voltage and Temperature



Input Common-Mode Range vs Supply Voltage



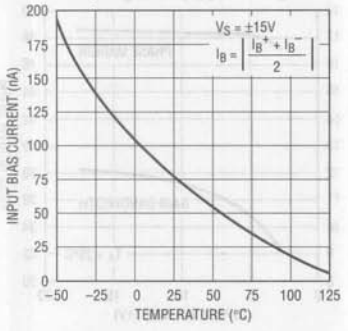
Input Bias Current vs Input Common-Mode Voltage



LINEAR TECHNOLOGY

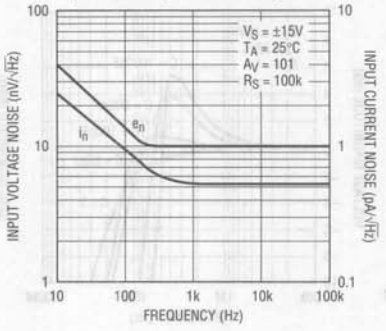
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



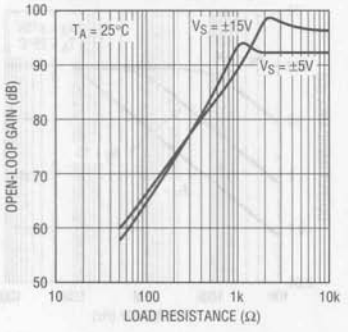
1355/1356 G04

Input Noise Spectral Density



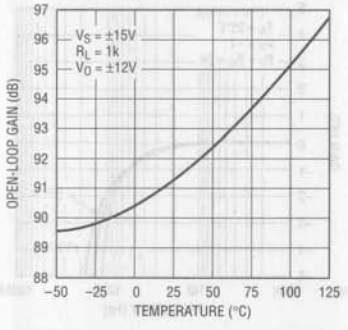
1355/1356 G05

Open-Loop Gain vs Resistive Load



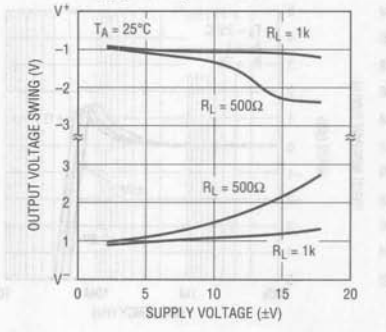
1355/1356 G06

Open-Loop Gain vs Temperature



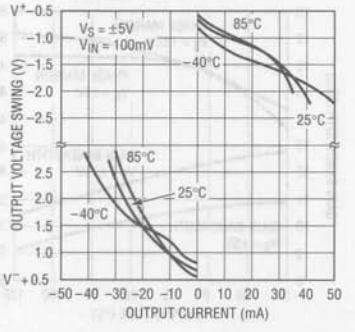
1355/1356 G07

Output Voltage Swing vs Supply Voltage



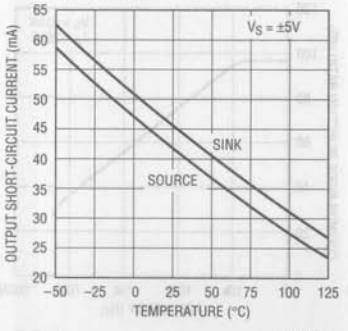
1355/1356 G09

Output Voltage Swing vs Load Current



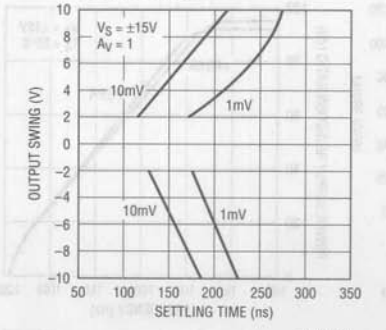
1355/1356 G09

Output Short-Circuit Current vs Temperature



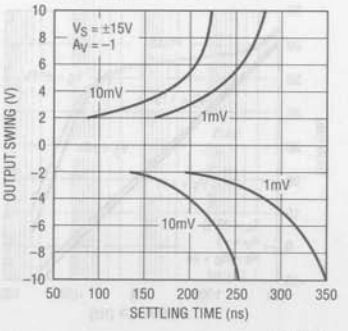
1355/1356 G10

Settling Time vs Output Step (Noninverting)



1355/1356 G11

Settling Time vs Output Step (Inverting)

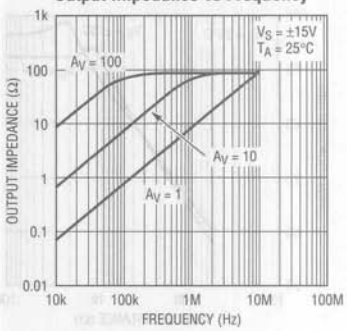


1355/1356 G12

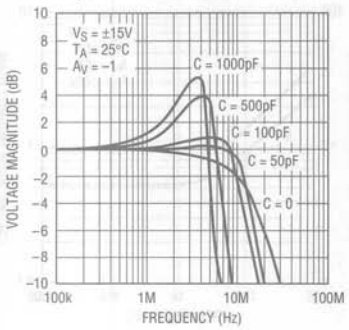
2

TYPICAL PERFORMANCE CHARACTERISTICS

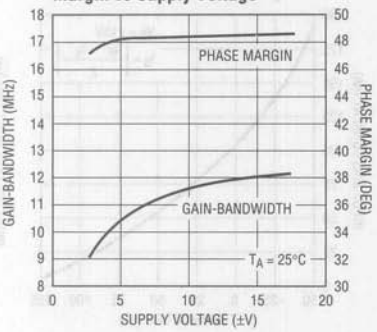
Output Impedance vs Frequency



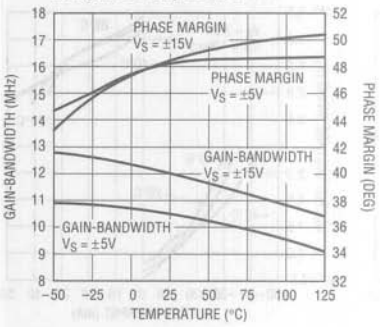
Frequency Response vs Capacitive Load



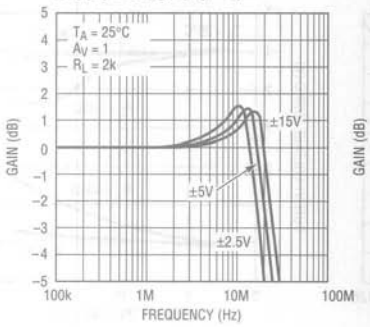
Gain-Bandwidth and Phase Margin vs Supply Voltage



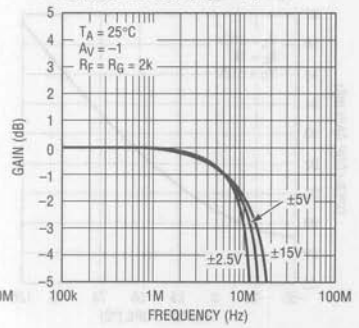
Gain-Bandwidth and Phase Margin vs Temperature



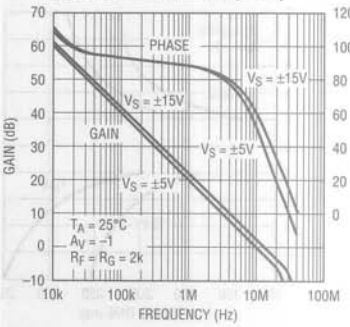
Frequency Response vs Supply Voltage (A_V = 1)



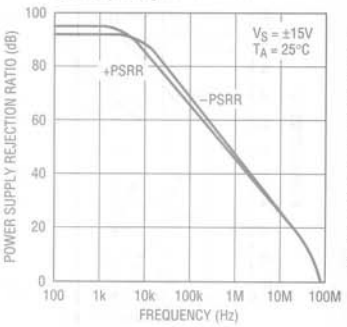
Frequency Response vs Supply Voltage (A_V = –1)



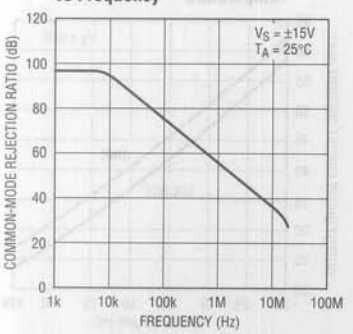
Gain and Phase vs Frequency



Power Supply Rejection Ratio vs Frequency

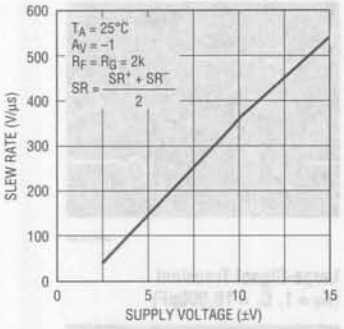


Common-Mode Rejection Ratio vs Frequency

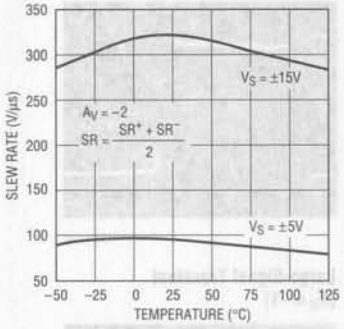


TYPICAL PERFORMANCE CHARACTERISTICS

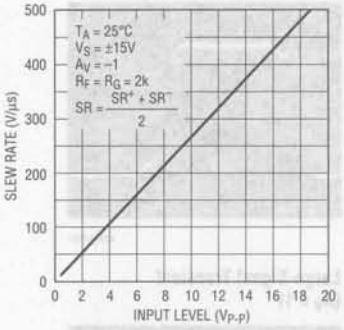
Slew Rate vs Supply Voltage



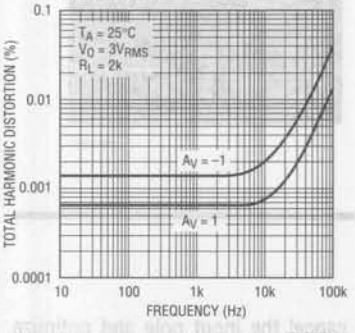
Slew Rate vs Temperature



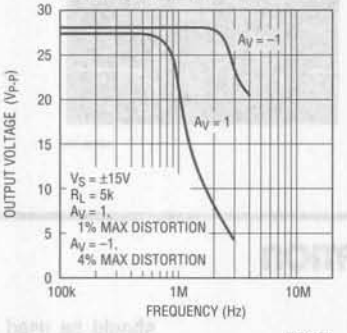
Slew Rate vs Input Level



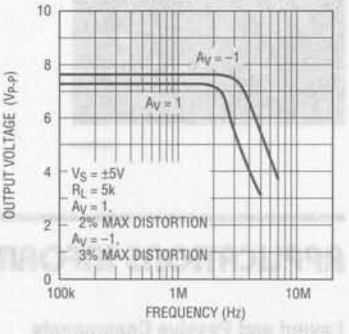
Total Harmonic Distortion vs Frequency



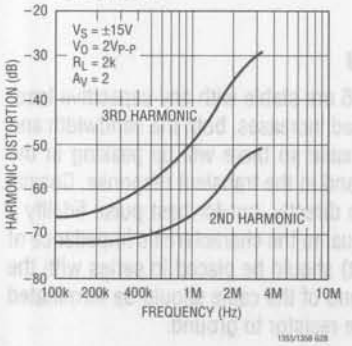
Undistorted Output Swing vs Frequency (±15V)



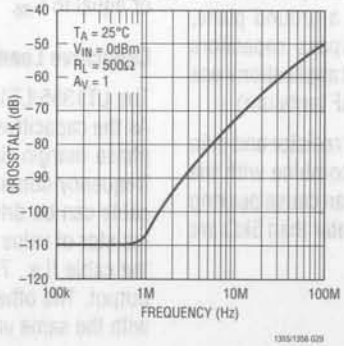
Undistorted Output Swing vs Frequency (±5V)



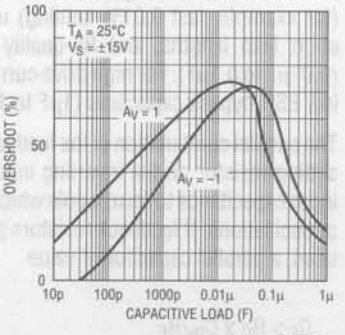
2nd and 3rd Harmonic Distortion vs Frequency



Crosstalk vs Frequency



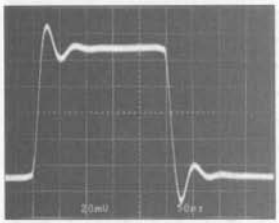
Capacitive Load Handling



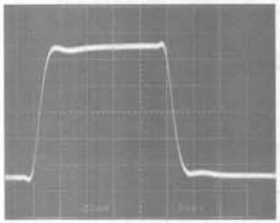
2

TYPICAL PERFORMANCE CHARACTERISTICS

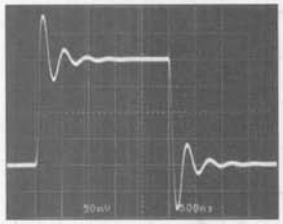
Small-Signal Transient ($A_V = 1$)



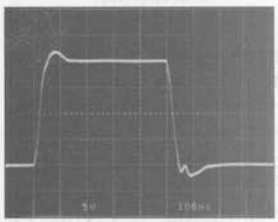
Small-Signal Transient ($A_V = -1$)



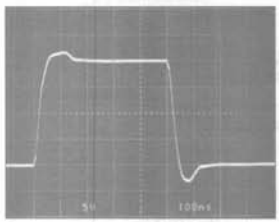
Small- Signal Transient ($A_V = -1$, $C_L = 1000pF$)



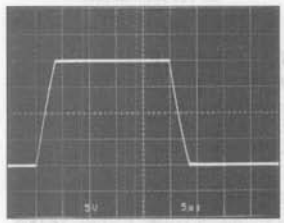
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



Large-Signal Transient ($A_V = 1$, $C_L = 10,000pF$)



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1355/LT1356 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1355/LT1356 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1355/LT1356 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Circuit Operation

The LT1355/LT1356 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive an 800Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1355/LT1356 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

2

Power Dissipation

The LT1355/LT1356 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1355CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1355CS8: $T_J = T_A + (P_D \times 190°C/W)$
LT1356CN: $T_J = T_A + (P_D \times 110°C/W)$
LT1356CS: $T_J = T_A + (P_D \times 150°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

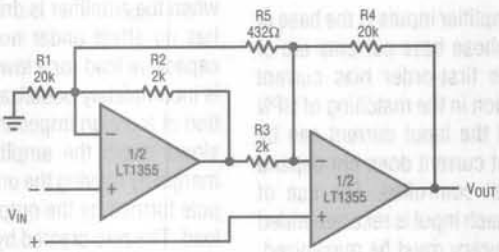
Example: LT1356 in S16 at 70°C, $V_S = \pm 15V$, $R_L = 1k$

$$P_{DMAX} = (30V)(1.45mA) + (7.5V)^2/1kW = 99.8mW$$

$$T_{JMAX} = 70°C + (4 \times 99.8mW)(150°C/W) = 130°C$$

TYPICAL APPLICATIONS

Instrumentation Amplifier

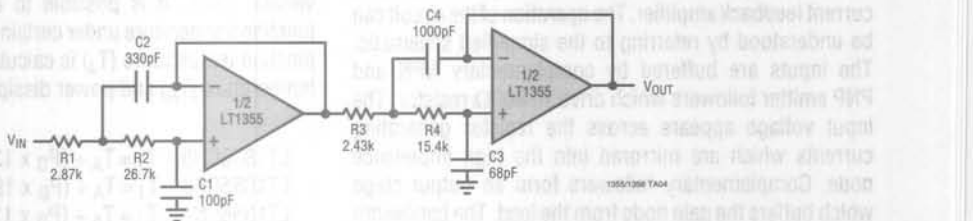


$$A_V = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 120kHz

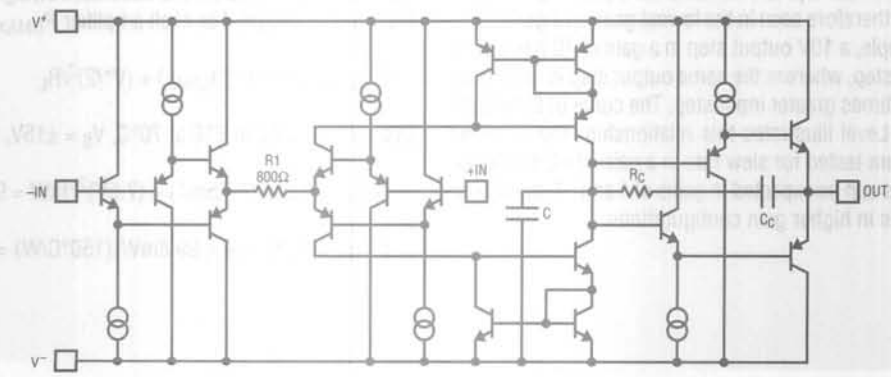
1355/1356 TA03

100kHz, 4th Order Butterworth Filter (Sallen-Key)



1355/1356 TA04

SIMPLIFIED SCHEMATIC



1355/1356 SS01

LINEAR TECHNOLOGY

25MHz, 600V/µs Op Amp

FEATURES

- **25MHz Gain-Bandwidth**
- **600V/µs Slew Rate**
- **2.5mA Maximum Supply Current**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/√Hz Input Noise Voltage
- 600µV Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, R_L=1k
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

The LT1357 is a high speed, very high slew rate operational amplifier with outstanding AC and DC performance. The LT1357 has much lower supply current, lower input offset voltage, lower input bias current, and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

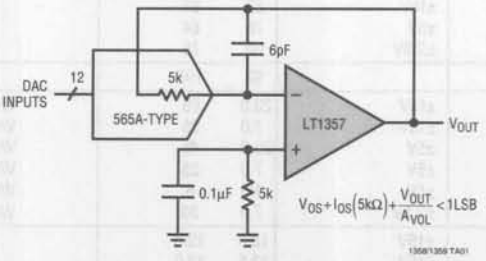
The LT1357 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1357 see the LT1358/LT1359 data sheet. For higher bandwidth devices with higher supply current see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

C-Load is a trademark of Linear Technology Corporation

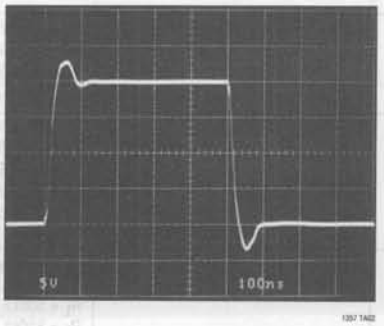
2

TYPICAL APPLICATION

DAC I-to-V Converter



A_V = –1 Large-Signal Response



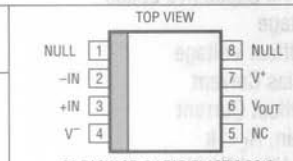
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

N8 PACKAGE, 8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1357CN8



S8 PACKAGE, 8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1357CS8
S8 PART MARKING
1357

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.2	0.6	mV
			±5V		0.2	0.6	mV
			±2.5V		0.3	0.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		40	120	nA
I_B	Input Bias Current		±2.5V to ±15V		120	500	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		8		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.8		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	35	80		MΩ
		Differential	±15V		6		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range $^+$		±15V	12.0	13.4		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.1		V
	Input Voltage Range $^-$		±15V		–13.2	–12.0	V
			±5V		–3.3	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	83	97		dB
		V_{CM} = ±2.5V	±5V	78	84		dB
		V_{CM} = ±0.5V	±2.5V	68	75		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	20.0	65		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	7.0	25		V/mV
		V_{OUT} = ±2.5V, R_L = 1k	±5V	20.0	45		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	7.0	25		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1.5	6		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	7.0	30		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.3	13.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	12.5	13.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.0	3.3		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = \pm12.5V$	±15V	25	30		mA
		$V_{OUT} = \pm3V$	±5V	20	25		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	30	42		mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	300	600		V/µs
			±5V	150	220		V/µs
	Full Power Bandwidth	10V Peak, (Note 3)	±15V		9.6		MHz
		3V Peak, (Note 3)	±5V		11.7		MHz
GBW	Gain-Bandwidth	f = 200kHz, R_L = 2k	±15V	18	25		MHz
			±5V	15	22		MHz
			±2.5V		20		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V		8		ns
			±5V		9		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		27		%
			±5V		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		9		ns
			±5V		11		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V		115		ns
		10V Step, 0.01%, $A_V = -1$	±15V		220		ns
		5V Step, 0.1%, $A_V = -1$	±5V		110		ns
		5V Step, 0.01%, $A_V = -1$	±5V		380		ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, R_L = 1k	±15V		0.1		%
			±5V		0.1		%
	Differential Phase	f = 3.58MHz, $A_V = 2$, R_L = 1k	±15V		0.50		Deg
			±5V		0.35		Deg
R_O	Output Resistance	$A_V = 1$, f = 100kHz	±15V		0.3		Ω
I_S	Supply Current		±15V		2.0	2.5	mA
			±5V		1.9	2.4	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			0.8	mV
			±5V	●			0.8	mV
			±2.5V	●			1.0	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			180	nA
I_B	Input Bias Current		±2.5V to ±15V	●			750	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	81			dB
		$V_{CM} = \pm2.5V$	±5V	●	77			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, R_L = 1k	±15V	●	15			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	5			V/mV
		$V_{OUT} = \pm2.5V$, R_L = 1k	±5V	●	15			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	1			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	5			V/mV

2

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	±15V	●	13.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	12.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	2.8			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.2V$	±15V	●	24.4			mA
		$V_{OUT} = \pm 2.8V$	±5V	●	18.7			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	25			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	225			V/µs
			±5V	●	125			V/µs
GBW	Gain-Bandwidth	$f = 200kHz, R_L = 2k$	±15V	●	15			MHz
			±5V	●	12			MHz
I_S	Supply Current		±15V	●			2.9	mA
			±5V	●			2.8	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.3	mV
			±5V	●			1.3	mV
			±2.5V	●			1.5	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			300	nA
I_B	Input Bias Current		±2.5V to ±15V	●			900	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$	±15V	●	80			dB
		$V_{CM} = \pm 2.5V$	±5V	●	76			dB
		$V_{CM} = \pm 0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L = 1k$	±15V	●	10.0			V/mV
		$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 1k$	±5V	●	10.0			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	±5V	●	2.5			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm 1V$, $R_L = 500\Omega$	±2.5V	●	2.5			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	2.6			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12V$	±15V	●	24.0			mA
		$V_{OUT} = \pm 2.6V$	±5V	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	180			V/µs
			±5V	●	100			V/µs

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
GBW	Gain-Bandwith	f = 200kHz, R_L = 2k	±15V	●	14			MHz
			±5V	●	11			MHz
I_S	Supply Current		±15V	●			3.0	mA
			±5V	●			2.9	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 3: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

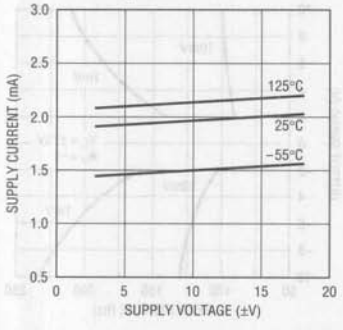
Note 4: This parameter is not 100% tested.

Note 5: The LT1357 is not tested and is not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

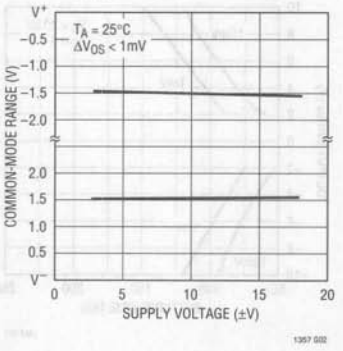
TYPICAL PERFORMANCE CHARACTERISTICS

2

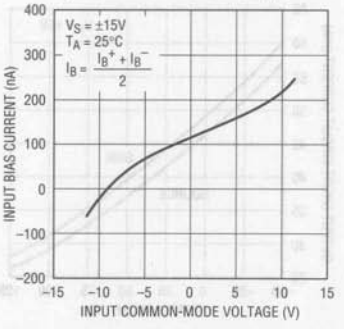
Supply Current vs Supply Voltage and Temperature



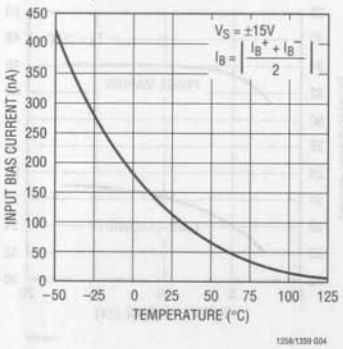
Input Common-Mode Range vs Supply Voltage



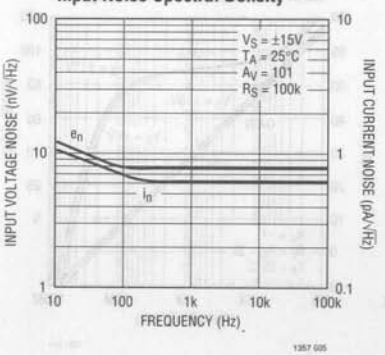
Input Bias Current vs Input Common-Mode Voltage



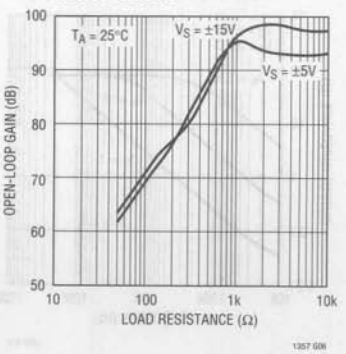
Input Bias Current vs Temperature



Input Noise Spectral Density

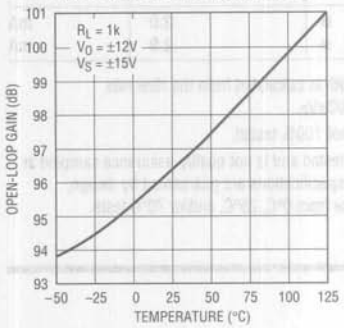


Open-Loop Gain vs Resistive Load

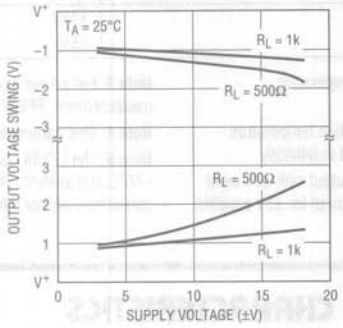


TYPICAL PERFORMANCE CHARACTERISTICS

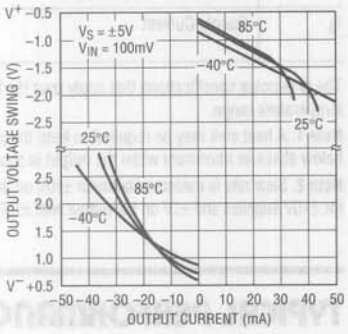
Open-Loop Gain vs Temperature



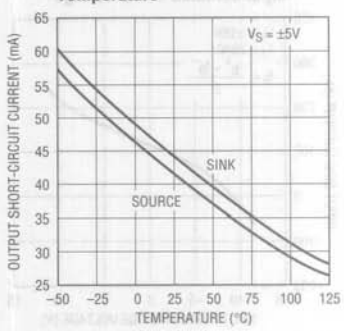
Output Voltage Swing vs Supply Voltage



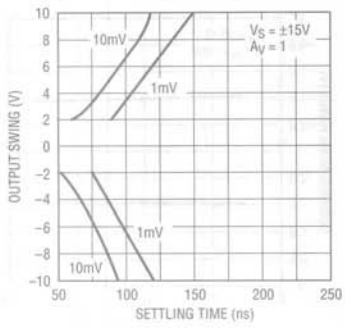
Output Voltage Swing vs Load Current



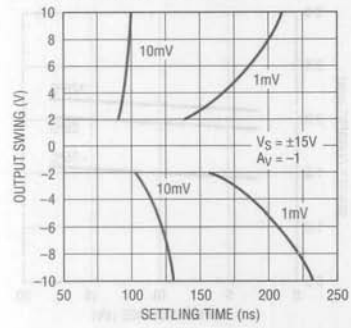
Output Short-Circuit Current vs Temperature



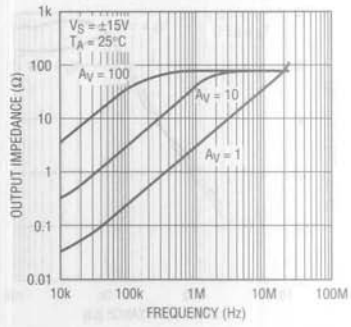
Settling Time vs Output Step (Noninverting)



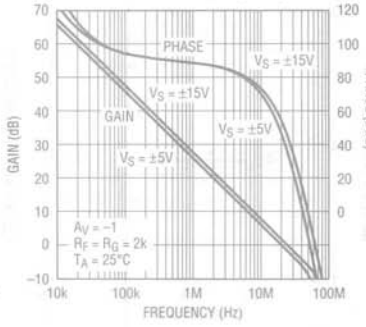
Settling Time vs Output Step (Inverting)



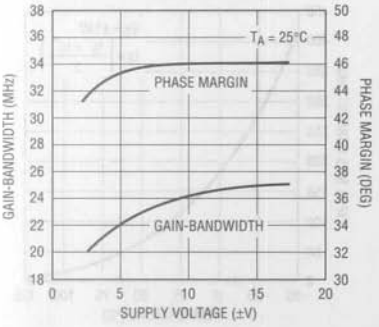
Output Impedance vs Frequency



Gain and Phase vs Frequency

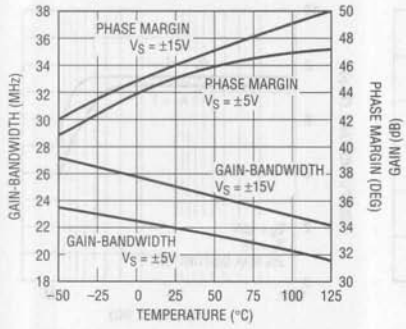


Gain-Bandwidth and Phase Margin vs Supply Voltage

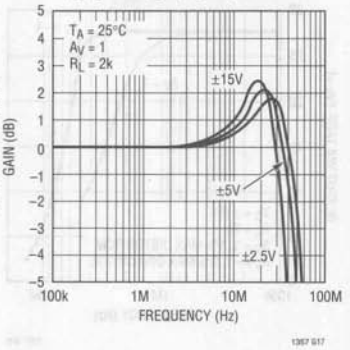


TYPICAL PERFORMANCE CHARACTERISTICS

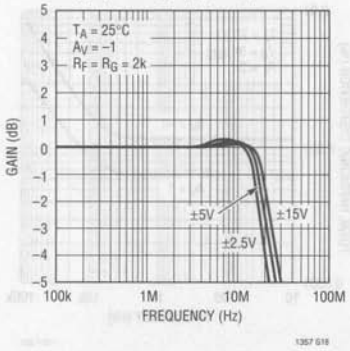
Gain-Bandwidth and Phase Margin vs Temperature



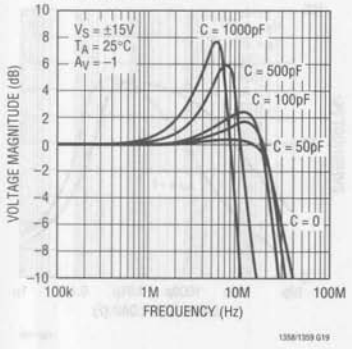
Frequency Response vs Supply Voltage (A_V = 1)



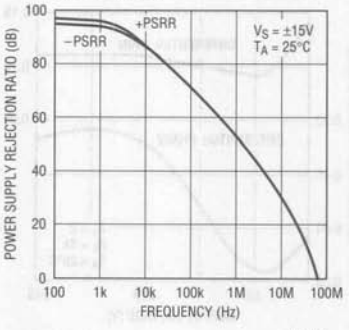
Frequency Response vs Supply Voltage (A_V = –1)



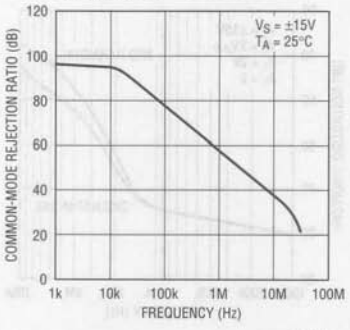
Frequency Response vs Capacitive Load



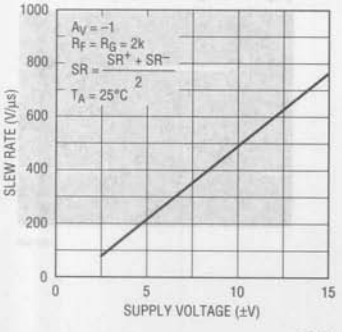
Power Supply Rejection Ratio vs Frequency



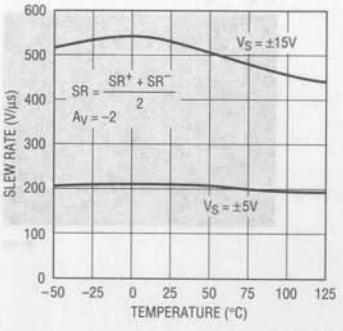
Common-Mode Rejection Ratio vs Frequency



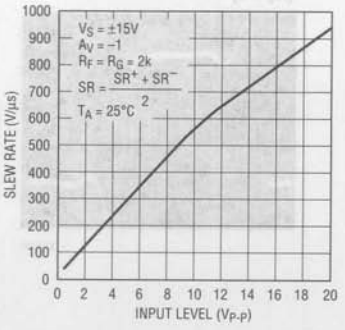
Slew Rate vs Supply Voltage



Slew Rate vs Temperature



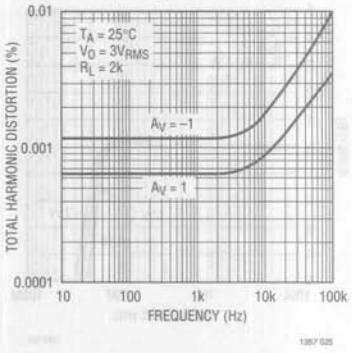
Slew Rate vs Input Level



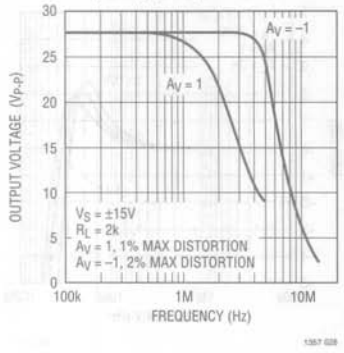
2

TYPICAL PERFORMANCE CHARACTERISTICS

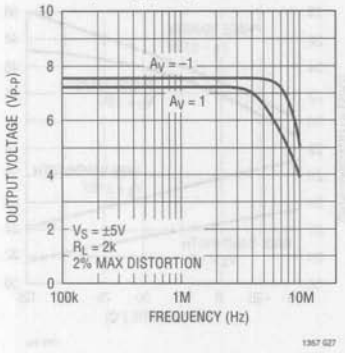
Total Harmonic Distortion vs Frequency



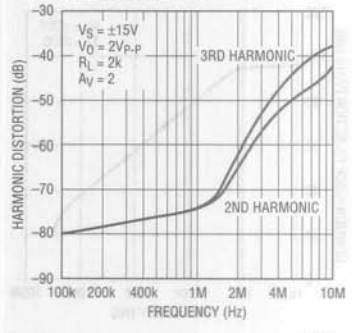
Undistorted Output Swing vs Frequency (±15V)



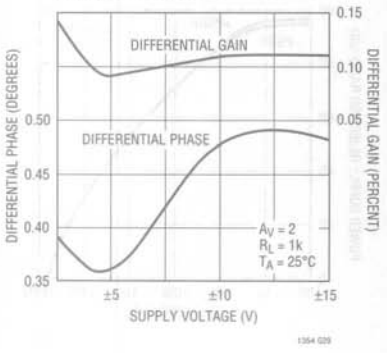
Undistorted Output Swing vs Frequency (±5V)



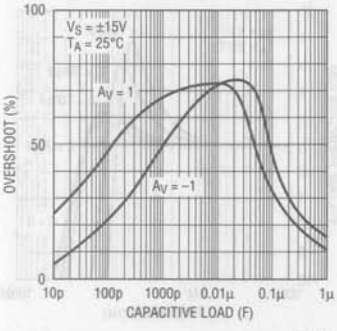
2nd and 3rd Harmonic Distortion vs Frequency



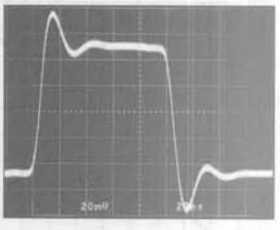
Differential Gain and Phase vs Supply Voltage



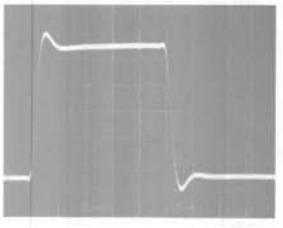
Capacitive Load Handling



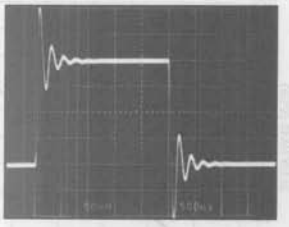
Small-Signal Transient (A_V = 1)



Small-Signal Transient (A_V = –1)

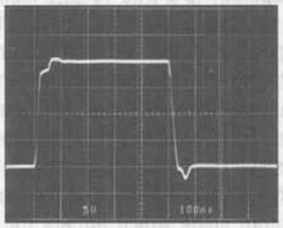


Small-Signal Transient (A_V = –1, C_L = 1000pF)

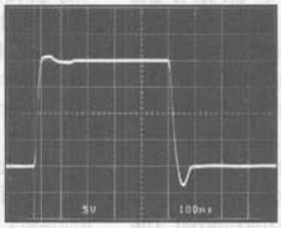


TYPICAL PERFORMANCE CHARACTERISTICS

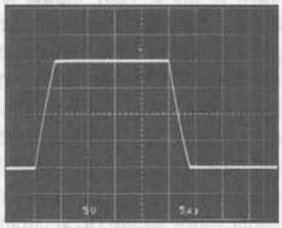
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



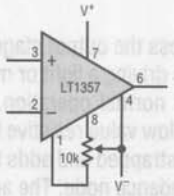
Large-Signal Transient ($A_V = 1$, $C_L = 10{,}000pF$)



APPLICATIONS INFORMATION

The LT1357 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1357 is shown below.

Offset Nulling



Layout and Passive Components

The LT1357 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1357 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 1000pF load shows 50% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited to 5V/µs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1357 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Power Dissipation

The LT1357 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1357CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1357CS8: $T_J = T_A + (P_D \times 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1357CS8 at 70°C, $V_S = \pm 15V$, $R_L = 120\Omega$ (Note: the minimum short-circuit current at 70°C is 25mA, so the output swing is guaranteed only to 3V with 120Ω.)

$$P_{DMAX} = (30V)(2.9mA) + (15V-3V)(25mA) = 387mW$$

$$T_{JMAX} = 70°C + (387mW)(190°C/W) = 144°C$$

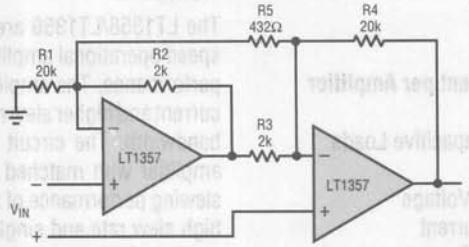
Circuit Operation

The LT1357 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1357 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

TYPICAL APPLICATIONS

Instrumentation Amplifier

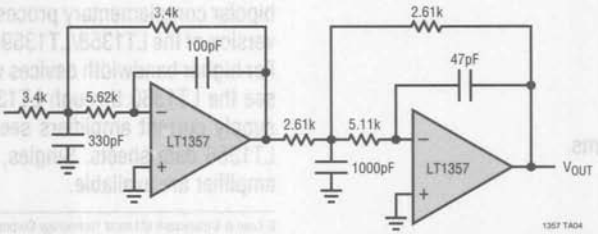


$$A_V = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 250kHz

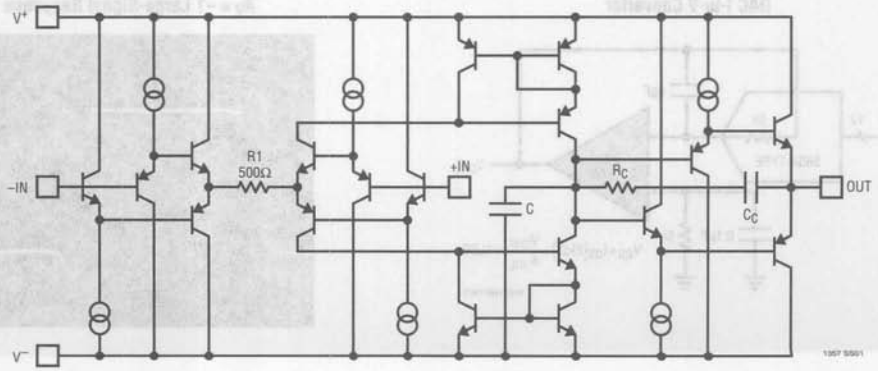
1357 TA03

200kHz, 4th Order Butterworth Filter



1357 TA04

SIMPLIFIED SCHEMATIC



1357 SS01

Dual and Quad 25MHz, 600V/µs Op Amps

FEATURES

- **25MHz Gain-Bandwidth**
- **600V/µs Slew Rate**
- **2.5mA Maximum Supply Current per Amplifier**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/√Hz Input Noise Voltage
- 600µV Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, R_L=1k
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

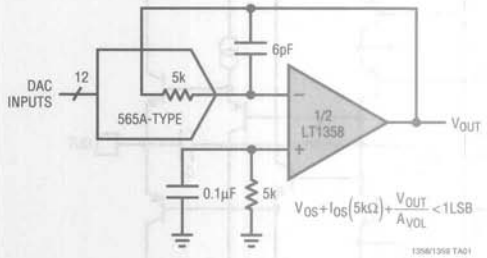
The LT1358/LT1359 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

The LT1358/LT1359 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1358/LT1359 see the LT1357 data sheet. For higher bandwidth devices with higher supply currents see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

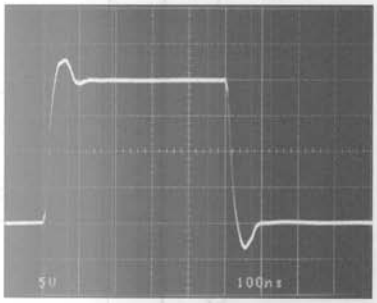
C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

DAC I-to-V Converter



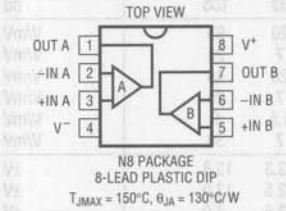
A_V = –1 Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

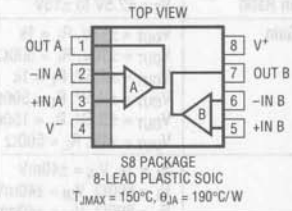
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



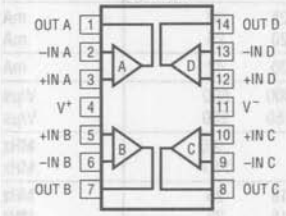
N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1358CN8



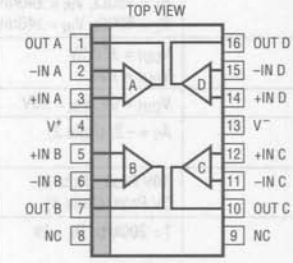
S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER	S8 PART MARKING
LT1358CS8	1358



N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1359CN



S PACKAGE
16-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1359CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.2	0.6	mV
			±5V		0.2	0.6	mV
			±2.5V		0.3	0.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		40	120	nA
I_B	Input Bias Current		±2.5V to ±15V		120	500	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		8		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.8		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	35	80		MΩ
	Input Resistance	Differential	±15V		6		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range$^+$		±15V	12.0	13.4		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.1		V
	Input Voltage Range$^-$		±15V		−13.2	−12.0	V
			±5V		−3.3	−2.5	V
			±2.5V		−0.9	−0.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	83	97		dB
		$V_{CM} = ±2.5V$	±5V	78	84		dB
		$V_{CM} = ±0.5V$	±2.5V	68	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$	±15V	20	65		V/mV
		$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	7	25		V/mV
		$V_{OUT} = ±2.5V$, $R_L = 1k$	±5V	20	45		V/mV
		$V_{OUT} = ±2.5V$, $R_L = 500Ω$	±5V	7	25		V/mV
		$V_{OUT} = ±2.5V$, $R_L = 150Ω$	±5V	1.5	6		V/mV
		$V_{OUT} = ±1V$, $R_L = 500Ω$	±2.5V	7	30		V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$	±15V	13.3	13.8		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±15V	12.5	13.0		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±5V	3.5	4.0		±V
		$R_L = 150Ω$, $V_{IN} = ±40mV$	±5V	3.0	3.3		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	$V_{OUT} = ±12.5V$	±15V	25	30		mA
		$V_{OUT} = ±3V$	±5V	20	25		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	30	42		mA
SR	Slew Rate	$A_V = −2$, (Note 2)	±15V	300	600		V/µs
			±5V	150	220		V/µs
	Full Power Bandwidth	10V Peak, (Note 3)	±15V		9.6		MHz
		3V Peak, (Note 3)	±5V		11.7		MHz
GBW	Gain-Bandwidth	$f = 200kHz$, $R_L = 2k$	±15V	18	25		MHz
			±5V	15	22		MHz
			±2.5V		20		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V		8		ns
			±5V		9		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		27		%
			±5V		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		9		ns
			±5V		11		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = −1$	±15V		115		ns
		10V Step, 0.01%, $A_V = −1$	±15V		220		ns
		5V Step, 0.1%, $A_V = −1$	±5V		110		ns
		5V Step, 0.01%, $A_V = −1$	±5V		380		ns
	Differential Gain	$f = 3.58MHz$, $A_V = 2$, $R_L = 1k$	±15V		0.1		%
			±5V		0.1		%
	Differential Phase	$f = 3.58MHz$, $A_V = 2$, $R_L = 1k$	±15V		0.50		Deg
			±5V		0.35		Deg
R_O	Output Resistance	$A_V = 1$, $f = 100kHz$	±15V		0.3		Ω
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		2.0	2.5	mA
		Each Amplifier	±5V		1.9	2.4	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			0.8	mV
			±5V	●			0.8	mV
			±2.5V	●			1.0	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			180	nA
I_B	Input Bias Current		±2.5V to ±15V	●			750	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	81			dB
		$V_{CM} = ±2.5V$	±5V	●	77			dB
		$V_{CM} = ±0.5V$	±2.5V	●	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$	±15V	●	15			V/mV
		$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	5			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 1k$	±5V	●	15			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 500Ω$	±5V	●	5			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 150Ω$	±5V	●	1			V/mV
		$V_{OUT} = ±1V$, $R_L = 500Ω$	±2.5V	●	5			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$	±15V	●	13.2			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±15V	●	12.2			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±5V	●	3.4			±V
		$R_L = 150Ω$, $V_{IN} = ±40mV$	±5V	●	2.8			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = ±12.2V$	±15V	●	24.4			mA
		$V_{OUT} = ±2.8V$	±5V	●	18.7			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	●	25			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	225			V/µs
			±5V	●	125			V/µs
GBW	Gain-Bandwidth	f = 200kHz, $R_L = 2k$	±15V	●	15			MHz
			±5V	●	12			MHz
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			2.9	mA
		Each Amplifier	±5V	●			2.8	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.3	mV
			±5V	●			1.3	mV
			±2.5V	●			1.5	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			300	nA
I_B	Input Bias Current		±2.5V to ±15V	●			900	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	80			dB
		$V_{CM} = ±2.5V$	±5V	●	76			dB
		$V_{CM} = ±0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	90			dB

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	10.0			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	●	10.0			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	2.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	2.5			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	2.6			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	±15V	●	24.0			mA
		$V_{OUT} = \pm2.6V$	±5V	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	±15V	●	180			V/µs
			±5V	●	100			V/µs
GBW	Gain-Bandwidth	f = 200kHz, $R_L = 2k$	±15V	●	14			MHz
			±5V	●	11			MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			3.0	mA
		Each Amplifier	±5V	●			2.9	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

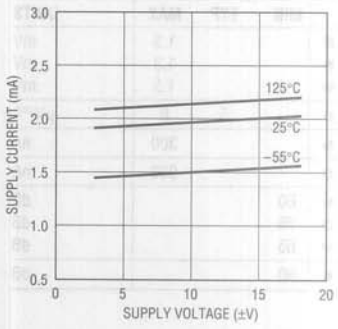
Note 3: Full power bandwidth is calculated from the slew rate measurement: $FPBW = (SR)/2\pi V_P$.

Note 4: This parameter is not 100% tested.

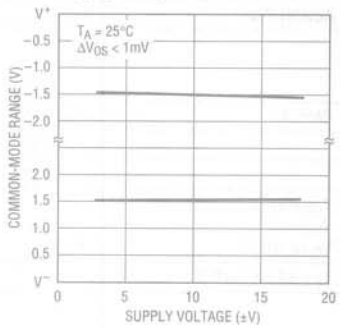
Note 5: The LT1358/LT1359 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

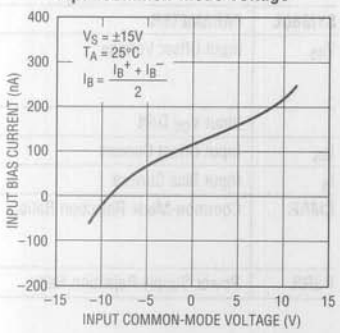
Supply Current vs Supply Voltage and Temperature



Input Common-Mode Range vs Supply Voltage



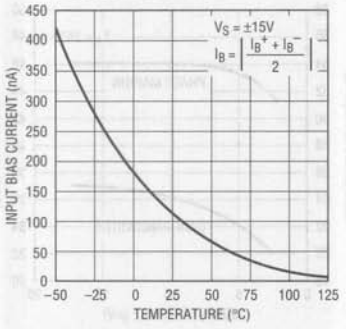
Input Bias Current vs Input Common-Mode Voltage



LINEAR TECHNOLOGY

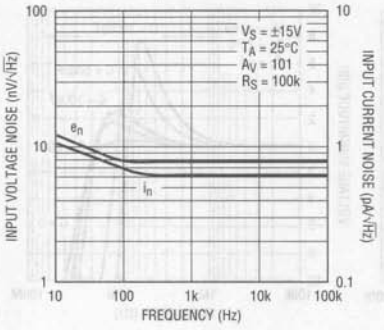
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



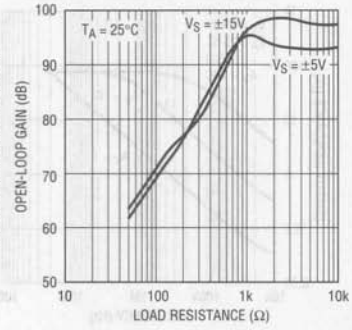
1358/1359 G04

Input Noise Spectral Density



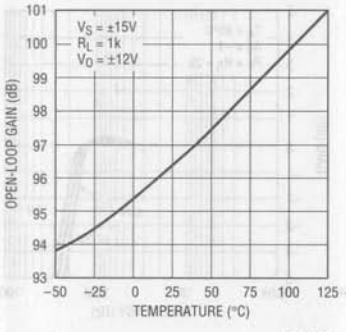
1358/1359 G05

Open-Loop Gain vs Resistive Load



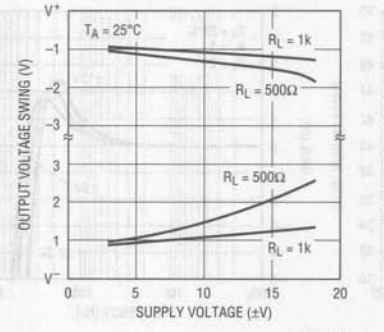
1358/1359 G06

Open-Loop Gain vs Temperature



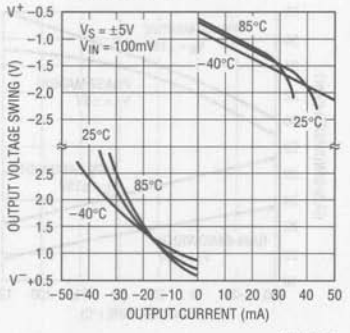
1358/1359 G07

Output Voltage Swing vs Supply Voltage



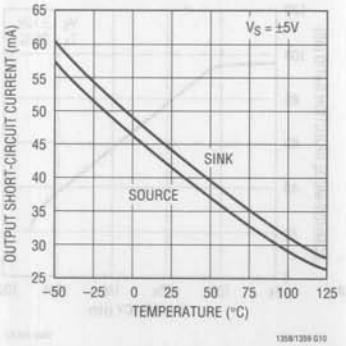
1358/1359 G08

Output Voltage Swing vs Load Current



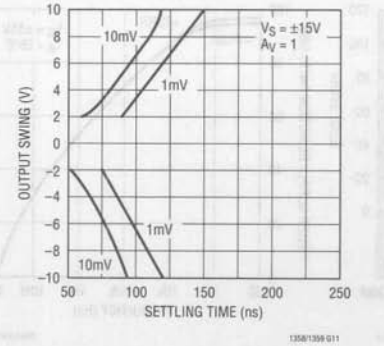
1358/1359 G09

Output Short-Circuit Current vs Temperature



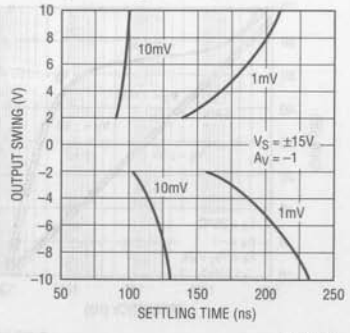
1358/1359 G10

Settling Time vs Output Step (Noninverting)



1358/1359 G11

Settling Time vs Output Step (Inverting)

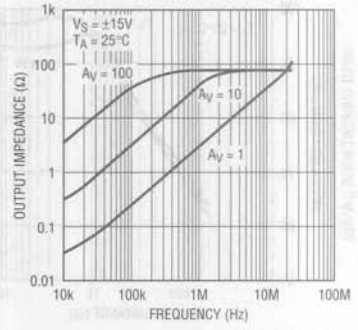


1358/1359 G12

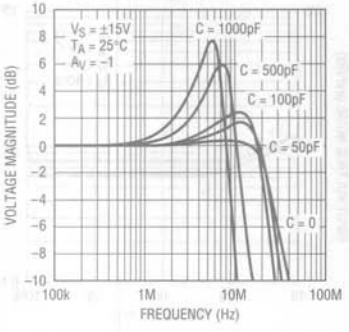
2

TYPICAL PERFORMANCE CHARACTERISTICS

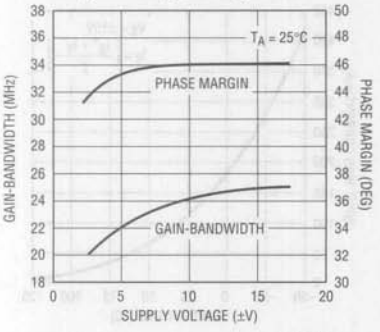
Output Impedance vs Frequency



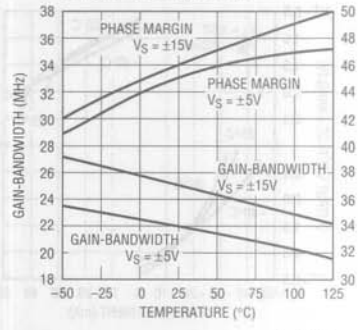
Frequency Response vs Capacitive Load



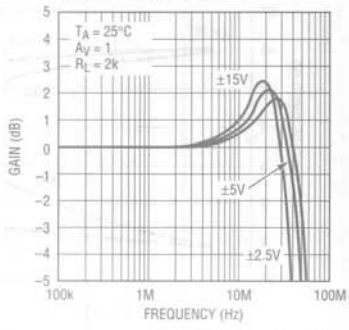
Gain-Bandwidth and Phase Margin vs Supply Voltage



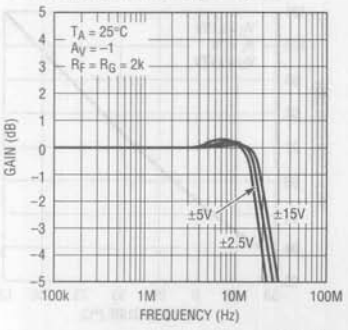
Gain-Bandwidth and Phase Margin vs Temperature



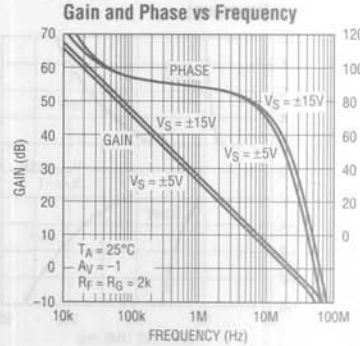
Frequency Response vs Supply Voltage (A_V = 1)



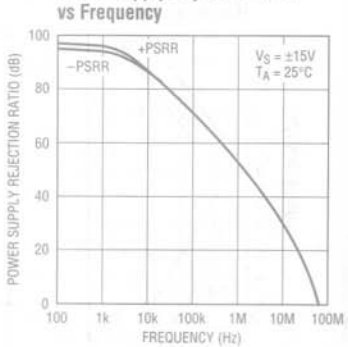
Frequency Response vs Supply Voltage (A_V = –1)



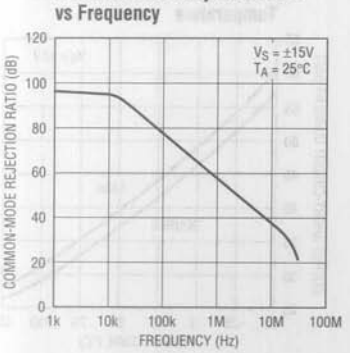
Gain and Phase vs Frequency



Power Supply Rejection Ratio vs Frequency

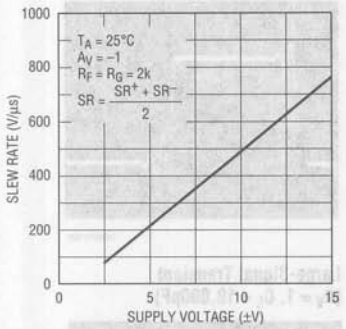


Common-Mode Rejection Ratio vs Frequency

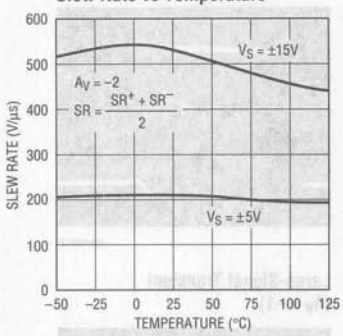


TYPICAL PERFORMANCE CHARACTERISTICS

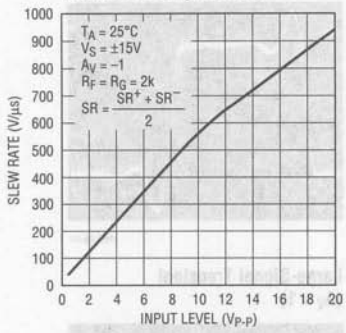
Slew Rate vs Supply Voltage



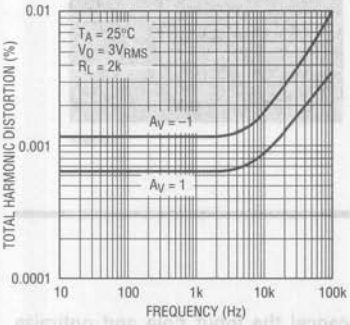
Slew Rate vs Temperature



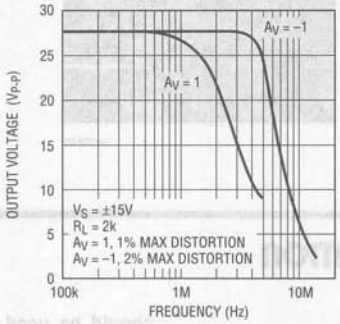
Slew Rate vs Input Level



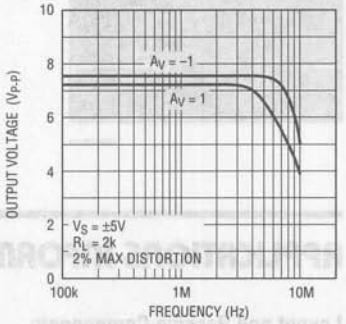
Total Harmonic Distortion vs Frequency



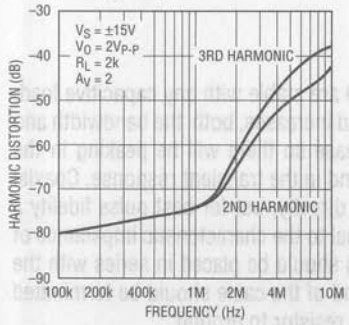
Undistorted Output Swing vs Frequency (±15V)



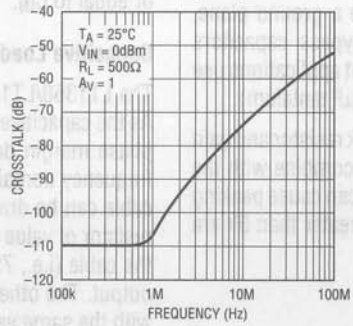
Undistorted Output Swing vs Frequency (±5V)



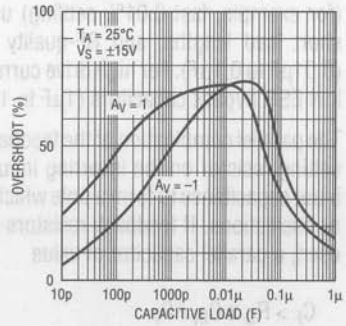
2nd and 3rd Harmonic Distortion vs Frequency



Crosstalk vs Frequency



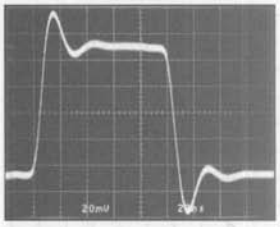
Capacitive Load Handling



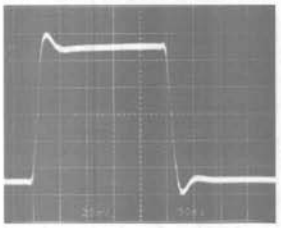
2

TYPICAL PERFORMANCE CHARACTERISTICS

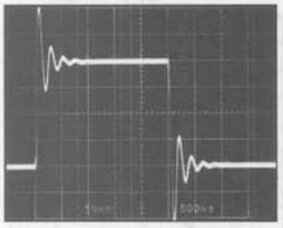
Small-Signal Transient ($A_V = 1$)



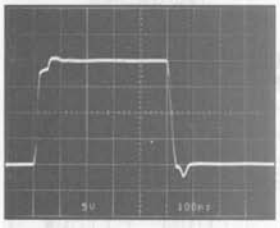
Small-Signal Transient ($A_V = -1$)



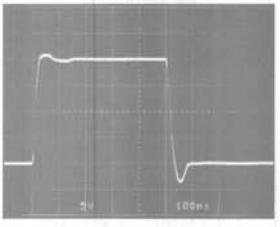
Small-Signal Transient ($A_V = -1$, $C_L = 1000pF$)



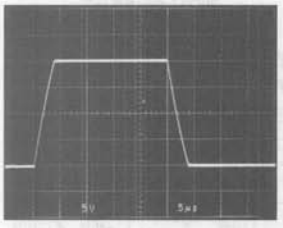
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



Large-Signal Transient ($A_V = 1$, $C_L = 10{,}000pF$)



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1358/LT1359 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN} / R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1358/LT1359 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1358/LT1359 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Circuit Operation

The LT1358/LT1359 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1358/LT1359 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

2

Power Dissipation

The LT1358/LT1359 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1358CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1358CS8: $T_J = T_A + (P_D \times 190°C/W)$
LT1359CN: $T_J = T_A + (P_D \times 110°C/W)$
LT1359CS: $T_J = T_A + (P_D \times 150°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

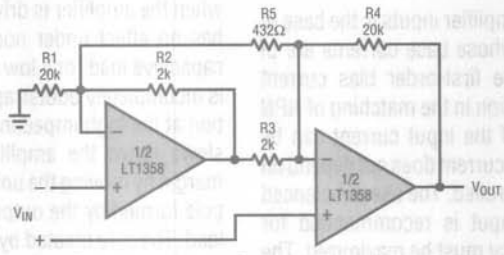
Example: LT1358 in S8 at 70°C, $V_S = \pm 15V$, $R_L = 500\Omega$

$$P_{DMAX} = (30V)(2.9mA) + (7.5V)^2/500\Omega = 200mW$$

$$T_{JMAX} = 70°C + (2 \times 200mW)(190°C/W) = 146°C$$

TYPICAL APPLICATIONS

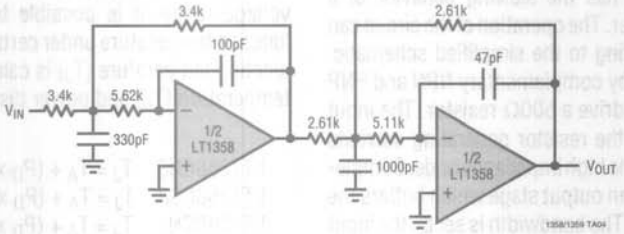
Instrumentation Amplifier



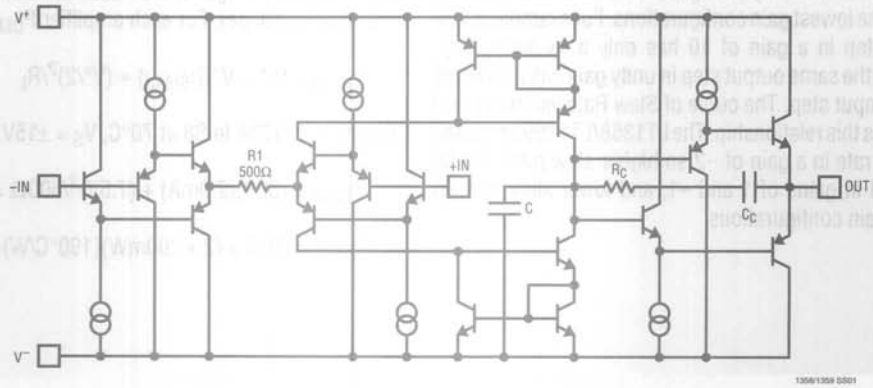
$$A_V = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 250kHz

200kHz, 4th Order Butterworth Filter



SIMPLIFIED SCHEMATIC



LINEAR TECHNOLOGY

50MHz, 800V/μs Op Amp

FEATURES

- **50MHz Gain-Bandwidth**
- **800V/μs Slew Rate**
- **5mA Maximum Supply Current**
- 9nV/√Hz Input Noise Voltage
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 1mV Maximum Input Offset Voltage
- 1μA Maximum Input Bias Current
- 250nA Maximum Input Offset Current
- ±13V Minimum Output Swing into 500Ω
- ±3.2V Minimum Output Swing into 150Ω
- 4.5V/mV Minimum DC Gain, R_L=1k
- 60ns Settling Time to 0.1%, 10V Step
- 0.2% Differential Gain, A_V=2, R_L=150Ω
- 0.3° Differential Phase, A_V=2, R_L=150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

The LT1360 is a high speed, very high slew rate operational amplifier with excellent DC performance. The LT1360 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500Ω load to ±13V with ±15V supplies and a 150Ω load to ±3.2V on ±5V supplies. The amplifier is also capable of driving any capacitive load which makes it useful in buffer or cable driver applications.

The LT1360 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1360 see the LT1361/1362 data sheet. For 70MHz amplifiers with 6mA of supply current per amplifier see the LT1363 and LT1364/1365 data sheets. For lower supply current amplifiers with bandwidths of 12MHz and 25MHz see the LT1354 through LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

C-Load is a trademark of Linear Technology Corporation

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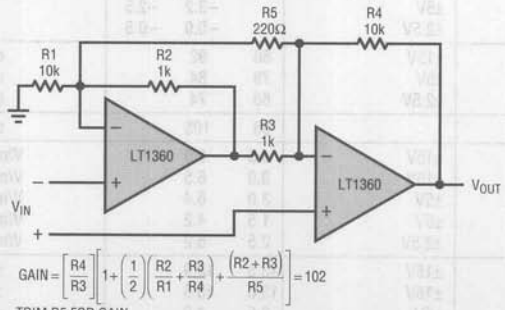
TYPICAL APPLICATION

Two Op Amp Instrumentation Amplifier

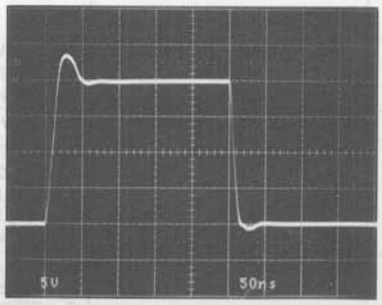


$$GAIN = \left[\frac{R4}{R3}\right]\left[1+\left(\frac{1}{2}\right)\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{(R2+R3)}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 500kHz

1360 TA01

A_V = –1 Large-Signal Response

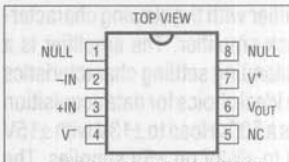


1360 TA02

ABSOLUTE MAXIMUM RATINGS

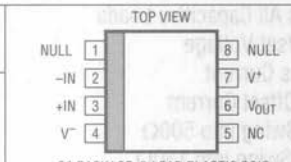
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE, 8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1360CN8



S8 PACKAGE, 8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1360CS8
S8 PART MARKING
1360

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V		0.3	1.0	mV
			±5V		0.3	1.0	mV
			±2.5V		0.4	1.2	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		80	250	nA
I_B	Input Bias Current		±2.5V to ±15V		0.3	1.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.9		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	20	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range +		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range –		±15V		–13.2	–12.0	V
			±5V		–3.2	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	86	92		dB
		V_{CM} = ±2.5V	±5V	79	84		dB
		V_{CM} = ±0.5V	±2.5V	68	74		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		93	105		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	4.5	9.0		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	3.0	6.5		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	3.0	6.4		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1.5	4.2		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	2.5	5.2		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.5	13.9		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	13.0	13.6		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.2	3.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = \pm13V$	±15V	26	34		mA
		$V_{OUT} = \pm3.2V$	±5V	21	29		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	40	54		mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	600	800		V/µs
			±5V	250	350		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)	±15V		12.7		MHz
		3V Peak, (Note 4)	±5V		18.6		MHz
GBW	Gain-Bandwidth	f = 1MHz	±15V		50		MHz
			±5V		37		MHz
			±2.5V		32		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V		3.1		ns
			±5V		4.3		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		35		%
			±5V		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		5.2		ns
			±5V		6.4		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V		60		ns
		10V Step, 0.01%, $A_V = -1$	±15V		90		ns
		5V Step, 0.1%, $A_V = -1$	±5V		65		ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, $R_L = 150\Omega$	±15V		0.20		%
			±5V		0.20		%
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.04		%
			±5V		0.02		%
	Differential Phase	f = 3.58MHz, $A_V = 2$, $R_L = 150\Omega$	±15V		0.40		Deg
			±5V		0.30		Deg
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.07		Deg
			±5V		0.26		Deg
R_O	Output Resistance	$A_V = 1$, f = 1MHz	±15V		1.4		Ω
I_S	Supply Current		±15V		4.0	5.0	mA
			±5V		3.8	4.8	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			1.5	mV
			±5V	●			1.5	mV
			±2.5V	●			1.7	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		9	12	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			350	nA
I_B	Input Bias Current		±2.5V to ±15V	●			1.5	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	84			dB
		$V_{CM} = \pm2.5V$	±5V	●	77			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to ±15V		●	91			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	3.6			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	2.4			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	2.4			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	1.0			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	2.0			V/mV

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.8			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.1			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12.8V$	±15V	●	25			mA
		$V_{OUT} = \pm3.1V$	±5V	●	20			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	32			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	475			V/µs
			±5V	●	185			V/µs
I_S	Supply Current		±15V	●			5.8	mA
			±5V	●			5.6	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.0	mV
			±5V	●			2.0	mV
			±2.5V	●			2.2	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		9	12	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			400	nA
I_B	Input Bias Current		±2.5V to ±15V	●			1.8	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	84			dB
		$V_{CM} = \pm2.5V$	±5V	●	77			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	1.3			V/mV
V_{OUT}	Output Swing	$R_L = 1k\Omega$, $V_{IN} = \pm40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12.0V$	±15V	●	24			mA
		$V_{OUT} = \pm3.0V$	±5V	●	20			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	30			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	450			V/µs
			±5V	●	175			V/µs
I_S	Supply Current		±15V	●			6.0	mA
			±5V	●			5.8	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 3: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±2V on the output with ±1.75V input for ±5V supplies.

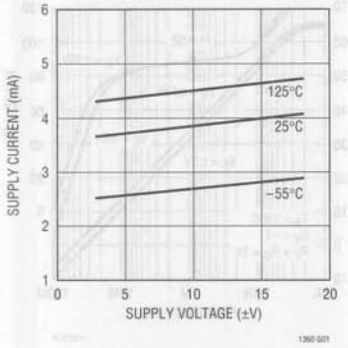
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 5: This parameter is not 100% tested.

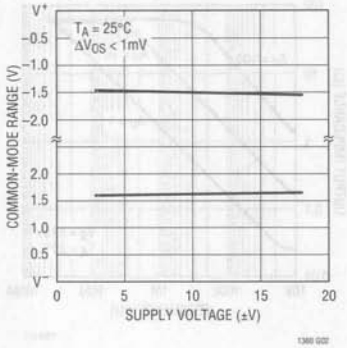
Note 6: The LT1360 is not tested and is not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

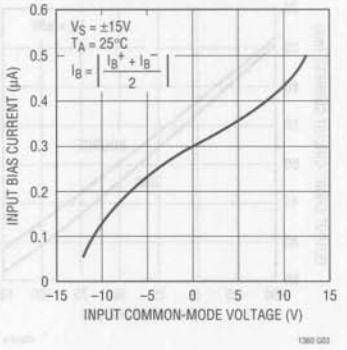
Supply Current vs Supply Voltage and Temperature



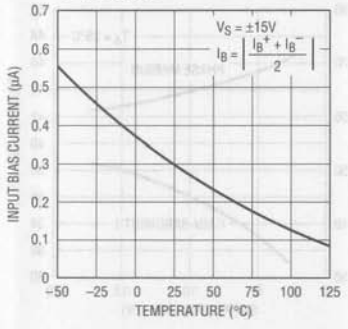
Input Common-Mode Range vs Supply Voltage



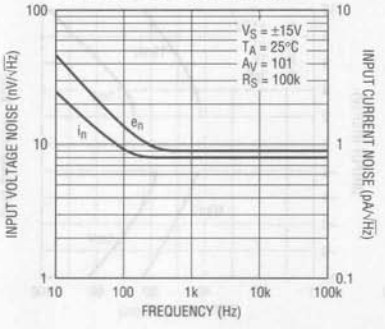
Input Bias Current vs Input Common-Mode Voltage



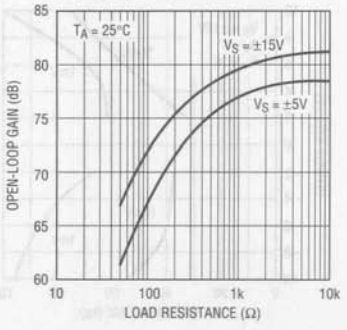
Input Bias Current vs Temperature



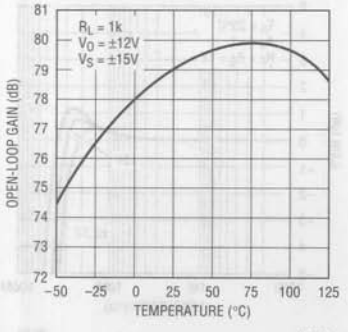
Input Noise Spectral Density



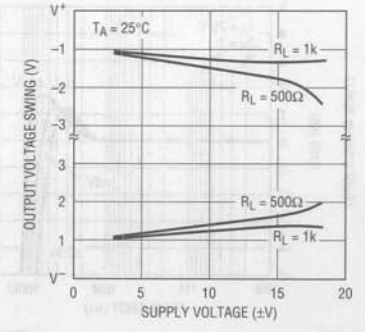
Open-Loop Gain vs Resistive Load



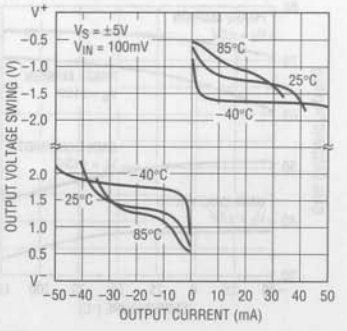
Open-Loop Gain vs Temperature



Output Voltage Swing vs Supply Voltage

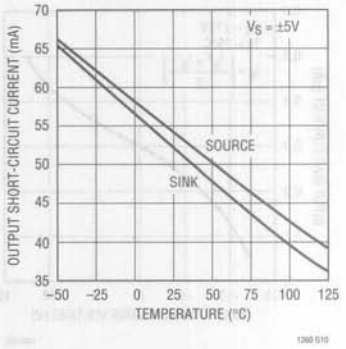


Output Voltage Swing vs Load Current

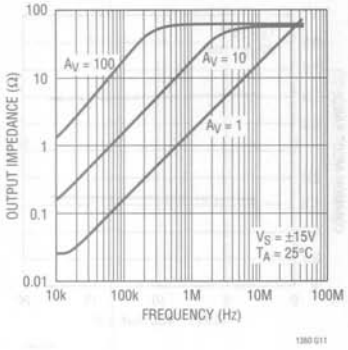


TYPICAL PERFORMANCE CHARACTERISTICS

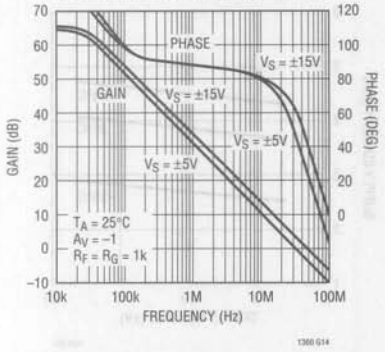
Output Short-Circuit Current vs Temperature



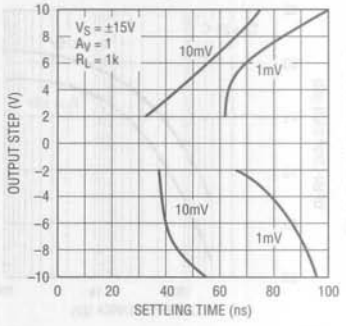
Output Impedance vs Frequency



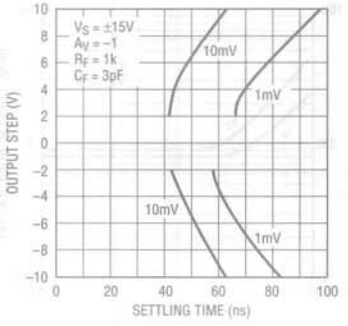
Gain and Phase vs Frequency



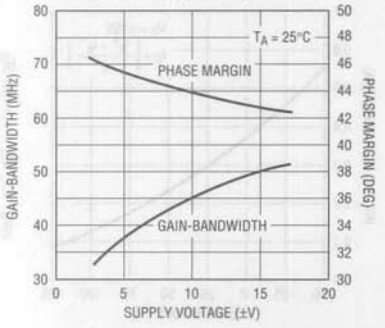
Settling Time vs Output Step (Noninverting)



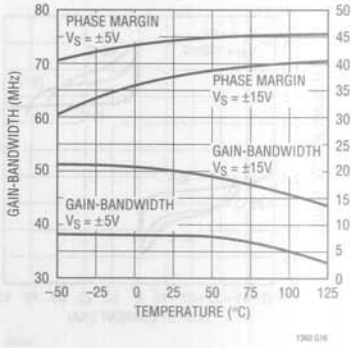
Settling Time vs Output Step (Inverting)



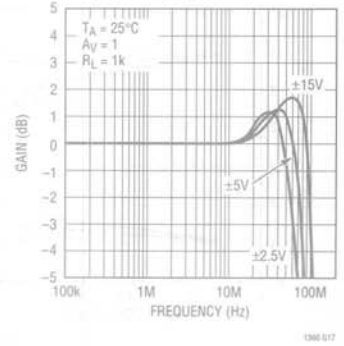
Gain-Bandwidth and Phase Margin vs Supply Voltage



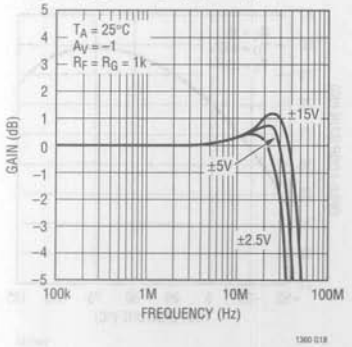
Gain-Bandwidth and Phase Margin vs Temperature



Frequency Response vs Supply Voltage (AV = 1)

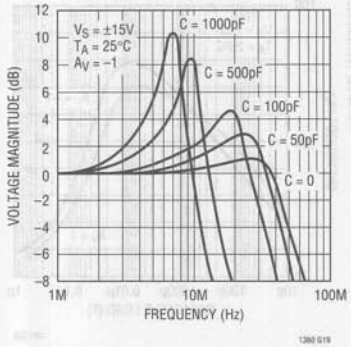


Frequency Response vs Supply Voltage (AV = –1)

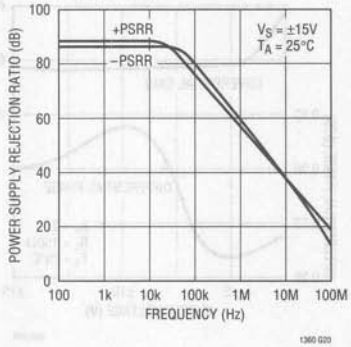


TYPICAL PERFORMANCE CHARACTERISTICS

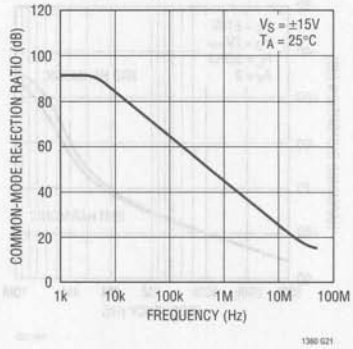
Frequency Response vs Capacitive Load



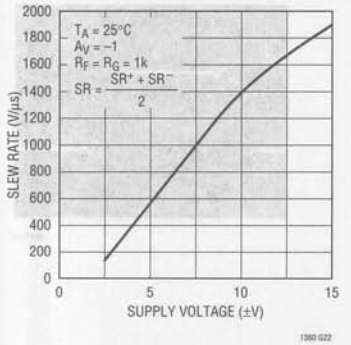
Power Supply Rejection Ratio vs Frequency



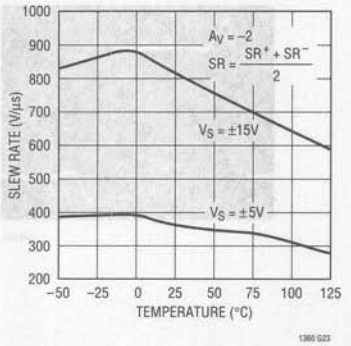
Common-Mode Rejection Ratio vs Frequency



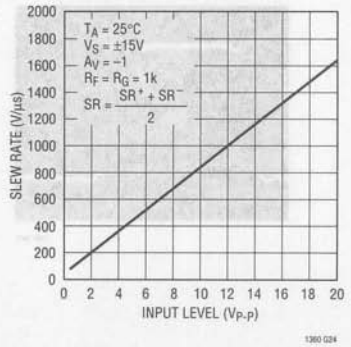
Slew Rate vs Supply Voltage



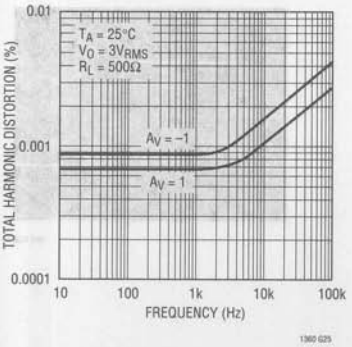
Slew Rate vs Temperature



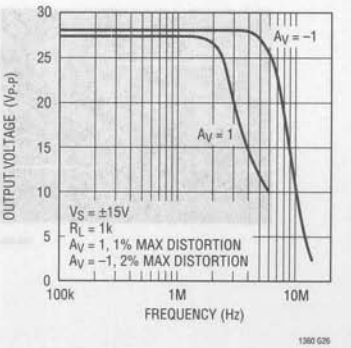
Slew Rate vs Input Level



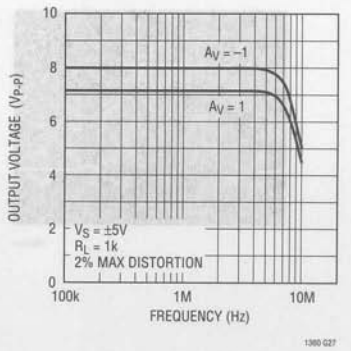
Total Harmonic Distortion vs Frequency



Undistorted Output Swing vs Frequency (±15V)



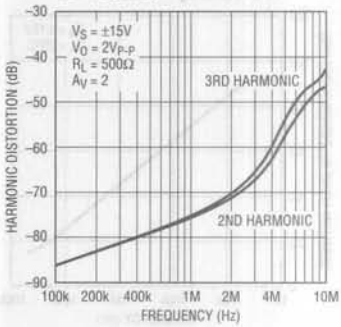
Undistorted Output Swing vs Frequency (±5V)



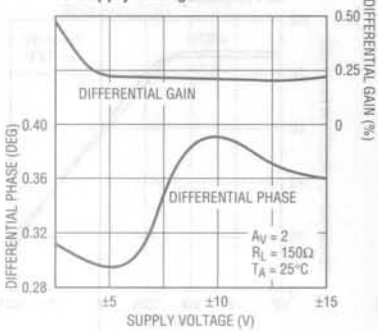
2

TYPICAL PERFORMANCE CHARACTERISTICS

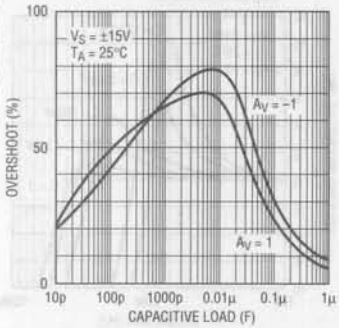
2nd and 3rd Harmonic Distortion vs Frequency



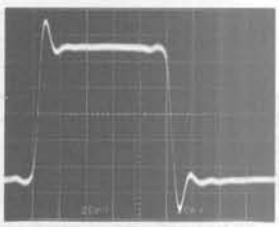
Differential Gain and Phase vs Supply Voltage



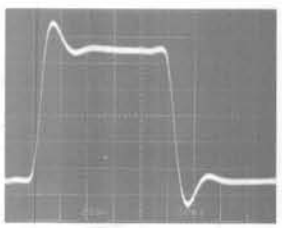
Capacitive Load Handling



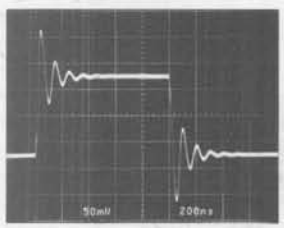
Small-Signal Transient (A_V = 1)



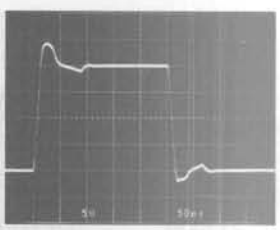
Small-Signal Transient (A_V = –1)



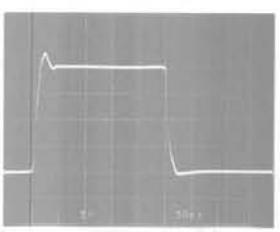
Small-Signal Transient (A_V = –1, C_L = 500pF)



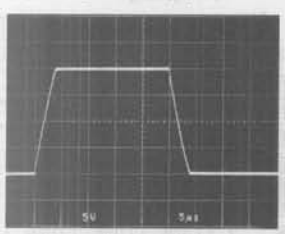
Large-Signal Transient (A_V = 1)



Large-Signal Transient (A_V = –1)



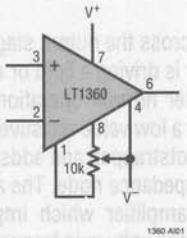
Large-Signal Transient (A_V = 1, C_L = 10,000pF)



APPLICATIONS INFORMATION

The LT1360 may be inserted directly into AD817, AD847, EL2020, EL2044, and LM6361 applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1360 is shown below.

Offset Nulling



Layout and Passive Components

The LT1360 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

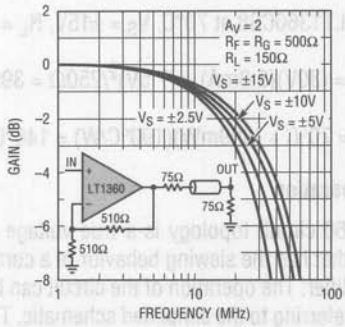
$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1360 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 500pF load shows 60% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited to 5V/µs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Cable Driver Frequency Response



Input Considerations

Each of the LT1360 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

APPLICATIONS INFORMATION

Power Dissipation

The LT1360 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1360CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1360CS8: $T_J = T_A + (P_D \times 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1360CS8 at 70°C, $V_S = \pm 15V$, $R_L = 250\Omega$

$$P_{DMAX} = (30V)(5.8mA) + (7.5V)^2/250\Omega = 399mW$$

$$T_{JMAX} = 70°C + (399mW)(190°C/W) = 146°C$$

Circuit Operation

The LT1360 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1360 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

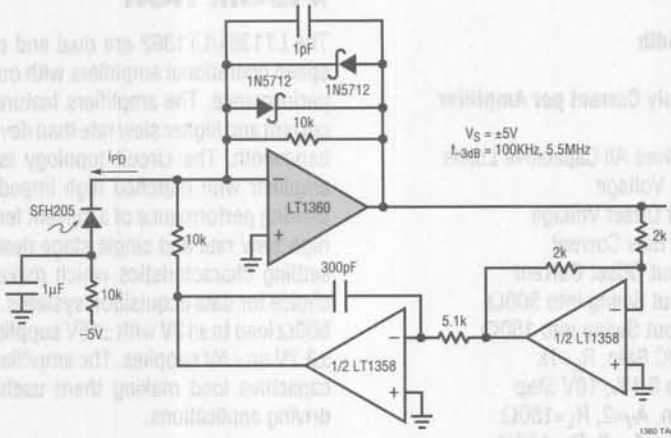
The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Comparison to Current Feedback Amplifiers

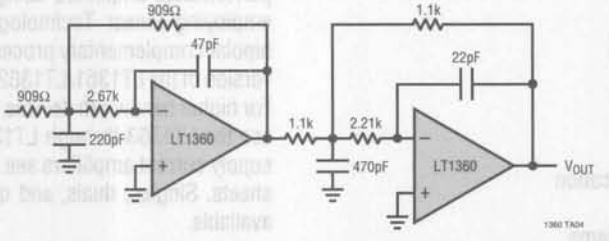
The LT1360 enjoys the high slew rates of Current Feedback Amplifiers (CFAs) while maintaining the characteristics of a true voltage feedback amplifier. The primary differences are that the LT1360 has two high impedance inputs and its closed loop bandwidth decreases as the gain increases. CFAs have a low impedance inverting input and maintain relatively constant bandwidth with increasing gain. The LT1360 can be used in all traditional op amp configurations including integrators and applications such as photodiode amplifiers and I-to-V converters where there may be significant capacitance on the inverting input. The frequency compensation is internal and not dependent on the value of the feedback resistor. For CFAs, the feedback resistance is fixed for a given bandwidth and capacitance on the inverting input can cause peaking or oscillations. The slew rate of the LT1360 in noninverting gain configurations is also superior in most cases.

TYPICAL APPLICATIONS

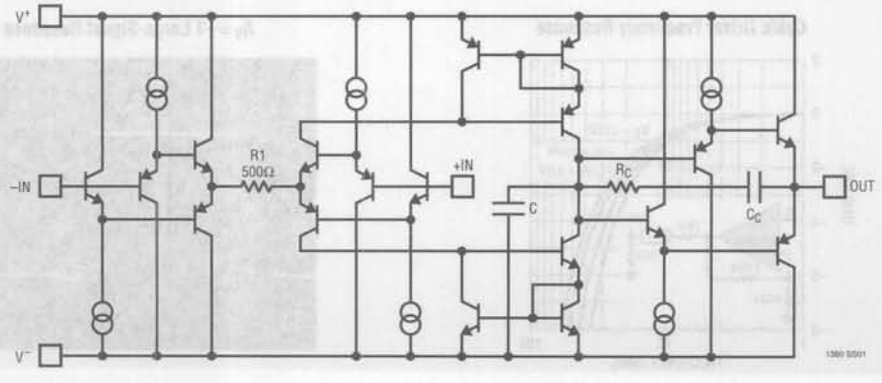
Photodiode Preamp with AC Coupling Loop



1MHz, 4th Order Butterworth Filter



SIMPLIFIED SCHEMATIC



Dual and Quad 50MHz, 800V/µs Op Amps

FEATURES

- **50MHz Gain-Bandwidth**
- **800V/µs Slew Rate**
- **5mA Maximum Supply Current per Amplifier**
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 9nV/√Hz Input Noise Voltage
- 1mV Maximum Input Offset Voltage
- 1µA Maximum Input Bias Current
- 250nA Maximum Input Offset Current
- ±13V Minimum Output Swing into 500Ω
- ±3.2V Minimum Output Swing into 150Ω
- 4.5V/mV Minimum DC Gain, R_L=1k
- 60ns Settling Time to 0.1%, 10V Step
- 0.2% Differential Gain, A_V=2, R_L=150Ω
- 0.3° Differential Phase, A_V=2, R_L=150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

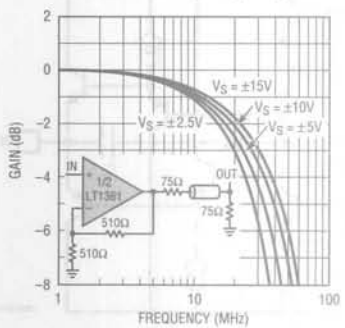
The LT1361/LT1362 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±13V with ±15V supplies and a 150Ω load to ±3.2V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer or cable driving applications.

The LT1361/LT1362 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1361/LT1362 see the LT1360 data sheet. For higher bandwidth devices with higher supply currents see the LT1363 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 to LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

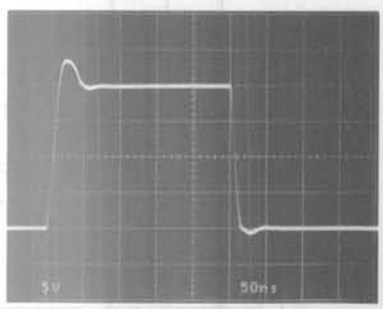
C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Cable Driver Frequency Response



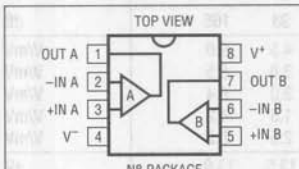
A_V = –1 Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

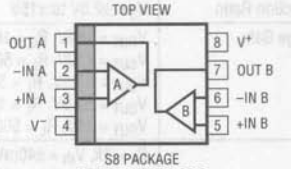
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



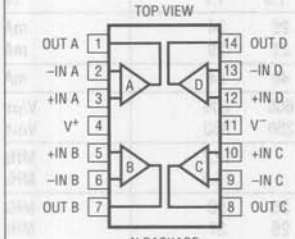
N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1361CN8



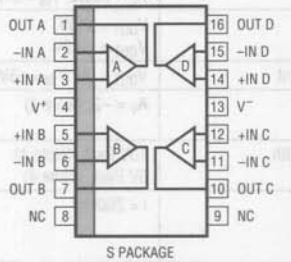
S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1361CS8
S8 PART MARKING
1361



N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1362CN



S PACKAGE
16-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1362CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V		0.3	1.0	mV
			±5V		0.3	1.0	mV
			±2.5V		0.4	1.2	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		80	250	nA
I_B	Input Bias Current		±2.5V to ±15V		0.3	1.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.9		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	20	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range +		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range −		±15V		−13.2	−12.0	V
			±5V		−3.2	−2.5	V
			±2.5V		−0.9	−0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	86	92		dB
		V_{CM} = ±2.5V	±5V	79	84		dB
		V_{CM} = ±0.5V	±2.5V	68	74		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		93	105		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	4.5	9.0		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	3.0	6.5		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	3.0	6.4		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1.5	4.2		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	2.5	5.2		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.5	13.9		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	13.0	13.6		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.2	3.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	V_{OUT} = ±13V	±15V	26	34		mA
		V_{OUT} = ±3.2V	±5V	21	29		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	40	54		mA
SR	Slew Rate	A_V = −2, (Note 3)	±15V	600	800		V/µs
			±5V	250	350		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)	±15V		12.7		MHz
		3V Peak, (Note 4)	±5V		18.6		MHz
GBW	Gain-Bandwidth	f = 200kHz	±15V	35	50		MHz
			±5V	25	37		MHz
			±2.5V		32		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10%-90%, 0.1V	±15V		3.1		ns
			±5V		4.3		ns
	Overshoot	A_V = 1, 0.1V	±15V		35		%
			±5V		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		5.2		ns
			±5V		6.4		ns
t_s	Settling Time	10V Step, 0.1%, A_V = −1	±15V		60		ns
		10V Step, 0.01%, A_V = −1	±15V		90		ns
		5V Step, 0.1%, A_V = −1	±5V		65		ns
	Differential Gain	f = 3.58MHz, A_V = 2, R_L = 150Ω	±15V		0.20		%
			±5V		0.20		%
		f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.04		%
			±5V		0.02		%
	Differential Phase	f = 3.58MHz, A_V = 2, R_L = 150Ω	±15V		0.40		Deg
			±5V		0.30		Deg
		f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.07		Deg
			±5V		0.26		Deg
R_O	Output Resistance	A_V = 1, f = 1MHz	±15V		1.4		Ω
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		4.0	5.0	mA
		Each Amplifier	±5V		3.8	4.8	mA

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			1.5	mV
			±5V	●			1.5	mV
			±2.5V	●			1.7	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		9	12	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			350	nA
I_B	Input Bias Current		±2.5V to ±15V	●			1.5	µA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	●	84			dB
		V_{CM} = ±2.5V	±5V	●	77			dB
		V_{CM} = ±0.5V	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	91			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	●	3.6			V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	●	2.4			V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	●	2.4			V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	●	1.0			V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	●	2.0			V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	●	13.4			±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	●	12.8			±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	●	3.4			±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	●	3.1			±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	●	1.2			±V
I_{OUT}	Output Current	V_{OUT} = ±12.8V	±15V	●	25			mA
		V_{OUT} = ±3.1V	±5V	●	20			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	32			mA
SR	Slew Rate	A_V = −2, (Note 3)	±15V	●	475			V/µs
			±5V	●	185			V/µs
GBW	Gain-Bandwidth	f = 200kHz	±15V	●	31			MHz
			±5V	●	22			MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			5.8	mA
		Each Amplifier	±5V	●			5.6	mA

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.0	mV
			±5V	●			2.0	mV
			±2.5V	●			2.2	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		9	12	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			400	nA
I_B	Input Bias Current		±2.5V to ±15V	●			1.8	µA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	●	84			dB
		V_{CM} = ±2.5V	±5V	●	77			dB
		V_{CM} = ±0.5V	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	90			dB

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	1.3			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12.0V$	±15V	●	24			mA
		$V_{OUT} = \pm3.0V$	±5V	●	20			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	30			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	450			V/µs
			±5V	●	175			V/µs
GBW	Gain-Bandwidth	f = 200kHz	±15V	●	30			MHz
			±5V	●	20			MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			6.0	mA
		Each Amplifier	±5V	●			5.8	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 3: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

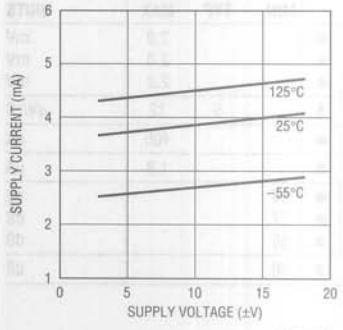
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 5: This parameter is not 100% tested.

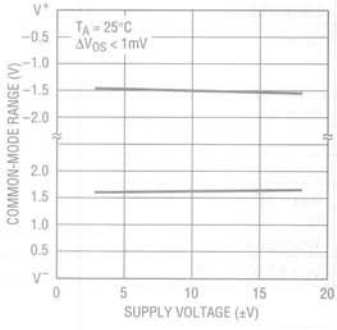
Note 6: The LT1361/LT1362 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

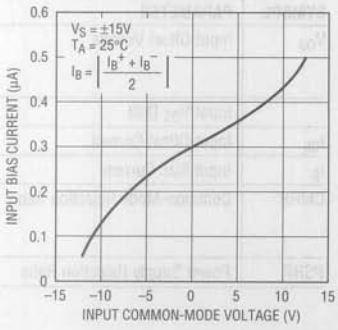
Supply Current vs Supply Voltage and Temperature



Input Common-Mode Range vs Supply Voltage

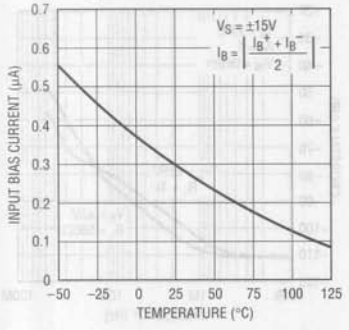


Input Bias Current vs Input Common-Mode Voltage

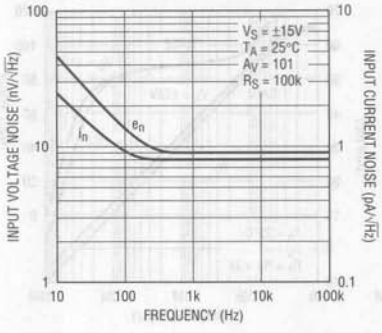


TYPICAL PERFORMANCE CHARACTERISTICS

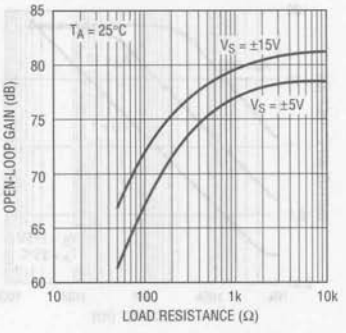
Input Bias Current vs Temperature



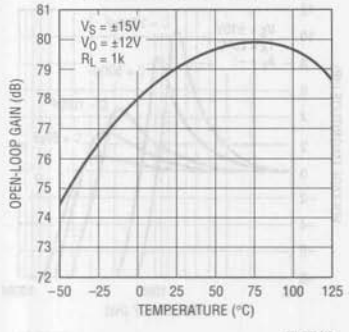
Input Noise Spectral Density



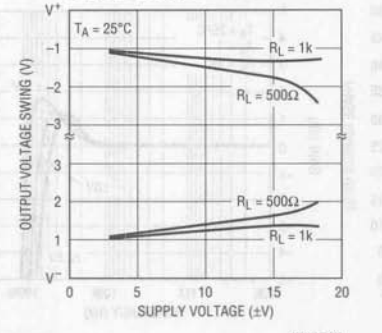
Open-Loop Gain vs Resistive Load



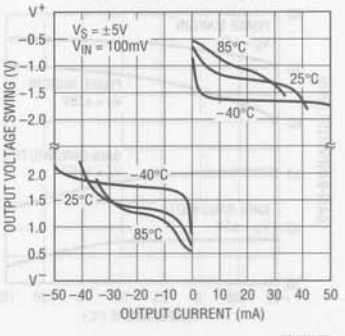
Open-Loop Gain vs Temperature



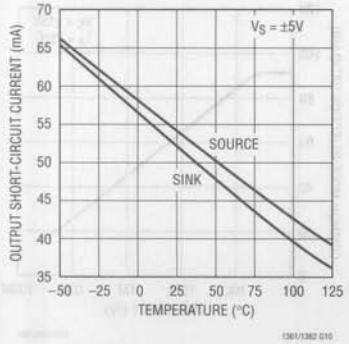
Output Voltage Swing vs Supply Voltage



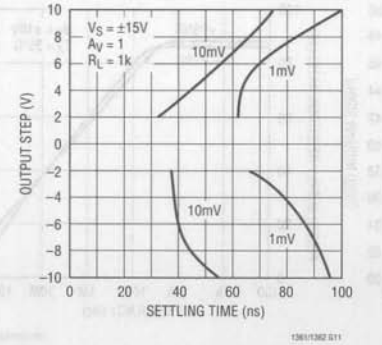
Output Voltage Swing vs Load Current



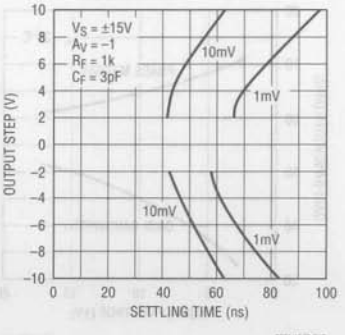
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)



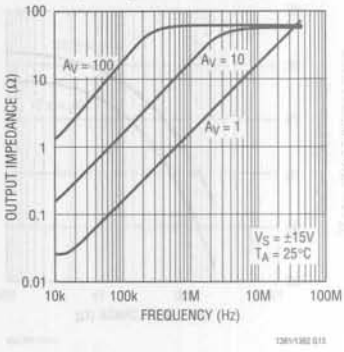
Settling Time vs Output Step (Inverting)



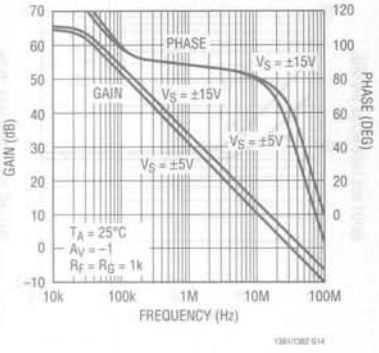
2

TYPICAL PERFORMANCE CHARACTERISTICS

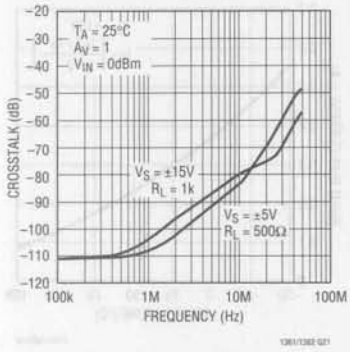
Output Impedance vs Frequency



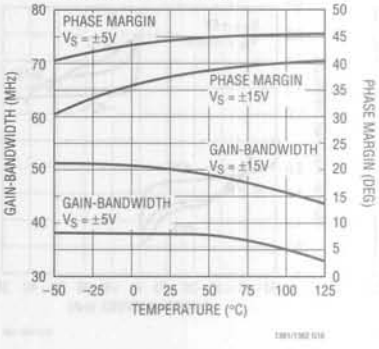
Gain and Phase vs Frequency



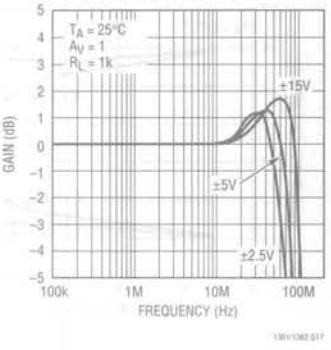
Crosstalk vs Frequency



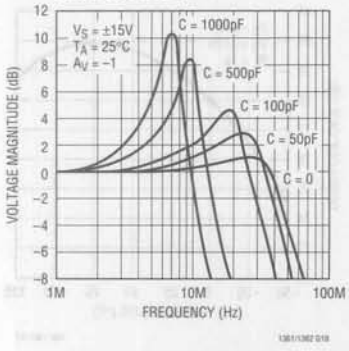
Gain-Bandwidth and Phase Margin vs Temperature



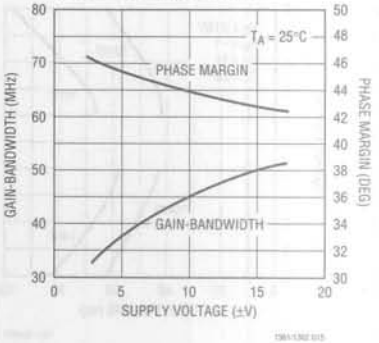
Frequency Response vs Supply Voltage (A_V = 1)



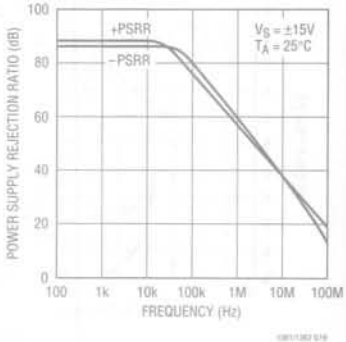
Frequency Response vs Capacitive Load



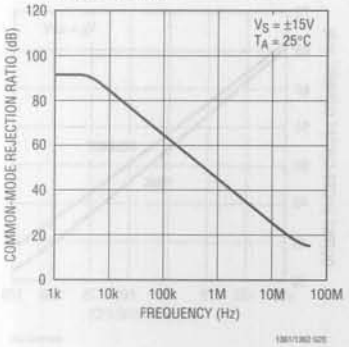
Gain-Bandwidth and Phase Margin vs Supply Voltage



Power Supply Rejection Ratio vs Frequency

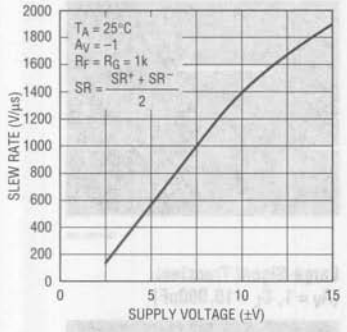


Common-Mode Rejection Ratio vs Frequency

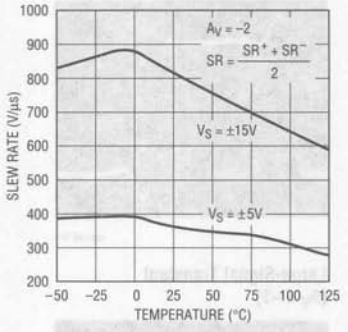


TYPICAL PERFORMANCE CHARACTERISTICS

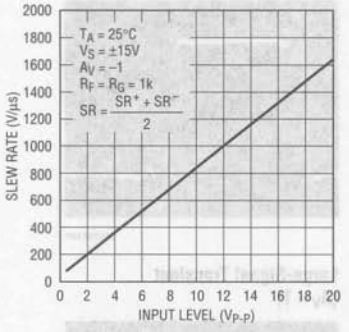
Slew Rate vs Supply Voltage



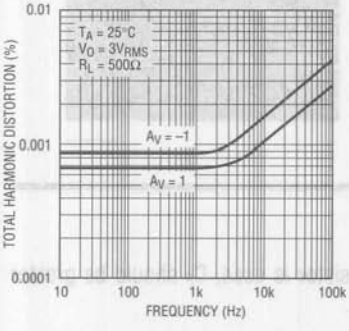
Slew Rate vs Temperature



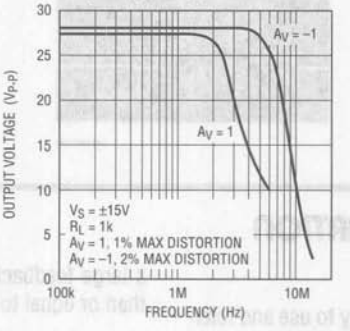
Slew Rate vs Input Level



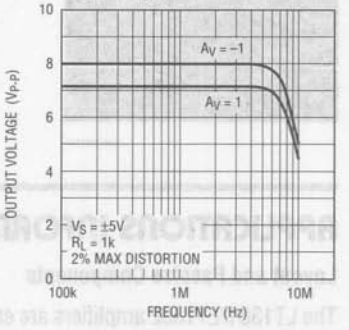
Total Harmonic Distortion vs Frequency



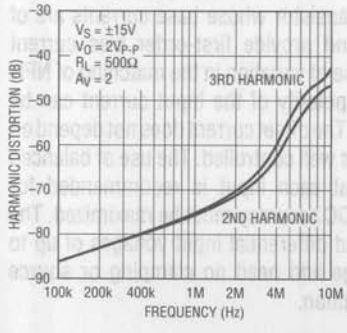
Undistorted Output Swing vs Frequency (±15V)



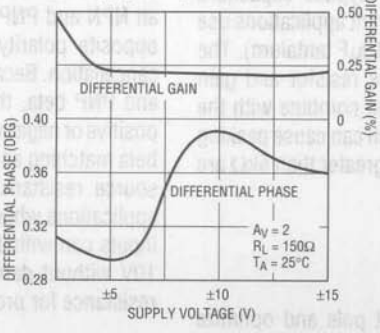
Undistorted Output Swing vs Frequency (±5V)



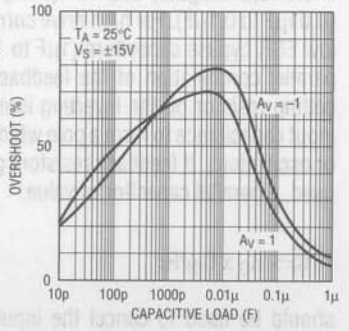
2nd and 3rd Harmonic Distortion vs Frequency



Differential Gain and Phase vs Supply Voltage



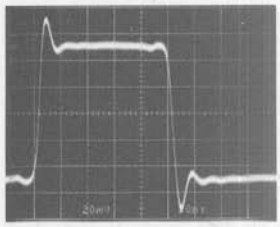
Capacitive Load Handling



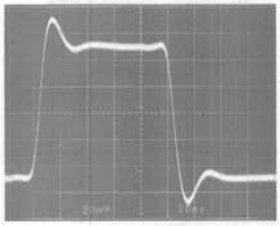
2

TYPICAL PERFORMANCE CHARACTERISTICS

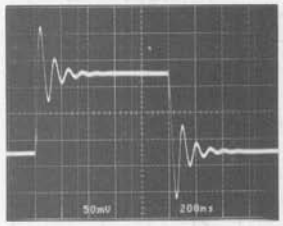
Small-Signal Transient ($A_V = 1$)



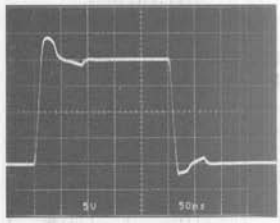
Small-Signal Transient ($A_V = -1$)



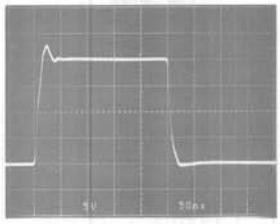
Small-Signal Transient ($A_V = -1$, $C_L = 500pF$)



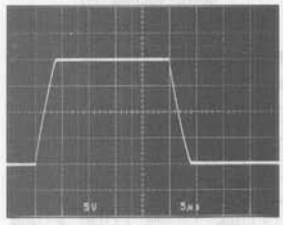
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



Large-Signal Transient ($A_V = 1$, $C_L = 10,000pF$)



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1361/LT1362 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Input Considerations

Each of the LT1361/LT1362 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

APPLICATIONS INFORMATION

Capacitive Loading

The LT1361/LT1362 are stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small signal response with 500pF load shows 60% peaking. The large signal response shows the output slew rate being limited to 5V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Circuit Operation

The LT1361/LT1362 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1361/LT1362 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

2

Power Dissipation

The LT1361/LT1362 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1361CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1361CS8: $T_J = T_A + (P_D \times 190°C/W)$
LT1362CN: $T_J = T_A + (P_D \times 110°C/W)$
LT1362CS: $T_J = T_A + (P_D \times 150°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

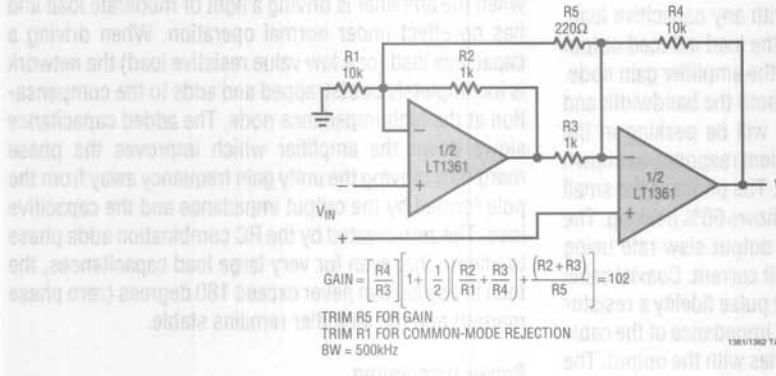
Example: LT1362 in S16 at 70°C, $V_S = \pm 5V$, $R_L = 100\Omega$

$$P_{DMAX} = (10V)(5.6mA) + (2.5V)^2/100\Omega = 119mW$$

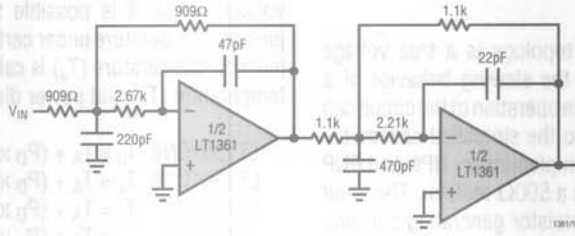
$$T_{JMAX} = 70°C + (4 \times 119mW)(150°C/W) = 141°C$$

TYPICAL APPLICATIONS

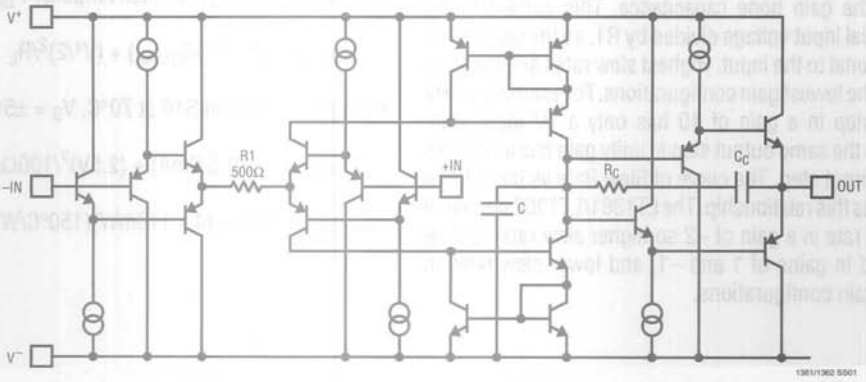
Two Op Amp Instrumentation Amplifier



1MHz, 4th Order Butterworth Filter



SIMPLIFIED SCHEMATIC



LINEAR TECHNOLOGY

70MHz, 1000V/µs Op Amp

FEATURES

- **70MHz Gain-Bandwidth**
- **1000V/µs Slew Rate**
- **7.5mA Maximum Supply Current**
- 9nV/√Hz Input Noise Voltage
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 1.5mV Maximum Input Offset Voltage
- 2µA Maximum Input Bias Current
- 350nA Maximum Input Offset Current
- 50mA Minimum Output Current
- ±7.5V Minimum Output Swing into 150Ω
- 4.5V/mV Minimum DC Gain, R_L=1k
- 50ns Settling Time to 0.1%, 10V Step
- 0.06% Differential Gain, A_V=2, R_L=150Ω
- 0.04° Differential Phase, A_V=2, R_L=150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

The LT1363 is a high speed, very high slew rate operational amplifier with excellent DC performance. The LT1363 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 150Ω load to ±7.5V with ±15V supplies and to ±3.4V on ±5V supplies. The amplifier is also capable of driving any capacitive load which makes it useful in buffer or cable driver applications.

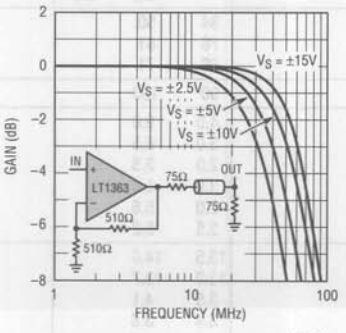
The LT1363 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1363 see the LT1364/1365 data sheet. For 50MHz amplifiers with 4mA of supply current per amplifier see the LT1360 and LT1361/1362 data sheets. For lower supply current amplifiers with bandwidths of 12MHz and 25MHz see the LT1354 through LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

C-Load is a trademark of Linear Technology Corporation

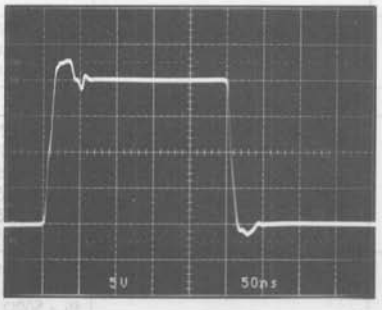
2

TYPICAL APPLICATION

Cable Driver Frequency Response



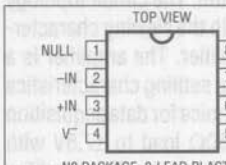
A_V = –1 Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

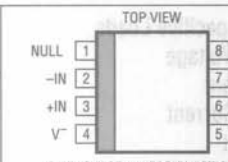
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE, 8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1363CN8



S8 PACKAGE, 8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1363CS8
S8 PART MARKING
1363

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V		0.5	1.5	mV
			±5V		0.5	1.5	mV
			±2.5V		0.7	1.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		120	350	nA
I_B	Input Bias Current		±2.5V to ±15V		0.6	2.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	12	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range⁺		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range⁻		±15V		–13.2	–12.0	V
			±5V		–3.2	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	±15V	84	90		dB
		V_{CM} = ±2.5V	±5V	76	81		dB
		V_{CM} = ±0.5V	±2.5V	66	71		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		90	100		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	4.5	9.0		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	3.0	6.5		V/mV
		V_{OUT} = ±7.5V, R_L = 150Ω	±15V	2.0	3.8		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	3.0	6.4		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	2.0	5.6		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	2.5	5.2		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.5	14.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	13.0	13.7		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.1		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.4	3.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = \pm7.5V$	±15V	50	60		mA
		$V_{OUT} = \pm3.4V$	±5V	23	29		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	70	105		mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	750	1000		V/µs
			±5V	300	450		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)	±15V		15.9		MHz
		3V Peak, (Note 4)	±5V		23.9		MHz
GBW	Gain-Bandwidth	f = 1MHz	±15V		70		MHz
			±5V		50		MHz
			±2.5V		40		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V		2.6		ns
			±5V		3.6		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		36		%
			±5V		23		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		4.6		ns
			±5V		5.6		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V		50		ns
		10V Step, 0.01%, $A_V = -1$	±15V		80		ns
		5V Step, 0.1%, $A_V = -1$	±5V		55		ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, $R_L = 150\Omega$	±15V		0.03		%
			±5V		0.06		%
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.01		%
			±5V		0.01		%
	Differential Phase	f = 3.58MHz, $A_V = 2$, $R_L = 150\Omega$	±15V		0.10		Deg
			±5V		0.04		Deg
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.05		Deg
			±5V		0.25		Deg
R_O	Output Resistance	$A_V = 1$, f = 1MHz	±15V		0.7		Ω
I_S	Supply Current		±15V		6.3	7.5	mA
			±5V		6.0	7.2	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.0	mV
			±5V	●			2.0	mV
			±2.5V	●			2.2	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			500	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	82			dB
		$V_{CM} = \pm2.5V$	±5V	●	74			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	64			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to ±15V		●	88			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	3.6			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	2.4			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	2.4			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	1.5			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	2.0			V/mV

2

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	12.8			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.3			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.8V$	±15V	●	25			mA
		$V_{OUT} = \pm 3.3V$	±5V	●	22			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	55			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	600			V/µs
			±5V	●	225			V/µs
I_S	Supply Current		±15V	●			8.7	mA
			±5V	●			8.4	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.5	mV
			±5V	●			2.5	mV
			±2.5V	●			2.7	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			600	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3.6	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$	±15V	●	82			dB
		$V_{CM} = \pm 2.5V$	±5V	●	74			dB
		$V_{CM} = \pm 0.5V$	±2.5V	●	64			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to ±15V		●	87			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L = 1k$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	±15V	●	1.5			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	±5V	●	1.5			V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	±5V	●	1.0			V/mV
		$V_{OUT} = \pm 1V$, $R_L = 500\Omega$	±2.5V	●	1.3			V/mV
V_{OUT}	Output Swing	$R_L = 1k\Omega$, $V_{IN} = \pm 40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±15V	●	12.7			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	±5V	●	3.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.7V$	±15V	●	25			mA
		$V_{OUT} = \pm 3.2V$	±5V	●	21			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm 3V$	±15V	●	50			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	550			V/µs
			±5V	●	180			V/µs
I_S	Supply Current		±15V	●			9.0	mA
			±5V	●			8.7	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 3: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±2V on the output with ±1.75V input for ±5V supplies.

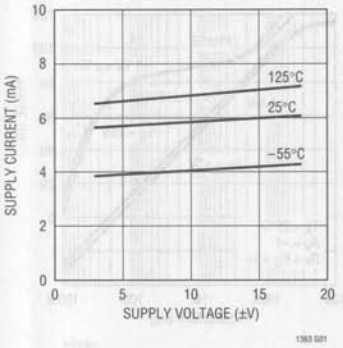
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 5: This parameter is not 100% tested.

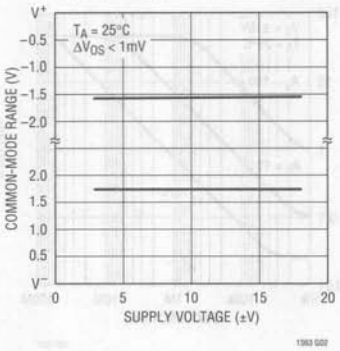
Note 6: The LT1363 is not tested and is not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

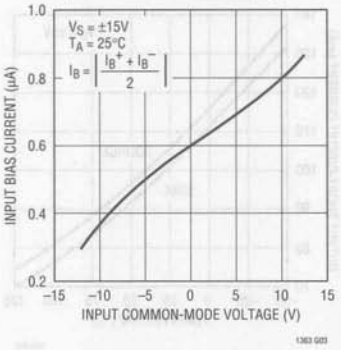
Supply Current vs Supply Voltage and Temperature



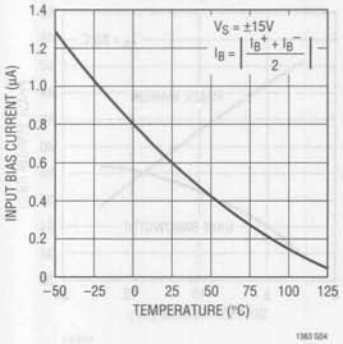
Input Common-Mode Range vs Supply Voltage



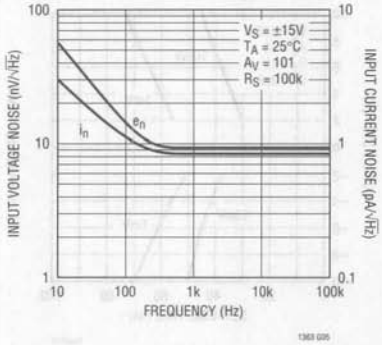
Input Bias Current vs Input Common-Mode Voltage



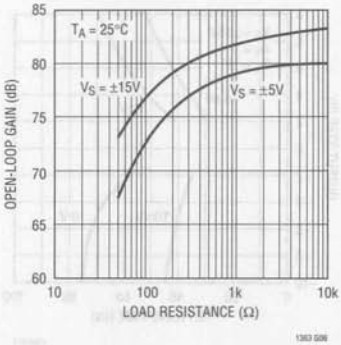
Input Bias Current vs Temperature



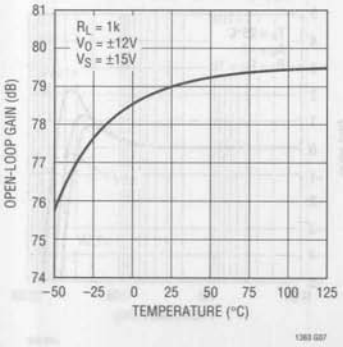
Input Noise Spectral Density



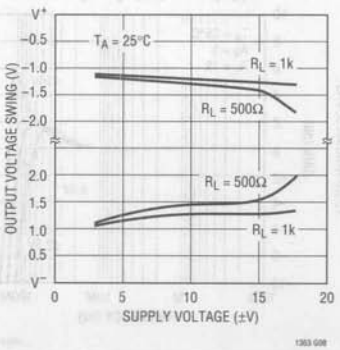
Open-Loop Gain vs Resistive Load



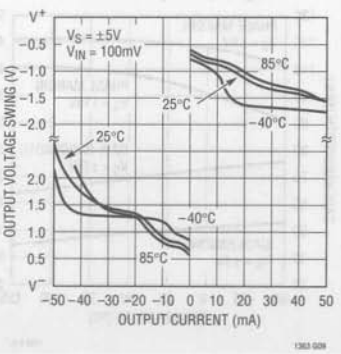
Open-Loop Gain vs Temperature



Output Voltage Swing vs Supply Voltage



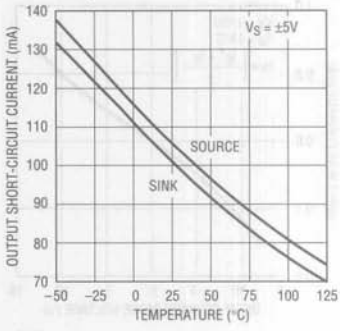
Output Voltage Swing vs Load Current



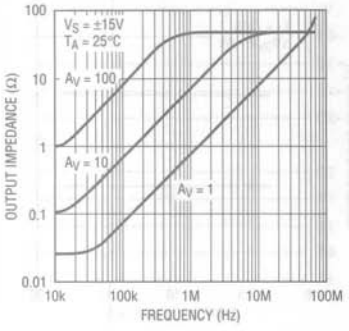
2

TYPICAL PERFORMANCE CHARACTERISTICS

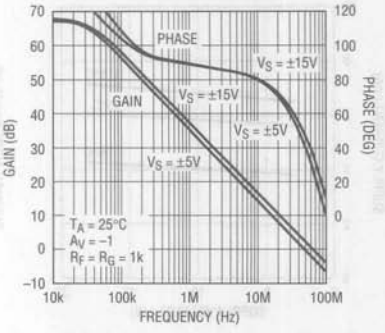
Output Short-Circuit Current vs Temperature



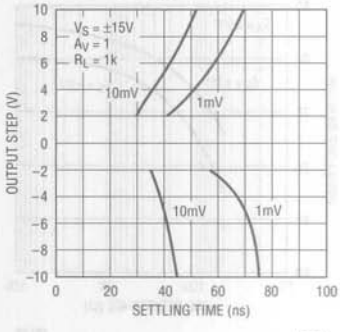
Output Impedance vs Frequency



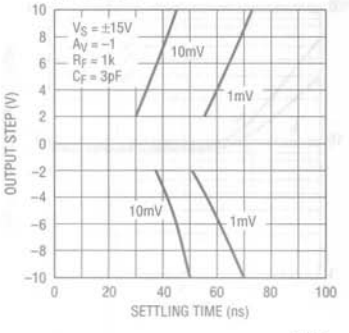
Gain and Phase vs Frequency



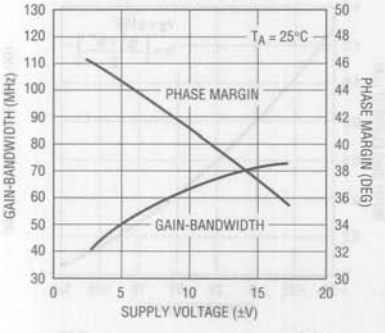
Settling Time vs Output Step (Noninverting)



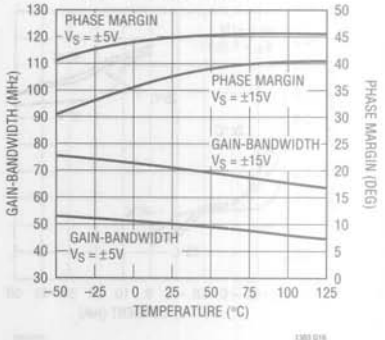
Settling Time vs Output Step (Inverting)



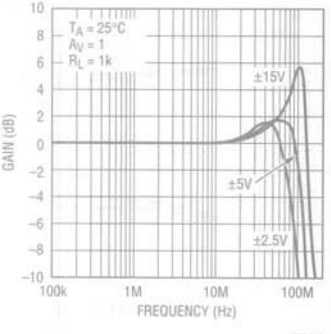
Gain-Bandwidth and Phase Margin vs Supply Voltage



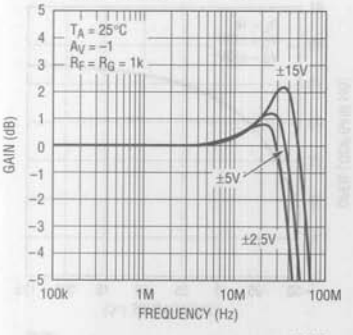
Gain-Bandwidth and Phase Margin vs Temperature



Frequency Response vs Supply Voltage (A_V = 1)

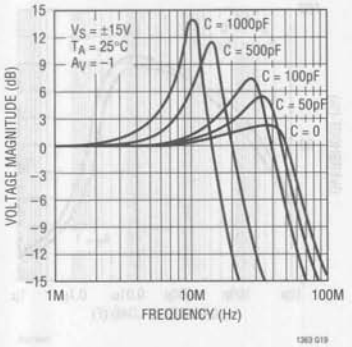


Frequency Response vs Supply Voltage (A_V = –1)

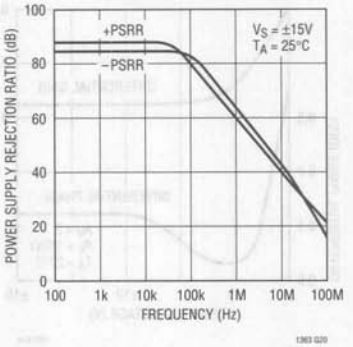


TYPICAL PERFORMANCE CHARACTERISTICS

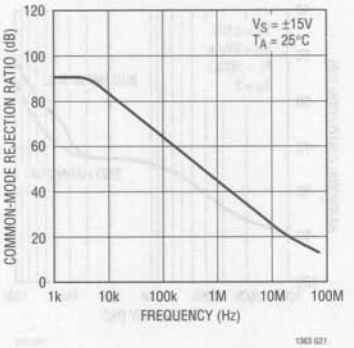
Frequency Response vs Capacitive Load



Power Supply Rejection Ratio vs Frequency

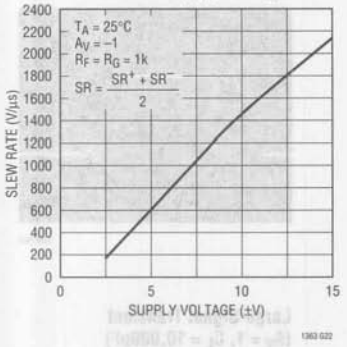


Common-Mode Rejection Ratio vs Frequency

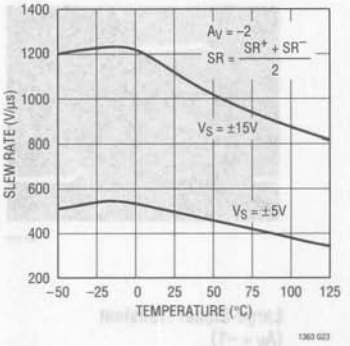


2

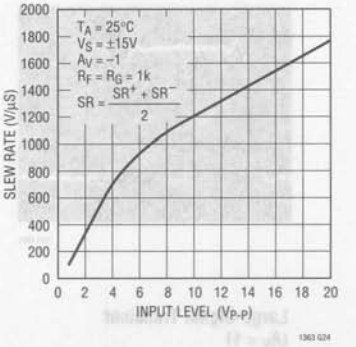
Slew Rate vs Supply Voltage



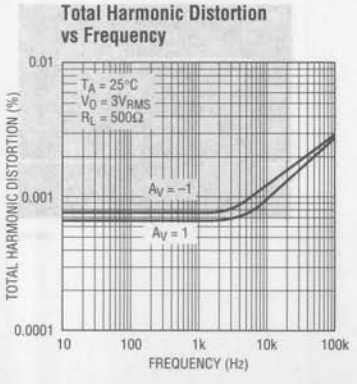
Slew Rate vs Temperature



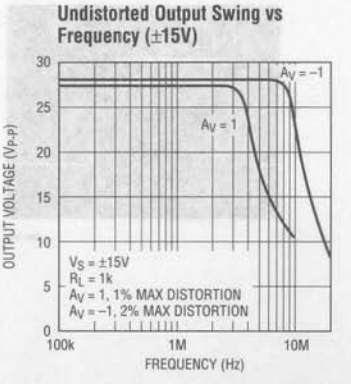
Slew Rate vs Input Level



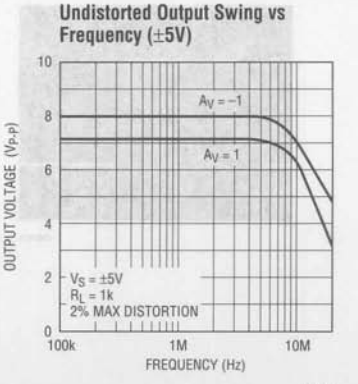
Total Harmonic Distortion vs Frequency



Undistorted Output Swing vs Frequency (±15V)

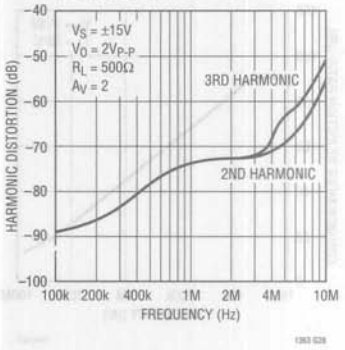


Undistorted Output Swing vs Frequency (±5V)

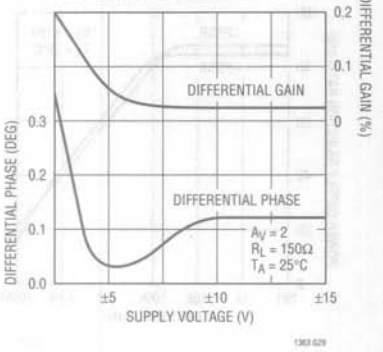


TYPICAL PERFORMANCE CHARACTERISTICS

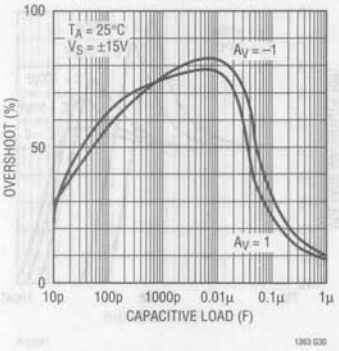
2nd and 3rd Harmonic Distortion vs Frequency



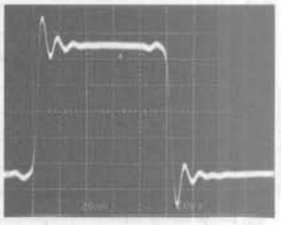
Differential Gain and Phase vs Supply Voltage



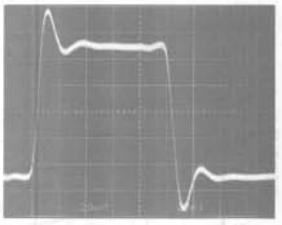
Capacitive Load Handling



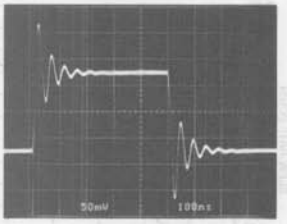
Small-Signal Transient (A_V = 1)



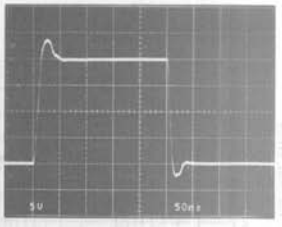
Small-Signal Transient (A_V = –1)



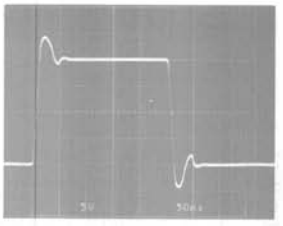
Small-Signal Transient (A_V = –1, C_L = 200pF)



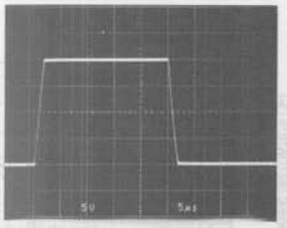
Large-Signal Transient (A_V = 1)



Large-Signal Transient (A_V = –1)



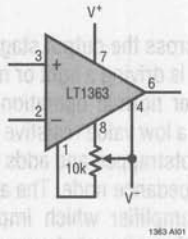
Large-Signal Transient (A_V = 1, C_L = 10,000pF)



APPLICATIONS INFORMATION

The LT1363 may be inserted directly into AD817, AD847, EL2020, EL2044, and LM6361 applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1363 is shown below.

Offset Nulling



Layout and Passive Components

The LT1363 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01μF to 0.1μF). For high drive current applications use low ESR bypass capacitors (1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1363 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 200pF load shows 62% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited to 10V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground. The response of a cable driver in a gain of 2 driving a 75Ω cable is shown on the front page of the data sheet.

Input Considerations

Each of the LT1363 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Single Supply Operation

The LT1363 is specified at ±15V, ±5V, and ±2.5V supplies, but it is also well suited to single supply operation down to a single 5V supply. The symmetrical input common-mode range and output swing make the device well suited for applications with a single supply if the the input and output swing ranges are centered (i.e., a DC bias of 2.5V on the input and the output). For 5V video applications with an assymetrical swing, an offset of 2V on the input works best.

APPLICATIONS INFORMATION

Power Dissipation

The LT1363 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1363CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1363CS8: $T_J = T_A + (P_D \times 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1363CS8 at 70°C, $V_S = \pm 15V$, $R_L = 390\Omega$

$$P_{DMAX} = (30V)(8.7mA) + (7.5V)^2/390\Omega = 405mW$$

$$T_{JMAX} = 70°C + (405mW)(190°C/W) = 147°C$$

Circuit Operation

The LT1363 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1363 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

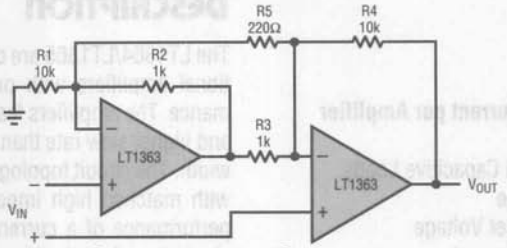
The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Comparison to Current Feedback Amplifiers

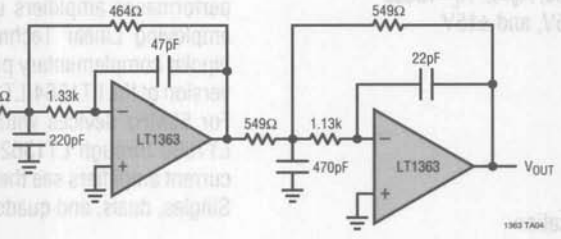
The LT1363 enjoys the high slew rates of Current Feedback Amplifiers (CFAs) while maintaining the characteristics of a true voltage feedback amplifier. The primary differences are that the LT1363 has two high impedance inputs and its closed loop bandwidth decreases as the gain increases. CFAs have a low impedance inverting input and maintain relatively constant bandwidth with increasing gain. The LT1363 can be used in all traditional op amp configurations including integrators and applications such as photodiode amplifiers and I-to-V converters where there may be significant capacitance on the inverting input. The frequency compensation is internal and not dependent on the value of the feedback resistor. For CFAs, the feedback resistance is fixed for a given bandwidth and capacitance on the inverting input can cause peaking or oscillations. The slew rate of the LT1363 in noninverting gain configurations is also superior in most cases.

TYPICAL APPLICATIONS

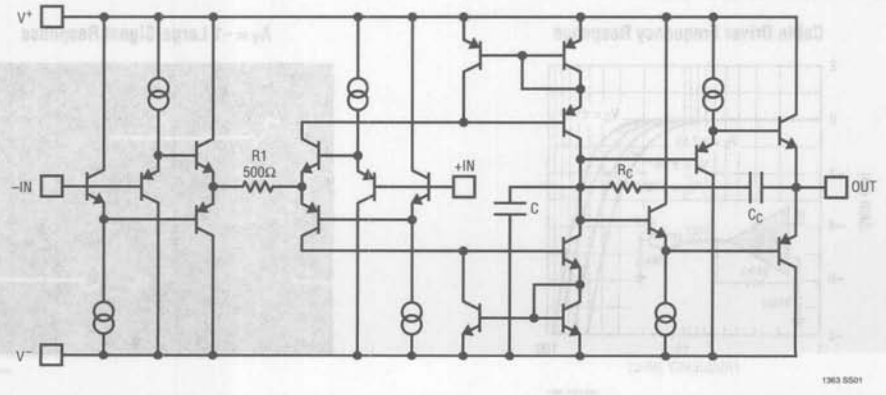
Two Op Amp Instrumentation Amplifier



2MHz, 4th Order Butterworth Filter



SIMPLIFIED SCHEMATIC



Dual and Quad 70MHz, 1000V/µs Op Amps

FEATURES

- **70MHz Gain-Bandwidth**
- **1000V/µs Slew Rate**
- **7.5mA Maximum Supply Current per Amplifier**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 9nV/√Hz Input Noise Voltage
- 1.5mV Maximum Input Offset Voltage
- 2µA Maximum Input Bias Current
- 350nA Maximum Input Offset Current
- 50mA Minimum Output Current
- ±7.5V Minimum Output Swing into 150Ω
- 4.5V/mV Minimum DC Gain, R_L=1k
- 50ns Settling Time to 0.1%, 10V Step
- 0.06% Differential Gain, A_V=2, R_L=150Ω
- 0.04° Differential Phase, A_V=2, R_L=150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

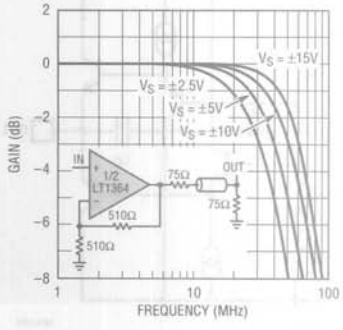
The LT1364/LT1365 are dual and quad high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 150Ω load to ±7.5V with ±15V supplies and to ±3.4V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer or cable driving applications.

The LT1364/LT1365 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1364/LT1365 see the LT1363 data sheet. For 50MHz devices with 4mA supply currents see the LT1360 through LT1362 data sheets. For lower supply current amplifiers see the LT1354 to LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

C-Load is a trademark of Linear Technology Corporation

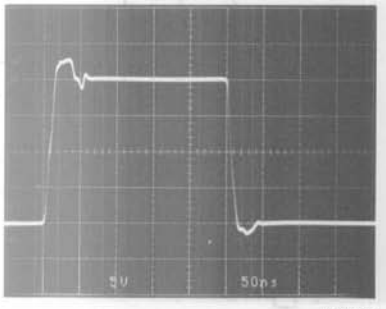
TYPICAL APPLICATION

Cable Driver Frequency Response



1364/1365 TA01

A_V = –1 Large-Signal Response

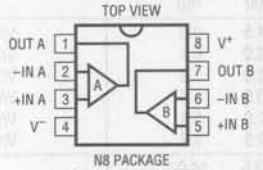


1364/1365 TA02

ABSOLUTE MAXIMUM RATINGS

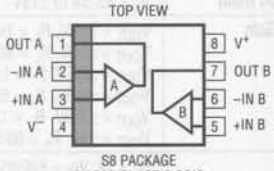
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



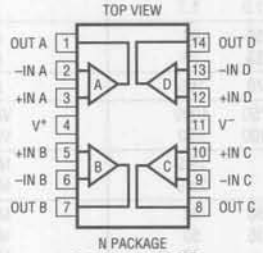
N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1364CN8



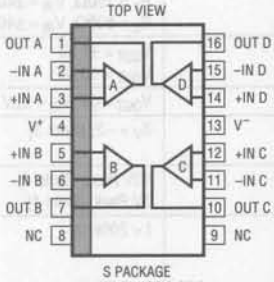
S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1364CS8
S8 PART MARKING
1364



N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1365CN



S PACKAGE
16-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1365CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V		0.5	1.5	mV
			±5V		0.5	1.5	mV
			±2.5V		0.7	1.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		120	350	nA
I_B	Input Bias Current		±2.5V to ±15V		0.6	2.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	12	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range $^+$		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range $^-$		±15V		−13.2	−12.0	V
			±5V		−3.2	−2.5	V
			±2.5V		−0.9	−0.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	84	90		dB
		$V_{CM} = ±2.5V$	±5V	76	81		dB
		$V_{CM} = ±0.5V$	±2.5V	66	71		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		90	100		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$	±15V	4.5	9.0		V/mV
		$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	3.0	6.5		V/mV
		$V_{OUT} = ±7.5V$, $R_L = 150Ω$	±15V	2.0	3.8		V/mV
		$V_{OUT} = ±2.5V$, $R_L = 500Ω$	±5V	3.0	6.4		V/mV
		$V_{OUT} = ±2.5V$, $R_L = 150Ω$	±5V	2.0	5.6		V/mV
		$V_{OUT} = ±1V$, $R_L = 500Ω$	±2.5V	2.5	5.2		V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$	±15V	13.5	14.0		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±15V	13.0	13.7		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±5V	3.5	4.1		±V
		$R_L = 150Ω$, $V_{IN} = ±40mV$	±5V	3.4	3.8		±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	$V_{OUT} = ±7.5V$	±15V	50	60		mA
		$V_{OUT} = ±3.4V$	±5V	23	29		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	70	105		mA
SR	Slew Rate	$A_V = −2$, (Note 3)	±15V	750	1000		V/µs
			±5V	300	450		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)	±15V		15.9		MHz
		3V Peak, (Note 4)	±5V		23.9		MHz
GBW	Gain-Bandwidth	f = 200kHz	±15V	50	70		MHz
			±5V	35	50		MHz
			±2.5V		40		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V		2.6		ns
			±5V		3.6		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		36		%
			±5V		23		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		4.6		ns
			±5V		5.6		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = −1$	±15V		50		ns
		10V Step, 0.01%, $A_V = −1$	±15V		80		ns
		5V Step, 0.1%, $A_V = −1$	±5V		55		ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, $R_L = 150Ω$	±15V		0.03		%
			±5V		0.06		%
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.01		%
			±5V		0.01		%
	Differential Phase	f = 3.58MHz, $A_V = 2$, $R_L = 150Ω$	±15V		0.10		Deg
			±5V		0.04		Deg
		f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V		0.05		Deg
			±5V		0.25		Deg
R_O	Output Resistance	$A_V = 1$, f = 1MHz	±15V		0.7		Ω
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		6.3	7.5	mA
		Each Amplifier	±5V		6.0	7.2	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.0	mV
			±5V	●			2.0	mV
			±2.5V	●			2.2	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			500	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	82			dB
		$V_{CM} = ±2.5V$	±5V	●	74			dB
		$V_{CM} = ±0.5V$	±2.5V	●	64			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	88			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$	±15V	●	3.6			V/mV
		$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	2.4			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 500Ω$	±5V	●	2.4			V/mV
		$V_{OUT} = ±2.5V$, $R_L = 150Ω$	±5V	●	1.5			V/mV
		$V_{OUT} = ±1V$, $R_L = 500Ω$	±2.5V	●	2.0			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$	±15V	●	13.4			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±15V	●	12.8			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±5V	●	3.4			±V
		$R_L = 150Ω$, $V_{IN} = ±40mV$	±5V	●	3.3			±V
		$R_L = 500Ω$, $V_{IN} = ±40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = ±12.8V$	±15V	●	25			mA
		$V_{OUT} = ±3.3V$	±5V	●	22			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	●	55			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	600			V/µs
			±5V	●	225			V/µs
GBW	Gain-Bandwidth	f = 200kHz	±15V	●	44			MHz
			±5V	●	31			MHz
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			8.7	mA
		Each Amplifier	±5V	●			8.4	mA

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)	±15V	●			2.5	mV
			±5V	●			2.5	mV
			±2.5V	●			2.7	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			600	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3.6	µA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±12V$	±15V	●	82			dB
		$V_{CM} = ±2.5V$	±5V	●	74			dB
		$V_{CM} = ±0.5V$	±2.5V	●	64			dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	87			dB

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	1.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	1.0			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	1.3			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.7			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12.7V$	±15V	●	25			mA
		$V_{OUT} = \pm3.2V$	±5V	●	21			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	50			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	550			V/µs
			±5V	●	180			V/µs
GBW	Gain-Bandwidth	f = 200kHz	±15V	●	43			MHz
			±5V	●	30			MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			9.0	mA
		Each Amplifier	±5V	●			8.7	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 3: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

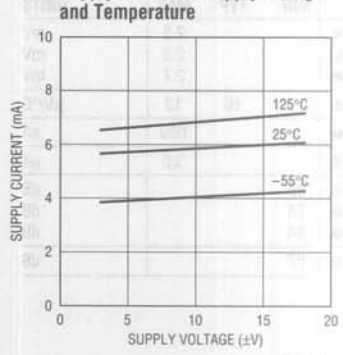
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 5: This parameter is not 100% tested.

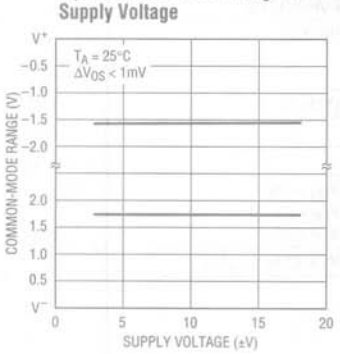
Note 6: The LT1364/LT1365 are not tested and are not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

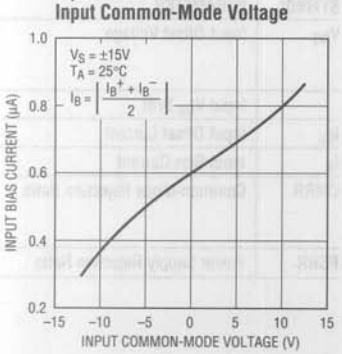
Supply Current vs Supply Voltage and Temperature



Input Common-Mode Range vs Supply Voltage



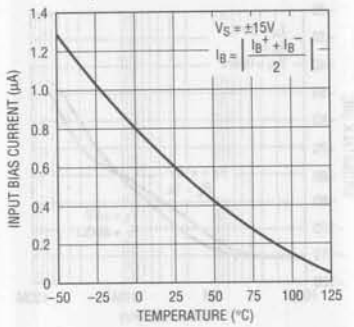
Input Bias Current vs Input Common-Mode Voltage



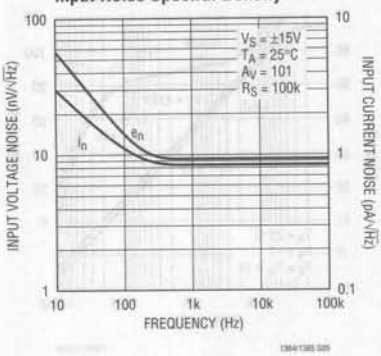
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

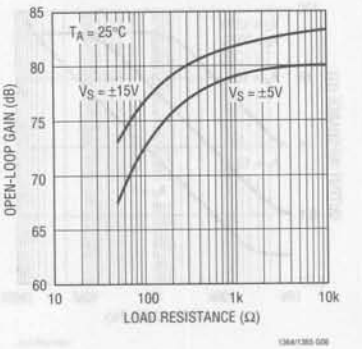
Input Bias Current vs Temperature



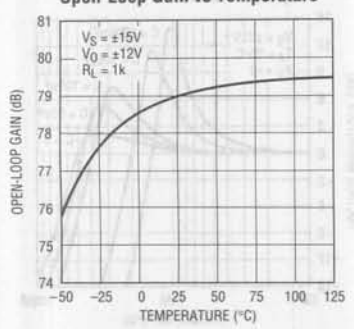
Input Noise Spectral Density



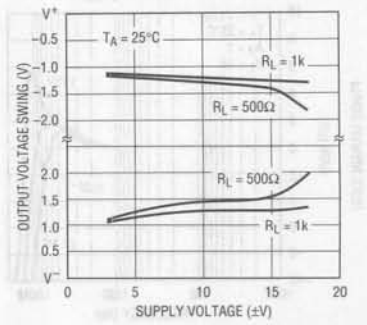
Open-Loop Gain vs Resistive Load



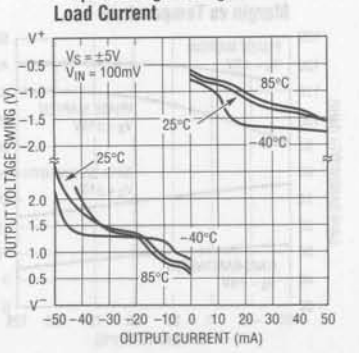
Open-Loop Gain vs Temperature



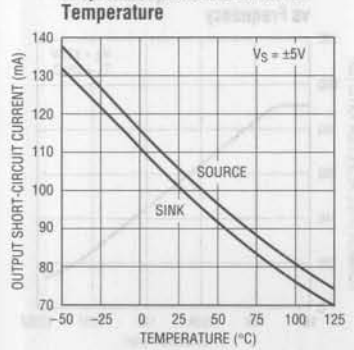
Output Voltage Swing vs Supply Voltage



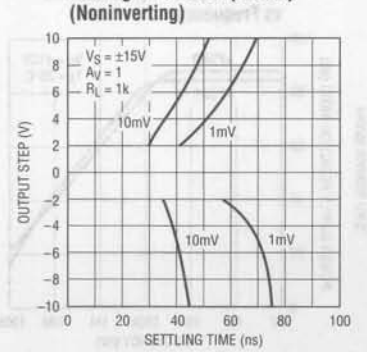
Output Voltage Swing vs Load Current



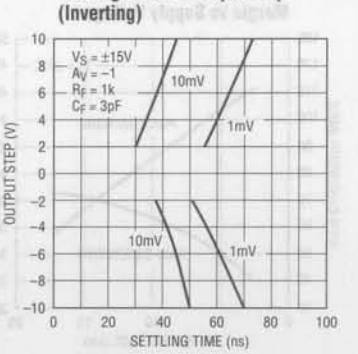
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)

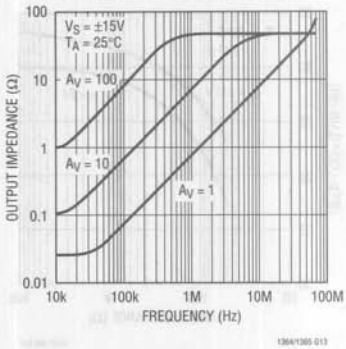


Settling Time vs Output Step (Inverting)

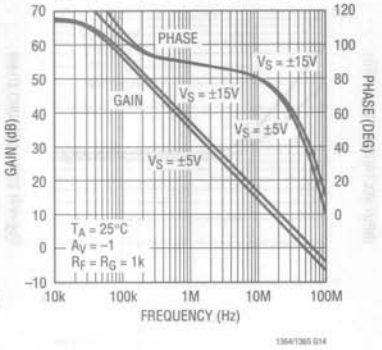


TYPICAL PERFORMANCE CHARACTERISTICS

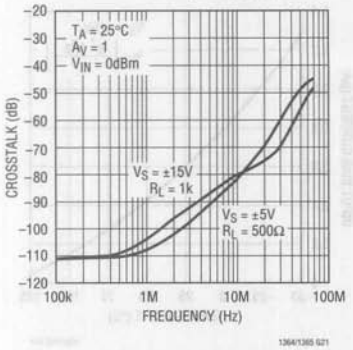
Output Impedance vs Frequency



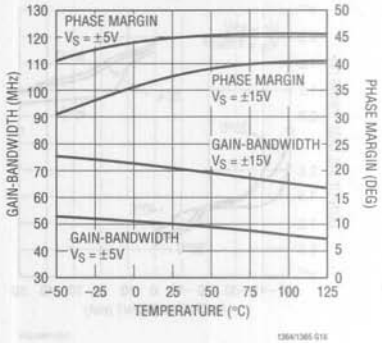
Gain and Phase vs Frequency



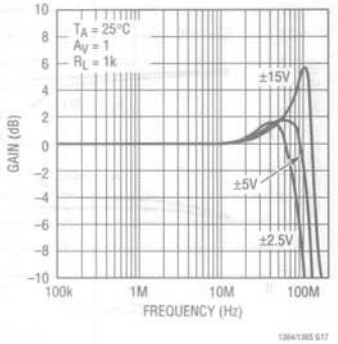
Crosstalk vs Frequency



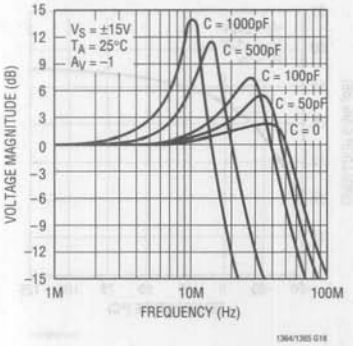
Gain-Bandwidth and Phase Margin vs Temperature



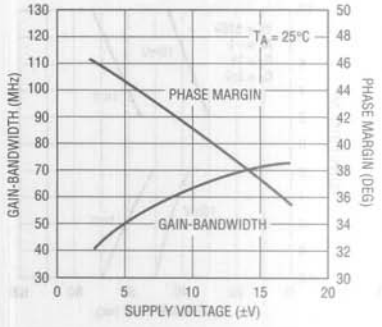
Frequency Response vs Supply Voltage (A_V = 1)



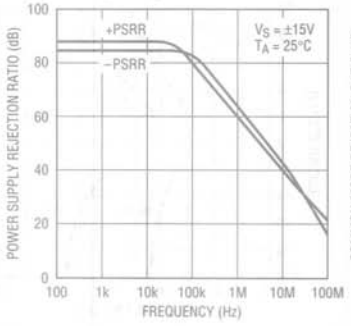
Frequency Response vs Capacitive Load



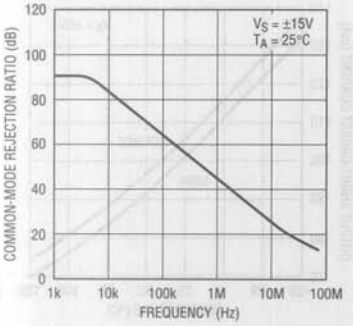
Gain-Bandwidth and Phase Margin vs Supply Voltage



Power Supply Rejection Ratio vs Frequency

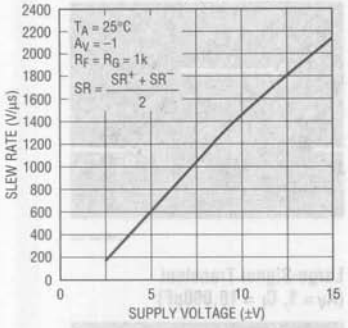


Common-Mode Rejection Ratio vs Frequency

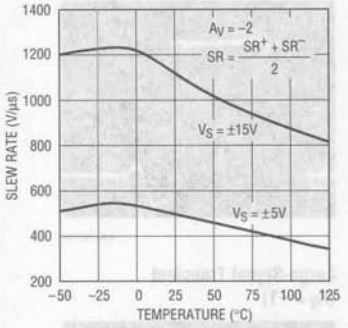


TYPICAL PERFORMANCE CHARACTERISTICS

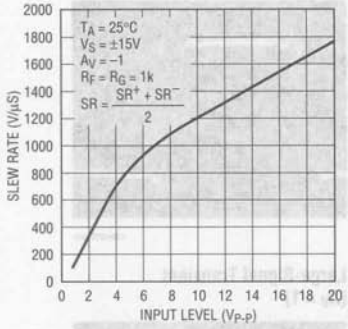
Slew Rate vs Supply Voltage



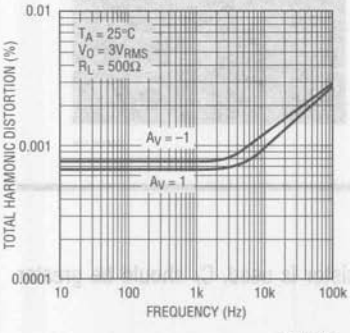
Slew Rate vs Temperature



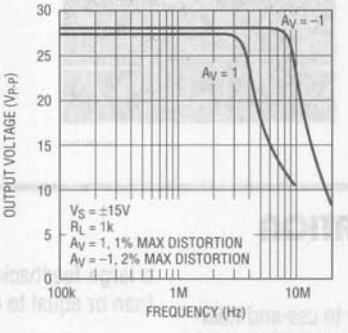
Slew Rate vs Input Level



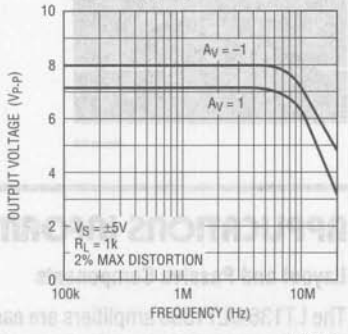
Total Harmonic Distortion vs Frequency



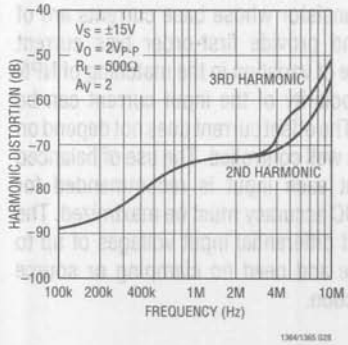
Undistorted Output Swing vs Frequency (±15V)



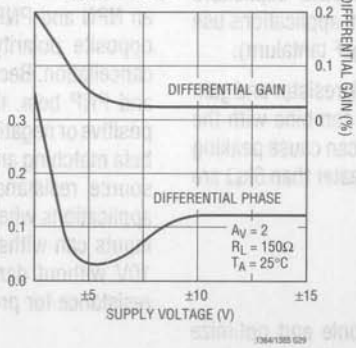
Undistorted Output Swing vs Frequency (±5V)



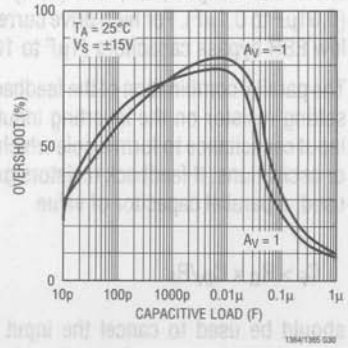
2nd and 3rd Harmonic Distortion vs Frequency



Differential Gain and Phase vs Supply Voltage



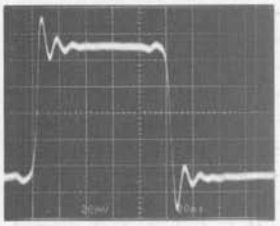
Capacitive Load Handling



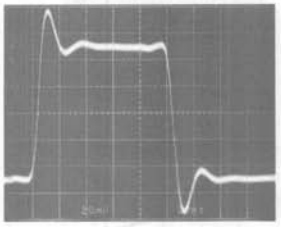
2

TYPICAL PERFORMANCE CHARACTERISTICS

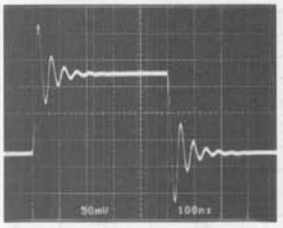
Small-Signal Transient ($A_V = 1$)



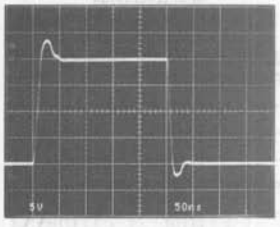
Small-Signal Transient ($A_V = -1$)



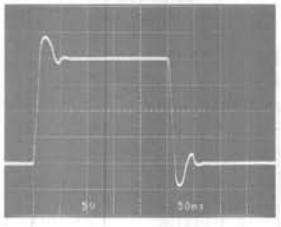
Small-Signal Transient ($A_V = -1$, $C_L = 200pF$)



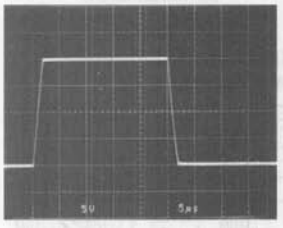
Large-Signal Transient ($A_V = 1$)



Large-Signal Transient ($A_V = -1$)



Large-Signal Transient ($A_V = 1$, $C_L = 10,000pF$)



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1364/LT1365 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Input Considerations

Each of the LT1364/LT1365 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

APPLICATIONS INFORMATION

Capacitive Loading

The LT1364/LT1365 are stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small signal response with 200pF load shows 62% peaking. The large signal response shows the output slew rate being limited to 10V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Circuit Operation

The LT1364/LT1365 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1364/LT1365 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1364/LT1365 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1364CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1364CS8: $T_J = T_A + (P_D \times 190°C/W)$
LT1365CN: $T_J = T_A + (P_D \times 110°C/W)$
LT1365CS: $T_J = T_A + (P_D \times 150°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

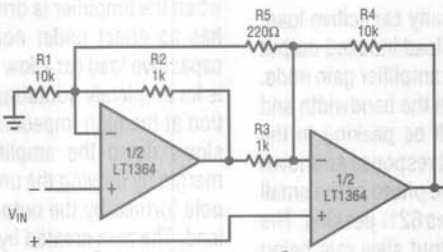
Example: LT1365 in S16 at 70°C, $V_S = \pm 5V$, $R_L = 150\Omega$

$$P_{DMAX} = (10V)(8.4mA) + (2.5V)^2/150\Omega = 126mW$$

$$T_{JMAX} = 70°C + (4 \times 126mW)(150°C/W) = 145°C$$

TYPICAL APPLICATIONS

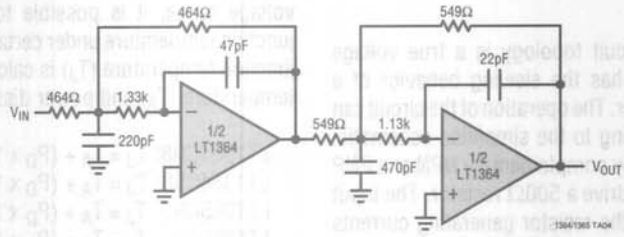
Two Op Amp Instrumentation Amplifier



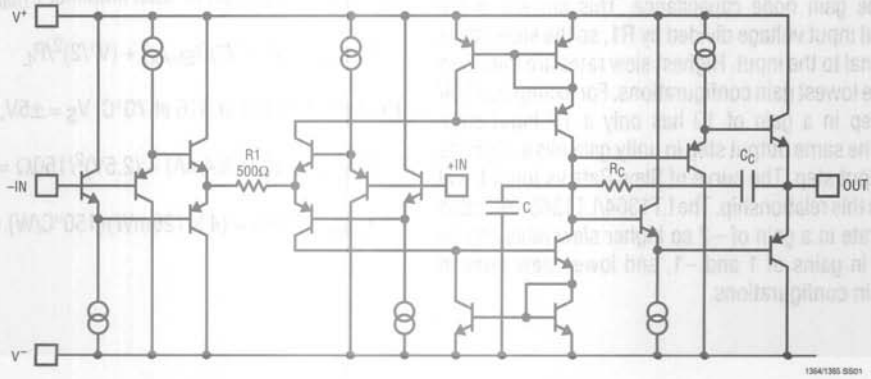
$$GAIN = \left[\frac{R4}{R3}\right]\left[1+\left(\frac{1}{2}\right)\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{(R2+R3)}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 700kHz

2MHz, 4th Order Butterworth Filter



SIMPLIFIED SCHEMATIC



LINEAR TECHNOLOGY

SECTION 2—AMPLIFIERS

ZERO DRIFT OPERATIONAL AMPLIFIERS

LTC1151, Dual ±15V Zero-Drift Operational Amplifier 2-356
LTC1152, Rail-to-Rail Input Rail-to-Rail Output Zero-Drift Op Amp 13-7
LTC1250, Very Low Noise Zero-Drift Bridge Amplifier 2-364

LINEAR TECHNOLOGY

LTC1151

Dual ±15V Zero-Drift Operational Amplifier

FEATURES

- Maximum Offset Voltage Drift: 0.05μV/°C
- High Voltage Operation: ±18V
- No External Components Required
- Maximum Offset Voltage: 5μV
- Low Noise: 1.5μV$_{P-P}$ (0.1Hz to 10Hz)
- Minimum Voltage Gain: 125dB
- Minimum CMRR: 106dB
- Minimum PSRR: 110dB
- Low Supply Current: 0.9mA/Amplifier
- Single Supply Operation: 4.75V to 36V
- Input Common-Mode Range Includes Ground
- Typical Overload Recovery Time: 20ms

APPLICATIONS

- Strain Gauge Amplifiers
- Instrumentation Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

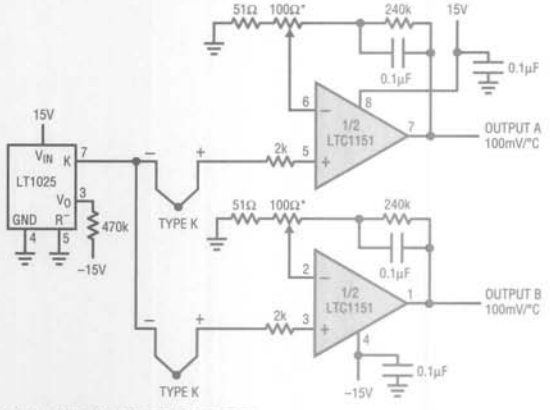
The LTC1151 is a high voltage, high performance dual zero-drift operational amplifier. The two sample-and-hold capacitors per amplifier required externally by other chopper amplifiers are integrated on-chip. The LTC1151 also incorporates proprietary high voltage CMOS structures which allow operation at up to 36V total supply voltage.

The LTC1151 has a typical offset voltage of 0.5μV, drift of 0.01μV/°C, 0.1Hz to 10Hz input noise voltage of 1.5μV$_{P-P}$, and a typical voltage gain of 140dB. It has a slew rate of 3V/μs and a gain-bandwidth product of 2.5MHz with a supply current of 0.9mA per amplifier. Overload recovery times from positive and negative saturation are 3ms and 20ms, respectively.

The LTC1151 is available in a standard 8-lead plastic DIP package as well as a 16-lead wide body SO. The LTC1151 is pin compatible with industry-standard dual op amps and runs from standard ±15V supplies, allowing it to plug in to most standard bipolar op amp sockets while offering significant improvement in DC performance.

TYPICAL APPLICATION

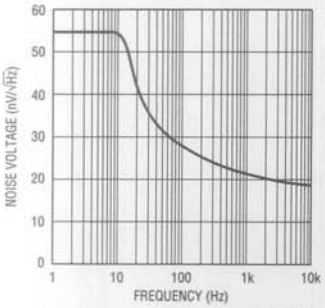
±15V Dual Thermocouple Amplifier



* FULL SCALE TRIM: TRIM FOR 10.0V OUTPUT WITH THERMOCOUPLE AT 100°C

1151 TA01

Noise Spectrum



1151 TA02

LINEAR TECHNOLOGY

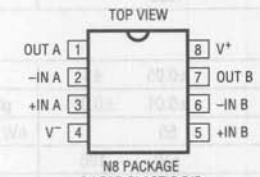
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration ..... Indefinite
Burn-In Voltage 36V

Operating Temperature Range
LTC1151C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

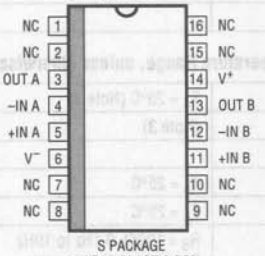


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1151CN8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 200°C/W

ORDER PART NUMBER

LTC1151CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1151C MIN	LTC1151C TYP	LTC1151C MAX	UNITS
Input Offset Voltage	T_A = 25°C (Note 3)			±0.5	±5	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50		nV/√mo
Input Offset Current	T_A = 25°C			±20	±200	pA
		●			±0.5	nA
Input Bias Current	T_A = 25°C			±15	±100	pA
		●			±0.5	nA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz			1.5		μV_{P-P}
	R_S = 100Ω, 0.1Hz to 1Hz			0.5		μV_{P-P}
Input Noise Current	f = 10Hz (Note 4)			2.2		fA/√Hz
Input Voltage Range	Positive	●	12	13.2		V
	Negative	●	–15	–15.3		V
Common-Mode Rejection Ratio	V_{CM} = V^- to 12V	●	106	130		dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	110	130		dB
Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = ±10V	●	125	140		dB

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1151C MIN	TYP	MAX	UNITS
Maximum Output Voltage Swing	R_L = 10k, T_A = 25°C		±13.5	±14.50		V
	R_L = 10k	●	+10.5/–13.5			V
	R_L = 100k			±14.95		V
Slew Rate	R_L = 10k, C_L = 50pF			2.5		V/µs
Gain-Bandwidth Product				2		MHz
Supply Current per Amplifier	No Load, T_A = 25°C			0.9	1.5	mA
	No Load	●			2.0	mA
Internal Sampling Frequency				1000		Hz

V_S = 5V, T_A = Operating Temperature Range, unless otherwise specified.

Input Offset Voltage	T_A = 25°C (Note 3)			±0.05	±5	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50		nV/√mo
Input Offset Current	T_A = 25°C			±10	100	pA
Input Bias Current	T_A = 25°C			±5	50	pA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz			2.0		μV_{P-P}
	R_S = 100Ω, 0.1Hz to 1Hz			0.7		μV_{P-P}
Input Noise Current	f = 10Hz (Note 4)			1.3		fA/√Hz
Input Voltage Range	Positive		2.7	3.2		V
	Negative		0	–0.3		V
Common-Mode Rejection Ratio	V_{CM} = 0V to 2.7V		110			dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	110	130		dB
Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.3V to 4.5V	●	115	140		dB
Maximum Output Voltage Swing	R_L = 10k to GND			4.85		V
	R_L = 100k to GND			4.97		V
Slew Rate	R_L = 10k, C_L = 50pF			1.5		V/µs
Gain Bandwidth Product				1.5		MHz
Supply Current per Amplifier	No Load, T_A = 25°C			0.5	1.0	mA
		●			1.5	mA
Internal Sampling Frequency				750		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1151.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

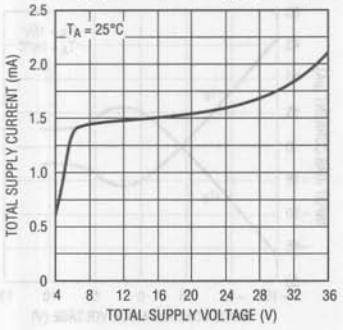
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \bullet I_b)}$$

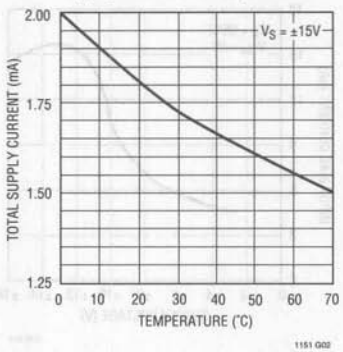
where $q = 1.6 \times 10^{-19}$ Coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

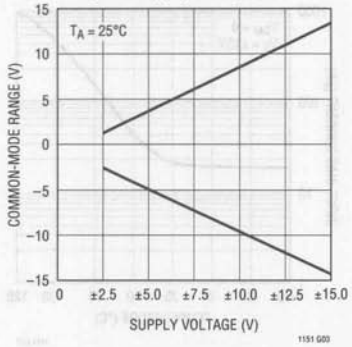
Supply Current vs Supply Voltage



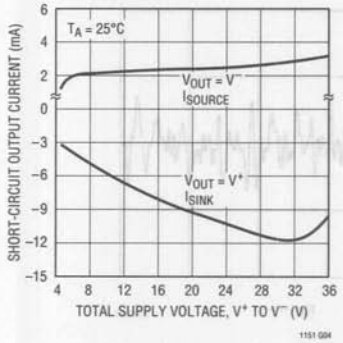
Supply Current vs Temperature



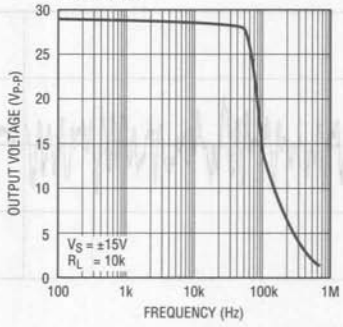
Common-Mode Input Voltage Range vs Supply Voltage



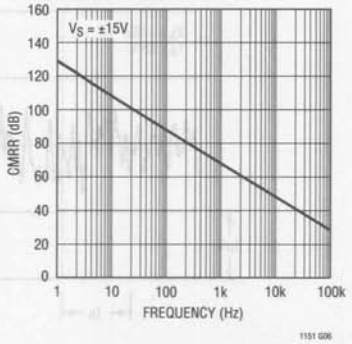
Output Short-Circuit Current vs Supply Voltage



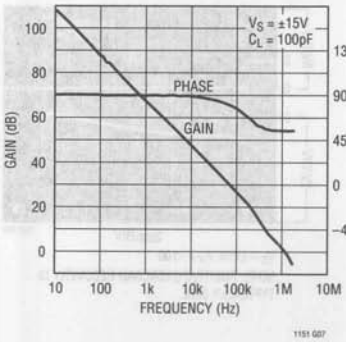
Undistorted Output Swing vs Frequency



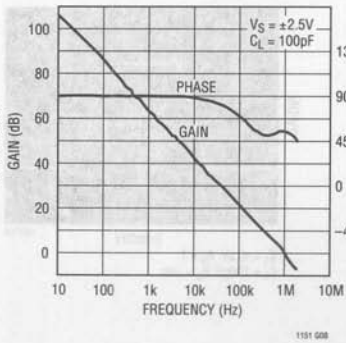
CMRR vs Frequency



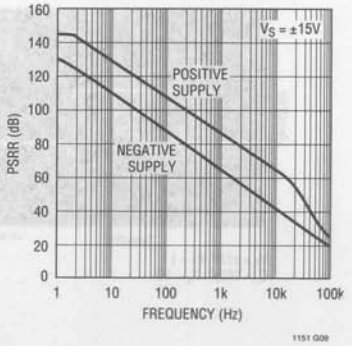
Gain and Phase vs Frequency



Gain and Phase vs Frequency



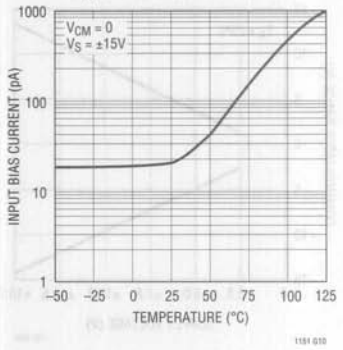
PSRR vs Frequency



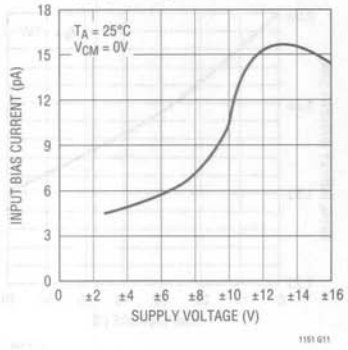
2

TYPICAL PERFORMANCE CHARACTERISTICS

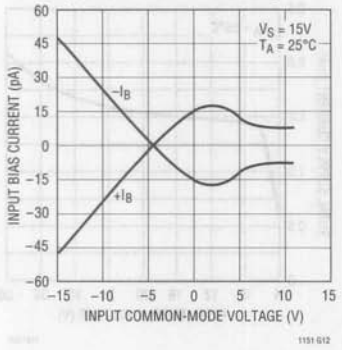
Input Bias Current Magnitude vs Temperature



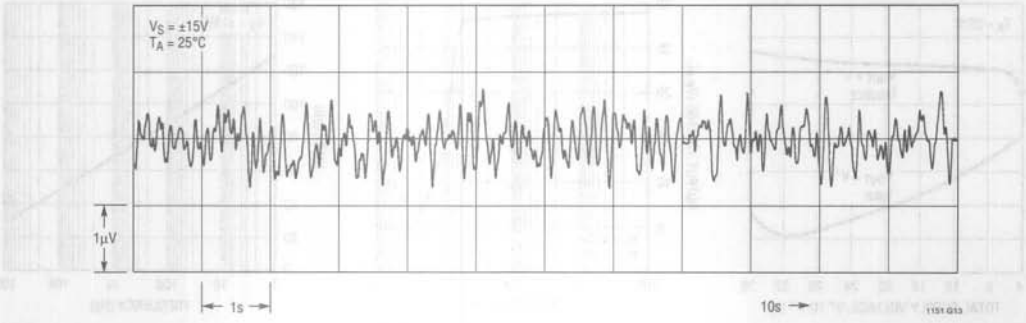
Input Bias Current Magnitude vs Supply Voltage



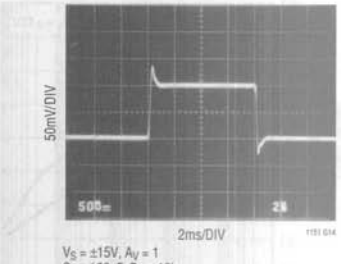
Input Bias Current vs Input Common-Mode Voltage



0.1Hz to 10Hz Noise

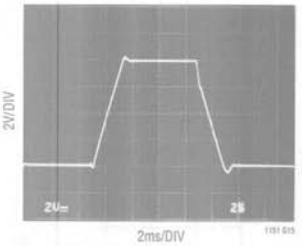


Small-Signal Transient Response



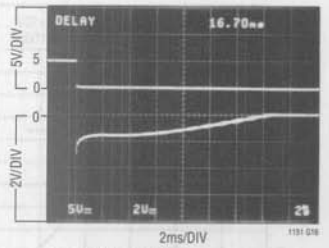
VS = ±15V, AV = 1
CL = 100pF, RL = 10k

Large-Signal Transient Response



VS = ±15V, AV = 1
CL = 100pF, RL = 10k

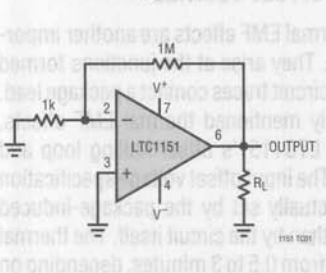
Negative Overload Recovery



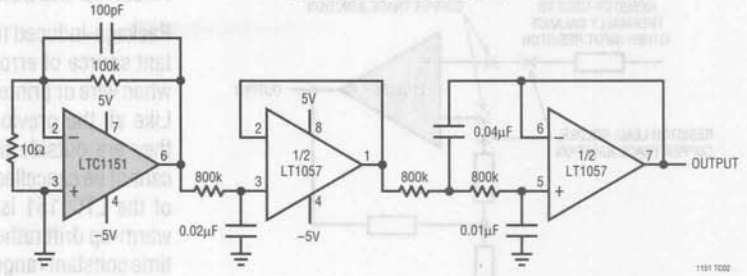
VS = ±15V, AV = –100
NOTE: POSITIVE OVERLOAD RECOVERY IS TYPICALLY 3ms.

TEST CIRCUITS

Offset Voltage Test Circuit



DC-10Hz Noise Test Circuit



APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1151 proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary, particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in noninverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1151's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C; four times the maximum drift specification of the LTC1151.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 1 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

APPLICATIONS INFORMATION

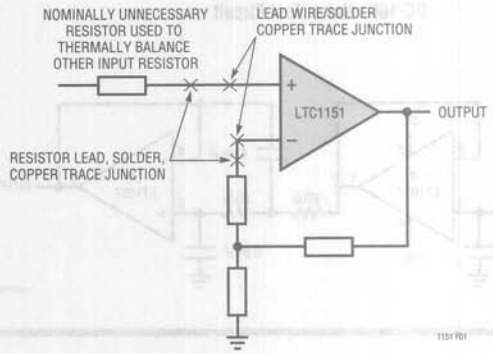


Figure 1. Extra Resistors Cancel Thermal EMF

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

RESISTOR TYPE	THERMAL EMF/°C GRADIENT
Tin Oxide	>1mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
Wire Wound Evenohm, Manganin	~2μV/°C

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. They arise at the junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, they are outside the LTC1151's offset nulling loop and cannot be cancelled. The input offset voltage specification of the LTC1151 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

ALIASING

Like all sampled data systems, the LTC1151 exhibits aliasing behavior at input frequencies near the sampling frequency. The LTC1151 includes a high frequency correction loop which minimizes this effect. As a result, aliasing is not a problem for many applications.

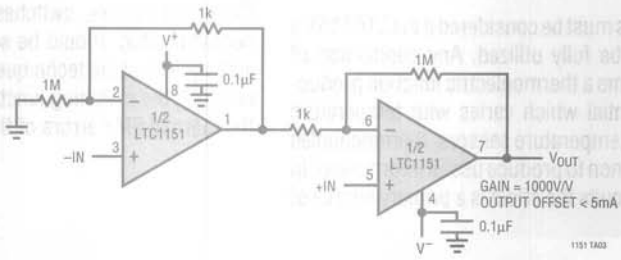
For a complete discussion of the correction circuitry and aliasing behavior, please refer to the LTC1051/LTC1053 data sheet.

LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1151 is typically 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation at minimum TTL supply voltage of 4.75V.

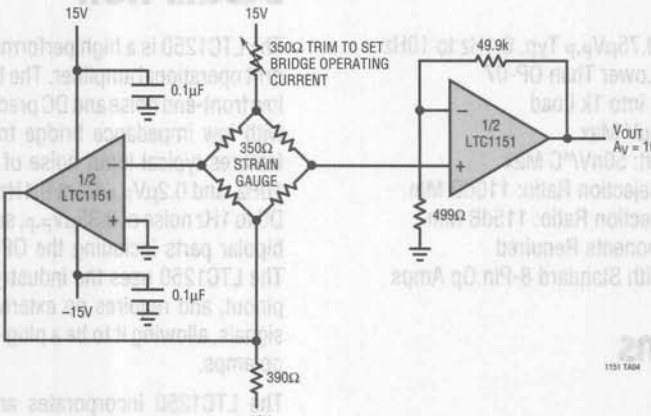
TYPICAL APPLICATIONS

High Voltage Instrumentation Amplifier



TYPICAL APPLICATIONS

Bridge Amplifier with Active Common-Mode Suppression



Very Low Noise Zero-Drift Bridge Amplifier

FEATURES

- Very Low Noise: 0.75μV$_{P-P}$ Typ, 0.1Hz to 10Hz
- DC to 1Hz Noise Lower Than OP-07
- Full Output Swing into 1k Load
- Offset Voltage: 10μV Max
- Offset Voltage Drift: 50nV/°C Max
- Common-Mode Rejection Ratio: 110dB Min
- Power Supply Rejection Ratio: 115dB Min
- No External Components Required
- Pin-Compatible with Standard 8-Pin Op Amps

APPLICATIONS

- Electronic Scales
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- High Resolution Data Acquisition
- Low Noise Transducers
- Instrumentation Amplifiers

DESCRIPTION

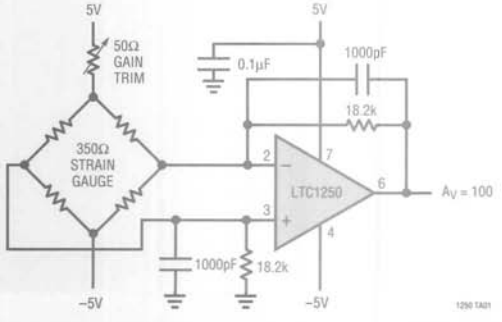
The LTC1250 is a high performance, very low noise zero-drift operational amplifier. The LTC1250's combination of low front-end noise and DC precision makes it ideal for use with low impedance bridge transducers. The LTC1250 features typical input noise of 0.75μV$_{P-P}$ from 0.1Hz to 10Hz, and 0.2μV$_{P-P}$ from 0.1Hz to 1Hz. The LTC1250 has DC to 1Hz noise of 0.35μV$_{P-P}$, surpassing that of low noise bipolar parts including the OP-07, OP-77, and LT1012. The LTC1250 uses the industry-standard single op amp pinout, and requires no external components or nulling signals, allowing it to be a plug-in replacement for bipolar op amps.

The LTC1250 incorporates an improved output stage capable of driving 4.3V into a 1k load with a single 5V supply; it will swing ±4.9V into 5k with ±5V supplies. The input common mode range includes ground with single power supply voltages above 12V. Supply current is 3mA with a ±5V supply, and overload recovery times from positive and negative saturation are 0.5ms and 1.5ms, respectively. The internal nulling clock is set at 5kHz for optimum low frequency noise and offset drift; no external connections are necessary.

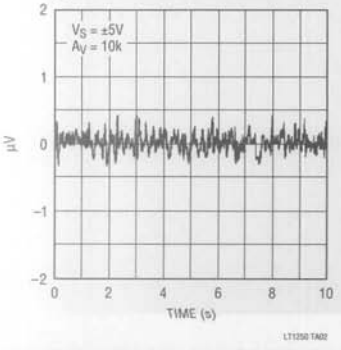
The LTC1250 is available in standard 8-pin ceramic and plastic DIPs, as well as an 8-pin SOIC package.

TYPICAL APPLICATION

Differential Bridge Amplifier



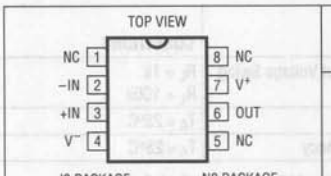
Input Referred Noise 0.1Hz to 10Hz



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LTC1250M ..... –55°C to 125°C
LTC1250C ..... 0°C TO 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°CW (J8)
T_{JMAX} = 110°C, θ_{JA} = 130°CW (N8)
T_{JMAX} = 110°C, θ_{JA} = 200°CW (S8)

ORDER PART NUMBER
LTC1250MJ8 LTC1250CJ8 LTC1250CN8 LTC1250CS8
S8 PART MARKING
1250

Consult factory for Industrial grade parts.

2

ELECTRICAL CHARACTERISTICS

V_{IN} = ±5V, T_A = Operating Temperature Range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±5	±10		±5	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
	Long Term Offset Drift				50			50		nV/√Mo
e_n	Input Noise Voltage (Note 2)	T_A = 25°C, 0.1Hz to 10Hz T_A = 25°C, 0.1Hz to 1Hz			0.75 0.2	1.0		0.75 0.2	1.0	μV_{P-P} μV_{P-P}
i_n	Input Noise Current	f = 10Hz			4.0			4.0		fA/√Hz
I_B	Input Bias Current	T_A = 25°C (Note 3)	 ●		±50	±150 ±950		±50	±200 ±450	pA pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 3)	 ●		±100	±300 ±500		±100	±400 ±500	pA pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = –4V to 3V	●	110	130		110	130		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	●	115	130		115	130		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = ±4V	●	125	170		125	170		dB
	Maximum Output Voltage Swing	R_L = 1k R_L = 100k	●	±4.0	4.3/–4.7 ±4.92		±4.0	4.3/–4.7 ±4.95		V V
SR	Slew Rate	R_L = 10k, C_L = 50pF			10			10		V/µs
GBW	Gain-Bandwidth Product				1.5			1.5		MHz
I_S	Supply Current	No Load, T_A = 25°C	 ●		3.0	4.0 7.0		3.0	4.0 5.0	mA mA
f_S	Internal Sampling Frequency	T_A = 25°C			4.75			4.75		kHz

V_{IN} = 5V, T_A = Operating Temperature Range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±2	±5		±2	±5	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
e_n	Input Noise Voltage (Note 2)	T_A = 25°C, 0.1Hz to 10Hz T_A = 25°C, 0.1Hz to 1Hz			1.0 0.3			1.0 0.3		μV_{P-P} μV_{P-P}
I_B	Input Bias Current	T_A = 25°C (Note 3)			±20	±100		±20	±100	pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 3)			±40	±200		±40	±200	pA

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = Operating Temperature Range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
	Maximum Output Voltage Swing	R_L = 1k	4.0	4.3		4.0	4.3		V
		R_L = 100k		4.95			4.95		V
I_S	Supply Current	T_A = 25°C		1.8	2.5		1.8	2.5	mA
f_S	Sampling Frequency	T_A = 25°C		3			3		kHz

The ● denotes specifications which apply over the full operating temperature range.

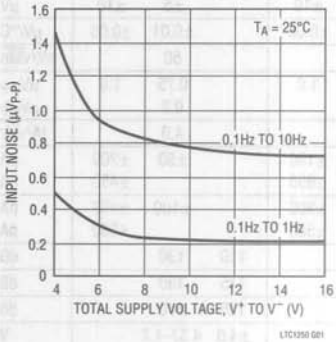
Note 1: These parametes are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

Note 2: 0.1Hz to 10Hz noise is specified DC coupled in a 10s window; 0.1Hz to 1Hz noise is specified in a 100s window with an RC high-pass filter at 0.1Hz. The LTC1250 is sample tested for noise; for 100% tested parts contact LTC Marketing Dept.

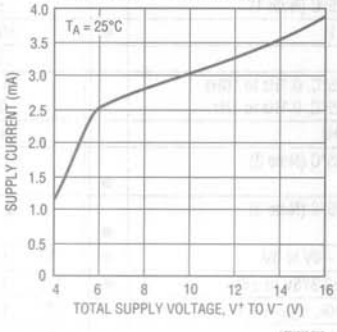
Note 3: At T ≤ 0°C these parameters are guaranteed by design and not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

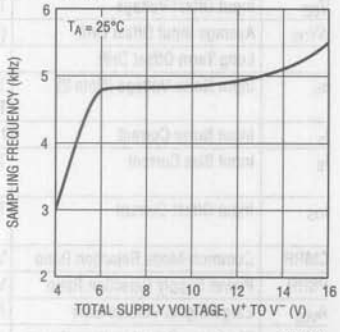
Input Noise vs Supply Voltage



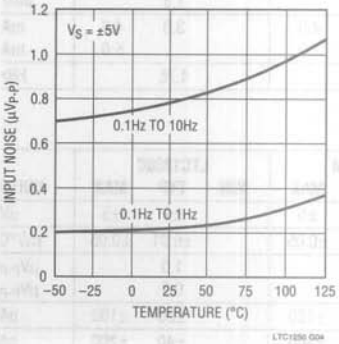
Supply Current vs Supply Voltage



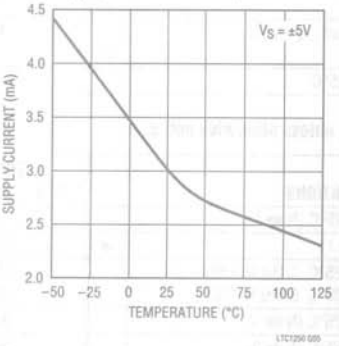
Sampling Frequency vs Supply Voltage



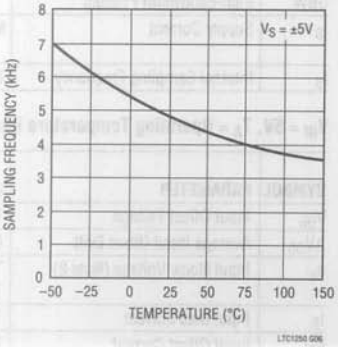
Input Noise vs Temperature



Supply Current vs Temperature

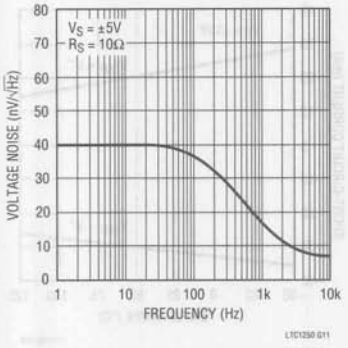


Sampling Frequency vs Temperature

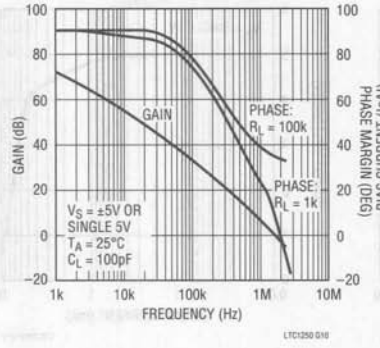


TYPICAL PERFORMANCE CHARACTERISTICS

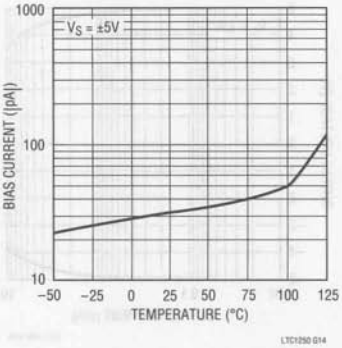
Voltage Noise vs Frequency



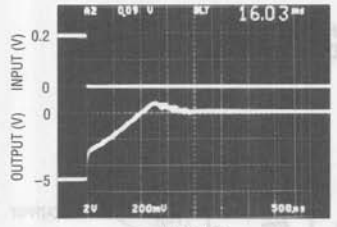
Gain/Phase vs Frequency



Bias Current (Magnitude) vs Temperature

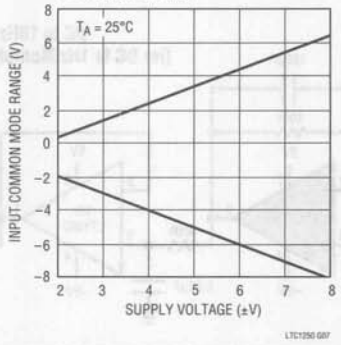


Overload Recovery

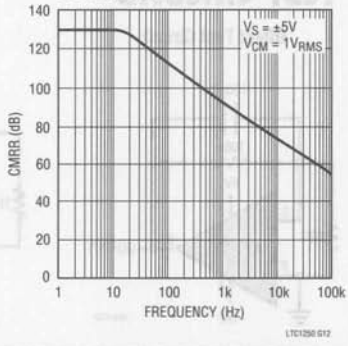


A_V = 100, R_L = 100k, C_L = 50pF, V_S = ±5V

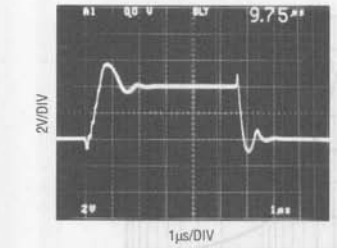
Common-Mode Input Range vs Supply Voltage



Common-Mode Rejection Ratio vs Frequency

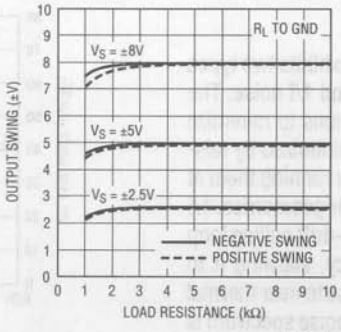


Transient Response

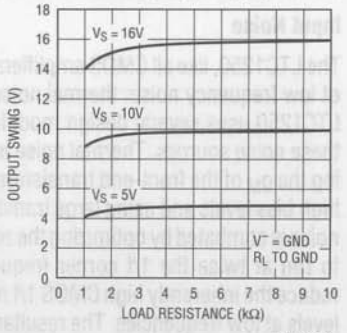


A_V = 1, R_L = 100k, C_L = 50pF, V_S = ±5V

Output Swing vs Load Resistance, Dual Supplies



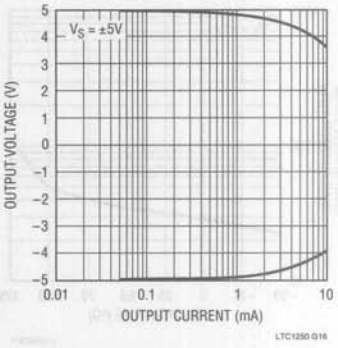
Output Voltage Swing vs Load Resistance, Single Supply



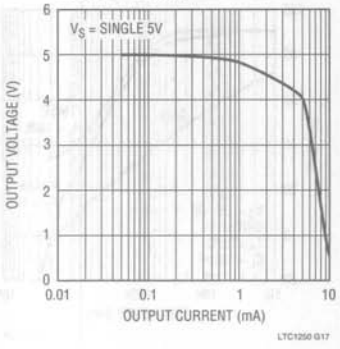
2

TYPICAL PERFORMANCE CHARACTERISTICS

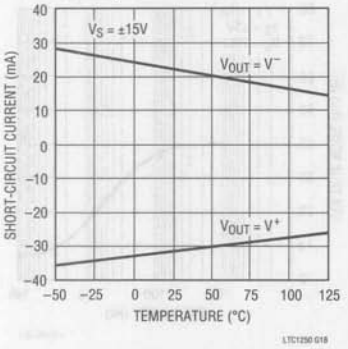
Output Swing vs Output Current, ±5V Supply



Output Swing vs Output Current, Single 5V Supply

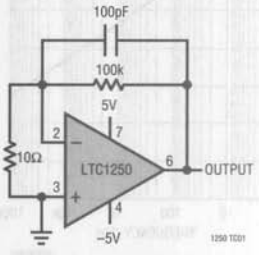


Short-Circuit Current vs Temperature

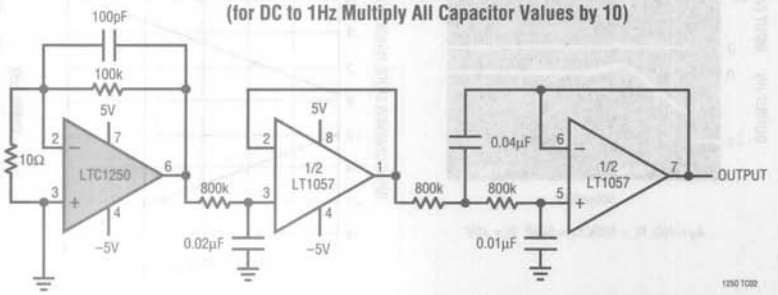


TEST CIRCUITS

Offset Test Circuit



DC to 10Hz Noise Test Circuit (for DC to 1Hz Multiply All Capacitor Values by 10)



APPLICATIONS INFORMATION

Input Noise

The LTC1250, like all CMOS amplifiers, exhibits two types of low frequency noise: thermal noise and 1/f noise. The LTC1250 uses several design modifications to minimize these noise sources. Thermal noise is minimized by raising the g_M of the front-end transistors by running them at high bias levels and using large transistor geometries. 1/f noise is combated by optimizing the zero-drift nulling loop to run at twice the 1/f corner frequency, allowing it to reduce the inherently high CMOS 1/f noise to near thermal levels at low frequencies. The resultant noise spectrum is quite low at frequencies below the internal 5kHz clock

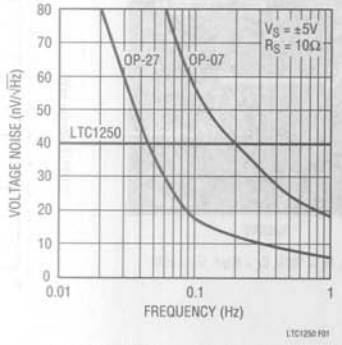


Figure 1. Voltage Noise vs Frequency

APPLICATIONS INFORMATION

frequency, approaching the best bipolar op amps at 10Hz and surpassing them below 1Hz (Figure 1). All this is accomplished in an industry-standard pinout; the LTC1250 requires no external capacitors, no nulling or clock signals, and conforms to industry-standard 8-pin DIP and 8-pin SOIC packages.

Input Capacitance and Compensation

The large input transistors create a parasitic 55pF capacitance from each input to V^+. This input capacitance will react with the external feedback resistors to form a pole which can affect amplifier stability. In low gain, high impedance configurations, the pole can land below the unity-gain frequency of the feedback network and degrade phase margin, causing ringing, oscillation, and other unpleasantness. This is true of any op amp, however, the 55pF capacitance at the LTC1250's inputs can affect stability with a feedback network impedance as low as 1.9k. This effect can be eliminated by adding a capacitor across the feedback resistor, adding a zero which cancels the input pole (Figure 2). The value of this capacitor should be:

$$C_F \geq \frac{55pF}{A_V}$$

where A_V = closed-loop gain. Note that C_F is not dependent on the value of R_F. Circuits with higher gain ($A_V > 50$) or low loop impedance should not require C_F for stability.

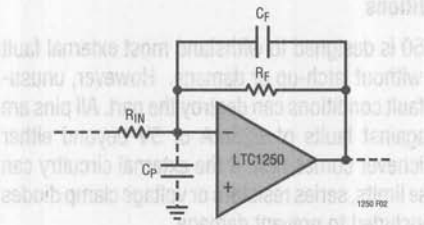


Figure 2. C_F Cancels Phase Shift Due to Parasitic C_P

Larger values of C_F, commonly used in band-limited DC circuits, may actually increase low frequency noise. The nulling circuitry in the LTC1250 closes a loop that includes the external feedback network during part of its cycle. This loop must settle to its final value within 150µs or it will not fully cancel the 1/f noise spectrum and the low frequency noise of the part will rise. If the loop is underdamped (large R_F, no C_F) it will ring for more than 150µs and the noise and offset will suffer.

The solution is to add C_F as above but beware! Too large a value of C_F will overdamp the loop, again preventing it from reaching a final value by the 150µs deadline. This condition doesn't affect the LTC1250's offset or output stability, but 1/f noise begins to rise. As a rule of thumb, the R_FC_F feedback pole should be ≥ 7kHz (1/150µs, the frequency at which the loop settles) for best 1/f performance; values between 100pF and 500pF work well with feedback resistors below 100k. This ensures adequate gain at 7kHz for the LTC1250 to properly null. High value feedback resistors (above 1M) may require experimentation to find the correct value because parasitics, both in the LTC1250 and on the PC board, play an increasing role. Low value resistors (below 5k) may not require a capacitor at all.

Input Bias Current

The inputs of the LTC1250, like all zero-drift op amps, draw only small switching spikes of AC bias current; DC leakage current is negligible except at very high temperatures. The large front-end transistors cause switching spikes 3 to 4 times greater than standard zero-drift op amps: the ±50pA bias current spec is still many times better than most bipolar parts. The spikes don't match from one input pin to the other, and are sometimes (but not always) of opposite polarity. As a result, matching the impedances at the inputs (Figure 3) will not cancel the bias current, and may cause additional errors. Don't do it.

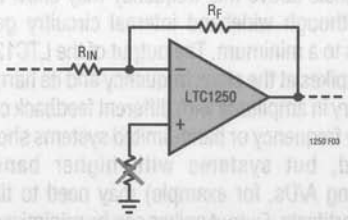


Figure 3. Extra Resistor Will *Not* Cancel Bias Current Errors

APPLICATIONS INFORMATION

Output Drive

The LTC1250 includes an enhanced output stage which provides nearly symmetrical output source/sink currents. This output is capable of swinging a minimum of ±4V into a 1k load with ±5V supplies, and can sink or source >20mA into low impedance loads. Lightly loaded ($R_L \geq 100k$), the LTC1250 will swing to within millivolts of either rail. In single supply applications, it will typically swing 4.3V into a 1k load with a 5V supply.

Minimizing External Errors

The input noise, offset voltage, and bias current specs for the LTC1250 are all well below the levels of circuit board parasitics. Thermocouples between the copper pins of the LTC1250 and the tin/lead solder used to connect them can overwhelm the offset voltage of the LTC1250, especially if a soldering iron has been around recently. Note also that when the LTC1250's output is heavily loaded, the chip may dissipate substantial power, raising the temperature of the package and aggravating thermocouples at the inputs. Although the LTC1250 will maintain its specified accuracy under these conditions, care must be taken in the layout to prevent or compensate circuit errors. Be especially careful of air currents when measuring low frequency noise; nearby moving objects (like people) can create very large noise peaks with an unshielded circuit board. For more detailed explanations and advice on how to avoid these errors, see the LTC1051/LTC1053 data sheet.

Sampling Behavior

The LTC1250's zero-drift nulling loop samples the input at ≈ 5kHz, allowing it to process signals below 2kHz with no aliasing. Signals above this frequency may show aliasing behavior, although wideband internal circuitry generally keeps errors to a minimum. The output of the LTC1250 will have small spikes at the clock frequency and its harmonics; these will vary in amplitude with different feedback configurations. Low frequency or band-limited systems should not be affected, but systems with higher bandwidth (oversampling A/Ds, for example) may need to filter out these clock artifacts. Output spikes can be minimized with a large feedback capacitor, but this will adversely affect noise performance (see Input Capacitance and Compensation on the previous page). Applications which require spike-free output in addition to minimum noise will need a low-pass filter after the LTC1250; a simple RC will usually do the job (Figure 4). The LTC1051/LTC1053 data sheet includes more information about zero-drift amplifier sampling behavior.

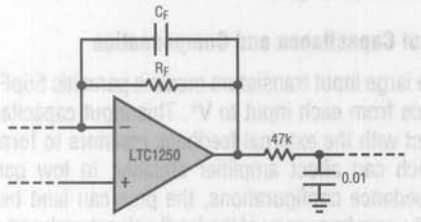


Figure 4. RC Output Pole Limits Bandwidth to 330Hz

Single Supply Operation

The LTC1250 will operate with single supply voltages as low as 4.5V, and the output swings to within millivolts of either supply when lightly loaded. The input stage will common mode to within 250mV of ground with a single 5V supply, and will common mode to ground with single supplies above 11V. Most bridge transducers bias their inputs above ground when powered from single supplies, allowing them to interface directly to the LTC1250 in single supply applications. Single-ended, ground-referenced signals will need to be level shifted slightly to interface to the LTC1250's inputs.

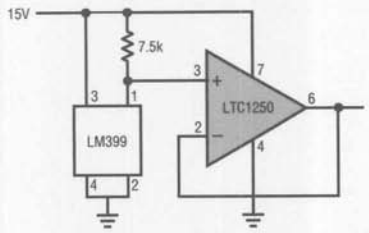
Fault Conditions

The LTC1250 is designed to withstand most external fault conditions without latch-up or damage. However, unusually severe fault conditions can destroy the part. All pins are protected against faults of ±25mA or 5V beyond either supply, whichever comes first. If the external circuitry can exceed these limits, series resistors or voltage clamp diodes should be included to prevent damage.

The LTC1250 includes internal protection against ESD damage. All data sheet parameters are maintained to 1kV ESD on any pin; beyond 1kV, the input bias and offset currents will increase, but the remaining specs are unaffected and the part remains functional to 5kV at the input pins and 8kV at the output pin. Extreme ESD conditions should be guarded against by using standard anti-static precautions.

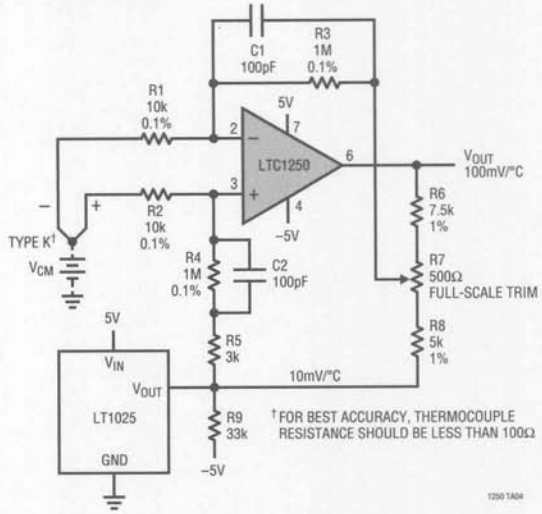
TYPICAL APPLICATIONS

Reference Buffer



±10ppm ERROR AT ±15mA
1μV$_{P-P}$ OUTPUT NOISE
2.5μV/°C DRIFT (DUE TO LM399)

Differential Thermocouple Amplifier



† FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 100Ω

2

SECTION 2—AMPLIFIERS

MULTIPLEXERS

LT1203/LT1205, 150MHz Video Multiplexers 2-374

LT1204, 4-Input Video Multiplexer with 75MHz Current Feedback Amplifier 2-389

150MHz Video Multiplexers

FEATURES

- **–3dB Bandwidth: 150MHz**
- **0.1dB Gain Flatness: 30MHz**
- **Channel-to-Channel Switching Time: 25ns**
- Turn-On/Turn-Off Time: 25ns
- High Slew Rate: 300V/µs
- Disabled Output Impedance: 10MΩ
- 50mV Switching Transient
- Channel Separation at 10MHz: >90dB
- Differential Gain: 0.02%
- Differential Phase: 0.02°
- Wide Supply Range: ±5V to ±15V
- Output Short-Circuit Protected
- Push-Pull Output

APPLICATIONS

- Broadcast Quality Video Multiplexing
- Picture-in-Picture Switching
- HDTV
- Computer Graphics
- Title Generation
- Video Crosspoint Matrices
- Video Routers

DESCRIPTION

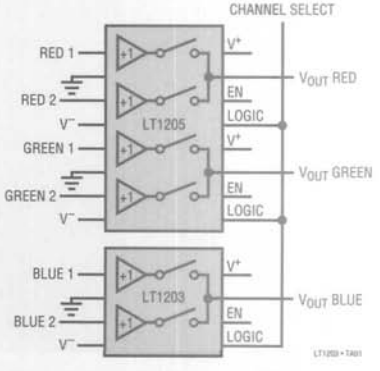
The LT1203 is a wideband 2-input video multiplexer designed for pixel switching and broadcast quality routing. The LT1205 is a dual version that is configured as a 4-input, 2-output multiplexer.

These multiplexers act as SPDT video switches with 10ns transition times at toggle rates up to 30MHz. The –3dB bandwidth is 150MHz and 0.1dB gain flatness is 30MHz. Many parts can be tied together at their outputs by using the enable feature which reduces the power dissipation and raises the output impedance to 10MΩ. Output capacitance when disabled is only 3pF and the LT1203 peaks less than 3dB into a 50pF load. Channel crosstalk and disable isolation are greater than 90dB up to 10MHz. An on-chip buffer interfaces to fast TTL or CMOS logic. Switching transients are only 50mV with a 25ns duration. The LT1203 and LT1205 outputs are protected against shorts to ground.

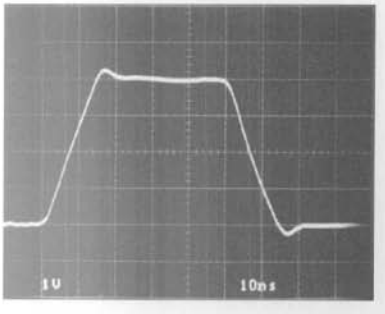
The LT1203/LT1205 are manufactured using Linear Technology's proprietary complementary bipolar process. The LT1203 is available in both the 8-lead PDIP and SO package while the LT1205 is available in the 16-lead narrow body SO package.

TYPICAL APPLICATION

High Speed RGB MUX



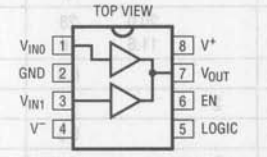
Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Signal Input Current (Note 1) ..... ±20mA
Logic Input Current (Note 2) ..... ±50mA
Output Short-Circuit Duration (Note 3) ..... Continuous
Specified Temperature Range (Note 4) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 5) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
S8 PACKAGE
8-LEAD PLASTIC SOIC

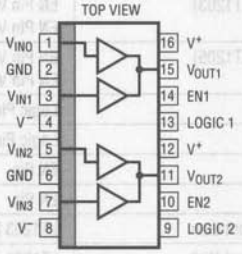
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER

LT1203CN8*
LT1203CS8*

S8 PART MARKING

1203



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1205CS*

*See Note 4
Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $\pm5V \le V_S \le \pm15V$, R_L = 1k, pulse tested, EN pin open or high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Output Offset Voltage	Any Input Selected	●		10	30	mV
	Output Offset Matching	Between Outputs	●		0.3	5	mV
$\Delta V_{OS}/\Delta T$	Output Offset Drift		●		40		µV/°C
I_{IN}	Input Current		●		0.6	5	µA
R_{IN}	Input Resistance	$V_S = \pm5V$, $V_{IN} = \pm2V$	●	1	5		MΩ
		$V_S = \pm15V$, $V_{IN} = \pm2V$	●	2	5		MΩ
C_{IN}	Input Capacitance	Input Selected			2.6		pF
		Input Deselected			2.6		pF
C_{OUT}	Disabled Output Capacitance	EN Pin Voltage ≤ 0.8V			2.8		pF
V_{IN}	Input Voltage (Note 1)	$V_S = \pm5V$	●	±2	±2.8		V
		$V_S = \pm15V$	●	±2	±3.0		V
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5$ to $\pm15V$	●	60	70		dB
	Gain Error	$V_S = \pm15V$, $V_{IN} = \pm2V$, R_L = 1k	●		2	4	%
		$V_S = \pm15V$, $V_{IN} = \pm2V$, $R_L = 400\Omega$	●		6	10	%
		$V_S = \pm5V$, $V_{IN} = \pm2V$, R_L = 1k	●		3	6	%

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, ±5V ≤ V_S ≤ ±15V, R_L = 1k, pulse tested, EN pin open or high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	V_S = ±15V, V_{IN} = ±2V, R_L = 400Ω	●	±1.8	±1.90		V
		V_S = ±5V, V_{IN} = ±2V, R_L = 1k	●	±1.8	±1.94		V
	Overload Swing (Note 1)	V_S = ±15V, V_{IN} = ±5V	●		±0.9	±1.5	V
		V_S = ±5V, V_{IN} = ±5V	●		±0.9	±1.5	V
I_{OUT}	Output Current	V_S = ±15V, V_{IN} = ±2V, R_L = 400Ω	●	±4.5	±4.75		mA
		V_S = ±5V, V_{IN} = ±2V, R_L = 1k	●	±1.8	±2.00		mA
R_{OUT}	Enabled Output Resistance	EN Pin Voltage = 2V, V_{OUT} = ±2V, V_S = ±15V	●		20	42	Ω
	Disabled Output Resistance	EN Pin Voltage = 0.5V, V_{OUT} = ±2V, V_S = ±15V	●	1	10		MΩ
I_S	Supply Current (LT1203)	EN Pin Voltage = 2V	●		10.0	14	mA
		EN Pin Voltage = 0.5V	●		5.8	8	mA
	Supply Current (LT1205)	EN Pin Voltage = 2V	●		20.0	28	mA
		EN Pin Voltage = 0.5V	●		11.6	16	mA
V_{IL}	Logic Low	Logic Pin	●			0.8	V
V_{IH}	Logic High	Logic Pin	●	2			V
	Enable Low	EN Pin	●			0.5	V
	Enable High	EN Pin	●	2			V
I_{IL}	Digital Input Current Low	LT1203 Pin 5, LT1205 Pins 9, 13 = 0V	●		1.5	6.5	µA
I_{IH}	Digital Input Current High	LT1203 Pin 5, LT1205 Pins 9, 13 = 5V	●		10	200	nA
I_{EN}	Enable Pin Current	LT1203 Pin 6, LT1205 Pins 10, 14	●		20	80	µA

AC CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 1k, EN pin open or high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR	Slew Rate (Note 6)		180	300		V/µs
FPBW	Full Power Bandwidth (Note 7)	V_{OUT} = $2V_{P-P}$	28.6	47.7		MHz
t_{SEL}	Channel-to-Channel Select Time (Note 8)	R_L = 10k		25	35	ns
	Enable Time (Note 9)	R_L = 1k		25	35	ns
	Disable Time (Note 9)	R_L = 1k		20	35	ns
t_r, t_f	Small-Signal Rise and Fall Time	V_{OUT} = $250mV_{P-P}$, 10% to 90%		2.6		ns
	Propagation Delay	V_{OUT} = $250mV_{P-P}$		2.9		ns
	Overshoot	V_{OUT} = $250mV_{P-P}$		5		%
	Crosstalk (Note 10)	R_S = 10Ω		90		dB
	Chip Disabled Crosstalk (Note 10)	R_L = 10Ω, EN Pin Voltage ≤ 0.8V		110		dB
	Channel Select Output Transient	All V_{IN} = 0V		50		mV_{P-P}
t_S	Settling Time	1%, V_{OUT} = 1V		30		ns
	Differential Gain (Note 11)	V_S = ±15V, R_L = 10k		0.02		%
	Differential Phase (Note 11)	V_S = ±15V, R_L = 10k		0.02		DEG
	Insertion Loss	R_L = 100k, C_L = 30pF, V_{OUT} = $500mV_{P-P}$, f = 1MHz		0.02		dB

The ● denotes specifications which apply over the specified temperature range.

Note 1: The analog inputs (pins 1, 3 for the LT1203, pins 1, 3, 5, 7 for the LT1205) are protected against ESD and overvoltage with internal SCRs. For inputs ≤±2.8V the SCR will not fire. Voltages above 2.8V will fire the SCR and the DC current should be limited to 20mA. To turn off the SCR the pin voltage must be reduced to less than 1V or the current reduced to less than 600µA.

Note 2: The digital inputs (pins 5, 6 for the LT1203, pins 9, 10, 13, 14 for the LT1205) are protected against ESD and overvoltage with internal SCRs. For inputs ≤±6V the SCR will not fire. Voltages above 6V will fire the SCR and the DC current should be limited to 50mA. To turn off the SCR the pin voltage must be reduced to less than 2V or the current reduced to less than 10mA.

Note 3: A heat sink may be required depending on the power supply voltage.

Note 4: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request, consult factory.

Note 5: T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formulas:

LT1203CN8: $T_J = T_A + (P_D \times 100°C/W)$

LT1203CS8: $T_J = T_A + (P_D \times 150°C/W)$

LT1205CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 6: Slew rate is measured at ±2.0V on a ±2.5V output signal while operating on ±15V supplies, R_L = 1k.

Note 7: Full power bandwidth is calculated from the slew rate measurement:

$FPBW = SR/2\pi V_{PEAK}$

Note 8: For the LT1203, apply 1VDC to pin 1 and measure the time for the appearance of 0.5V at pin 7 when pin 5 goes from 5V to 0V. Apply 1VDC to pin 1 and measure the time for disappearance of 0.5V at pin 7 when pin 5 goes from 0V to 5V. Apply 1VDC to pin 3 and measure the time for the appearance of 0.5V at pin 7 when pin 5 goes from 0V to 5V. Apply 1VDC to pin 3 and measure the time for disappearance of 0.5V at pin 7 when pin 5 goes from 5V to 0V. For the LT1205 the same test is performed on both MUXs.

Note 9: For the LT1203, apply 1VDC to pin 1 and measure the time for the appearance of 0.5V at pin 7 when pin 6 goes from 0V to 5V. Pin 5 voltage = 0V. Apply 1VDC to pin 1 and measure the time for disappearance of 0.2V at pin 7 when pin 6 goes from 5V to 0V. Pin 5 voltage = 0V. Apply 1VDC to pin 3 and measure the time for the appearance of 0.5V at pin 7 when pin 6 goes from 0V to 5V. Pin 5 voltage = 5V. Apply 1VDC to pin 3 and measure the time for disappearance of 0.2V at pin 7 when pin 5 goes from 5V to 0V. Pin 5 voltage = 5V. For the LT1205 the same test is performed on both MUXs.

Note 10: V_{IN} = 0dBm (0.223V_{RMS}) at 10MHz on one input with the other input selected and R_S = 10Ω. For disable crosstalk all inputs are driven simultaneously. In disable the output impedance is very high and signal couples across the package; the load impedance determines the crosstalk.

Note 11: Differential gain and phase are measured using a Tektronix TSG120 YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is 0.1% and 0.1°. Ten identical MUXs were cascaded giving an effective resolution of 0.01% and 0.01°.

2

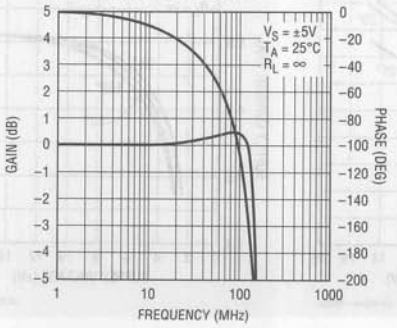
TRUTH TABLE

LOGIC	EN	V_{OUT}
0	1	V_{IN0}
1	1	V_{IN1}
0	0*	HIGH Z_{OUT}
1	0	HIGH Z_{OUT}

*Must be ≤0.5V

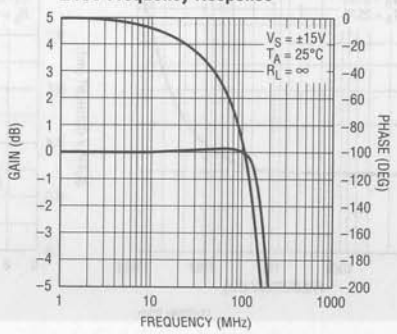
TYPICAL PERFORMANCE CHARACTERISTICS

±5V Frequency Response



LT1203/05 • TPC01

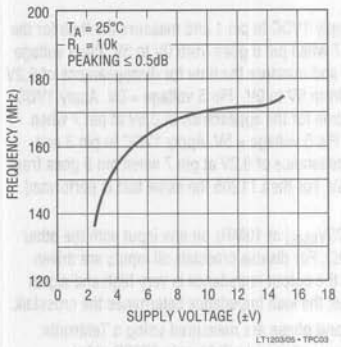
±15V Frequency Response



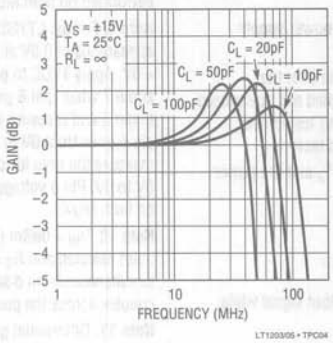
LT1203/05 • TPC02

TYPICAL PERFORMANCE CHARACTERISTICS

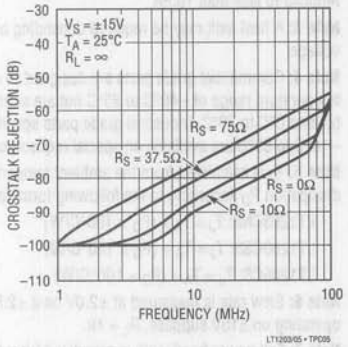
–3dB Bandwidth vs Supply Voltage



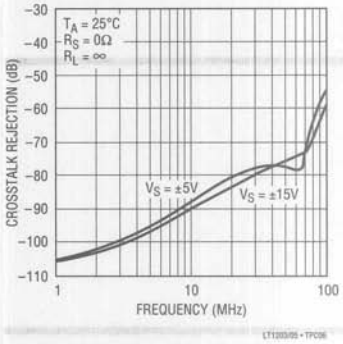
Frequency Response with Capacitive Loads



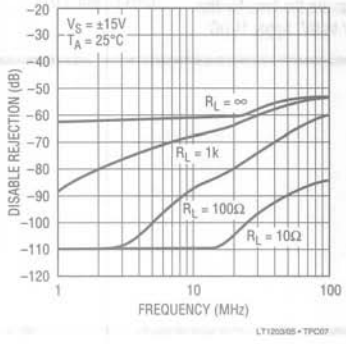
Crosstalk Rejection vs Frequency



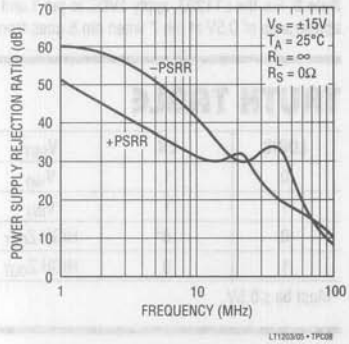
Crosstalk Rejection vs Frequency



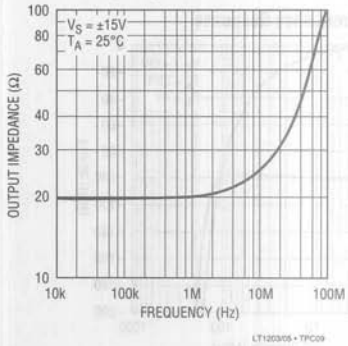
Disable Rejection vs Frequency



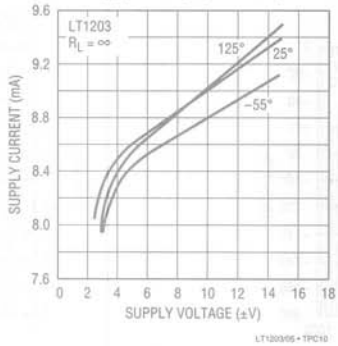
Power Supply Rejection Ratio vs Frequency



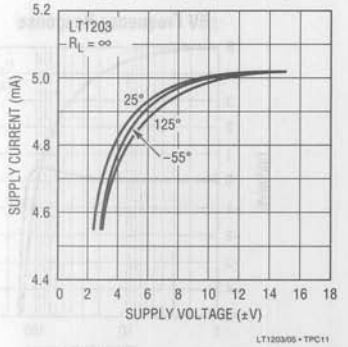
Output Impedance (Enabled) vs Frequency



Supply Current vs Supply Voltage (Enabled)

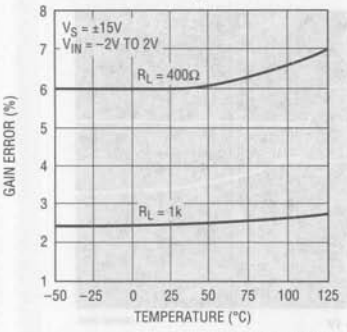


Supply Current vs Supply Voltage (Disabled)

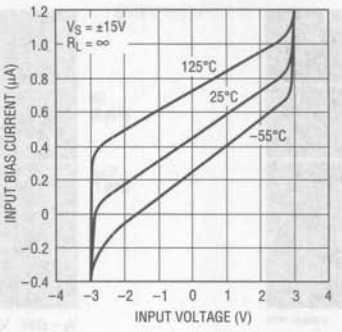


TYPICAL PERFORMANCE CHARACTERISTICS

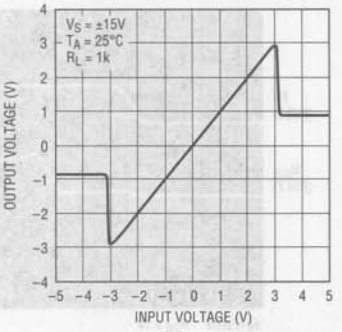
Gain Error vs Temperature



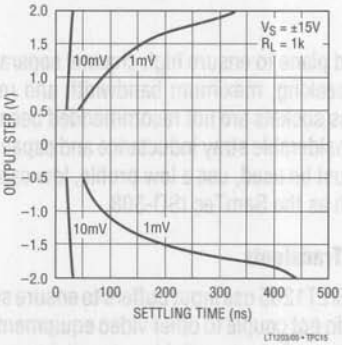
Input Bias Current vs Input Voltage



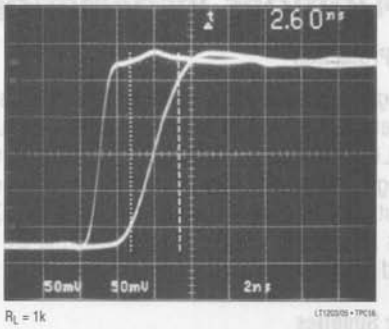
Output Voltage vs Input Voltage



Settling Time to 1mV and 10mV vs Output Step

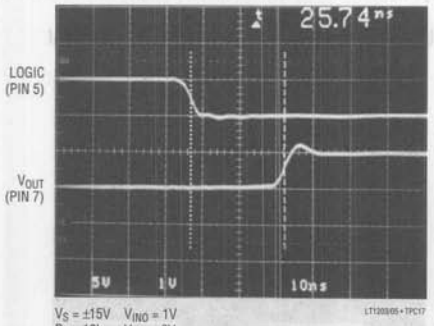


Small-Signal Rise Time



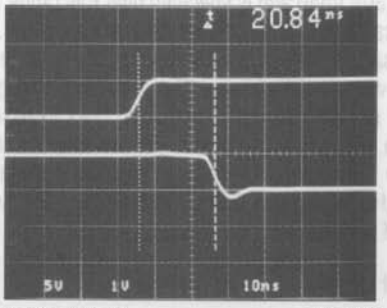
R_L = 1k

V_{IN1} to V_{IN0} Select Time



V_S = ±15V V_{INO} = 1V
R_L = 10k V_{IN1} = 0V

V_{IN0} to V_{IN1} Select Time

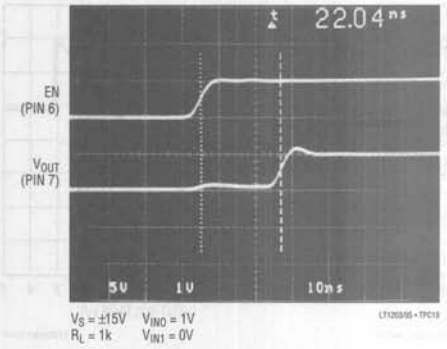


V_S = ±15V V_{INO} = 1V
R_L = 10k V_{IN1} = 0V

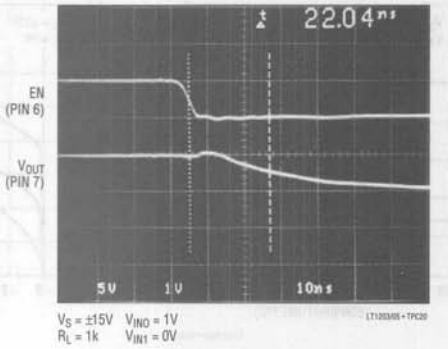
2

TYPICAL PERFORMANCE CHARACTERISTICS

Channel 1 Enable



Channel 1 Disable



APPLICATIONS INFORMATION

Input Protection

The logic inputs have ESD protection (≥2kV) and shorting them to 12V or 15V will cause excessive current to flow. Limit the current to less than 50mA when driving the logic above 6V. The analog inputs are protected against ESD and overvoltage with internal SCRs. For inputs ≥±2.8V the SCRs will fire and the DC current should be limited to 20mA.

Power Supplies

The LT1203/LT1205 will operate from ±5V (10V total) to ±15V (30V total) and is specified over this range. Characteristics change very little over this voltage range. It is not necessary to use equal value supplies however, the output offset voltage will change. The offset will change about 300µV per volt of supply mismatch. The LT1203/LT1205 have a very wide bandwidth yet are tolerant of power supply bypassing. The power supplies should be bypassed with a 0.1µF or 0.01µF ceramic capacitor within 0.5 inch of the part.

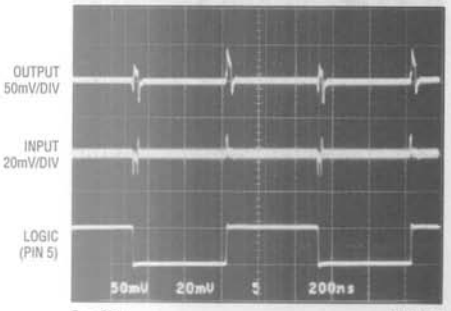
Circuit Layout

Use a ground plane to ensure a low impedance ground is available throughout the PCB layout. Separate the inputs with ground plane to ensure high channel separation. For minimum peaking, maximum bandwidth and maximum gain flatness sockets are not recommended because they can add considerable stray inductance and capacitance. If a socket must be used, use a low profile, low capacitance socket such as the SamTec ISO-308.

Switching Transients

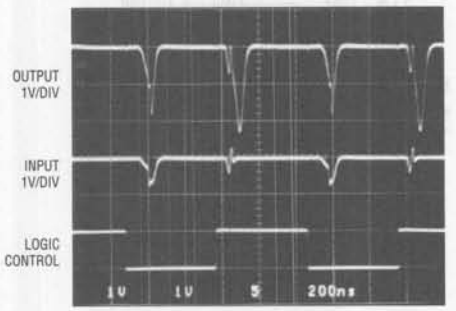
The LT1203/LT1205 use input buffers to ensure switching transients do not couple to other video equipment sharing the input line. Output switching transients are about 50mV$_{P-P}$ with a 20ns duration and input transients are

LT1203 Channel-to-Channel Switching Transient



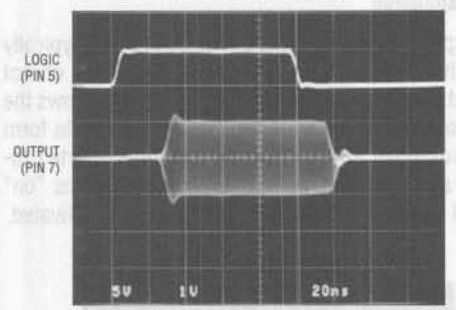
APPLICATIONS INFORMATION

CMOS MUX Channel-to-Channel Switching Transient



$R_S = 50\Omega$
NOTE: 50 TIMES LARGER THAN LT1203 TRANSIENT

LT1203 Switching Inputs



CHANNEL 1 = 0V
CHANNEL 2 = 2MHz SINEWAVE

only $10mV_{P-P}$. A photo of the switching transients from a CMOS MUX shows glitches to be 50 times larger than on the LT1203. Also shown is the output of the LT1203 switching on and off a 2MHz sinewave cleanly and without abnormalities.

Pixel Switching

The multiplexers are fabricated on LTC's Complementary Bipolar Process to attain fast switching speed, high bandwidth, and a wide supply voltage range compatible with traditional video systems. Channel-to-channel switching time and Enable time are both 25ns, therefore delay is the same when switching between channels or between ICs. To demonstrate the switching speed of the LT1203/LT1205 the RGB MUX of Figure 1 is used to switch RGB Workstation inputs with a 22ns pixel width. Figure 2a is a photo showing the Workstation output and RGB MUX output. The slight rise time degradation at the RGB MUX output is due to the bandwidth of the LT1260 current feedback amplifier used to drive the 75Ω cable. In Figure 2b, the LT1203 switches to an input at zero at the end of the first pixel and removes the following pixels.

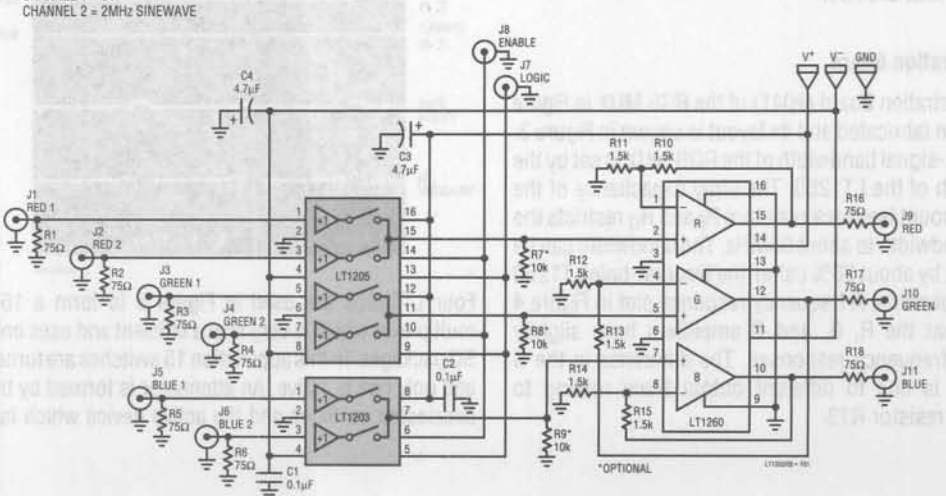


Figure 1. RGB MUX

APPLICATIONS INFORMATION

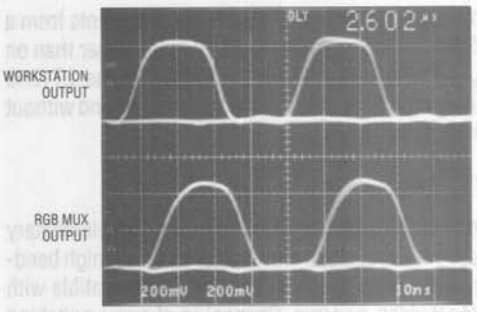


Figure 2a. Workstation and RGB MUX Output

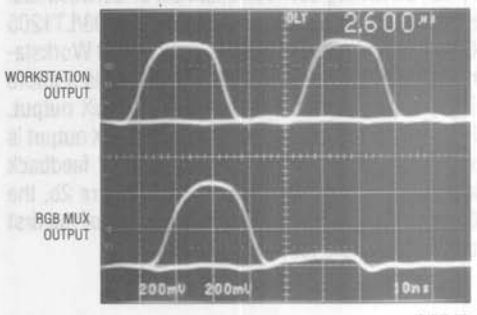


Figure 2b. RGB MUX Output Switched to Ground After One Pixel

Demonstration Board

A Demonstration Board (#041) of the RGB MUX in Figure 1 has been fabricated and its layout is shown in Figure 3. The small-signal bandwidth of the RGB MUX is set by the bandwidth of the LT1260. The stray capacitance of the surface mount feedback resistors R_F and R_G restricts the –3dB bandwidth to about 95MHz. The bandwidth can be improved by about 20% using the through-hole LT1260 and components. A frequency response plot in Figure 4 shows that the R, G, and B amplifiers have slightly different frequency responses. The difference in the G amplifier is due to different output trace routing to feedback resistor R13.

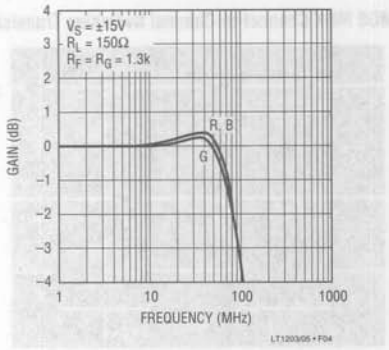
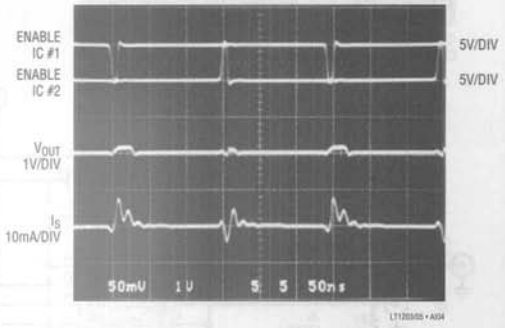


Figure 4. RGB MUX Frequency Response of Demonstration Board #041

Input Expansion

The output impedance of the LT1203/LT1205 is typically 20Ω when enabled and 10MΩ when disabled or not selected. This high disabled output impedance allows the output of many LT1205s to be shorted together to form large crosspoint arrays. With their outputs shorted together, shoot-through current is low because the "on" channel is disabled before the "off" channel is activated.

Timing and Supply Current Waveforms



Four LT1205s are used in Figure 5 to form a 16-to-1 multiplexer which is very space efficient and uses only six SO packages. In this application 15 switches are turned off and only one is active. An attenuator is formed by the 15 deselected switches and the active device which has an

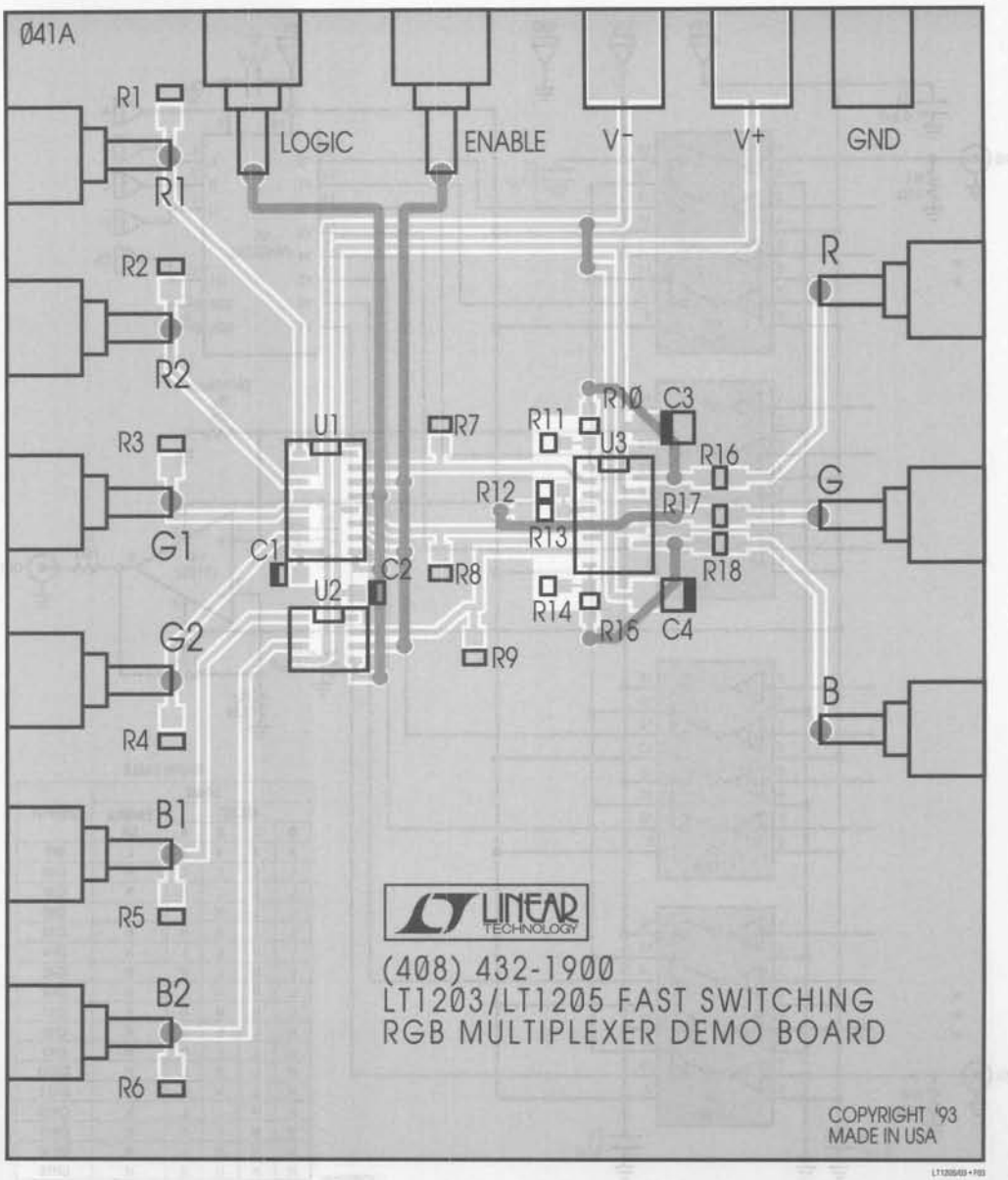
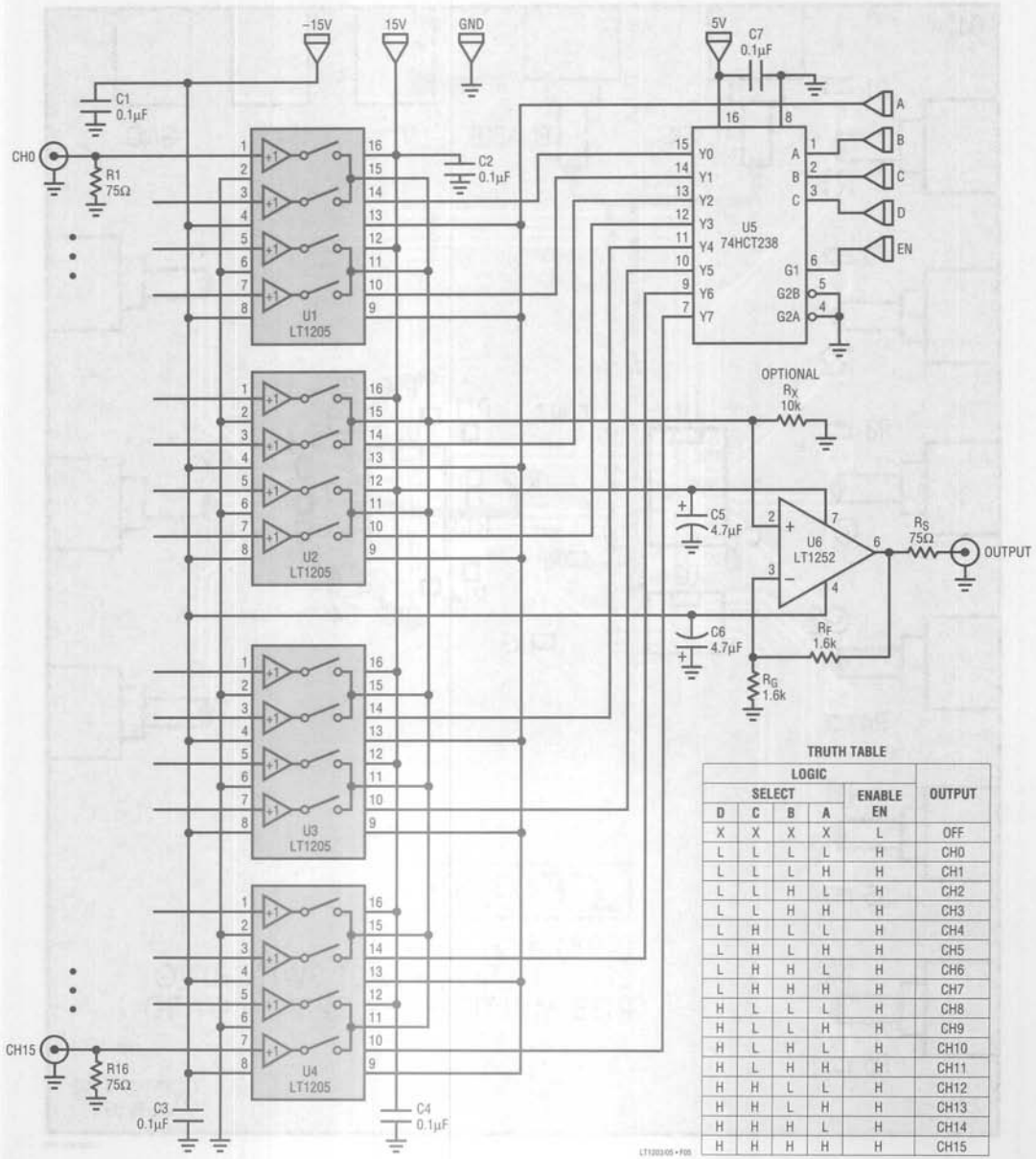


Figure 3. Demo Board #041 Layout

APPLICATIONS INFORMATION



TRUTH TABLE

LOGIC					
SELECT				ENABLE	OUTPUT
D	C	B	A	EN	
X	X	X	X	L	OFF
L	L	L	L	H	CH0
L	L	L	H	H	CH1
L	L	H	L	H	CH2
L	L	H	H	H	CH3
L	H	L	L	H	CH4
L	H	L	H	H	CH5
L	H	H	L	H	CH6
L	H	H	H	H	CH7
H	L	L	L	H	CH8
H	L	L	H	H	CH9
H	L	H	L	H	CH10
H	L	H	H	H	CH11
H	H	L	L	H	CH12
H	H	L	H	H	CH13
H	H	H	L	H	CH14
H	H	H	H	H	CH15

Figure 5. 16-to-1 Multiplexer and Truth Table

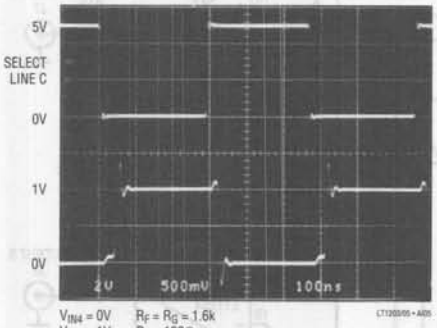
APPLICATIONS INFORMATION

output impedance of only 25Ω at 10MHz. This attenuator is responsible for the outstanding All Hostile Crosstalk Rejection of 90dB at 10MHz with 15 input signals.

Several suggestions to attain this high rejection include:

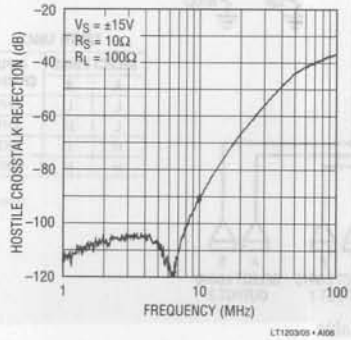
1. Mount the feedback resistors for the surface mount LT1252 on the back side of the PC board.
2. Keep the feedback trace (pin 3) of the LT1252 as short as possible.
3. Route V^+ and V^- for the LT1205s on the component (top) side and under the devices (between inputs and outputs).
4. Use the backside of the PC board as a solid ground plane. Connect the LT1205 device grounds and bypass capacitors grounds as vias to the backside ground plane.

16-to-1 MUX, Switching LT1205 Enable Lines

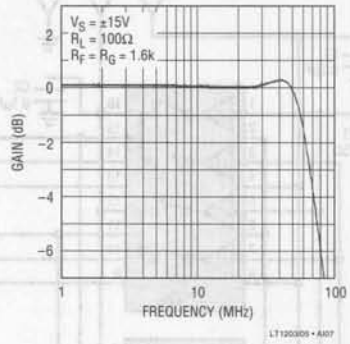


V_{IN4} = 0V $R_F = R_G$ = 1.6k
V_{IN0} = 1V R_L = 100Ω

16-to-1 Multiplexer All Hostile Crosstalk Rejection



16-to-1 MUX Response

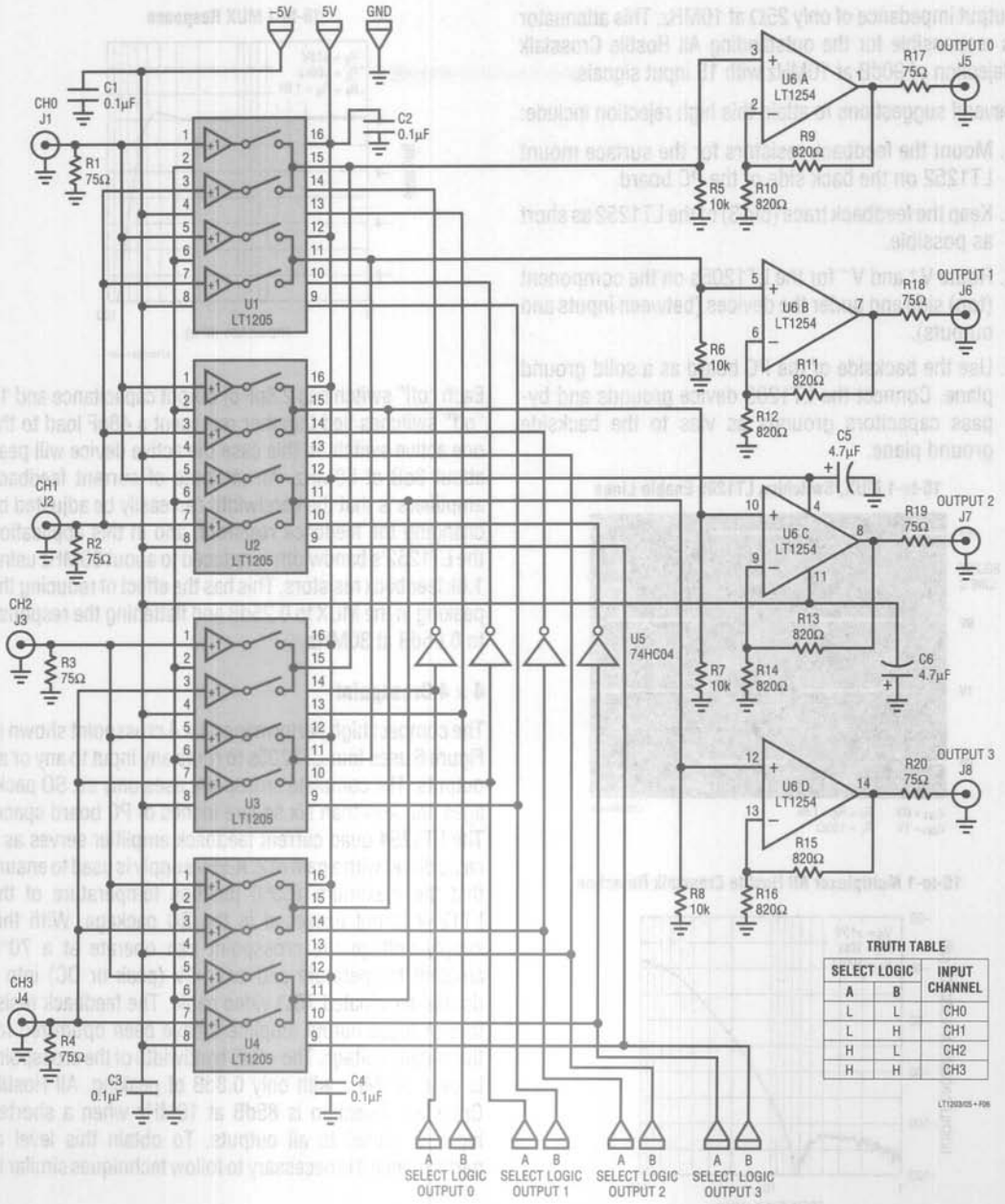


Each "off" switch has 2.8pF of output capacitance and 15 "off" switches tied together represent a 48pF load to the one active switch. In this case the active device will peak about 3dB at 50MHz. An attribute of current feedback amplifiers is that the bandwidth can easily be adjusted by changing the feedback resistors, and in this application the LT1252's bandwidth is reduced to about 60MHz using 1.6k feedback resistors. This has the effect of reducing the peaking in the MUX to 0.25dB and flattening the response to 0.05dB at 30MHz.

4 × 4 Crosspoint

The compact high performance 4 × 4 crosspoint shown in Figure 6 uses four LT1205s to route any input to any or all outputs. The complete crosspoint uses only six SO packages and less than six square inches of PC board space. The LT1254 quad current feedback amplifier serves as a cable driver with a gain of 2. A ±5V supply is used to ensure that the maximum 150°C junction temperature of the LT1254 is not exceeded in the SO package. With this supply voltage the crosspoint can operate at a 70°C ambient temperature and drive 2V (peak or DC) into a double-terminated 75Ω video cable. The feedback resistors of these output amplifiers have been optimized for this supply voltage. The –3dB bandwidth of the crosspoint is over 100MHz with only 0.8dB of peaking. All Hostile Crosstalk Rejection is 85dB at 10MHz when a shorted input is routed to all outputs. To obtain this level of performance it is necessary to follow techniques similar to

APPLICATIONS INFORMATION



TRUTH TABLE

SELECT LOGIC		INPUT CHANNEL
A	B	
L	L	CH0
L	H	CH1
H	L	CH2
H	H	CH3

LT1203/05 • F06

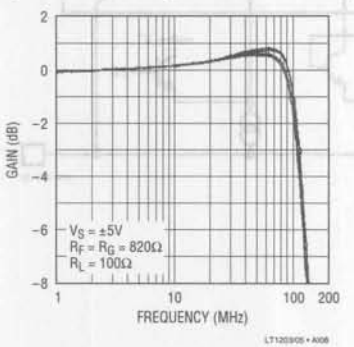
Figure 6. 4 × 4 Crosspoint and Truth Table

APPLICATIONS INFORMATION

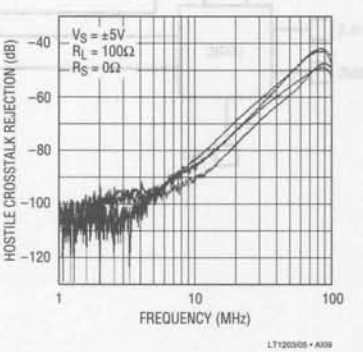
those used in the 16-to-1 crosspoint with one additional suggestion: Surround the LT1205 output traces by ground plane and route them away from the (–) inputs of the other three LT1254s.

Each pair of logic inputs labeled Select Logic Output is used to select a particular output. The truth table is used to select the desired input and is applied to each pair of logic inputs. For example, to route Channel 1 Input to Output 3, the 4th pair of logic inputs labeled Select Logic Output 3 is coded A = Low and B = High. To route Channel 3 Input to all outputs, set all eight logic inputs High. Channel 3 is the default input with all logic inputs open. To shut off all channels a pair of LT1259s can be substituted for the LT1254. The LT1259 is a dual current feedback amplifier with a shutdown pin that reduces the supply current to 0μA.

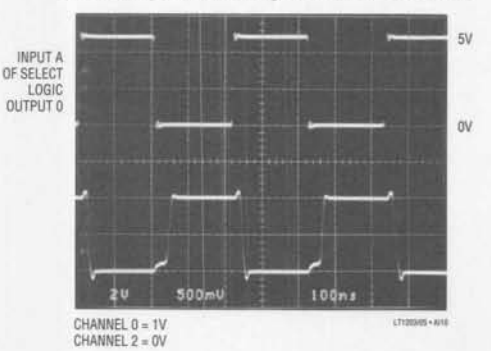
Response of All Four Inputs for the 4 × 4 Crosspoint



4 × 4 Crosspoint, All Hostile Rejection

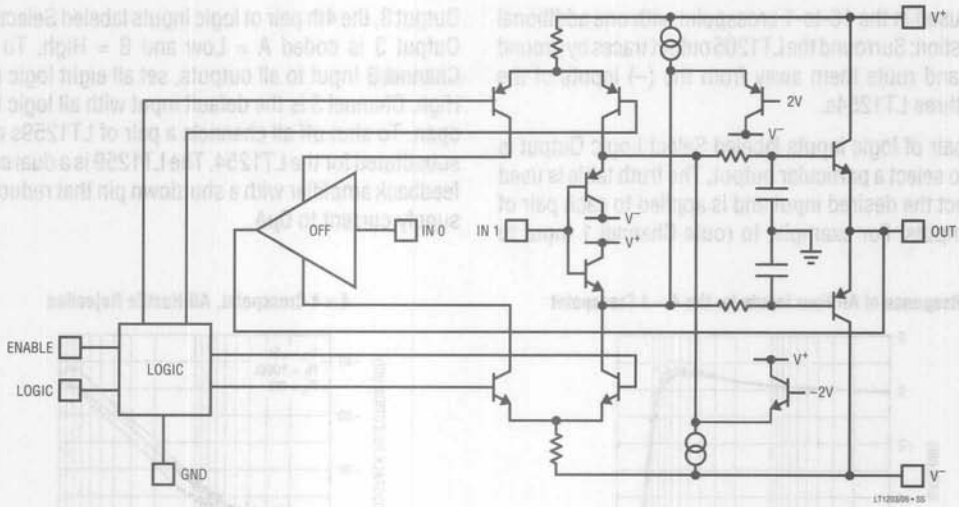


4 × 4 Crosspoint, Switching Channel 0 to Channel 2



CHANNEL 0 = 1V
CHANNEL 2 = 0V

SIMPLIFIED SCHEMATIC



4-Input Video Multiplexer with 75MHz Current Feedback Amplifier

FEATURES

- **0.1dB Gain Flatness > 30MHz**
- **Channel Separation at 10MHz: 90dB**
- **40mV Switching Transient, Input Referred**
- –3dB Bandwidth, A_V = 2, R_L = 150Ω: 75MHz
- Channel-to-Channel Switching Time: 120ns
- Easy to Expand for More Inputs
- Large Input Range: ±6V
- 0.04% Differential Gain, R_L = 150Ω
- 0.06° Differential Phase, R_L = 150Ω
- High Slew Rate: 1000V/µs
- Output Swing, R_L = 400Ω: ±13V
- Wide Supply Range: ±5V to ±15V

APPLICATIONS

- Broadcast Quality Video Multiplexing
- Large Matrix Routing
- Medical Imaging
- Large Amplitude Signal Multiplexing
- Programmable Gain Amplifiers

DESCRIPTION

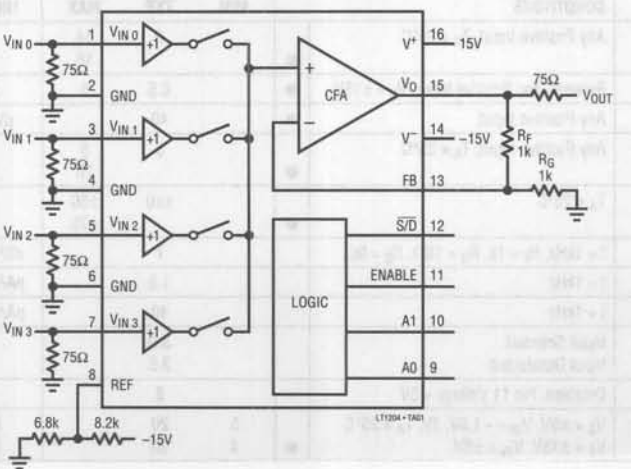
The LT1204 is a 4-input video multiplexer designed to drive 75Ω cables and easily expand into larger routing systems. Wide bandwidth, high slew rate, and low differential gain and phase make the LT1204 ideal for broadcast quality signal routing. Channel separation and disable isolation are greater than 90dB up to 10MHz. The channel-to-channel output switching transient is only 40mV_{P-P}, with a 50ns duration, making the transition imperceptible on high quality monitors.

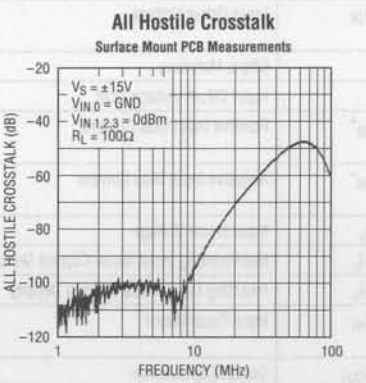
A unique feature of the LT1204 is its ability to expand into larger routing matrices. This is accomplished by a patent pending circuit that bootstraps the feedback resistors in the disable condition, raising the true output impedance of the circuit. The effect of this feature is to eliminate cable misterminations in large systems.

The large input and output signal levels supported by the LT1204 when operated on ±15V supplies make it ideal for general purpose analog signal selection and multiplexing. A shutdown feature reduces the supply current to 1.5mA.

2

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
– Input Current (Pin 13) ..... ±15mA
+Input and Control/Logic Current (Note 1) ..... ±50mA
Output Short-Circuit Duration (Note 2) ..... Continuous
Specified Temperature Range (Note 3) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 4) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

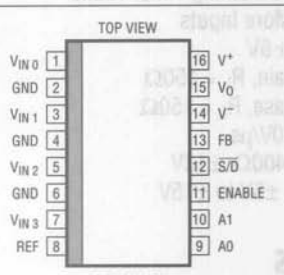
PACKAGE/ORDER INFORMATION

N PACKAGE
16-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1204CN*



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER

LT1204CS*

*See Note 3
Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $\pm5V \le V_S \le \pm15V$, $V_{CM} = 0V$, Pin 8 grounded and pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Any Positive Input, T_A = 25°C			5	14	mV
			●			16	mV
	Offset Matching	Between Any Positive Input, V_S = ±15V	●		0.5	5	mV
	Input Offset Voltage Drift	Any Positive Input	●		40		µV/°C
I_{IN}^+	Positive Input Bias Current	Any Positive Input, T_A = 25°C			3	8	µA
			●			10	µA
I_{IN}^-	Negative Input Bias Current	T_A = 25°C			±10	±50	µA
			●			±75	µA
e_n	Input Noise Voltage	f = 1kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			7		nV/√Hz
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.5		pA/√Hz
$-i_n$	Inverting Input Noise Current Density	f = 1kHz			40		pA/√Hz
C_{IN}	Input Capacitance	Input Selected			3.0		pF
		Input Deselected			3.5		pF
C_{OUT}	Output Capacitance	Disabled, Pin 11 Voltage = 0V			8		pF
R_{IN}	Positive Input Resistance, Any Positive Input	V_S = ±5V, V_{IN} = –1.5V, 2V, T_A = 25°C		5	20		MΩ
		V_S = ±15V, V_{IN} = ±5V	●	4	20		MΩ

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $\pm5V \le V_S \le \pm15V$, $V_{CM} = 0V$, Pin 8 grounded and pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Voltage Range, Any Positive Input	$V_S = \pm5V$, $T_A = 25°C$		2.0	2.5		V
				−1.5	−2.0		V
		$V_S = \pm15V$	●	±5.0	±6.0		V
		$V_S = \pm15V$, Pin 8 Voltage = −5V	●	3.75	4.0		V
CMRR	Common-Mode Rejection Ratio	$V_S = \pm5V$, $V_{CM} = -1.5V, 2V$, $T_A = 25°C$		48	55		dB
		$V_S = \pm15V$, $V_{CM} = \pm5V$	●	48	58		dB
	Negative Input Current Common-Mode Rejection	$V_S = \pm5V$, $V_{CM} = -1.5V, 2V$, $T_A = 25°C$			0.05	1	µA/V
		$V_S = \pm15V$, $V_{CM} = \pm5V$	●		0.05	1	µA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm15V$	●	60	76		dB
	Negative Input Current Power Supply Rejection	$V_S = \pm4.5V$ to $\pm15V$	●		0.5	5	µA/V
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 1k$	●	57	73		dB
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_L = 150\Omega$	●	57	66		dB
R_{OL}	Transresistance $\Delta V_O/\Delta I_{IN}^-$	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 1k$	●	115	310		kΩ
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_L = 150\Omega$	●	115	210		kΩ
V_{OUT}	Output Voltage Swing	$V_S = \pm15V$, $R_L = 400\Omega$, $T_A = 25°C$		±12	±13.5		V
			●	±10			V
		$V_S = \pm5V$, $R_L = 150\Omega$, $T_A = 25°C$		±3.0	±3.7		V
			●	±2.5			V
I_{OUT}	Output Current	$R_L = 0\Omega$, $T_A = 25°C$		35	55	125	mA
I_S	Supply Current (Note 5)	Pin 11 = 5V	●		19	24	mA
		Pin 11 = 0V	●		19	24	mA
		Pin 12 = 0V	●		1.5	3.5	mA
	Disabled Output Resistance	$V_S = \pm15V$, Pin 11 = 0V, $V_O = \pm5V$, $R_F = R_G = 1k$	●	14	25		kΩ
		$V_S = \pm15V$, Pin 11 = 0V, $V_O = \pm5V$, $R_F = 2k$, $R_G = 222\Omega$	●	8	20		kΩ

DIGITAL INPUT CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm15V$, $R_F = 2k$, $R_G = 220\Omega$, $R_L = 400\Omega$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	Pins 9, 10, 11, 12	●			0.8	V
V_{IH}	Input High Voltage	Pins 9, 10, 11, 12	●	2			V
I_{IL}	Input Low Current	Pins 9, 10 Voltage = 0V	●		1.5	6	µA
I_{IH}	Input High Current	Pins 9, 10 Voltage = 5V	●		10	150	nA
	Enable Low Input Current	Pin 11 Voltage = 0V	●		4.5	15	µA
	Enable High Input Current	Pin 11 Voltage = 5V	●		200	300	µA
$I_{\overline{S/D}}$	Shutdown Input Current	Pin 12 Voltage $0V \le V_{\overline{S/D}} \le 5V$	●		20	80	µA
t_{sel}	Channel-to-Channel Select Time (Note 6)	Pin 8 Voltage = −5V, $T_A = 25°C$			120	240	ns
t_{dis}	Disable Time (Note 7)	Pin 8 Voltage = −5V, $T_A = 25°C$			40	100	ns
t_{en}	Enable Time (Note 8)	Pin 8 Voltage = −5V, $T_A = 25°C$			110	200	ns
$t_{\overline{S/D}}$	Shutdown Assert or Release Time (Note 9)	Pin 8 Voltage = −5V, $T_A = 25°C$			1.4	3.4	µs

AC CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, $R_F = R_G = 1k$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_r, t_f	Small-Signal Rise and Fall Time	$R_L = 150\Omega$, $V_{OUT} = \pm125mV$		5.6		ns
SR	Slew Rate (Note 10)	$R_L = 400\Omega$	500	1000		V/µs
	Channel Select Output Transient	All $V_{IN} = 0V$, $R_L = 400\Omega$, Input Referred		40		mV
t_S	Settling Time	0.1%, $V_{OUT} = 10V$, $R_L = 1k$		70		ns
	All Hostile Crosstalk (Note 11)	SO PCB #028, $R_L = 100\Omega$, $R_S = 10\Omega$		92		dB
	Disable Crosstalk (Note 11)	SO PCB #028, Pin 11 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		95		dB
	Shutdown Crosstalk (Note 11)	SO PCB #028, Pin 12 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		92		dB
	All Hostile Crosstalk (Note 11)	P-DIP PCB #029, $R_L = 100\Omega$, $R_S = 10\Omega$		76		dB
	Disable Crosstalk (Note 11)	P-DIP PCB #029, Pin 11 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		81		dB
	Shutdown Crosstalk (Note 11)	P-DIP PCB #029, Pin 12 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		76		dB
	Differential Gain (Note 12)	$V_S = \pm15V$, $R_L = 150\Omega$ $V_S = \pm5V$, $R_L = 150\Omega$		0.04 0.04		% %
	Differential Phase (Note 12)	$V_S = \pm15V$, $R_L = 150\Omega$ $V_S = \pm5V$, $R_L = 150\Omega$		0.06 0.12		DEG DEG

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: Analog and digital inputs (Pins 1, 3, 5, 7, 9, 10, 11 and 12) are protected against ESD and overvoltage with internal SCRs. For inputs < ±6V the SCR will not fire, voltages above 6V will fire the SCRs and the DC current should be limited to 50mA. To turn off the SCR the pin voltage must be reduced to less than 2V or the current reduced to less than 10mA.

Note 2: A heat sink may be required depending on the power supply voltage.

Note 3: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

Note 4: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1204CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1204CS: $T_J = T_A + (P_D \times 90°C/W)$

Note 5: The supply current of the LT1204 has a negative temperature coefficient. For more information see Typical Performance Characteristics.

Note 6: Apply 0.5V DC to Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 5V to 0V. Pin 10 Voltage = 0V. Apply 0.5V DC to Pin 3 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 0V to 5V. Pin 10 Voltage = 0V. Apply 0.5V DC to Pin 5 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 5V to 0V. Pin 10 Voltage = 5V. Apply 0.5V DC to Pin 7 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 0V to 5V. Pin 10 Voltage = 5V.

Note 7: Apply 0.5V DC to Pin 1 and measure the time for the disappearance of 5V at Pin 15 when Pin 11 goes from 5V to 0V. Pins 9 and 10 are at 0V.

Note 8: Apply 0.5V DC to Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 11 goes from 0V to 5V. Pins 9 and 10 are at 0V. Above a 1MHz toggle rate, t_{en} reduces.

Note 9: Apply 0.5V DC at Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 12 goes from 0V to 5V. Pins 9 and 10 are at 0V. Then measure the time for the disappearance of 5V DC to 500mV at Pin 15 when Pin 12 goes from 5V to 0V.

Note 10: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with $R_F = 2k$, $R_G = 220\Omega$ and $R_L = 400\Omega$.

Note 11: V_{IN} = 0dBm (0.223V_{RMS}) at 10MHz on any 3 inputs with the 4th input selected. For Disable crosstalk and Shutdown crosstalk all 4 inputs are driven simultaneously. A 6dB output attenuator is formed by a 50Ω series output resistor and the 50Ω input impedance of the HP4195A Network Analyzer. $R_F = R_G = 1k$.

Note 12: Differential Gain and Phase are measured using a Tektronix TSG120 YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Five identical MUXs were cascaded giving an effective resolution of 0.02% and 0.02°.

TYPICAL AC PERFORMANCE

Measurements taken from SO Demonstration Board #028.

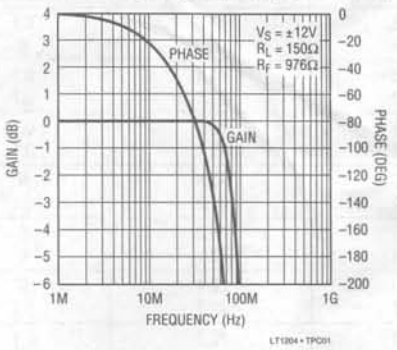
V_S (V)	A_V	R_L (Ω)	R_F (Ω)	R_G (Ω)	SMALL SIGNAL −3dB BW (MHz)	SMALL SIGNAL 0.1dB BW (MHz)	SMALL SIGNAL PEAKING (dB)
±15	1	150	1.1k	None	88.5	48.3	0.1
		1k	1.6k	None	95.6	65.8	0
±12	1	150	976	None	82.6	49.1	0.1
		1k	1.3k	None	90.2	63.6	0.1
±5	1	150	665	None	65.5	43.6	0.1
		1k	866	None	68.2	42.1	0.1
±15	2	150	787	787	75.7	45.8	0
		1k	887	887	82.2	61.3	0.1
±12	2	150	750	750	71.9	45.0	0
		1k	845	845	77.5	52.1	0
±5V	2	150	590	590	58.0	32.4	0
		1k	649	649	62.1	42.7	0.1
±15	10	150	866	95.3	44.3	28.7	0.1
		1k	1k	110	47.4	30.9	0.1
±12	10	150	825	90.9	43.5	27.2	0
		1k	931	100	46.3	32.1	0.1
±5	10	150	665	73.2	37.2	22.1	0
		1k	750	82.5	39.3	27.8	0.1

TRUTH TABLE

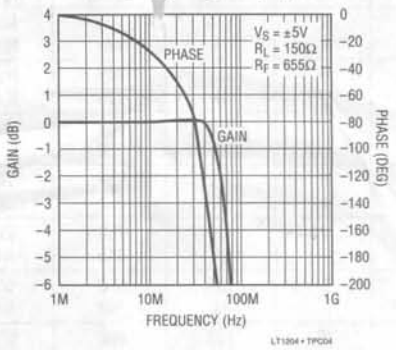
A1	A0	ENABLE	$\overline{\text{SHUTDOWN}}$	CHANNEL SELECTED
0	0	1	1	$V_{IN\,0}$
0	1	1	1	$V_{IN\,1}$
1	0	1	1	$V_{IN\,2}$
1	1	1	1	$V_{IN\,3}$
X	X	0	1	High Z Output
X	X	X	0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

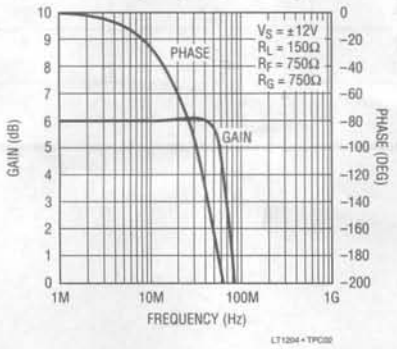
±12V Frequency Response, $A_V = 1$



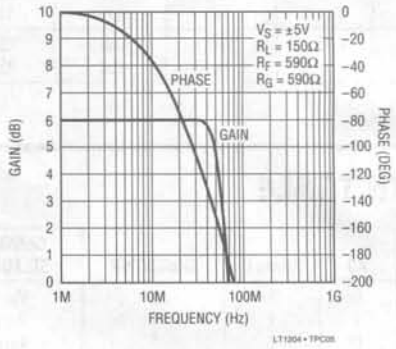
±5V Frequency Response, $A_V = 1$



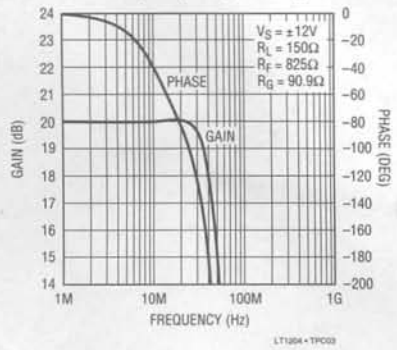
±12V Frequency Response, $A_V = 2$



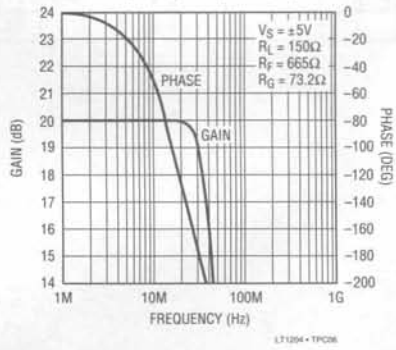
±5V Frequency Response, $A_V = 2$



±12V Frequency Response, $A_V = 10$

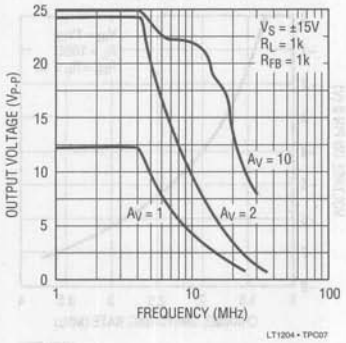


±5V Frequency Response, $A_V = 10$

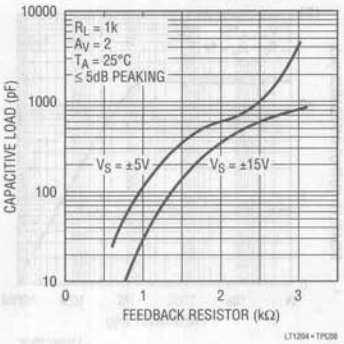


TYPICAL PERFORMANCE CHARACTERISTICS

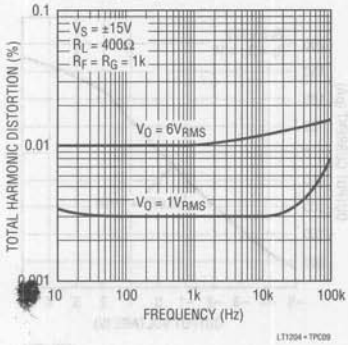
Maximum Undistorted Output vs Frequency



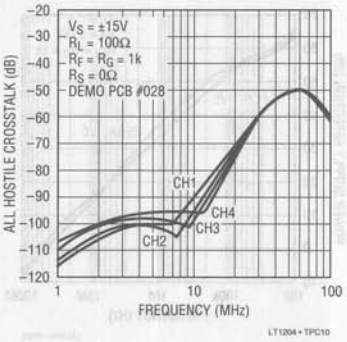
Maximum Capacitive Load vs Feedback Resistor



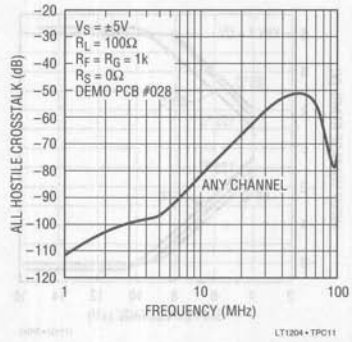
Total Harmonic Distortion vs Frequency



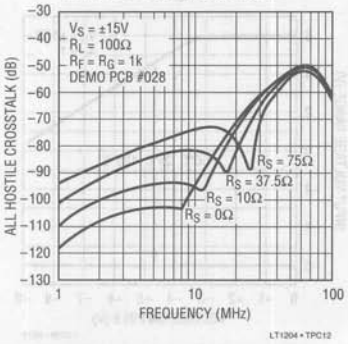
±15V All Hostile Crosstalk vs Frequency



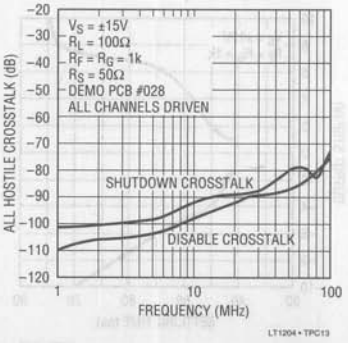
±5V All Hostile Crosstalk vs Frequency



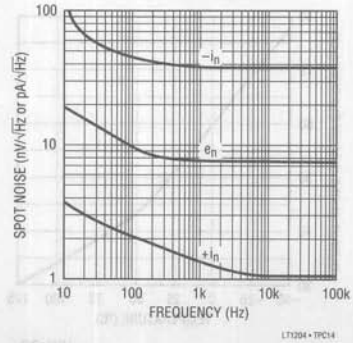
All Hostile Crosstalk vs Frequency, Various Source Resistance



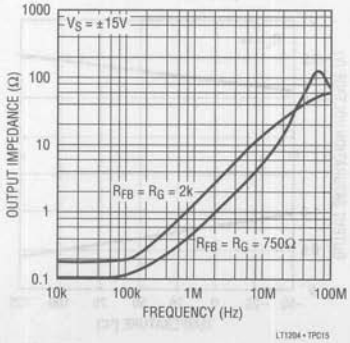
Disable and Shutdown Crosstalk vs Frequency



Spot Noise Voltage and Current vs Frequency



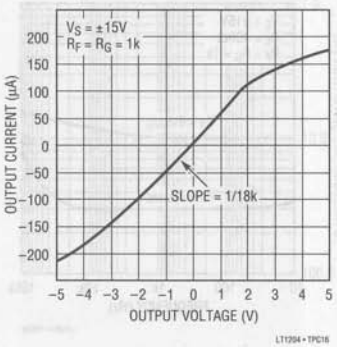
Amplifier Output Impedance vs Frequency



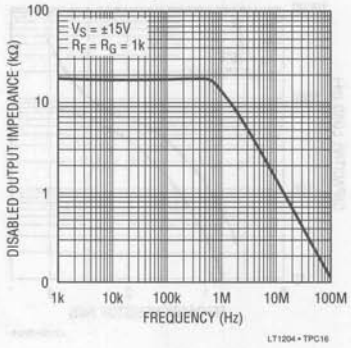
2

TYPICAL PERFORMANCE CHARACTERISTICS

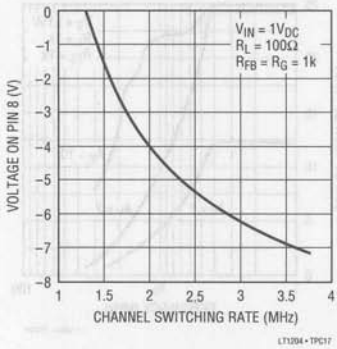
Output Disable V-I Characteristic



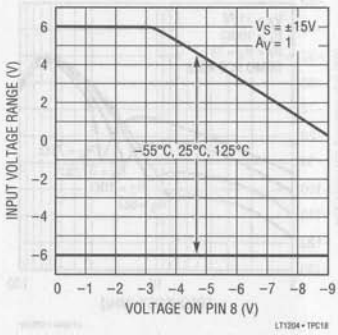
Disabled Output Impedance vs Frequency



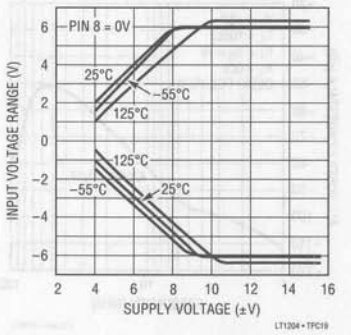
Maximum Channel Switching Rate vs Pin 8 Voltage



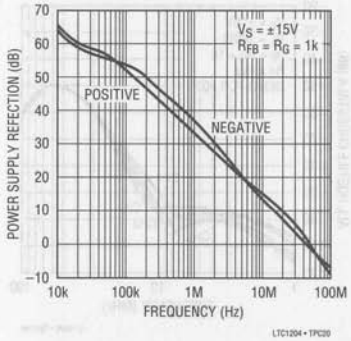
Input Voltage Range vs Pin 8 Voltage



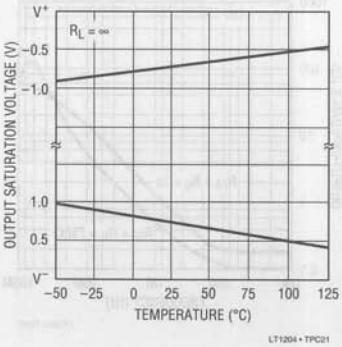
Input Voltage Range vs Supply Voltage



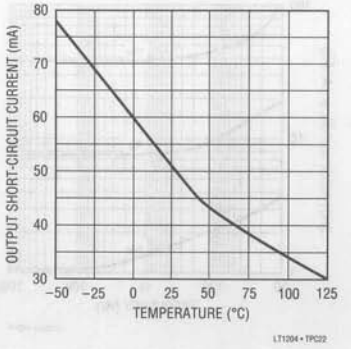
Power Supply Rejection vs Frequency



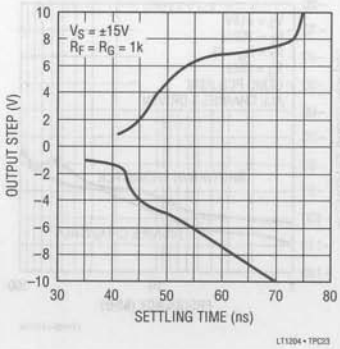
Output Saturation Voltage vs Temperature



Output Short-Circuit Current vs Temperature

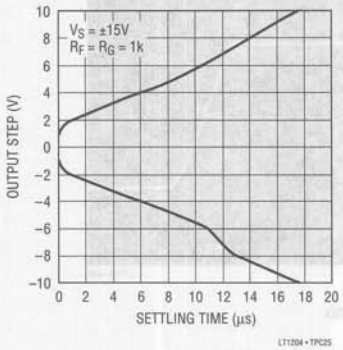


Settling Time to 10mV vs Output Step

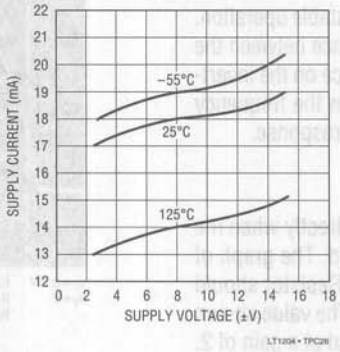


TYPICAL PERFORMANCE CHARACTERISTICS

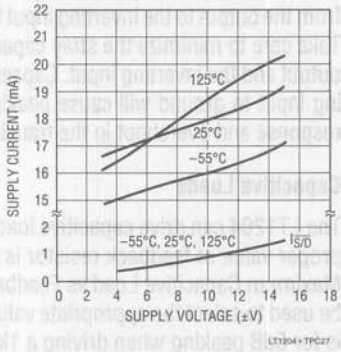
Settling Time to 1mV vs Output Step



Enabled Supply Current vs Supply Voltage



Disabled and Shutdown Supply Current vs Supply Voltage



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APPLICATIONS INFORMATION

Logic Inputs

The logic inputs of the LT1204 are compatible with all 5V logic. All pins have ESD protection (>2kV), and shorting them to 12V or 15V will cause excessive currents to flow. Limit the current to less than 50mA when driving the logic above 6V.

Power Supplies

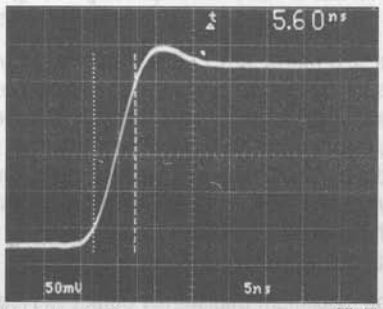
The LT1204 will operate from ±5V (10V total) to ±15V (30V total) and is specified over this range. It is not necessary to use equal value supplies, however, the offset voltage and inverting input bias current will change. The offset voltage changes about 600µV per volt of supply mismatch. The inverting bias current changes about 2.5µA per volt of supply mismatch. The power supplies should be bypassed with quality tantalum capacitors.

Feedback Resistor Selection

The small-signal bandwidth of the LT1204 is set by the external feedback resistors and internal junction capacitors. As a result the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and the load resistor. These effects are outlined in the resistor selection guide of the Typical AC Performance table. Bandwidths range as high as 95MHz and are specified over a very wide range of conditions. An advantage of the current feedback topology used in the LT1204 is well-controlled frequency response. In all cases of the performance table the peaking is 0.1dB or less. If more peaking can be tolerated, larger bandwidths can be obtained by lowering the feedback resistor. For gains of 2 or less, the 0.1dB bandwidth is greater than 30MHz for all loads and supply voltages.

At high gains (low values of R_G) the disabled output resistance drops slightly due to loading of the internal buffer amplifier as discussed in Multiplexer Expansion.

Small-Signal Rise Time, A_V = 2



APPLICATIONS INFORMATION

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response and overshoot in the transient response.

Capacitive Loads

The LT1204 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1k load at a gain of 2. This is a worst case condition. The amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present. The disadvantage is that the gain is a function of load resistance.

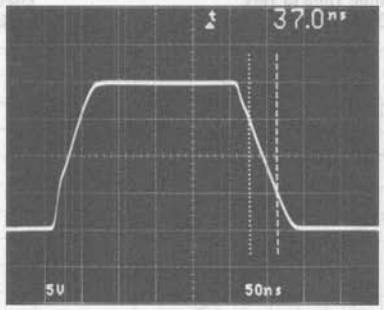
Slew Rate

The slew rate of the current feedback amplifier on the LT1204 is not independent of the amplifier gain the way slew rate is in a traditional op amp. This is because both the input and the output stage have slew rate limitations. In high gain settings the signal amplitude between the negative input and any driven positive input is small and the overall slew rate is that of the output stage. For gains less than 10, the overall slew rate is limited by the input stage.

The input slew rate of the LT1204 is approximately 135V/μs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and the internal capacitances. At a gain of 10 with a 1k feedback resistor and ±15 supplies, the output slew rate is typically 1000V/μs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

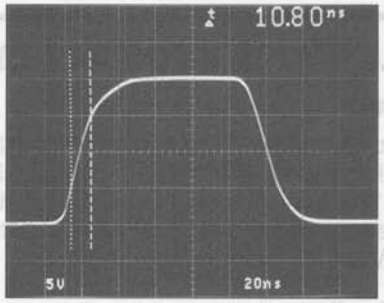
The graph, Maximum Undistorted Output vs Frequency, relates the slew rate limitations to sinusoidal inputs for various gain configurations.

Large-Signal Transient Response



$V_S = \pm 15V$ $R_F = 1k$
$A_V = 2$ $R_G = 1k$
$R_L = 400\Omega$

Large-Signal Transient Response



$V_S = \pm 15V$ $R_F = 910\Omega$
$A_V = 10$ $R_G = 100\Omega$
$R_L = 400\Omega$

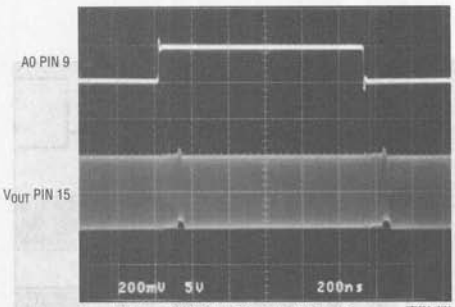
Switching Characteristics and Pin 8

Switching between channels is a "make-before-break" condition where both inputs are on momentarily. The buffers isolate the inputs when the "make-before-break" switching occurs. The input with the largest positive voltage determines the output level. If both inputs are equal, there is only a 40mV error at the input of the CFA during the transition. The reference adjust (pin 8) allows the user to trade off positive input voltage range for switching time. For example, on ±15V supplies, setting the voltage on pin 8 to −6.8V reduces the switching transient to a 50ns duration, and reduces the positive input range from 6V to 2.35V. The negative input range remains unchanged at −6V. When switching video "in picture," this short transient is imperceptible even on high quality

APPLICATIONS INFORMATION

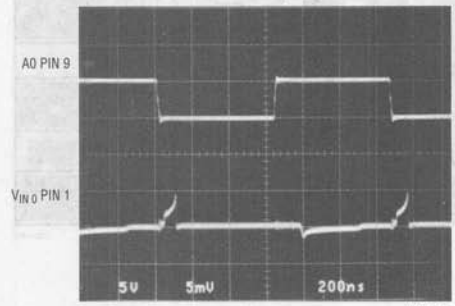
monitors. The reference pin has no effect when the LT1204 is operating on ±5V, and should be grounded. On supply voltages above ±8V, the range of voltages for pin 8 should be between −6.5V and −7.5V. Reducing pin 8 voltage below −7.5V turns "on" the "off" tee switch, and the isolation between channels is lost.

Channel-to-Channel Switching



$V_{IN\,0}$ AND $V_{IN\,1}$ CONNECTED TO 2MHz SINEWAVE
PIN 8 VOLTAGE = −6.8V, V_S = ±15V

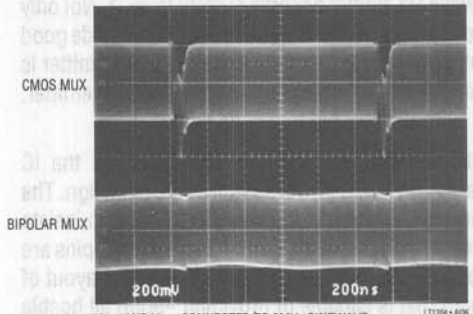
Transient at Input Buffer



SWITCHING BETWEEN $V_{IN\,0}$ AND $V_{IN\,1}$
R_S = 50Ω, V_{REF} = −6.8V, V_S ±15V

Competitive video multiplexers built in CMOS are bidirectional and suffer from poor output-to-input isolation and cause transients to feed to the inputs. CMOS MUXs have been built with "break-before-make" switches to eliminate the talking between channels, but these suffer from output glitches large enough to interfere with sync circuitry. Multiplexers built on older bipolar processes that switch lateral PNP transistors take several µs to settle and blur the transition between pictures.

Competitive MUXs



$V_{IN\,0}$ AND $V_{IN\,1}$ CONNECTED TO 2MHz SINEWAVE

Crosstalk

The crosstalk, or more accurately all hostile crosstalk, is measured by driving a signal into any 3 of the 4 inputs and selecting the 4th input with the logic control. This 4th input is either shorted to ground or terminated in an impedance. All hostile crosstalk is defined as the ratio in dB of the signal at the output of the CFA to the signal on the 3 driven inputs, and is input referred. Disable crosstalk is measured with all 4 inputs driven and the part disabled. Crosstalk is critical in many applications where video multiplexers are used. In professional video systems a crosstalk figure of −72dB is a desirable specification.

The key to the outstanding crosstalk performance of the LT1204 is the use of tee switches (see Figure 1). When the tee switch is on (Q2 off) Q1 and Q3 are a pair of emitter followers with excellent AC response for driving the CFA. When the decoder turns off the tee switch (Q2 on) the

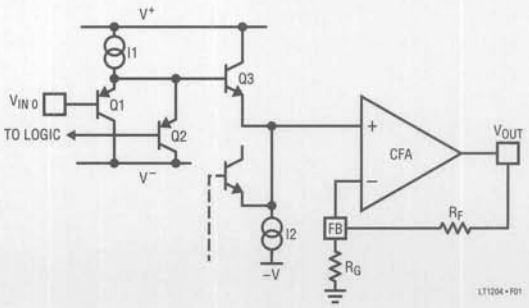


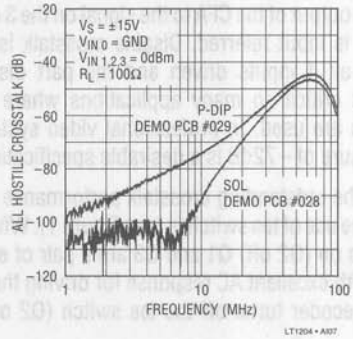
Figure 1. Tee Switch

APPLICATIONS INFORMATION

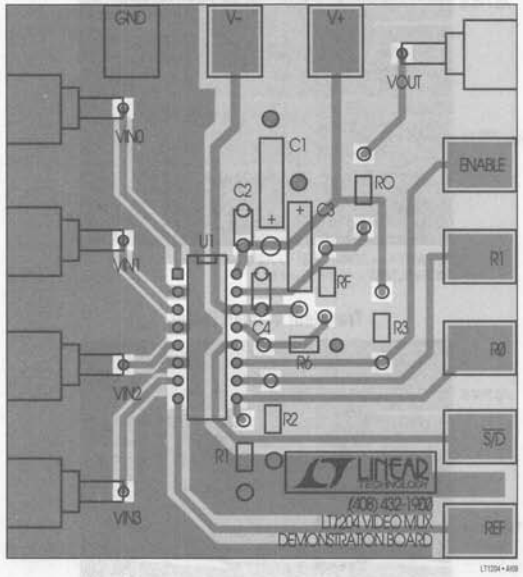
emitter base junctions of Q1 and Q3 become reverse biased while Q2 emitter absorbs current from I1. Not only do the reverse biased emitter base junctions provide good isolation, but any signal at $V_{IN\,0}$ coupling to Q1 emitter is further attenuated by the shunt impedance of Q2 emitter. Current from I2 is routed to any on switch.

Crosstalk performance is a strong function of the IC package, the PC board layout as well as the IC design. The die layout utilizes grounds between each input to isolate adjacent channels, while the output and feedback pins are on opposite sides of the die from the input. The layout of a PC board that is capable of providing –90dB all hostile crosstalk at 10MHz is not trivial. That level corresponds to a 30μV output below a 1V input at 10MHz. A demonstration board has been fabricated to show the component and ground placement required to attain these crosstalk numbers. A graph of all hostile crosstalk for both the P-DIP and SO packages is shown. It has been found empirically from these PC boards that capacitive coupling across the package of greater than 3fF (0.003pF) will diminish the rejection, and it is recommended that this proven layout be copied into designs. The key to the success of the SOL PC board #028 is the use of a ground plane guard around pin 13, the feedback pin.

All Hostile Crosstalk

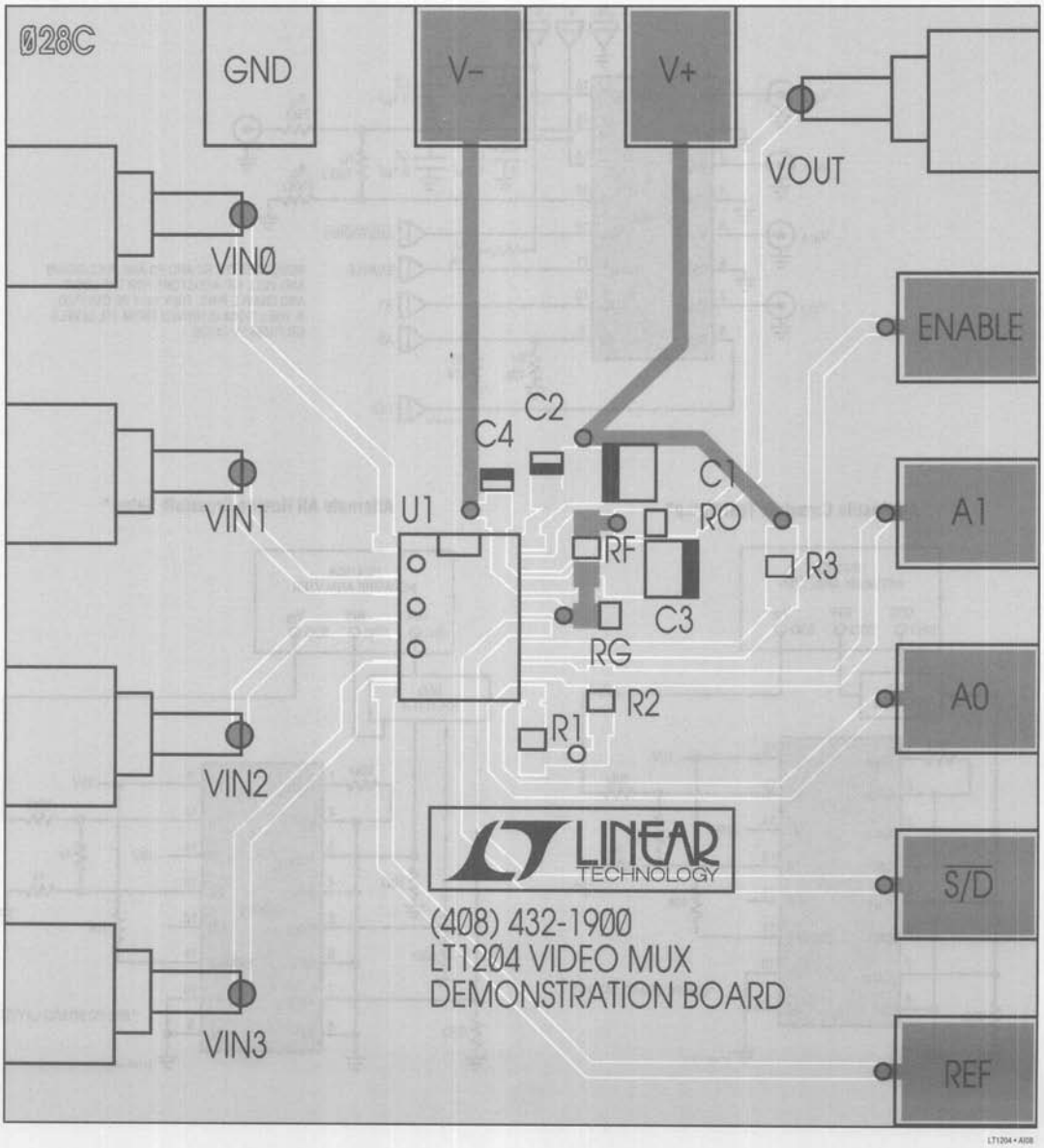


P-DIP PC Board #029, Component Side



APPLICATIONS INFORMATION

SOL PC Board #028, Component Side



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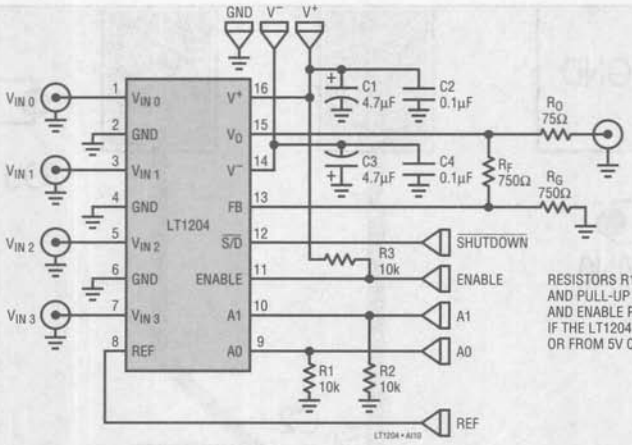
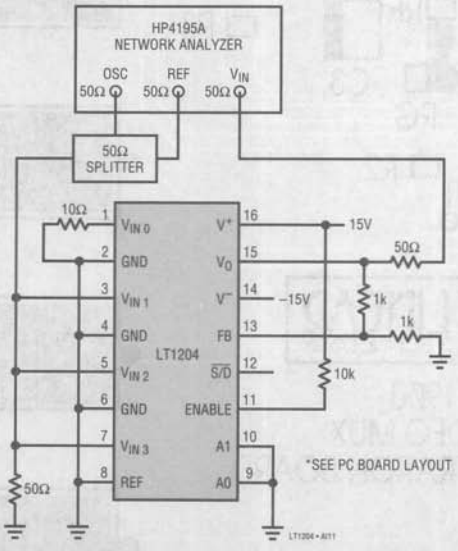
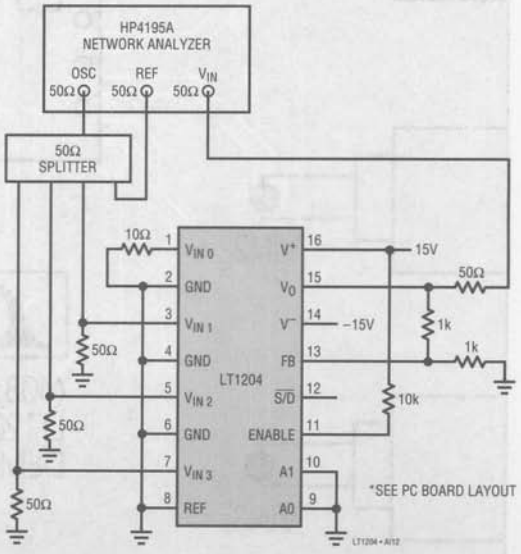
Demonstration PC Board Schematic



All Hostile Crosstalk Test Setup*



Alternate All Hostile Crosstalk Setup*

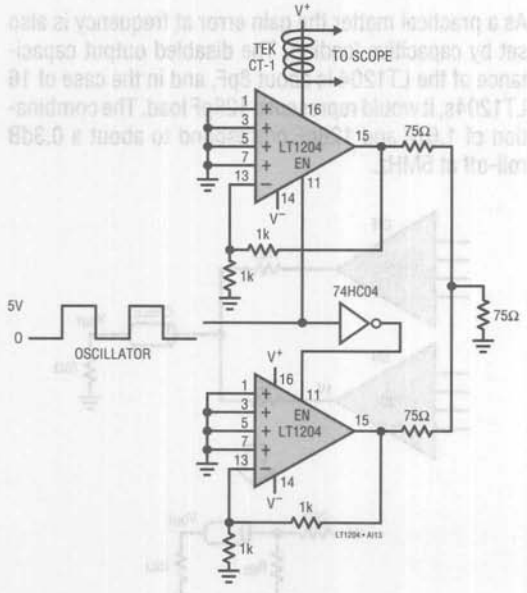


APPLICATIONS INFORMATION

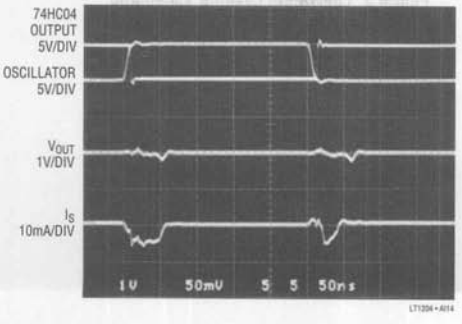
Multiplexer Expansion Pin 11 and Pin 12

To expand the number of MUX inputs, LT1204s can be paralleled by shorting their outputs together. The multiplexer disable logic has been designed to prevent shoot-through current when two or more amplifiers have their outputs shorted together. (Shoot-through current is a spike of power supply current caused by both amplifiers being on at once.)

Monitoring Supply Current Spikes



Timing and Supply Current Waveforms



The multiplexer uses a circuit to ensure the disabled amplifiers do not load or alter the cable termination. When the LT1204 is disabled (pin 11 low) the output stage is turned off and an active buffer senses the output and drives the feedback pin to the CFA (Figure 2). This bootstraps the feedback resistors and raises the true output impedance of the circuit. For the condition where $R_F = R_G = 1k$, the Disable Output Resistance is typically raised to 25k and drops to 20k for $A_V = 10$, $R_F = 2k$ and $R_G = 222\Omega$ due to loading of the feedback buffer. Operating the Disable feature with $R_G < 100\Omega$ is not recommended.

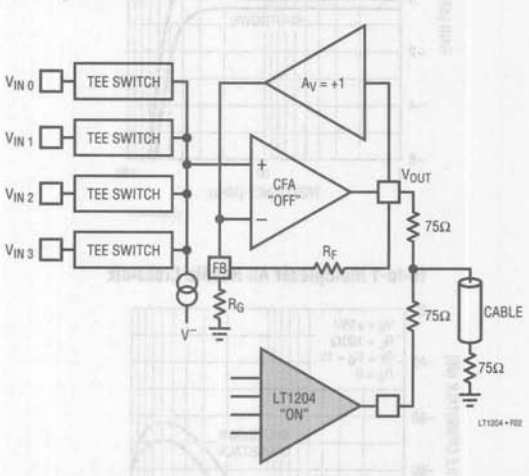


Figure 2. Active Buffer Drives FB Pin 13

A shutdown feature (pin 12 low) reduces the supply current to 1.5mA and lowers the power dissipation when the LT1204 is not in use. If the part is shut down, the bootstrapping is inoperative and the feedback resistors will load the output. If the CFA is operated at a gain of +1, however, the feedback resistor will not load the output even in shutdown because there is no resistive path to ground, but there will be a –6dB loss through the cable system.

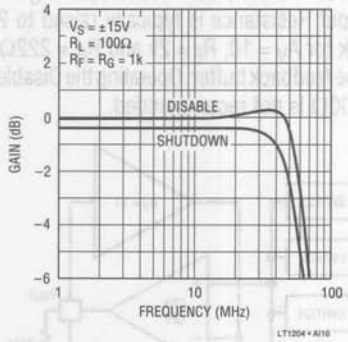
A frequency response plot shows the effect of using the disable feature versus using the shutdown feature. In this example 4 LT1204s were connected together at their outputs forming a 16-to-1 MUX. The plot shows the effect of the bootstrapping circuit that eliminates the

APPLICATIONS INFORMATION

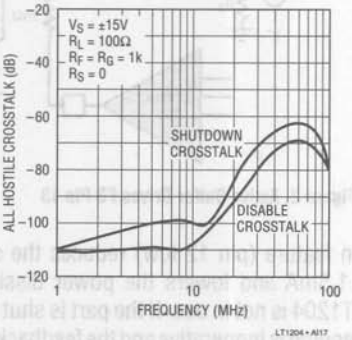
improper cable termination due to feedback resistors loading the cable.

The limit to the number of expanded inputs is set by the acceptable error budget of the system.

16-to-1 MUX Response Using Disable vs Shutdown



16-to-1 Multiplexer All Hostile Crosstalk



For a 64-to-1 MUX we need 16 LT1204s. The equivalent load resistance due to the feedback resistor R_{EQ} in Disable is 25k/15 = 1.67k. See Figure 3.

$$V_O = \frac{75R_{EQ}}{75(75) + 150R_{EQ}}, V_O = 0.489V$$

This voltage represents a 2.1% loading error. If the shutdown feature is used instead of the disable feature, then the LT1204 could expand to only an 8-to-1 MUX for the same error.

As a practical matter the gain error at frequency is also set by capacitive loading. The disabled output capacitance of the LT1204 is about 8pF, and in the case of 16 LT1204s, it would represent a 128pF load. The combination of 1.67k and 128pF correspond to about a 0.3dB roll-off at 5MHz.

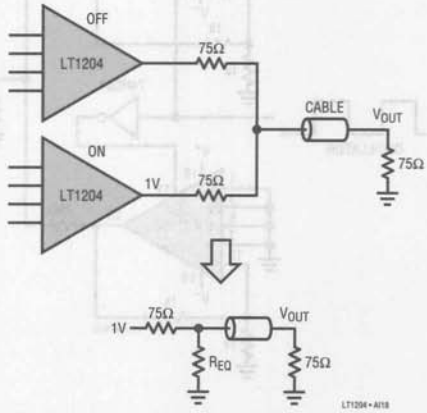


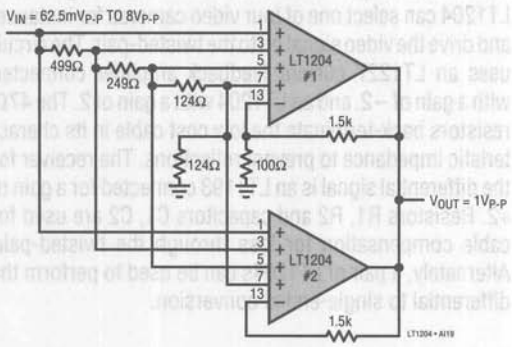
Figure 3. Equivalent Loading Schematic

TYPICAL APPLICATIONS

Programable Gain Amplifier (PGA)

Two LT1204s and seven resistors make a Programable Gain Amplifier with a 128-to-1 gain range. The gain is proportional to 2^N where N is the 3-bit binary value of the select logic. An input attenuator alters the input signal by 1, 0.5, 0.25 and 0.125 to form an amplifier with a gain of 16, 8, 4, 2, when LT1204 #1 is selected. LT1204 #2 is connected to the same attenuator. When enabled (LT1204 #1 disabled), it results in gain of 1, 0.5, 0.25 and 0.125. The wide input common-mode range of the LT1204 is needed to accept inputs of $8V_{P-P}$.

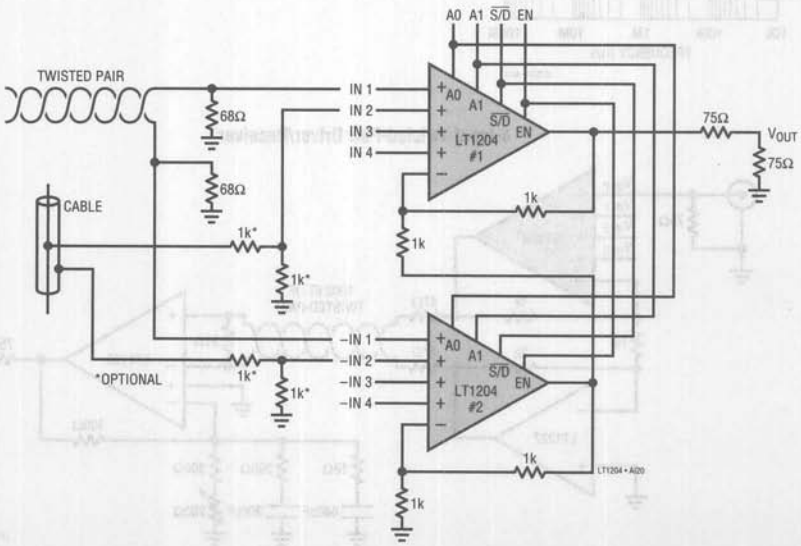
Programable Gain Amplifier Accepts Inputs from $62.5mV_{P-P}$ to $8V_{P-P}$



4-Input Differential Receiver

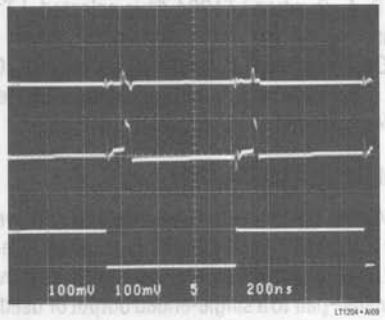
LT1204s can be connected inverting and noninverting as shown to make a 4-input differential receiver. The receiver can be used to convert differential signals sent over a low cost twisted-pair to a single-ended output or used in video loop-thru connections. The logic inputs A0 and A1 are tied together because the same channels are selected on each LT1204. By using the Disable feature, the number of differential inputs can be increased by adding pairs of LT1204s and tying the outputs of the noninverting LT1204s (#1) together. Switching transients are reduced in this receiver because the transient from LT1204 #2 subtracted from the transient of LT1204 #1.

4-Input Differential Receiver

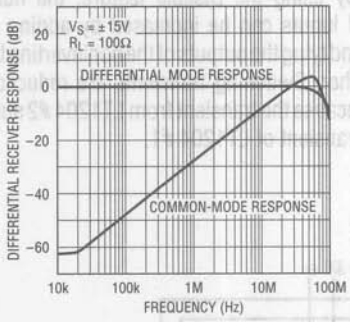


TYPICAL APPLICATIONS

Differential Receiver Switching Waveforms



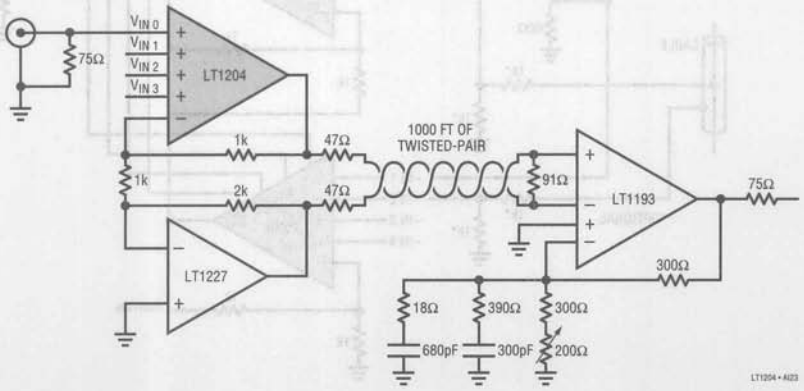
Differential Receiver Response



4-Input Twisted-Pair Driver

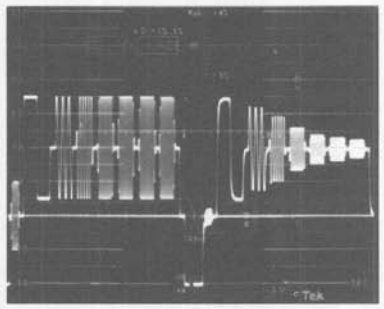
It is possible to send and receive color composite video signals appreciable distances on a low cost twisted-pair. The cost advantage of this technique is significant. Standard 75Ω RG-59/U coaxial cable cost between 25¢ and 50¢ per foot. PVC twisted-pair is only pennies per foot. Differential signal transmission resists noise because the interference is present as a common-mode signal. The LT1204 can select one of four video cameras for instance, and drive the video signal on to the twisted-pair. The circuit uses an LT1227 current feedback amplifier connected with a gain of –2, and an LT1204 with a gain of 2. The 47Ω resistors back-terminate the low cost cable in its characteristic impedance to prevent reflections. The receiver for the differential signal is an LT1193 connected for a gain of +2. Resistors R1, R2 and capacitors C1, C2 are used for cable compensation for loss through the twisted-pair. Alternately, a pair of LT1204s can be used to perform the differential to single-ended conversion.

4-Input Twisted-Pair Driver/Receiver



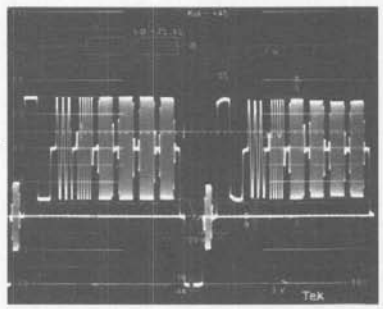
TYPICAL APPLICATIONS

Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair, No Cable Compensation



LT1204 • A04

Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair, with Cable Compensation



LT1204 • A05

SECTION 3—INSTRUMENTATION AMPLIFIERS

SECTION 3—INSTRUMENTATION AMPLIFIERS

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PROPRIETARY PRODUCTS

LTC1043, Dual Instrumentation Switched Capacitor Building Block ..... '90DB 11-15

LTC1100, Precision, Zero Drift Instrumentation Amplifier ..... '92DB 3-4

LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100) ..... '92DB 3-11

LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100) ..... '92DB 3-23

LT1193, Video Difference Amplifier, Adjustable Gain ..... '92DB 2-159

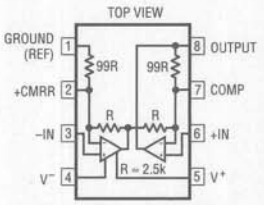
LT1194, Video Difference Amplifier, Gain of 10 ..... '92DB 2-171

Complete Instrumentation Amplifiers in 8-Pin Packages

- LTC1100: Zero Offset, Drift; Gain of 100
- LT1101: Micropower, Single Supply; Gain of 10 or 100
- LT1102: High Speed JFET Input; Gain of 10 or 100

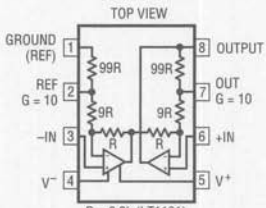
PARAMETER	LTC1100A $V_S = \pm5V$	LT1101A $V_S = 5V$	LT1102A $V_S = \pm15V$
Offset (Max)	10µV	160µV	600µV
Offset Drift (Max)	100nV/°C	2µV/°C	8µV/°C
Bias Current (Max)	50pA	8nA	40pA
Noise (0.1Hz to 10Hz)	1.9µV$_{P-P}$ Typ	0.9µV$_{P-P}$ Typ	2.8µV$_{P-P}$ Typ
Gain	100/10 (SOL PKG)	10/100	10/100
Gain Error (Max)	0.05%	0.05%	0.05%
Gain Drift	4ppm/°C Typ	4ppm/°C Max	18ppm/°C Max
Gain Nonlinearity (Max)	8ppm	8ppm	14ppm
CMRR (G = 100)(Min)	104dB	95dB	84dB
Power Supply (Max)	Single, Dual, 16V	Single, Dual, 44V	Dual, 44V
Supply Current (Max)	2.8mA	130µA	5mA
Slew Rate	1.5V/µs Typ	0.06V/µs Min	21V/µs Min (6:10)
Bandwidth (G = 10)	18kHz Typ	22kHz Min	2MHz Min

LTC1100



N8 PACKAGE 8-LEAD PLASTIC DIP J8 PACKAGE 8-LEAD CERAMIC DIP

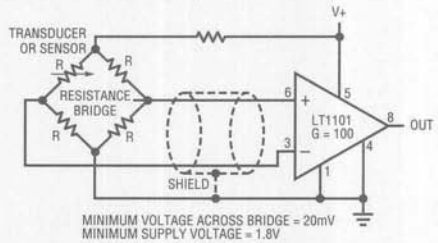
LT1101/LT1102



R = 9.2k (LT1101)
R = 1.8k (LT1102)

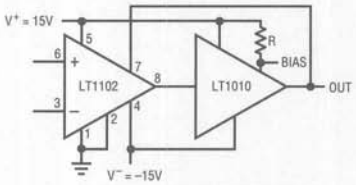
N8 PACKAGE 8-LEAD PLASTIC DIP J8 PACKAGE 8-LEAD CERAMIC DIP

Differential Voltage Amplification from a Resistance Bridge (Single 5V Powered)



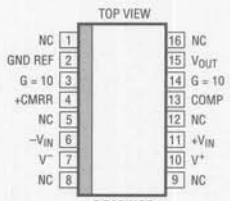
MINIMUM VOLTAGE ACROSS BRIDGE = 20mV
MINIMUM SUPPLY VOLTAGE = 1.8V

Wideband Instrumentation Amplifier with ±150mA Output Current



OUTPUT = ±10V INTO 75Ω TO 330kHz (R = 50Ω)
±10V INTO 200Ω TO 330kHz (R = 200Ω)
DRIVES 2.2nF CAP LOAD
GAIN = 10, DEGRADED 0.01% DUE TO LT1010

LTC1100CS



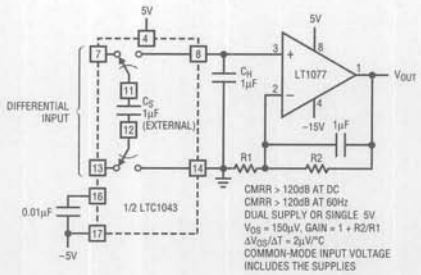
S PACKAGE 16-LEAD PLASTIC SOL

Dual Precision Instrumentation Switched Capacitor Building Block: LTC1043

- Up to 120dB CMRR
- Adjustable Gain-Set by Output Op Amp
- Offset and Offset Drift as Low as Output Amp Specs
- Precise, Charge-Balanced Switching
- Up to 5MHz Clock Rate
- Internal or External Clock

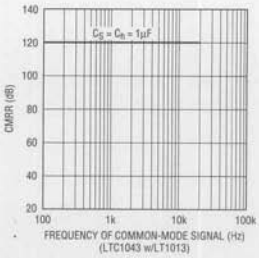
PARAMETER	LTC1043 (USING LTC1050 AMPLIFIER)
Offset	0.5µV
Offset Drift	50nV/°C
Bias Current	10pA
Noise (0.1Hzk to 10Hz)	1.6µV
Gain	Resistor Programmable
Gain Error	Resistor Limited 0.001% Possible
Gain Drift	Resistor Limited <1ppm/°C Possible
Gain Nonlinearity	Resistor Limited 1ppm Possible
CMRR	120dB
Power Supply	Single, Dual (18V, ±9V Max)
Supply Current	2mA
Slew Rate	1mV/ms
Bandwidth	10Hz

Instrumentation Amplifier



CMRR > 120dB AT DC
CMRR > 120dB AT 60Hz
DUAL SUPPLY OR SINGLE 5V
V_{OS} = 150µV, GAIN = 1 + R2/R1
$\Delta V_{OS}/\Delta T$ = 2µV/°C
COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

CMRR vs Frequency



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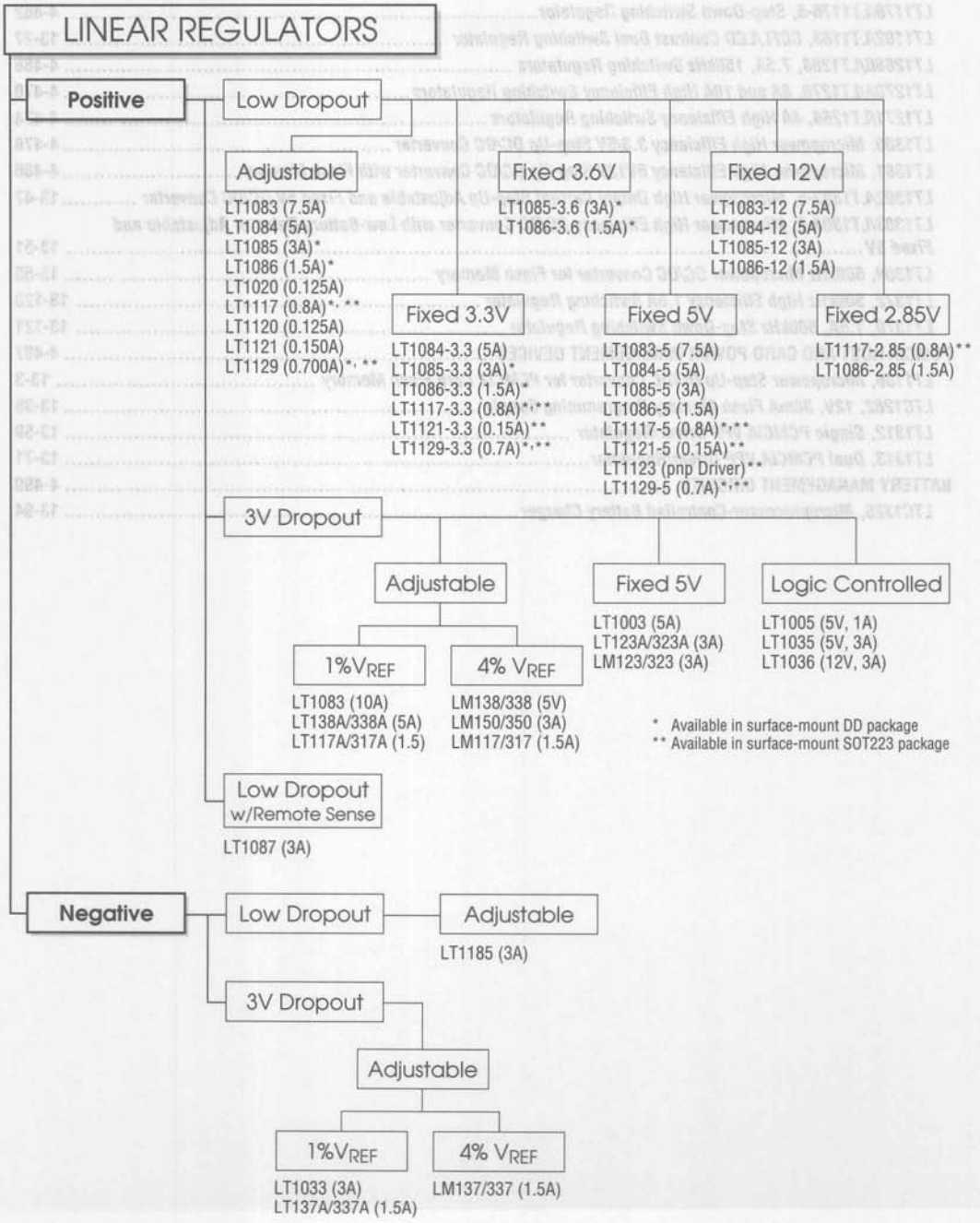
LINEAR REGULATORS



SWITCH CURRENT / OSCILLATOR FREQUENCY →	OPTIMIZED FOR STEP-UP OR FLYBACK CONFIGURATIONS				OPTIMIZED FOR STEP-DOWN OR INVERTING APPLICATIONS	OFF-LINE AND/OR PWM CONTROLLERS		
	40kHz	60kHz	100kHz	150kHz	100kHz	200kHz	500kHz	1MHz
10A		LT1270A						
8A		LT1270						
7.5A				LT1268				
5A	LT1070		LT1170		LT1074			
4A		LT1271	LT1269					
2.5A	LT1071		LT1171					
2A					LT1076*	LT1103		
1.25A	LT1072		LT1172		LT1176*			
1A		LT1082						
External						LT1105	LT124x	LT1246

	INPUT VOLTAGE (V) MIN	MAX	MAXIMUM SWITCH VOLTAGE (V)	MAX RATED SWITCH CURRENT (A)	PACKAGES AVAILABLE
LT1070	3	40	65	5	K, T
LT1070HV	3	60	75	5	K, T
LT1071	3	40	65	2.5	K, T
LT1071HV	3	60	75	2.5	K, T
LT1072	3	40	65	1.25	K, T, N8, S8, S16
LT1072HV	3	60	75	1.25	K, T
LT1074	8	40	65	5	K, Q, T
LT1074HV	8	60	75	5	K, T
LT1076*	8	40	65	2	K, R, T, Y
LT1076HV	8	60	75	2	K, R, T, Y
LT1082	3	75	100	1	J8, N8, S, T
LT1170	3	40	65	5	K, T, Q
LT1170HV	3	60	75	5	K, T
LT1171	3	40	65	2.5	K, Q, T
LT1171HV	3	60	75	2.5	K, T
LT1172	3	40	65	1.25	K, T, N8, S8, S16, Q
LT1172HV	3	60	75	1.25	K, T
LT1176*	8	38	38	1.25	N, S
LT1268	3	30	60	7.5	T, Q
LT1269	3	30	60	4	S, T, Q
LT1270A	3	30	60	10	T
LT1270	3	30	60	8	T
LT1271	3	30	60	4	T, Q

*Fixed 5V output version available

Commercial Temperature

CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	MIL/ IND TEMP	FEATURE/COMMENTS
10.0	Pos Adj	LT1038CK	Steel TO-3	35	1.2 to 33	M	2% V_{OUT} Tol, Plug In Compatible with 317, 350, 338 Types
	Switching	LT1270ACT	TO-220	30	Adjustable		Self-Contained 60kHz PWM and 10 Amp Switch in a 5-Pin Package
8.0	Switching	LT1270CT	TO-220	30	Adjustable		Self-Contained 60kHz PWM and 8 Amp Switch in a 5-Pin Package
7.5	Pos Fixed	LT1083CK-5	Steel TO-3	30	5	M	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1083CP-5	Plastic TO-3P	30	5		
		LT1083CK-12	Steel TO-3	30	12	M	
		LT1083CP-12	Plastic TO-3P	30	12		
	Pos Adj	LT1083CK	Steel TO-3	30	1.2 to 29	M, I	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT1083CP	Plastic TO-3P	30	1.2 to 29		
	Switching	LT1268CQ	Plastic DD	30	Adjustable		Self-Contained 150kHz PWM and 7.5A Switch in 5-Pin Package
		LT1268CT	TO-220	30	Adjustable		
5.0	Pos Fixed	LT1003CK	Steel TO-3	20	5	M	2% V_{OUT} Tol
		LT1003CP	Plastic TO-3P	20	5		
		LT1084CT-3.3	TO-220	30	3.3		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1084CK-5	Steel TO-3	30	5	M	
		LT1084CP-5	Plastic TO-3P	30	5		
		LT1084CT-5	TO-220	30	5		
		LT1084CK-12	Steel TO-3	30	12	M	
		LT1084CP-12	Plastic TO-3P	30	12		
		LT1084CT-12	TO-220	30	12		
	Pos Adj	LT338AK LM338K	Steel TO-3	35	1.2 to 32	M	LT338A Has 1% V_{REF} Tol
		LT338AP LM338P	Plastic TO-3P	35	1.2 to 32		
		LT1084CK	Steel TO-3	30	1.2 to 29	M, I	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT1084CP	Plastic TO-3P	30	1.2 to 29		
		LT1084CT	TO-220	30	Adjustable		
		LT1087CT	TO-220	30	1.2 to 29		Low Dropout (1.2V) with Kelvin Sense
	Switching	LT1070CK	Steel TO-3	40	Adjustable	M, I	Self-Contained 40kHz PWM and 5A Switch in a 5-Pin Package
		LT1070CT	TO-220	40	Adjustable	I	
		LT1070HVCK	Steel TO-3	60	Adjustable	M	
		LT1070HVCT	TO-220	60	Adjustable	I	
		LT1074CK	Steel TO-3	45	Adjustable	M	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package
		LT1074CT	TO-220	45	Adjustable	I	
		LT1074CY	7-Lead TO-220	45	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 7-Pin Package
		LT1074HVCK	Steel TO-3	64	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package
		LT1074HVCT	TO-220	64	Adjustable	I	
		LT1074HVCY	7-Lead TO-220	64	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 7-Pin Package
		LT1170CK	Steel TO-3	40	Adjustable	M	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package
		LT1170CQ	Plastic DD	30	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package
		LT1170CT	TO-220	40	Adjustable	I	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package
		LT1170HVCT	TO-220	60	Adjustable		
4.0	Switching	LT1269CQ	Plastic DD	30	Adjustable		Self-Contained 100kHz PWM and 4A Switch in 5-Pin Package
		LT1269CT	TO-220	30	Adjustable		
		LT1269CS	20-Lead SOIC	30	Adjustable		Self-Contained 100kHz PWM and 4A Switch in 20-Lead SOIC Pkg
		LT1271CQ	Plastic DD	30	Adjustable		Self-Contained 60kHz PWM and 4A Switch in 5-Pin Package
		LT1271CT	TO-220	30	Adjustable		
3.0	Pos Fixed	LT323AK LM323K	Steel TO-3	20	5	M	LT323A Has 1% V_{OUT} Tol
		LT323AT	TO-220	20	5		LT323A Has 1% V_{OUT} Tol
		LT1085CT-3.3	TO-220	30	3.3		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CM-3.3	Plastic DD	30	3.3		Low Dropout (1.2V), 1% V_{OUT} Tol 3-Pin Surface Mount Package
		LT1085CM-3.6	Plastic DD	30	3.6		
		LT1085CT-3.6	TO-220	30	3.6		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CK-5	Steel TO-3	30	5	M, I	
		LT1085CT-5	TO-220	30	5	I	
		LT1085CK-12	Steel TO-3	30	12	M, I	
		LT1085CT-12	TO-220	30	12	I	
	Pos Adj	LT350AK LM350K	Steel TO-3	35	1.2 to 33	M	LT350A Has 1% V_{REF} Tol
		LT350AT LM350T	TO-220	35	1.2 to 33		
		LT350AP LM350P	Plastic TO-3P	35	1.2 to 33		
		LT1085CK	Steel TO-3	30	1.2 to 29	M, I	Low Dropout (1.2V), Pin Compatible with 317, 350 Types
		LT1085CT	TO-220	30	1.2 to 29	I	

Commercial Temperature

CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	MIL/IND TEMP	FEATURE/COMMENTS
3.0	Neg Adj	LT1033CK LT1033CP LT1033CT	Steel TO-3 Plastic TO-3P TO-220	35 35 35	–1.2 to –32 –1.2 to –32 –1.2 to –32	M	2% V_{REF} Tol
		LT1185CT	TO-220	35	–2.5 to –25	M, I	Low Dropout (0.75V) with Prog Current Limit and Shutdown
	Dual Pos Fixed	LT1035CK LT1035CT	Steel TO-3 TO-220	20 20	Two 5V Outputs Two 5V Outputs	M	Logic Controlled Main Output Voltage, 75mA Auxiliary Output
	Positive	LT1036CK LT1036CT	Steel TO-3 TO-220	30 30	12, 5 12, 5	M	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
2.5	Switching	LT1071CK LT1071CT LT1071HVCK LT1071HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	Adjustable Adjustable Adjustable Adjustable	M I M I	Self-Contained 40kHz PWM and 2.5A Switch in a 5-Pin Package
		LT1171CK LT1171CT LT1171HVCT	Steel TO-3 TO-220 TO-220	40 40 60	Adjustable Adjustable Adjustable	M I	Self-Contained 100kHz PWM and 2.5A Switch in a 5-Pin Package
		LT1171CQ	Plastic DD	40	Adjustable		Self-Contained 100kHz PWM and 2.5A Switch in a 5-Pin Sur Mt Pack
2.0	Switching	LT1076CK	Steel TO-3	45	Adjustable	M	Self-Contained 100kHz PWM and 2A Switch
		LT1076CR	Plastic DD	45	Adjustable		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Sur Mt Pack
		LT1076CT LT1076HVCK	TO-220 Steel TO-3	45 64	Adjustable Adjustable	I	Self-Contained 100kHz PWM and 2A Switch
		LT1076HVCT	TO-220	64	Adjustable	I	Self-Contained 100kHz PWM and 2A Switch in a 5-Pin Package
		LT1076CY-5 LT1076HVCY-5	7-Lead TO-220 7-Lead TO-220	45 64	5 5		100kHz PWM and 2A Switch in 7-Pin Package with Shutdown and Fixed 5V Output
		LT1076CR-5	Plastic DD	45	5		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Sur Mt Pack
		LT1076CY LT1076HVCY	7-Lead TO-220 7-Lead TO-220	45 64	Adjustable Adjustable		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Package
		LT1103CY	7-Lead TO-220	30	Adjustable	I	Designed for AC Line Powered Applications, Minimum External Components Required for 75W Isolated Power Supply
		LT1302CN8 LT1302CS8	8-Pin Plastic DIP 8-Pin Plastic SOIC	10 10	Adjustable Adjustable		Micropower Switching Regulator Works Down to 2V Input and Produces 5V at 600mA
1.5	Pos Fixed	LT1086CT-2.85	TO-220	30	2.85		Intended for SCSI-2 Active Termination
0.5 to 1.5	Pos Fixed	LT1086CT-3.3 LT1086CM-3.3	TO-220 Plastic DD	30 30	3.3 3.3		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1086CT-3.6 LT1086CM-3.6	TO-220 Plastic DD	30 30	3.6 3.6		Low Dropout (1.2V) 1% V_{OUT} Tol
		LT1086CK-5 LT1086CT-5 LT1086CK-12 LT1086CT-12	Steel TO-3 TO-220 Steel TO-3 TO-220	30 30 30 30	5 5 12 12	M,I I M, I I	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT317AK LM317K LT317AH LM317H LT317AT LM317T	Steel TO-3 TO-39 TO-220	40 40 40	1.2 to 37 1.2 to 37 1.2 to 37	M M	LT317A Has 1% V_{REF} Tol
		LT1086CK LT1086CT LT1086CH	Steel TO-3 TO-220 TO-39	30 30 30	1.2 to 29 1.2 to 29 1.2 to 29	M, I I M	Low Dropout (1.2V),1% V_{REF} Tol Pin-Compatible with 317 Types
		LT1086CM	Plastic DD	30	1.2 to 29		Low Dropout (1.2V), 1% V_{REF} Tol 3-Pin Surface Mount Package
	Neg Adj	LT337AK LM337K LT337AH LM337H LT337AT LM337H	Steel TO-3 TO-39 TO-220	40 40 40	–1.2 to –37 –1.2 to –37 –1.2 to –37	M M	LT337A Has 1% V_{REF} Tol
	Pos Adj High Voltage	LT317AHVK LM317HVK LT317AHVH LM317HVH	Steel TO-3 TO-39	60 60	1.2 to 57 1.2 to 57	M M	LT317AHV Has 1% V_{REF} Tol
	Neg Adj High Voltage	LT337AHVK LM337HVK LT337AHVH LM337HVH	Steel TO-3 TO-39	50 50	–1.2 to –47 –1.2 to –47	M M	LT337AHV Has 1% V_{REF} Tol
1.25	Switching	LT1072CK LT1072CT LT1072HVCK LT1072HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	Adjustable Adjustable Adjustable Adjustable	M, I I M, I I	Self-Contained 40kHz PWM and 1.25A Switch in a 5-Pin Package
		LT1072CJ8 LT1072CN8 LT1072CS8	8-Pin CERDIP 8-Pin Plastic DIP 8-Pin Plastic SOIC	40 40 40	Adjustable Adjustable Adjustable	M I	Self-Contained 40kHz PWM and 1.25A Switch

4

Commercial Temperature

CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	MIL/IND TEMP	FEATURE/COMMENTS
1.25	Switching	LT1172CK	Steel TO-3	40	Adjustable	M	Self-Contained 100kHz PWM and 1.25A Switch
		LT1172CT	TO-220	40	Adjustable		
		LT1172HVCT	TO-220	60	Adjustable		
		LT1172CJ8	8-Pin CERDIP	40	Adjustable	M	
		LT1172CN8	8-Pin Plastic DIP	40	Adjustable	I	
		LT1172CQ	Plastic DD	40	Adjustable		
		LT1172CS8	8-Pin Plastic SOIC	40	Adjustable	I	
		LT1176CN8	8-Pin Plastic DIP	38	Adjustable		Self-Contained 100kHz PWM and 1.2A Switch in 8-Pin DIP Package
		LT1176CN8-5	8-Pin Plastic DIP	38	5		
		LT1176CS	20-Lead SOIC	38	Adjustable		Self-Contained 100kHz PWM and 1.2A Switch in 20-Lead SOIC
		LT1176CS-5	20-Lead SOIC	38	5		
1.0	Dual Pos Fixed	LT1005CK	Steel TO-3	20	Two 5V Outputs	M	Logic Controlled Main Output Voltage
		LT1005CT	TO-220	20	Two 5V Outputs		
	Switching	LT1073CN8	8-Pin Plastic DIP	15	Adjustable		Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions)
		LT1073CS8	8-Pin Plastic SOIC	15	Adjustable		
		LT1073CN8-5	8-Pin Plastic DIP	15	5		
		LT1073CS8-5	8-Pin Plastic SOIC	15	5		
		LT1073CN8-12	8-Pin Plastic DIP	15	12		
		LT1073CS8-12	8-Pin Plastic SOIC	15	12		
		LT1082CN8	8-Pin Plastic DIP	75	Adjustable	I	60kHz PWM and 1A, 100V Switch
		LT1082CT	TO-220	75	*	I	60kHz PWM and 1A, 100V Switch
		LT1107CN8	8-Pin Plastic DIP	36	Adjustable	M	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$, Allows Use of Surface Mount Inductors.
		LT1107CS8	8-Pin Plastic SOIC	36	Adjustable		
		LT1107CN8-5	8-Pin Plastic DIP	36	5	M	
		LT1107CS8-5	8-Pin Plastic SOIC	36	5		
		LT1107CN8-12	8-Pin Plastic DIP	36	12	M	
		LT1107CS8-12	8-Pin Plastic SOIC	36	12		
		LT1108CN	8-Pin Plastic DIP	36	Adjustable		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions) Optimized for $V_{IN} \geq 2V$
		LT1108CS	8-Pin Plastic SOIC	36	Adjustable		
		LT1108CN-5	8-Pin Plastic DIP	36	5		
		LT1108CS-5	8-Pin Plastic SOIC	36	5		
		LT1108CN-12	8-Pin Plastic DIP	36	12		
		LT1108CS-12	8-Pin Plastic SOIC	36	12		
		LT1109CZ-5	3-Pin TO-92	36	5		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$. Available in 3-Pin TO-92 Package. N8/S8 Versions Also Offer Shutdown Feature. 12V Version Ideal for Flash Memory Vpp Pulse Generation from 5V or 3V
		LT1109CZ-12	3-Pin TO-92	36	12		
		LT1109CN8-5	8-Pin Plastic DIP	36	5		
		LT1109CS8-12	8-Pin Plastic SOIC	36	5		
		LT1109CN8-5	8-Pin Plastic DIP	36	12		
		LT1109CS8-12	8-Pin Plastic SOIC	36	12		
		LT1109ACN	8-Pin Plastic DIP	36	Adjustable		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$. 12V Version Ideal for Flash Memory Vpp Pulse Generation from 5V or 2V. Includes Shutdown Feature.
		LT1109ACS	8-Pin Plastic SOIC	36	Adjustable		
		LT1109ACN-5	8-Pin Plastic DIP	36	5		
		LT1109ACS-5	8-Pin Plastic SOIC	36	5		
		LT1109ACN-12	8-Pin Plastic DIP	36	12		
		LT1109ACS-12	8-Pin Plastic SOIC	36	12		
		LT1110CN8	8-Pin Plastic DIP	15	Adjustable		Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions). 60kHz Oscillator Allows Use of Surface Mount Inductors
		LT1110CS8	8-Pin Plastic SOIC	15	Adjustable		
		LT1110CN8-5	8-Pin Plastic DIP	15	5		
		LT1110CS8-5	8-Pin Plastic SOIC	15	5		
		LT1110CN8-12	8-Pin Plastic DIP	15	12		
		LT1110CS8-12	8-Pin Plastic SOIC	15	12		
		LT1111CN8	8-Pin Plastic DIP	36	Adjustable	M	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$. 70kHz Oscillator Allows Use of Surface Mount Inductors
		LT1111CS8	8-Pin Plastic SOIC	36	Adjustable	I	
		LT1111CN8-5	8-Pin Plastic DIP	36	5	M	
		LT1111CS8-5	8-Pin Plastic SOIC	36	5		
		LT1111CN8-12	8-Pin Plastic DIP	36	12	M	
		LT1111CS8-12	8-Pin Plastic SOIC	36	12		
		LT1173CN8	8-Pin Plastic DIP	36	Adjustable		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$
		LT1173CS8	8-Pin Plastic SOIC	36	Adjustable		
		LT1173CN8-5	8-Pin Plastic DIP	36	5		
		LT1173CS8-5	8-Pin Plastic SOIC	36	5		
		LT1173CN8-12	8-Pin Plastic DIP	36	12		
		LT1173CS8-12	8-Pin Plastic SOIC	36	12		
		LT1300CN8	8-Pin Plastic DIP	7	3.3/5		Micropower Switching Regulator Works Down to 1.8V Input. Includes Selectable 3.3V or 5V Output and Shutdown
		LT1300CS8	8-Pin Plastic SOIC	7	3.3/5		

Commercial Temperature

CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	MIL/IND TEMP	FEATURE/COMMENTS
1.0	Switching	LT1301CN8	8-Pin Plastic DIP	10	5/12	I	Micropower Switching Regulator Works Down to 1.8V Input.
		LT1301CS8	8-Pin Plastic SOIC	10	5/12	I	Optimized for Flash Memory VPP Generation from 5V or 2V
		LT1303CN8	8-Pin Plastic DIP	7	Adjustable		Micropower Switching Regulator Works Down ot 1.8V Input.
		LT1303CS8	8-Pin Plastic SOIC	7	Adjustable		Includes Low-Battery Detector
800mA	Pos Fixed	LT1117CST	3-Pin SOT-223	15	Adjustable		Adjustable Low Dropout Regulator, SOT-223 Package
		LT1117CST-2.85	3-Pin SOT-223	12	2.85		Active SCSI-2 Terminator, SOT-223 Package
		LT1117CST-3.3	3-Pin SOT-223	10	3.3		3.3 Low Dropout Regulator, SOT-223 Package
		LT1117CST-5	3-Pin SOT-223	10	5		5V Low Dropout Regulator, SOT-223 Package
700mA	Pos	LT1129CS8	8-Lead SOIC	30	Adjustable		Micropower Regulator With Shutdown, Dropout Voltage = 0.4V,
		LT1129CS8-3.3	8-Lead SOIC	30	3.3	I	Reverse Battery Protection in Low Thermal Resistance SO-8 Package
		LT1129CS8-5	8-Lead SOIC	30	5	I	
		LT1129CT	5-Pin TO-220	30	Adjustable	I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V,
		LT1129CQ	Plastic DD	30	Adjustable	I	Reverse Battery Protection
		LT1129CT-3.3	5-Pin TO-220	30	3.3	I	
		LT1129CST-3.3	3-Pin SOT-223	30	3.3	I	
		LT1129CQ-3.3	5-Pin DD	30	3.3	I	
		LT1129CT-5	5-Pin TO-220	30	5	I	
		LT1129CST-5	3-Pin SOT-223	30	5	I	
		LT1129CQ-5	5-Pin DD	30	5	I	
400mA	Switching	LTC1174CN8	8-Lead DIP	13.5	Adjustable	I	Micropower Step-Down Switching Regulator With 90% Efficiency.
		LTC1174CN8-3.3	8-Lead DIP	13.5	3.3		Selectable 200mA or 400mA Current Limit. Intended for 6V-9V
		LTC1174CN8-5	8-Lead DIP	13.5	5		Battery Applications
		LTC1174CS8	8-Lead SOIC	13.5	Adjustable	I	
		LTC1174CS8-3.3	8-Lead SOIC	13.5	3.3		
		LTC1174CS8-5	8-Lead SOIC	13.5	5		
150mA	Pos	LT1121ACS8	8-Lead SOIC	30	Adjustable	I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V,
		LT1121ACS8-3.3	8-Lead SOIC	30	3.3	I	Reverse Battery Protection in Low Thermal Resistance SO-8 Package
		LT1121ACS8-5	8-Lead SOIC	30	5	I	
		LT1121CN8	8-Pin Plastic DIP	30	Adjustable	I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V,
		LT1121CS8	8-Pin Plastic SOIC	30	Adjustable	I	Reverse Battery Protection
		LT1121CN8-3.3	8-Pin Plastic DIP	30	3.3	I	
		LT1121CS8-3.3	8-Pin Plastic SOIC	30	3.3	I	
		LT1121CST-3.3	3-Pin SOT-223	30	3.3	I	
		LT1121CN8-5	8-Pin Plastic DIP	30	5	I	
		LT1121CS8-5	8-Pin Plastic SOIC	30	5	I	
		LT1121CST-5	3-Pin SOT-223	30	5	I	
125mA	Pos Adj	LT1020CJ	14-Pin CERDIP	36	4 to 30	M, I	Dropout Voltage = 0.4V, 40µA I_Q, Reference and Comparator
		LT1020CN	14-Pin Plastic	36	4 to 30	I	
		LT1020CS	16-Pin Plastic SOL	36	4 to 30	I	
		LT1120CJ8	8-Pin CERDIP	36	4 to 30	M	Dropout Voltage = 0.4V, 40µA I_Q, Reference, Comparator, Shutdown,
		LT1120CN8	8-Pin Plastic DIP	36	4 to 30	I	8-Pin Package
		LT1120CH	8-Pin TO-5	36	4 to 30		
100mA	Pos Adj	LT1431CJ8	8-Pin CERDIP	36	2.5 to 36	M	0.4% Initial Tolerance, 1% Over Temperature
		LT1431CN8	8-Pin Plastic DIP	36	2.5 to 36	I	
		LT1431CS8	8-Pin Plastic SOIC	36	2.5 to 36	I	
		LT1431CZ	TO-92	36	2.5 to 36	I	
20mA to 100mA	Switched Capacitor	LT1026CJ8	8-Pin CERDIP	10	*	M	Dual Voltage Converter, 10mA Output, $5V_{IN}$, $\pm 10V_{OUT}$
		LT1026CN8	8-Pin Plastic DIP	10	*		
		LT1026CH	8-Pin TO-5 Can	10	*	M	
		LTC1044CJ8	8-Pin CERDIP	9.5	*	M	Voltage Converter, 20mA Output
		LTC1044CN8	8-Pin Plastic DIP	9.5	*		
		LTC1044CH	8-Pin TO-5 Can	9.5	*	M	
		LTC1044CS8	8-Pin Plastic SOIC	9.5	*		
		LTC1044ACN8	8-Pin Plastic DIP	13	*	I	
		LTC1044ACS8	8-Pin Plastic SOIC	13	*	I	
		LTC1046CN8	8-Pin Plastic DIP	6	*	I	50mA Output Current, 165µA Supply Current, 35Ω Max Output
		LTC1046CS8	8-Pin Plastic SOIC	6	*	I	Impedance
		LT1054CJ8	8-Pin CERDIP	16	†	M	Voltage Converter and Regulator, 100mA Output,
		LT1054CN8	8-Pin Plastic DIP	16	†	I	25kHz Switching Rate
		LT1054CH	8-Pin TO-5 Can	16	†	M	
		LT1054CS	16-Pin Plastic SOL	16	†	I	
		LTC1144CN8	8-Pin Plastic DIP	20	*	I	Voltage Converter, 20mA Output, Up to 18V Operation
		LTC1144CS8	8-Pin Plastic SOIC	20	*	I	

* These devices are non-regulating converters.
† The available output voltage range is dependent upon the mode of operation selected.

POWER SUPPLY PRODUCTS SELECTION GUIDE

Power Factor Correction Controllers

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1248	Average Current-Mode Power Factor Corrector	N16, S16	Low Line Current Distortion, >0.99 Power Factor, Synchronization, Overvoltage Protection
LT1249	Average Current-Mode Power Factor Corrector	N8, S8	Low Parts Count, Full Feature Power Factor Correction

Regulating Pulse-Width Modulators

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1105	Off-Line Regulating Pulse Width Modulator	N8, N14	Designed for AC Line Powered Applications
LT1241 Series	500kHz Regulating Pulse Width Modulators	J8, N8, S8	Improved Replacements for UC1842, 1843, 1844, 1845
LT1246	1MHz Regulating Pulse Width Modulator	J8, N8, S8	1MHz Current Mode PWM, 1.5% V_{REF}
LT1524/LT3524	Regulating Pulse Width Modulator	J, N, S	Improved SG1524, 2% V_{REF}, Guaranteed Oscillator Accuracy
LT1525A/LT3525A LT1527A/LT3527A	Regulating Pulse Width Modulator	J, N	Improved SG1525A/1527A Switching Regulator with Undervoltage Lockout, Guaranteed Long Term Stability
LT1526/LT3526	Regulating Pulse Width Modulator	J, N	Switching Regulator Control with Soft Start, Current Limit, Metering Logic, Undervoltage Lockout, Guaranteed Long Term Stability
SG1524/SG3524	Regulating Pulse Width Modulator	J, N	Industry Standard Switching Power Supply Control Circuit
SG1525A/SG3525A	Regulating Pulse Width Modulator	J, N	More Features Than 1524 Series, 100mA Source/Sink Outputs
SG1527A/SG3527A	Regulating Pulse Width Modulator	J, N	Same as SG1525A with Inverted Output Logic
LT1846/3846 LT1847/3847	Current Mode Regulating Pulse Width Modulator	J, N	Current Mode PWM with UV Lockout, Soft Start, 1% V_{REF}, 500kHz Operation, 200mA Totem Pole Outputs

Ultra-High Efficiency Switching Regulator Controllers

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LTC1142	Dual Step-Down Switching Regulator Controller	SSOP	Dual Synchronous Switching Regulator Controllers with both 3.3V and 5V Outputs
LTC1142HV	Dual Step-Down Switching Regulator Controller	SSOP	20V Max Input Voltage Dual 3.3V and 5V Output Synchronous Switching Regulator
LTC1143	Dual Step-Down Switching Regulator Controller	S16	Dual Switching Regulator Controller with Low Parts Count and both 3.3V and 5V Outputs
LTC1147	Step-Down Switching Regulator Controller	N8, S8	Low Parts Count, 90% Efficiency Using a Single External P-Channel MOSFET
LTC1148	Step-Down Switching Regulator Controller	N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 16V Inputs.
LTC1148HV	Step-Down Switching Regulator Controller	N,S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 20V Inputs.
LTC1149	Step-Down Switching Regulator Controller	N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 48V Inputs.
LTC1159	Step-Down Switching Regulator Controller	N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 40V Inputs.
LT1432	Step-Down Switching Regulator Controller	N8, S8	Provides High Efficiency 5V Output Using LT1170 Series Regulator and Minimum External Parts
LT1432-3.3	Step-Down Switching Regulator Controller	N8, S8	Provides High Efficiency 5V Output Using LT1170 Series Regulator and Minimum External Parts

LT1103/1105 Off-Line Switching Regulators

APPLICATION	LT1105	LT1103 (Internal Sense Resistor)
Universal Off-Line	10W to Over 100W	10W to 50W
Battery Charger, Isolated Off-Line	OK	OK
Telecom, –48V Input Isolated	OK	OK
Low Voltage Isolated DC/DC (≤24V)	Requires External MOSFET	Needs No MOSFET
High Voltage Isolated DC/DC	OK	OK

Regulator Drivers

BASE DRIVE CURRENT	PART NUMBER	PACKAGE TYPE	V_{IN} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE	FEATURES/ COMMENTS
150mA	LT1123CZ	TO-92	30	5.0	Requires External PNP, 1% Output Tolerance, 600µA Quiescent Current

The following tables form a shortform component selection guide for a collection of commonly used battery-powered DC/DC conversion applications. No design is required since inductor, capacitor and resistor values are completely specified. Choose the appropriate LTC DC/DC converter for your application from the following tables.

The LT1073, LT1107, LT1108, LT1110, LT1111, LT1173, LTC1174, and LT1303 all have low-battery detection capability.

Step-Up From One Cell (1V)

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
5	40	LT1073-5	95	82	100	0	1	Lowest I_Q
	40	LT1110-5	350	27	33	0	1	Best For Surface Mount
12	15	LT1073-12	95	82	100	0	1	Lowest I_Q
	15	LT1110-12	350	27	33	0	1	Best For Surface Mount

Adjustable versions also available for V_{OUT} up to 50V

Step-Up From Two Cells (2V)

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
3.3	400	LT1300**	120	10	100	–	2	Selectable 3.3V/5V Out
5	90	LT1173-5	110	47	100	47	1	Lowest I_Q
		LT1111-5	300	18	33	47	1	Surface Mount
	150	LT1107-5	300	33	33	47	1	Surface Mount
		LT1108-5	110	100	100	47	1	Lowest I_Q
	220	LT1300**	120	10	100	–	2	Selectable 3.3V/5V Out
		LT1301**	120	10	100	–	2	Selectable 5V/12V Out
	600	LT1302	200	10	100	–	*	Highest Power Output
12	20	LT1173-12	110	47	47	47	1	Lowest I_Q
		LT1111-12	300	18	22	47	1	Surface Mount
	40	LT1107-12	300	27	33	47	1	Surface Mount
		LT1108-12	110	82	100	47	1	Lowest I_Q
	50	LT1301**	120	10	100	–	2	Selectable 5V/12V Out
	120	LT1302	200	3.3	66	–	*	Highest Power Output

*See LT1302 data sheet **For low-battery detection use LT1303

Step-Up From 5V To 12V

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
12	90	LT1173-12	110	120	100	0	1	Lowest I_Q
		LT1111-12	300	47	33	0	1	Surface Mount
	175	LT1107-12	300	60	32	0	1	Surface Mount
		LT1108-12	110	180	100	0	1	Lowest I_Q
	200	LT1301**	120	33	47	–	2	True Shutdown

**For low-battery detection use LT1303

Flash Memory VPP (12V) Generation

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	FIG	COMMENTS
5	12	60	LT1109-12	320	33	22	3	Small, SMT
		120	LT1109A-12	320	27	47	3	Small, SMT
		200	LT1301**	120	27	47	2	True Shutdown
2 Cells	12	60	LT1109A-12	320	10	22	1	All Surface Mount
		80	LT1301**	120	10	47	2	True Shutdown

**For low-battery detection use LT1303

Basic Step-Up Converters

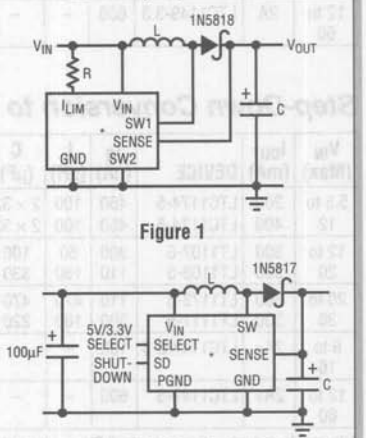


Figure 1

Figure 2

Flash Memory VPP Generator

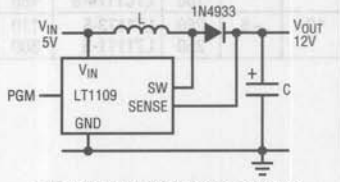


Figure 3

4

Step-Down Conversion to 3.3V

V_{IN} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	I_{PGM}	Fig	COMMENTS
4.5 to 12.5	200 425	LTC1174-3.3 LTC1174-3.3	450 450	50 50	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, Surface Mount
5 to 16	2A	LTC1148-3.3	160	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4
12 to 60	2A	LTC1149-3.3	600	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4

Step-Down Conversion to 5V

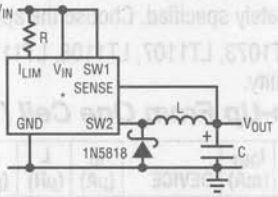
V_{IN} (Max)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R/ I_{PGM}	Fig	COMMENTS
5.5 to 12	200 400	LTC1174-5 LTC1174-5	450 450	100 100	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, Surface Mount
12 to 20	300 300	LT1107-5 LT1108-5	300 110	60 180	100 330	100 100	4 4	Surface Mount Lowest I_Q
20 to 30	300 300	LT1173-5 LT1111-5	110 300	470 180	470 220	100 100	4 4	Lowest I_Q Surface Mount
6 to 16	2A+	LTC1147/8-5	160	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4
12 to 60	2A+	LTC1149-5	600	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4

Adjustable output voltages up to 6.2V can be obtained with the adjustable versions of LT1173, LT1111, LT1107, LT1108, or LT1110.

Positive-to-Negative Voltage Conversion

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	Fig	COMMENTS
5	–5	75	LT1108-5 LT1107-5	110 300	100 33	100 33	100 100	6 6	Lowest I_Q Surface Mount
		150	LTC1174-5	450	50	2 × 33	–	7	Surface Mount
12	–5	250 250	LT1173-5 LT1111-5	110 300	470 180	220 82	100 100	6 6	Lowest I_Q Surface Mount

Step-Down Converters



*SEE TABLES FOR RECOMMENDED PART, INDUCTOR, CAPACITOR, AND RESISTOR VALUES

Figure 4

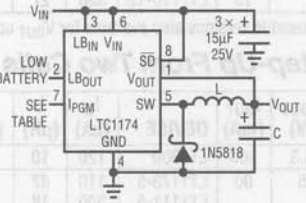
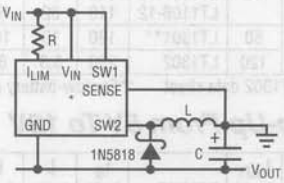


Figure 5

Positive-to-Negative Converters



*SEE TABLES FOR RECOMMENDED PART, INDUCTOR, CAPACITOR, AND RESISTOR VALUES

Figure 6

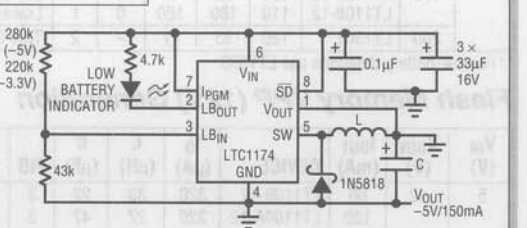


Figure 7

POWER AND MOTOR CONTROL CIRCUITS

High-Side Switch Drivers

LTC1153 – Electronic Circuit Breaker w/ Programmable Trip, Reset, Current Level
LTC1154 – Single N-Ch FET Switch Driver w/ Short-Circuit Protection
LTC1155 – Dual N-Ch FET Switch Drivers w/ Short-Circuit Protection
LTC1156 – Quad N-Ch FET Switch Drivers w/ Short-Circuit Protection
LTC1157 – Dual N-Ch FET Switch Drivers for 3.3V Operation (Also for Low Cost 5V Applications)
LT1161 – Quad High Voltage N-Channel FET Switch Drivers with Reset and Short-Circuit Portection
LTC1163 – Triple N-Ch FET Switch Drivers for 1.8V Operation (and up to 5V Applications)
LTC1165 – Triple N-Ch FET Switch Drivers for 1.8V Operation (and up to 5V Applications)
LTC1255 – Dual N-Ch FET Switch Drivers w/ Short Circuit Protection, 24V Operation

Integrated High-Side Switches

LT1188 – 1.5A HSS, Output Protected Against Inductive Kickback
Controlled Slew Rate/Low RF Noise
STATUS Line for Diagnostics
Protected Against Overtemp, Load Faults

LT1089 – 7.5A HSS Low Loss, Only 1.5V at 7.5A
Protected Against Overtemp, Overcurrent
Low Quiescent Current

Half Bridge N-Ch MOSFET Drivers

LT1158 – 5V to 30V Operation, Drives DC Motors and Switching Power Supply N-Ch MOSFET Switch Gates, On-Chip Charge Pump, Adaptive Anti-Shoot-Through, Fully Protected, 150ns Transition Times Driving 3000pF

PRODUCT	PACKAGES	FUNCTION	MIN V_{SUPPLY}	MAX V_{IN}	COMMENTS
LT1089	TO-220, TO-3	7.5A High-Side Switch	4V	20V	Low loss, Low I_Q
LTC1153	8-Pin DIP, SO	Electronic Circuit Breaker	4.5V	22V	Has Adjustable Reset Time
LTC1154	8-Pin DIP, SO	Single High-Side Driver	4.5V	22V	Single Version of LTC1155
LTC1155	8-Pin DIP, SO	Dual High-Side Driver	4.5V	22V	Good for Power Management
LTC1156	16-Pin DIP, SO	Quad High-Side Driver	4.5V	22V	Good for Multiple Supply Switching
LTC1157	8-Pin DIP, SO	Dual 3.3V High-Side Driver	2.7V	7V	Good for 3.3V Power Management
LT1158	16-Pin DIP, SO	Half-Bridge Driver	4.5V	36V	Synchronous Switching Regulators Too
LT1161	20-Pin DIP, SO	Quad High-Side Driver	8V	60V	Good for Industrial (48V) Applications
LTC1163	8-Pin DIP, SO	Triple High-Side Driver	1.8V	6V	Good for Two-Cell Power Management
LTC1165	8-Pin DIP, SO	Triple High-Side Driver	1.8V	6v	Inverted Logic Version of LTC1163
LT1188	TO-220, TO-3	1.5A High-Side Switch	5V	30V	Good for Automotive
LTC1255	8-Pin DIP, SO	Dual High-Side Driver	9V	30V	Good for Industrial (24V) Applications

SECTION 4—POWER PRODUCTS

INDUCTORLESS DC TO DC CONVERTERS

LTC1044A, 12V CMOS Voltage Converter 4-16
LT1054, Switched-Capacitor Voltage Converter with Regulator 4-26
LTC1144, Switched-Capacitor Wide Input Range Voltage Converter with Shutdown 4-38

4

12V CMOS Voltage Converter

FEATURES

- **1.5V to 12V Operating Supply Voltage Range**
- **13V Absolute Maximum Rating**
- 200μA Maximum No Load Supply Current at 5V
- Boost Pin (Pin 1) for Higher Switching Frequency
- 97% Minimum Open Circuit Voltage Conversion Efficiency
- 95% Minimum Power Conversion Efficiency
- I_S = 1.5μA with 5V Supply When OSC Pin = 0V or V^+
- High Voltage Upgrade to ICL7660/LTC1044

APPLICATIONS

- Conversion of 10V to ±10V Supplies
- Conversion of 5V to ±5V Supplies
- Precise Voltage Division: $V_{OUT} = V_{IN}/2 \pm 20ppm$
- Voltage Multiplication: $V_{OUT} = \pm nV_{IN}$
- Supply Splitter: $V_{OUT} = \pm V_S/2$
- Automotive Applications
- Battery Systems with 9V Wall Adapters/Chargers

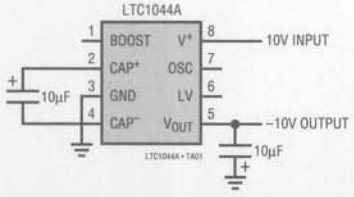
DESCRIPTION

The LTC1044A is a monolithic CMOS switched-capacitor voltage converter. It plugs in for ICL7660/LTC1044 in applications where higher input voltage (up to 12V) is needed. The LTC1044A provides several conversion functions without using inductors. The input voltage can be inverted ($V_{OUT} = -V_{IN}$), doubled ($V_{OUT} = 2V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

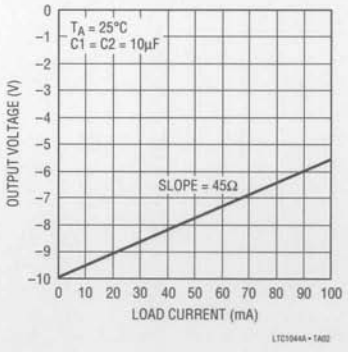
To optimize performance in specific applications, a boost function is available to raise the internal oscillator frequency by a factor of 7. Smaller external capacitors can be used in higher frequency operation to save board space. The internal oscillator can also be disabled to save power. The supply current drops to 1.5μA at 5V input when the OSC pin is tied to GND or V^+.

TYPICAL APPLICATION

Generating –10V from 10V



Output Voltage vs Load Current, V^+ = 10V

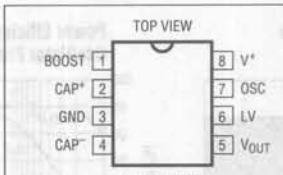


ABSOLUTE MAXIMUM RATINGS

(Note 1)

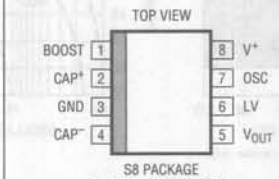
Supply Voltage 13V
Input Voltage on Pins 1, 6 and 7
(Note 2) ..... $-0.3V < V_{IN} < V^+ + 0.3V$
Current into Pin 6 ..... 20μA
Output Short-Circuit Duration
$V^+ \leq 6.5V$ ..... Continuous
Operating Temperature Range
LTC1044AC ..... 0°C to 70°C
LTC1044AI ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1044ACN8
LTC1044AIN8



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1044ACS8
LTC1044AIS8

S8 PART MARKING
1044A
1044AI

Consult factory for Military grade parts

4

ELECTRICAL CHARACTERISTICS

V^+ = 5V, C_{OSC} = 0pF, T_A = 25°C, See Test Circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1044AC MIN	LTC1044AC TYP	LTC1044AC MAX	LTC1044AI MIN	LTC1044AI TYP	LTC1044AI MAX	UNITS
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7, No Connection			60	200		60	200	μA
		$R_L = \infty$, Pins 1 and 7, No Connection, V^+ = 3V			15			15		μA
	Minimum Supply Voltage	R_L = 10k	●	1.5			1.5			V
	Maximum Supply Voltage	R_L = 10k	●			12			12	V
R_{OUT}	Output Resistance	I_L = 20mA, f_{OSC} = 5kHz				100			100	Ω
			●			120			130	Ω
		V^+ = 2V, I_L = 3mA, f_{OSC} = 1kHz	●			310			325	Ω
f_{OSC}	Oscillator Frequency	V^+ = 5V, (Note 3)	●	5			5			kHz
		V^+ = 2V	●	1			1			kHz
P_{EFF}	Power Efficiency	R_L = 5k, f_{OSC} = 5kHz		95	98		95	98		%
	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9		%
	Oscillator Sink or Source Current	V_{OSC} = 0V or V^+								
		Pin 1 (BOOST) = 0V	●			3			3	μA
		Pin 1 (BOOST) = V^+	●			20			20	μA

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

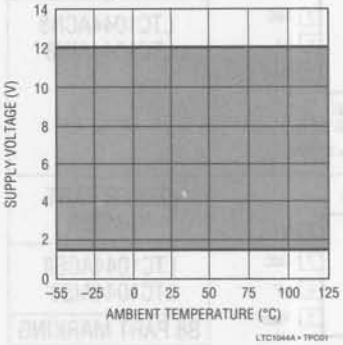
Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044A.

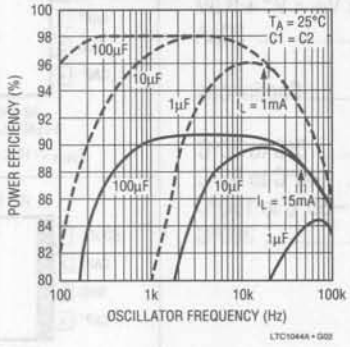
Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS Using the Test Circuit

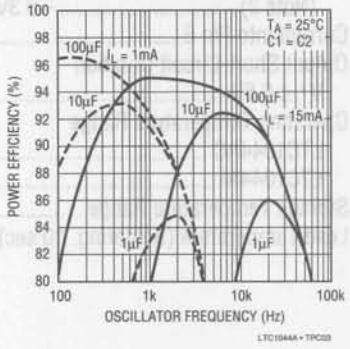
Operating Voltage Range vs Temperature



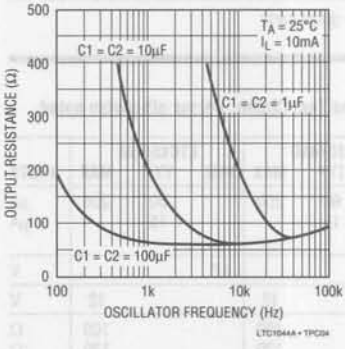
Power Efficiency vs Oscillator Frequency, V⁺ = 5V



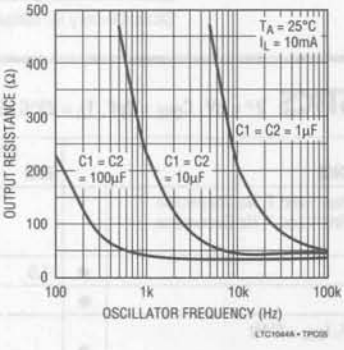
Power Efficiency vs Oscillator Frequency, V⁺ = 10V



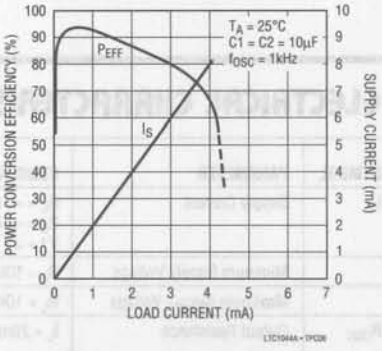
Output Resistance vs Oscillator Frequency, V⁺ = 5V



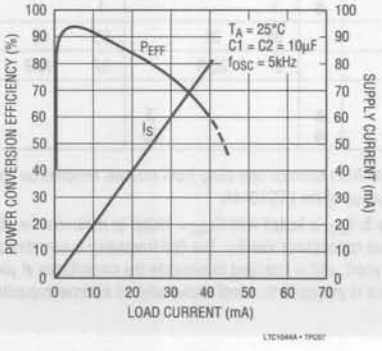
Output Resistance vs Oscillator Frequency, V⁺ = 10V



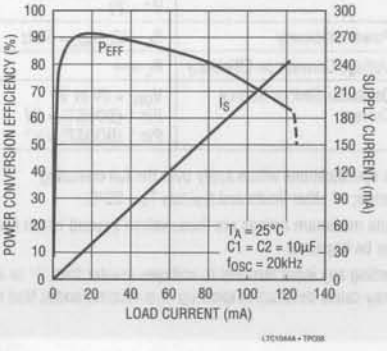
Power Conversion Efficiency vs Load Current, V⁺ = 2V



Power Conversion Efficiency vs Load Current, V⁺ = 5V

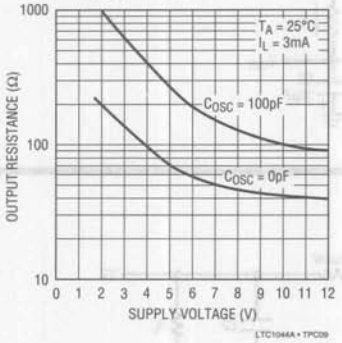


Power Conversion Efficiency vs Load Current, V⁺ = 10V

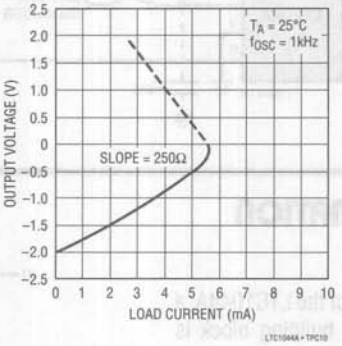


TYPICAL PERFORMANCE CHARACTERISTICS Using the Test Circuit

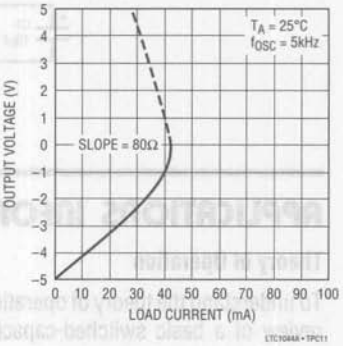
Output Resistance vs Supply Voltage



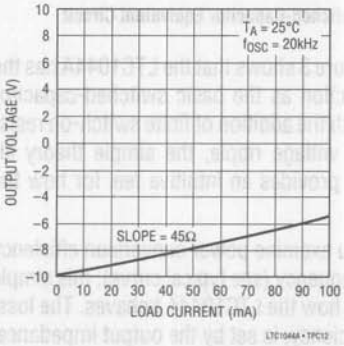
Output Voltage vs Load Current, V⁺ = 2V



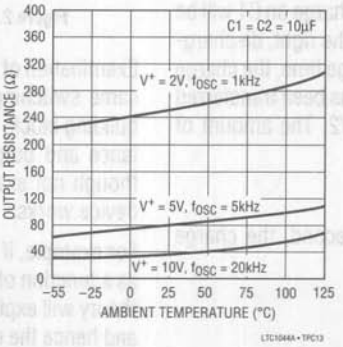
Output Voltage vs Load Current, V⁺ = 5V



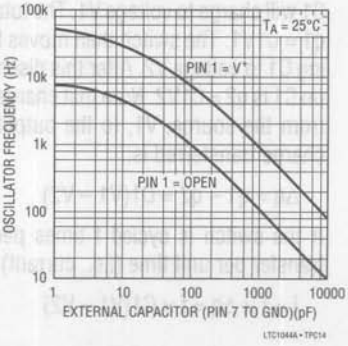
Output Voltage vs Load Current, V⁺ = 10V



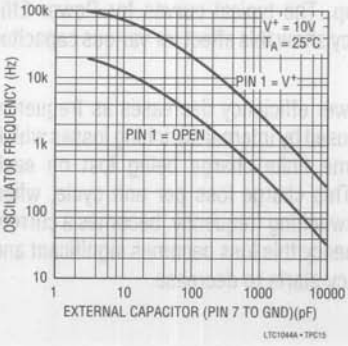
Output Resistance vs Temperature



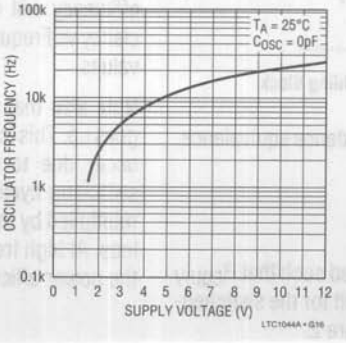
Oscillator Frequency as a Function of C_{OSC}, V⁺ = 5V



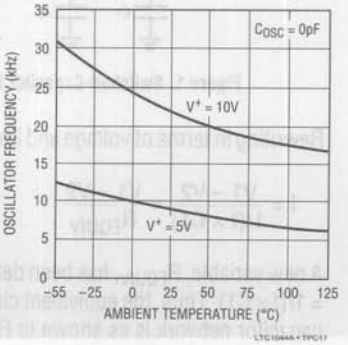
Oscillator Frequency as a Function of C_{OSC}, V⁺ = 10V



Oscillator Frequency vs Supply Voltage

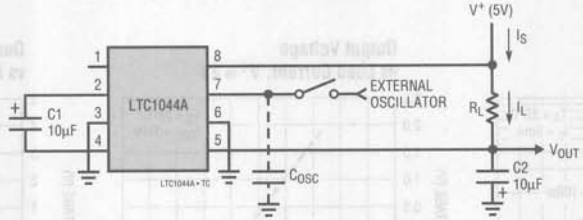


Oscillator Frequency vs Temperature



4

TEST CIRCUIT



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044A, a review of a basic switched-capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2)$$

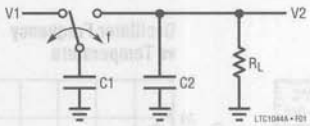


Figure 1. Switched-Capacitor Building Block

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{1/(f \times C1)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/(f \times C1)$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 2.

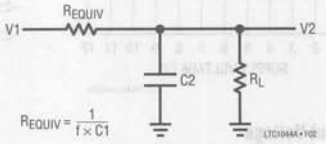


Figure 2. Switched-Capacitor Equivalent Circuit

Examination of Figure 3 shows that the LTC1044A has the same switching action as the basic switched-capacitor building block. With the addition of finite switch-on resistance and output voltage ripple, the simple theory although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044A behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the $1/(f \times C1)$ term, and power efficiency will drop. The typical curves for Power Efficiency vs Frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

APPLICATIONS INFORMATION

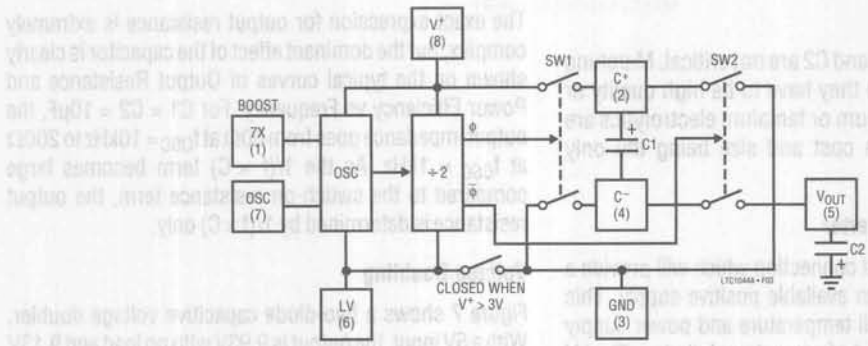


Figure 3. LTC1044A Switched-Capacitor Voltage Converter Block Diagram

LV (Pin 6)

The internal logic of the LTC1044A runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V^+ less than 3V, the LV pin should be tied to GND. For V^+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered, or driven from an external source. Figure 4 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased and hence, the frequency is increased by approximately 7 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044A from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open as shown in Figure 5. The output current from pin 7 is small (typically 0.5μA) so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 4. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 5).

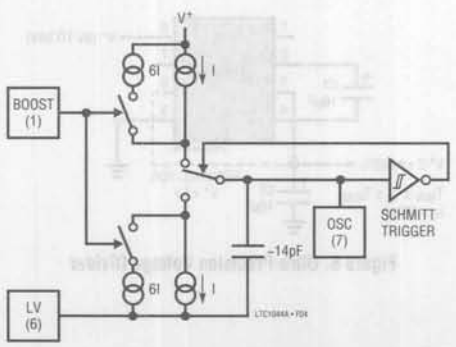


Figure 4. Oscillator

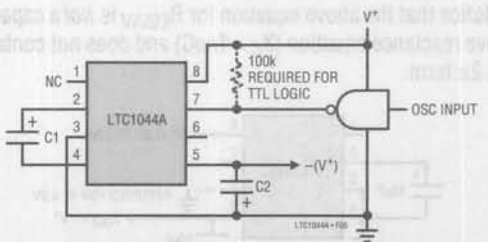


Figure 5. External Clocking

APPLICATIONS INFORMATION

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices with cost and size being the only consideration.

Negative Voltage Converter

Figure 6 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be "floated", since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms:

1. The equivalent switched-capacitor resistance (see Theory of Operation).
2. A term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and C1 = 10μF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \times C1}$$

$$= \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\Omega$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

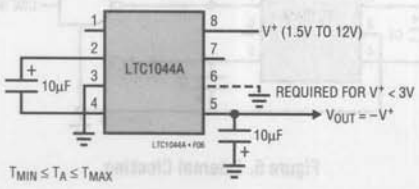


Figure 6. Negative Voltage Converter

The exact expression for output resistance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of Output Resistance and Power Efficiency vs Frequency. For C1 = C2 = 10μF, the output impedance goes from 60Ω at f_{OSC} = 10kHz to 200Ω at f_{OSC} = 1kHz. As the $1/(f \times C)$ term becomes large compared to the switch-on resistance term, the output resistance is determined by $1/(f \times C)$ only.

Voltage Doubling

Figure 7 shows a two-diode capacitive voltage doubler. With a 5V input, the output is 9.93V with no load and 9.13V with a 10mA load. With a 10V input, the output is 19.93V with no load and 19.28V with a 10mA load.

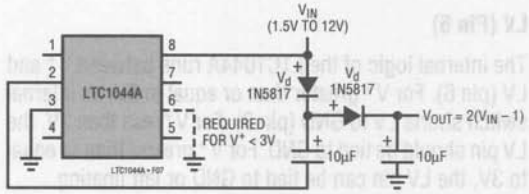


Figure 7. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 8. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy the load current can be increased.

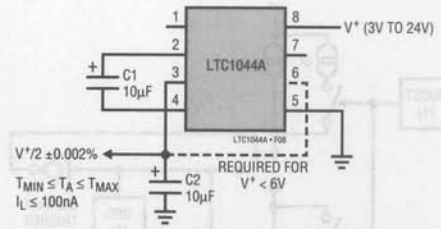


Figure 8. Ultra-Precision Voltage Divider

APPLICATIONS INFORMATION

Battery Splitter

A common need in many systems is to obtain (+) and (–) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 9 is a simple solution. It provides symmetrical ± output voltages, both equal to one half input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3 as shown by the dashed line.

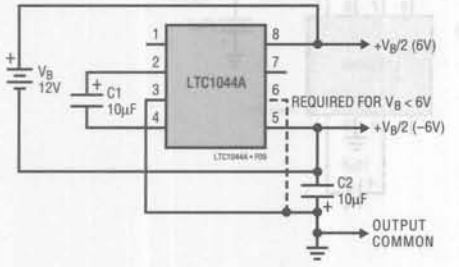


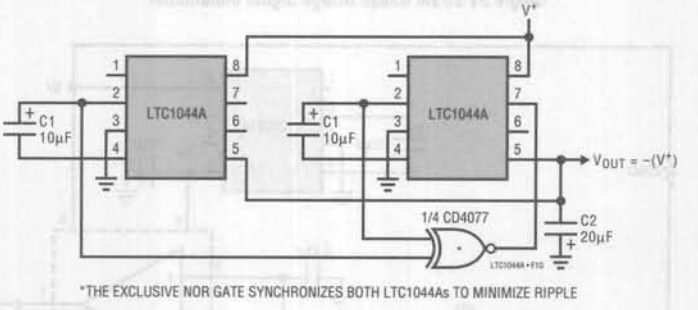
Figure 9. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044A is shown in Figures 10 and 11.

Figure 10 shows two LTC1044As connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by $1/(f \times C1)$, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figure 11 makes use of "stacking" two LTC1044As to provide even higher voltages. A negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044A is connected, as shown schematically by the switch. The available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.



*THE EXCLUSIVE NOR GATE SYNCHRONIZES BOTH LTC1044As TO MINIMIZE RIPPLE

Figure 10. Paralleling for Lower Output Resistance

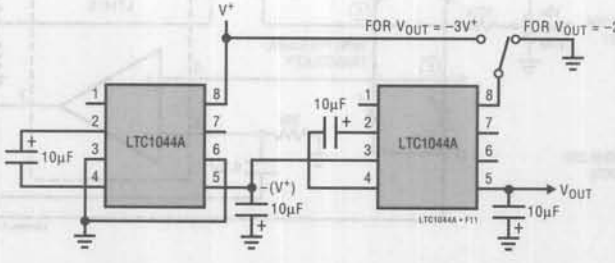
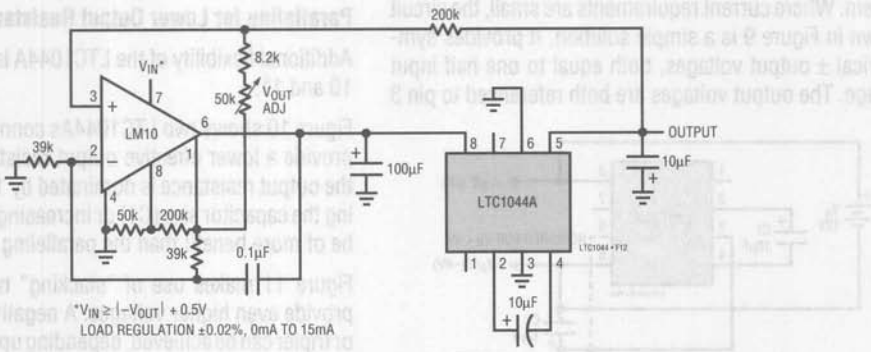


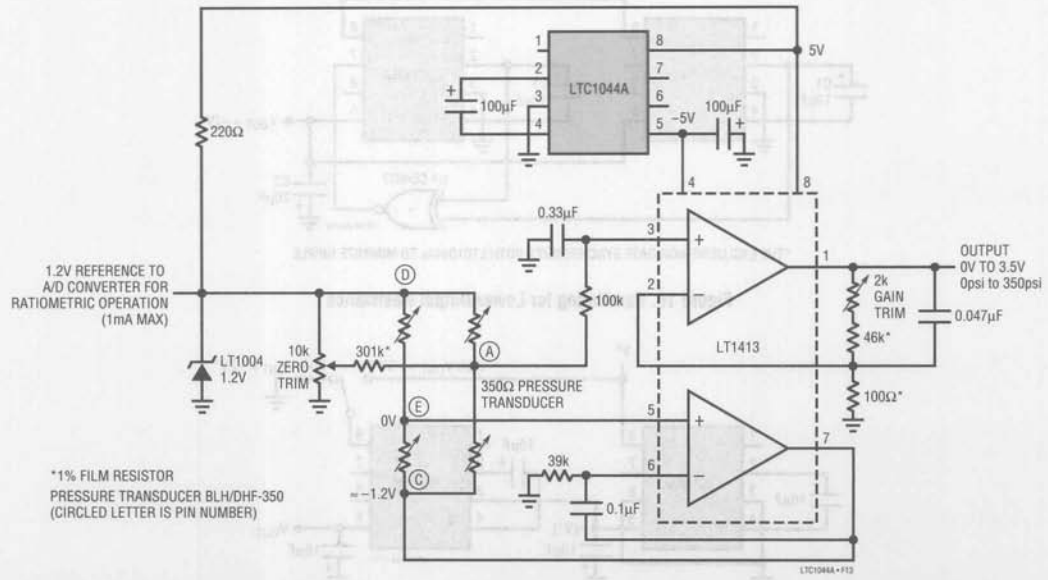
Figure 11. Stacking for Higher Voltage

TYPICAL APPLICATIONS

Low Output Impedance Voltage Converter

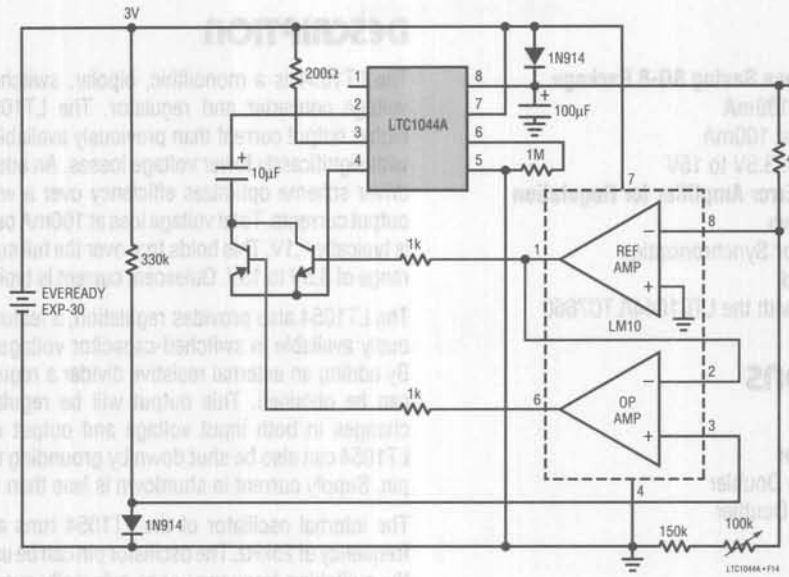


Single 5V Strain Gauge Bridge Signal Conditioner

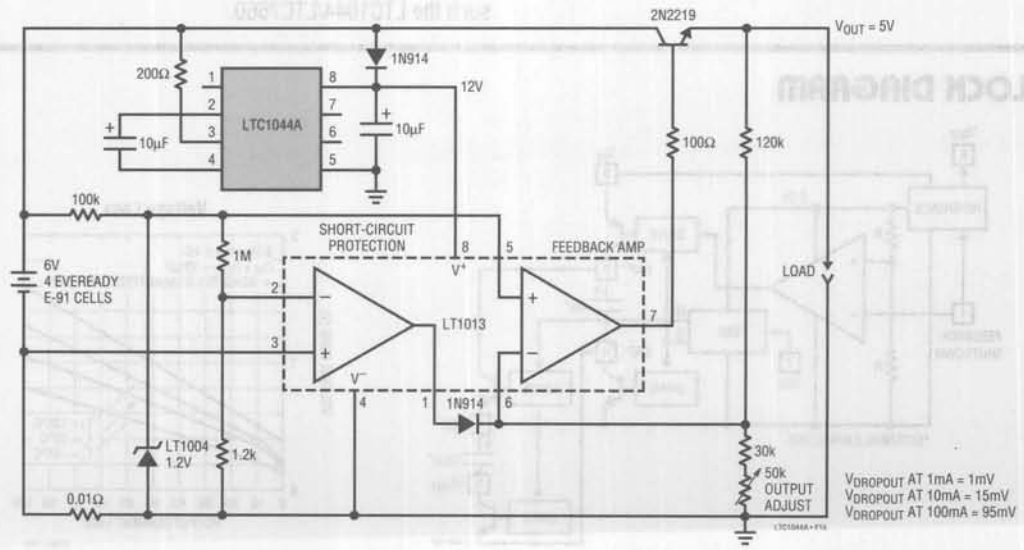


TYPICAL APPLICATIONS

Regulated Output 3V to 5V Converter



Low Dropout 5V Regulator



4

Switched-Capacitor Voltage Converter with Regulator

FEATURES

- **Available in Space Saving SO-8 Package**
- **Output Current: 100mA**
- Low Loss: 1.1V at 100mA
- Operating Range: 3.5V to 15V
- **Reference and Error Amplifier for Regulation**
- External Shutdown
- External Oscillator Synchronization
- Can Be Paralleled
- Pin Compatible with the LTC1044/LTC7660

APPLICATIONS

- Voltage Inverter
- Voltage Regulator
- Negative Voltage Doubler
- Positive Voltage Doubler

DESCRIPTION

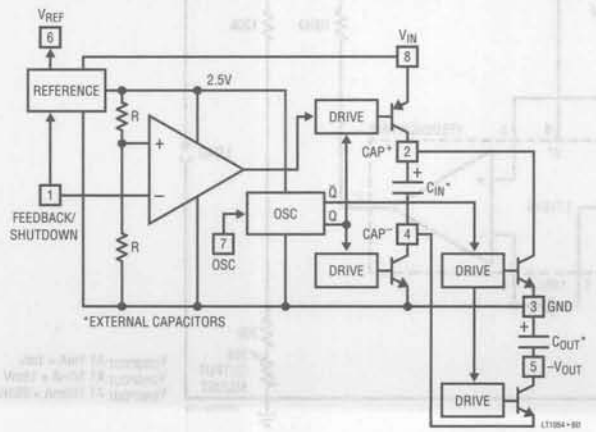
The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch driver scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

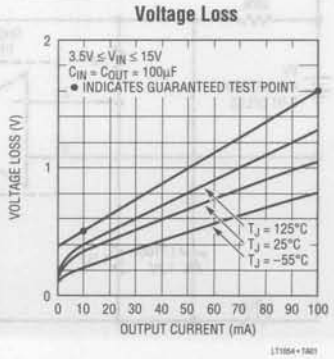
The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than 100μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such the LTC1044/LTC7660.

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 16V

Input Voltage

- Pin 1 ..... $0V \le V_{PIN1} \le V^+$
- Pin 3 (S Package) ..... $0V \le V_{PIN3} \le V^+$
- Pin 7 ..... $0V \le V_{PIN7} \le V_{REF}$
- Pin 13 (S Package) ..... $0V \le V_{PIN13} \le V_{REF}$

Operating Temperature Range

- LT1054C ..... 0°C to 70°C
- LT1054I ..... –40°C to 85°C
- LT1054M ..... –55°C to 125°C

Junction Temperature Range (Note 2)

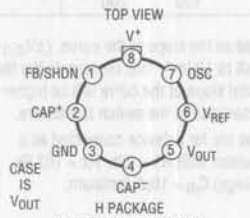
- LT1054C ..... 125°C
- LT1054I ..... 125°C
- LT1054M ..... 150°C

Storage Temperature Range

- H, J8, N8 and S8 Packages ..... –55°C to 150°C
- S Package ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

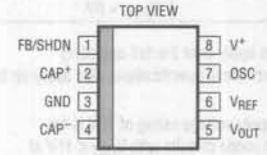
PACKAGE/ORDER INFORMATION (Note 6)



H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 150°C, θ_{JA} = 150°C, θ_{JC} = 45°C/W

ORDER PART NUMBER
LT1054CH
LT1054MH



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = XXX°C, θ_{JA} = XXX°C/W

SEE REGULATION AND CAPACITOR SELECTION SECTIONS IN THE APPLICATIONS INFORMATION FOR IMPORTANT INFORMATION ON THE S8 DEVICE

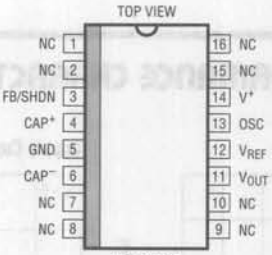
ORDER PART NUMBER
LT1054CS8
S8 PART MARKING
1054

J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LT1054CJ8
LT1054CN8
LT1054IN8
LT1054MJ8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1054CS
LT1054IS

4

ELECTRICAL CHARACTERISTICS (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{LOAD} = 0mA					
	V_{IN} = 3.5V	●		2.5	4.0	mA
	V_{IN} = 15V	●		3.0	5.0	mA
Supply Voltage Range		●	3.5		15	V
Voltage Loss ($V_{IN} - \|V_{OUT}\|$)	$C_{IN} = C_{OUT}$ = 100µF Tantalum (Note 3)					
	I_{OUT} = 10mA	●		0.35	0.55	V
	I_{OUT} = 100mA	●		1.10	1.60	V
Output Resistance	ΔI_{OUT} = 10mA to 100mA (Note 4)	●		10	15	Ω
Oscillator Frequency	3.5V ≤ V_{IN} ≤ 15V	●	15	25	35	kHz
Reference Voltage	I_{REF} = 60µA, T_J = 25°C		2.35	2.50	2.65	V
		●	2.25		2.75	V
Regulated Voltage	V_{IN} = 7V, T_J = 25°C, R_L = 500Ω (Note 5)		−4.70	−5.00	−5.20	V
Line Regulation	7V ≤ V_{IN} ≤ 12V, R_L = 500Ω (Note 5)	●		5	25	mV
Load Regulation	V_{IN} = 7V, 100Ω ≤ R_L ≤ 500Ω (Note 5)	●		10	50	mV
Maximum Switch Current				300		mA
Supply Current in Shutdown	V_{PIN1} = 0V	●		100	200	µA

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with V_{OUT} ≤ 15V at pin 5, (pin 11 S package) this rating may be increased to 20V.

Note 2: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

Note 3: For voltage loss tests, the device is connected as a voltage inverter, with pins 1, 6, and 7 (3, 12, and 13 S package) unconnected. The voltage losses may be higher in other configurations.

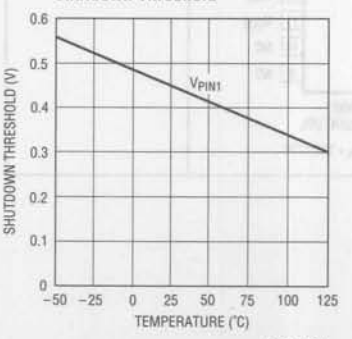
Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10mA to 100mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents <10mA due to the characteristics of the switch transistors.

Note 5: All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20k, R2 = 102.5k, C1 = 0.002µF, (C1 = 0.05µF S package) C_{IN} = 10µF tantalum, C_{OUT} = 100µF tantalum.

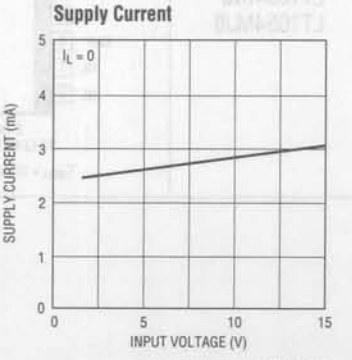
Note 6: The S8 package uses a different die than the H, J8, N8 and S packages. The S8 device will meet all the existing data sheet parameters. See Regulation and Capacitor Selection sections in Applications Information for differences in application requirements.

TYPICAL PERFORMANCE CHARACTERISTICS

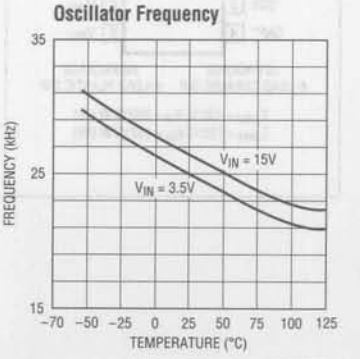
Shutdown Threshold



Supply Current

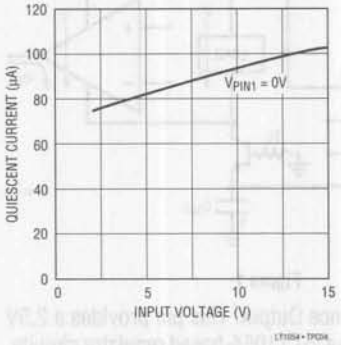


Oscillator Frequency



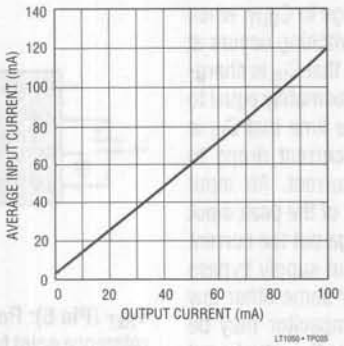
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current in Shutdown



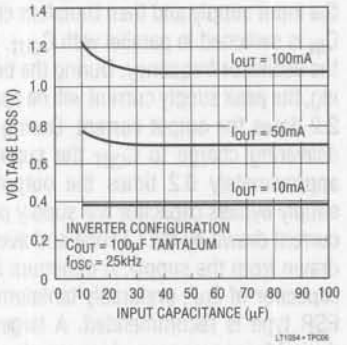
LT1054 • TPC04

Average Input Current



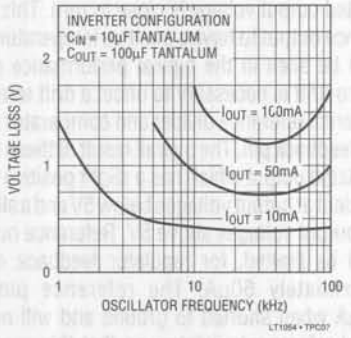
LT1050 • TPC05

Output Voltage Loss



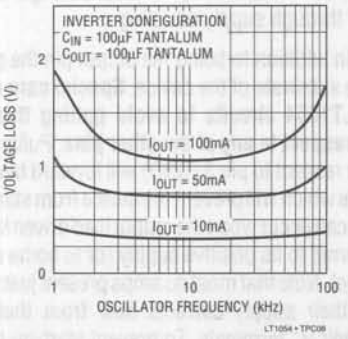
LT1054 • TPC06

Output Voltage Loss



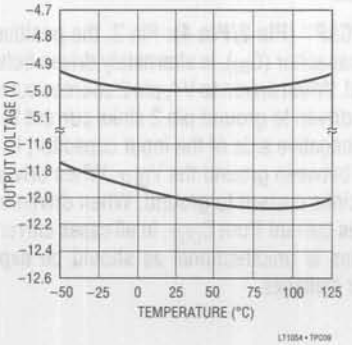
LT1054 • TPC07

Output Voltage Loss



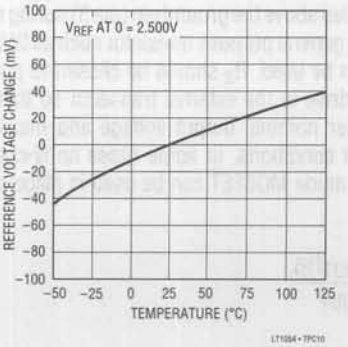
LT1054 • TPC08

Regulated Output Voltage



LT1054 • TPC09

Reference Voltage Temperature Coefficient



LT1054 • TPC10

4

PIN FUNCTIONS

V^+ (Pin 8): Input Supply. The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054 and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2µF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example, when the actual input supply is connected to the LT1054 through long leads, or when the pulse current drawn by the LT1054 might affect other circuitry through supply coupling.

V_{OUT} (Pin 5): In addition to being the output pin the pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins.** Pulling pin 5 positive with respect to pin 3 (GND) will forward bias the substrate diode which will prevent the device from starting. This condition can occur when the output load driven by the LT1054 is referred to its positive supply (or to some other positive voltage). Note that most op amps present just such a load since their supply currents flow from their V^+ terminals to their V^- terminals. To prevent start-up problems with this type of load an external transistor must be added as shown in Figure 1. This will prevent V_{OUT} (pin 5) from being pulled above the ground pin (pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. R_X should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions. In some cases an N-channel enhancement mode MOSFET can be used in place of the transistor.

$$R_X \leq \frac{(|V_{OUT}|)\beta}{I_{OUT}}$$

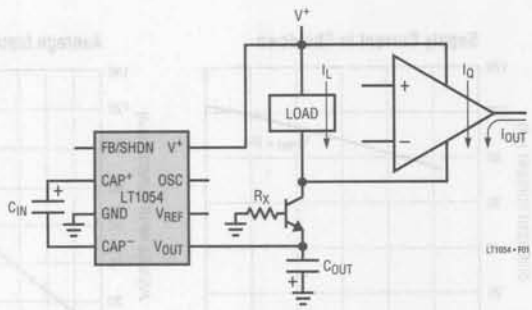


Figure 1

V_{REF} (Pin 6): Reference Output. This pin provides a 2.5V reference point for use in LT1054-based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60µA. The reference pin will draw ≈100µA when shorted to ground and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

CAP^+/CAP^- (Pin 2/Pin 4): Pin 2, the positive side of the input capacitor (C_{IN}), is alternately driven between V^+ and ground. When driven to V^+, pin 2 sources current from V^+. When driven to ground pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor, is driven alternately between ground the V_{OUT}. When driven to ground, pin 4 sinks current to ground. When driven to V_{OUT} pin 4 sources current from C_{OUT}. In all cases current flow in the switches is unidirectional as should be expected using bipolar switches.

PIN FUNCTIONS

OSC (Pin 7): Oscillator Pin. This pin can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally pin 7 is connected to the oscillator timing capacitor ($C_t \approx 150pF$) which is alternately charged and discharged by current sources of $\pm 7\mu A$ so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be lowered by adding an external capacitor (C1, Figure 2) from pin 7 to ground. This will increase the charge and discharge times which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2, Figure 2, in the range of 5pF to 20pF) from pin 2 to pin 7. This capacitor will couple charge into C_t at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from pin 7 to the reference pin (pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 2. Pulling up pin 7 to an external voltage is **not recommended**. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R1/R2 divider allowing pin 6 to be used as a pull-up point for pin 7.

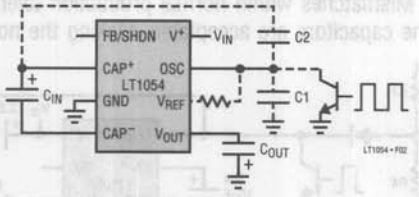


Figure 2

FB/SHDN (Pin 1): Feedback/Shutdown Pin. This pin has two functions. Pulling pin 1 below the shutdown threshold (≈0.45V) puts the device into shutdown. In shutdown the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100μA (see Typical Performance Characteristics). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off-time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p > 100\mu s$) or a logic high. Diode coupling the restart signal into pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R3/R4 in Figure 5 should be chosen to provide a signal level at pin 1 of 0.7V to 1.1V.

Pin 1 is also the inverting input of the LT1054's error amplifier and as such can be used to obtain a regulated output voltage.

4

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched-capacitor building block is helpful.

In Figure 3 when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

APPLICATIONS INFORMATION

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

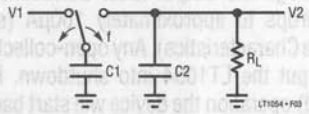


Figure 3. Switched-Capacitor Building Block

A new variable R_{EQUIV} is defined such that $R_{EQUIV} = 1/fC1$. Thus the equivalent circuit for the switched-capacitor network is as shown in Figure 4. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see Typical Performance Characteristics). As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise.

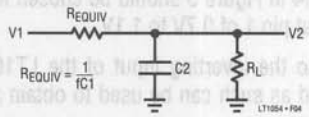


Figure 4. Switched-Capacitor Equivalent Circuit

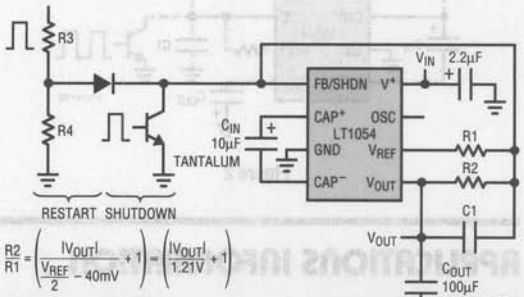
Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

Regulation

The error amplifier of the LT1054 servos the drive to the PNP switch to control the voltage across the input capacitor (C_{IN}) which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be chosen to be 20k or greater because the reference output current is limited to ≈100μA. R2 should be chosen to be in the range of 100k to 300k. For optimum results the ratio of C_{IN}/C_{OUT} is recommended to be 1/10. C1, required for good load regulation at light load currents, should be 0.002μF for all output voltages.

A new die layout was required to fit into the physical dimensions of the S8 package. Although the new die of the LT1054CS8 will meet all the specifications of the existing LT1054 data sheet, subtle differences in the layout of the new die require consideration in some application circuits. In regulating mode circuits using the LT1054CS8 the nominal values of the capacitors, C_{IN} and C_{OUT}, must be approximately equal for proper operation at elevated junction temperatures. This is different from the earlier part. Mismatches within normal production tolerances for the capacitors are acceptable. Making the nominal



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) - \left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

WHERE V_{REF} = 2.5V NOMINAL

FOR EXAMPLE: TO GET V_{OUT} = –5V REFERRED TO THE GROUND PIN OF THE LT1054, CHOOSE R1 = 20k, THEN

$$R2 = 20k\left(\frac{|-5V|}{\frac{2.5V}{2} - 40mV} + 1\right) = 102.6k^*$$

*CHOOSE THE CLOSEST 1% VALUE

Figure 5

APPLICATIONS INFORMATION

capacitor values equal will ensure proper operation at elevated junction temperatures at the cost of a small degradation in the transient response of regulator circuits. For unregulated circuits the values of C_{IN} and C_{OUT} are normally equal for all packages. For S8 applications assistance in unusual applications circuits, please consult the factory.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in Typical Performance Characteristics. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see Typical Applications).

Capacitor Selection

For unregulated circuits the nominal values of C_{IN} and C_{OUT} should be equal. For regulated circuits see the section on Regulation. While the exact values of C_{IN} and C_{OUT} are noncritical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four due to the fact that switch currents are approximately two times higher than output current and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output impedance of the LT1054 by 4Ω. This represents a significant increase in the voltage losses. For C_{OUT} the affect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current and the ESR of the capacitor will cause a step function to occur in the output ripple at the switch transitions. This step function will degrade the output regulation for changes in output load current and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost. Where physical size is a concern some of the newer chip type surface mount tantalum capacitors can be used. These capacitors are normally rated at working voltages in the 10V to 20V range and exhibit very low ESR (in the range of 0.1Ω).

Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

where dV = peak-to-peak ripple and f = oscillator frequency.

For output capacitors with significant ESR a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$(2I_{OUT})$(ESR of C_{OUT})

Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})(0.2)$$

where both V_{IN} and V_{OUT} are referred to the ground pin (pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials. This can be accomplished by placing a resistor in series with C_{IN} as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor without affecting the output regulation. Because switch current is approximately 2.2 times the output current and the resistor will cause a voltage drop when C_{IN} is both charging and discharging, the resistor should be chosen as:

$R_X = V_X/(4.4\ I_{OUT})$

4

APPLICATIONS INFORMATION

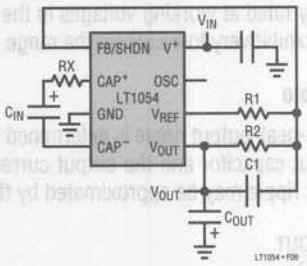


Figure 6

where

$V_X \approx V_{IN} - [(LT1054\ Voltage\ Loss)(1.3) + |V_{OUT}|]$

and I_{OUT} = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a 12V to −5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$P = (12V - |-5V|)(100mA) + (12V)(100mA)(0.2)$
$P = 700mW + 240mW = 940mW$

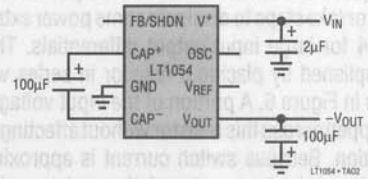
At θ_{JA} of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external resistor (R_X). First find how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

$V_X = 12V - [(1.6V)(1.3) + |-5V|] = 4.9V$ and
$R_X = 4.9V/(4.4)(100mA) = 11\Omega$

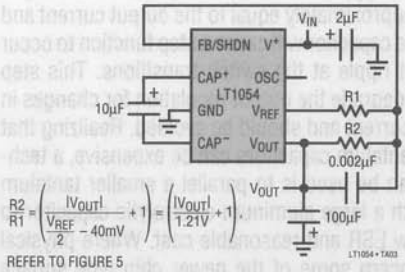
This resistor will reduce the power dissipated by the LT1054 by (4.9V)(100mA) = 490mW. The total power dissipated by the LT1054 would then be = (940mW − 490mW) = 450mW. The junction temperature rise would now be only 58°C. Although commercial devices are guaranteed to be functional up to a junction temperature of 125°C, the specifications are only guaranteed up to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst case numbers with no heat sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

TYPICAL APPLICATIONS

Basic Voltage Inverter



Basic Voltage Inverter/Regulator

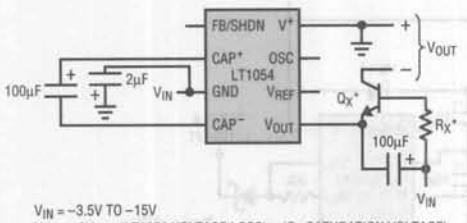


$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right).$$

REFER TO FIGURE 5

TYPICAL APPLICATIONS

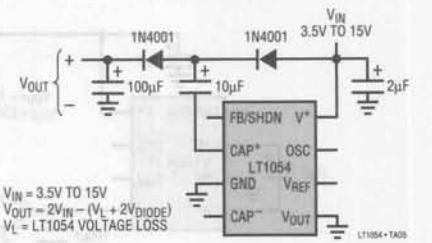
Negative Voltage Doubler



V_{IN} = −3.5V TO −15V
$V_{OUT} = 2V_{IN}$ + (LT1054 VOLTAGE LOSS) + (Q_X SATURATION VOLTAGE)
*SEE FIGURE 3

LT1054 • TA04

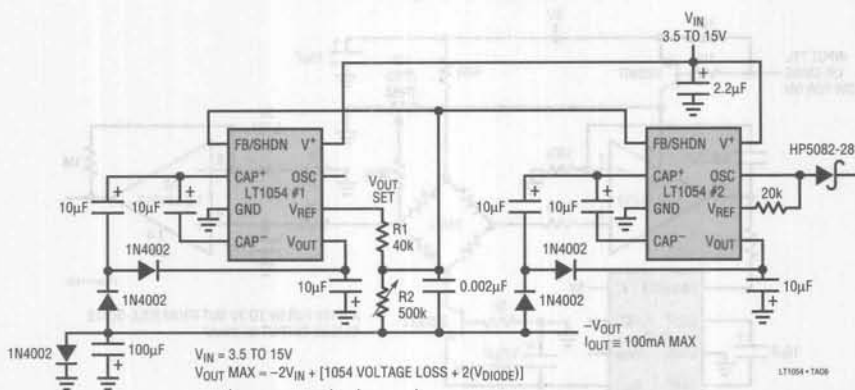
Positive Doubler



V_{IN} = 3.5V TO 15V
$V_{OUT} = 2V_{IN} - (V_L + 2V_{DIODE})$
V_L = LT1054 VOLTAGE LOSS

LT1054 • TA05

100mA Regulating Negative Doubler

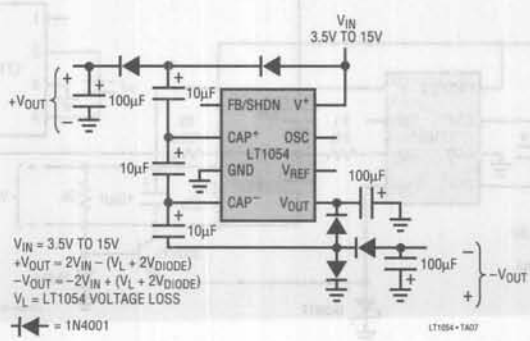


V_{IN} = 3.5 TO 15V
V_{OUT} MAX = $-2V_{IN}$ + [1054 VOLTAGE LOSS + 2(V_{DIODE})]

$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$, REFER TO FIGURE 5

LT1054 • TA06

Dual Output Voltage Doubler

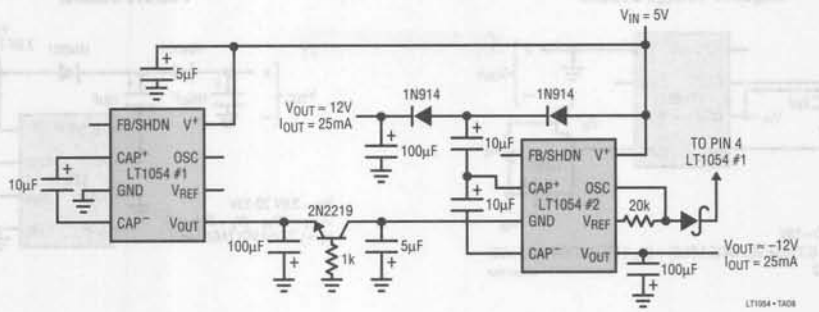


V_{IN} = 3.5V TO 15V
$+V_{OUT} = 2V_{IN} - (V_L + 2V_{DIODE})$
$-V_{OUT} = -2V_{IN} + (V_L + 2V_{DIODE})$
V_L = LT1054 VOLTAGE LOSS
= 1N4001

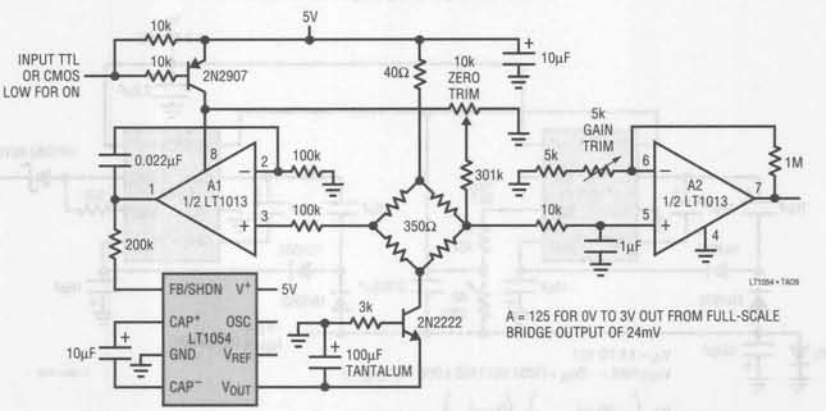
LT1054 • TA07

TYPICAL APPLICATIONS

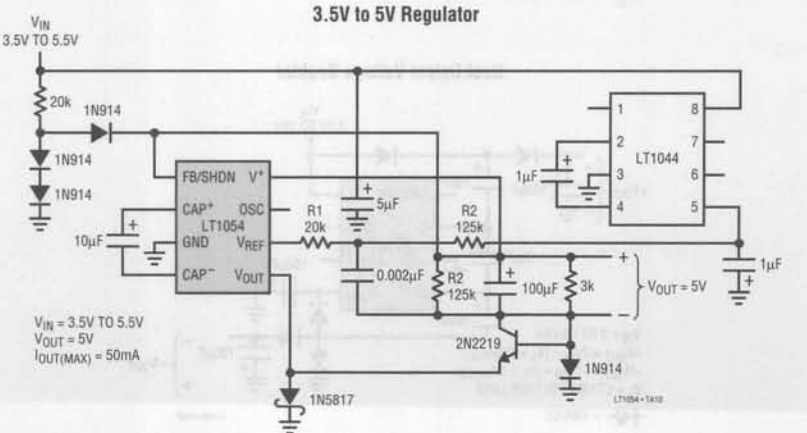
5V to ±12V Converter



Strain Gage Bridge Signal Conditioner

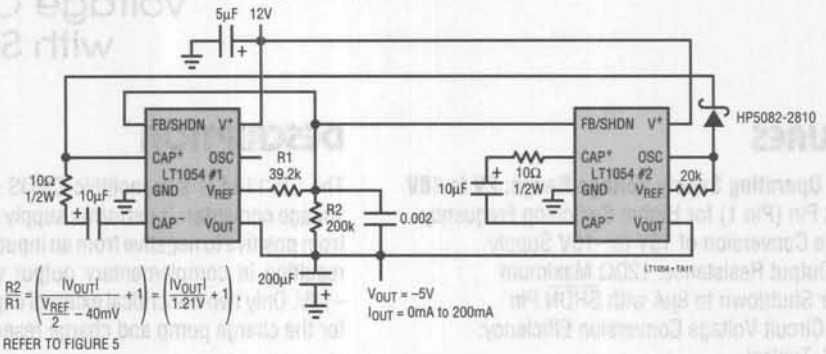


3.5V to 5V Regulator



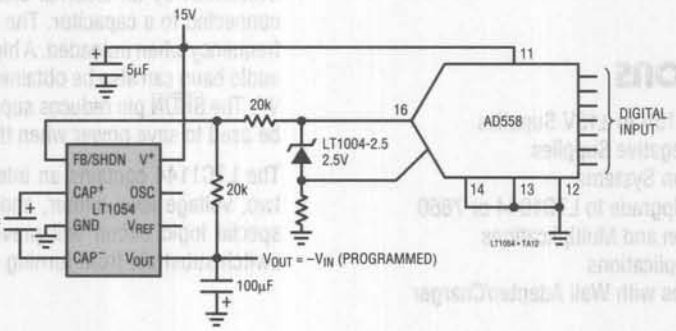
TYPICAL APPLICATIONS

Regulating 200mA, 12V to –5V Converter

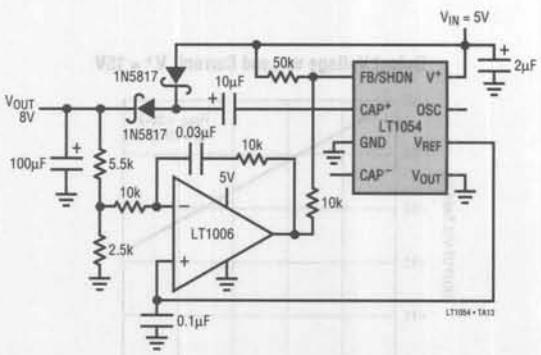


$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

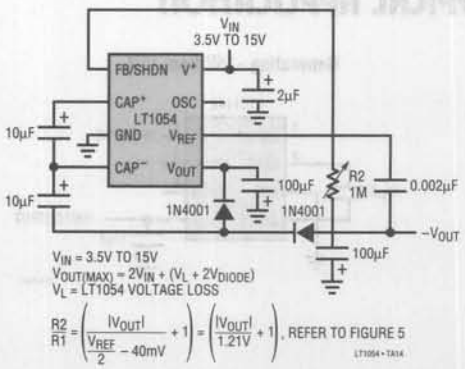
Digitally Programmable Negative Supply



Positive Doubler with Regulation (5V to 8V Converter)



Negative Doubler with Regulator



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right), \text{ REFER TO FIGURE 5}$$

THE TYPICAL APPLICATIONS CIRCUITS WERE VERIFIED USING THE STANDARD LT1054. FOR S8 APPLICATIONS ASSISTANCE IN ANY OF THE UNUSUAL APPLICATIONS CIRCUITS PLEASE CONSULT THE FACTORY.

Switched-Capacitor Wide Input Range Voltage Converter with Shutdown

FEATURES

- **Wide Operating Supply Voltage Range: 2V to 18V**
- Boost Pin (Pin 1) for Higher Switching Frequency
- Simple Conversion of 15V to –15V Supply
- Low Output Resistance: 120Ω Maximum
- Power Shutdown to 8μA with $\overline{SHDN}$ Pin
- Open Circuit Voltage Conversion Efficiency: 99.9% Typical
- Power Conversion Efficiency: 93% Typical
- Easy to Use

APPLICATIONS

- Conversion of 15V to ±15V Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- High Voltage Upgrade to LTC1044 or 7660
- Voltage Division and Multiplications
- Automotive Applications
- Battery Systems with Wall Adapter/Charger

DESCRIPTION

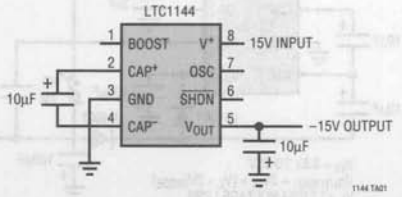
The LTC1144 is a monolithic CMOS switched-capacitor voltage converter. It performs supply voltage conversion from positive to negative from an input range of 2V to 18V, resulting in complementary output voltages of –2V to –18V. Only two noncritical external capacitors are needed for the charge pump and charge reservoir functions.

The converter has an internal oscillator that can be overdriven by an external clock or slowed down when connected to a capacitor. The oscillator runs at a 10kHz frequency when unloaded. A higher frequency outside the audio band can also be obtained if the Boost Pin is tied to V^+. The $\overline{SHDN}$ pin reduces supply current to 8μA and can be used to save power when the converter is not in use.

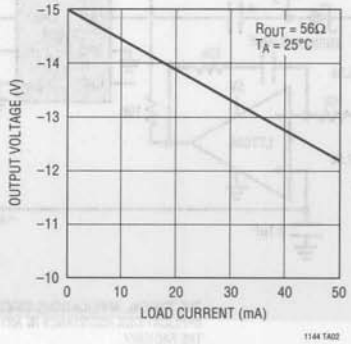
The LTC1144 contains an internal oscillator, divide-by-two, voltage level shifter, and four power MOSFETs. A special logic circuit will prevent the power N-channel switch substrate from turning on.

TYPICAL APPLICATION

Generating –15V from 15V



Output Voltage vs Load Current, V^+ = 15V

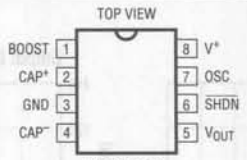


ABSOLUTE MAXIMUM RATINGS

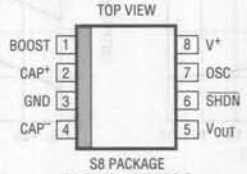
(Note 1)

Supply Voltage (V^+) (Transient) 20V
Supply Voltage (V^+) (Operating) 18V
Input Voltage on Pins 1, 6, 7
(Note 2) ..... $-0.3V < V_{IN} < (V^+) + 0.3V$
Output Short-Circuit Duration
$V^+ \leq 10V$ ..... Indefinite
$V^+ \leq 15V$ ..... 30 sec
$V^+ \leq 20V$ ..... Not Protected
Power Dissipation 500mW
Operating Temperature Range
LTC1144C ..... 0°C to 70°C
LTC1144I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1144CN8 LTC1144IN8
LTC1144CS8 LTC1144IS8
S8 PART MARKING
1144 1144I

Consult factory for Military grade parts.

4

ELECTRICAL CHARACTERISTICS

V^+ = 15V, C_{OSC} = 0pF, T_A = 25°C, Test Circuit Figure 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1144C MIN	LTC1144C TYP	LTC1144C MAX	LTC1144I MIN	LTC1144I TYP	LTC1144I MAX	UNITS
	Supply Voltage Range	R_L = 10k	●	2		18	2		18	V
I_S	Supply Current	$R_L = \infty$, Pins 1, 6 No Connection, f_{OSC} = 10kHz	 ●			1.1 1.3			1.1 1.6	mA mA
		$\overline{SHDN}$ = 0V, $R_L = \infty$, Pins 1, 7 No Connection	●		0.008	0.03		0.008	0.035	mA
		V^+ = 5V, $R_L = \infty$, Pins 1, 6 No Connection, f_{OSC} = 4kHz	 ●			0.10 0.13			0.10 0.15	mA mA
		V^+ = 5V, $\overline{SHDN}$ = 0V, $R_L = \infty$, Pins 1, 7 No Connection	●		0.002	0.015		0.002	0.018	mA
R_{OUT}	Output Resistance	V^+ = 15V, I_L = 20mA at 10kHz	 ●		56	100 120		56	100 140	Ω Ω
		V^+ = 5V, I_L = 3mA at 4kHz	●		90	250		90	300	Ω
f_{OSC}	Oscillator Frequency	V^+ = 15V (Note 3) V^+ = 5V			10 4			10 4		kHz kHz
	Power Efficiency	R_L = 2k at 10kHz	●	90	93		90	93		%
	Voltage Conversion Efficiency	$R_L = \infty$	●	97.0	99.9		97.0	99.9		%
	Oscillator Sink or Source Current	V^+ = 5V (V_{OSC} = 0V to 5V) V^+ = 15V (V_{OSC} = 0V to 15V)			0.5 4			0.5 4		µA µA

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals at T_A = 25°C.

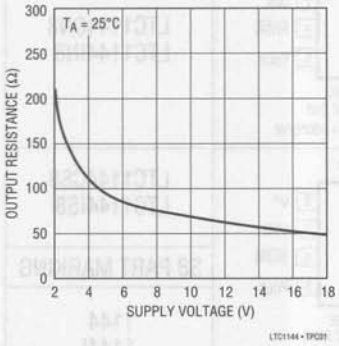
Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1144.

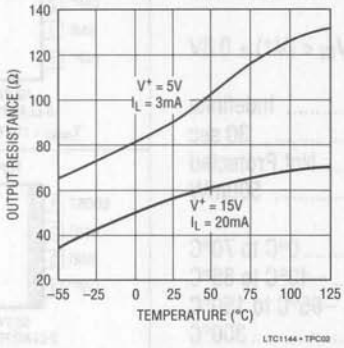
Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS

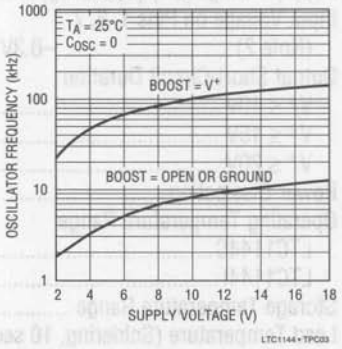
Output Resistance vs Supply Voltage



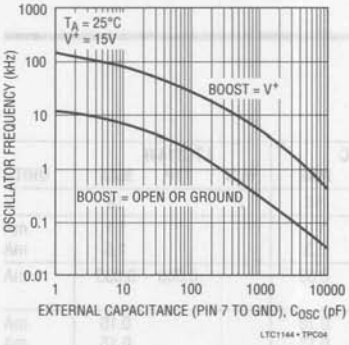
Output Resistance vs Temperature



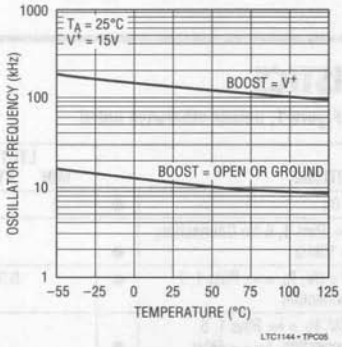
Oscillator Frequency vs Supply Voltage



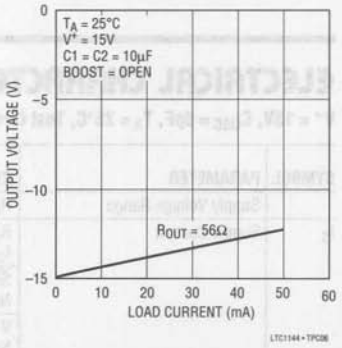
Oscillator Frequency as a Function of C_{OSC}



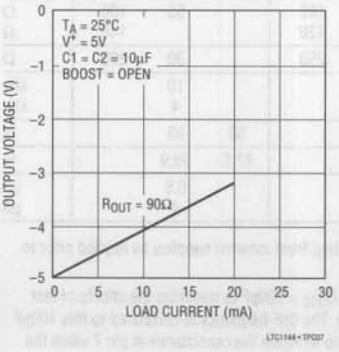
Oscillator Frequency vs Temperature



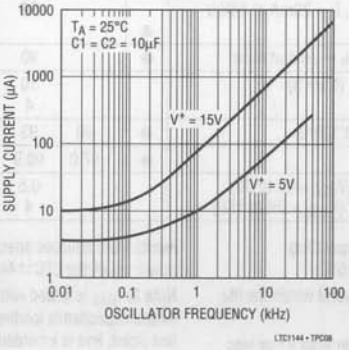
Output Voltage vs Load Current



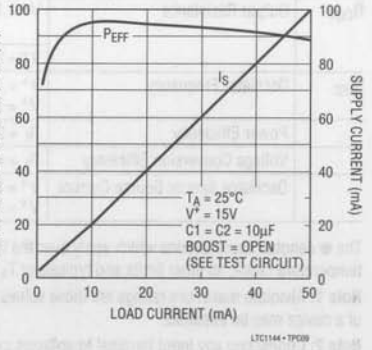
Output Voltage vs Load Current



Supply Current as a Function of Oscillator Frequency

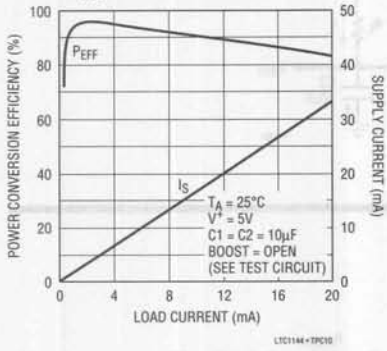


Power Conversion Efficiency and Supply Current vs Load Current

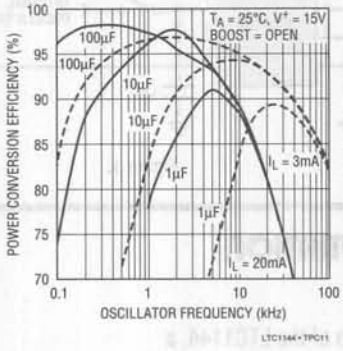


TYPICAL PERFORMANCE CHARACTERISTICS

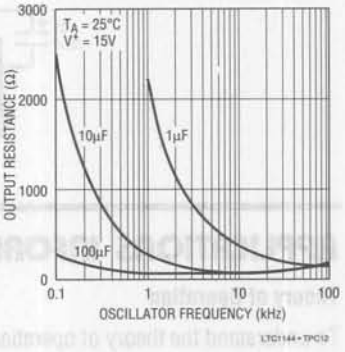
Power Conversion Efficiency and Supply Current vs Load Current



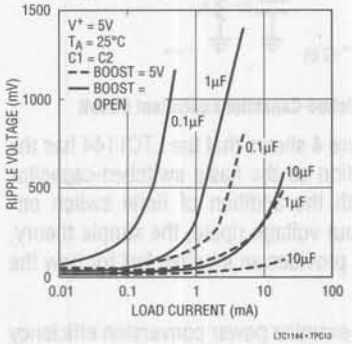
Power Conversion Efficiency vs Oscillator Frequency



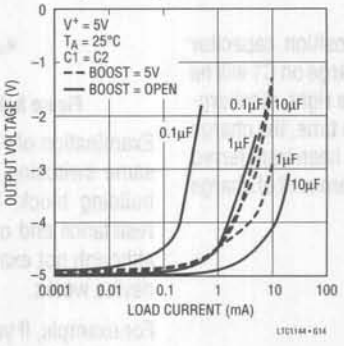
Output Resistance vs Oscillator Frequency



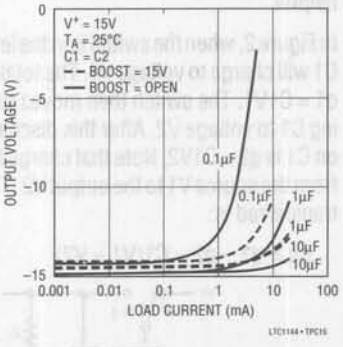
Ripple Voltage vs Load Current



Output Voltage vs Load Current



Output Voltage vs Load Current



PIN FUNCTIONS

Boost (Pin 1): This pin will raise the oscillator frequency by a factor of 10 if tied high.

CAP+ (Pin 2): Positive Terminal for Pump Capacitor.

GND (Pin 3): Ground Reference.

CAP– (Pin 4): Negative Terminal for Pump Capacitor.

V_{OUT} (Pin 5): Output of the Converter.

$\overline{SHDN}$ (Pin 6): Shutdown Pin. Tie to V+ pin or leave floating for normal operation. Tie to ground when in shutdown mode.

OSC (Pin 7): Oscillator Input Pin. This pin can be overdriven with an external clock or can be slowed down by connecting an external capacitor between this pin and ground.

V+ (Pin 8): Input Voltage.

TEST CIRCUIT

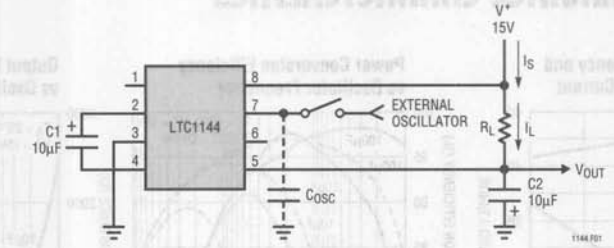


Figure 1.

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1144, a review of a basic switched-capacitor building block is helpful.

In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

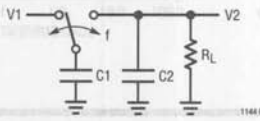


Figure 2. Switched-Capacitor Building Block

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2)$$

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{\left(\frac{1}{f \times C1}\right)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable R_{EQUIV} has been defined such that $R_{EQUIV} = 1/(f \times C1)$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 3.

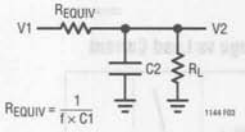


Figure 3. Switched-Capacitor Equivalent Circuit

Examination of Figure 4 shows that the LTC1144 has the same switching action as the basic switched-capacitor building block. With the addition of finite switch on-resistance and output voltage ripple, the simple theory, although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see Figure 5), this simple theory will explain how the LTC1144 behaves. The loss,

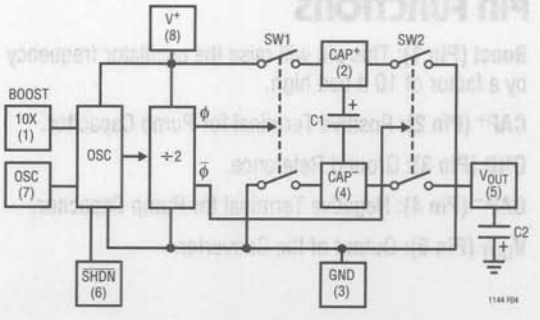


Figure 4. LTC1144 Switched-Capacitor Voltage Converter Block Diagram

APPLICATIONS INFORMATION

and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the $1/(f \times C1)$ term and power efficiency will drop.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

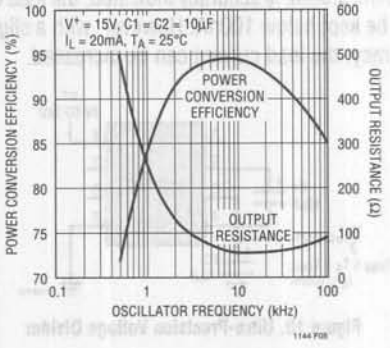


Figure 5. Power Conversion Efficiency and Output Resistance vs Oscillator Frequency

$\overline{SHDN}$ (Pin 6)

The LTC1144 has a $\overline{SHDN}$ pin that will disable the internal oscillator when it is pulled low. The supply current will also drop to 8µA.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 6 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased, and hence the frequency is increased by approximately 10 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

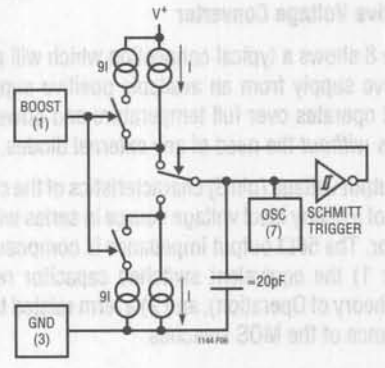


Figure 6. Oscillator

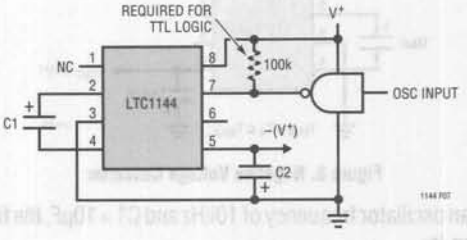


Figure 7. External Clocking

Driving the LTC1144 from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open as shown in Figure 7. The output current from pin 7 is small, typically 4µA, so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 6. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 7).

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 8 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with a 56Ω resistor. The 56Ω output impedance is composed of two terms: 1) the equivalent switched capacitor resistance (see Theory of Operation), and 2) a term related to the on-resistance of the MOS switches.

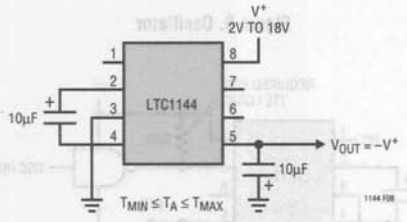


Figure 8. Negative Voltage Converter

At an oscillator frequency of 10kHz and C1 = 10µF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2)\times C1} = \frac{1}{5\times10^{3}\times10\times10^{-6}} = 20\Omega$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is extremely complex, but the dominant effect of the capacitor is clearly shown in Figure 5. For C1 = C2 = 10µF, the output impedance goes from 56Ω at f_{OSC} = 10kHz to 250Ω at f_{OSC} = 1kHz. As the $1/(f\times C)$ term becomes large compared to the switch on-resistance term, the output resistance is determined by $1/(f\times C)$ only.

Voltage Doubling

Figure 9 shows a two-diode capacitive voltage doubler. With a 15V input, the output is 29.45V with no load and 28.18V with a 10mA load.

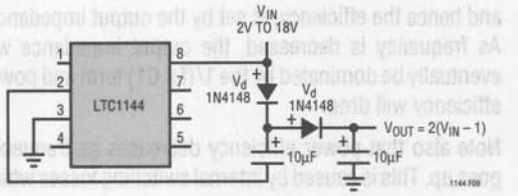


Figure 9. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 10. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

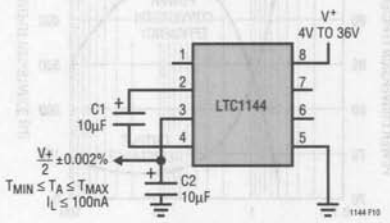


Figure 10. Ultra-Precision Voltage Divider

Battery Splitter

A common need in many systems is to obtain (+) and (–) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 11 is a simple solution. It provides symmetrical ± output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common).

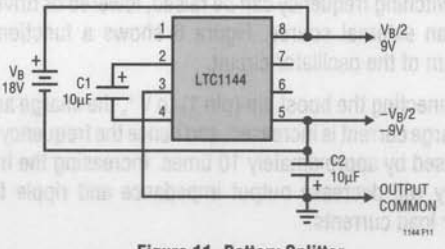


Figure 11. Battery Splitter

TYPICAL APPLICATIONS

Regulated –5V Output Voltage

Figure 12 shows a regulated –5V output with a 9V input. With a 0mA to 5mA load current, the R_{OUT} is below 20Ω.

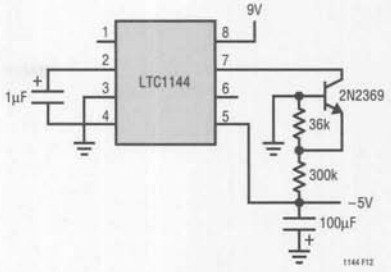


Figure 12. A Regulated –5V Supply

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1144 is shown in Figure 13. Two LTC1144s are connected in parallel to provide a lower effective output resistance. However, if the output resistance is dominated by 1/(f × C1), increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

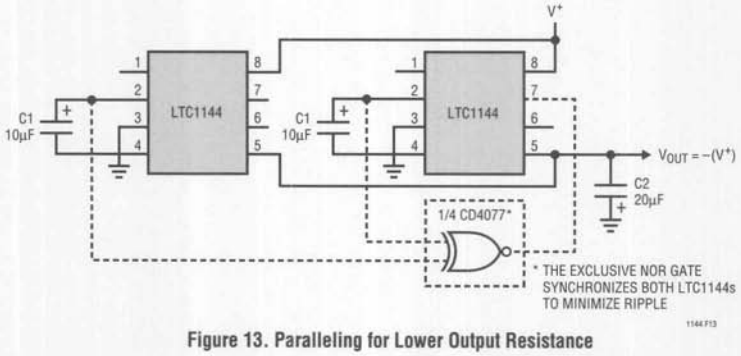


Figure 13. Paralleling for Lower Output Resistance

SECTION 4—POWER PRODUCTS

LINEAR REGULATORS

LT1083/LT1084/LT1085, 7.5A, 5A, 3A Low Dropout Positive Adjustable Regulators 4-48
LT1083/LT1084/LT1085 Fixed, 3A, 5A, 7.5A Low Dropout Positive Fixed Regulators 4-61
LT1086 Series, 1.5A Low Dropout Positive Regulators Adjustable and Fixed 2.85V, 3.3V, 3.6V, 5V, 12V 4-72
LT1117/LT1117-2.85/LT1117-3.3/LT1117-5, 800mA Low Dropout Positive Regulators Adjustable and Fixed 2.85V, 3.3V, 5V 4-85
LT1120, Micropower Regulator with Comparator and Shutdown 4-96
LT1120A, Micropower Regulator with Comparator and Shutdown 4-107
LT1121/LT1121-3.3/LT1121-5, Micropower Low Dropout Regulators with Shutdown 4-114
LT1129/LT1129-3.3/LT1129-5, Micropower Low Dropout Regulators with Shutdown 4-125
LT1585, 4A Low Dropout Fast Response Positive Regulator Adjustable and Fixed 13-136

4

7.5A, 5A, 3A Low Dropout Positive Adjustable Regulators

FEATURES

- Three-Terminal Adjustable
- Output Current of 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- Line Regulation: 0.015%
- Load Regulation: 0.01%
- 100% Thermal Limit Functional Test
- Fixed Versions Available

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DEVICE	OUTPUT CURRENT*
LT1083	7.5A
LT1084	5.0A
LT1085	3.0A

*For a 1.5A low dropout regulator see the LT1086 data sheet.

DESCRIPTION

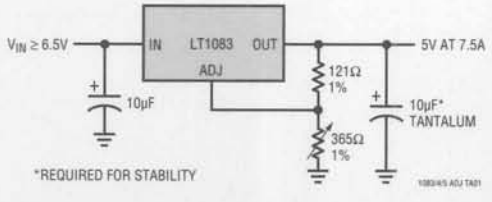
The LT1083 series of positive adjustable regulators are designed to provide 7.5A, 5A and 3A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input-to-output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

The LT1083/LT1084/LT1085 devices are pin compatible with older three-terminal regulators. A 10µF output capacitor is required on these new devices. However, this is included in most regulator designs.

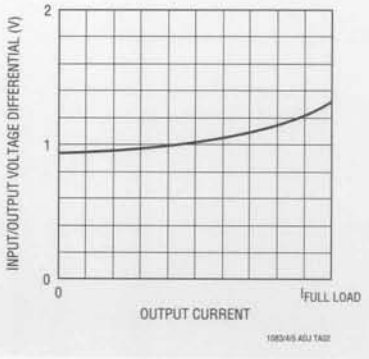
Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

TYPICAL APPLICATION

5V, 7.5A Regulator



Dropout Voltage vs Output Current



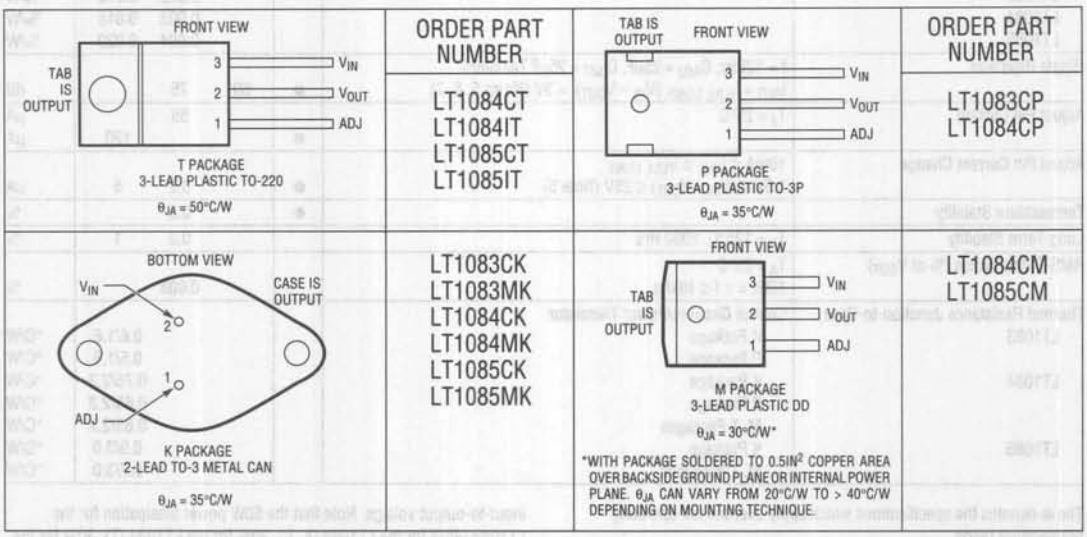
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input-to-Output Voltage Differential
"C" Grades 30V
"I" Grades 30V
"M" Grades 35V
Operating Junction Temperature Range
"C" Grades: Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C
"I" Grades: Control Section ..... –40°C to 125°C
Power Transistor ..... –40°C to 150°C
"M" Grades: Control Section ..... –55°C to 150°C
Power Transistor ..... –55°C to 200°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

100% thermal shutdown functional test.

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_J = 25°C, ($V_{IN} - V_{OUT}$) = 3V		1.238	1.250	1.262	V
	10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 25V (Notes 3, 5, 6)	●	1.225	1.250	1.270	V
Line Regulation	I_{LOAD} = 10mA, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V, T_J = 25°C (Notes 1, 2)			0.015	0.2	%
		●		0.035	0.2	%
	M Grade: 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V (Notes 1, 2)	●		0.05	0.5	%
	C, I Grades: 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 30V (Notes 1, 2)	●		0.05	0.5	%

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation	$(V_{IN} - V_{OUT}) = 3V$					
	$10mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	$T_J = 25°C$ (Notes 1, 2, 3, 5)			0.1	0.3	%
		●		0.2	0.4	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = I_{FULLLOAD}$ (Notes 4, 5, 7)	●		1.3	1.5	V
Current Limit						
LT1083	$(V_{IN} - V_{OUT}) = 5V$	●	8.0	9.5		A
	$(V_{IN} - V_{OUT}) = 25V$	●	0.4	1.0		A
LT1084	$(V_{IN} - V_{OUT}) = 5V$	●	5.5	6.5		A
	$(V_{IN} - V_{OUT}) = 25V$	●	0.3	0.6		A
LT1085	$(V_{IN} - V_{OUT}) = 5V$	●	3.2	4.0		A
	$(V_{IN} - V_{OUT}) = 25V$	●	0.2	0.5		A
Minimum Load Current	$(V_{IN} - V_{OUT}) = 25V$	●		5	10	mA
Thermal Regulation	$T_A = 25°C$, 30ms Pulse					
LT1083				0.002	0.010	%/W
LT1084				0.003	0.015	%/W
LT1085				0.004	0.020	%/W
Ripple Rejection	f = 120Hz, $C_{ADJ} = 25\mu F$, $C_{OUT} = 25\mu F$ Tantalum					
	$I_{OUT} = I_{FULL\ LOAD}$, $(V_{IN} - V_{OUT}) = 3V$ (Notes 5, 6, 7)	●	60	75		dB
Adjust Pin Current	$T_J = 25°C$			55		μA
		●			120	μA
Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	$1.5V \le (V_{IN} - V_{OUT}) \le 25V$ (Note 5)	●		0.2	5	μA
Temperature Stability		●		0.5		%
Long Term Stability	$T_A = 125°C$, 1000 Hrs			0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$					
	$10Hz = \le f \le 10kHz$			0.003		%
Thermal Resistance Junction-to-Case	Control Circuitry/Power Transistor					
LT1083	K Package				0.6/1.6	°C/W
	P Package				0.5/1.6	°C/W
LT1084	K Package				0.75/2.3	°C/W
	P Package				0.65/2.3	°C/W
	M, T Packages				0.65/2.7	°C/W
LT1085	K Package				0.9/3.0	°C/W
	M, T Packages				0.7/3.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissapation (60W for the LT1083, 45W for the LT1084 (K, P), 30W for the LT1084 (T) and 30W for the LT1085). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULLLOAD}$ curve is defined as the minimum value of current limit as a function of input-to-output voltage. Note that the 60W power dissipation for the LT1083 (45W for the LT1084 (K, P), 30W for the LT1084 (T), 30W for the LT1085) is only achievable over a limited range of input-to-output voltage.

Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

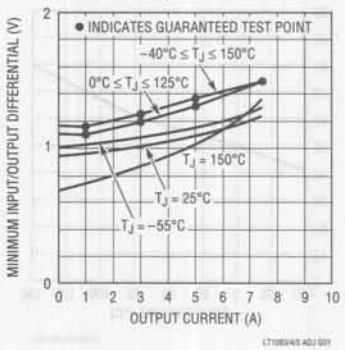
Note 5: For LT1083 $I_{FULL\ LOAD}$ is 5A for $-55°C \le T_J < -40°C$ and 7.5A for $T_J \ge -40°C$.

Note 6: $1.7V \le (V_{IN} - V_{OUT}) \le 25V$ for LT1084 at $-55°C \le T_J \le -40°C$.

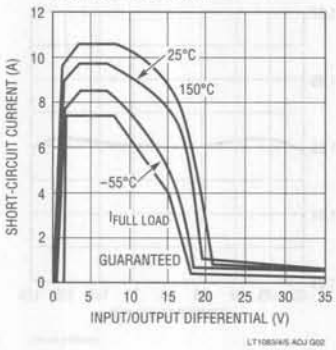
Note 7: Dropout is 1.7V maximum for LT1084 at $-55°C \le T_J \le -40°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

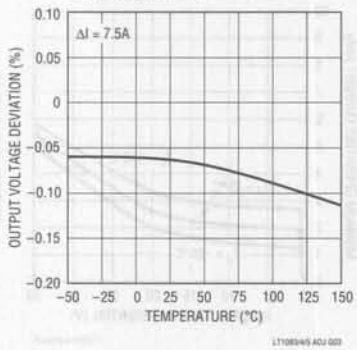
LT1083
Dropout Voltage



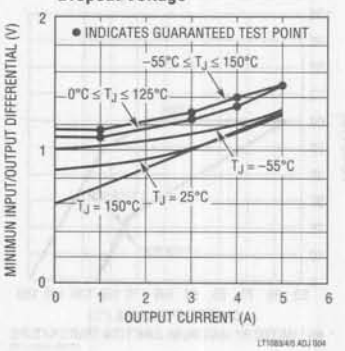
LT1083
Short-Circut Current



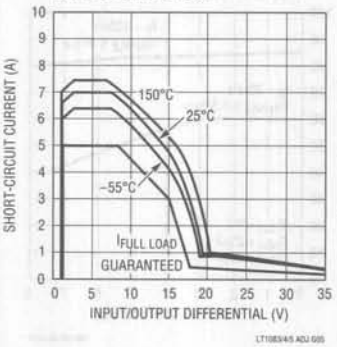
LT1083
Load Regulation



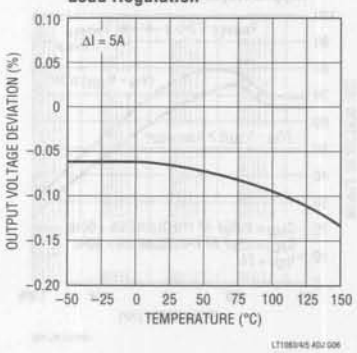
LT1084
Dropout Voltage



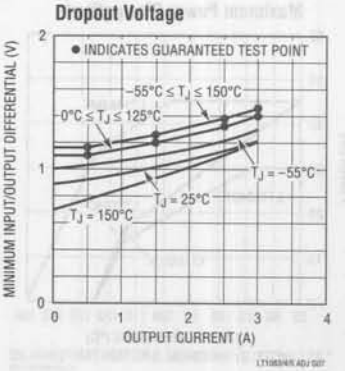
LT11084
Short-Circut Current



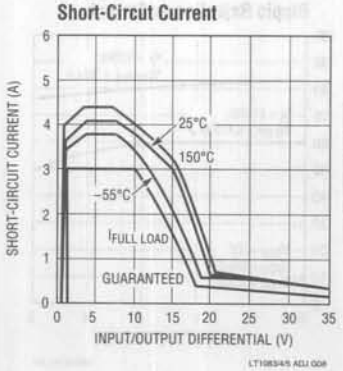
LT1084
Load Regulation



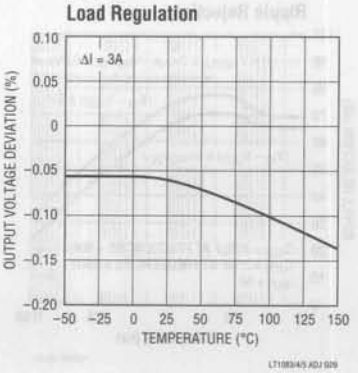
LT1085
Dropout Voltage



LT1085
Short-Circut Current



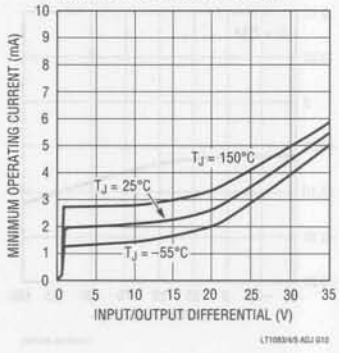
LT1085
Load Regulation



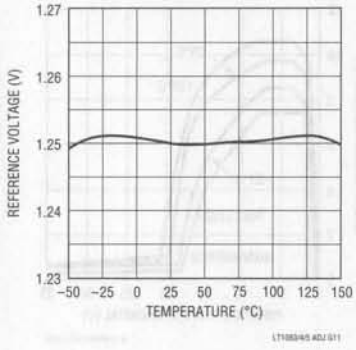
4

TYPICAL PERFORMANCE CHARACTERISTICS

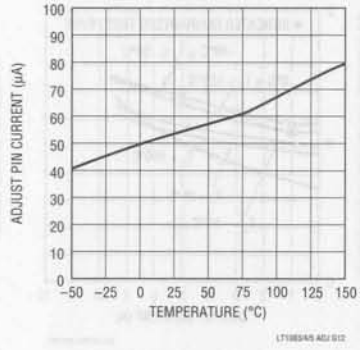
Minimum Operating Current



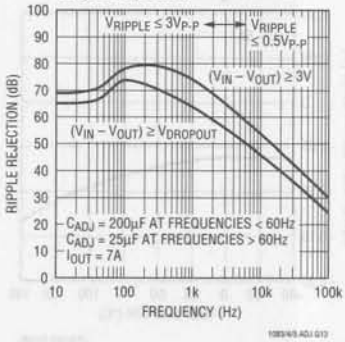
Temperature Stability



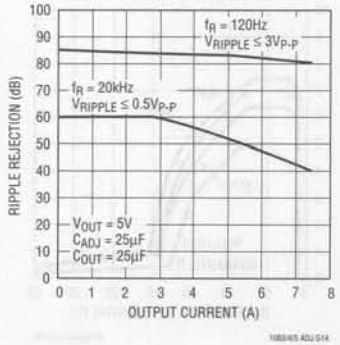
Adjust Pin Current



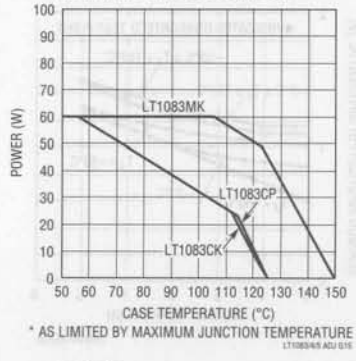
LT1083
Ripple Rejection



LT1083
Ripple Rejection vs Current

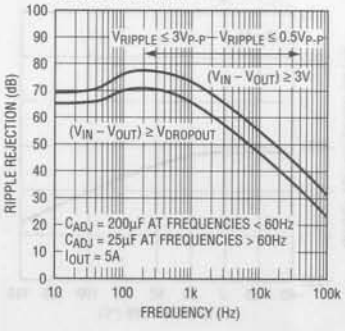


LT1083
Maximum Power Dissipation*

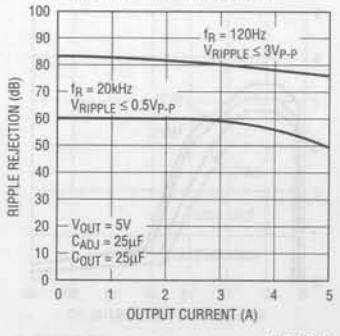


* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

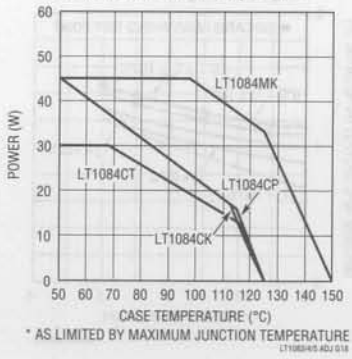
LT1084
Ripple Rejection



LT1084
Ripple Rejection vs Current



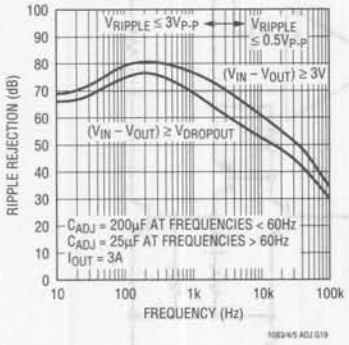
LT1084
Maximum Power Dissipation*



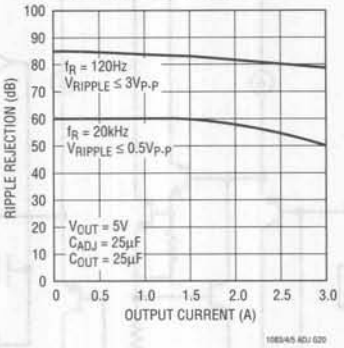
* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS

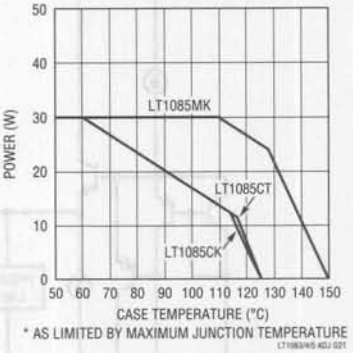
LT1085
Ripple Rejection



LT1085
Ripple Rejection vs Current

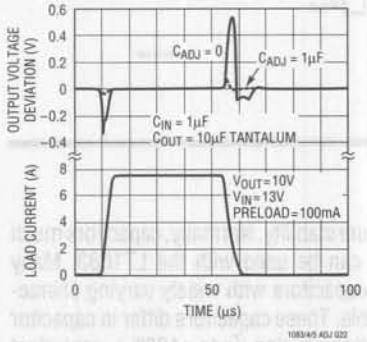


LT1085
Maximum Power Dissipation*

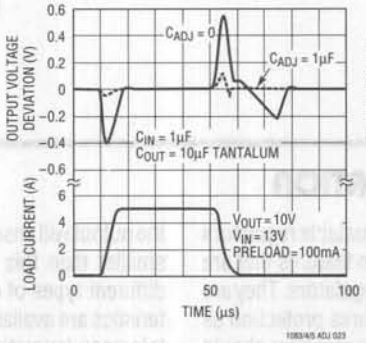


* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

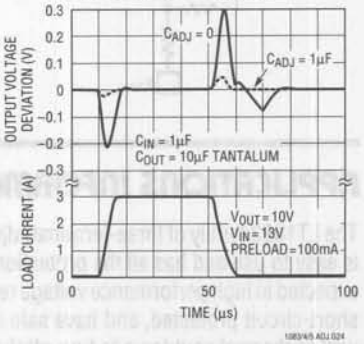
LT1083
Load Transient Response



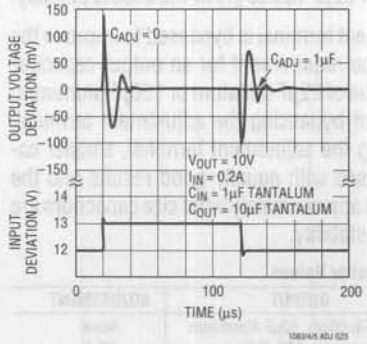
LT1084
Load Transient Response



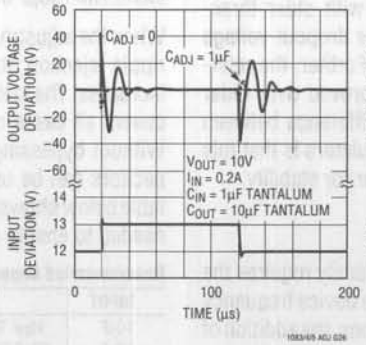
LT1085
Load Transient Response



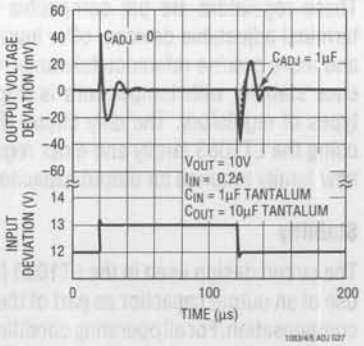
LT1083
Line Transient Response



LT1084
Line Transient Response

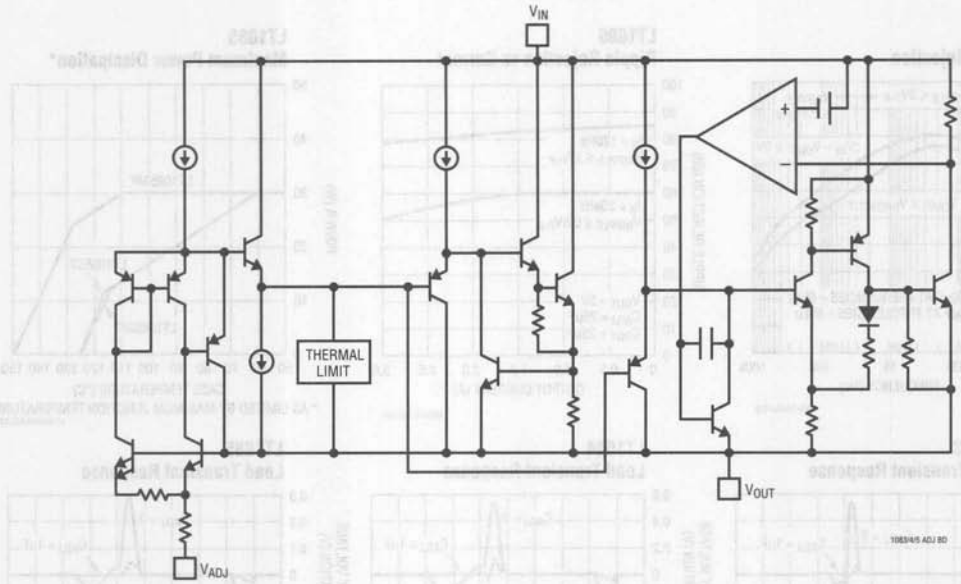


LT1085
Line Transient Response



4

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT1083 family of three-terminal adjustable regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short-circuit protected, and have safe area protection as well as thermal shutdown to turn off the regulator should the junction temperature exceed about 165°C.

These regulators are pin compatible with older three-terminal adjustable devices, offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1083 family and older regulators is that this new family requires an output capacitor for stability.

Stability

The circuit design used in the LT1083 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150µF aluminium electrolytic or a 22µF solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1083. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150µF or 22µF values given will ensure stability.

When the adjustment terminal is bypassed to improve the ripple rejection, the requirement for an output capacitor increases. The value of 22µF tantalum or 150µF aluminum covers all cases of bypassing the adjustment terminal. Without bypassing the adjustment terminal, smaller capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

INPUT	OUTPUT	ADJUSTMENT
10µF	10µF Tantalum, 50µF Aluminum	None
10µF	22µF Tantalum, 150µF Aluminum	20µF

APPLICATIONS INFORMATION

Normally, capacitor values on the order of 100µF are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1083 regulators.

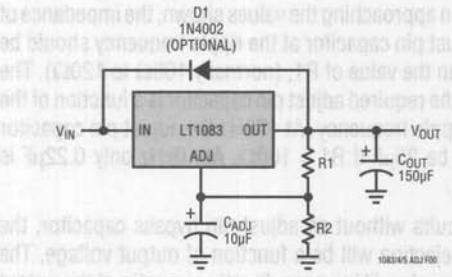
Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1083 series and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however, it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

In normal operation, the LT1083 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1083 adjustment pin are limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short-circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1083 family can handle microsecond surge currents of 50A to 100A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with a high value of output capacitors, such as 1000µF to 5000µF and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1083 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ±25V, with respect to the output without any device degradation. Of course, as with any IC regulator, exceeding the maximum input to output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1083 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1083 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1083.

APPLICATIONS INFORMATION

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

The typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1, (normally 100Ω to 120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 25µF if R1 = 100Ω. At 10kHz only 0.22µF is needed.

For circuits without an adjust pin bypass capacitor, the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or four times larger. Ripple rejection will be degraded by 12dB from the value shown on the typical curve.

Output Voltage

The LT1083 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor R1 between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

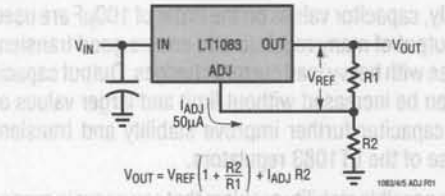


Figure 1. Basic Adjustable Regulator

Load Regulation

Because the LT1083 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider R1 is connected *directly* to the case *not to the load*. This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_P \times \left(\frac{R2+R1}{R1}\right),\ R_P = \text{Parasitic Line Resistance}$$

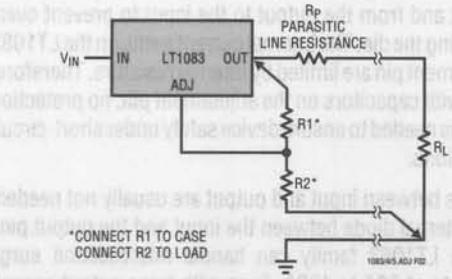


Figure 2. Connections for Best Load Regulation

APPLICATIONS INFORMATION

Connected as shown, R_P is not multiplied by the divider ratio. R_P is about 0.004Ω per foot using 16-gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible and use large wire or PC board traces.

Thermal Considerations

The LT1083 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction-to-case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

For example, using an LT1083CK (TO-3, Commercial) and assuming:

V_{IN} (max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 6A,

T_A = 75°C, $\theta_{HEAT\ SINK}$ = 1°C/W,

$\theta_{CASE\text{-}TO\text{-}HEAT\ SINK}$ = 0.2°C/W for K package with thermal compound.

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT})(I_{OUT}) = 24W$$

Junction temperature will be equal to:

$$T_J = T_A + P_D\ (\theta_{HEAT\ SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\ SINK} + \theta_{JC})$$

For the Control Section:

$T_J = 75°C + 24W\ (1°C/W + 0.2°C/W + 0.6°C/W) = 118°C$
$118°C < 125°C = T_{JMAX}$ (Control Section Commercial Range)

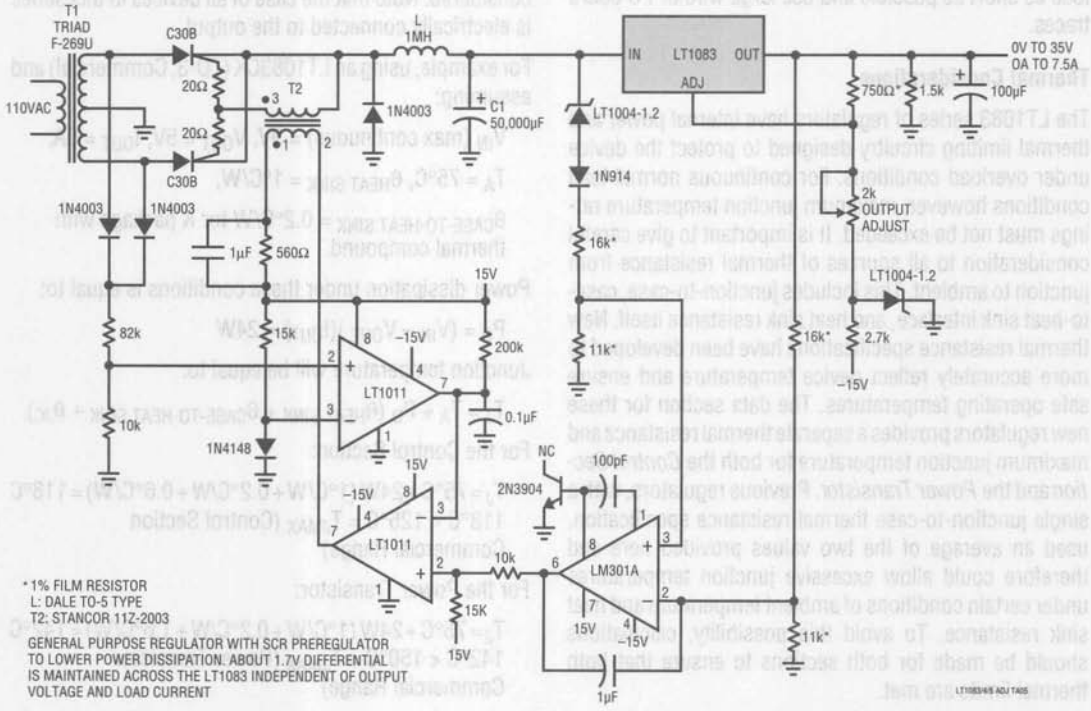
For the Power Transistor:

$T_J = 75°C + 24W\ (1°C/W + 0.2°C/W + 1.6°C/W) = 142°C$
$142°C < 150°C = T_{JMAX}$ (Power Transistor Commercial Range)

In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

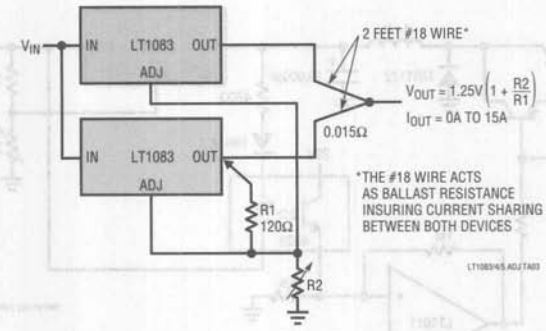
TYPICAL APPLICATIONS

7.5A Variable Regulator

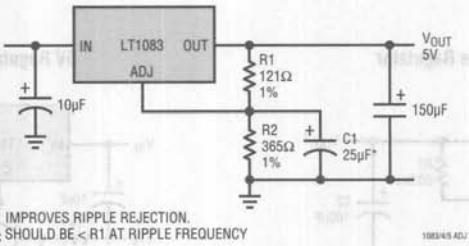


TYPICAL APPLICATIONS

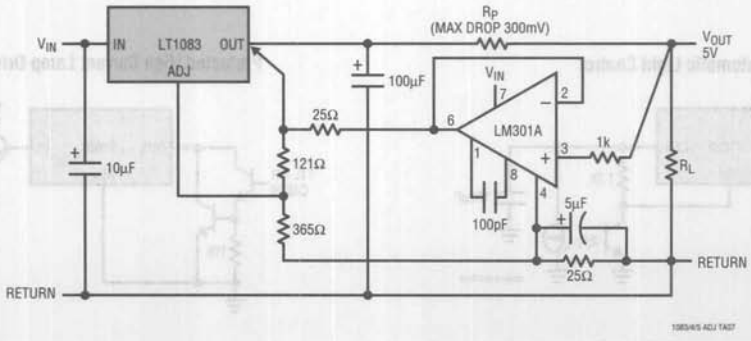
Paralleling Regulators



Improving Ripple Rejection

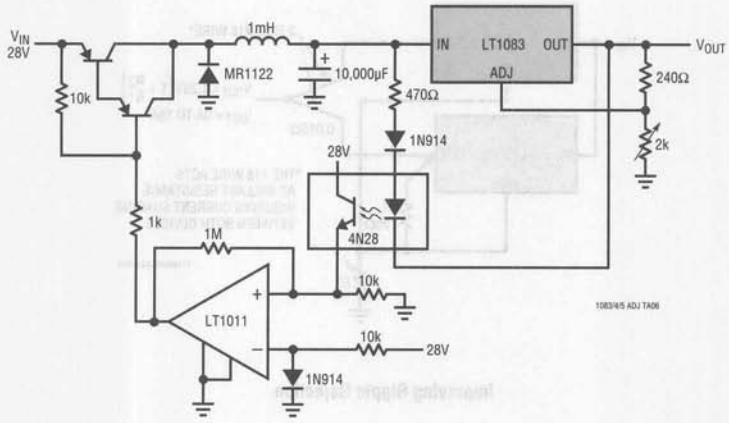


Remote Sensing

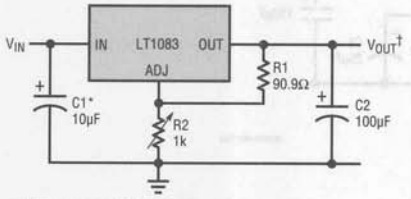


TYPICAL APPLICATIONS

High Efficiency Regulator with Switching Preregulator



1.2V to 15V Adjustable Regulator

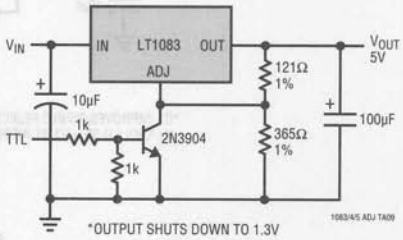


*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$$\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

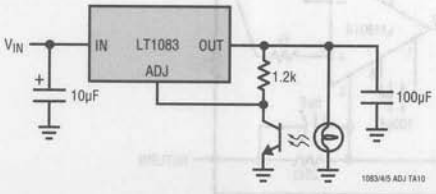
1083/4/5 ADJ TA08

5V Regulator with Shutdown*

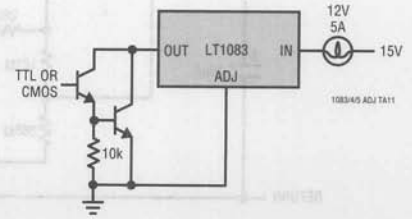


*OUTPUT SHUTS DOWN TO 1.3V

Automatic Light Control



Protected High Current Lamp Driver



LT1083/LT1084/LT1085 Fixed

3A, 5A, 7.5A Low Dropout Positive Fixed Regulators

FEATURES

- Three-Terminal 5V and 12V
- Output Current of 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- Line Regulation: 0.015%
- Load Regulation: 0.1%
- 100% Thermal Limit Functional Test
- Adjustable Versions Available

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DEVICE	OUTPUT CURRENT*
LT1083	7.5 Amps
LT1084	5.0 Amps
LT1085	3.0 Amps

*For a 1.5A low dropout regulator see the LT1086 data sheet.

DESCRIPTION

The LT1083 series of positive adjustable regulators are designed to provide 3A, 5A and 7.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the output voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

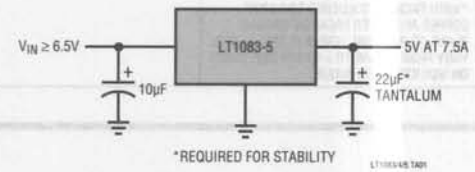
The 1083 series devices are pin compatible with older three-terminal regulators. A 10µF output capacitor is required on these new devices; however, this is usually included in most regulator designs.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

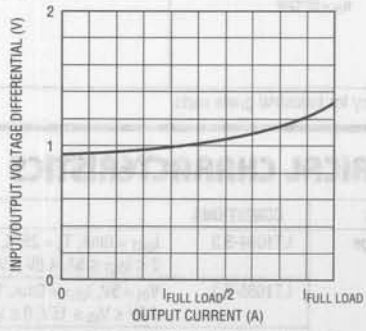
4

TYPICAL APPLICATION

5V, 7.5A Regulator



Dropout Voltage vs Output Current



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input Voltage (Note 1) 30V
Operating Input Voltage
- 3.3V, 3.6V Devices 20V
- 5V Devices 20V
- 12V Devices 25V

Operating Junction Temperature Range
- "C" Grades
  - Control Section ..... 0°C to 125°C
  - Power Transistor ..... 0°C to 150°C
- "M" Grades
  - Control Section ..... –55°C to 150°C
  - Power Transistor ..... –55°C to 200°C

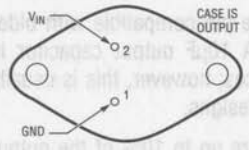
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note 1: Although the devices maximum operating voltage is limited, (20V for a 3V, 5V device, and 25V for a 12V device) the devices are guaranteed to withstand transient input voltages up to 30V. For input voltages greater than the maximum operating input voltage some degradation of specifications will occur. For input/output voltage differentials greater than 15V, a minimum external load of 5mA is required to maintain regulation.

PRECONDITIONING

100% Thermal Limit Functional Test.

PACKAGE/ORDER INFORMATION

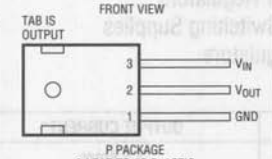


K PACKAGE
2-LEAD TO-3 METAL CAN

θ_{JA} = 35°C/W

ORDER PART NUMBER

LT1083CK-5 LT1084MK-5
LT1083CK-12 LT1084MK-12
LT1083MK-5 LT1085CK-5
LT1083MK-12 LT1085CK-12
LT1084CK-5 LT1085MK-5
LT1084CK-12 LT1085MK-12

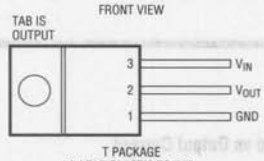


P PACKAGE
3-LEAD TO-3P PLASTIC

θ_{JA} = 45°C/W

ORDER PART NUMBER

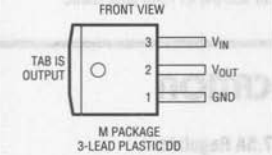
LT1083CP-5
LT1083CP-12
LT1084CP-5
LT1084CP-12



T PACKAGE
3-LEAD PLASTIC TO-220

θ_{JA} = 50°C/W

LT1084CT-3.3
LT1084CT-5
LT1084CT-12
LT1085CT-3.3
LT1085CT-3.6
LT1085CT-5
LT1085CT-12



M PACKAGE
3-LEAD PLASTIC DD

θ_{JA} = 30°C/W*

* WITH PACKAGE SOLDERED TO 0.52IN^2 COPPER AREA OVER BACKSIDE GROUND PLANE OR INTERNAL POWER PLANE. θ_{JA} CAN VARY FROM 20°C/W TO > 40°C/W DEPENDING ON MOUNTING TECHNIQUE.

LT1085CM-3.3
LT1085CM-3.6

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	LT1084-3.3	I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 8V (K Package Only)		3.270	3.300	3.330	V
		$0 \le I_{OUT} \le 5A$, $4.8V \le V_{IN} \le 15V$ (Note 8)	●	3.235	3.300	3.365	V
	LT1085-3.3	V_{IN} = 5V, I_{OUT} = 0mA, T_J = 25°C (K Package Only)		3.270	3.300	3.330	V
		$4.8V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 3A$ (Note 8)	●	3.235	3.300	3.365	V
	LT1085-3.6	V_{IN} = 5V, I_{OUT} = 0mA, T_J = 25°C (K Package Only)		3.564	3.600	3.636	V
		$5V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 3A$ (Note 8)	●	3.500		3.672	V
		$5V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 3A$, $T_J \ge 0°C$ (Note 8)		3.528		3.672	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	LT1085-3.6	$5V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 2.5A$ (Note 8)	●	3.528		3.672	V
		$V_{IN} = 4.75V$, $I_{OUT} = 3A$, $T_J \ge 0°C$		3.350		3.672	V
		$V_{IN} = 4.75V$, $I_{OUT} = 2.5A$, $T_J \ge 0°C$		3.450		3.672	V
		$V_{IN} = 4.75V$, $I_{OUT} = 1.5A$, $T_J > 0°C$		3.528		3.672	V
	LT1083/4/5-5	$I_{OUT} = 0mA$, $T_J = 25°C$, $V_{IN} = 8V$ (K Package Only)		4.950	5.000	5.050	V
		$0 \le I_{OUT} \le I_{FULLOAD}$, $6.5V \le V_{IN} \le 20V$ (Notes 3, 5, 6, 8)		4.900	5.000	5.100	V
	LT1083/4/5-12	$I_{OUT} = 0mA$, $T_J = 25°C$, $V_{IN} = 15V$ (K Package Only)		11.880	12.000	12.120	V
		$0 \le I_{OUT} \le I_{FULLOAD}$, $13.5V \le V_{IN} \le 25V$ (Notes 3, 5, 6, 8)		11.760	12.000	12.240	V
Line Regulation	LT1084-3.3	$I_{OUT} = 0mA$, $T_J = 25°C$, $4.8V \le V_{IN} \le 15V$			0.5	6	mV
			●		1.0	6	mV
	LT1085-3.3	$4.8V \le V_{IN} \le 15V$, $I_{OUT} = 0mA$, $T_J = 25°C$			0.5	6	mV
			●		1.0	6	mV
	LT1085-3.6	$4.8V \le V_{IN} \le 15V$, $I_{OUT} = 0mA$, $T_J = 25°C$			0.5	6	mV
			●		1.0	6	mV
	LT1083/4/5-5	$I_{OUT} = 0mA$, $T_J = 25°C$, $6.5V \le V_{IN} \le 20V$ (Notes 1, 2)			0.5	10	mV
			●		1.0	10	mV
	LT1083/4/5-12	$I_{OUT} = 0mA$, $T_J = 25°C$, $13.5V \le V_{IN} \le 25V$ (Notes 1, 2)			1.0	25	mV
			●		2.0	25	mV
Load Regulation	LT1084-3.3	$V_{IN} = 5V$, $0 \le I_{OUT} \le 5A$, $T_J = 25°C$			3	15	mV
			●		7	20	mV
	LT1085-3.3	$V_{IN} = 5V$, $0 \le I_{OUT} \le 3A$, $T_J = 25°C$			3	15	mV
			●		7	20	mV
	LT1085-3.6	$V_{IN} = 5.25V$, $0 \le I_{OUT} \le 3A$, $T_J = 25°C$			3	15	mV
			●		7	20	mV
	LT1083/4/5-5	$V_{IN} = 8V$, $0 \le I_{OUT} \le I_{FULLLOAD}$, $T_J = 25°C$ (Notes 1, 2, 3, 5)			5	20	mV
			●		10	35	mV
	LT1083/4/5-12	$V_{IN} = 15V$, $0 \le I_{OUT} \le I_{FULLLOAD}$, $T_J = 25°C$ (Notes 1, 2, 3, 5)			12	36	mV
			●		24	72	mV
Dropout Voltage	LT1084/5-3.3	$\Delta V_{OUT} = 33mV$, $I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●		1.3	1.5	V
	LT1085-3.6	$\Delta V_{OUT} = 36mV$, $I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●		1.3	1.5	V
	LT1083/4/5-5	$\Delta V_{OUT} = 50mV$, $I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●		1.3	1.5	V
	LT1083/4/5-12	$\Delta V_{OUT} = 120mV$, $I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●		1.3	1.5	V
Current Limit	LT1083-5	$V_{IN} = 10V$	●	8.0	9.5		A
	LT1083-12	$V_{IN} = 17V$	●	8.0	9.5		A
	LT1084-3.3	$V_{IN} = 8V$	●	5.5	6.5		A
	LT1084-5	$V_{IN} = 10V$	●	5.5	6.5		A
	LT1084-12	$V_{IN} = 17V$	●	5.5	6.5		A
	LT1085-3.3/3.6	$V_{IN} = 8V$	●	3.2	4.0		A
	LT1085-5	$V_{IN} = 10V$	●	3.2	4.0		A
	LT1085-12	$V_{IN} = 17V$	●	3.2	4.0		A
Quiescent Current	LT1084-3.3	$V_{IN} = 18V$	●		5.0	10.0	mA
	LT1085-3.3	$V_{IN} = 18V$	●		5.0	10.0	mA
	LT1085-3.6	$V_{IN} = 18V$	●		5.0	10.0	mA
	LT1083/4/5-5	$V_{IN} \le 20V$	●		5.0	10.0	mA
	LT1083/4/5-12	$V_{IN} \le 25V$	●		5.0	10.0	mA
Thermal Regulation	LT1083-5/12	$T_A = 25°C$, 30ms pulse			0.002	0.010	%/W
	LT1084-3.3/5/12				0.003	0.015	%/W
	LT1085-3.3/3.6/5/12				0.004	0.020	%/W
Ripple Rejection	$f = 120Hz$, $C_{OUT} = 25\mu F$ Tantalum, $I_{OUT} = I_{FULLLOAD}$						
	LT1084-3.3	$f = 120Hz$, $C_{OUT} = 25\mu F$ Tantalum, $I_{OUT} = 5A$, $V_{IN} = 6.3V$	●	60	72		dB

4

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Ripple Rejection	LT1085-3.3	f = 120Hz, C_{OUT} = 25µF Tantalum, V_{IN} = 6.3V, I_{OUT} = 3A	●	60	72		dB
	LT1085-3.6	f = 120Hz, C_{OUT} = 25µF Tantalum, V_{IN} = 6.6V, I_{OUT} = 3A	●	60	72		dB
	LT1083/4/5-5	V_{IN} = 8V (Note 5)	●	60	68		dB
	LT1083/4/5-12	V_{IN} = 15V (Note 5)	●	54	60		dB
Temperature Stability			●		0.5		%
Long Term Stability	T_A = 125°C, 1000 Hrs.				0.03	1.0	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz = ≤ f ≤ 10kHz				0.003		%
Thermal Resistance Junctrion-to-Case	Control Circuitry/Power Transistor (See Applications Information)						
	LT1083	K Package				0.6/1.6	°C/W
		P Package				0.5/1.6	°C/W
	LT1084	K Package				0.75/2.3	°C/W
		P Package				0.65/2.3	°C/W
		T Package				0.65/2.7	°C/W
	LT1085	K Package				0.9/3.0	°C/W
		T Package				0.7/3.0	°C/W
		DD Package				0.7/3.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (60W for the LT1083, 45W for the LT1084 (K, P), 30W for the LT1084 (T) and 30W for the LT1085). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output range.

Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULLLOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 60W power dissipation for the LT1083 (45W for the LT1084 (K, P), 30W for the LT1084 (T), 30W for the LT1085) is only achievable over a limited range of input to output voltage.

Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

Note 5: For LT1083 $I_{FULL\ LOAD}$ is 5A for $-55°C \le T_J \le -40°C$ and 7.5A for $T_J \ge -40°C$.

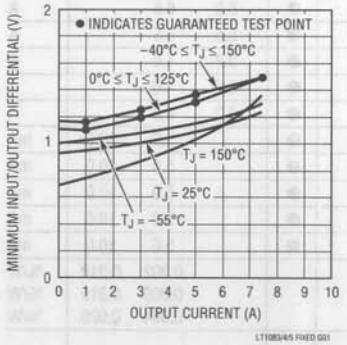
Note 6: $1.7V \le (V_{IN} - V_{OUT}) \le 25V$ for LT1084 at $-55°C \le T_J \le -40°C$.

Note 7: Dropout voltage 1.7V maximum for LT1084 at $-55 \le T_J \le -40°C$.

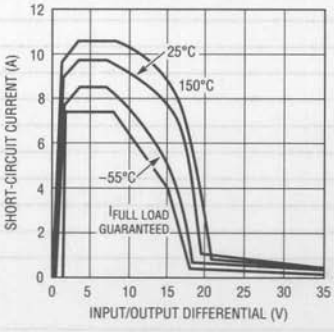
Note 8: Full load current is not available at all input-output voltages. See Notes 2,3,5.

TYPICAL PERFORMANCE CHARACTERISTICS

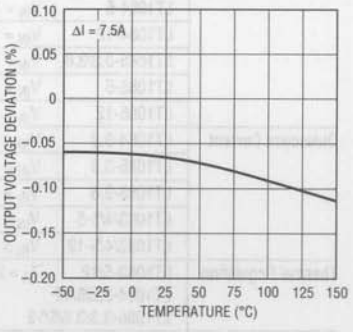
LT1083 Dropout Voltage



LT1083 Short-Circuit Current

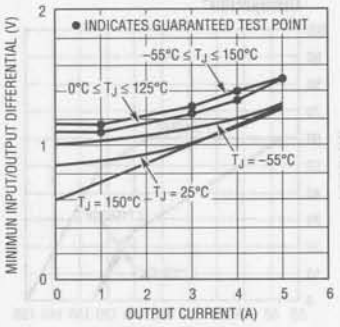


LT1083 Load Regulation

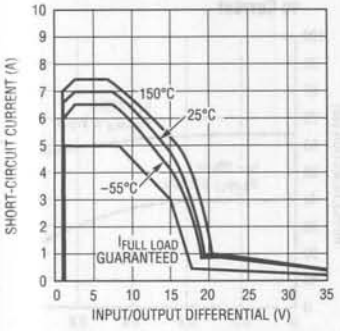


TYPICAL PERFORMANCE CHARACTERISTICS

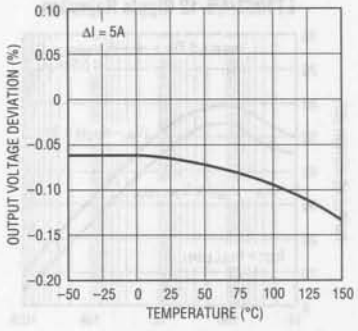
LT1084 Dropout Voltage



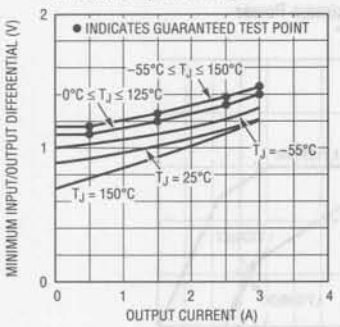
LT1084 Short Circuit Current



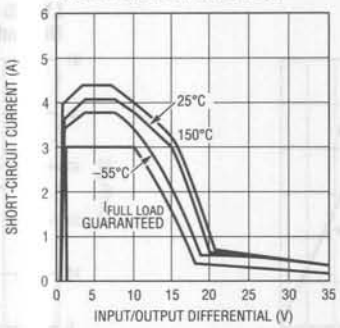
LT1084 Load Regulation



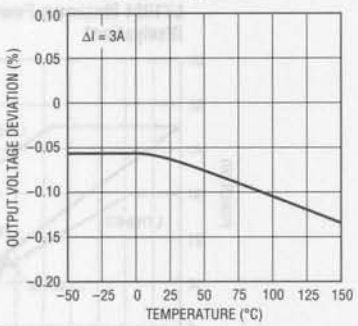
LT1085 Dropout Voltage



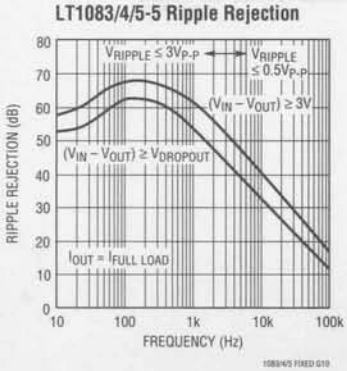
LT1085 Short-Circuit Current



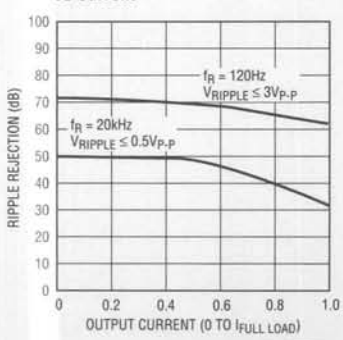
LT1085 Load Regulation



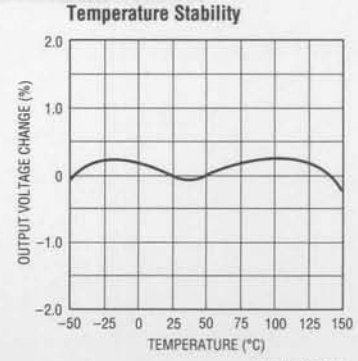
LT1083/4/5-5 Ripple Rejection



LT1083/4/5-5 Ripple Rejection vs Current



Temperature Stability



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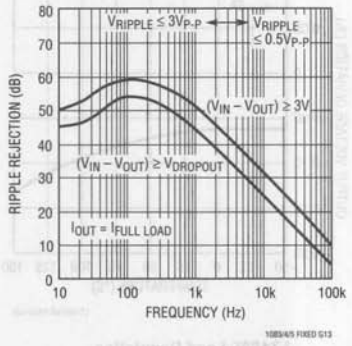
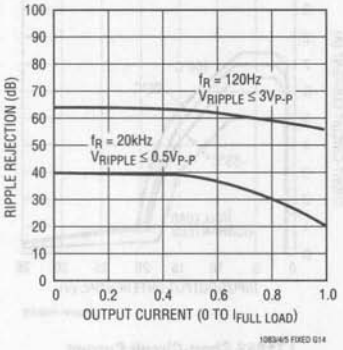
TYPICAL PERFORMANCE CHARACTERISTICS

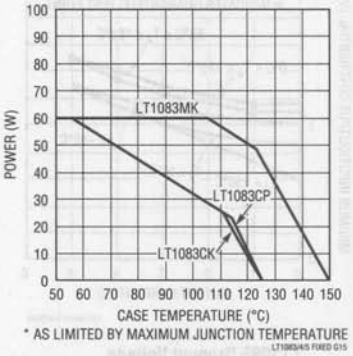
LT1083/4/5-12 Ripple Rejection



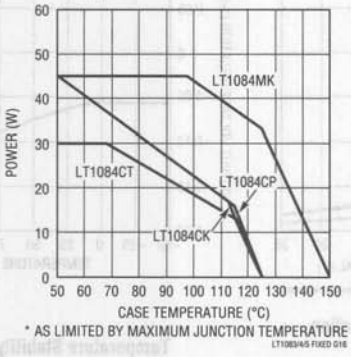
LT1083/4/5-12 Ripple Rejection vs Current



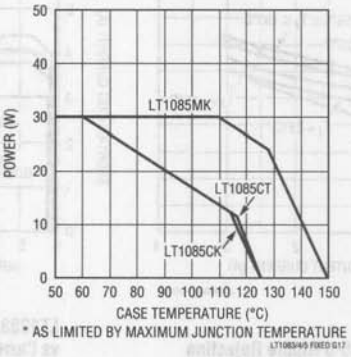
LT1083 Maximum Power Dissipation*



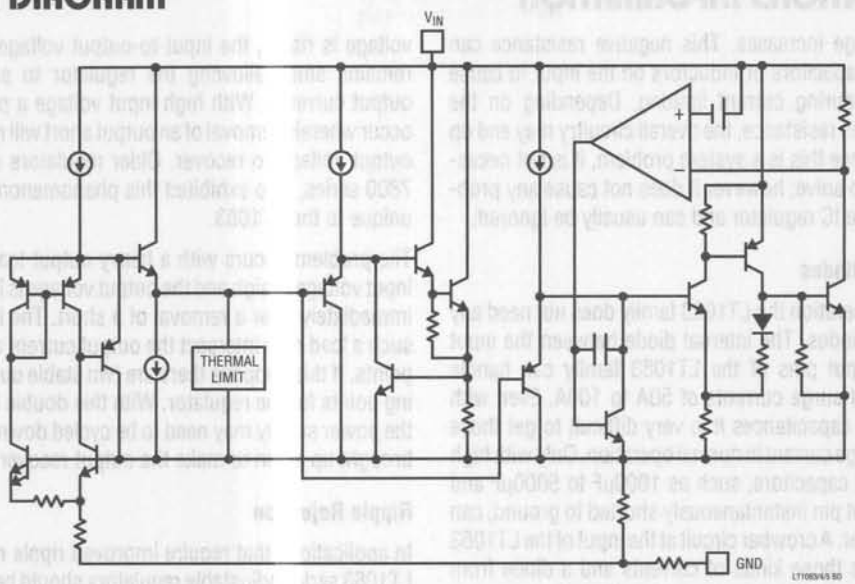
LT1084 Maximum Power Dissipation*



LT1085 Maximum Power Dissipation*



BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT1083 family of three-terminal regulators are easy to use and have all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C.

These regulators offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1083 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1083 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150µF aluminum electrolytic or a 22µF solid tantalum on the output will ensure stability. Normally capacitors much smaller than this can be used with the LT1083. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150µF or 22µF values given will ensure stability.

Normally, capacitor values on the order of 100µF are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitance further improve stability and transient response of the LT1083 regulators.

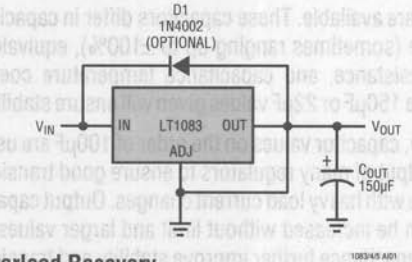
Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because in current limit the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negitive resistance since increasing voltage causes current to decrease. Negitive resistance during current limit is not unique to the LT1083 series and has been present on all power IC regulators. The value of negative resistance is a function of how fast the current limit is folded back as input-to-

APPLICATIONS INFORMATION

output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillations during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

In normal operation the LT1083 family does not need any protection diodes, The internal diode between the input and the output pins of the LT1083 family can handle microsecond surge currents of 50A to 100A. Even with large output capacitances it is very difficult to get those values of surge current in normal operation. Only with high value output capacitors, such as 1000µF to 5000µF and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1083 can generate those kinds of currents and a diode from output-to-input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate currents large enough to do any damage.



Overload Recovery

Like any of the IC power regulators, the LT1083 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1083 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small allowing the regulator to supply large output currents. With high input voltage a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators such as the 7800 series, also exhibited this phenomenon so it is not unique to the LT1083.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens there are two stable output operating points for the regulator. With this double intersection the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

In applications that require improved ripple rejection the LT1083 series adjustable regulators should be used. With LT1083 series adjustable regulators the addition of a bypass capacitor from the adjust pin to ground will reduce output ripple by the ratio of $V_{OUT}/1.25V$. See LT1083 series adjustable regulator data sheet.

Load Regulation

Because the LT1083 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will not be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for the load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the ground pin of the device returned to the negative side of the load.

Thermal Considerations

The LT1083 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, and heat sink resistance itself. New

APPLICATIONS INFORMATION

thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Section*. Previous regulators, with a single junction-to-case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat sink interface is strongly recommended. If the case of the device must be electronically isolated, a thermally conductive spacer can be used as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electronically connected to the ouput.

For example, using a LT1083-5CK (TO-3, Commercial) and assuming:

V_{IN}(max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 6A,
T_A = 75°C $\theta_{HEAT\ SINK}$ = 1°C/W,
$\theta_{CASE\text{-}TO\text{-}HEAT\ SINK}$ = 0.2°C/W for K package with thermal compound.

Power dissipation under these conditions is equal to:

$P_D = (V_{IN} - V_{OUT})\ (I_{OUT})$ = 24W

Junction temperature will be equal to:

$T_J = T_A + P_D\ (\theta_{HEAT\ SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\ SINK} + \theta_{JC})$

For the Control Section:

T_J = 75°C + 24W (1°C/W + 0.2°C/W + 0.6°C/W) = 118°C
118°C < 125°C = T_{JMAX} (Control Section Commercial Range)

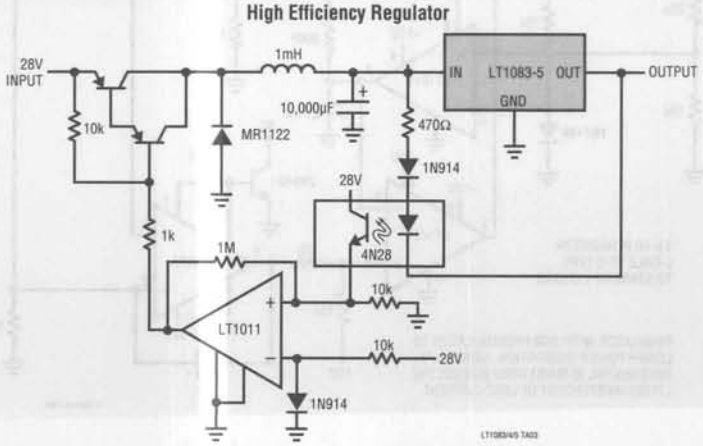
For the Power Transistor:

T_J = 75°C + 24W (1°C/W + 0.2°C/W + 1.6°C/W) = 142°C
142°C < 150°C = T_{JMAX} (Power Transistor Commercial Range)

in both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

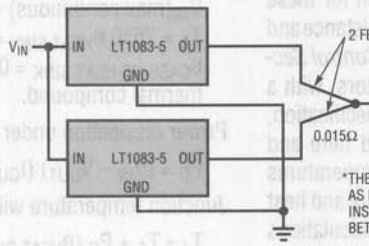
TYPICAL APPLICATIONS

High Efficiency Regulator

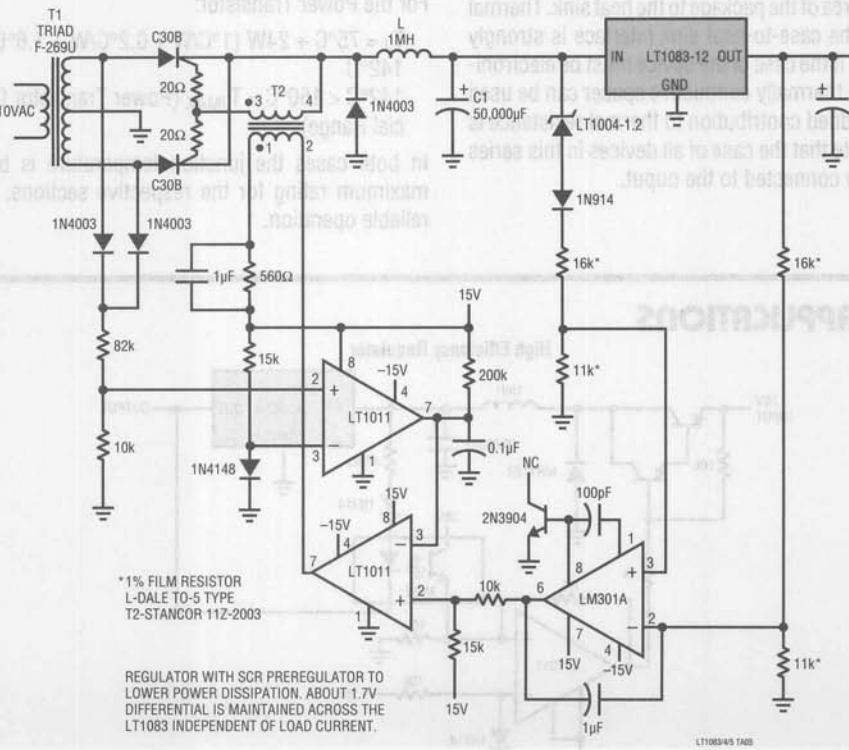


TYPICAL APPLICATIONS

Paralleling Regulators

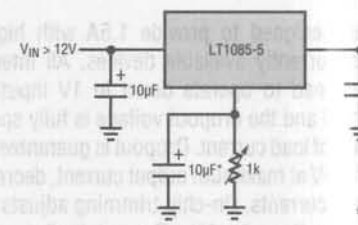


7.5A Regulator



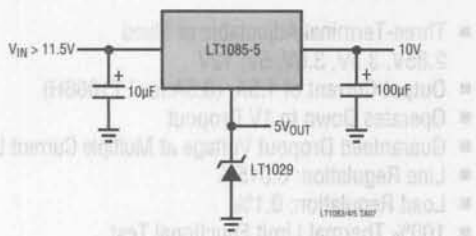
TYPICAL APPLICATIONS

Adjusting Output Voltage

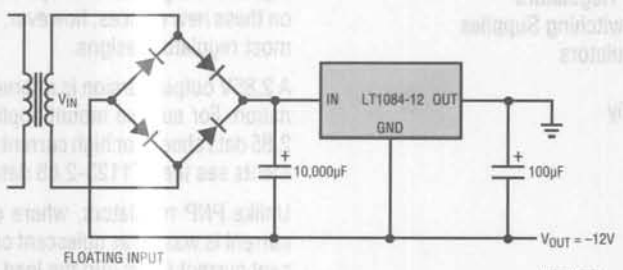


*OPTIONAL IMPROVES RIPPLE REJECTION

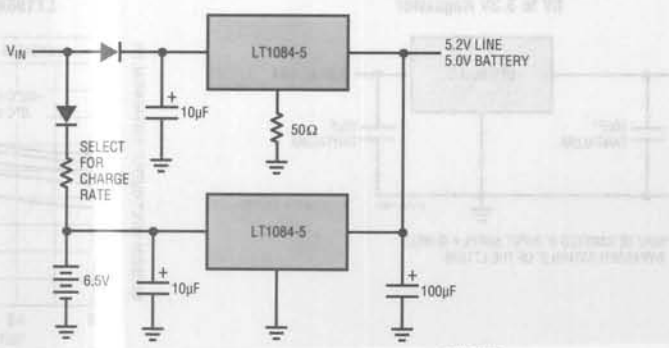
Regulator with Reference



Low Dropout Negative Supply



Battery Backed Up Regulated Supply



1.5A Low Dropout Positive Regulators Adjustable and Fixed 2.85V, 3.3V, 3.6V, 5V, 12V

FEATURES

- Three-Terminal Adjustable or Fixed 2.85V, 3.3V, 3.6V, 5V, 12V
- Output Current of 1.5A, (0.5A for LT1086H)
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- Line Regulation: 0.015%
- Load Regulation: 0.1%
- 100% Thermal Limit Functional Test

APPLICATIONS

- SCSI-2 Active Terminator
- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers
- Microprocessor Supply

DESCRIPTION

The LT1086 is designed to provide 1.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input-to-output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference/ouput voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

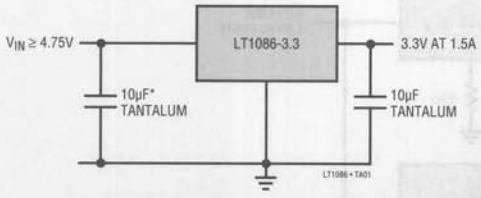
The LT1086 is pin compatible with older three-terminal adjustable regulators. A 10µF output capacitor is required on these new devices; however, this is usually included in most regulator designs.

A 2.85V output version is offered for SCSI-2 active termination. For surface mount applications see the LT1117-2.85 data sheet. For high current or lower dropout requirements see the LT1123-2.85 data sheet.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1086 quiescent current flows into the load, increasing efficiency.

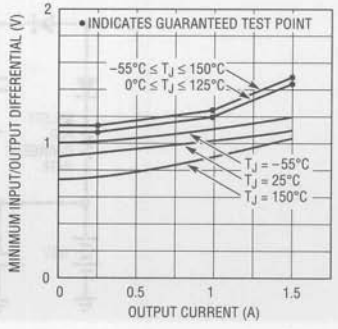
TYPICAL APPLICATION

5V to 3.3V Regulator



*MAY BE OMITTED IF INPUT SUPPLY IS WELL BYPASSED WITHIN 2" OF THE LT1086

LT1086 Dropout Voltage



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input Voltage (Note 1) 30V
Operating Input Voltage
- Adjustable Devices 25V
- 2.85V Devices 18V
- 3.3V, 3.6V, and 5V Devices 20V
- 12V Devices 25V

Operating Junction Temperature Range
- "C" Grades
  - Control Section ..... 0°C to 125°C
  - Power Transistor ..... 0°C to 150°C
- "M" Grades
  - Control Section ..... –55°C to 150°C
  - Power Transistor ..... –55°C to 200°C

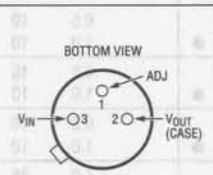
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note 1: Although the device's maximum operating voltage is limited, (18V for a 2.85V device, 20V for a 5V device, and 25V for adjustable and 12V devices) the devices are guaranteed to withstand transient input voltages up to 30V. For input voltages greater than the maximum operating input voltage some degradation of specifications will occur. For 5V and 12V devices operating at input/output voltage differentials greater than 15V, a minimum external load of 5mA is required to maintain regulation.

PRECONDITIONING

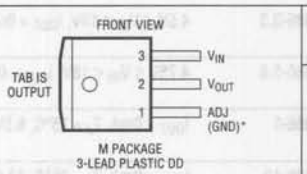
100% Thermal Shutdown Functional Test.

PACKAGE/ORDER INFORMATION



H PACKAGE
3-LEAD TO-39 METAL CAN
θ_{JA} = 150°C/W

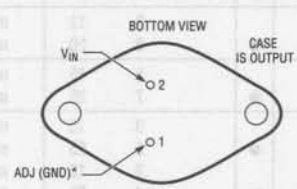
ORDER PART NUMBER
LT1086MH



M PACKAGE
3-LEAD PLASTIC DD
θ_{JA} = 30°C/W**

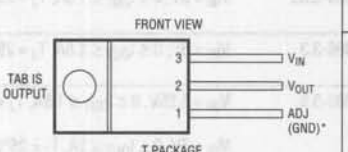
** WITH PACKAGE SOLDERED TO 0.5IN² COPPER AREA OVER BACKSIDE GROUND PLANE OR INTERNAL POWER PLANE. θ_{JA} CAN VARY FROM 20°C/W TO >40°C/W DEPENDING ON MOUNTING TECHNIQUE.

ORDER PART NUMBER
LT1086CM
LT1086CM-3.3
LT1086CM-3.6



K PACKAGE
2-LEAD TO-3 METAL CAN
θ_{JA} = 35°C/W

ORDER PART NUMBER
LT1086CK
LT1086CK-5
LT1086CK-12
LT1086MK
LT1086MK-5
LT1086MK-12



T PACKAGE
3-LEAD PLASTIC TO-220
θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1086CT
LT1086CT-2.85
LT1086CT-3.3
LT1086CT-3.6
LT1086CT-5
LT1086CT-12

*For fixed versions.
Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (Note 2)	LT1086, LT1086H	I_{OUT} = 10mA, T_J = 25°C, ($V_{IN} - V_{OUT}$) = 3V (K Package Only)		1.238	1.250	1.262	V
		10mA ≤ I_{OUT} ≤ 1.5A, (0.5A for LT1086H), 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V	●	1.225	1.250	1.270	V
Output Voltage (Note 2)	LT1086-2.85	I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 5V (K Package Only)		2.82	2.85	2.88	V
		0V ≤ I_{OUT} ≤ 1.5A, 4.35V ≤ V_{IN} ≤ 18V	●	2.79	2.85	2.91	V
	LT1086-3.3	V_{IN} = 5V, I_{OUT} = 0mA, T_J = 25°C (K Package Only)		3.267	3.300	3.333	V
		4.75V ≤ V_{IN} ≤ 15V, 0V ≤ I_{OUT} ≤ 1.5A	●	3.235	3.300	3.365	V
	LT1086-3.6	V_{IN} = 5V, I_{OUT} = 0mA, T_J = 25°C		3.564	3.600	3.636	V
		5V ≤ V_{IN} ≤ 18V, 0 ≤ I_{OUT} ≤ 1.5A	●	3.500		3.672	V
		4.75V ≤ V_{IN} ≤ 18V, 0 ≤ I_{OUT} ≤ 1A, T_J ≥ 0°C		3.500		3.672	V
		V_{IN} = 4.75V, I_{OUT} = 1.5A, T_J ≥ 0°C		3.300		3.672	V
	LT1086-5	I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 8V (K Package Only)		4.950	5.000	5.050	V
		0 ≤ I_{OUT} ≤ 1.5A, 6.5V ≤ V_{IN} ≤ 20V	●	4.900	5.000	5.100	V
	LT1086-12	I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 15V (K Package Only)		11.880	12.000	12.120	V
		0 ≤ I_{OUT} ≤ 1.5A, 13.5V ≤ V_{IN} ≤ 25V	●	11.760	12.000	12.240	V
Line Regulation	LT1086, LT1086H	I_{LOAD} = 10mA, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V, T_J = 25°C			0.015	0.2	%
			●		0.035	0.2	%
	LT1086-2.85	I_{OUT} = 0mA, T_J = 25°C, 4.35V ≤ V_{IN} ≤ 18V			0.3	6	mV
			●		0.6	6	mV
	LT1086-3.3	4.5V ≤ V_{IN} ≤ 18V, I_{OUT} = 0mA, T_J = 25°C			0.5	10	mV
			●		1.0	10	mV
	LT1086-3.6	4.75V ≤ V_{IN} ≤ 18V, I_{OUT} = 0mA, T_J = 25°C			0.5	10	mV
			●		1.0	10	mV
	LT1086-5	I_{OUT} = 0mA, T_J = 25°C, 6.5V ≤ V_{IN} ≤ 20V			0.5	10	mV
			●		1.0	10	mV
	LT1086-12	I_{OUT} = 0mA, T_J = 25°C, 13.5V ≤ V_{IN} ≤ 25V			1.0	25	mV
			●		2.0	25	mV
Load Regulation	LT1086, LT1086H	($V_{IN} - V_{OUT}$) = 3V, 10mA ≤ I_{OUT} ≤ 1.5A, (0.5A for LT1086H) T_J = 25°C (Notes 1, 2)			0.1	0.3	%
			●		0.2	0.4	%
	LT1086-2.85	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 1.5A, T_J = 25°C (Notes 1, 2)			3	12	mV
			●		6	20	mV
	LT1086-3.3	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 1.5A, T_J = 25°C (Notes 1, 2)			3	15	mV
			●		7	25	mV
	LT1086-3.6	V_{IN} = 5.25V, 0 ≤ I_{OUT} ≤ 1.5A, T_J = 25°C (Notes 1, 2)			3	15	mV
			●		6	25	mV
		V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 1A, T_J = 25°C			2	15	mV
			●		4	25	mV
	LT1086-5	V_{IN} = 8V, 0 ≤ I_{OUT} ≤ 1.5A, T_J = 25°C (Notes 1, 2)			5	20	mV
			●		10	35	mV
	LT1086-12	V_{IN} = 15V, 0 ≤ I_{OUT} ≤ 1.5A, T_J = 25°C (Notes 1, 2)			12	36	mV
			●		24	72	mV
Dropout Voltage ($V_{IN} - V_{OUT}$)	LT1086/-2.85/-3.3/-3.6/-5/-12	ΔV_{OUT}, ΔV_{REF} = 1%, I_{OUT} = 1.5A (Note 3)	●		1.3	1.5	V
	LT1086H	ΔV_{REF} = 1%, I_{OUT} = 0.5A (Note 3)	●		0.95	1.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Current Limit	LT1086/-2.85/-3.3/-3.6/-5/-12	$(V_{IN} - V_{OUT}) = 5V$	●	1.50	2.00	2.8	A
		$(V_{IN} - V_{OUT}) = 25V$	●	0.05	0.15		A
	LT1086H	$(V_{IN} - V_{OUT}) = 5V$	●	0.50	0.700	1.2	A
		$(V_{IN} - V_{OUT}) = 25V$	●	0.02	0.075		A
Minimum Load Current	LT1086/LT1086H	$(V_{IN} - V_{OUT}) = 25V$ (Note 4)	●		5	10	mA
Quiescient Current	LT1086-2.85	$V_{IN} \leq 18V$	●		5	10	mA
	LT1086-3.3	$V_{IN} \leq 18V$	●		5	10	mA
	LT1086-3.6	$V_{IN} \leq 18V$	●		5	10	mA
	LT1086-5	$V_{IN} \leq 20V$	●		5	10	mA
	LT1086-12	$V_{IN} \leq 25V$	●		5	10	mA
Thermal Regulation	$T_A = 25°C$, 30ms pulse				0.008	0.04	%/W
Ripple Rejection	f = 120Hz, $C_{OUT} = 25\mu F$ Tantalum, $I_{OUT} = 1.5A$, ($I_{OUT} = 0.5A$ for LT1086H)						
	LT1086, LT1086H	$C_{ADJ} = 25\mu F$, $(V_{IN} - V_{OUT}) = 3V$	●	60	75		dB
	LT1086-2.85	$V_{IN} = 6V$	●	60	72		dB
	LT1086-3.3	$V_{IN} = 6.3V$	●	60	72		dB
	LT1086-3.6	$V_{IN} = 6.6V$	●	60	72		dB
	LT1086-5	$V_{IN} = 8V$	●	60	68		dB
	LT1083-12	$V_{IN} = 15V$	●	54	60		dB
Adjust Pin Current	LT1086, LT1086H	$T_J = 25°C$			55		µA
			●			120	µA
Adjust Pin Current Change	LT1086, LT1086H	$10mA \leq I_{OUT} \leq 1.5A$, (0.5A for LT1086H)					µA
		$1.5V \leq (V_{IN} - V_{OUT}) \leq 15V$	●		0.2	5	
Temperature Stability			●		0.5		%
Long Term Stability	$T_A = 125°C$, 1000 Hrs.				0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz = \leq f \leq 10kHz$				0.003		%
Thermal Resistance Junction-to-Case	H Package: Control Circuitry/Power Transistor					15/20	°C/W
	K Package: Control Circuitry/Power Transistor					1.7/4.0	°C/W
	M Package: Control Circuitry/Power Transistor					1.5/4.0	°C/W
	T Package: Control Circuitry/Power Transistor					1.5/4.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Line and load regulation are measured at a constant junction temperature by low duty cycle pulse testing. Load regulation is measured at the output lead ≈1/8" from the package.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation of 15W (3W for the LT1086H). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output range. See Short-Circuit Current curve for available output current.

Note 3: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

Note 4: Minimum load current is defined as the minimum output current required to maintain regulation. At 25V input/output differential the device is guaranteed to regulate if the output current is greater than 10mA.

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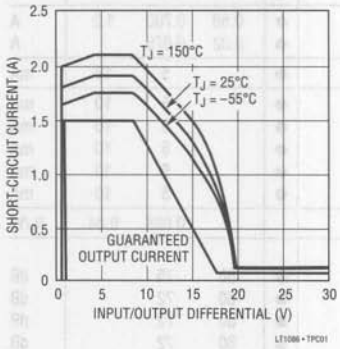
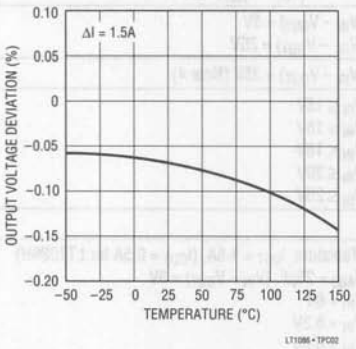
TYPICAL PERFORMANCE CHARACTERISTICS

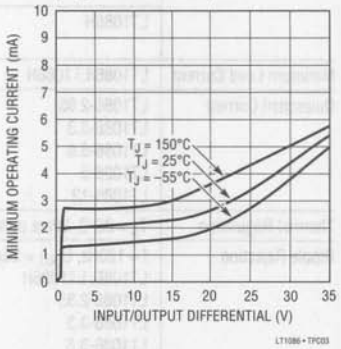
LT1086 Short-Circuit Current



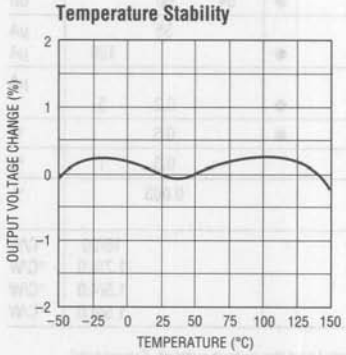
LT1086 Load Regulation



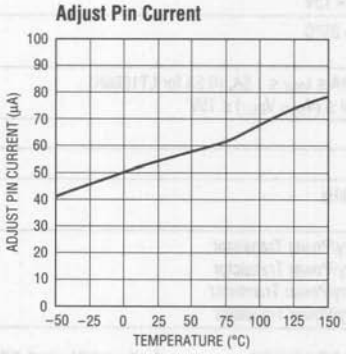
Minimum Operating Current (Adjustable Device)



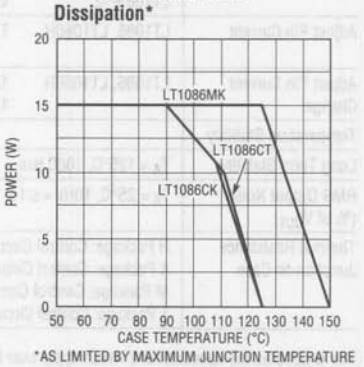
Temperature Stability



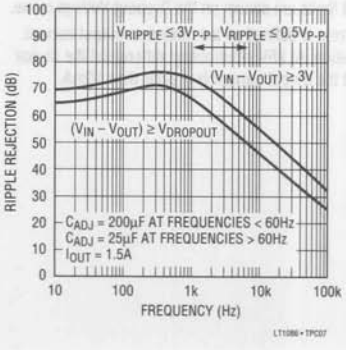
Adjust Pin Current



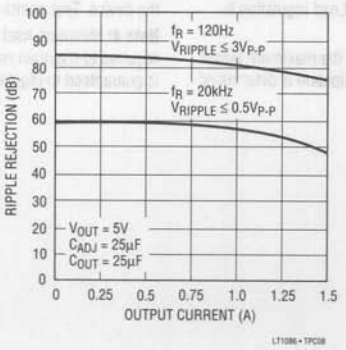
LT1086 Maximum Power Dissipation*



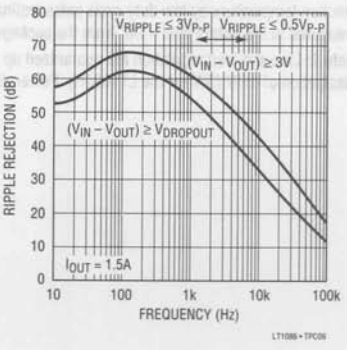
LT1086 Ripple Rejection



LT1086 Ripple Rejection vs Current

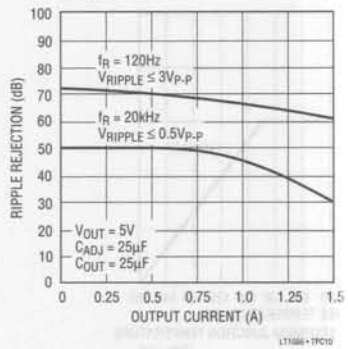


LT1086-5 Ripple Rejection

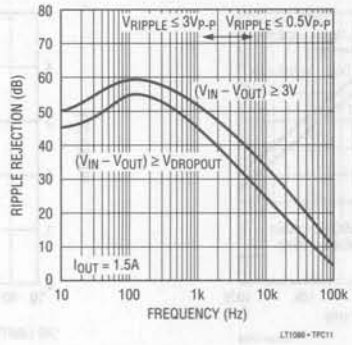


TYPICAL PERFORMANCE CHARACTERISTICS

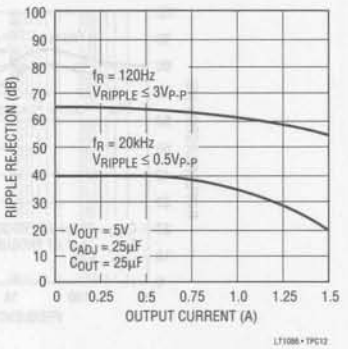
LT1086-5 Ripple Rejection vs Current



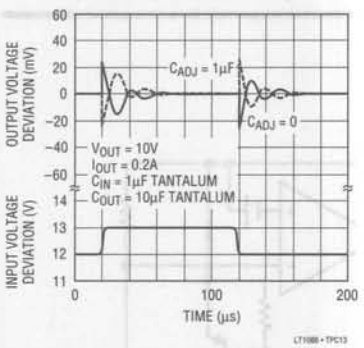
LT1086-12 Ripple Rejection



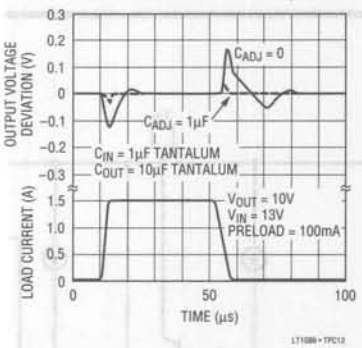
LT1086-12 Ripple Rejection vs Current



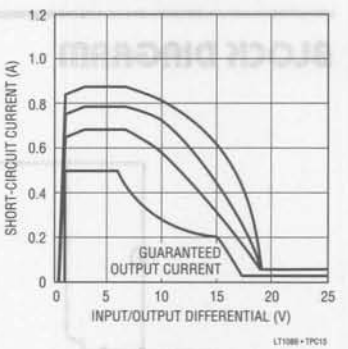
LT1086 Line Transient Response



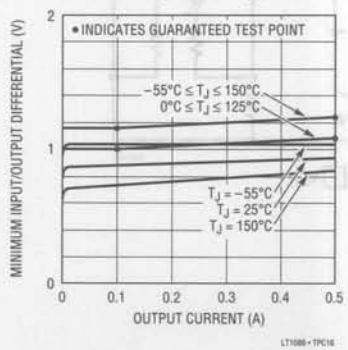
LT1086 Load Transient Response



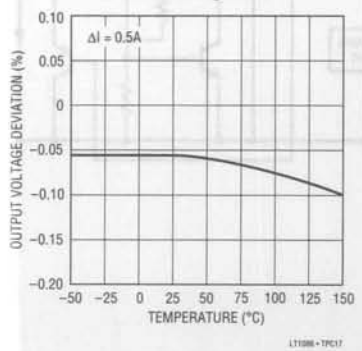
LT1086H Short-Circuit Current



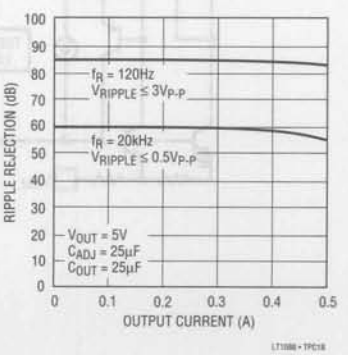
LT1086H Dropout Voltage



LT1086H Load Regulation



LT1086H Ripple Rejection vs Current



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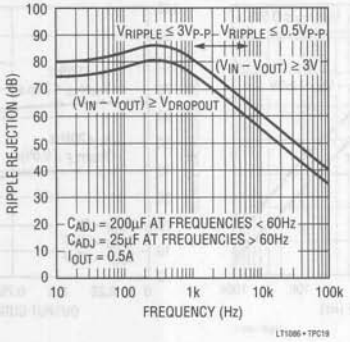
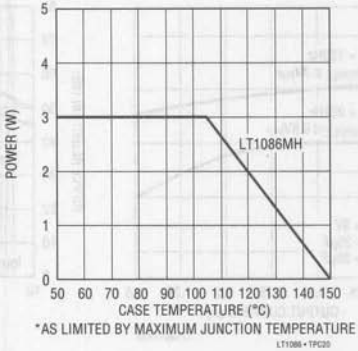
TYPICAL PERFORMANCE CHARACTERISTICS

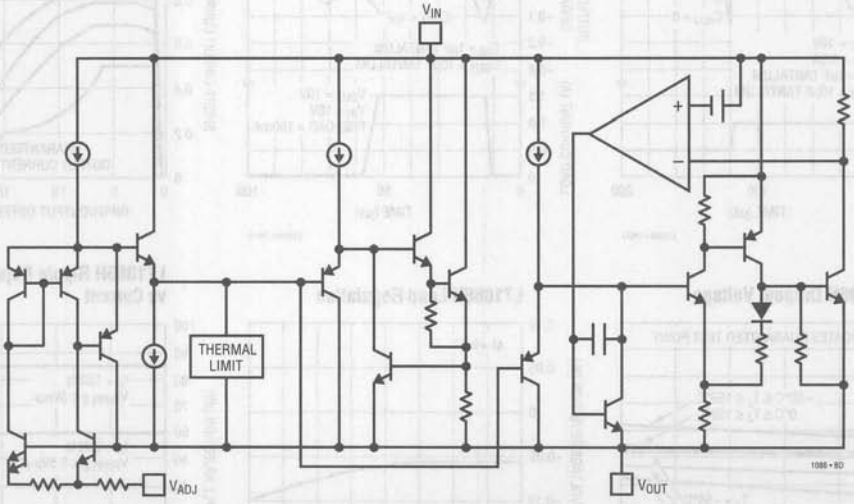
LT1086H Ripple Rejection



LT1086H Maximum Power Dissipation*



BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT1086 family of three-terminal regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short-circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C at the sense point.

These regulators are pin compatible with older three-terminal adjustable devices, offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1086 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1086 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150µF aluminum electrolytic or a 22µF solid tantalum on the output will ensure stability. Normally capacitors much smaller than this can be used with the LT1086. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150µF or 22µF values given will ensure stability.

When using the LT1086 the adjustment terminal can be bypassed to improve ripple rejection. When the adjustment terminal is bypassed the requirement for an output capacitor increases. The values of 22µF tantalum or 150µF aluminum cover all cases of bypassing the adjustment terminal. For fixed voltage devices or adjustable devices without an adjust pin bypass capacitor, smaller output capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

INPUT	OUTPUT	ADJUSTMENT
10µF	10µF Tantalum, 50µF Aluminum	None
10µF	22µF Tantalum, 150µF Aluminum	20µF

Normally, capacitor values on the order of 100µF are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1086 regulators.

Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negitive resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1086 series and has been present on all power IC regulators. The value of negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

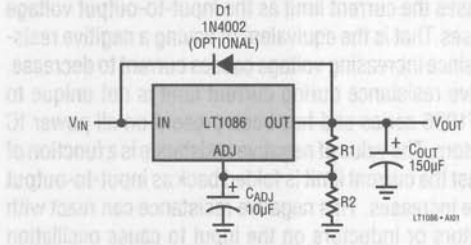
In normal operation the LT1086 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1086 adjustment pin are limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short-circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1086 family can handle microsecond surge currents of 10A to 20A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with high value output capacitors such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1086 can generate those kinds of currents and a diode from output to input is then recommended. Normal power supply cycling or even

APPLICATIONS INFORMATION

plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ±25V, with respect to the output without any device degradation. Of course as with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1086 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1086 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators such as the 7800 series also exhibited this phenomenon, so it is not unique to the LT1086.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens there are two stable output operating points for the regulator. With this double intersection the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

For the LT1086 the typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor at the ripple frequency should equal the value of R1, (normally 100Ω to 120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 13µF if R1 = 100Ω. At 10kHz only 0.16µF is needed.

For circuits without an adjust pin bypass capacitor the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or four times larger. Ripple rejection will be degraded by 12dB from the value shown on the LT1086 curve. Typical curves are provided for the 5V and 12V devices since the adjust pin is not available.

Output Voltage

The LT1086 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor R1 between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is chosen to be the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. For fixed voltage devices R1 and R2 are included in the device.

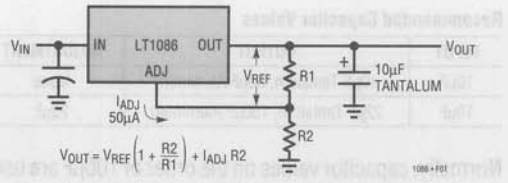


Figure 1. Basic Adjustable Regulator

APPLICATIONS INFORMATION

Load Regulation

Because the LT1086 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider R1 is connected *directly* to the case *not to the load*. This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_P \times \frac{R2 + R1}{R1},\ R_P = \text{Parasitic Line Resistance}$$

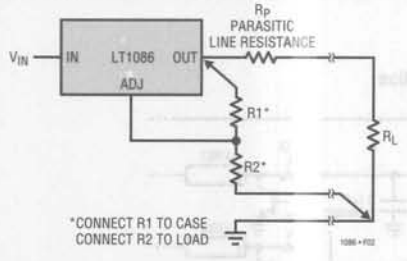


Figure 2. Connections for Best Load Regulation

Connected as shown R_P is not multiplied by the divider ratio. R_P is about 0.004Ω per foot using 16-gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible and use large wire or PC board traces.

Note that the resistance of the package leads for the H package ≈0.06Ω/in. While it is usually not possible to connect the load directly to the package, it is possible to connect larger wire or PC traces close to the case to avoid voltage drops that will degrade load regulation.

For fixed voltage devices the top of R1 is internally Kelvin connected and the ground pin can be used for negative side sensing.

Thermal Considerations

The LT1086 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction-to-case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

For example, using a LT1086CK (TO-3, Commercial) and assuming:

V_{IN}(max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 1A,
T_A = 75°C, $\theta_{HEAT\ SINK}$ = 3°C/W,
$\theta_{CASE\text{-}TO\text{-}HEAT\ SINK}$ = 0.2°C/W for K package with thermal compound.

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT})\ (I_{OUT}) = 4W$$

Junction temperature will be equal to:

$$T_J = T_A + P_D\ (\theta_{HEAT\ SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\ SINK} + \theta_{JC})$$

For the Control Section:

T_J = 75°C + 4W (3°C/W + 0.2°C/W + 0.7°C/W) = 95°C
95°C < 125°C = T_{JMAX} (Control Section Commercial Range)

For the Power Transistor:

T_J = 75°C + 4W (3°C/W + 0.2°C/W + 4°C/W) = 103.8°C
103.8°C < 150°C = T_{JMAX} (Power Transistor Commercial Range)

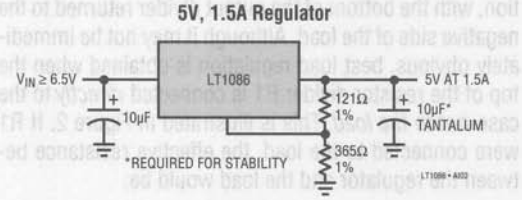
4

APPLICATIONS INFORMATION

In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

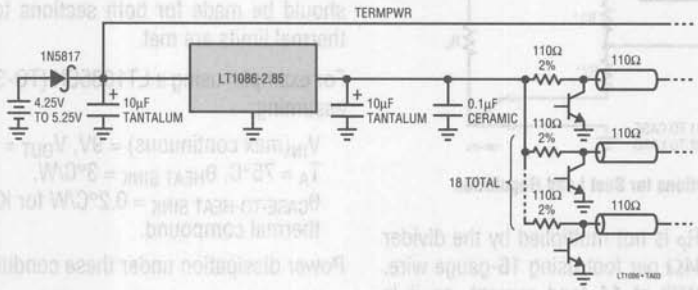
Junction-to-case thermal resistance for the K and T packages is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. While this is also the lowest resistance path for the H package, most available heat sinks for this package are of the clip-on type that attach to the cap of the package. The data sheet specification for thermal resistance for the H package is therefore written to reflect this. In all cases proper mounting is required to ensure the best possible heat flow from the die to the heat sink. Thermal compound at the case-to-heat sink interface is strongly recommended. In the case of the H package, mounting the device so that heat can flow out the bottom of the case will significantly lower thermal resistance (≈ a factor of 2). If the case of the device must be electrically isolated, a thermally conductive spacer can be used as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

5V, 1.5A Regulator

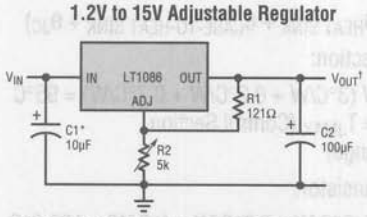


TYPICAL APPLICATIONS

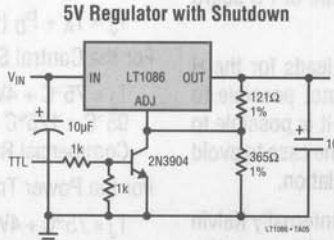
SCSI-2 Active Termination



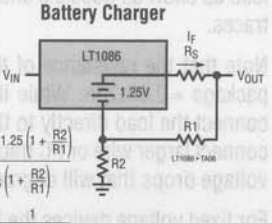
1.2V to 15V Adjustable Regulator



5V Regulator with Shutdown

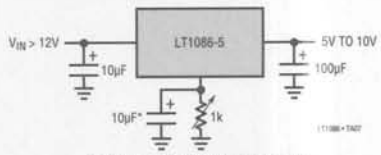


Battery Charger



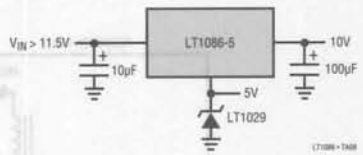
TYPICAL APPLICATIONS

Adjusting Output Voltage of Fixed Regulators

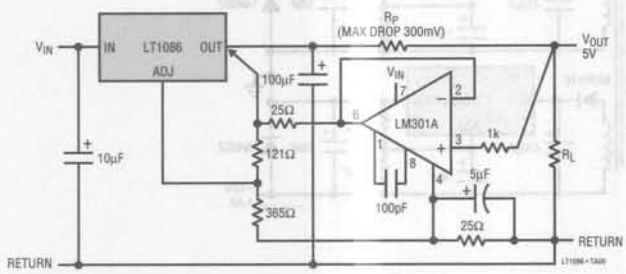


*OPTIONAL IMPROVES RIPPLE REJECTION

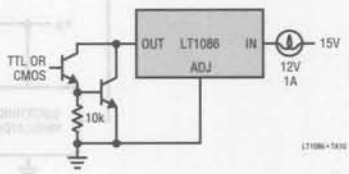
Regulator with Reference



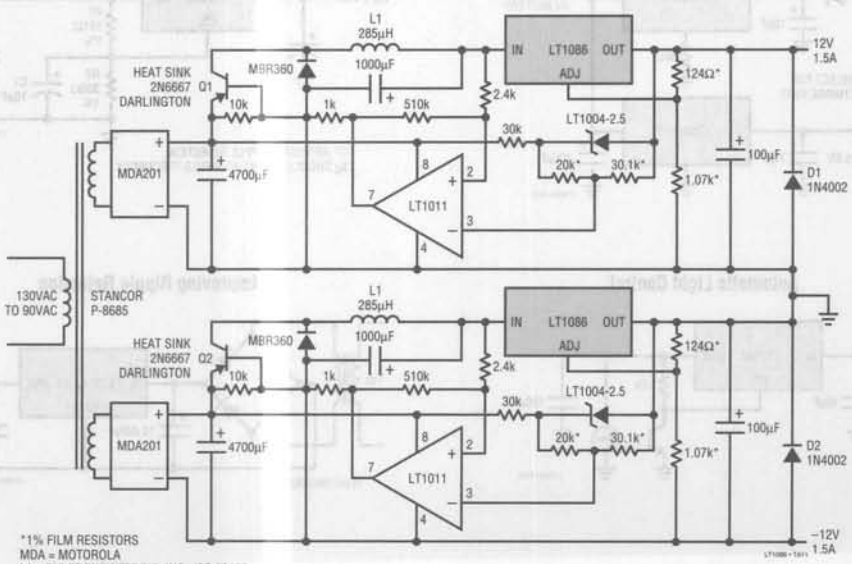
Remote Sensing



Protected High Current Lamp Driver



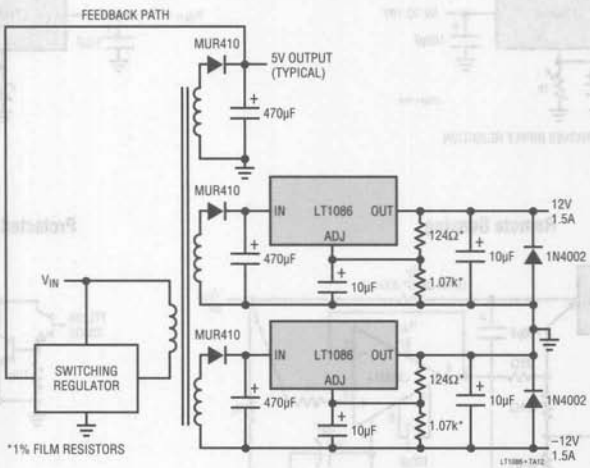
High Efficiency Dual Linear Supply



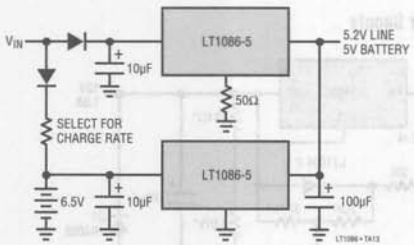
*1% FILM RESISTORS
MDA = MOTOROLA
L1 = PULSE ENGINEERING, INC. #PE-92106

TYPICAL APPLICATIONS

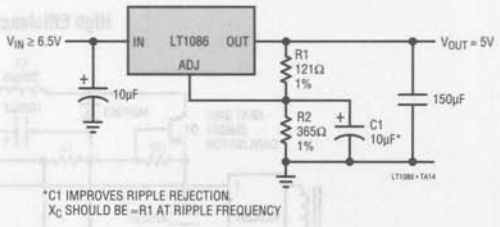
High Efficiency Dual Supply



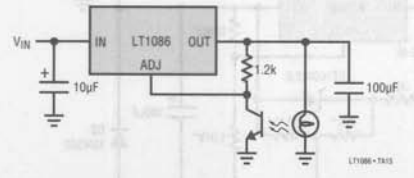
Battery Backed Up Regulated Supply



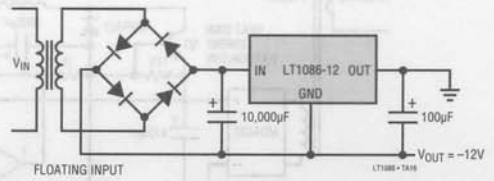
Improving Ripple Rejection



Automatic Light Control



Improving Ripple Rejection



800mA Low Dropout Positive Regulators Adjustable and Fixed 2.85V, 3.3V, 5V

FEATURES

- Space Saving SOT-223 Surface Mount Package
- Three-Terminal Adjustable or Fixed 2.85V, 3.3V, 5V
- Output Current of 800mA
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.2% Line Regulation Max
- 0.4% Load Regulation Max

APPLICATIONS

- Active SCSI Terminators
- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Battery Chargers
- 5V to 3.3V Linear Regulators

DESCRIPTION

The LT1117 is a positive low dropout regulator designed to provide up to 800mA of output current. The device is available in an adjustable version and fixed output voltages of 2.85V, 3.3V and 5V. The 2.85V version is designed specifically to be used in Active Terminators for the SCSI bus. All internal circuitry is designed to operate down to 1V input to output differential. Dropout voltage is guaranteed at a maximum of 1.2V at 800mA, decreasing at lower load currents. On chip trimming adjusts the reference/output voltage to within ± 1%. Current limit is also trimmed in order to minimize the stress on both the regulator and the power source circuitry under overload conditions.

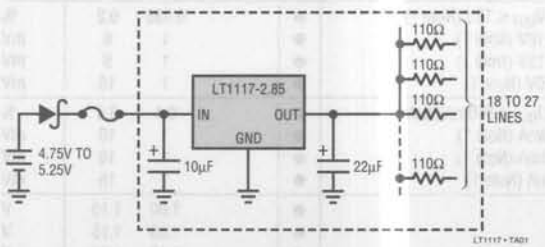
The low profile surface mount SOT-223 package allows the device to be used in applications where space is limited. The LT1117 requires a minimum of 10µF of output capacitance for stability. Output capacitors of this size or larger are normally included in most regulator designs.

Unlike PNP type regulators where up to 10% of the output current is wasted as quiescent current, the quiescent current of the LT1117 flows into the load, increasing efficiency.

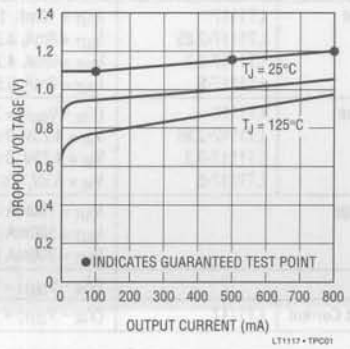
4

TYPICAL APPLICATION

Active Terminator for SCSI-2 Bus



Dropout Voltage (V_{IN} – V_{OUT})

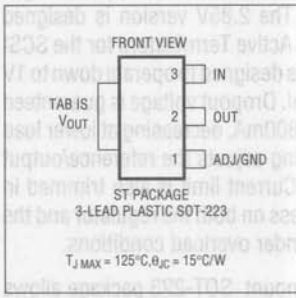


ABSOLUTE MAXIMUM RATINGS

Input Voltage
Operating Voltage
LT1117, LT1117-3.3, LT1117-5 ..... 15V
LT1117-2.85 ..... 10V
Surge Voltage
LT1117, LT1117-3.3, LT1117-5 ..... 20V

Operating JunctionTemperature Range ..... 0°C to 125°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature ..... (See Soldering Methods)

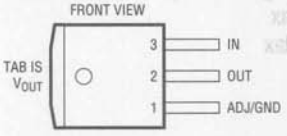
PACKAGE/ORDER INFORMATION



ST PACKAGE
3-LEAD PLASTIC SOT-223

$T_{J\,MAX}$ = 125°C, θ_{JC} = 15°C/W

ORDER PART NUMBER
LT1117CST
LT1117CST-2.85
LT1117CST-3.3
LT1117CST-5
PART MARKING
1117 11173
11172 11175



M PACKAGE
3-LEAD PLASTIC DD

$T_{J\,MAX}$ = 125°C, θ_{JC} = 10°C/W

ORDER PART NUMBER
LT1117CM
LT1117CM-2.85
LT1117CM-3.3
LT1117CM-5
PART MARKING
1117 11173
11172 11175

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	LT1117	I_{OUT} = 10mA, ($V_{IN} - V_{OUT}$) = 2V, T_J = 25°C		1.238	1.250	1.262	V
		10 ≤ I_{OUT} ≤ 800mA, 1.4V ≤ ($V_{IN} - V_{OUT}$) ≤ 10V	●	1.225	1.250	1.270	V
Output Voltage	LT1117-2.85	I_{OUT} = 10mA, V_{IN} = 4.85V, T_J = 25°C		2.820	2.850	2.880	V
		0 ≤ I_{OUT} ≤ 800mA, 4.25V ≤ V_{IN} ≤ 10V	●	2.790	2.850	2.910	V
		0 ≤ I_{OUT} ≤ 500mA, V_{IN} = 3.95V	●	2.790	2.850	2.910	V
	LT1117-3.3	I_{OUT} = 10mA, V_{IN} = 5V, T_J = 25°C		3.267	3.300	3.333	V
		0 ≤ I_{OUT} ≤ 800mA, 4.75V ≤ V_{IN} ≤ 10V	●	3.235	3.300	3.365	V
	LT1117-5	I_{OUT} = 10mA, V_{IN} = 7V, T_J = 25°C		4.950	5.000	5.050	V
		0 ≤ I_{OUT} ≤ 800mA, 6.50V ≤ V_{IN} ≤ 12V	●	4.900	5.000	5.100	V
Line Regulation	LT1117	I_{OUT} = 10mA, 1.5V ≤ $V_{IN} - V_{OUT}$ ≤ 15V (Note 1)	●		0.035	0.2	%
	LT1117-2.85	I_{OUT} = 0mA, 4.25V ≤ V_{IN} ≤ 10V (Note 1)	●		1	6	mV
	LT1117-3.3	I_{OUT} = 0mA, 4.75V ≤ V_{IN} ≤ 15V (Note 1)	●		1	6	mV
	LT1117-5	I_{OUT} = 0mA, 6.5V ≤ V_{IN} ≤ 15V (Note 1)	●		1	10	mV
Load Regulation	LT1117	($V_{IN} - V_{OUT}$) = 3V, 10mA ≤ I_{OUT} ≤ 800mA (Note 1)	●		0.1	0.4	%
	LT1117-2.85	V_{IN} = 4.25V, 0 ≤ I_{OUT} ≤ 800mA (Note 1)	●		1	10	mV
	LT1117-3.3	V_{IN} = 4.75V, 0 ≤ I_{OUT} ≤ 800mA (Note 1)	●		1	10	mV
	LT1117-5	V_{IN} = 6.5V, 0 ≤ I_{OUT} ≤ 800mA (Note 1)	●		1	15	mV
Dropout Voltage		I_{OUT} = 100mA (Note 2)	●		1.00	1.10	V
		I_{OUT} = 500mA (Note 2)	●		1.05	1.15	V
		I_{OUT} = 800mA (Note 2)	●		1.10	1.20	V
Current Limit		($V_{IN} - V_{OUT}$) = 5V, T_J = 25°C,		800	950	1200	mA
Minimum Load Current	LT1117	($V_{IN} - V_{OUT}$) = 15V (Note 3)	●		1.7	5	mA

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current	LT1117-2.85	$V_{IN} \leq 10V$	●		5	10	mA
	LT1117-3.3	$V_{IN} \leq 15V$	●		5	10	mA
	LT1117-5	$V_{IN} \leq 15V$	●		5	10	mA
Thermal Regulation		$T_A = 25°C$, 30ms Pulse			0.01	0.1	%/W
Ripple Rejection		$f_{RIPPLE} = 120Hz$, $(V_{IN} - V_{OUT}) = 3V$, $V_{RIPPLE} = 1Vp\text{-}p$	●	60	75		dB
Adjust Pin Current			●		55	120	µA
Adjust Pin Current Change		$10mA \leq I_{OUT} \leq 800mA$, $1.4V \leq (V_{IN} - V_{OUT}) \leq 10V$	●		0.2	5	µA
Temperature Stability					0.5		%
Long Term Stability		$T_A = 125°C$, 1000Hrs			0.3		%
RMS Output Noise		(% of V_{OUT}), $10Hz \leq f \leq 10kHz$			0.003		%
Thermal Resistance		(Junction-to-Case, at Tab)			15		°C/W

The ● denotes specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specification for changes in output voltage due to heating effects. Load regulation and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

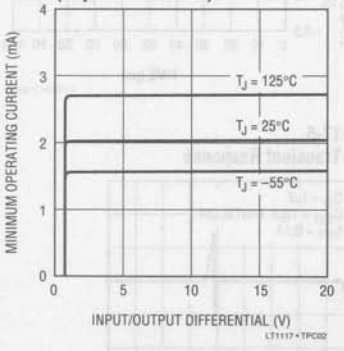
Note 2: Dropout voltage is specified over the full output current range of the device. Dropout voltage is defined as the minimum input/output differential measured at the specified output current. Test points and limits are also shown on the Dropout Voltage curve.

Note 3: Minimum load current is defined as the minimum output current required to maintain regulation.

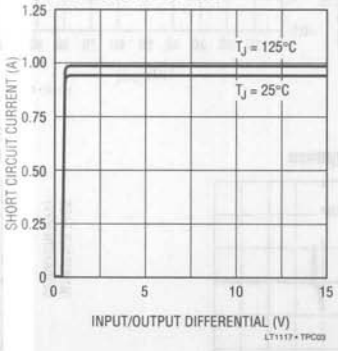
4

TYPICAL PERFORMANCE CHARACTERISTICS

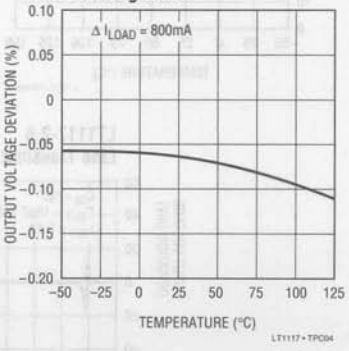
Minimum Operating Current (Adjustable Device)



Short-Circuit Current

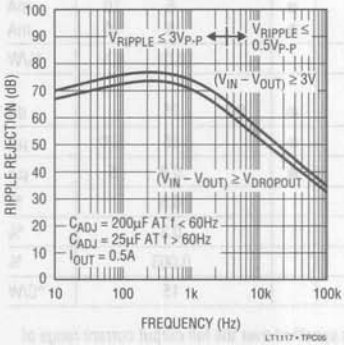


Load Regulation

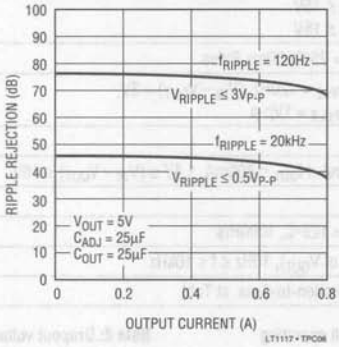


TYPICAL PERFORMANCE CHARACTERISTICS

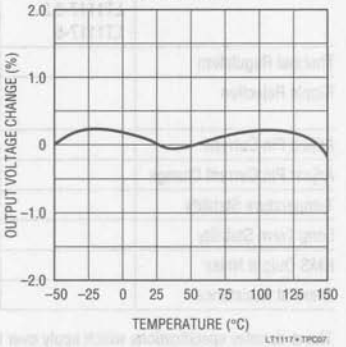
LT1117 Ripple Rejection



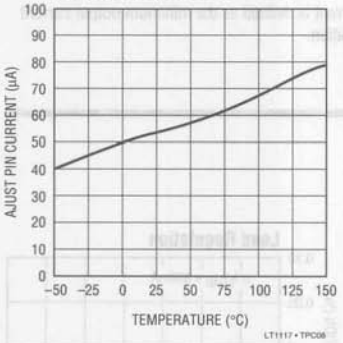
LT1117 Ripple Rejection vs Current



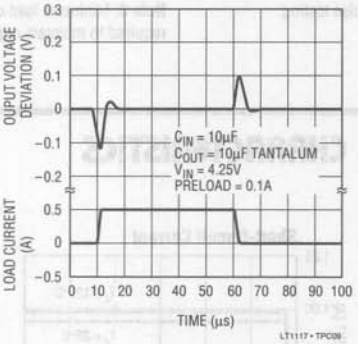
Temperature Stability



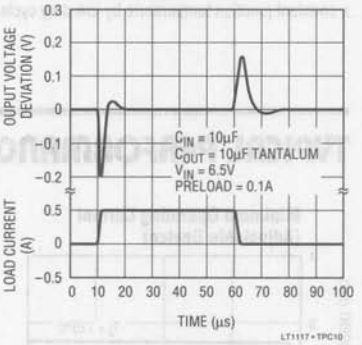
Adjust Pin Current



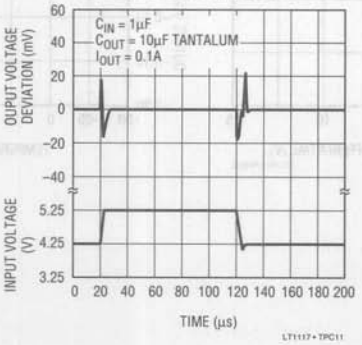
LT1117-2.85
Load Transient Response



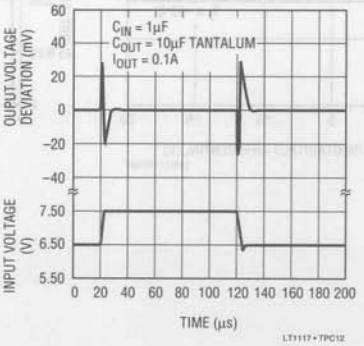
LT1117-5
Load Transient Response



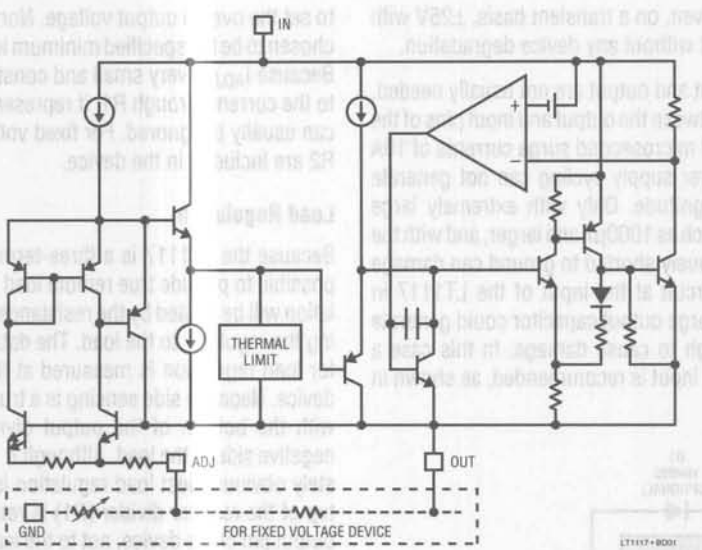
LT1117-2.8
Line Transient Response



LT1117-5
Line Transient Response



BLOCK DIAGRAM



APPLICATION HINTS

The LT1117 family of three-terminal regulators are easy to use. They are protected against short circuit and thermal overloads. Thermal protection circuitry will shutdown the regulator should the junction temperature exceed 165°C at the sense point. These regulators are pin compatible with older three-terminal adjustable regulators, offer lower dropout voltage and more precise reference tolerance. Reference stability over temperature is improved over older types of regulators.

Stability

The LT1117 family of regulators requires an output capacitor as part of the device frequency compensation. A minimum of 10µF of tantalum or 50µF of aluminum electrolytic is required. The ESR of the output capacitor should be less than 0.5Ω. Surface mount tantalum capacitors, which have very low ESR, are available from several manufacturers.

When using the LT1117 adjustable device the adjust terminal can be bypassed to improve ripple rejection. When the adjust terminal is bypassed the required value of the output capacitor increases. The device will require an output capacitor of 22µF tantalum or 150µF aluminum electrolytic when the adjust pin is bypassed.

Normally, capacitor values on the order of 100µF are used in the output of many regulators to ensure good load transient response with large load current changes. Output capacitance can be increased without limit and larger values of output capacitance further improve stability and transient response.

Protection Diodes

In normal operation, the LT1117 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjust pin and the output and between the output and input to prevent over stressing the die. The internal current paths on the LT1117 adjust pin are limited by internal resistors. Therefore, even with capacitors on the adjust pin, no protection diode is needed to ensure device safety under short circuit conditions. The

APPLICATION HINTS

adjust pin can be driven, on a transient basis, ±25V with respect to the output without any device degradation.

Diodes between input and output are not usually needed. The internal diode between the output and input pins of the device can withstand microsecond surge currents of 10A to 20A. Normal power supply cycling can not generate currents of this magnitude. Only with extremely large output capacitors, such as 1000µF and larger, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input of the LT1117 in combination with a large output capacitor could generate currents large enough to cause damage. In this case a diode from output to input is recommended, as shown in Figure 1.

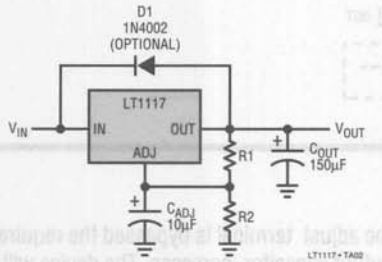


Figure 1.

Output Voltage

The LT1117 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 2). By placing a resistor between these two terminals, a constant current is caused to flow through R1 and down through R2

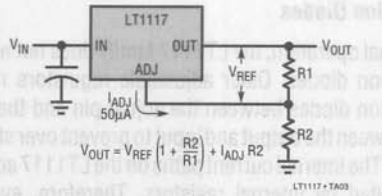


Figure 2. Basic Adjustable Regulator

to set the overall output voltage. Normally this current is chosen to be the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared to the current through R1, it represents a small error and can usually be ignored. For fixed voltage devices R1 and R2 are included in the device.

Load Regulation

Because the LT1117 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the output pin of the device. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R1) is returned directly to the output pin of the device, not to the load. This is illustrated in Figure 3. Connected as shown, R_P is not multiplied by the divider ratio. If R1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_P \times \frac{R2+R1}{R1}, R_P = \text{Parasitic Line Resistance}$$

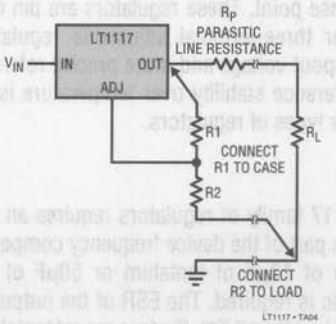


Figure 3. Connections for Best Load Regulation

For fixed voltage devices the top of R1 is internally Kelvin connected, and the ground pin can be used for negative side sensing.

APPLICATION HINTS

Thermal Considerations

LT1117 series regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous normal load conditions however, the maximum junction temperature rating of 125°C must not be exceeded.

It is important to give careful consideration to all sources of thermal resistance from junction to ambient. For the SOT-223 package, which is designed to be surface mounted, additional heat sources mounted near the device must also be considered. Heat sinking is accomplished using the heat spreading capability of the PC board and its copper traces. The thermal resistance of the LT1117 is 15°C/W from the junction to the tab. Thermal resistances from tab to ambient can be as low as 30°C/W. The total thermal resistance from junction to ambient can be as low as 45°C/W. This requires a reasonable sized PC board with at least one layer of copper to spread the heat across the board and couple it into the surrounding air.

Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the Length/Area ratio of the thermal resistor between layers is small. The data in Table 1 was taken using 1/16" FR-4 board with 1oz. copper foil. It can be used as a rough guideline in estimating thermal resistance.

Table 1.

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 Sq. mm	2500 Sq. mm	2500 Sq. mm	45°C/W
1000 Sq. mm	2500 Sq. mm	2500 Sq. mm	45°C/W
225 Sq. mm	2500 Sq. mm	2500 Sq. mm	53°C/W
100 Sq. mm	2500 Sq. mm	2500 Sq. mm	59°C/W
1000 Sq. mm	1000 Sq. mm	1000 Sq. mm	52°C/W
1000 Sq. mm	0	1000 Sq. mm	55°C/W

* Tab of device attached to topside copper

The thermal resistance for each application will be affected by thermal interactions with other components on the board. Some experimentation will be necessary to determine the actual value.

The power dissipation of the LT1117 is equal to:

$$P_D = (V_{IN} - V_{OUT})(I_{OUT})$$

Maximum junction temperature will be equal to:

$T_J = T_{A(MAX)} + P_D$(Thermal Resistance (junction-to-ambient))

Maximum junction temperature must not exceed 125°C.

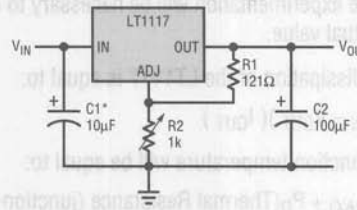
Ripple Rejection

The curves for Ripple Rejection were generated using an adjustable device with the adjust pin bypassed. These curves will hold true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency, should be < R1. R1 is normally in the range of 100Ω-200Ω. The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz, with R1=100Ω, the adjust pin capacitor should be > 13μF. At 10kHz only 0.16μF is needed.

For fixed voltage devices, and adjustable devices without an adjust pin capacitor, the output ripple will increase as the ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, the output ripple will be increased by the ratio of 5V/1.25V. It will increase by a factor of four. Ripple rejection will be degraded by 12dB from the value shown on the curve.

TYPICAL APPLICATIONS

1.2V to 10V Adjustable Regulator

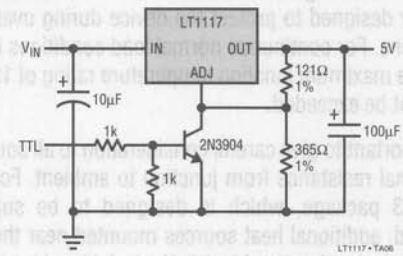


* NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

† $V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

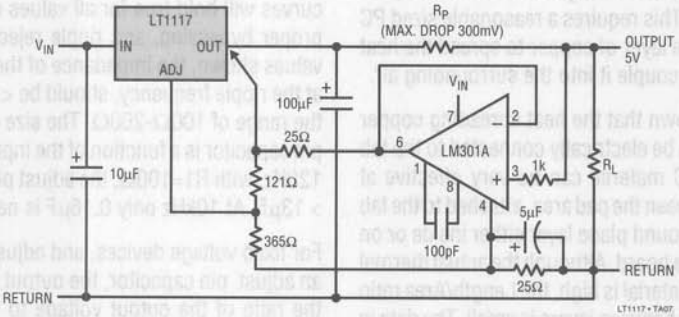
LT1117 • TA05

5V Regulator with Shutdown



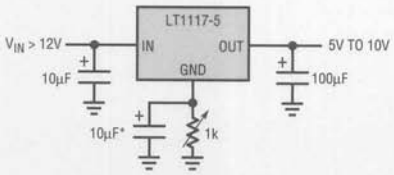
LT1117 • TA06

Remote Sensing



LT1117 • TA07

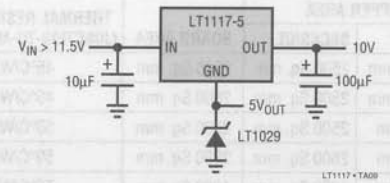
Adjusting Output Voltage of Fixed Regulators



* OPTIONAL IMPROVES RIPPLE REJECTION

LT1117 • TA08

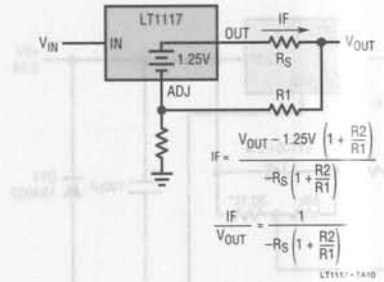
Regulator with Reference



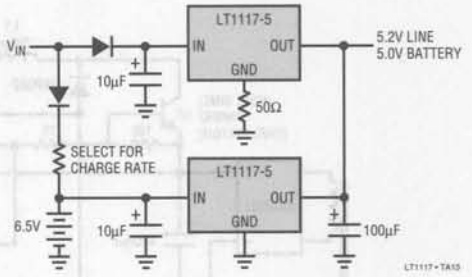
LT1117 • TA09

TYPICAL APPLICATIONS

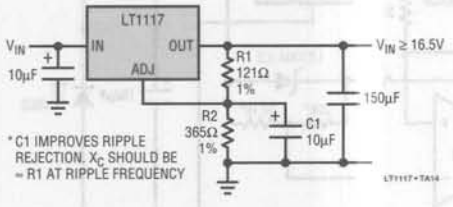
Battery Charger



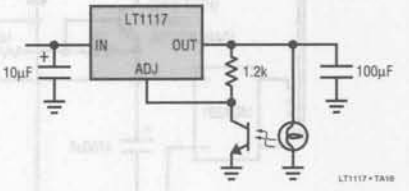
Battery Backed Up Regulated Supply



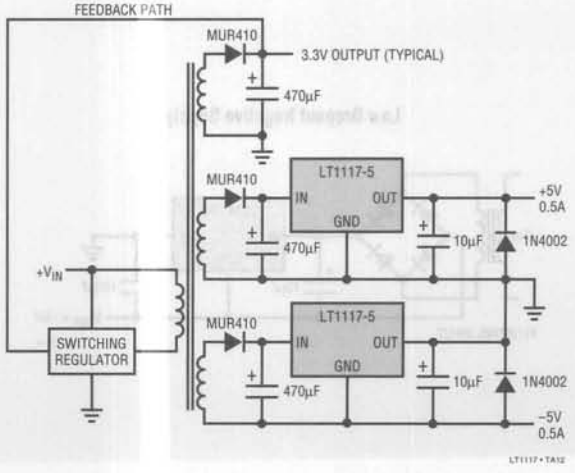
Improving Ripple Rejection



Automatic Light Control



High Efficiency Dual Supply



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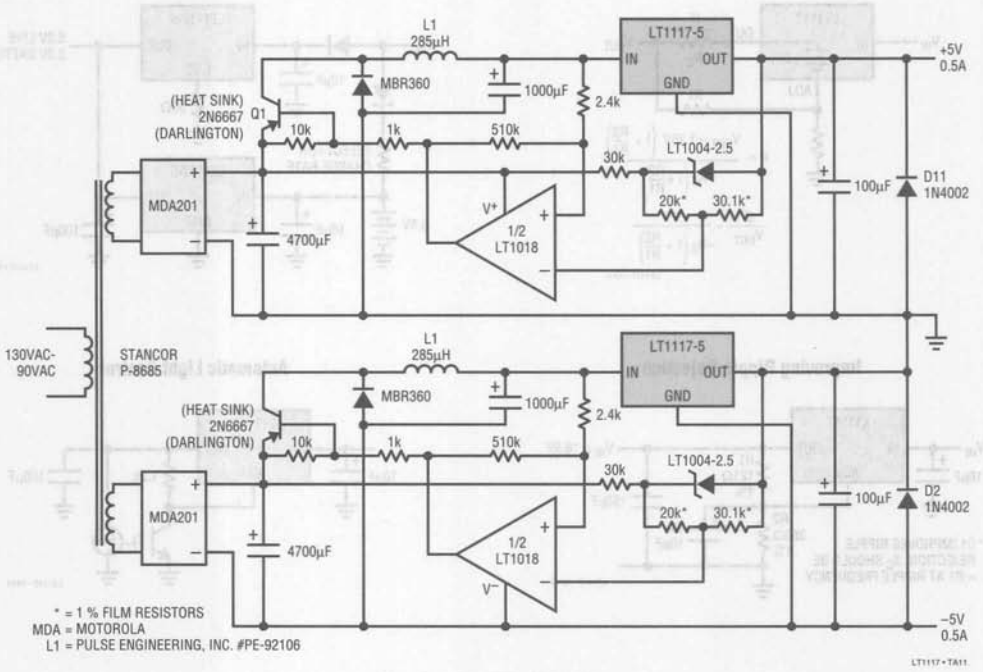
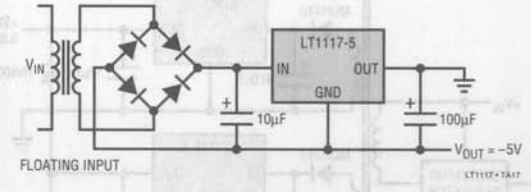
TYPICAL APPLICATIONS

High Efficiency Dual Linear Supply

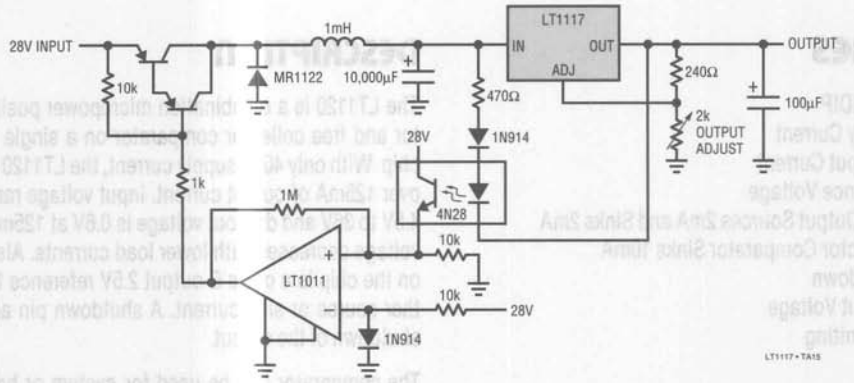


Low Dropout Negative Supply



TYPICAL APPLICATIONS

High Efficiency Regulator



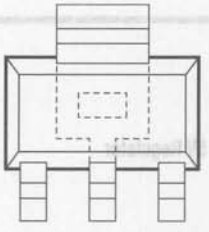
4

SOLDERING METHODS

The SOT-223 is manufactured with gull wing leadform for surface mount applications. The leads and heatsink are solder plated and allow easy soldering using non-active or mildly active fluxes. The package is constructed with three leads exiting one side of the package and one heatsink exiting the other side, and the die attached to the heatsink internally.

The recommended methods of soldering SOT-223 are: vapor phase reflow and infrared reflow with preheat of component to within 65°C of the solder temperature. Hand soldering and wave soldering are not recommended since these methods can easily damage the part with excessive thermal gradients across the package.

Care must be exercised during surface mount to minimize large (> 30°C per second) thermal shock to the package.



Micropower Regulator with Comparator and Shutdown

FEATURES

- 8-Lead MiniDIP
- 40μA Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 2mA and Sinks 2mA
- Open Collector Comparator Sinks 10mA
- Logic Shutdown
- 0.2V Dropout Voltage
- Thermal Limiting

APPLICATIONS

- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments
- Memory Keep Alive

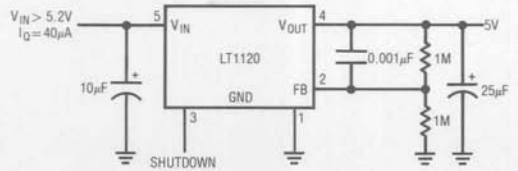
DESCRIPTION

The LT1120 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40μA supply current, the LT1120 can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A shutdown pin allows logic shutdown of the output.

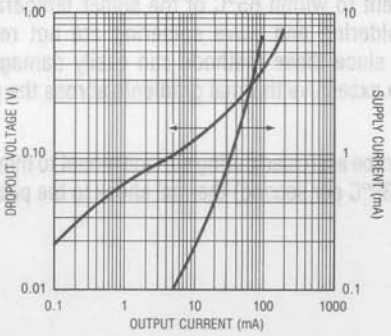
The comparator can be used for system or battery monitoring. For example, the comparator can be used to warn of low system voltage. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance.

The 2.5V reference will source or sink current. This allows it to be used as a supply splitter or auxiliary output.

5V Regulator



Dropout Voltage and Supply Current



ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
NPN Collector Voltage 36V
Output Short Circuit Duration ..... Indefinite
Power Dissipation ..... Internally Limited

Operating Temperature Range
LT1120C ..... 0°C to 100°C
Storage Temperature Range
LT1120C ..... –65°C to 150°C

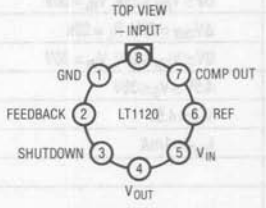
PACKAGE/ORDER INFORMATION

J8 PACKAGE
8-LEAD CERAMIC MINIDIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

N8 PACKAGE
8-LEAD PLASTIC MINIDIP
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

S8 PACKAGE
8-LEAD SURFACE MOUNT
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1120CJ8 LT1120CN8 LT1120CS8
S8 PART MARKING
1120



H PACKAGE
8-LEAD TO-5 METAL CAN
T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

ORDER PART NUMBER
LT1120CH

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_J = 25°C

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Voltage	$4.5V \le V_{IN} \le 36V$		2.46	2.50	2.54	V
Line Regulation	$4.5V \le V_{IN} \le 36V$			0.01	0.015	%/V
Load Regulation	$-2.0mA \le I_{REF} \le 2mA$, V_{IN} = 12V			0.3	0.6	%
Output Source Current	V_{IN} = 5V		2	4		mA
Output Sink Current	V_{IN} = 5V		2	4		mA
Temperature Stability				1		%
Regulator						
Supply Current	V_{IN} = 6V, $I_{OUT} \le 100\mu A$			45	80	μA
	V_{IN} = 36V, $I_{OUT} \le 100\mu A$			75	100	μA
	V_{IN} = 12V, I_{OUT} = 125mA			11	20	mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$		125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$			0.2	0.5	%
Line Regulation	$6V \le V_{IN} \le 36V$			0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$			0.02	0.05	V
	I_{OUT} = 125mA			0.4	0.65	V
Feedback Sense Voltage	V_{IN} = 12V		2.44	2.5	2.56	V
Shutdown Pin Voltage		Normal			0.4	V
	$V_{OUT} \le 0.5V$	Shutdown	2.2	1.4		V
Shutdown Pin Current	V_{IN} = 1.4V			25		μA

4

ELECTRICAL CHARACTERISTICS $T_J = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator					
Feedback Bias Current			15	40	nA
Minimum Load Current	$V_{IN} = 36V$		1	5	µA
Short Circuit Current	$V_{IN} = 36V$		300	400	mA
Comparator					
Offset Voltage	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$		3	7	mV
Bias Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$ (Note 1)		15	40	nA
Offset Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$		4	15	nA
Gain	$\Delta V_{OUT} = 29V$, $R_L = 20k$	2000	10000		V/V
Common Mode Rejection	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$	80	94		dB
Power Supply Rejection	$4.5V \le V_S \le 36V$	80	96		dB
Output Sink Current	$V_{IN} = 4.5V$	10	18		mA
Saturation Voltage	$I_{OUT} = 1mA$		0.4	0.6	V
Input Voltage Range		0		$V_{IN} - 1$	V
Response Time			5		µs
Leakage Current				2	µA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Voltage	$4.5V \le V_{IN} \le 36V$	●	2.40	2.50	2.55	V
Line Regulation	$4.5V \le V_{IN} \le 36V$	●		0.01	0.02	%/V
Load Regulation	$-2.0mA \le I_{REF} \le 2mA$, $V_{IN} = 12V$	●		0.4	0.8	%
Output Source Current	$V_{IN} = 5V$	●	2			mA
Output Sink Current	$V_{IN} = 5V$	●	2			mA
Regulator						
Supply Current	$V_{IN} = 6V$, $I_{OUT} \le 100µA$	●		65	95	µA
	$V_{IN} = 36V$, $I_{OUT} \le 100µA$	●		85	100	µA
	$V_{IN} = 12V$, $I_{OUT} = 125mA$	●		11	20	mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●			1	%
Line Regulation	$6V \le V_{IN} \le 36V$	●			0.02	%/V
Dropout Voltage	$I_{OUT} = 100µA$	●			0.06	V
	$I_{OUT} = 125mA$	●			0.85	V
Feedback Sense Voltage	$V_{IN} = 12V$	●	2.38	2.5	2.57	V
Feedback Bias Current		●			50	nA
Minimum Load Current	$V_{IN} = 36V$	●			50	µA
Short Circuit Current	$V_{IN} = 36V$	●		300	400	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Comparator						
Offset Voltage		●			10	mV
Bias Current	V_{IN} = 36V (Note 1)	●		15	60	nA
Gain	ΔV_{OUT} = 29V, R_L = 20k	●	1000			V/V
Output Sink Current	V_{IN} = 4.5V (Note 2)	●	5	10		mA
Leakage Current	V_{IN} = 36V	●			8	μA

The ● denotes specifications which apply over full operating temperature range.

Note 1: For $0V \leq V_{CM} \leq 0.1V$ and $T_A > 85°C$ I bias max is 100nA.

Note 2: For $T_A \leq -40°C$ output $I_{SINK\ (MIN)}$ to 2.5mA.

PIN FUNCTIONS

Pin 1—Ground.

Pin 2—Feedback. This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

Pin 3—Shutdown. A logic 1 shuts off main regulator. Caution: noise or leakage into the shutdown pin can affect output voltage.

Pin 4—Regulator Output. Main output, requires 10μF output capacitor. Can be shorted to V_{IN} or ground without damaging device.

Pin 5—Input Supply. Bypass with 10μF cap. Must always be more positive than ground.

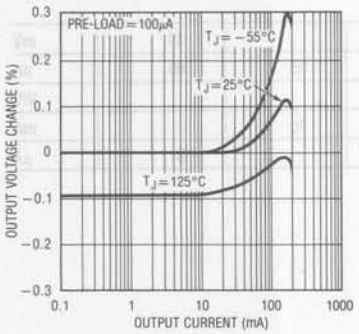
Pin 6—Reference. 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 7—Comparator Output. May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

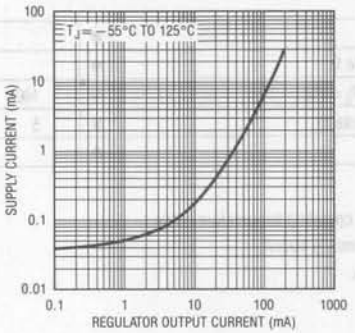
Pin 8—Comparator Input. Inverting comparator input.

TYPICAL PERFORMANCE CHARACTERISTICS

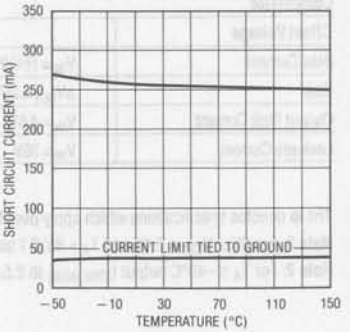
Regulator Load Regulation



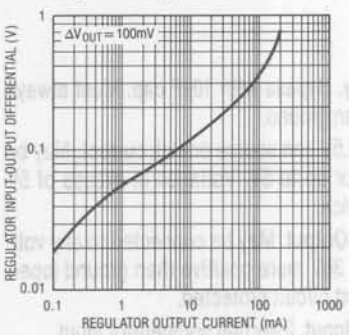
Supply Current



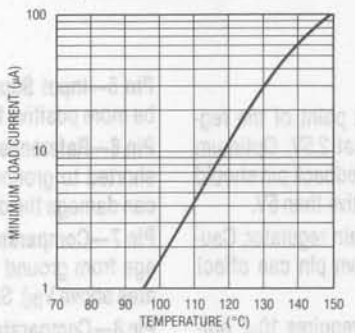
Regulator Short Circuit Current



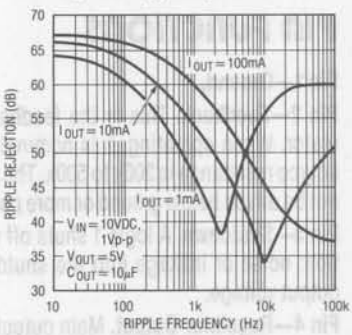
Dropout Voltage



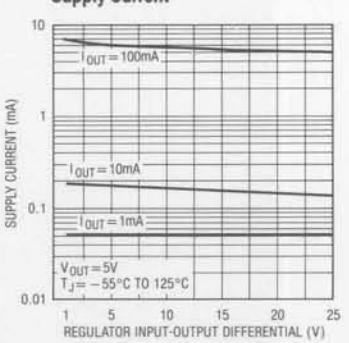
Regulator Minimum Load Current



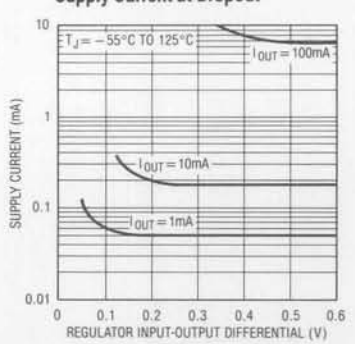
Regulator Ripple Rejection



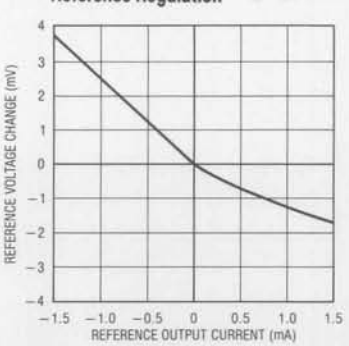
Supply Current



Supply Current at Dropout

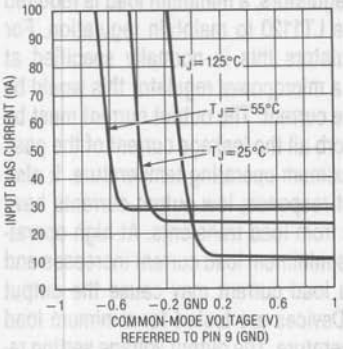


Reference Regulation

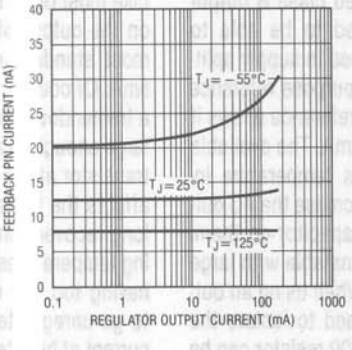


TYPICAL PERFORMANCE CHARACTERISTICS

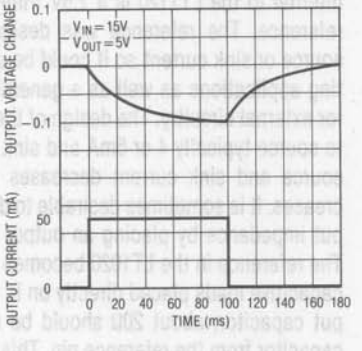
Comparator Input Bias Current



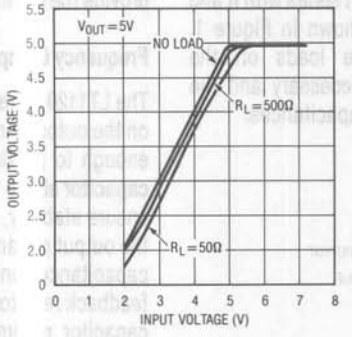
Feedback Pin Current



Regulator Thermal Regulation



LT1120 Turn-On Characteristic



APPLICATION HINTS

The LT1120 is especially suited for micropower system applications. For example, the comparator section of the LT1020 may be used as a battery checker to provide an indication of low battery. Another type of system application for the LT1120 would be to generate the equivalent of split supplies off of a single power input. The regulator section provides regulated output voltage and the reference, which can both source and sink current is then an artificial system ground providing a split supply for the system.

For many applications the comparator can be frequency compensated to operate as an amplifier. Compensation values for various gains are given in the datasheet. The comparator gain is purposely low to make it easier to frequency compensate as an amplifier. The NPN output is capable of sinking 10mA and can drive loads connected to voltages in excess of the positive power supply. This is useful for driving switches or linear regulators off of a higher input voltage.

4

APPLICATION HINTS

Reference

Internal to the LT1120 is a 2.5V trimmed class B output reference. The reference was designed to be able to source or sink current so it could be used in supply splitting applications as well as a general purpose reference for external circuitry. The design of the reference allows it to source typically 4 or 5mA and sink 2mA. The available source and sink current decreases as temperature increases. It is sometimes desirable to decrease the AC output impedance by placing an output capacitor on them. The reference in the LT1020 becomes unstable with large capacitive loads placed directly on it. When using an output capacitor, about 20Ω should be used to isolate the capacitor from the reference pin. This 20Ω resistor can be placed directly in series with the capacitor or alternatively the reference line can have 20Ω placed in series with it and then a capacitor to ground. This is shown in Figure 1. Other than placing large capacitive loads on the reference, no other precautions are necessary and the reference is stable with nominal stray capacitances.

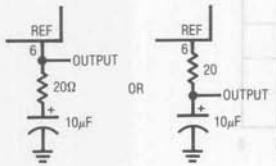


Figure 1. Bypassing Reference

Overload Protection

The main regulator in the LT1120 is current limited at approximately 250mA. The current limit is stable with both input voltage and temperature.

Like most other IC regulators, a minimum load is required on the output of the LT1120 to maintain regulation. For most standard regulators this is normally specified at 5mA. Of course, for a micropower regulator this would be a tremendously large current. The output current must be large enough to absorb all the leakage current of the pass transistor at the maximum operating temperature. It also affects the transient response; low output currents have long recovery times from load transients. At high operating temperatures the minimum load current increases and having too low of a load current may cause the output to go unregulated. Devices are tested for minimum load current at high temperature. The output voltage setting resistors to the feedback terminal can usually be used to provide the minimum load current.

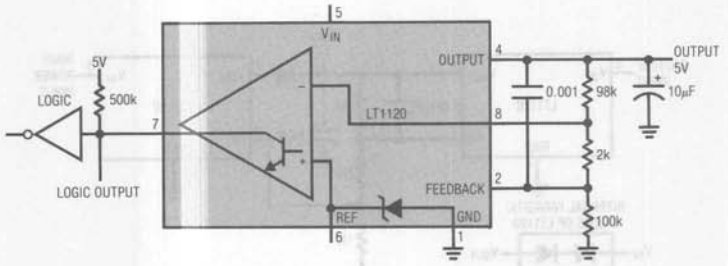
Frequency Compensation

The LT1120 is frequency compensated by a dominant pole on the output. An output capacitor of 10μF is usually large enough to provide good stability. **Increasing the output capacitor above 10μF further improves stability.** In order to ensure stability, a feedback capacitor is needed between the output pin and the feedback pin. This is because stray capacitance can form another pole with the large value of feedback resistors used with the LT1120. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

With the large dynamic operating range of the output current, 10000:1, frequency response changes widely. Low AC impedance capacitors are needed to insure stability. While solid tantalum are best, aluminum electrolytics can be used but larger capacitor values may be needed.

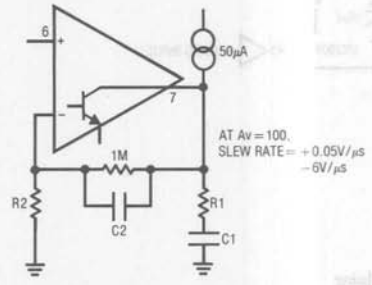
TYPICAL APPLICATIONS

Regulator with Output Voltage Monitor



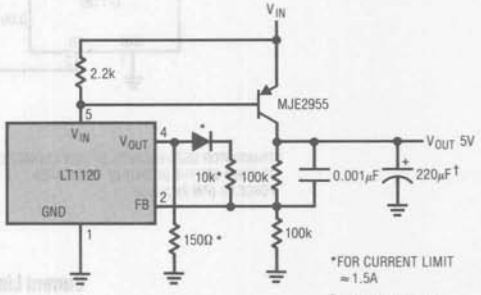
LOGIC OUTPUT GOES LOW WHEN V_{OUT} DROPS BY 100mV

Compensating the Comparator as an Op Amp



Av	R1	C1	C2	R2
1	33Ω	0.1µF	0.001µF	—
10	100Ω	0.047µF	—	100k
100	10k	0.002µF	—	10k

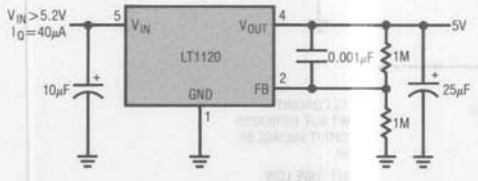
1 Amp Low Dropout Regulator



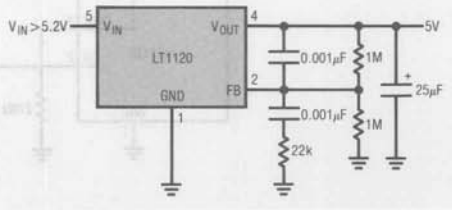
*FOR CURRENT LIMIT ≈ 1.5A

†MUST HAVE LOW ESR. SEVERAL 100µF CAPACITORS CAN BE PARALLELED.

5V Regulator

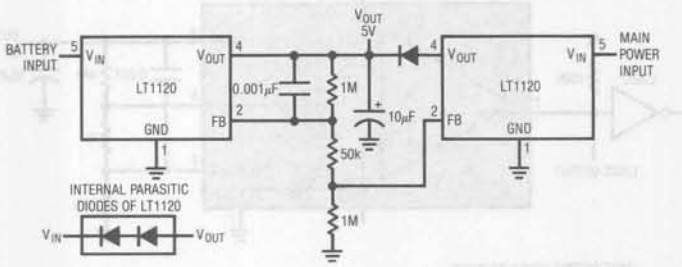


Regulator with Improved Transient Response

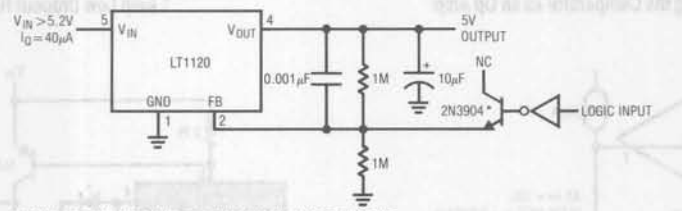


TYPICAL APPLICATIONS

Battery Backup Regulator

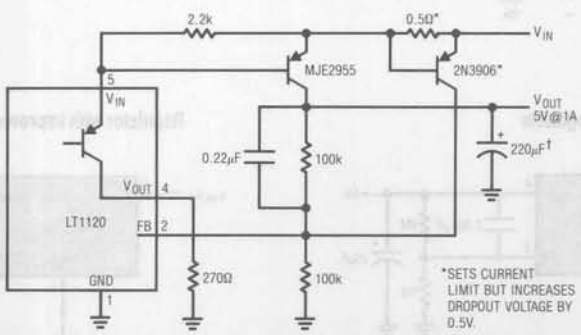


5V Regulator with Feedback Shutdown



*TRANSISTOR USED BECAUSE OF LOW LEAKAGE CHARACTERISTICS. TO TURN OFF THE OUTPUT OF THE LT1120 FORCE FB (PIN 2) >2.5V.

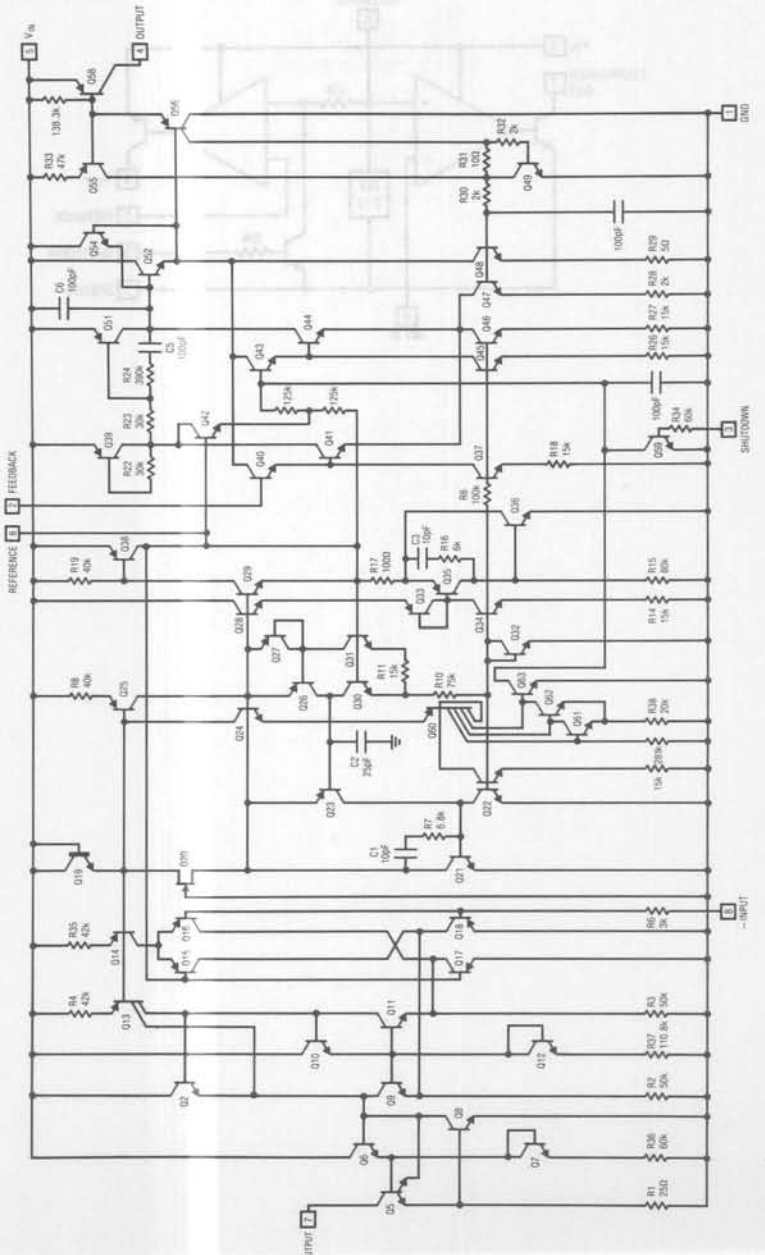
Current Limited 1 Amp Regulator



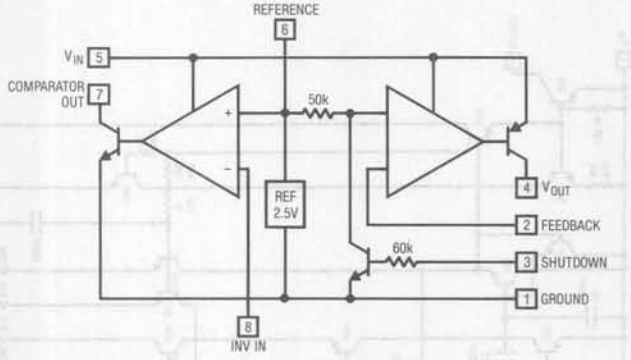
*SETS CURRENT LIMIT BUT INCREASES DROPOUT VOLTAGE BY 0.5V.

†MUST HAVE LOW ESR. SEVERAL 100μF CAPACITORS CAN BE PARALLELED.

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



Micropower Regulator with Comparator and Shutdown

FEATURES

- **20μA Supply Current**
- 8-Lead SOIC
- 125mA Output Current
- 2.5V Reference
- Reference Output Sources 4mA and Sinks 4mA
- Open Collector Comparator Sinks 10mA
- Logic Shutdown
- 0.2V Dropout Voltage
- Thermal Limiting

APPLICATIONS

- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments
- Memory Keep Alive

DESCRIPTION

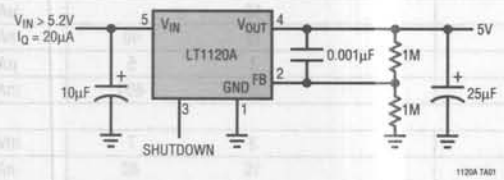
The LT1120A is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 20μA supply current, the LT1120A can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. This allows it to be used as a supply splitter or auxiliary output. A shutdown pin allows logic shutdown of the output.

The comparator can be used for system or battery monitoring. For example, the comparator can be used to warn of low system voltage. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance.

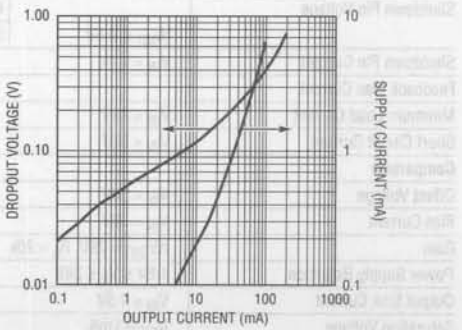
4

TYPICAL APPLICATION

5V Regulator



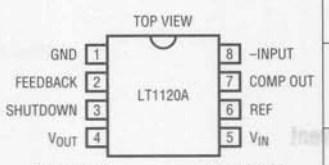
Dropout Voltage and Supply Current



ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
NPN Collector Voltage 36V
Output Short-Circuit Duration ..... Indefinite
Power Dissipation ..... Internally Limited
Operating Temperature Range
LT1120AC ..... 0°C to 100°C
Storage Temperature Range
LT1120AC ..... –65°C to 150°C

PACKAGE/ORDER INFORMATION



T_{JMAX} = 110°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 190°C/W (S)

ORDER PART NUMBER
LT1120ACN8 LT1120ACS8
S8 PART MARKING
1120A

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_J = 25°C

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Voltage	$4.5V \le V_{IN} \le 36V$		2.46	2.50	2.54	V
Line Regulation	$4.5V \le V_{IN} \le 36V$			0.01	0.015	%/V
Load Regulation	$-2.0mA \le I_{REF} \le 2mA$, V_{IN} = 12V			0.3	0.6	%
Output Source Current	V_{IN} = 5V		2	4		mA
Output Sink Current	V_{IN} = 5V		2	4		mA
Temperature Stability				1		%
Regulator						
Supply Current	V_{IN} = 6V, $I_{OUT} \le 100\mu A$			20	25	µA
	V_{IN} = 36V, $I_{OUT} \le 100\mu A$			30	40	µA
	V_{IN} = 12V, I_{OUT} = 125mA			11	20	mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$		125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$			0.2	0.5	%
Line Regulation	$6V \le V_{IN} \le 36V$			0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$			0.02	0.05	V
	I_{OUT} = 125mA			0.40	0.65	V
Feedback Sense Voltage	V_{IN} = 12V		2.44	2.5	2.56	V
Shutdown Pin Voltage		Normal			0.4	V
	$V_{OUT} \le 0.5V$	Shutdown	2.2	1.4		V
Shutdown Pin Current	V_{IN} = 1.4V			10		µA
Feedback Bias Current				15	40	nA
Minimum Load Current	V_{IN} = 36V			1	5	µA
Short Circuit Current	V_{IN} = 36V			250	400	mA
Comparator						
Offset Voltage	V_{IN} = 36V			3	7	mV
Bias Current	V_{IN} = 36V			15	40	nA
Gain	ΔV_{OUT} = 29V, R_L = 20k		2000	10000		V/V
Power Supply Rejection	$4.5V \le V_S \le 36V$		80	96		dB
Output Sink Current	V_{IN} = 4.5V		10	18		mA
Saturation Voltage	I_{OUT} = 1mA			0.4	0.6	V
Input Voltage Range			0		V_{IN} – 1	V
Response Time				5		µs
Leakage Current	V_{IN} = 36V, V(Pin 7) = 36V				2	µA

ELECTRICAL CHARACTERISTICS

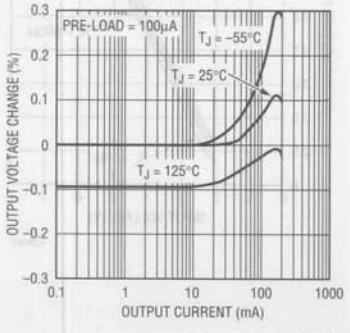
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Voltage	$4.5V \le V_{IN} \le 36V$	●	2.40	2.50	2.55	V
Line Regulation	$4.5V \le V_{IN} \le 36V$	●		0.01	0.02	%/V
Load Regulation	$-2.0mA \le I_{REF} \le 2mA$, $V_{IN} = 12V$	●		0.4	0.8	%
Output Source Current	$V_{IN} = 5V$	●	2			mA
Output Sink Current	$V_{IN} = 5V$	●	2			mA
Regulator						
Supply Current	$V_{IN} = 6V$, $I_{OUT} \le 100\mu A$	●		30	40	µA
	$V_{IN} = 36V$, $I_{OUT} \le 100\mu A$	●		40	50	µA
	$V_{IN} = 12V$, $I_{OUT} = 125mA$	●		11	20	mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●			1	%
Line Regulation	$6V \le V_{IN} \le 36V$	●			0.02	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$	●			0.06	V
	$I_{OUT} = 125mA$	●			0.85	V
Feedback Sense Voltage	$V_{IN} = 12V$	●	2.38	2.5	2.57	V
Feedback Bias Current		●			50	nA
Minimum Load Current	$V_{IN} = 36V$	●			50	µA
Short Circuit Current	$V_{IN} = 36V$	●		240	400	mA
Comparator						
Offset Voltage	$V_{IN} = 36V$	●			10	mV
Bias Current	$V_{IN} = 36V$	●		15	60	nA
Gain	$\Delta V_{OUT} = 29V$, $R_L = 20k$	●	1000			V/V
Output Sink Current (Note 1)	$V_{IN} = 4.5V$	●	5	10		mA
Leakage Current	$V_{IN} = 36V$, V(Pin 7) = 36V	●			8	µA

The ● denotes specifications which apply over the operating temperature range.

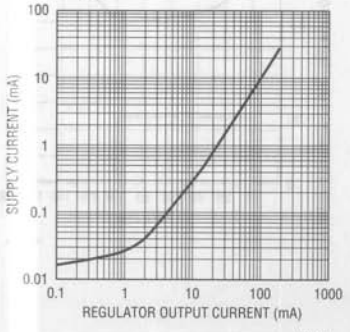
Note 1: For $T_A \le -40°C$ output sink current drops to 2.5mA.

TYPICAL PERFORMANCE CHARACTERISTICS

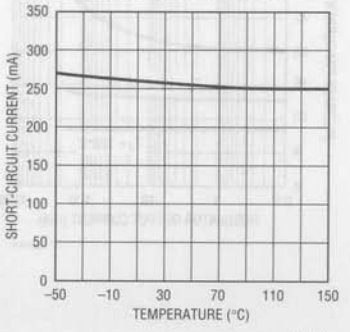
Regulator Load Regulation



Supply Current



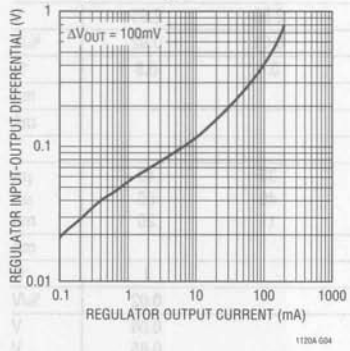
Regulator Short-Circuit Current



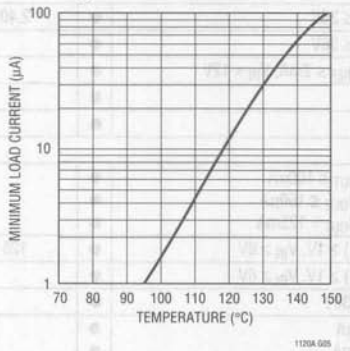
4

TYPICAL PERFORMANCE CHARACTERISTICS

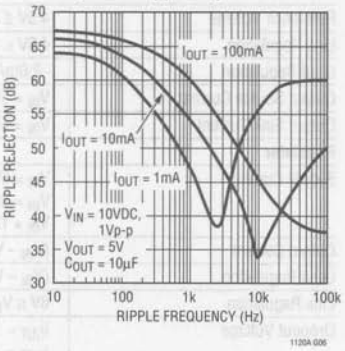
Dropout Voltage



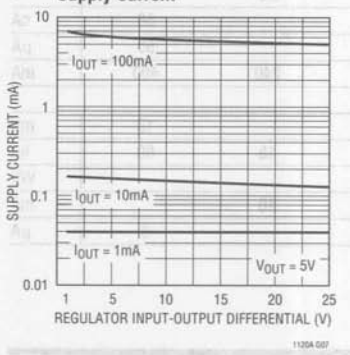
Regulator Minimum Load Current



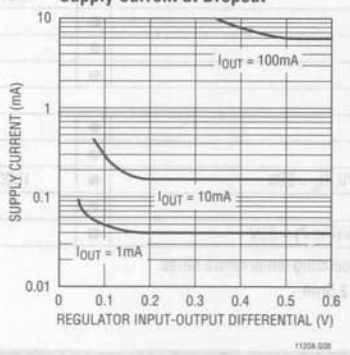
Regulator Ripple Rejection



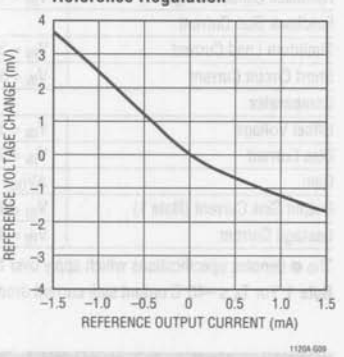
Supply Current



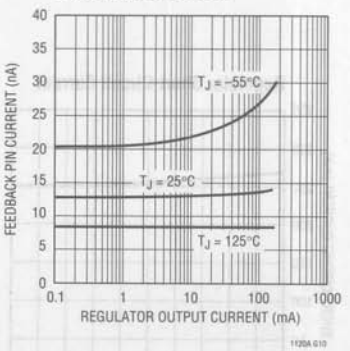
Supply Current at Dropout



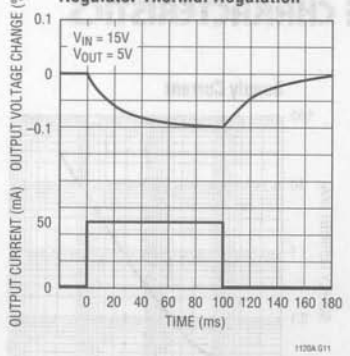
Reference Regulation



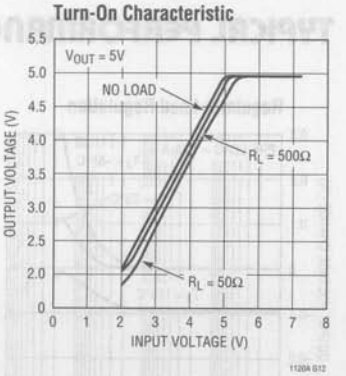
Feedback Pin Current



Regulator Thermal Regulation



Turn-On Characteristic



PIN FUNCTIONS

Pin 1 (Ground).

Pin 2 (Feedback): This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

Pin 3 (Shutdown): A logic 1 shuts off main regulator. Caution: noise or leakage into the shutdown pin can affect output voltage.

Pin 4 (Regulator Output): Main output, requires 10µF output capacitor. Can be shorted to V_{IN} or ground without damaging device.

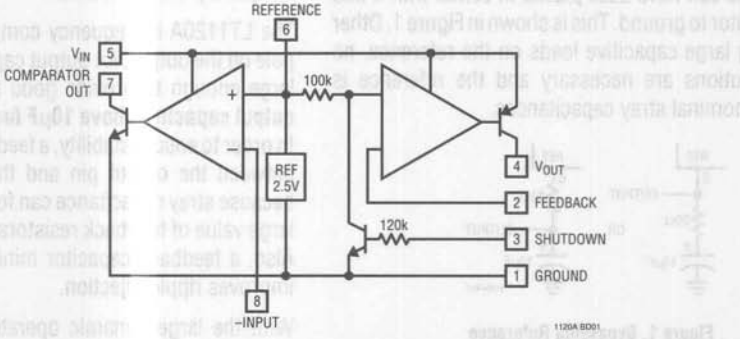
Pin 5 (Input Supply): Bypass with 10µF cap. Must always be more positive than ground.

Pin 6 (Reference): 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 7 (Comparator Output): May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

Pin 8 (Comparator Input): Inverting comparator input.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT1120A is especially suited for micropower system applications. For example, the comparator section of the LT1120A may be used as a battery checker to provide an indication of low battery. Another type of system application for the LT1120A would be to generate the equivalent of split supplies off of a single power input. The regulator section provides regulated output voltage and the reference, which can both source and sink current is then an artificial system ground providing a split supply for the system.

For many applications the comparator can be frequency compensated to operate as an amplifier. Compensation values for various gains are given in the data sheet. The comparator gain is purposely low to make it easier to frequency compensate as an amplifier. The NPN output is capable of sinking 10mA and can drive loads connected to voltages in excess of the positive power supply. This is useful for driving switches or linear regulators off of a higher input voltage.

APPLICATIONS INFORMATION

Reference

Internal to the LT1120A is a 2.5V trimmed class B output reference. The reference was designed to be able to source or sink current so it could be used in supply splitting applications as well as a general purpose reference for external circuitry. The design of the reference allows it to source and sink typically 4mA. The available source and sink current decreases as temperature increases. It is sometimes desirable to decrease the AC output impedance by placing an output capacitor on Pin 6. The reference in the LT1120A becomes unstable with large capacitive loads placed directly on it. When using an output capacitor, about 20Ω should be used to isolate the capacitor from the reference pin. This 20Ω resistor can be placed directly in series with the capacitor or alternatively the reference line can have 20Ω placed in series with it and then a capacitor to ground. This is shown in Figure 1. Other than placing large capacitive loads on the reference, no other precautions are necessary and the reference is stable with nominal stray capacitances.

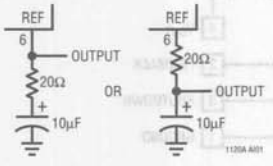


Figure 1. Bypassing Reference

Overload Protection

The main regulator in the LT1120A is current limited at approximately 250mA. The current limit is stable with both input voltage and temperature.

Like most other IC regulators, a minimum load is required on the output of the LT1120A to maintain regulation. For most standard regulators this is normally specified at 5mA. Of course, for a micropower regulator this would be a tremendously large current. The output current must be large enough to absorb all the leakage current of the pass transistor at the maximum operating temperature. It also affects the transient response; low output currents have long recovery times from load transients. At high operating temperatures the minimum load current increases and having too low of a load current may cause the output to go unregulated. Devices are tested for minimum load current at high temperature. The output voltage setting resistors to the feedback terminal can usually be used to provide the minimum load current.

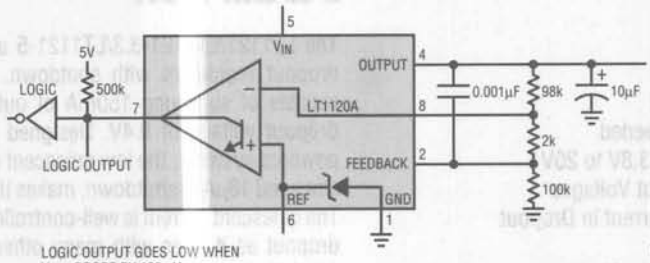
Frequency Compensation

The LT1120A is frequency compensated by a dominant pole on the output. An output capacitor of 10µF is usually large enough to provide good stability. **Increasing the output capacitor above 10µF further improves stability.** In order to ensure stability, a feedback capacitor is needed between the output pin and the feedback pin. This is because stray capacitance can form another pole with the large value of feedback resistors used with the LT1120A. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

With the large dynamic operating range of the output current, 10000:1, frequency response changes widely. Low AC impedance capacitors are needed to insure stability. While solid tantalum are best, aluminum electrolytics can be used but larger capacitor values may be needed.

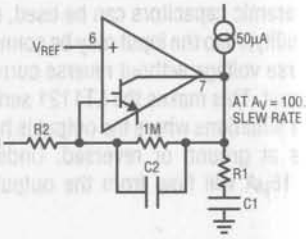
TYPICAL APPLICATIONS

Regulator with Output Voltage Monitor



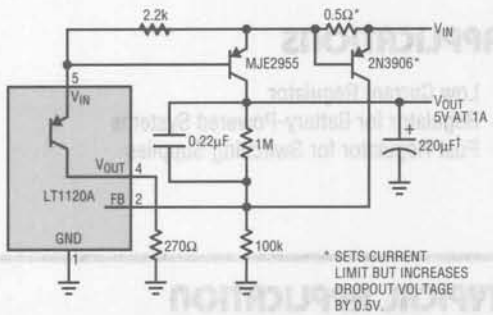
LOGIC OUTPUT GOES LOW WHEN V_{OUT} DROPS BY 100mV

Compensating the Comparator as an Op Amp



A_V	R1	C1	C2	R2
–1	33Ω	0.1µF	0.001µF	1M
–10	100Ω	0.047µF	–	100k
–100	10k	0.002µF	–	10k

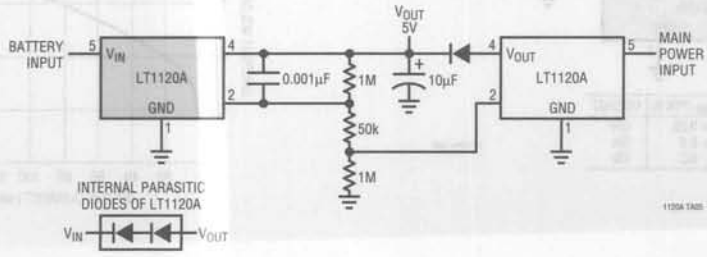
Current Limited 1 Amp Regulator



* SETS CURRENT LIMIT BUT INCREASES DROPOUT VOLTAGE BY 0.5V.

† MUST HAVE LOW ESR. SEVERAL 100µF CAPACITORS CAN BE PARALLELED.

Battery Backup Regulator



Micropower Low Dropout Regulators with Shutdown

FEATURES

- 0.4V Dropout Voltage
- 150mA Output Current
- 30μA Quiescent Current
- No Protection Diodes Needed
- Adjustable Output from 3.8V to 20V
- 3.3V and 5V Fixed Output Voltages
- Controlled Quiescent Current in Dropout
- Shutdown
- 16μA Quiescent Current in Shutdown
- Stable with 0.33μF Output Capacitor
- Reverse Battery Protection
- No Reverse Current with Input Low
- Thermal Limiting

APPLICATIONS

- Low Current Regulator
- Regulator for Battery-Powered Systems
- Post Regulator for Switching Supplies

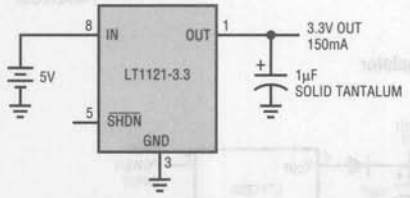
DESCRIPTION

The LT1121/LT1121-3.3/LT1121-5 are micropower low dropout regulators with shutdown. These devices are capable of supplying 150mA of output current with a dropout voltage of 0.4V. Designed for use in battery-powered systems, the low quiescent current, 30μA operating and 16μA in shutdown, makes them an ideal choice. The quiescent current is well-controlled; it does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1121/LT1121-3.3/LT1121-5 include the ability to operate with very small output capacitors. They are stable with only 0.33μF on the output while most older devices require between 1μF and 100μF for stability. Small ceramic capacitors can be used, enhancing manufacturability. Also the input may be connected to ground or a reverse voltage without reverse current flow from output to input. This makes the LT1121 series ideal for backup power situations where the output is held high and the input is at ground or reversed. Under these conditions only 16μA will flow from the output pin to ground.

TYPICAL APPLICATION

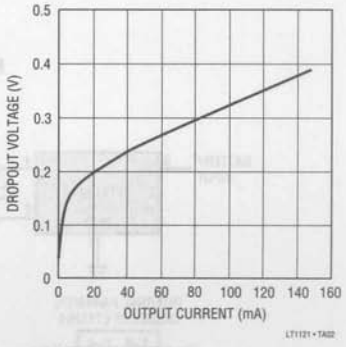
5V Battery-Powered Supply with Shutdown



V_{SHDN} (PIN 5)	OUTPUT
< 0.25	OFF
> 2.8	ON
NC	ON

LT1121 • TA01

Dropout Voltage



LT1121 • TA02

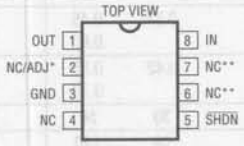
ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... ±30V*
Output Pin Reverse Current 10mA
Adjust Pin Current 10mA
Shutdown Pin Input Voltage (Note 1) ..... 6.5V, –0.6V
Shutdown Pin Input Current (Note 1) 20mA
Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature Range (Note 2)
LT1121C-X ..... 0°C to 125°C
LT1121I-X ..... –40°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*For applications requiring input voltage ratings greater than 30V, contact the factory.

PACKAGE/ORDER INFORMATION



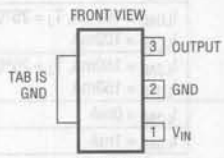
N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

θ_{JA} = 120°C/W (N8, S8)
θ_{JA} = 70°C/W (AS8)

*PIN 2 = NC FOR LT1121-3.3/LT1121-5
= ADJ FOR LT1121

**PINS 6 AND 7 ARE FLOATING (NO INTERNAL CONNECTION) ON THE STANDARD S8 PACKAGE.
PINS 6 AND 7 CONNECTED TO GROUND ON THE A VERSION OF THE LT1121 (S8 ONLY). CONNECTING PINS 6 AND 7 TO THE GROUND PLANE WILL REDUCE THERMAL RESISTANCE. SEE THERMAL RESISTANCE TABLES IN THE APPLICATIONS INFORMATION SECTION.



ST PACKAGE
3-LEAD PLASTIC SOT-223

LT1121 • P003

θ_{JA} = 50°C/W

Z PACKAGE
3-LEAD PLASTIC TO-92

LT1121 • P002

θ_{JA} = 150°C/W

ORDER PART NUMBER		S8 PART MARKING		ORDER PART NUMBER	ORDER PART NUMBER
LT1121CN8	LT1121IS8	1121	1121A	LT1121CST-3.3	LT1121CZ-3.3
LT1121CN8-3.3	LT1121IS8-3.3	11213	121A3	LT1121IST-3.3	LT1121IZ-3.3
LT1121CN8-5	LT1121IS8-5	11215	121A5	LT1121CST-5	LT1121CZ-5
LT1121IN8	LT1121ACS8	1121I	121AI	LT1121IST-5	LT1121IZ-5
LT1121IN8-3.3	LT1121ACS8-3.3	121I3	121AI3		
LT1121IN8-5	LT1121ACS8-5	121I5	121AI5		
LT1121CS8	LT1121AIS8				
LT1121CS8-3.3	LT1121AIS8-3.3				
LT1121CS8-5	LT1121AIS8-5				

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Regulated Output Voltage (Note 3)	LT1121-3.3	V_{IN} = 3.8V, I_{OUT} = 1mA, T_J = 25°C		3.250	3.300	3.350	V
		4.3V < V_{IN} < 20V, 1mA < I_{OUT} < 150mA	●	3.200	3.300	3.400	V
	LT1121-5	V_{IN} = 5.5V, I_{OUT} = 1mA, T_J = 25°C		4.925	5.000	5.075	V
		6V < V_{IN} < 20V, 1mA < I_{OUT} < 150mA	●	4.850	5.000	5.150	V
	LT1121 (Note 4)	V_{IN} = 4.3V, I_{OUT} = 1mA, T_J = 25°C		3.695	3.750	3.805	V
		4.8V < V_{IN} < 20V, 1mA < I_{OUT} < 150mA	●	3.640	3.750	3.860	V
Line Regulation	LT1121-3.3	ΔV_{IN} = 4.8V to 20V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1121-5	ΔV_{IN} = 5.5V to 20V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1121 (Note 4)	ΔV_{IN} = 4.3V to 20V, I_{OUT} = 1mA	●		1.5	10	mV

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation	LT1121-3.3	ΔI_{LOAD} = 1mA to 150mA, T_J = 25°C		−12	−20	mV
		ΔI_{LOAD} = 1mA to 150mA ●		−20	−30	mV
	LT1121-5	ΔI_{LOAD} = 1mA to 150mA, T_J = 25°C		−17	−30	mV
		ΔI_{LOAD} = 1mA to 150mA ●		−28	−45	mV
	LT1121 (Note 4)	ΔI_{LOAD} = 1mA to 150mA, T_J = 25°C		−12	−20	mV
		ΔI_{LOAD} = 1mA to 150mA ●		−18	−30	mV
Dropout Voltage (Note 5)	I_{LOAD} = 1mA, T_J = 25°C			0.13	0.16	V
	I_{LOAD} = 1mA ●				0.25	V
	I_{LOAD} = 50mA, T_J = 25°C			0.30	0.35	V
	I_{LOAD} = 50mA ●				0.50	V
	I_{LOAD} = 100mA, T_J = 25°C			0.37	0.45	V
	I_{LOAD} = 100mA ●				0.60	V
	I_{LOAD} = 150mA, T_J = 25°C			0.42	0.55	V
	I_{LOAD} = 150mA ●				0.70	V
Ground Pin Current (Note 6)	I_{LOAD} = 0mA ●			30	50	µA
	I_{LOAD} = 1mA ●			90	120	µA
	I_{LOAD} = 10mA ●			350	500	µA
	I_{LOAD} = 50mA ●			1.5	2.5	mA
	I_{LOAD} = 100mA ●			4.0	7.0	mA
	I_{LOAD} = 150mA ●			7.0	14.0	mA
Adjust Pin Bias Current (Notes 4, 7)	T_J = 25°C			150	300	nA
Shutdown Threshold	V_{OUT} = Off to On ●			1.2	2.8	V
	V_{OUT} = On to Off ●		0.25	0.75		V
Shutdown Pin Current (Note 8)	V_{SHDN} = 0V ●			6	10	µA
Quiescent Current in Shutdown (Note 9)	V_{IN} = 6V, V_{SHDN} = 0V ●			15	22	µA
Ripple Rejection	$V_{IN} - V_{OUT}$ = 1V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.1A		50	58		dB
Current Limit	$V_{IN} - V_{OUT}$ = 7V, T_J = 25°C			200	500	mA
Input Reverse Leakage Current	V_{IN} = −20V, V_{OUT} = 0V ●				1.0	mA
Reverse Output Current (Note 10)	LT1121-3.3	V_{OUT} = 3.3V, V_{IN} = 0V		16	25	µA
	LT1121-5	V_{OUT} = 5V, V_{IN} = 0V		16	25	µA
	LT1121 (Note 4)	V_{OUT} = 3.8V, V_{IN} = 0V		16	25	µA

The ● denotes specifications which apply over the operating temperature range.

Note 1: The Shutdown pin input voltage rating is required for a low impedance source. Internal protection devices connected to the shutdown pin will turn on and clamp the pin to approximately 7V or −0.6V. This range allows the use of 5V logic devices to drive the pin directly. For high impedance sources or logic running on supply voltages greater than 5.5V, the maximum current driven into the shutdown pin must be limited to less than 20mA.

Note 2: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended. For T_J > 110°C and I_{OUT} < 1mA, output voltage may increase by 1%.

Note 3: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current the input voltage range must be limited.

Note 4: The LT1121 (adjustable version) is tested and specified with the adjust pin connected to the output pin.

Note 5: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output voltage will be equal to: ($V_{IN} - V_{DROPOUT}$).

Note 6: Ground pin current is tested with $V_{IN} = V_{OUT}$ (nominal) and a current source load. This means that the device is tested while operating in its dropout region. This is the worst case ground pin current. The ground pin current will decrease slightly at higher input voltages.

Note 7: Adjust pin bias current flows into the adjust pin.

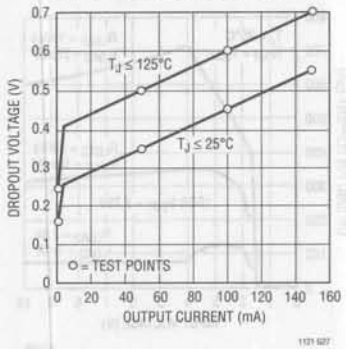
Note 8: Shutdown pin current at V_{SHDN} = 0V flows out of the shutdown pin.

Note 9: Quiescent current in shutdown is equal to the sum total of the shutdown pin current (6µA) and the ground pin current (9µA).

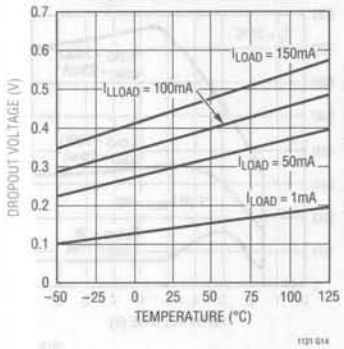
Note 10: Reverse output current is tested with the input pin grounded and the output pin forced to the rated output voltage. This current flows into the output pin and out of the ground pin.

TYPICAL PERFORMANCE CHARACTERISTICS

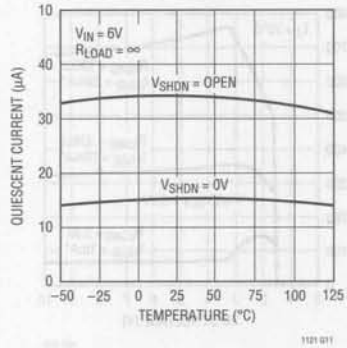
Guaranteed Dropout Voltage



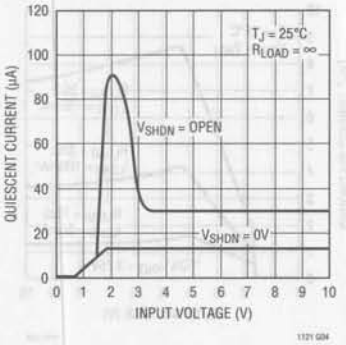
Dropout Voltage



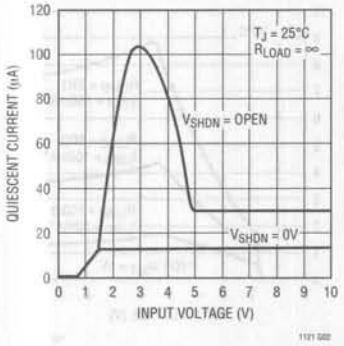
Quiescent Current



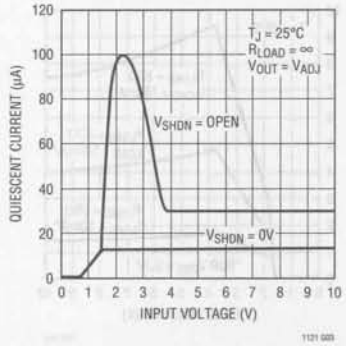
LT1121-3.3 Quiescent Current



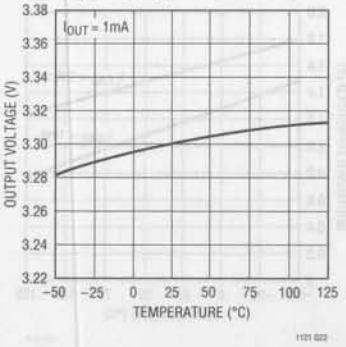
LT1121-5 Quiescent Current



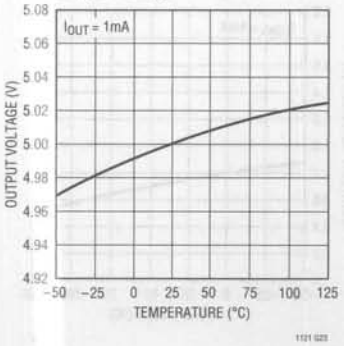
LT1121 Quiescent Current



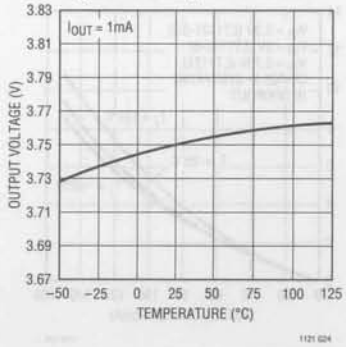
LT1121-3.3 Output Voltage



LT1121-5 Output Voltage



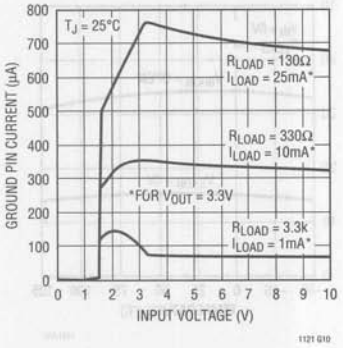
LT1121 Adjust Pin Voltage



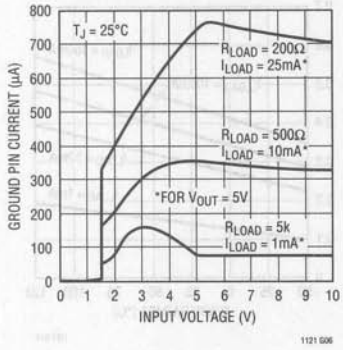
4

TYPICAL PERFORMANCE CHARACTERISTICS

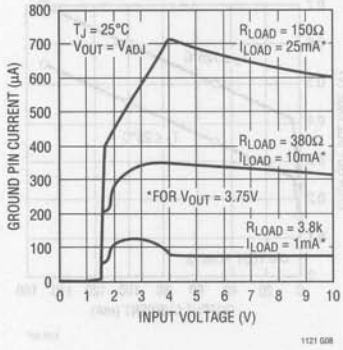
LT1121-3.3 Ground Pin Current



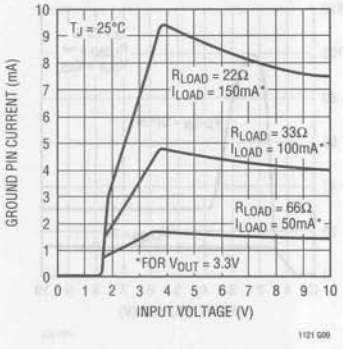
LT1121-5 Ground Pin Current



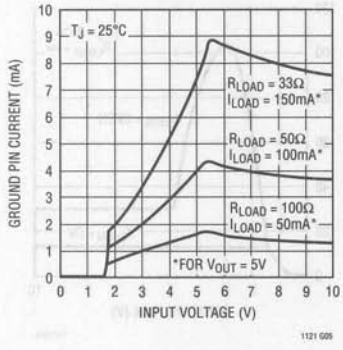
LT1121 Ground Pin Current



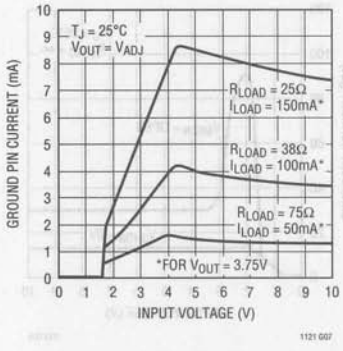
LT1121-3.3 Ground Pin Current



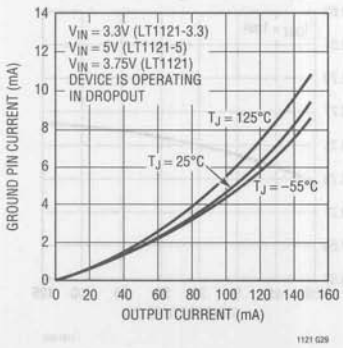
LT1121-5 Ground Pin Current



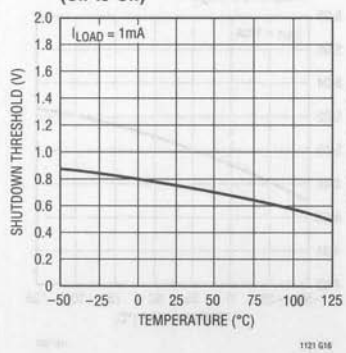
LT1121 Ground Pin Current



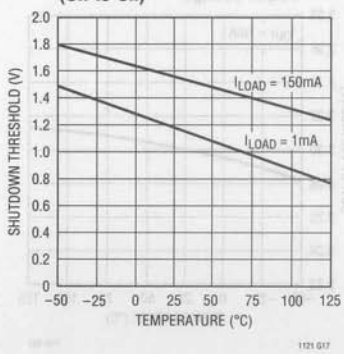
Ground Pin Current



Shutdown Pin Threshold (On-to-Off)

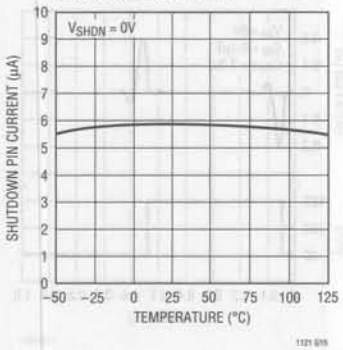


Shutdown Pin Threshold (Off-to-On)

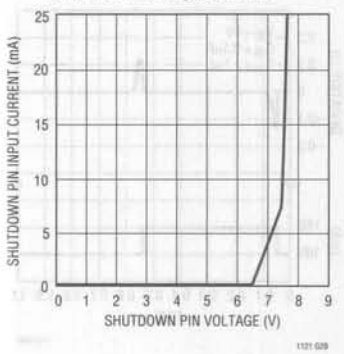


TYPICAL PERFORMANCE CHARACTERISTICS

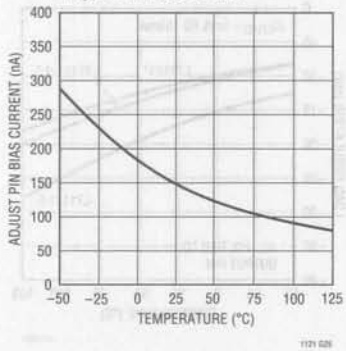
Shutdown Pin Current



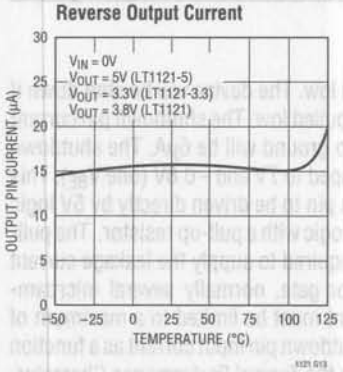
Shutdown Pin Input Current



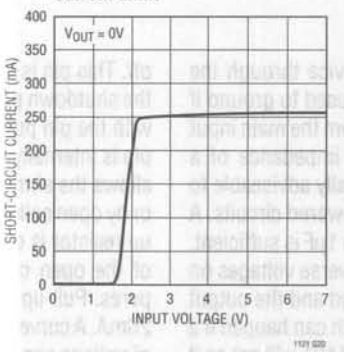
LT1121
Adjust Pin Bias Current



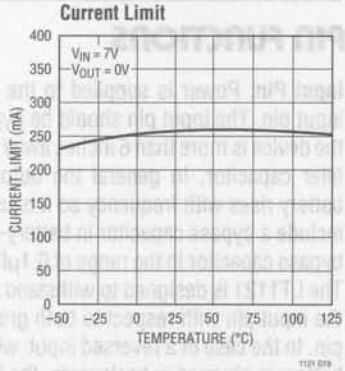
Reverse Output Current



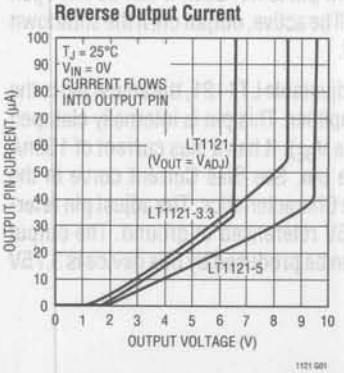
Current Limit



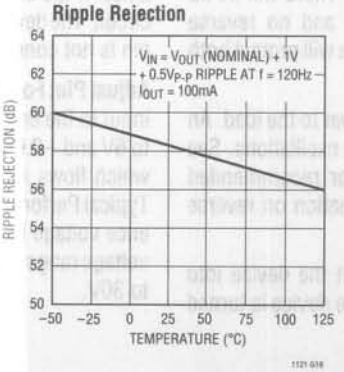
Current Limit



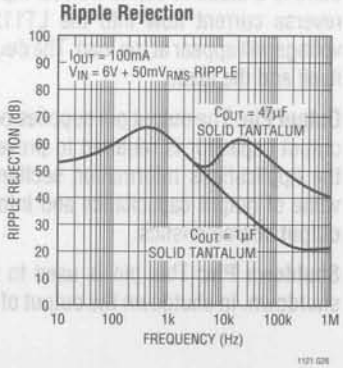
Reverse Output Current



Ripple Rejection



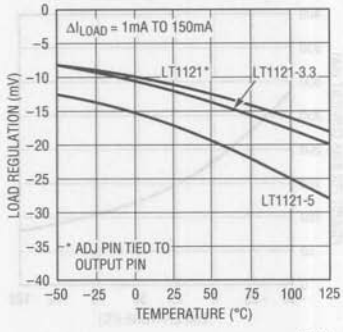
Ripple Rejection



4

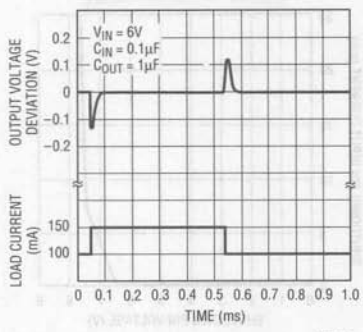
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation



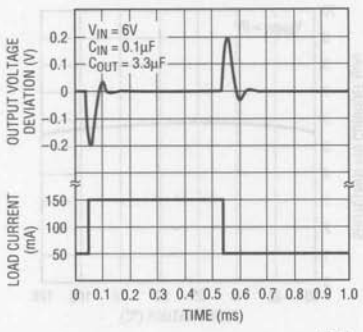
1121 G21

LT1121-5
Load Transient Response



1121 G30

LT1121-5
Load Transient Response



1121 G31

PIN FUNCTIONS

Input Pin: Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than 6 inches away from the main input filter capacitor. In general the output impedance of a battery rises with frequency so it is usually adviseable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 0.1µF to 1µF is sufficient. The LT1121 is designed to withstand reverse voltages on the input pin with respect to both ground and the output pin. In the case of a reversed input, which can happen if a battery is plugged in backwards, the LT1121 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1121 and no reverse voltage will appear at the load. The device will protect both itself and the load.

Output Pin: The output pin supplies power to the load. An output capacitor is required to prevent oscillations. See the Applications Information section for recommended value of output capacitance and information on reverse output characteristics.

Shutdown Pin: This pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the shutdown pin is pulled low. The shutdown pin current with the pin pulled to ground will be 6µA. The shutdown pin is internally clamped to 7V and –0.6V (one V_{BE}). This allows the shutdown pin to be driven directly by 5V logic or by open collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open collector gate, normally several microamperes. Pull-up current must be limited to a maximum of 20mA. A curve of shutdown pin input current as a function of voltage appears in the Typical Performance Characteristics. If the shutdown pin is not used it can be left open circuit. The device will be active, output on, if the shutdown pin is not connected.

Adjust Pin: For the adjustable LT1121, the adjust pin is the input to the error amplifier. This pin is internally clamped to 6V and –0.6V (one V_{BE}). It has a bias current of 150nA which flows into the pin. See Bias Current curve in the Typical Performance Characteristics. The adjust pin reference voltage is 3.75V referenced to ground. The output voltage range that can be produced by this device is 3.75V to 30V.

APPLICATIONS INFORMATION

The LT1121 is a micropower low dropout regulator with shutdown, capable of supplying up to 150mA of output current at a dropout voltage of 0.4V. The device operates with very low quiescent current (30μA). In shutdown the quiescent current drops to only 16μA. In addition to the low quiescent current the LT1121 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against both reverse input voltages and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1121 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The adjustable version of the LT1121 has an output voltage range of 3.75V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output voltage to maintain the voltage at the adjust pin at 3.75V. The current in R1 is then equal to 3.75V/R1. The current in R2 is equal to the sum of the current in R1 and the adjust pin bias current. The adjust pin bias current, 150nA at 25°C, flows through R2 into the adjust pin. The output voltage can be calculated according to the formula in Figure 1. The value of R1 should be less than 400k to minimize errors in the output voltage caused by the adjust pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Adjust Pin Voltage vs Temperature and Adjust Pin Bias Current vs Temperature appear in the Typical Performance Characteristics. The reference voltage at the adjust pin has a slight positive temperature coefficient of approximately 15ppm/°C. The adjust pin bias current has a negative temperature coefficient. These effects are small and will tend to cancel each other.

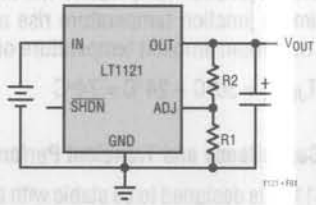


Figure 1. Adjustable Operation

The adjustable device is specified with the adjust pin tied to the output pin. This sets the output voltage to 3.75V. Specifications for output voltage greater than 3.75V will be proportional to the ratio of the desired output voltage to 3.75V (V_{OUT}/3.75V). For example: load regulation for an output current change of 1mA to 150mA is –12mV typical at V_{OUT} = 3.75V. At V_{OUT} = 12V, load regulation would be:

$$\left(\frac{12V}{3.75V}\right) \times (-12mV) = (-38mV)$$

Thermal Considerations

Power handling capability will be limited by maximum rated junction temperature (125°C). Power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$, and
2. Ground pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$.

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1121 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

Heat sinking, for surface mount devices, is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices. Tables 1 through 5 list thermal resistances for each package. Measured values of thermal resistance for several different board sizes and copper areas are listed for each package. All measurements were

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APPLICATIONS INFORMATION

taken in still air, on 3/32" FR-4 board with 1oz copper. All NC leads were connected to the ground plane.

Table 1. N8 Package*

COPPER AREA			THERMAL RESISTANCE
TOPSIDE	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq. mm	2500 sq. mm	80°C/W
1000 sq mm	2500 sq. mm	2500 sq. mm	80°C/W
225 sq mm	2500 sq. mm	2500 sq. mm	85°C/W
1000 sq mm	1000 sq. mm	1000 sq. mm	91°C/W

* Device is mounted on topside. Leads are through hole and are soldered to both sides of board.

Table 2. S8 Package

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	120°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	120°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	125°C/W
100 sq. mm	1000 sq. mm	1000 sq. mm	131°C/W

* Device is mounted on topside.

Table 3. AS8 Package*

COPPER AREA			
TOPSIDE**	BACKSIDE	BOARD AREA	
2500 sq. mm	2500 sq. mm	2500 sq. mm	60°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	60°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	68°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	74°C/W

* Pins 3, 6, and 7 are ground.
** Device is mounted on topside.

Table 4. SOT-223 Package
(Thermal Resistance Junction-to-Tab 20°C/W)

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	50°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	50°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	58°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	64°C/W
1000 sq. mm	1000 sq. mm	1000 sq. mm	57°C/W
1000 sq. mm	0	1000 sq. mm	60°C/W

* Tab of device attached to topside copper

Table 5. TO-92 Package

	THERMAL RESISTANCE
Package alone	220°C/W
Package soldered into PC board with plated through holes only	175°C/W
Package soldered into PC board with 1/4 sq. inch of copper trace per lead	145°C/W
Package soldered into PC board with plated through holes in board, no extra copper trace, and a clip-on type heat sink: Thermalloy type 2224B	160°C/W
Aavid type 5754	135°C/W

Calculating Junction Temperature

Example: given an output voltage of 3.3V, an input voltage range of 4.5V to 7V, an output current range of 0mA to 100mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

Power dissipated by the device will be equal to:

$$I_{OUT\ MAX} \times (V_{IN\ MAX} - V_{OUT}) + (I_{GND} \times V_{IN})$$

where, $I_{OUT\ MAX} = 100mA$
$V_{IN\ MAX} = 7V$
I_{GND} at ($I_{OUT} = 100mA$, $V_{IN} = 7V$) = 5mA

so, $P = 100mA \times (7V - 3.3V) + (5mA \times 7V)$
$= 0.405W$

If we use an SOT-223 package, then the thermal resistance will be in the range of 50°C/W to 65°C/W depending on copper area. So the junction temperature rise above ambient will be less than or equal to:

$$0.405W \times 60°C/W = 24°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 24°C = 74°C$$

Output Capacitance and Transient Performance

The LTC1121 is designed to be stable with a wide range of output capacitors. The minimum recommended value is 1µF with an ESR of 3Ω or less. For applications where space is very limited, capacitors as low as 0.33µF can be used if combined with a small series resistor. Assuming

APPLICATIONS INFORMATION

that the ESR of the capacitor is low (ceramic) the suggested series resistor is shown in Table 5. The LT1121 is a micropower device and output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response. Bypass capacitors, used to decouple individual components powered by the LT1121, will increase the effective value of the output capacitor.

Table 5.

OUTPUT CAPACITANCE	SUGGESTED SERIES RESISTOR
0.33µF	2Ω
0.47µF	1Ω
0.68µF	1Ω
>1µF	None Needed

Protection Features

The LT1121 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 30V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backwards.

For fixed voltage versions of the device, the output can be pulled below ground without damaging the device. If the input is open circuit or grounded the output can be pulled below ground by 20V. The output will act like an open circuit, no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. For the adjustable version of the device, the output pin is internally clamped at one diode drop below ground. Reverse current for the adjustable device must be limited to 5mA.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will vary depending on the conditions. Many battery-powered circuits incorporate some form of power management. The following information will help optimize battery life. Table 6 summarizes the following information.

The reverse output current will follow the curve in Figure 2 when the input pin is pulled to ground. This current flows through the output pin to ground. The state of the shutdown pin will have no effect on output current when the input pin is pulled to ground.

In some applications it may be necessary to leave the input to the LT1121 unconnected when the output is held high. This can happen when the LT1121 is powered from a rectified AC source. If the AC source is removed, then the input of the LT1121 is effectively left floating. The reverse output current also follows the curve in Figure 2 if the input pin is left open. The state of the shutdown pin will have no effect on the reverse output current when the input pin is floating.

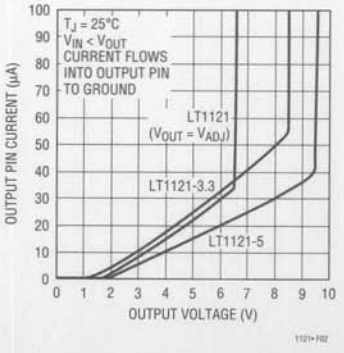


Figure 2. Reverse Output Current

APPLICATIONS INFORMATION

When the input of the LT1121 is forced to a voltage below its nominal output voltage and its output is held high, the reverse output current will still follow the curve in Figure 2. This condition can occur if the input of the LT1121 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or by a second regulator circuit. When the input pin is forced below the output pin or the output pin is pulled above the input pin, the input current will typically drop to less than 2μA (see Figure 3). The state of the shutdown pin will have no effect on the reverse output current when the output is pulled above the input.

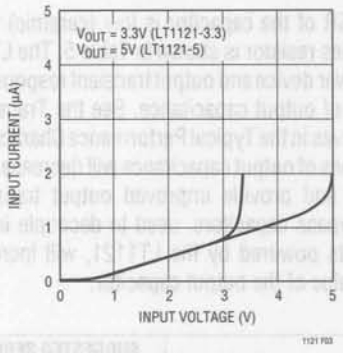


Figure 3. Input Current

Table 6. Fault Conditions

INPUT PIN	SHDN PIN	OUTPUT PIN	
< V_{OUT} (Nominal)	Open (Hi)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15μA (See Figure 2) Input Current ≈ 1μA (See Figure 3)
< V_{OUT} (Nominal)	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15μA (See Figure 2) Input Current ≈ 1μA (See Figure 3)
Open	Open (Hi)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15μA (See Figure 2)
Open	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15μA (See Figure 2)
≤ 0.8V	Open (Hi)	≤ 0V	Output Current = 0
≤ 0.8V	Grounded	≤ 0V	Output Current = 0
> 1.5V	Open (Hi)	≤ 0V	Output Current = Short-Circuit Current
−30V < V_{IN} < 30V	Grounded	≤ 0V	Output Current = 0

Micropower Low Dropout Regulators with Shutdown

FEATURES

- 0.4V Dropout Voltage
- 700mA Output Current
- 50μA Quiescent Current
- No Protection Diodes Needed
- Adjustable Output from 3.8V to 30V
- 3.3V and 5V Fixed Output Voltages
- Controlled Quiescent Current in Dropout
- Shutdown
- 16μA Quiescent Current in Shutdown
- Stable with 3.3μF Output Capacitor
- Reverse Battery Protection
- No Reverse Output Current
- Thermal Limiting
- Surface Mount

APPLICATIONS

- Low Current Regulator
- Regulator for Battery-Powered Systems
- Post Regulator for Switching Supplies
- 5V to 3.3V Logic Regulator

DESCRIPTION

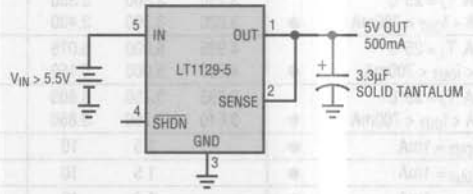
The LT1129/LT1129-3.3/LT1129-5 are micropower low dropout regulators with shutdown. The devices are capable of supplying 700mA of output current with a dropout voltage of 0.4V at maximum output. Designed for use in battery-powered systems the low quiescent current, 50μA operating and 16μA in shutdown, make them an ideal choice. The quiescent current does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1129 /LT1129-3.3/LT1129-5 include the ability to operate with small output capacitors. They are stable with only 3.3μF on the output while most older devices require between 10μF and 100μF for stability. Also the input may be connected to ground or a reverse voltage without reverse current flow from output to input. This makes the LT1129/LT1129-3.3/LT1129-5 ideal for backup power situations where the output is held high and the input is at ground or reversed. Under these conditions, only 16μA will flow from the output pin to ground. The devices are available in 5-lead TO-220, 5-lead DD, and 3-lead SOT-223 packages.

4

TYPICAL APPLICATION

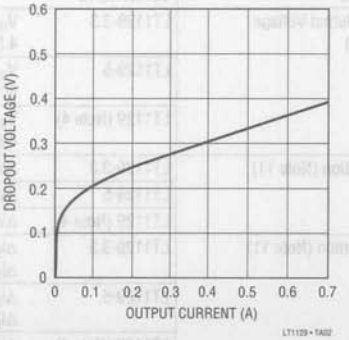
5V Supply with Shutdown



V_{SHDN} (PIN 4)	OUTPUT
< 0.25	OFF
> 2.8	ON
NC	ON

LT1129 • TA01

Dropout Voltage



LT1129 • TA02

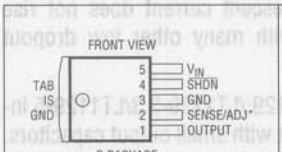
ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... ±30V*
Output Pin Reverse Current 10mA
Sense Pin Current 10mA
Adjust Pin Current 10mA
Shutdown Pin Input Voltage (Note 1) ..... 6.5V, –0.6V
Shutdown Pin Input Current (Note 1) 20mA
Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature Range (Note 2)
LT1129C-X ..... 0°C to 125°C
LT1129C-X Extended Temperature Range (Note 11) ..... –40°C to 125°C
LT1129I-X ..... –40°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

* For applications requiring input voltage ratings greater than 30V, contact the factory.

PACKAGE/ORDER INFORMATION

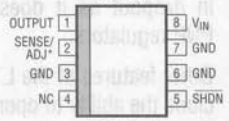


Q PACKAGE
5-LEAD DD

*PIN 2 = SENSE FOR LT1129-3.3/LT1129-5
= ADJ FOR LT1129

θ_{JA} = 30°C/W

ORDER PART NUMBER
LT1129CQ
LT1129CQ-3.3
LT1129CQ-5
LT1129IQ
LT1129IQ-3.3
LT1129IQ-5

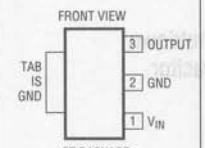


S8 PACKAGE
8-LEAD PLASTIC SO

*PIN 2 = SENSE FOR LT1129-3.3/LT1129-5
= ADJ FOR LT1129

θ_{JA} = 60°C/W

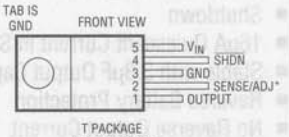
ORDER PART NUMBER	PART MARKING
LT1129CS8	1129
LT1129CS8-3.3	11293
LT1129CS8-5	11295
LT1129IS8	
LT1129IS8-3.3	
LT1129IS8-5	



ST PACKAGE
3-LEAD PLASTIC SOT-223

θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1129CST-3.3
LT1129CST-5
LT1129IST-3.3
LT1129IST-5



T PACKAGE
5-LEAD TO-220

*PIN 2 = SENSE FOR LT1129-3.3/LT1129-5
= ADJ FOR LT1129

θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1129CT
LT1129CT-3.3
LT1129CT-5
LT1129IT
LT1129IT-3.3
LT1129IT-5

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Regulated Output Voltage (Notes 3,11)	LT1129-3.3	V_{IN} = 3.8V, I_{OUT} = 1mA, T_J = 25°C		3.250	3.300	3.350	V
		4.3V < V_{IN} < 20V, 1mA < I_{OUT} < 700mA	●	3.200	3.300	3.400	V
	LT1129-5	V_{IN} = 5.5V, I_{OUT} = 1mA, T_J = 25°C		4.925	5.000	5.075	V
		6V < V_{IN} < 20V, 1mA < I_{OUT} < 700mA	●	4.850	5.000	5.150	V
	LT1129 (Note 4)	V_{IN} = 4.3V, I_{OUT} = 1mA, T_J = 25°C		3.695	3.750	3.805	V
		4.8V < V_{IN} < 20V, 1mA < I_{OUT} < 700mA	●	3.640	3.750	3.860	V
Line Regulation (Note 11)	LT1129-3.3	ΔV_{IN} = 4.8V to 20V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1129-5	ΔV_{IN} = 5.5V to 20V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1129 (Note 4)	ΔV_{IN} = 4.3V to 20V, I_{OUT} = 1mA	●		1.5	10	mV
Load Regulation (Note 11)	LT1129-3.3	ΔI_{LOAD} = 1mA to 700mA, T_J = 25°C			6	20	mV
		ΔI_{LOAD} = 1mA to 700mA	●		15	30	mV
	LT1129-5	ΔI_{LOAD} = 1mA to 700mA, T_J = 25°C			6	20	mV
		ΔI_{LOAD} = 1mA to 700mA	●		20	30	mV
	LT1129 (Note 4)	ΔI_{LOAD} = 1mA to 700mA, T_J = 25°C			6	20	mV
		ΔI_{LOAD} = 1mA to 700mA	●		15	30	mV

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage (Note 5)	I_{LOAD} = 10mA, T_J = 25°C			0.13	0.20	V
	I_{LOAD} = 10mA	●			0.25	V
	I_{LOAD} = 100mA, T_J = 25°C			0.25	0.35	V
	I_{LOAD} = 100mA	●			0.45	V
	I_{LOAD} = 500mA, T_J = 25°C			0.37	0.45	V
	I_{LOAD} = 500mA	●			0.60	V
	I_{LOAD} = 700mA, T_J = 25°C			0.45	0.55	V
	I_{LOAD} = 700mA	●			0.70	V
Ground Pin Current (Note 6)	I_{LOAD} = 0mA	●		50	70	µA
	I_{LOAD} = 10mA	●		310	450	µA
	I_{LOAD} = 100mA	●		2.0	3.5	mA
	I_{LOAD} = 300mA	●		10	20	mA
	I_{LOAD} = 500mA	●		25	45	mA
	I_{LOAD} = 700mA	●		50	90	mA
Adjust Pin Bias Current (Notes 4, 7)	T_J = 25°C			150	300	nA
Shutdown Threshold	V_{OUT} = Off to On	●		1.2	2.8	V
	V_{OUT} = On to Off	●	0.25	0.75		V
Shutdown Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V	●		6	10	µA
Quiescent Current in Shutdown (Note 9)	V_{IN} = 6V, V_{SHDN} = 0V	●		15	25	µA
Ripple Rejection	$V_{IN} - V_{OUT}$ = 1V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.7A, T_J = 25°C		58	64		dB
Current Limit	$V_{IN} - V_{OUT}$ = 7V, T_J = 25°C			1.2	1.6	A
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1.0	mA
Reverse Output Current (Note 10)	LT1129-3.3	V_{OUT} = 3.3V, V_{IN} = 0V		16	25	µA
	LT1129-5	V_{OUT} = 5V, V_{IN} = 0V		16	25	µA
	LT1129 (Note 4)	V_{OUT} = 3.8V, V_{IN} = 0V		16	25	µA

The ● denotes specifications which apply over the operating temperature range.

Note 1: The shutdown pin input voltage rating is required for a low impedance source. Internal protection devices connected to the shutdown pin will turn on and clamp the pin to approximately 7V or –0.6V. This range allows the use of 5V logic devices to drive the pin directly. For high impedance sources or logic running on supply voltages greater than 5.5V, the maximum current driven into the shutdown pin must be limited to less than 20mA.

Note 2: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended. For T_J > 110°C and I_{OUT} < 1mA, output voltage may increase by 1%.

Note 3: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current the input voltage range must be limited.

Note 4: The LT1129 is tested and specified with the adjust pin connected to the output pin.

Note 5: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output voltage will be equal to ($V_{IN} - V_{DROPOUT}$). Dropout voltage is measured between the input pin and the output pin. External voltage drops between the output pin and the sense pin will add to the dropout voltage.

Note 6: Ground pin current is tested with $V_{IN} = V_{OUT}$ (nominal) and a current source load. This means that the device is tested while operating in its dropout region. This is the worst case ground pin current. The ground pin current will decrease slightly at higher input voltages.

Note 7: Adjust pin bias current flows into the adjust pin.

Note 8: Shutdown pin current at V_{SHDN} = 0V flows out of the shutdown pin.

Note 9: Quiescent current in shutdown is equal to the sum total of the shutdown pin current (6µA) and the ground pin current (9µA).

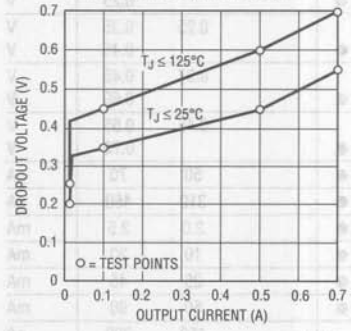
Note 10: Reverse output current is tested with the input pin grounded. The output pin and the sense pin are forced to the rated output voltage. This current flows into the sense pin and out of the ground pin. For the LT1129 (adjustable version) the sense pin is internally tied to the output pin.

Note 11: For C grade devices Regulated Output Voltage, Line Regulation, and Load Regulation are guaranteed over the extended temperature range of –40°C to 125°C. These parameters are not tested or quality assurance sampled at –40°C. They are guaranteed by design, correlation and/or inference from 25°C and/or 0°C tests.

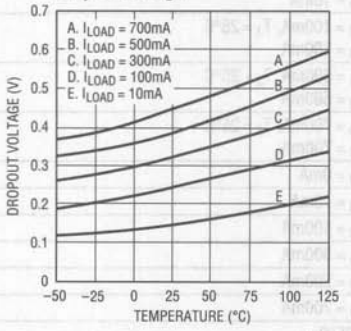
4

TYPICAL PERFORMANCE CHARACTERISTICS

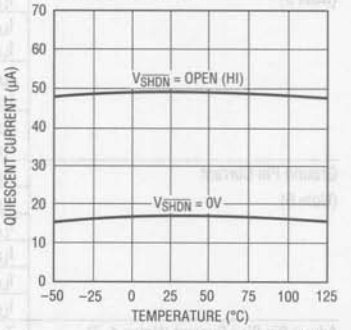
Guaranteed Dropout Voltage



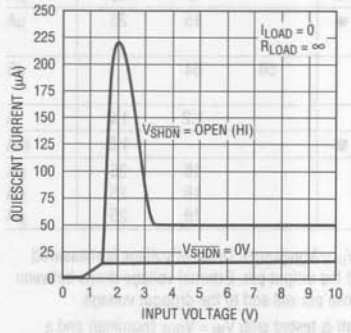
Dropout Voltage



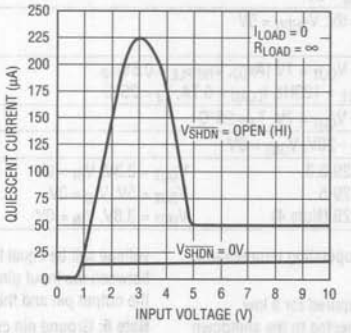
Quiescent Current



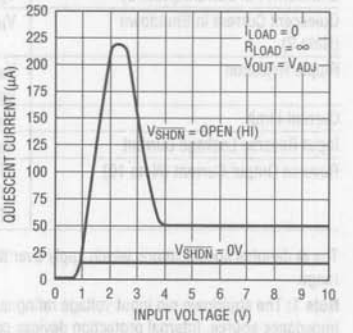
LT1129-3.3 Quiescent Current



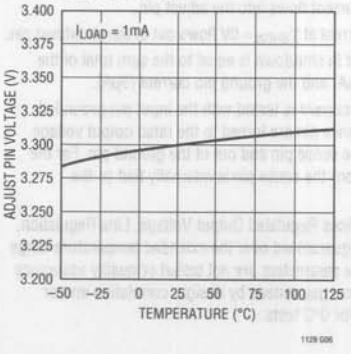
LT1129-5 Quiescent Current



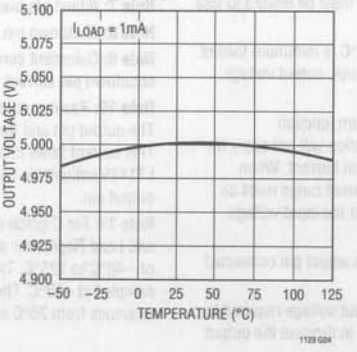
LT1129 Quiescent Current



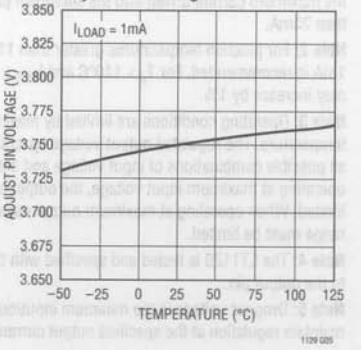
LT1129-3.3 Output Voltage



LT1129-5 Output Voltage

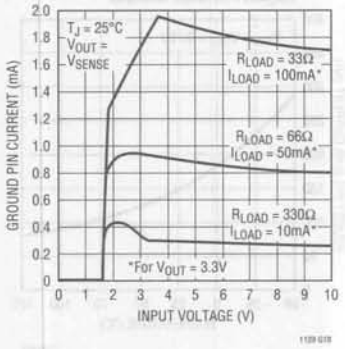


LT1129 Adjust Pin Voltage

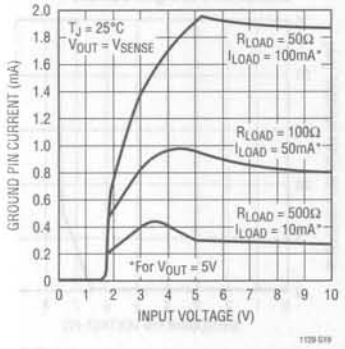


TYPICAL PERFORMANCE CHARACTERISTICS

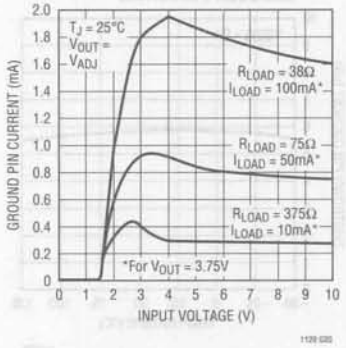
LT1129-3.3 Ground Pin Current



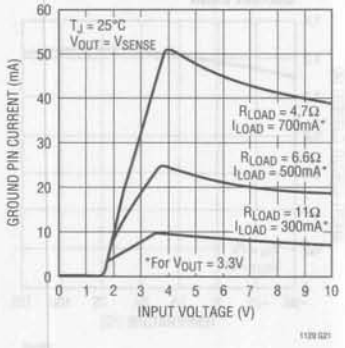
LT1129-5 Ground Pin Current



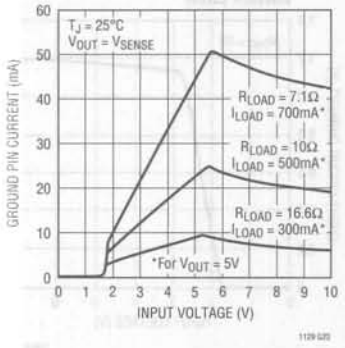
LT1129 Ground Pin Current



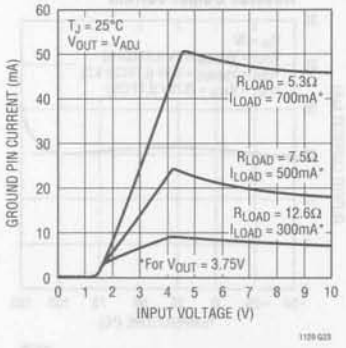
LT1129-3.3 Ground Pin Current



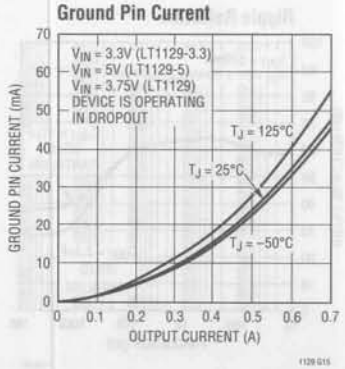
LT1129-5 Ground Pin Current



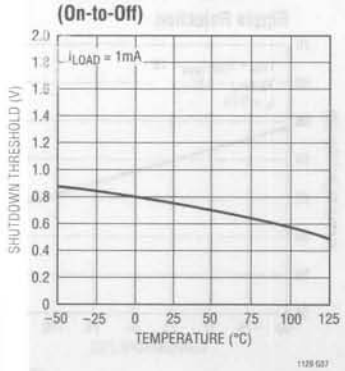
LT1129 Ground Pin Current



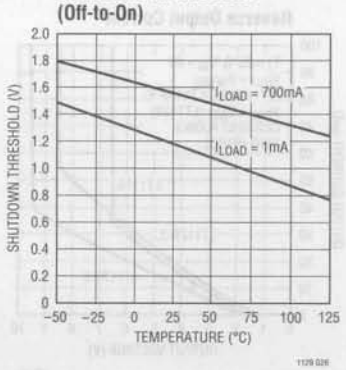
Ground Pin Current



Shutdown Pin Threshold (On-to-Off)



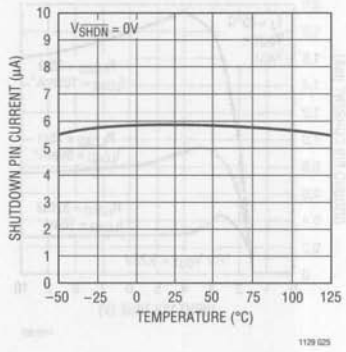
Shutdown Pin Threshold (Off-to-On)



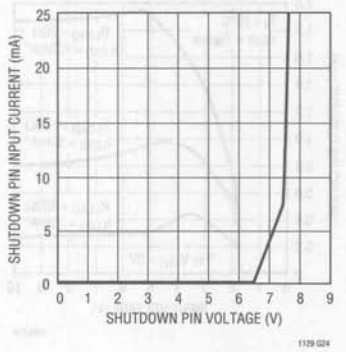
4

TYPICAL PERFORMANCE CHARACTERISTICS

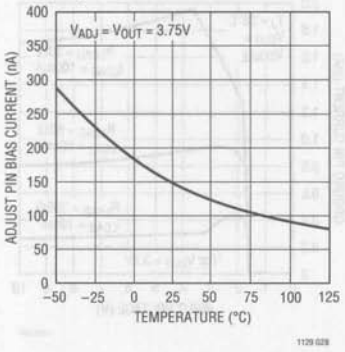
Shutdown Pin Current



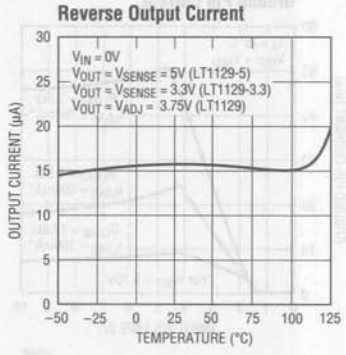
Shutdown Pin Input Current



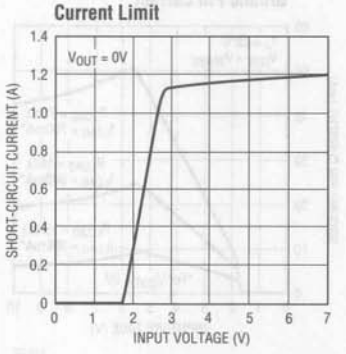
Adjust Pin Bias Current



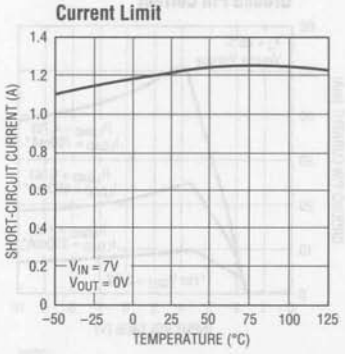
Reverse Output Current



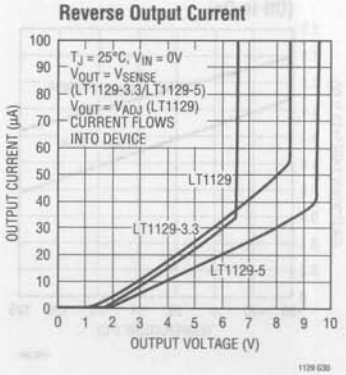
Current Limit



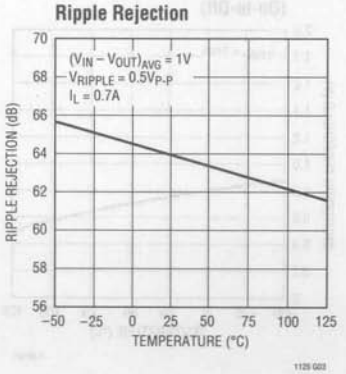
Current Limit



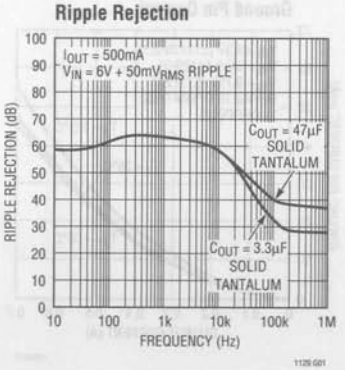
Reverse Output Current



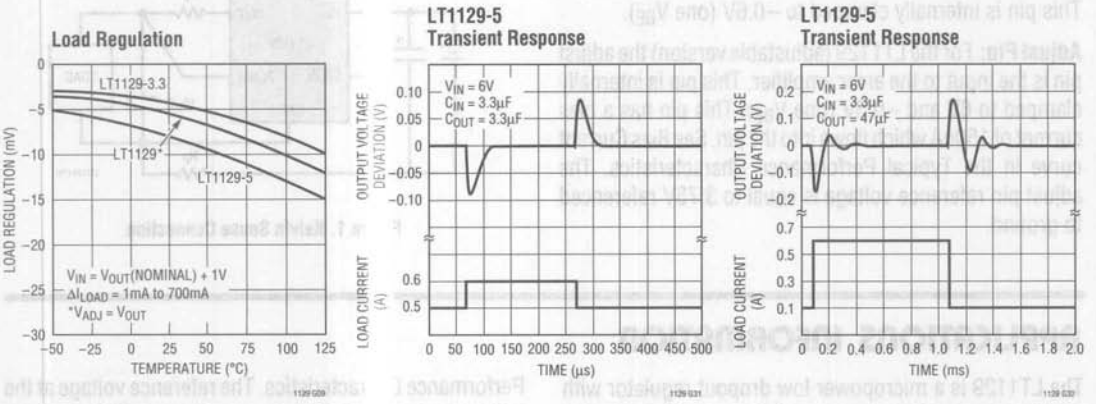
Ripple Rejection



Ripple Rejection



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

Input Pin: Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than 6 inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT1129 is designed to withstand reverse voltages on the input pin with respect to both ground and the output pin. In the case of a reversed input, which can happen if a battery is plugged in backwards, the LT1129 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1129 and no reverse voltage will appear at the load. The device will protect both itself and the load.

Output Pin: The output pin supplies power to the load. An output capacitor is required to prevent oscillations. See the Applications Information section for recommended value of output capacitance and information on reverse output characteristics.

Shutdown Pin ($\overline{SHDN}$): This pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the shutdown pin is actively pulled low. The shutdown pin current with the pin pulled to ground will be 6µA. The shutdown pin is internally clamped to 7V and –0.6V (one V_{BE}). This allows the shutdown pin to be driven directly by 5V logic or by open collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open collector gate, normally several microamperes. Pull-up current must be limited to a maximum of 20mA. A curve of shutdown pin input current as a function of voltage appears in the Typical Performance Characteristics. If the shutdown pin is not used it can be left open circuit. The device will be active, output on, if the shutdown pin is not connected.

Sense Pin: For fixed voltage versions of the LT1129 (LT1129-3.3, LT1129-5) the sense pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the sense pin is connected to the output pin. For most applications the sense pin is connected directly to the output pin at the regulator. In critical applications small voltage drops caused by the resistance (R_P) of PC traces between the regulator and the load, which would normally degrade regulation, may be eliminated by connecting the sense pin to the output pin at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The sense pin bias

PIN FUNCTIONS

current is 15μA at the nominal regulated output voltage. This pin is internally clamped to –0.6V (one V_{BE}).

Adjust Pin: For the LT1129 (adjustable version) the adjust pin is the input to the error amplifier. This pin is internally clamped to 6V and –0.6V (one V_{BE}). This pin has a bias current of 150nA which flows into the pin. See Bias Current curve in the Typical Performance Characteristics. The adjust pin reference voltage is equal to 3.75V referenced to ground.

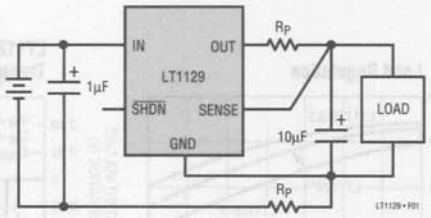


Figure 1. Kelvin Sense Connection

APPLICATIONS INFORMATION

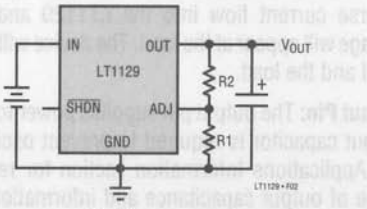
The LT1129 is a micropower low dropout regulator with shutdown, capable of supplying 700mA of output current at a dropout voltage of 0.4V. The device operates with very low quiescent current (50μA). In shutdown the quiescent current drops to only 16μA. In addition to the low quiescent current the LT1129 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against reverse input voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1129 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The adjustable version of the LT1129 has an output voltage range of 3.75V to 30V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output voltage to maintain the voltage at the adjust pin at 3.75V. The current in R1 is then equal to 3.75V/R1. The current in R2 is equal to the sum of the current in R1 and the adjust pin bias current. The adjust pin bias current, 150nA at 25°C, flows through R2 into the adjust pin. The output voltage can be calculated according to the formula in Figure 2. The value of R1 should be less than 400k to minimize errors in the output voltage caused by the adjust pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Adjust Pin Voltage vs Temperature and Adjust Pin Bias Current vs Temperature appear in the Typical Performance Characteristics. The reference voltage at the adjust pin has a positive temperature coefficient of approximately 15ppm/°C. The adjust pin bias current has a negative temperature coefficient. These effects are small and will tend to cancel each other.

The adjustable device is specified with the adjust pin tied to the output pin. This sets the output voltage to 3.75V. Specifications for output voltages greater than 3.75V will be proportional to the ratio of the desired output voltage to 3.75V (V_{OUT}/3.75V). For example: load regulation for an output current change of 1mA to 700mA is –6mV typical at V_{OUT} = 3.75V. At V_{OUT} = 12V, load regulation would be:

$$\left(\frac{12V}{3.75V}\right)\times(-6mV)=(-19mV)$$



$V_{OUT} = 3.75V\left(1+\frac{R2}{R1}\right)+(I_{ADJ} \cdot R2)$

V_{ADJ} = 3.75V

I_{ADJ} = 150nA at 25°C

OUTPUT RANGE = 3.75V to 30V

Figure 2. Adjustable Operation

APPLICATIONS INFORMATION

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$, and
2. Ground pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$.

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1129 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the length/area ratio of the thermal resistor between layers is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistances for each package. For the TO-220 package, thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different board sizes and copper areas are listed for each package. All measurements were taken in still air on 3/32" FR-4 board with 1-oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape. Some experimentation will be necessary to determine the actual value.

Table 1. Q Package, 5-Lead DD

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	25°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	27°C/W
125 sq. mm	2500 sq. mm	2500 sq. mm	35°C/W

* Tab of device attached to topside copper

Table 2. ST Package, 3-Lead SOT-223

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	45°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	45°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	53°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	59°C/W

* Tab of device attached to topside copper

Table 3. S8 Package, 8-Lead Plastic SOIC

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	55°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	55°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	63°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	69°C/W

* Device attached to topside copper

T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 5°C/W

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4.5V to 5.5V, an output current range of 0mA to 500mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT\ MAX} \times (V_{IN\ MAX} - V_{OUT}) + (I_{GND} \times V_{IN\ MAX})$$

where, $I_{OUT\ MAX} = 500mA$

$V_{IN\ MAX} = 5.5V$

I_{GND} at ($I_{OUT} = 500mA$, $V_{IN} = 5.5V$) = 25mA

so, $P = 500mA \times (5.5V - 3.3V) + (25mA \times 5.5V)$
$= 1.24W$

If we use a DD package, then the thermal resistance will be in the range of 25°C/W to 35°C/W depending on copper area. So the junction temperature rise above ambient will be approximately equal to:

$$1.24W \times 30°C/W = 37.2°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 37.2°C = 87.2°C$$

Output Capacitance and Transient Performance

The LT1129 is designed to be stable with a wide range of output capacitors. The minimum recommended value is 3.3µF with an ESR of 2Ω or less. The LT1129 is a micropower device and output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response. Bypass capacitors, used to decouple individual components powered by the LT1129, will increase the effective value of the output capacitor.

Protection Features

The LT1129 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, and reverse voltages from output to input. For fixed voltage devices the output and sense pins are tied together at the output.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 30V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backwards.

For fixed voltage versions of the device, the sense pin is internally clamped to one diode drop below ground. For the adjustable version of the device, the output pin is internally clamped at one diode drop below ground. If the output pin of an adjustable device, or the sense pin of a fixed voltage device, is pulled below ground, with the input open or grounded, current must be limited to less than 5mA.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will vary depending on the conditions. Many battery-powered circuits incorporate some form of power management. The following information will help optimize battery life. Table 3 summarizes the following information.

Output current will be minimized if the input pin of the LT1129 is pulled to ground when the output is held high. Figure 3 shows reverse output current as a function of output voltage with the input pin pulled to ground. This current flows through the device to ground. This curve will hold as long as the input pin is pulled below about 0.8V or if the impedance from the input pin to ground is less than 50kΩ. The state of the shutdown pin will have no effect on output current when the input pin is pulled to ground.

In some applications it may be necessary to leave the input to the LT1129 unconnected when the output is held high. This can happen when the LT1129 is powered from a rectified AC source. If the AC source is removed, then the input of the LT1129 is effectively left floating. In this configuration the reverse output current is slightly higher. It is roughly equal to the normal quiescent current. Note that in this configuration the state of the shutdown pin has a significant effect on the output current. Pulling the shutdown pin to ground will minimize the output current in this configuration. Figure 4 shows output current as a function of output voltage with the input pin floating (open circuit or connected to an input bypass capacitor) and the

APPLICATIONS INFORMATION

shutdown pin floating (open circuit). Figure 5 shows output current as a function of output voltage with the input floating and the shutdown pin pulled to ground.

When the input of the LT1129 is forced to a voltage below its nominal output voltage and its output is held high, the output current will follow the curve shown in Figure 6. This can happen if the input of the LT1129 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or by a second regulator circuit.

Users with applications requiring lower reverse currents should contact the factory about the availability of a modified version of the LT1129.

Table 4. Fault Conditions

INPUT PIN	$\overline{SHDN}$ PIN	OUTPUT/SENSE PINS	
≤ 0.8V	Open (Hi)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3)
≤ 0.8V	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3)
Open	Open (Hi)	> 1V	Reverse Output Current ≈ 200µA Peak (See Figure 4)
Open	Grounded	> 1V	Reverse Output Current ≈ 35µA at V_{OUT} = V_{OUT} (Nominal) (See Figure 5)
0.8V ≤ V_{IN} ≤ V_{OUT}	Open (Hi)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 300µA Peak (See Figure 6)
0.8V ≤ V_{IN} ≤ V_{OUT}	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 300µA (See Figure 6)

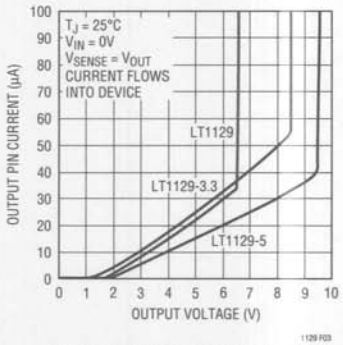


Figure 3. Reverse Output Current

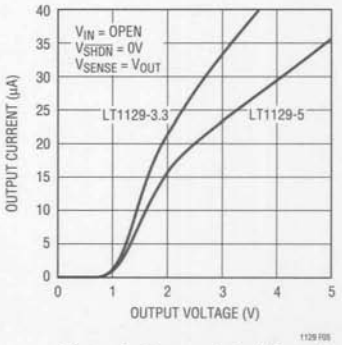


Figure 5. Reverse Output Current

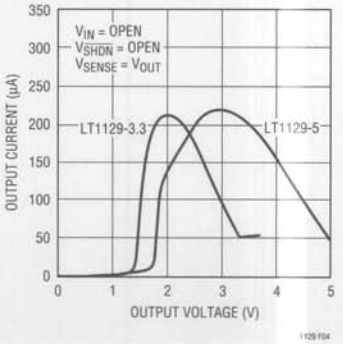


Figure 4. Reverse Output Current

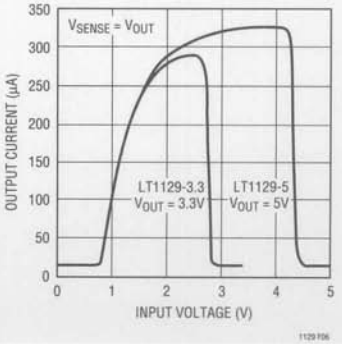


Figure 6. Reverse Output Current

SECTION 4—POWER PRODUCTS

POWER AND MOTOR CONTROL

LTC1153, Auto-Reset Electronic Circuit Breaker 4-138
LTC1154, High-Side Micropower MOSFET Driver 4-152
LTC1157, 3.3V Dual Micropower High-Side/Low-Side MOSFET Driver 4-167
LT1161, Quad Protected High-Side MOSFET Driver 4-175
LTC1163/LTC1165, Triple 1.8V to 6V High-Side MOSFET Drivers 4-186
LT1248, Power Factor Controller 4-194
LT1249, Power Factor Controller 4-205
LTC1255, Dual 24V High-Side MOSFET Driver 4-215

Auto-Reset Electronic Circuit Breaker

FEATURES

- Programmable Trip Delay: 15µs to >100ms
- Programmable Trip Current: 1mA to >20A
- Programmbale Auto-Reset Time: 1ms to >10 sec.
- 4.5V to 18V Supply Range
- Drives Low $R_{DS(ON)}$ N-Channel MOSFETs
- Status Output Indicates Fault Condition
- Thermal Trip with PTC Thermistor
- 8µA I_Q in Standby Mode
- No External Charge Pump Capacitors
- Available in 8-Pin SOIC

APPLICATIONS

- Power Bus Circuit Breaker
- SCSI Termination Power Protection
- Regulator Over-Current Protection
- Battery Short-Circuit Protection
- DC Motor Stall Protection
- Sensitive System Power Interrupt

DESCRIPTION

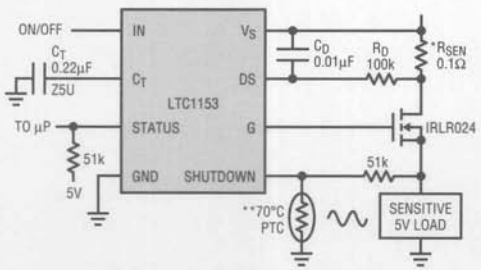
The LTC1153 electronic circuit breaker drives a low cost N-channel MOSFET to interrupt power to a sensitive electronic load in the event of an over-current condition. The breaker remains tripped for a period of time set by an external timing capacitor and then is automatically reset. This cycle continues until the over-current condition is removed, protecting both the sensitive load and the MOSFET switch.

The trip current, trip delay time and auto-reset period are programmable over a wide range to accommodate a variety of load impedances. An active high shutdown input is also provided and interfaces directly to a PTC thermistor for thermal circuit breaking. An open-drain output is provided to report breaker status to the µP.

The LTC1153 is available in both 8-pin DIP and 8-pin SOIC packages.

TYPICAL APPLICATION

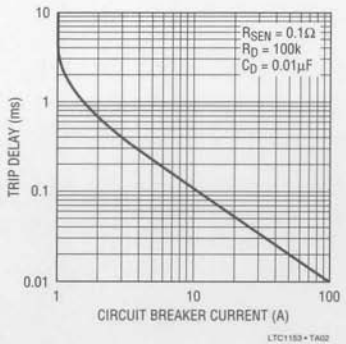
5V/1A Electronic Circuit Breaker with 1ms Trip Delay, 200ms Auto-Reset Period and 70°C Thermal Shutdown



ALL COMPONENTS SHOWN ARE SURFACE MOUNT.
* IMS026 INTERNATIONAL MANUFACTURING SERVICE, INC. (401) 683-9700
** RL2006-100-70-30-PT1 KEYSTONE CARBON COMPANY (814) 781-1591

LTC1153 • TA01

Trip Delay Time

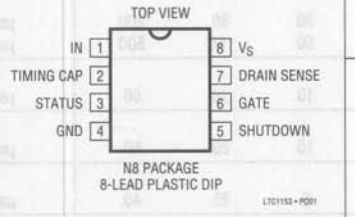


LTC1153 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Input Voltage ..... (V_S + 0.3V) to (GND – 0.3V)
Timing Capacitor Voltage... (VS + 0.3V) to (GND – 0.3V)
Gate Voltage ..... (VS + 24V) to (GND – 0.3V)
Status Output Voltage 15V
Current (Any Pin) 50mA
Operating Temperature
LTC1153C ..... 0°C to 70°C
Storage Temperature Range ..... –65°c to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

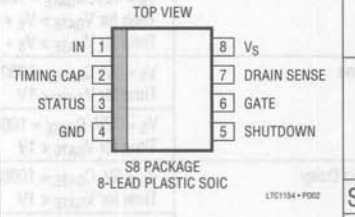
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LTC1153CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	S8 PART MARKING
LTC1153CS8	1153

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 4.5V to 18V, T_A = 25°C, C_T = 0.1µF, V_{SD} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1153C MIN	LTC1153C TYP	LTC1153C MAX	UNITS
V_S	Supply Voltage		●	4.5		18	V
I_Q	Quiescent Current OFF	V_S = 5V, V_{IN} = 0V			8	20	µA
I_Q	Quiescent Current ON	V_S = 5V, V_{IN} = 5V			85	120	µA
I_Q	Quiescent Current ON	V_S =12V, V_{IN} = 5V			180	400	µA
V_{INH}	Input High Voltage		●	2			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	0V < V_{IN} < V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
V_{CT}	Timing Capacitor Threshold Voltage	V_S = 5V V_S = 12V		2.1 2.0	2.5 2.6	2.9 3.2	V V
I_{CT}	Timing Capacitor Current	V_S = 12V		3.0	4.2	6.0	µA
V_{SDH}	Shutdown Input High Voltage		●	2			V
V_{SDL}	Shutdown Input Low Voltage		●			0.8	V
I_{SD}	Shutdown Input Current	0V < V_{IN} < V_S	●			±1	µA
V_{SEN}	Drain Sense Threshold Voltage		 ●	80 75	100 100	120 125	mV mV
I_{SEN}	Drain Sense Input Current	0V < V_{SEN} < V_S	●			±0.1	µA

ELECTRICAL CHARACTERISTICS

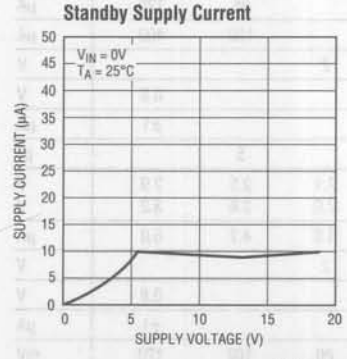
V_S = 4.5V to 18V, T_A = 25°C, C_T = 0.1µF, V_{SD} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1153C MIN	LTC1153C TYP	LTC1153C MAX	UNITS
$V_{GATE} - V_S$	Gate Voltage Above Supply	V_S = 5V	●	6.0	7.0	9.0	V
		V_S = 6V	●	7.5	8.3	15.0	V
		V_S = 12V	●	15.0	18.0	25.0	V
V_{STAT}	Status Output Low Voltage	I_{STAT} = 400µA	●		0.05	0.4	V
I_{STAT}	Status Output Leakage Current	V_{STAT} = 12V	●			1	µA
t_{ON}	Turn-ON Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 2V$		30	110	300	µs
		Time for $V_{GATE} > V_S + 5V$		100	450	1000	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 5V$		20	80	200	µs
		Time for $V_{GATE} > V_S + 10V$		50	160	500	µs
t_{OFF}	Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		10	36	60	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		10	28	60	µs
t_{TD}	Minimum Trip Delay	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		5	25	40	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		5	23	40	µs
t_{SD}	Shutdown Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$			17	40	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$			13	35	µs

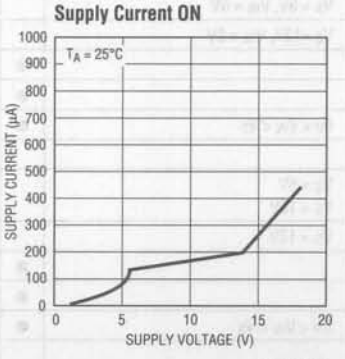
The ● denotes specifications which apply over the operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

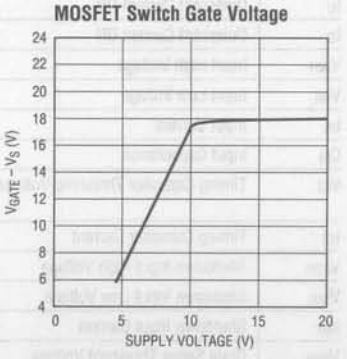
Standby Supply Current



Supply Current ON

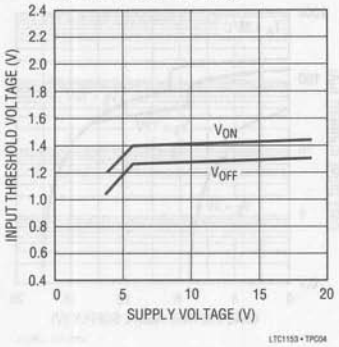


MOSFET Switch Gate Voltage

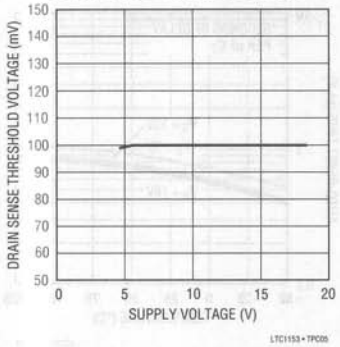


TYPICAL PERFORMANCE CHARACTERISTICS

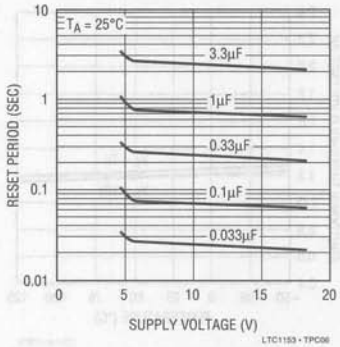
Input Threshold Voltage



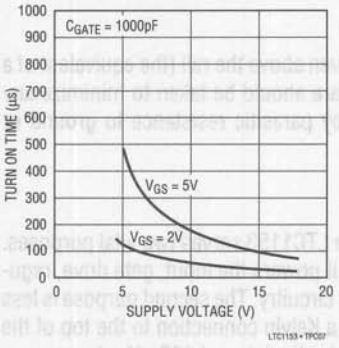
Drain Sense Threshold Voltage



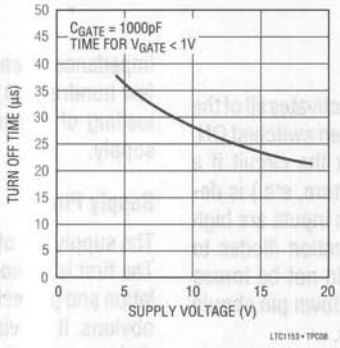
Auto-Reset Period



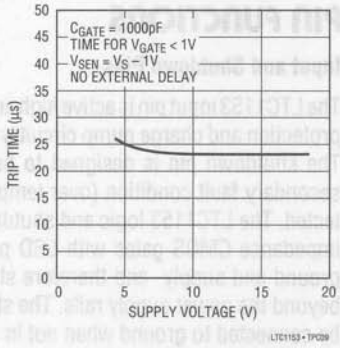
MOSFET Gate Turn-ON Time



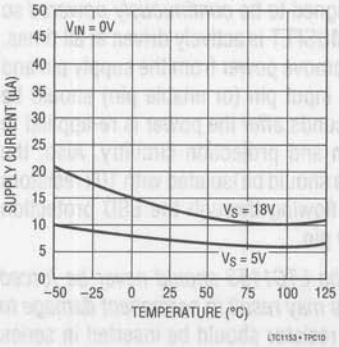
MOSFET Gate Turn-OFF Time



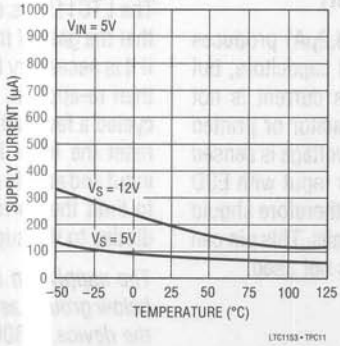
Built-In Trip Delay



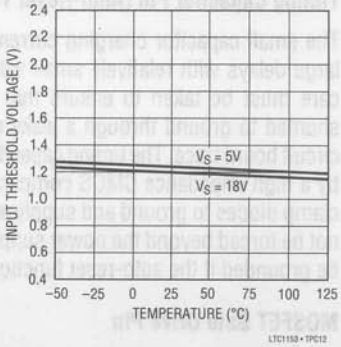
Standby Supply Current



Supply Current ON



Input ON Threshold Voltage



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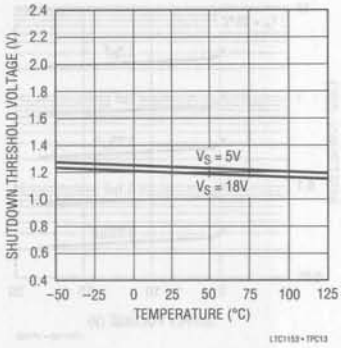
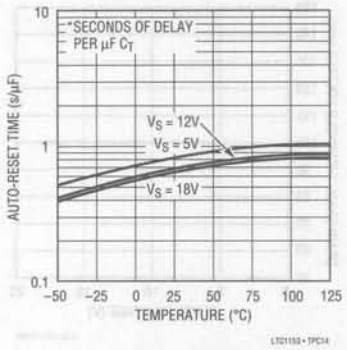
TYPICAL PERFORMANCE CHARACTERISTICS

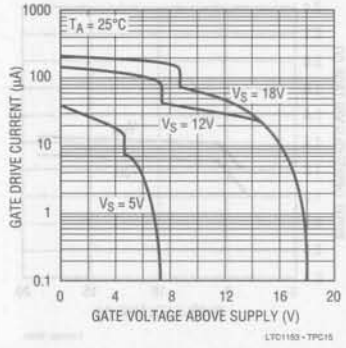
Shutdown Threshold Voltage



Auto-Reset Time*



MOSFET Gate Drive Current



PIN FUNCTIONS

Input and Shutdown Pins

The LTC1153 input pin is active high and activates all of the protection and charge pump circuitry when switched ON. The shutdown pin is designed to break the circuit if a secondary fault condition (over temperature, etc.) is detected. The LTC1153 logic and shutdown inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails. The shutdown pin should be connected to ground when not in use.

Timing Capacitor Pin (Auto-Reset Timer)

The small capacitor charging current (4.2µA) produces large delays with relatively small valued capacitors, but care must be taken to ensure that this current is not shunted to ground through a leaky capacitor or printed circuit board trace. The timing capacitor voltage is sensed by a high impedance CMOS comparator input with ESD clamp diodes to ground and supply and therefore should not be forced beyond the power supply rails. This pin can be grounded if the auto-reset function is not used.

MOSFET Gate Drive Pin

The MOSFET gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1153 serves two vital purposes. The first is obvious: it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious: it provides a Kelvin connection to the top of the drain sense resistor for the internal 100mV reference.

The LTC1153 is designed to be *continuously powered* so that the gate of the MOSFET is actively driven at all times. If it is necessary to remove power from the supply pin and then re-apply it, the input pin (or enable pin) should be cycled a few milliseconds *after* the power is re-applied to reset the input latch and protection circuitry. Also, the input and enable pins should be isolated with 10k resistors to limit the current flowing through the ESD protection diodes to the supply pin.

The supply pin of the LTC1153 should never be forced below ground as this may result in permanent damage to the device. A 300Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

PIN FUNCTIONS

Drain Sense Pin

The drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will trip and the MOSFET switch will be turned off.

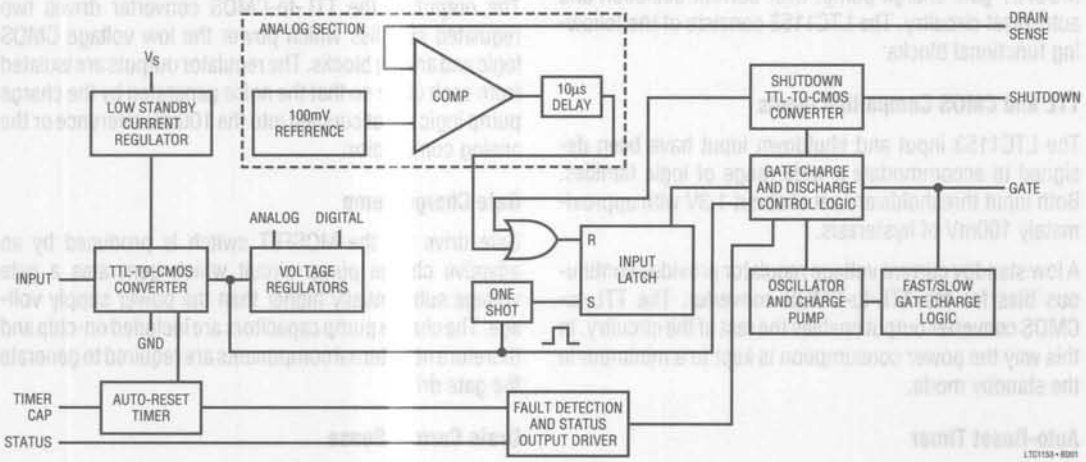
This pin is also a high impedance CMOS gate with ESD protection and therefore should not be forced beyond the power supply rails.

Some loads, such as large supply capacitor, lamps, or motors require high inrush currents. An RC time is added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false trigger during start-up. This trip delay can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET switch in risk of being destroyed by a short-circuit condition. (see Applications Information Section).

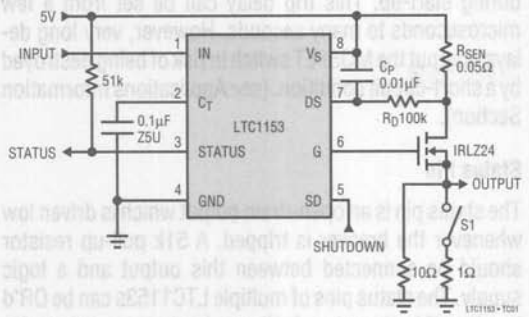
Status Pin

The status pin is an open-drain output which is driven low whenever the breaker is tripped. A 51k pull-up resistor should be connected between this output and a logic supply. The status pins of multiple LTC1153s can be OR'd together if independent fault sensing is not required. No connection is required to this pin when not in use.

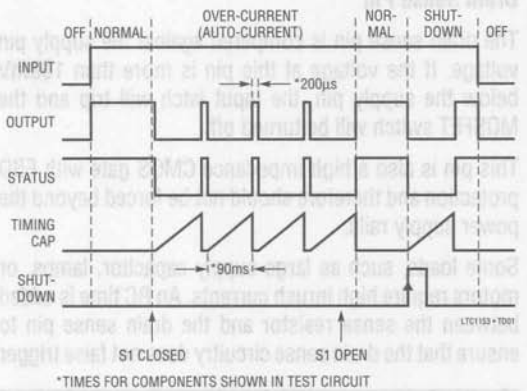
BLOCK DIAGRAM



TEST CIRCUIT



TIMING DIAGRAM



*TIMES FOR COMPONENTS SHOWN IN TEST CIRCUIT

LTC1153 OPERATION

The LTC1153 is an electronic circuit breaker with built-in MOSFET gate charge pump, over-current detection and auto-reset circuitry. The LTC1153 consists of the following functional blocks:

TTL and CMOS Compatible Inputs

The LTC1153 input and shutdown input have been designed to accommodate a wide range of logic families. Both input thresholds are set at about 1.3V with approximately 100mV of hysteresis.

A low standby current voltage regulator provides continuous bias for the TTL-to-CMOS converter. The TTL-to-CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

Auto-Reset Timer

An external timing capacitor, C_T, is ramped up by a small current whenever a fault is detected, i.e., the switch latched off. When the timing capacitor ramps up to approximately 2.5V, the switch is turned back on and the timing capacitor discharged. If the circuit breaker output is still in an overload state, the breaker will latch off and this cycle will continue until the fault condition is removed.

Internal Voltage Regulation

The output of the TTL-to-CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the MOSFET switch is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and therefore no external components are required to generate the gate drive.

Drain Current Sense

The LTC1153 is configured to sense the current flowing into the drain of an N-channel MOSFET switch. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.10Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged via a relatively large N-channel transistor.

LTC1153 OPERATION

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions in normal operation. If a short-circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

Status Output Driver

The status circuitry continuously monitors the input and the gate charge control logic. The open-drain output is driven low when the input is turned ON and the breaker is latched off. The status circuitry is reset along with the input latch when the auto-reset circuitry retries the breaker or the input is cycled low.

APPLICATIONS INFORMATION

MOSFET and Load Protection

The LTC1153 protects the power MOSFET switch by removing drive from the gate as soon as an over-current condition is detected and breaking the circuit to the load. Resistive and inductive loads can be protected with no external time delay in series with the drain sense pin. High inrush current loads, however, require that the trip delay time be set long enough to start the load but short enough to ensure the safety of the MOSFET.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET switch or the load is subjected to an overload condition. The drain sense circuitry has a built-in trip delay of approximately 10μs to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to "mask" short load current transients and the starting of a small capacitor (<1μF) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 1.

Inductive Loads

Loads that are primarily inductive, such as relays, solenoids and stepper motor windings should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The built-in 10μs trip delay will ensure that the breaker is not false-tripped by a supply or load transient. No external delay components are required as shown in Figure 2.

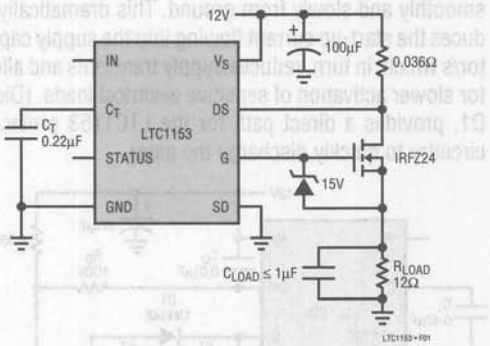


Figure 1. Protecting Resistive Loads

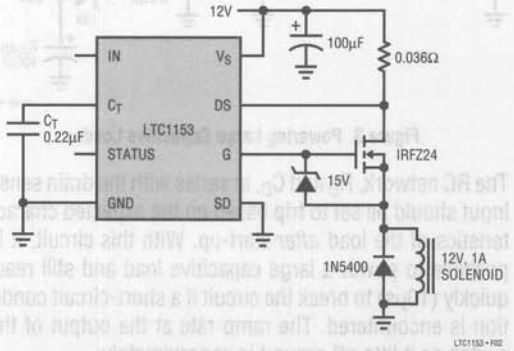


Figure 2. Protecting Inductive Loads

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating

APPLICATIONS INFORMATION

should be connected across the load, as shown in Figure 2, to safely divert the stored energy.

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 3. The gate drive to the power MOSFET switch is passed through an RC delay network, R1 and C1, which greatly reduces the turn on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the start-up current flowing into the supply capacitor/s which, in turn, reduces supply transients and allows for slower activation of sensitive electrical loads. (Diode, D1, provides a direct path for the LTC1153 protection circuitry to quickly discharge the gate).

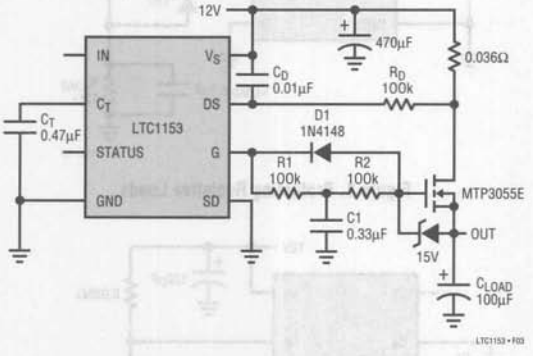


Figure 3. Powering Large Capacitive Loads

The RC network, R_D and C_D, in series with the drain sense input should be set to trip based on the expected characteristics of the load *after* start-up. With this circuit, it is possible to power a large capacitive load and still react quickly (10µs) to break the circuit if a short-circuit condition is encountered. The ramp rate at the output of the switch as it lifts off ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH})/(R1 \times C1)$$

And therefore the current flowing into the capacitor during start-up is approximately:

$$I_{START\text{-}UP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 3, the start-up current is less than 100mA and does not false-trip the breaker.

Lamp Loads

The inrush current created by a lamp during turn-on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 4 shifts the trip threshold up by a factor of 11:1 (to 30A) for 100ms while the bulb is turned on. The trip threshold then drops down to 2.7A after the inrush current has subsided.

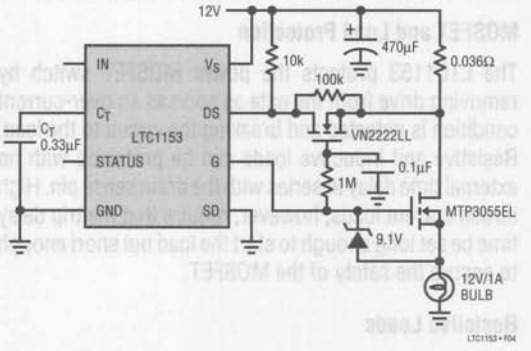


Figure 4. Lamp Driver with Delayed Protection

Selecting R_D and C_D

Figure 5 is a graph of normalized breaker trip time versus breaker current. This graph is used to select the two delay components, R_D and C_D, which make up a simple RC delay between the drain sense resistor and the drain sense input.

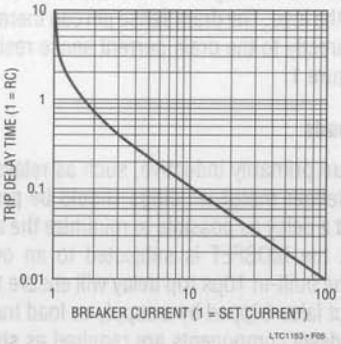


Figure 5. Trip Delay Time vs Breaker Current

APPLICATIONS INFORMATION

The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the set current. (The set current is defined as the current required to develop 100mV across the drain sense resistor).

Note that the trip delay time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the manufacturer for safe operation. (See MOSFET data sheet for further S.O.A. information).

Using a Speed-Up Diode

Another way to reduce the trip delay time is to "bypass" the delay resistor with a small signal diode as shown in Figure 6. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the trip delay time. The drain sense resistor value is selected to limit the maximum DC breaker current to 4A.

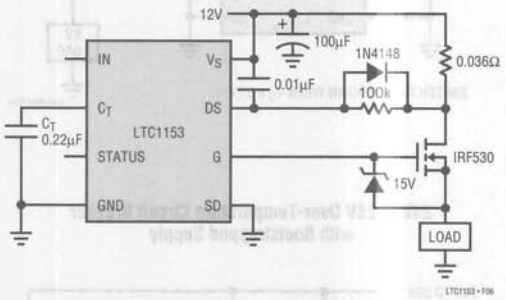


Figure 6. Using a Speed-Up Diode

Reverse Battery Protection

The LTC1153 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 7. The resistor limits the supply current to less than 50mA with –12V applied. Since the LTC1153 draws very little current while in normal operation, the drop across the ground resistor is minimal. the 5V µP (or control logic) is protected by the 10k resistors in series with the input and status pins.

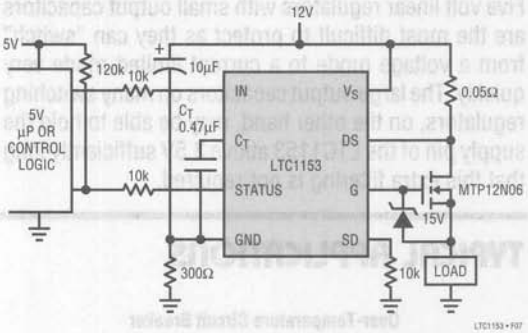


Figure 7. Reverse Battery Protection

Current Limited Power Supplies

The LTC1153 requires at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply to the LTC1153 be held higher than 3.5V at all times, even when the output of the switch is short circuited to ground. The output voltage of a current limited regulator may drop very quickly during short-circuit and pull the supply pin of the LTC1153 below 3.5V before the shut-down circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should be added as shown in Figure 8 which holds the supply pin of the LTC1153 high long enough for the over-current shutdown circuitry to respond and fully discharge the gate, i.e., break the circuit.

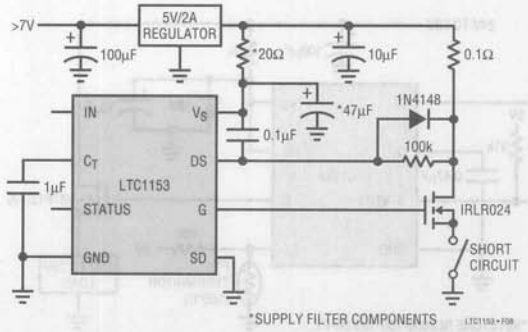


Figure 8. Supply Filter for Current Limited Supplies

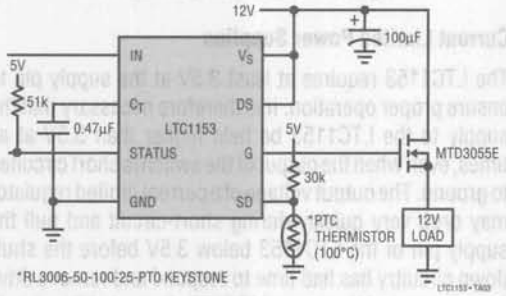
APPLICATIONS INFORMATION

Five volt linear regulators with small output capacitors are the most difficult to protect as they can "switch" from a voltage mode to a current limited mode very quickly. The large output capacitors on many switching regulators, on the other hand, may be able to hold the supply pin of the LTC1153 above 3.5V sufficiently long that this extra filtering is not required.

Because the LTC1153 is micropower in both the standby and ON state, the voltage drop across the supply filter is less than 2mV, and does not significantly alter the accuracy of the 100mV drain sense threshold voltage.

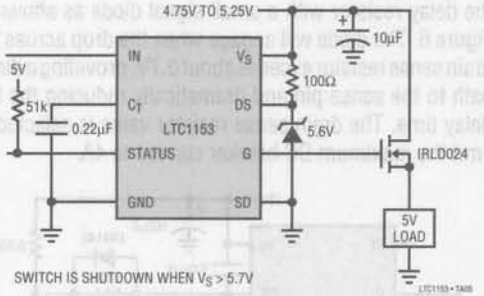
TYPICAL APPLICATIONS

Over-Temperature Circuit Breaker



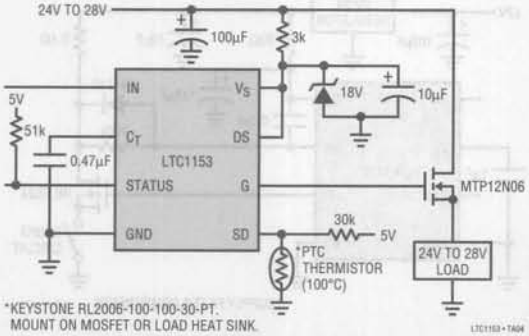
*RL3006-50-100-25-PTO KEYSTONE

Over-Voltage Circuit Breaker



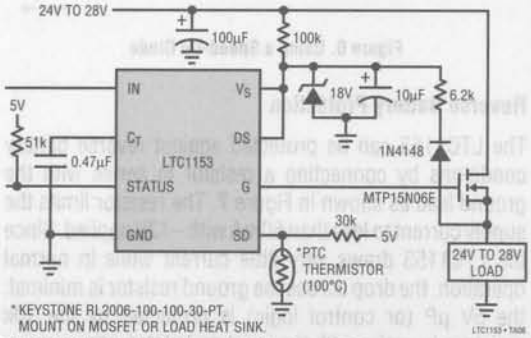
SWITCH IS SHUTDOWN WHEN $V_S > 5.7V$

24V to 28V Over-Temperature Circuit Breaker



*KEYSTONE RL2006-100-100-30-PT.
MOUNT ON MOSFET OR LOAD HEAT SINK.

24V to 28V Over-Temperature Circuit Breaker with Bootstrapped Supply

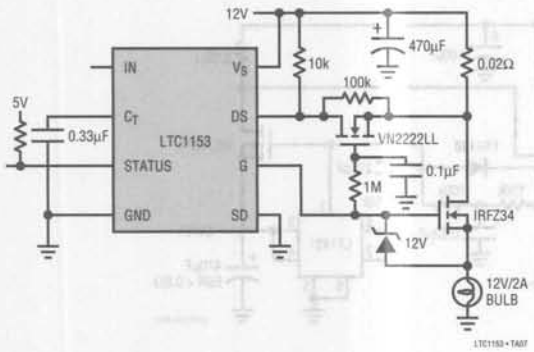


*KEYSTONE RL2006-100-100-30-PT.
MOUNT ON MOSFET OR LOAD HEAT SINK.

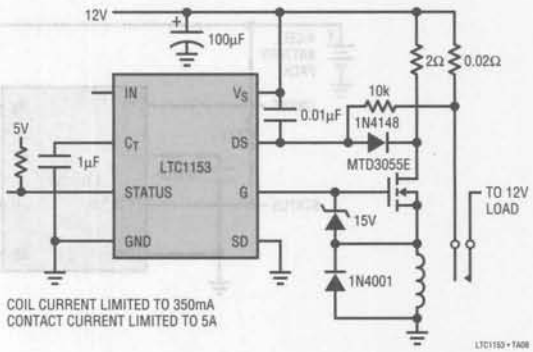
** BOOTSTRAPPING REDUCES $I_{Q(OFF)}$ TO 60µA, $I_{Q(ON)}$ = 1mA.

TYPICAL APPLICATIONS

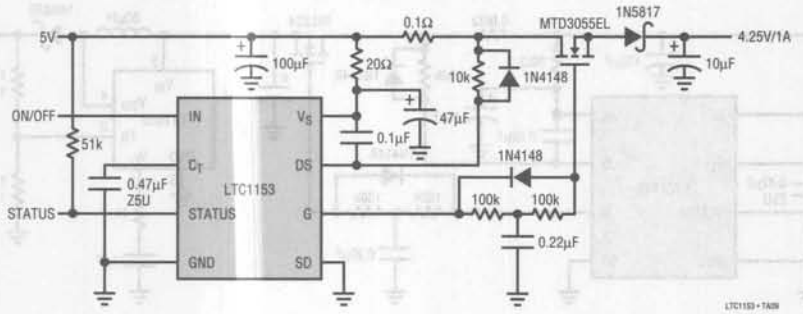
12V Lamp Driver/Circuit Breaker with Auto-Reset



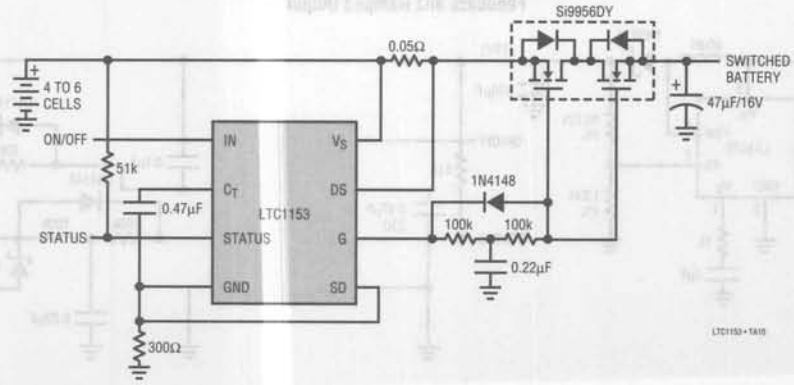
Relay Driver with Over-Current Protection and Status Feedback



SCSI Termination Power 1A Circuit Breaker with Auto-Reset and Ramped Turn-On

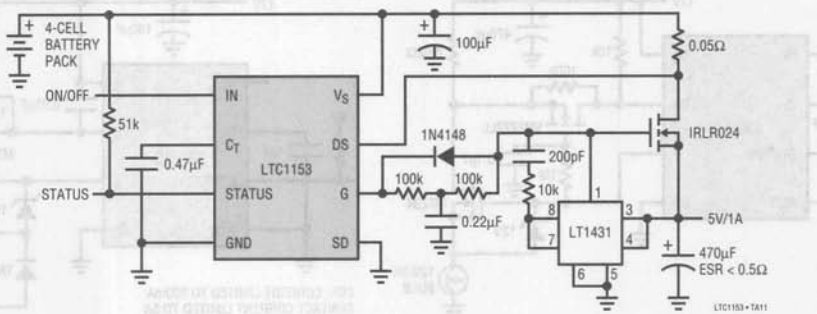


Logic Controlled Battery Switch with Reverse Battery Protection, Ramped Turn-On and 10µA Standby Current

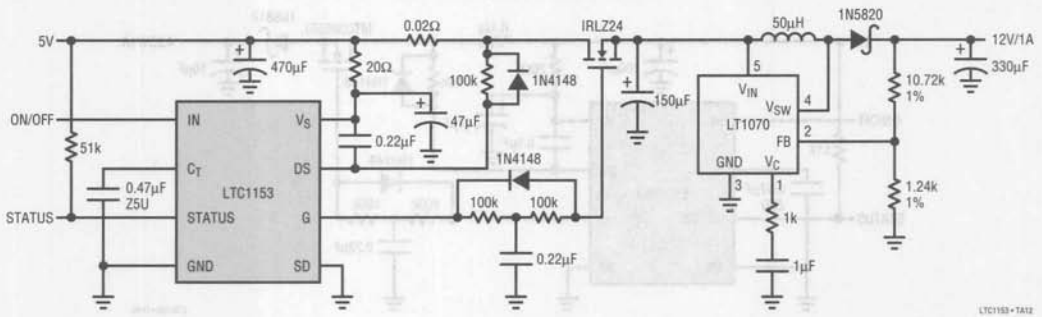


TYPICAL APPLICATIONS

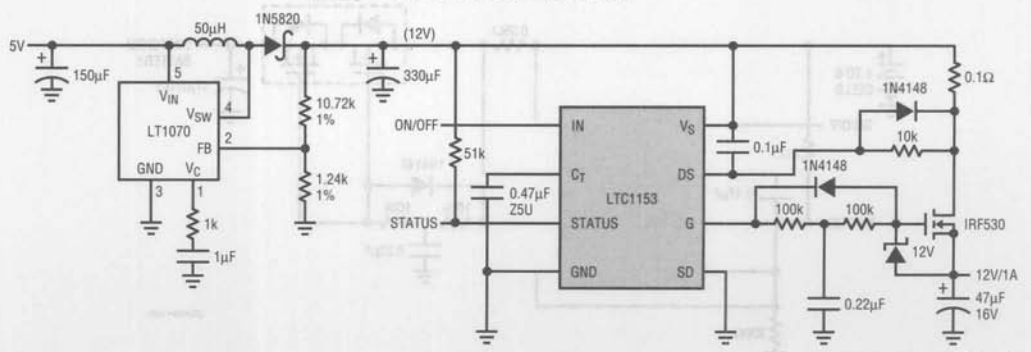
"4 Cell-to-5V" Regulator with 2A Current Limit, Auto-Reset, Ramped Turn-On and 10μA Standby Current



12V Step-Up Regulator with Soft Start, Auto-Reset Circuit Breaker (Pre-Regulator), Status Feedback and 10μA Standby Current

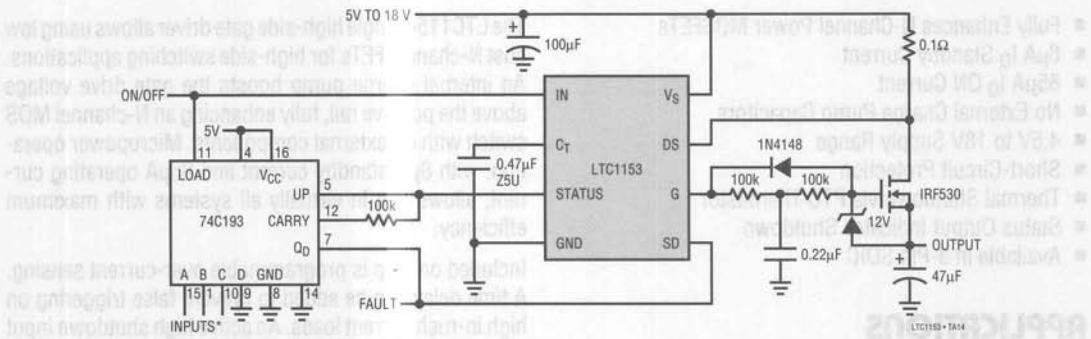


12V Step-Up Regulator with 1A Circuit Breaker (Post Regulator), Breaker Status Feedback and Ramped Output



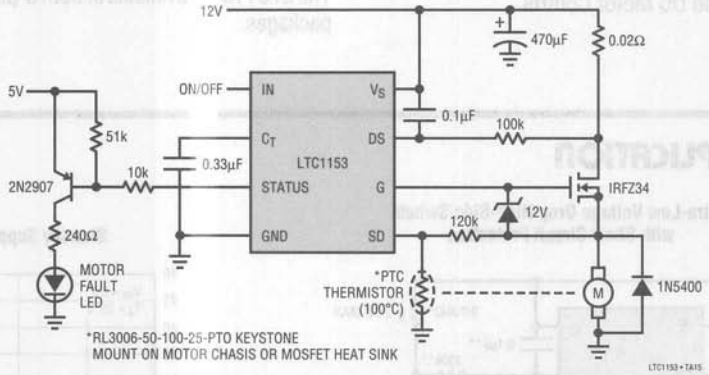
TYPICAL APPLICATIONS

Auto-Reset Circuit Breaker with Programmable (1-6) Number of Retries Using Binary Counter



*SET WITH 3-BIT BINARY WORD = 7 – N

DC Motor Driver with Stall-Current Circuit Breaking (Auto-Reset), Thermal Overload Shutdown and 10µA Standby Current



4

High-Side Micropower MOSFET Driver

FEATURES

- Fully Enhances N-Channel Power MOSFETs
- 8μA I_Q Standby Current
- 85μA I_Q ON Current
- No External Charge Pump Capacitors
- 4.5V to 18V Supply Range
- Short-Circuit Protection
- Thermal Shutdown via PTC Thermistor
- Status Output Indicates Shutdown
- Available in 8-Pin SOIC

APPLICATIONS

- Laptop Computer Power Switching
- SCSI Termination Power Switching
- Cellular Telephone Power Management
- Battery Charging and Management
- High-Side Industrial and Automotive Switching
- Stepper Motor and DC Motor Control

DESCRIPTION

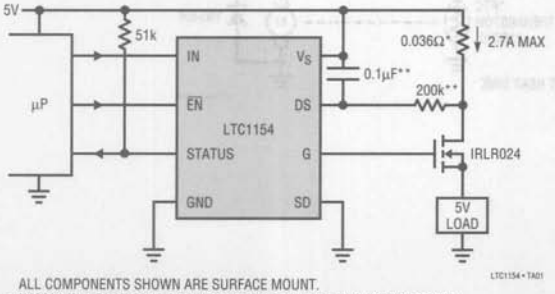
The LTC1154 single high-side gate driver allows using low cost N-channel FETs for high-side switching applications. An internal charge pump boosts the gate drive voltage above the positive rail, fully enhancing an N-channel MOS switch with no external components. Micropower operation, with 8μA standby current and 85μA operating current, allows use in virtually all systems with maximum efficiency.

Included on chip is programmable over-current sensing. A time delay can be added to prevent false triggering on high in-rush current loads. An active high shutdown input is also provided and interfaces directly to a standard PTC thermistor for thermal shutdown. An open-drain output is provided to report switch status to the μP. An active low enable input is provided to control multiple switches in banks.

The LTC1154 is available in both 8-pin DIP and 8-pin SOIC packages.

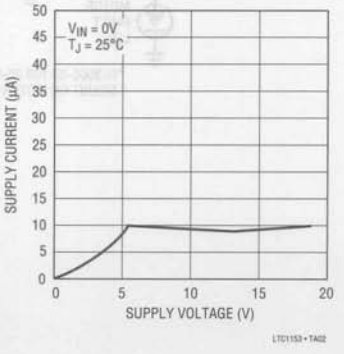
TYPICAL APPLICATION

Ultra-Low Voltage Drop High-Side Switch with Short-Circuit Protection



ALL COMPONENTS SHOWN ARE SURFACE MOUNT.
* IMS026 INTERNATIONAL MANUFACTURING SERVICE, INC. (401) 683-9700
** NOT REQUIRED IF LOAD IS RESISTIVE OR INDUCTIVE.

Standby Supply Current



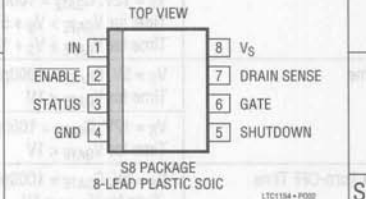
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Input Voltage ..... (V_S + 0.3V) to (GND – 0.3V)
Enable Input Voltage ..... (V_S + 0.3V) to (GND – 0.3V)
Gate Voltage ..... (V_S + 24V) to (GND – 0.3V)
Status Output Voltage 15V
Current (Any Pin) 50mA
Operating Temperature
LTC1154C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LTC1154CN8



T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	S8 PART MARKING
LTC1154CS8	1154

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 4.5V to 18V, T_A = 25°C, $V_{\overline{EN}}$ = 0V, V_{SD} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1154C MIN	LTC1154C TYP	LTC1154C MAX	UNITS
V_S	Supply Voltage		●	4.5		18.0	V
I_Q	Quiescent Current OFF	V_S = 5V, V_{IN} = 0V			8	20	µA
I_Q	Quiescent Current ON	V_S = 5V, V_{IN} = 5V			85	120	µA
I_Q	Quiescent Current ON	V_S = 12V, V_{IN} = 5V			180	400	µA
V_{INH}	Input High Voltage		●	2			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	0V < V_{IN} < V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
$V_{\overline{ENH}}$	$\overline{ENABLE}$ Input High Voltage		●	3.5	2.6		V
$V_{\overline{ENL}}$	$\overline{ENABLE}$ Input Low Voltage		●		1.0	0.6	V
$I_{\overline{EN}}$	$\overline{ENABLE}$ Input Current	0V < V_{IN} < V_S	●			±1	µA
V_{SDH}	Shutdown Input High Voltage		●	2			V
V_{SDL}	Shutdown Input Low Voltage		●			0.8	V
I_{SD}	Shutdown Input Current	0V < V_{IN} < V_S	●			±1	µA
V_{SEN}	Drain Sense Threshold Voltage		 ●	80 75	100 100	120 125	mV mV
I_{SEN}	Drain Sense Input Current	0V < V_{SEN} < V_S	●			±0.1	µA

ELECTRICAL CHARACTERISTICS

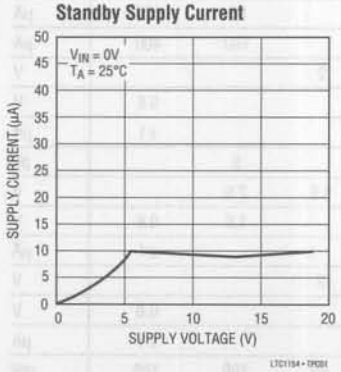
V_S = 4.5V to 18V, T_A = 25°C, $V_{\overline{EN}}$ = 0V, V_{SD} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1154C MIN	LTC1154C TYP	LTC1154C MAX	UNITS
$V_{GATE} - V_S$	Gate Voltage Above Supply	V_S = 5V	●	6.0	7.0	9.0	V
		V_S = 6V	●	7.5	8.3	15.0	V
		V_S = 12V	●	15.0	18.0	25.0	V
V_{STAT}	Status Output Low Voltage	I_{STAT} = 400µA	●		0.05	0.4	V
I_{STAT}	Status Output Leakage Current	V_{STAT} = 12V	●			1	µA
t_{ON}	Turn-ON Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 2V$		30	110	300	µs
		Time for $V_{GATE} > V_S + 5V$		100	450	1000	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 5V$		20	80	200	µs
		Time for $V_{GATE} > V_S + 10V$		50	160	500	µs
t_{OFF}	Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		10	36	60	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		10	28	60	µs
t_{SC}	Short-Circuit Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		5	25	40	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$		5	23	40	µs
t_{SD}	Shutdown Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$			17	40	µs
		V_S = 12V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 1V$			13	35	µs

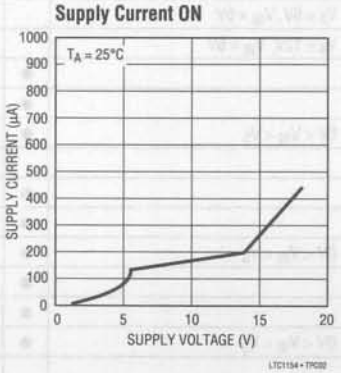
The ● denotes specifications which apply over the operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

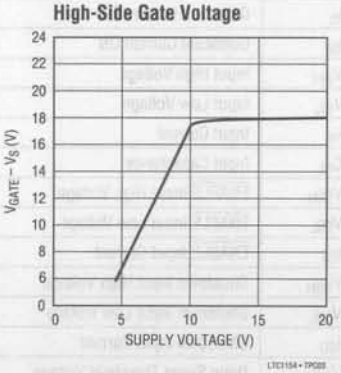
Standby Supply Current



Supply Current ON

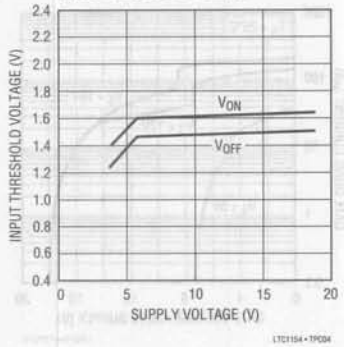


High-Side Gate Voltage

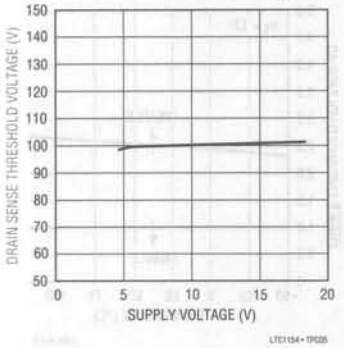


TYPICAL PERFORMANCE CHARACTERISTICS

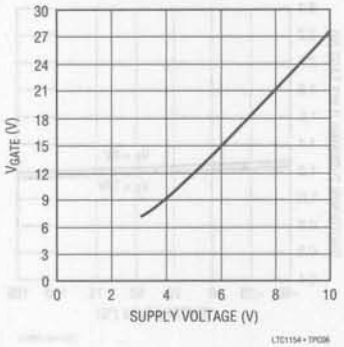
Input Threshold Voltage



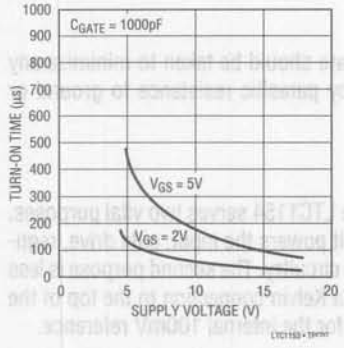
Drain Sense Threshold Voltage



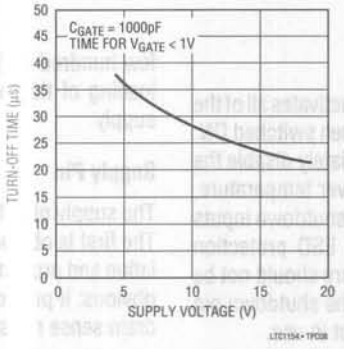
Low-Side Gate Voltage



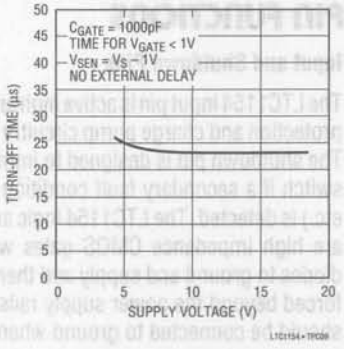
Turn-ON Time



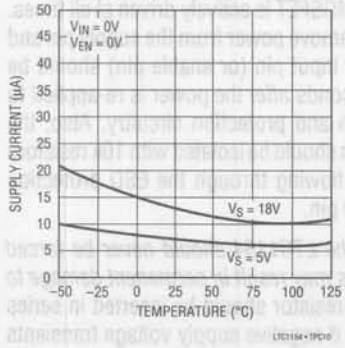
Turn-OFF Time



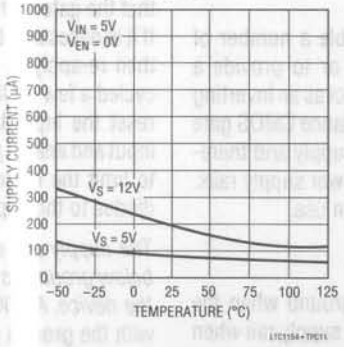
Short-Circuit Turn-OFF Delay Time



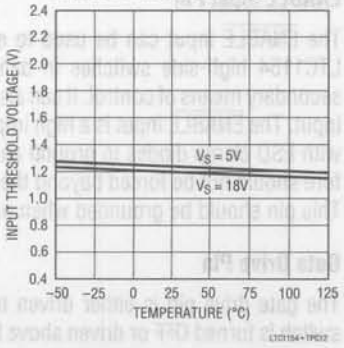
Standby Supply Current



Supply Current ON



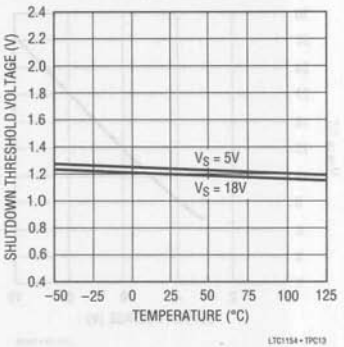
Input ON Threshold Voltage



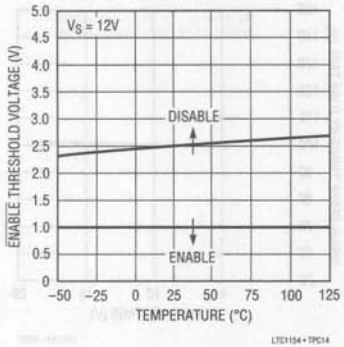
4

TYPICAL PERFORMANCE CHARACTERISTICS

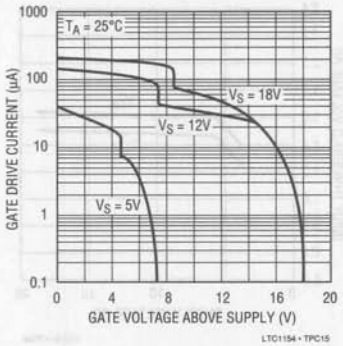
Shutdown Threshold Voltage



$\overline{\text{ENABLE}}$ Threshold Voltage



Gate Drive Current



PIN FUNCTIONS

Input and Shutdown Pins

The LTC1154 input pin is active high and activates all of the protection and charge pump circuitry when switched ON. The shutdown pin is designed to immediately disable the switch if a secondary fault condition (over temperature, etc.) is detected. The LTC1154 logic and shutdown inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails. The shutdown pin should be connected to ground when not in use.

$\overline{\text{ENABLE}}$ Input Pin

The $\overline{\text{ENABLE}}$ input can be used to enable a number of LTC1154 high-side switches in banks or to provide a secondary means of control. It can also act as an inverting input. The $\overline{\text{ENABLE}}$ input is a high impedance CMOS gate with ESD clamp diodes to ground and supply and therefore should not be forced beyond the power supply rails. This pin should be grounded when not in use.

Gate Drive Pin

The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1154 serves two vital purposes. The first is obvious: it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious: it provides a Kelvin connection to the top of the drain sense resistor for the internal 100mV reference.

The LTC1154 is designed to be continuously powered so that the gate of the MOSFET is actively driven at all times. If it is necessary to remove power from the supply pin and then re-apply it, the input pin (or enable pin) should be cycled a few milliseconds *after* the power is re-applied to reset the input latch and protection circuitry. Also, the input and enable pins should be isolated with 10k resistors to limit the current flowing through the ESD protection diodes to the supply pin.

The supply pin of the LTC1154 should never be forced below ground as this may result in permanent damage to the device. A 300Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

PIN FUNCTIONS

Drain Sense Pin

The drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input, or $\overline{\text{ENABLE}}$ input, to reset the short-circuit latch and turn the MOSFET back on.

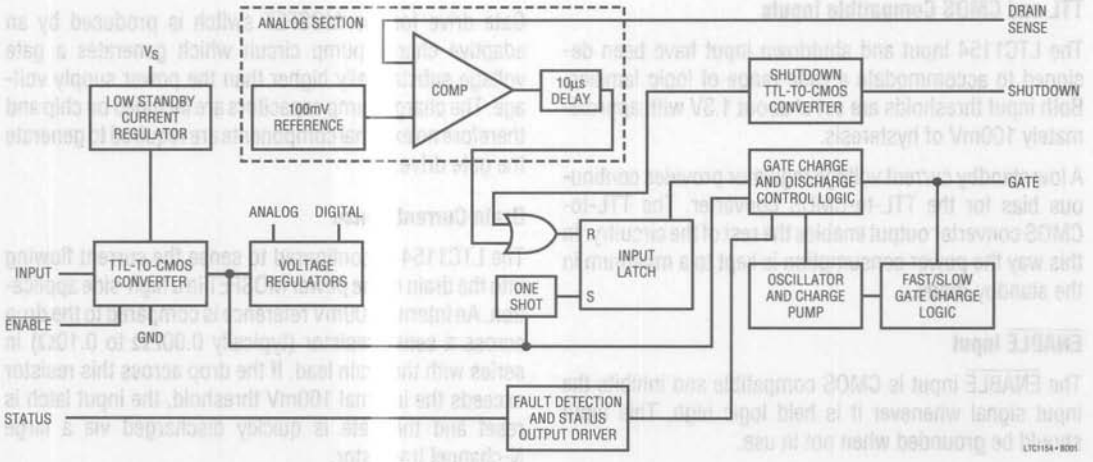
This pin is also a high impedance CMOS gate with ESD protection and therefore should not be forced beyond the power supply rails. To defeat the over current protection, short the drain sense to supply.

Some loads, such as large supply capacitors, lamps, or motors require high in-rush currents. An RC time delay can be added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false-trigger during start-up. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET in risk of being destroyed by a short-circuit condition. (see Applications Information Section).

Status Pin

The status pin is an open-drain output which is driven low whenever a fault condition is detected. A 51k pull-up resistor should be connected between this output and a logic supply. The status pins of multiple LTC1154s can be OR'd together if independent fault sensing is not required. No connection is required to this pin when not in use.

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS		SWITCH CONDITION
IN	$\overline{EN}$	SD	GATE	STATUS	
X	H	X	L	H	SWITCH OFF
L	X	X	L	H	SWITCH OFF
H	L	L	H	H	SWITCH ON
H	L	L	L	L	SWITCH LATCHED OFF (OVER CURRENT)
H	L	⌐¯_	L	L	SWITCH LATCHED OFF (SHUTDOWN)

L = LOGIC LOW
H = LOGIC HIGH
X = IRRELEVANT
⌐¯_ = EDGE TRIGGERED

The Truth Table demonstrates how the LTC1154 receives inputs and returns status information to the µP. The $\overline{ENABLE}$ and input signal from the µP controls the switch in its normal operating mode, where the rise and fall time of the gate drive are controlled to limit EMI and RFI emissions. The shutdown and over-current detection circuitry however, switch the gate off at a much higher rate to limit the exposure of the MOSFET switch and the load to dangerous conditions. The status pin remains high as long as the switch is operating normally, and is driven low only when a fault condition is detected. Note that the shutdown pin is edge-sensitive and latches the output off even if the shutdown pin returns to a low state.

LTC1154 OPERATION

The LTC1154 is a single micropower MOSFET driver with built-in protection, status feedback and gate charge pump. The LTC1154 consists of the following functional blocks:

TTL and CMOS Compatible Inputs

The LTC1154 input and shutdown input have been designed to accommodate a wide range of logic families. Both input thresholds are set at about 1.3V with approximately 100mV of hysteresis.

A low standby current voltage regulator provides continuous bias for the TTL-to-CMOS converter. The TTL-to-CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

$\overline{ENABLE}$ Input

The $\overline{ENABLE}$ input is CMOS compatible and inhibits the input signal whenever it is held logic high. This input should be grounded when not in use.

Internal Voltage Regulation

The output of the TTL-to-CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the MOSFET switch is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and therefore no external components are required to generate the gate drive.

Drain Current Sense

The LTC1154 is configured to sense the current flowing into the drain of the power MOSFET in a high-side application. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.10Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged via a large N-channel transistor.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have

LTC1154 OPERATION

been set to minimize RFI and EMI emissions in normal operation. If a short-circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

Status Output Driver

The status circuitry continuously monitors the fault detection logic. This open-drain output is driven low when the gate of the MOSFET is driven low by the protection circuitry. The status circuitry is reset along with the input latch when the input, or $\overline{\text{ENABLE}}$ input, is cycled.

APPLICATIONS INFORMATION

MOSFET and Load Protection

The LTC1154 protects the power MOSFET switch by removing drive from the gate as soon as an over-current condition is detected. Resistive and inductive loads can be protected with no external time delay in series with the drain sense pin. Lamp loads, however, require that the over-current protection by delayed long enough to start the lamp but short enough to ensure the safety of the MOSFET.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10µs to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to "mask" short load current transients and the starting of a small capacitor (<1µF) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 1.

Inductive Loads

Loads that are primarily inductive, such as relays, solenoids and stepper motor windings should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The built-in 10µs delay will ensure that the over-current protection is not false-triggered by a supply or load transient. No external delay components are required as shown in Figure 2.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 2, to safely divert the stored energy.

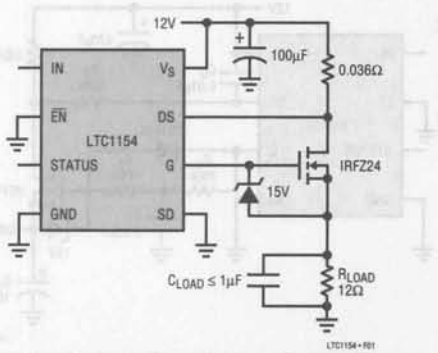


Figure 1. Protecting Resistive Loads

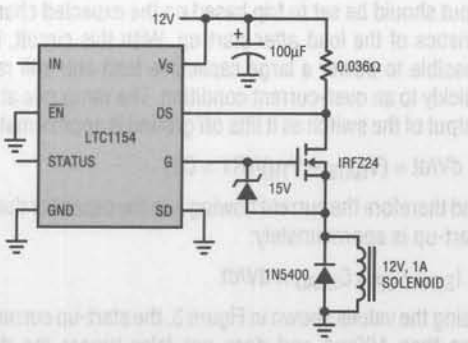


Figure 2. Protecting Inductive Loads

APPLICATIONS INFORMATION

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 3. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn-on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the start-up current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation of sensitive electrical loads. (Diode, D1, provides a direct path for the LTC1154 protection circuitry to quickly discharge the gate in the event of an over-current condition).

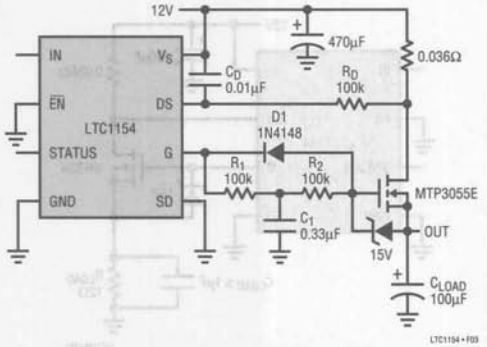


Figure 3. Powering Large Capacitive Loads

The RC network, R_D and C_D, in series with the drain sense input should be set to trip based on the expected characteristics of the load *after* start-up. With this circuit, it is possible to power a large capacitive load and still react quickly to an over-current condition. The ramp rate at the output of the switch as it lifts off ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH})/(R1 \times C1)$$

And therefore the current flowing into the capacitor during start-up is approximately:

$$I_{START\text{-}UP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 3, the start-up current is less than 100mA and does not false-trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

Lamp Loads

The in-rush current created by a lamp during turn-on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 4 shifts the current limit threshold up by a factor of 11:1 (to 30A) for 100ms when the bulb is first turned on. The current limit then drops down to 2.7A after the in-rush current has subsided.

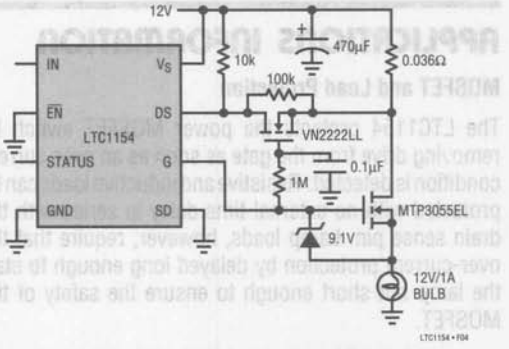


Figure 4. Lamp Driver with Delayed Protection

Selecting R_D and C_D

Figure 5 is a graph of normalized over-current shutdown time versus normalized MOSFET current. This graph is used to select the two delay components, R_D and C_D, which make up a simple RC delay between the drain sense resistor and the drain sense input.

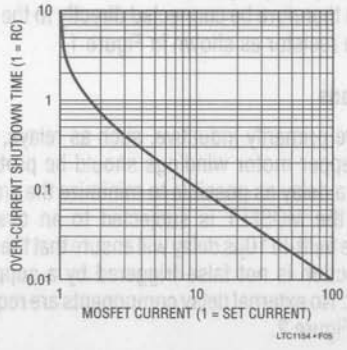


Figure 5. Over-Current Shutdown Time vs MOSFET Current

APPLICATIONS INFORMATION

The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the current. (The set current is defined as the current required to develop 100mV across the drain sense resistor).

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the manufacturer for safe operation. (See MOSFET data sheet for further information).

Using a Speed-Up Diode

To reduce the amount of time that the power MOSFET is in a short-circuit condition, "bypass" the delay resistor with a small signal diode as shown in Figure 6. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 2.8A. The diode conducts when the drain current exceeds 20A and reduces the turn-off time to 15µs.

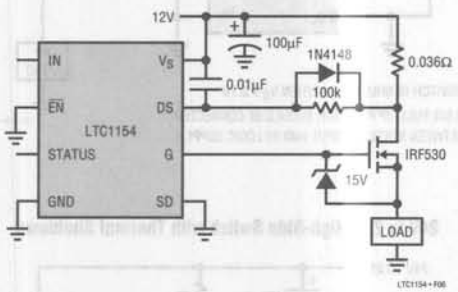


Figure 6. Using a Speed-Up Diode

Reverse Battery Protection

The LTC1154 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 7. The resistor limits the supply current to less than 50mA with –12V applied.

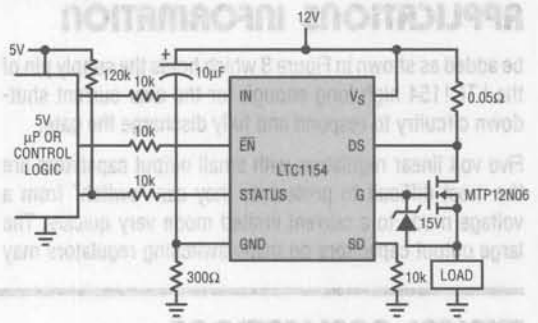


Figure 7. Reverse Battery Protection

Since the LTC1154 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V µP (or control logic) is protected by the 10k resistors in series with the input and status pins.

Current Limited Power Supplies

The LTC1154 requires at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply to the LTC1154 be held higher than 3.5V at all times, even when the output of the switch is short circuited to ground. The output voltage of a current limited regulator may drop very quickly during short circuit and pull the supply pin of the LTC1154 below 3.5V before the shutdown circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should

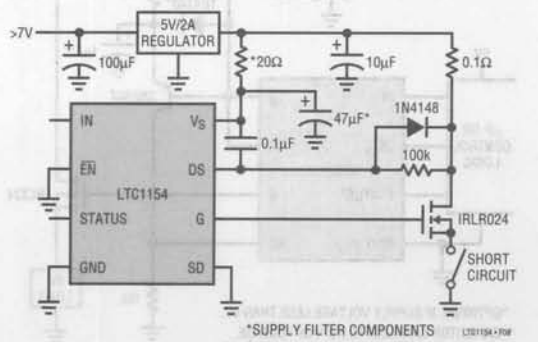


Figure 8. Supply Filter for Current Limited Supplies

APPLICATIONS INFORMATION

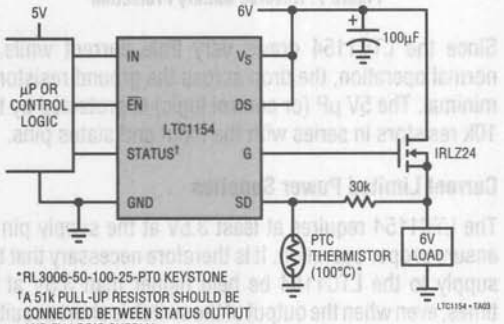
be added as shown in Figure 8 which holds the supply pin of the LTC1154 high long enough for the over-current shutdown circuitry to respond and fully discharge the gate.

Five volt linear regulators with small output capacitors are the most difficult to protect as they can "switch" from a voltage mode to a current limited mode very quickly. The large output capacitors on many switching regulators may be able to hold the supply pin of the LTC1154 above 3.5V sufficiently long that this extra filtering is not required.

Because the LTC1154 is micropower in both the standby and ON state, the voltage drop across the supply filter is less than 2mV, and does not significantly alter the accuracy of the 100mV drain sense threshold voltage.

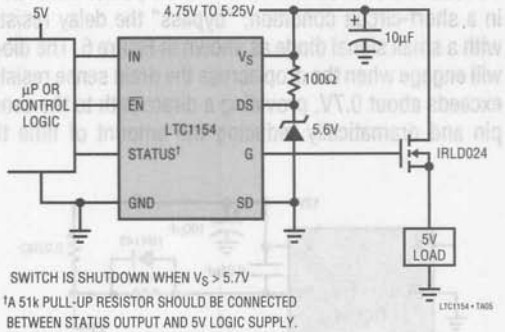
TYPICAL APPLICATIONS

High-Side Driver with Thermal Shutdown



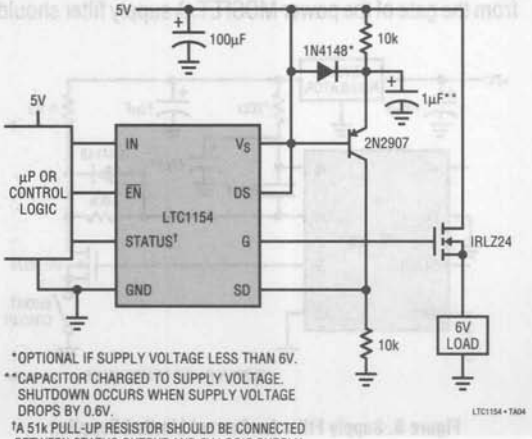
*RL3006-50-100-25-PTO KEYSTONE
†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

High-Side Driver with Over-Voltage Shutdown



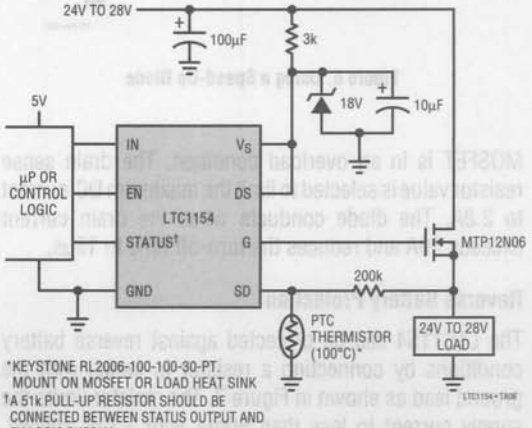
SWITCH IS SHUTDOWN WHEN V_S > 5.7V
†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

High-Side Driver with Under-Voltage Shutdown



*OPTIONAL IF SUPPLY VOLTAGE LESS THAN 6V.
**CAPACITOR CHARGED TO SUPPLY VOLTAGE. SHUTDOWN OCCURS WHEN SUPPLY VOLTAGE DROPS BY 0.6V.
†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

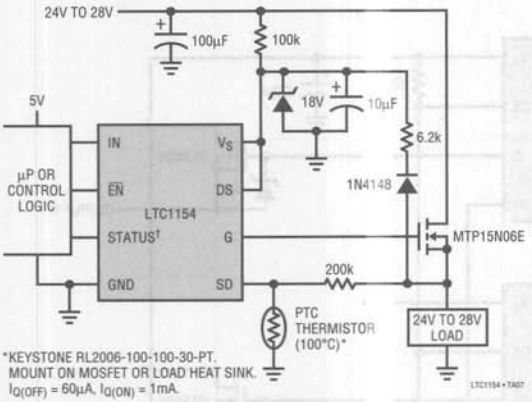
24V to 28V High-Side Switch with Thermal Shutdown



*KEYSTONE RL2006-100-100-30-PT. MOUNT ON MOSFET OR LOAD HEAT SINK
†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

TYPICAL APPLICATIONS

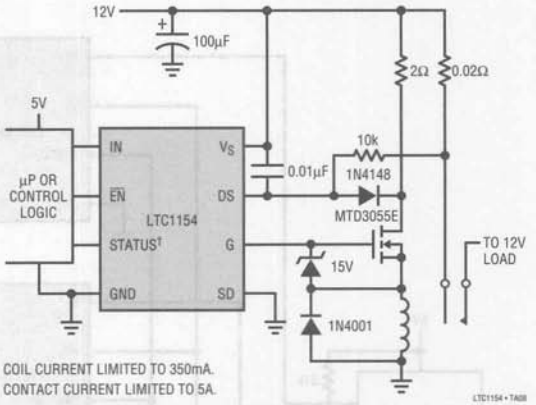
24V to 28V Switch with Bootstrapped Supply



*KEYSTONE RL2006-100-100-30-PT. MOUNT ON MOSFET OR LOAD HEAT SINK. $I_{Q(OFF)}$ = 60µA, $I_{Q(ON)}$ = 1mA.

†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

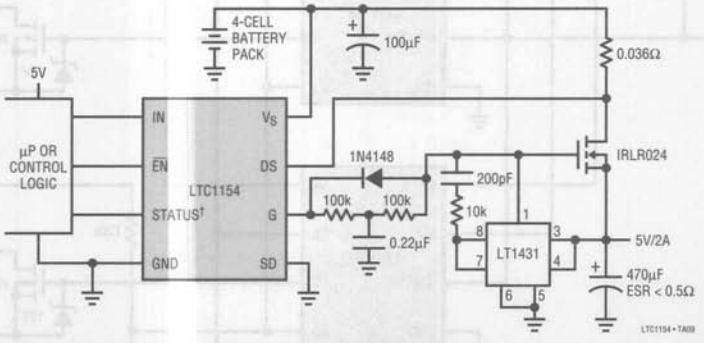
High-Side Relay Driver with Over-Current Protection and Status Feedback



COIL CURRENT LIMITED TO 350mA.
CONTACT CURRENT LIMITED TO 5A.

†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

"4-Cell-to-5V" Extremely Low Voltage Drop Regulator with Over-Current Shutdown, Status Feedback, Ramped Turn-ON and 8µA Standby Current

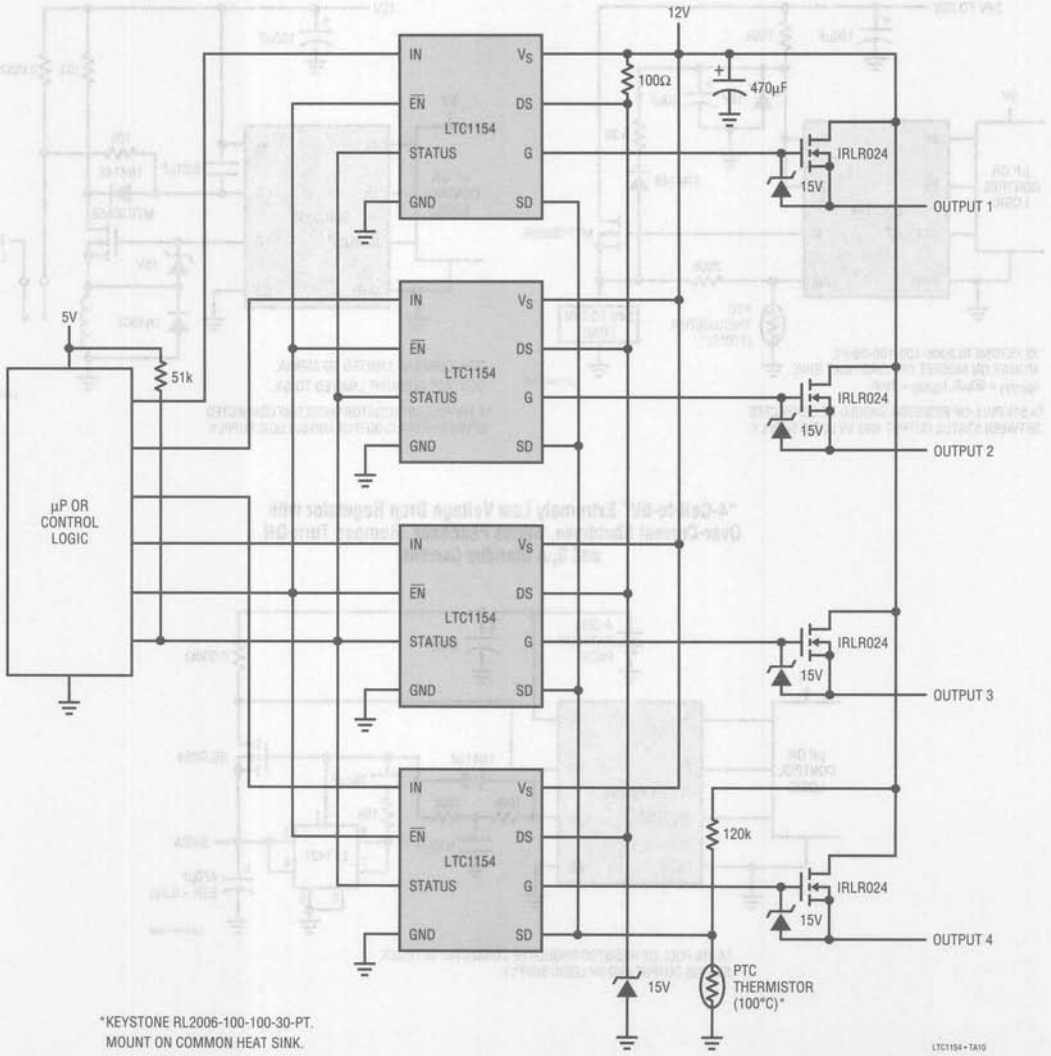


†A 51k PULL-UP RESISTOR SHOULD BE CONNECTED BETWEEN STATUS OUTPUT AND 5V LOGIC SUPPLY.

4

TYPICAL APPLICATIONS

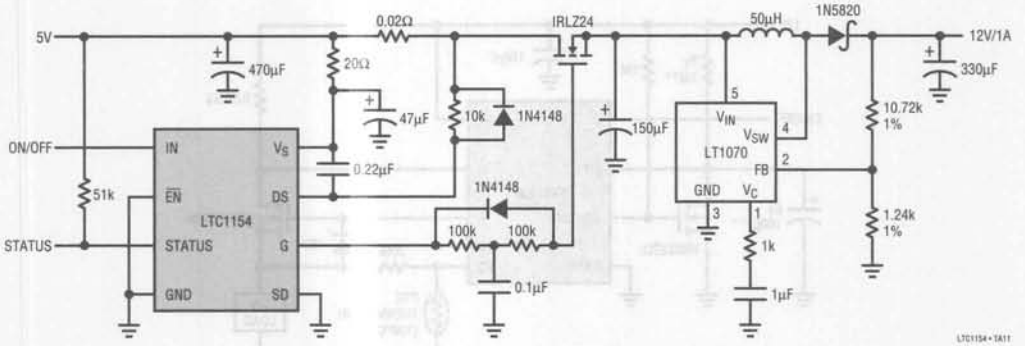
Bank Controlled High-Side Switches with "Global" Thermal and Over-Voltage Shutdown



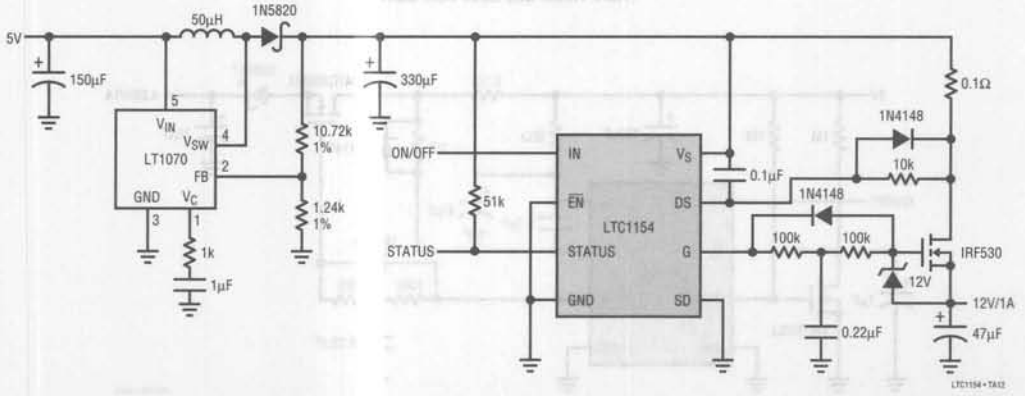
*KEYSTONE RL2006-100-100-30-PT.
MOUNT ON COMMON HEAT SINK.

TYPICAL APPLICATIONS

12V Step-Up Regulator with Ultra-Low Standby Current, Over-Current Protection and Status Feedback

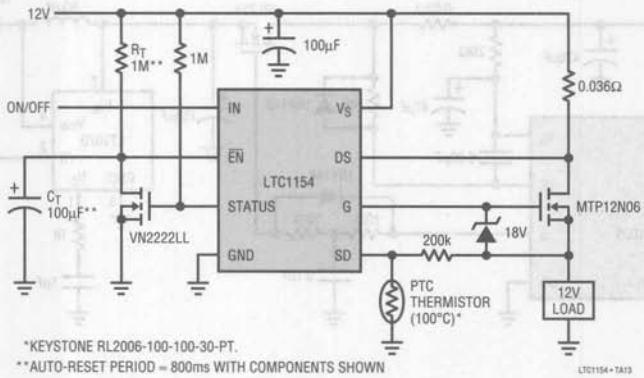


12V Step-Up Regulator with 1A Over-Current Protection, Switch Status Feedback and Ramped Output



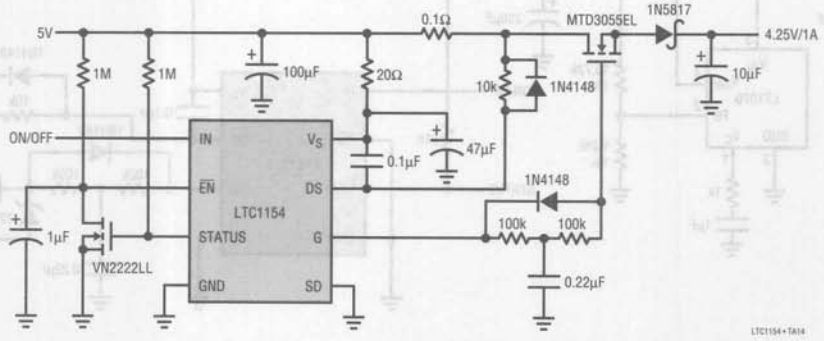
TYPICAL APPLICATIONS

Auto-Reset High-Side Switch with Over-Current and Over-Current Temperature Shutdown



*KEYSTONE RL2006-100-100-30-PT.
**AUTO-RESET PERIOD = 800ms WITH COMPONENTS SHOWN

SCSI Termination Power Switch with 1A Over-Current Shutdown, Auto-Reset and Load Soft-Start



3.3V Dual Micropower High-Side/Low-Side MOSFET Driver

FEATURES

- Allows Lowest Drop 3.3V Supply Switching
- Operates on 3.3V or 5V Nominal Supplies
- 3 Microamps Standby Current
- 80 Microamps ON Current
- Drives Low Cost N-Channel Power MOSFETs
- No External Charge Pump Components
- Controlled Switching ON and OFF Times
- Compatible with 3.3V and 5V Logic Families
- Available in 8-Pin SOIC

APPLICATIONS

- Notebook Computer Power Management
- Palmtop Computer Power Management
- P-Channel Switch Replacement
- Battery Charging and Management
- Mixed 5V and 3.3V Supply Switching
- Stepper Motor and DC Motor Control
- Cellular Telephones and Beepers

DESCRIPTION

The LTC1157 dual 3.3V micropower MOSFET gate driver makes it possible to switch either supply or ground reference loads through a low $R_{DS(ON)}$ N-channel switch (N-channel switches are required at 3.3V because P-channel MOSFETs do not have guaranteed $R_{DS(ON)}$ with $V_{GS} \leq 3.3V$). The LTC1157 internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground), fully enhancing a logic level N-channel switch for 3.3V high-side applications and a standard N-channel switch for 3.3V low-side applications. The gate drive voltage at 5V is typically 8.8V above supply (13.8V above ground), so standard N-channel MOSFET switches can be used for both high-side and low-side applications.

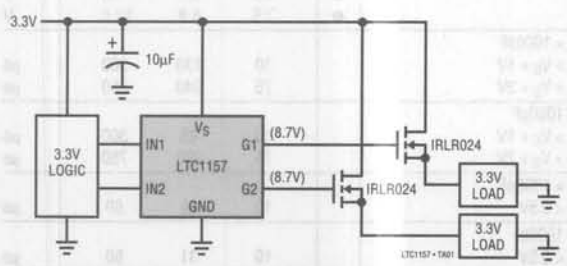
Micropower operation, with 3μA standby current and 80μA operating current, makes the LTC1157 well suited for battery-powered applications.

The LTC1157 is available in both 8-pin DIP and SOIC.

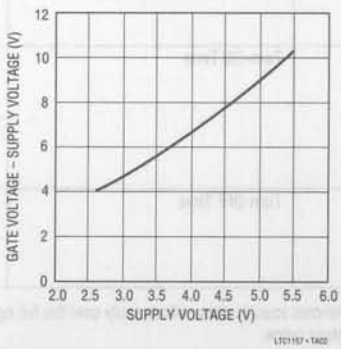
4

TYPICAL APPLICATION

Ultra Low Voltage Drop 3.3V Dual High-Side Switch



Gate Voltage Above Supply

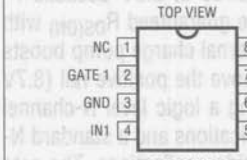


ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.3V to 7V
Any Input Voltage ..... (V_S + 0.3V) to (GND – 0.3V)
Any Output Voltage ..... (V_S + 12V) to (GND – 0.3V)
Current (Any Pin) 50mA

Operating Temperature Range
LTC1157C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

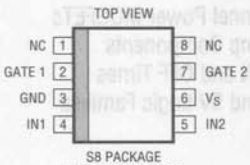
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1157CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1157CS8
S8 PART MARKING
1157

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 2.7V to 5.5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1157C MIN	TYP	MAX	UNITS
I_Q	Quiescent Current OFF	V_S = 3.3V, $V_{IN1} = V_{IN2}$ = 0V (Note 1)			3	10	µA
	Quiescent Current ON	V_S = 3.3V, V_{IN} = 3.3V (Note 2)			80	160	µA
		V_S = 5V, V_{IN} = 5V (Note 2)			180	400	µA
V_{INH}	Input High Voltage		●	70% × V_S			V
V_{INL}	Input Low Voltage		●			15% × V_S	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
$V_{GATE} - V_S$	Gate Voltage Above Supply	V_S = 3V	●	4.0	4.7	6.5	V
		V_S = 3.3V	●	4.5	5.4	7.0	V
		V_S = 5V	●	7.5	8.8	12.0	V
t_{ON}	Turn-ON Time	V_S = 3.3V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		30	130	300	µs
		Time for $V_{GATE} > V_S + 2V$		75	240	750	µs
		V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		30	85	300	µs
		Time for $V_{GATE} > V_S + 2V$		75	230	750	µs
t_{OFF}	Turn-OFF Time	V_S = 3.3V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 0.5V$		10	36	60	µs
		V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} < 0.5V$		10	31	60	µs

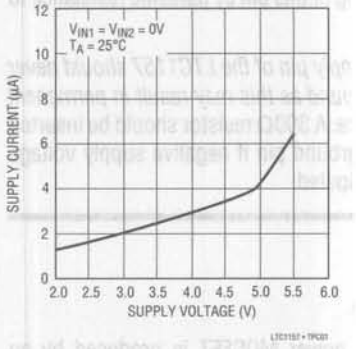
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Quiescent current OFF is for both channels in OFF condition.

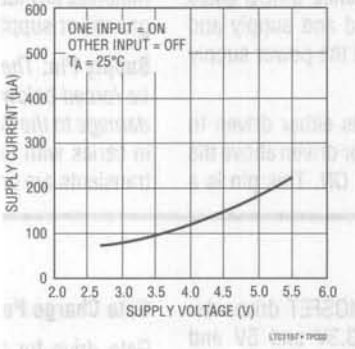
Note 2: Quiescent current ON is per driver and is measured independently.

TYPICAL PERFORMANCE CHARACTERISTICS

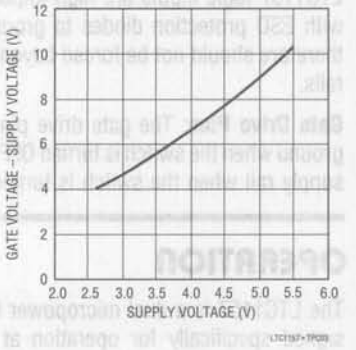
Standby Supply Current



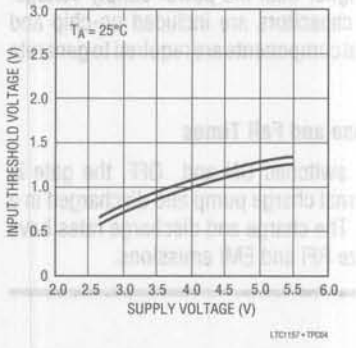
Supply Current per Driver ON



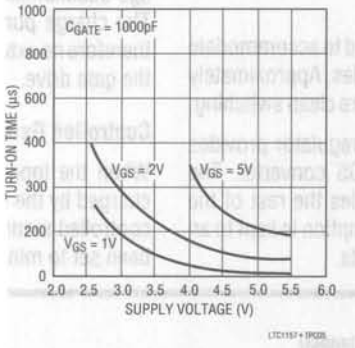
Gate Voltage Above Supply



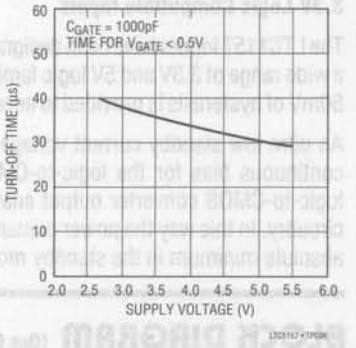
Input Threshold Voltage



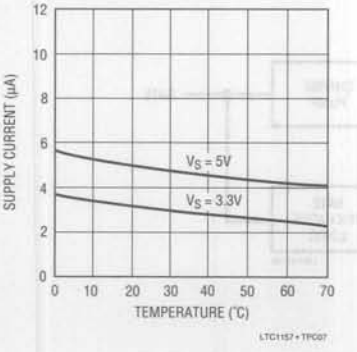
Turn-ON Time



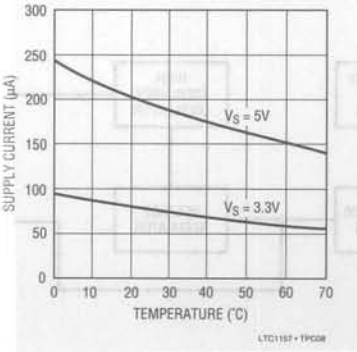
Turn-OFF Time



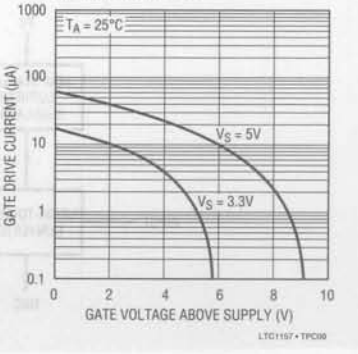
Standby Supply Current



Supply Current per Driver ON



Gate Drive Current



4

PIN FUNCTIONS

Input Pins: The LTC1157 input pins are active high and activate the charge pump circuitry when switched ON. The LTC1157 logic inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails.

Gate Drive Pins: The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin: *The supply pin of the LTC1157 should never be forced below ground as this may result in permanent damage to the device.* A 300Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

OPERATION

The LTC1157 is a dual micropower MOSFET driver designed specifically for operation at 3.3V and 5V and includes the following functional blocks:

3.3V Logic Compatible Inputs

The LTC1157 inputs have been designed to accommodate a wide range of 3.3V and 5V logic families. Approximately 50mV of hysteresis is provided to ensure clean switching.

An ultra low standby current voltage regulator provides continuous bias for the logic-to-CMOS converter. The logic-to-CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to an absolute minimum in the standby mode.

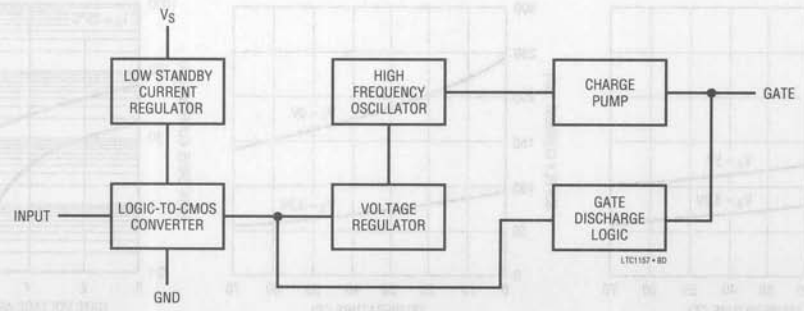
Gate Charge Pump

Gate drive for the power MOSFET is produced by an internal charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and therefore no external components are required to generate the gate drive.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

MOSFET Selection

The LTC1157 is designed to operate with both standard and logic level N-channel MOSFET switches. The choice of switch is determined primarily by the operating supply voltage.

Logic Level MOSFET Switches at 3.3V

Logic level switches should be used with the LTC1157 when powered from 2.7V to 4V. Although there is some variation among manufacturers, logic level MOSFET switches are typically rated with V_{GS} = 4V with a maximum continuous V_{GS} rating of ±10V. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic level MOSFETs are frequently designated by an "L" and are usually available in surface mount packaging. Some logic level MOSFETs are rated up to ±15V and can be used in applications which require operation over the entire 2.7V to 5.5V range.

Standard MOSFET Switches at 5V

Standard N-channel MOSFET switches should be used with the LTC1157 when powered from 4V to 5.5V supply as the built-in charge pump produces ample gate drive to fully enhance these switches when powered from a 5V nominal supply. Standard N-channel MOSFET switches are rated with V_{GS} = 10V and are generally restricted to a maximum of ±20V.

Powering Large Capacitive Loads

Electrical subsystems in portable battery-powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly powered however, these capacitors may themselves become the source of supply glitching.

For example, if a 100µF capacitor is powered through a switch with a slew rate of 0.1V/µs, the current during start-up is:

$$I_{START} = C(dV/dt)$$
$$= (100 \times 10^{-6})\ (1 \times 10^{5})$$
$$= 10A$$

Obviously, this is too much current for the regulator (or output capacitor) to supply and the output will glitch by as much as a few volts.

The start-up current can be substantially reduced by limiting the slew rate at the gate of an N-channel switch as shown in Figure 1. The gate drive output of the LTC1157

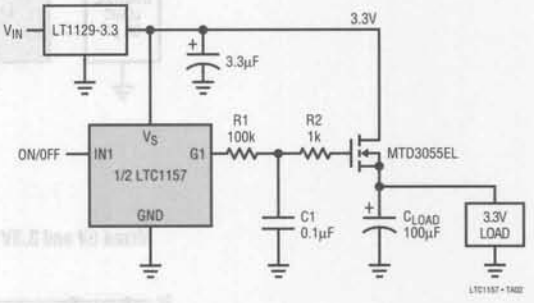


Figure 1. Powering a Large Capacitive Load

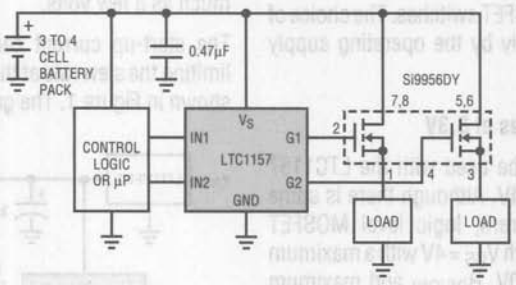
is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately 1.5×10^{-4}V/µs. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the start-up current to approximately 15mA which is easily managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. Also, it is good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Reverse Battery Protection

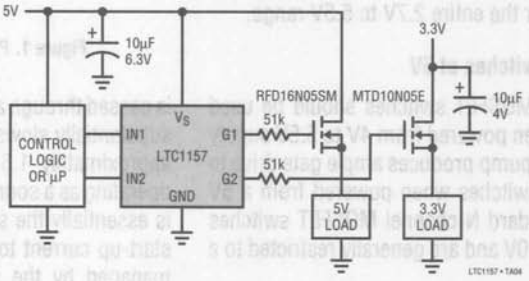
The LTC1157 can be protected against reverse battery conditions by connecting a 300Ω resistor in series with the ground pin. The resistor limits the supply current to less than 12mA with –3.6V applied. Since the LTC1157 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 3.3V µP (or control logic) can be protected by adding 10k resistors in series with the input pins.

TYPICAL APPLICATIONS

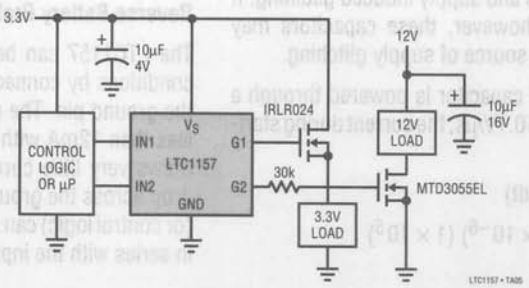
Ultra Low Drop 3 to 4 Cell Dual High-Side Switch



Mixed 5V and 3.3V Dual High-Side Switch

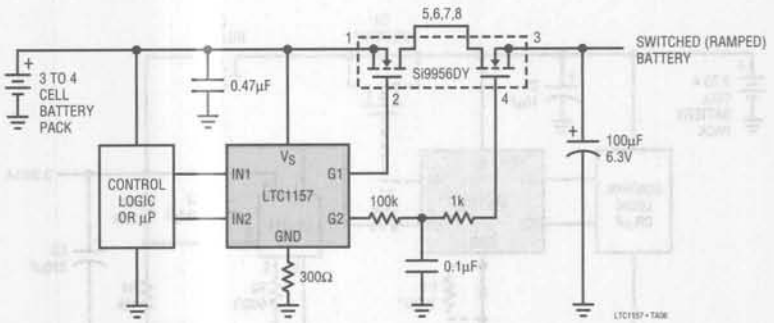


Mixed 3.3V and 12V High- and Low-Side Switching

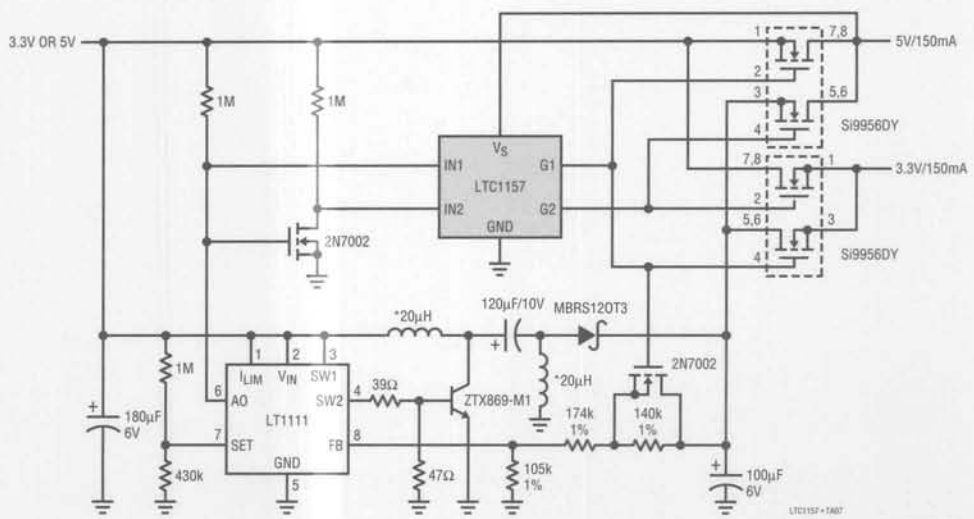


TYPICAL APPLICATIONS

Ultra Low Voltage Drop Battery Switch with Reverse Battery Protection, Ramped Output and 3μA Standby Current



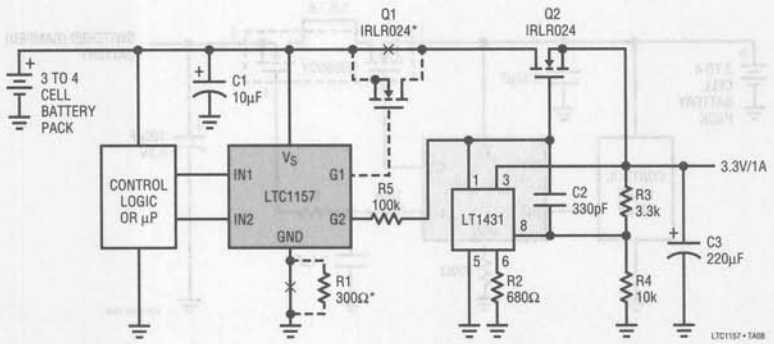
Generating 3.3V and 5V from a 3.3V or 5V Source (Automatic Switching)



*CTX20-3 COILTRONICS

TYPICAL APPLICATIONS

3.3V Ultra Low Voltage Drop Regulator with Optional Reverse Battery Protection and 3μA Standby Current



*OPTIONAL REVERSE BATTERY PROTECTION. ADD R1 IN SERIES WITH THE GROUND LEAD AND ADD Q1 IN SERIES WITH THE BATTERY AS SHOWN.

Quad Protected High-Side MOSFET Driver

FEATURES

- Fully Enhances N-Channel MOSFET Switches
- **8V to 48V Power Supply Range**
- **Protected from –15V to 60V Supply Transients**
- **Individual Short-Circuit Protection**
- **Individual Automatic Restart Timers**
- Programmable Current Limit, Delay Time, and Auto-Restart Period
- Voltage-Limited Gate Drive
- Defaults to OFF State with Open Input
- Flowthrough Input to Output Pinout
- Available in 20-Lead DIP or SOL Package

APPLICATIONS

- Industrial Control
- Avionics Systems
- Automotive Switches
- Stepper Motor and DC Motor Control
- Electronic Circuit Breaker

DESCRIPTION

The LT1161 is a quad high-side gate driver allowing the use of low cost N-channel power MOSFETs for high-side switching applications. It has four independent switch channels, each containing a completely self-contained charge pump to fully enhance an N-channel MOSFET switch with no external components.

Also included in each switch channel is a drain sense comparator that is used to sense switch current. When a preset current level is exceeded, the switch is turned off. The switch remains off for a period of time set by an external timing capacitor and then automatically attempts to restart. If the fault is still present, this cycle repeats until the fault is removed, thus protecting the MOSFET.

The LT1161 has been specifically designed for harsh operating environments such as industrial, avionics, and automotive applications where poor supply regulation and/or transients may be present. The device will not sustain damage from supply voltages of –15V to 60V.

4

TYPICAL APPLICATION

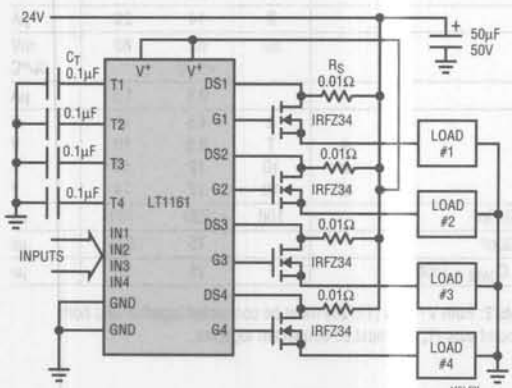
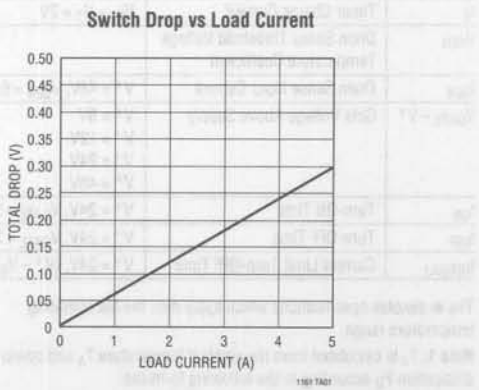


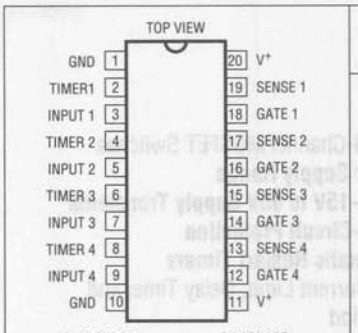
Figure 1. Protected Quad High-Side Switch



ABSOLUTE MAXIMUM RATINGS

Supply Voltages (Pins 11, 20) ..... −15V to 60V
Input Voltages (Pins 3, 5, 7, 9) ..... (GND − 0.3V) to 15V
Gate Voltages (Pins 12, 14, 16, 18) 75V
Sense Voltages (Pins 13, 15, 17, 19) ..... $V^+ \pm 5V$
Current (Any Pin) 50mA
Operating Temperature Range
LT1161C ..... 0°C to 70°C
LT1161I ..... −40°C to 85°C
Junction Temperature Range (Note 1)
LT1161C ..... 0°C to 125°C
LT1161I ..... −40°C to 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1161CN
LT1161CS
LT1161IN
LT1161IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V^+ = 12V to 48V each channel, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current	All Channels OFF (Note 2)		3	4.5	6.5	mA
$\Delta I_{S(ON)}$	Delta Supply Current (ON State)	Measure Increase in I_S per Channel			1	1.35	mA
V_{INH}	Input High Voltage		●	2			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	V_{IN} = 2V	●	15	30	50	µA
		V_{IN} = 5V	●	55	110	185	µA
C_{IN}	Input Capacitance				5		pF
$V_{T(TH)}$	Timer Threshold Voltage	V_{IN} = 2V, Adjust V_T	●	2.7	3	3.3	V
$V_{T(CL)}$	Timer Clamp Voltage	V_{IN} = 0.8V		3.2	3.5	3.8	V
I_T	Timer Charge Current	$V_{IN} = V_T$ = 2V		9	14	20	µA
V_{SEN}	Drain Sense Threshold Voltage			50	65	80	mV
	Temperature Coefficient				+0.33		%/°C
I_{SEN}	Drain Sense Input Current	V^+ = 48V, V_{SEN} = 65mV			0.5	1.5	µA
$V_{GATE} - V^+$	Gate Voltage Above Supply	V^+ = 8V		4	4.5	6	V
		V^+ = 12V	●	7	8.5	10	V
		V^+ = 24V	●	10	12	14	V
		V^+ = 48V	●	10	12	14	V
t_{ON}	Turn-ON Time	V^+ = 24V, V_{GATE} > 32V, C_{GATE} = 1000pF		100	220	400	µs
t_{OFF}	Turn-OFF Time	V^+ = 24V, V_{GATE} < 2V, C_{GATE} = 1000pF			75	200	µs
$t_{OFF(CL)}$	Current Limit Turn-OFF Time	V^+ = 24V, ($V^+ - V_{SENSE}$) → 0.1V, C_{GATE} = 1000pF			25	50	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

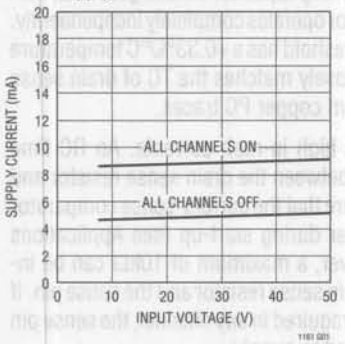
LT1161CN, LT1161IN: $T_J = T_A + (P_D \times 70°C/W)$

LT1161CS, LT1161IS: $T_J = T_A + (P_D \times 110°C/W)$

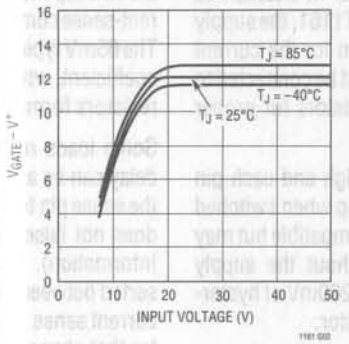
Note 2: Both V^+ pins (11, 20) must be connected together and both ground pins (1, 10) must be connected together.

TYPICAL PERFORMANCE CHARACTERISTICS

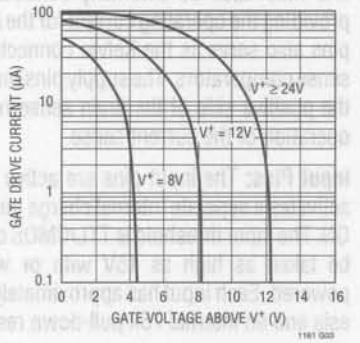
Supply Current



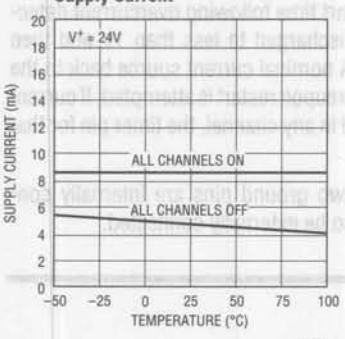
MOSFET Gate Voltage Above V⁺



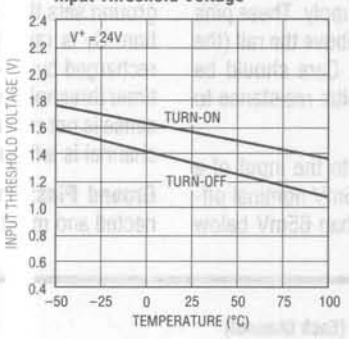
MOSFET Gate Drive Current



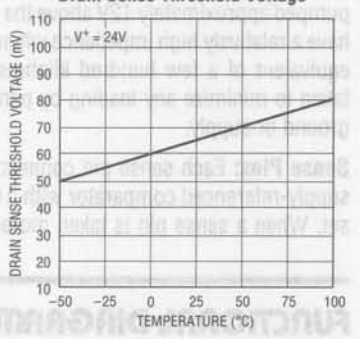
Supply Current



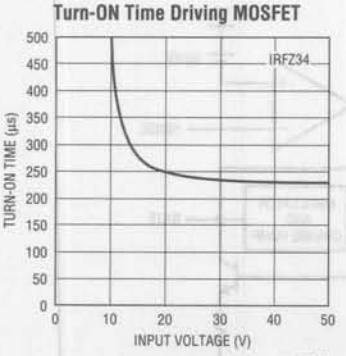
Input Threshold Voltage



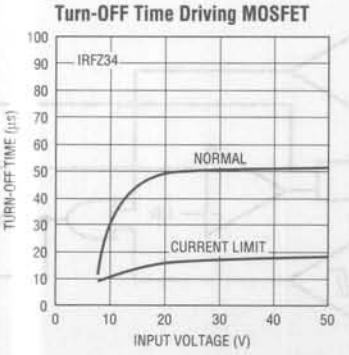
Drain Sense Threshold Voltage



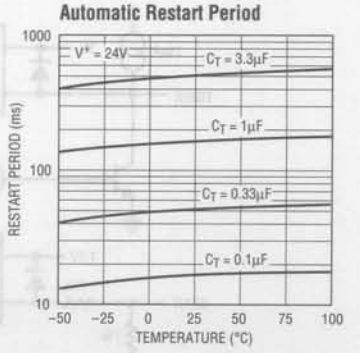
Turn-ON Time Driving MOSFET



Turn-OFF Time Driving MOSFET



Automatic Restart Period



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PIN FUNCTIONS

Supply Pins: The two supply pins are internally connected and must also be externally connected. In addition to providing the operating current for the LT1161, the supply pins also serve as the Kelvin connection for the current sense comparators. The supply pins must be connected to the positive side of the drain sense resistors for proper operation of the current sense.

Input Pins: The input pins are active high and each pin activates a separate internal charge pump when switched ON. The input threshold is TTL/CMOS compatible but may be taken as high as 15V with or without the supply powered. Each input has approximately 200mV of hysteresis and an internal 75k pull-down resistor.

Gate Pins: The gate pins drive the power MOSFET gates. When an input is ON, the corresponding gate pin is pumped approximately 12V above the supply. These pins have a relatively high impedance when above the rail (the equivalent of a few hundred kilohms). Care should be taken to minimize any loading by parasitic resistance to ground or supply.

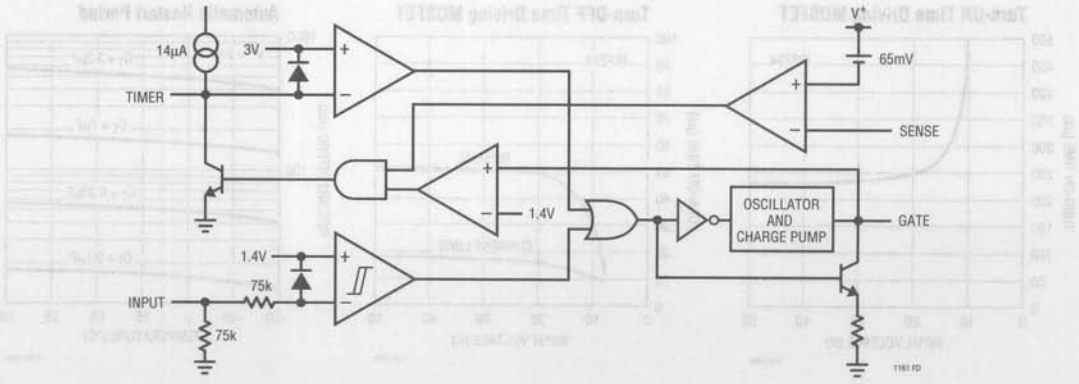
Sense Pins: Each sense pin connects to the input of a supply-referenced comparator with a 65mV nominal offset. When a sense pin is taken more than 65mV below supply, the MOSFET gate for that channel is driven low and the corresponding timing capacitor discharged. Each current-sense comparator operates completely independently. The 65mV typical threshold has a +0.33%/°C temperature coefficient, which closely matches the TC of drain sense resistors formed from copper PC traces.

Some loads require high in-rush currents. An RC time delay can be added between the drain sense resistor and the sense pin to ensure that the current-sense comparator does not false trigger during start-up (see Applications Information). However, a maximum of 10kΩ can be inserted between a drain sense resistor and the sense pin. If current sense is not required in any channel, the sense pin for that channel is tied to supply.

Timer Pins: A timing capacitor C_T from each timer pin to ground sets the restart time following overcurrent detection. C_T is rapidly discharged to less than 1V and then recharged by a 14μA nominal current source back to the timer threshold, whereupon restart is attempted. If current sense is not required in any channel, the timer pin for that channel is left open.

Ground Pins: The two ground pins are internally connected and must also be externally connected.

FUNCTIONAL DIAGRAM (Each Channel)



OPERATION (Each Channel, Refer to Functional Diagram)

The LT1161 gate pin has two states, OFF and ON. In the OFF state it is held low, while in the ON state it is pumped to 12V above supply by a self-contained 750kHz charge pump. The OFF state is activated when either the input pin is below 1.4V or the timer pin is below 3V. Conversely, for the ON state to be activated, both the input and timer pins must be above their thresholds.

If left open, the input pin is held low by a 75k resistor, while the timer pin is held a diode drop above 3V by a 14μA pull-up current source. Thus the timer pin automatically reverts to the ON state, subject to the input also being high. The input has approximately 200mV of hysteresis.

The sense pin normally connects to the drain of the power MOSFET, which returns through a low valued drain sense resistor to supply. When the gate is ON and the MOSFET drain current exceeds the level required to generate a 65mV drop across the drain sense resistor, the sense comparator activates a pull-down NPN which rapidly pulls the timer pin below 3V. This in turn causes the timer comparator to override the input pin and activate the gate pin OFF state, thus protecting the power MOSFET. In order for the sense comparator to accurately sense MOSFET drain current, the LT1161 supply pins must be connected directly to the positive side of the drain sense resistors.

When the MOSFET gate voltage is less than 1.4V, the timer pin is released. The 14μA current source then slowly charges the timing capacitor back to 3V where the charge pump again starts to drive the gate pin high. If a fault still exists, such as a short circuit, the sense comparator threshold will again be exceeded and the timer cycle will repeat until the fault is removed (see Figure 2).

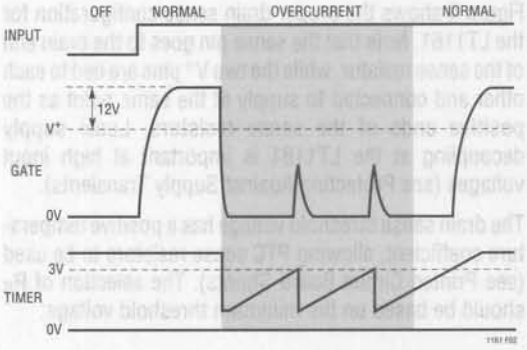


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

Input/Supply Sequencing

There are no input/supply sequencing requirements for the LT1161. The input may be taken up to 15V with the supply at 0V. When the supply is turned on with an input high, the MOSFET turn-on will be inhibited until the timing capacitor charges to 3V (i.e., for one restart cycle). The two V^+ pins (11, 20) must always be connected to each other.

Isolating the Inputs

Operation in harsh environments may require isolation to prevent ground transients from damaging control logic. The LT1161 easily interfaces to low cost opto-isolators. The network shown in Figure 3 ensures that the input will be pulled above 2V, but not exceed the absolute maximum rating, for supply voltages of 12V to 48V over the entire temperature range. In order to maintain the OFF state, the opto must have less than 20μA of dark current (leakage) hot.

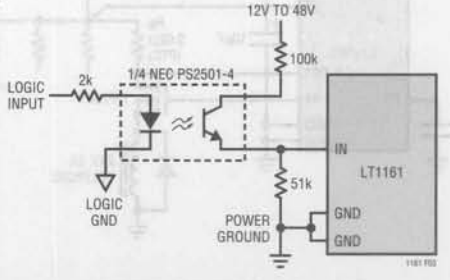


Figure 3. Isolating the Inputs

APPLICATIONS INFORMATION

Drain Sense Configuration

The LT1161 uses supply-referenced current sensing. One input of each channel's current-sense comparator is connected to a drain sense pin, while the second input is offset 65mV below the supply bus inside the device. For this reason, pins 11 and 20 of the LT1161 must be treated not only as supply pins, but as the reference inputs for the current-sense comparators.

Figure 4 shows the proper drain sense configuration for the LT1161. Note that the sense pin goes to the drain end of the sense resistor, while the two V^+ pins are tied to each other and connected to supply at the same point as the positive ends of the sense resistors. Local supply decoupling at the LT1161 is important at high input voltages (see Protecting Against Supply Transients).

The drain sense threshold voltage has a positive temperature coefficient, allowing PTC sense resistors to be used (see Printed Circuit Board Shunts). The selection of R_S should be based on the minimum threshold voltage:

$$R_S = \frac{50mV}{I_{SET}}$$

Thus the 0.02Ω drain sense resistor in Figure 4 would yield a minimum trip current of 2.5A. This simple configuration is appropriate for resistive or inductive loads which do not generate large current transients at turn-on.

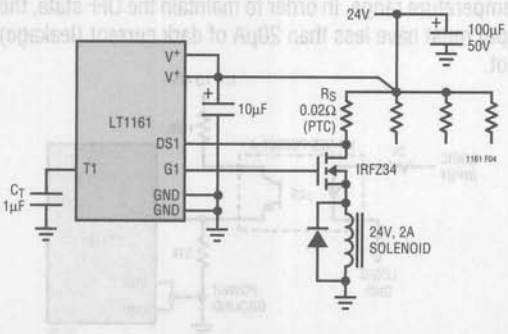


Figure 4. Drain Sense Configuration

Automatic Restart Period

The timing capacitor C_T shown in Figure 4 determines the length of time the power MOSFET is held off following a current limit trip. Curves are given in the Typical Performance Characteristics to show the restart period for various values of C_T. For example, C_T = 0.33µF yields a 50ms restart period.

Defeating Automatic Restart

Some applications are required to remain off after a fault occurs. When the LT1161 is being driven from CMOS logic, this can be easily implemented by connecting resistor R1 between the input and timer pins as shown in Figure 5. R1 supplies the sustaining current for an SCR which latches the timer pin low. This prevents the MOSFET gate from turning ON until the input has been recycled.

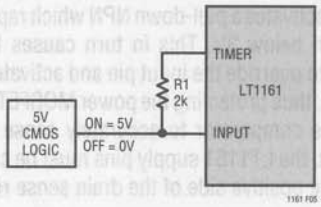


Figure 5. Latch-Off Input Network (Auto-Restart Defeated)

Inductive vs Capacitive Loads

Turning on an inductive load produces a relatively benign ramp in MOSFET current. However, when an inductive load is turned off, the current stored in the inductor needs somewhere to decay. A clamp diode connected directly across each inductive load normally serves this purpose. If a diode is not employed the LT1161 clamps the MOSFET gate 0.7V below ground. This causes the MOSFET to resume conduction during the current decay with (V^+ + V_{GS} + 0.7V) across it, resulting in high dissipation peaks.

Capacitive loads exhibit the opposite behavior. Any load that includes a decoupling capacitor will generate a current equal to $C_{LOAD} \times (\partial V/\partial t)$ during capacitor in-rush. With large electrolytic capacitors, the resulting current

APPLICATIONS INFORMATION

spike can play havoc with the power supply and false trip the current-sense comparator.

Turn-on ∂V/∂t is controlled by the addition of the simple network shown in Figure 6. This network takes advantage of the fact that the MOSFET acts as a source follower during turn-on. Thus the ∂V/∂t on the source can be controlled by controlling the ∂V/∂t on the gate:

$$\frac{\partial V}{\partial t} = \frac{V^+ - V_{TH}}{10^5 \times C1}$$

where V_{TH} is the MOSFET gate threshold voltage. Multiplying C_{LOAD} times this ∂V/∂t yields the value of the current spike. For example, if $V^+ = 24V$, $V_{TH} = 2V$, and $C1 = 0.1\mu F$, ∂V/∂t = 2.2V/ms, resulting in a 2.2A turn-on spike into 1000µF. The diode and second resistor in the network ensure fast current limit turn-off.

When turning off a capacitive load, the source of the MOSFET can "hang up" if the load resistance does not discharge C_{LOAD} as fast as the gate is being pulled down. If this is the case, a diode may have to be added from source to gate to prevent $V_{GS(MAX)}$ from being exceeded.

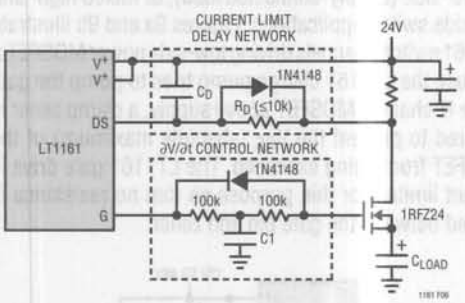


Figure 6. ∂V/∂t Control and Current Limit Delay

Adding Current Limit Delay

When capacitive loads are being switched or in very noisy environments, it is desirable to add delay in the drain current-sense path to prevent false tripping (inductive loads normally do not need delay). This is accomplished by the current limit delay network shown in Figure 6. R_D and C_D delay the overcurrent trip for drain currents up to approximately $10 \times I_{SET}$, above which the diode conducts and provides immediate turn-off (see Figure 7). *To ensure proper operation of the timer, C_D must be ≤ C_T.*

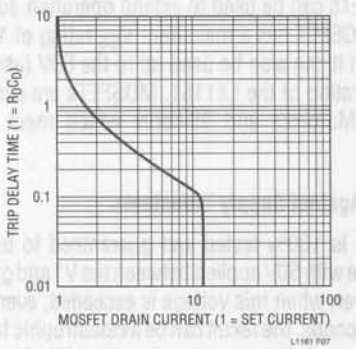


Figure 7. Current Limit Delay Time

Printed Circuit Board Shunts

The sheet resistance of 1oz. copper clad is approximately $5 \times 10^{-4}\Omega$/square with a temperature coefficient of +0.39%/°C. Since the LT1161 drain sense threshold has a similar temperature coefficient (+0.33%/°C), this offers the possibility of nearly zero TC current sensing using "free" drain sense resistors made out of PC trace material.

A conservative approach is to use 0.02" of width for each 1A of current for 1oz. copper. Combining the LT1161 drain sense threshold with the 1oz. copper sheet resistance results in a simple expression for width and length:

Width (1oz. Cu) = $0.02" \times I_{SET}$

Length (1oz. Cu) = 2"

The width for 2oz. copper would be halved while the length would remain the same.

Bends may be incorporated into the resistor to reduce space; each bend is equivalent to approximately 0.6 × width of straight length. Kelvin connections should be employed by running separate traces from the ends of the resistors back to the LT1161 V^+ and sense pins. See Application Note 53 for further information on printed circuit board shunts.

APPLICATIONS INFORMATION

Low Voltage/Wide Supply Range Operation

When the supply is <12V, the LT1161 charge pumps do not produce sufficient gate voltage to fully enhance standard N-channel MOSFETs. For these applications, logic-level MOSFETs can be used to extend operation down to 8V. If the MOSFET has a maximum V_{GS} rating of 15V or greater, then it can also be used up to the 60V (absolute maximum) rating of the LT1161. MOSFETs are available from both Motorola and Siliconix which meet these criteria.

Protecting Against Supply Transients

The LT1161 is 100% tested and guaranteed to be safe from damage with 60V applied between the V^+ and ground pins. However, when this voltage is exceeded, even for a few microseconds, the result can be a catastrophic failure. For this reason *it is imperative that the LT1161 not be exposed to supply transients above 60V.*

For proper current-sense operation, the V^+ pins are required to be connected to the positive side of the drain sense resistors (see Drain Sense Configuration). Therefore, the best way to prevent supply transients is to ensure that the supply is adequately decoupled at the point where the V^+ pins and drain sense resistors meet. Several hundred microfarads may be required with high current switches.

When operating voltages approach the 60V absolute maximum rating of the LT1161, local supply decoupling between the V^+ pins (11, 20) and ground pins (1, 10) is highly recommended. A small ferrite bead between the supply connection and local capacitor can also be effective in suppressing transients. Note however, that resistance should not be added in series with the V^+ pins because it will cause an error in the current sense threshold.

Fault Feedback

Two methods can be used to derive switch status. First, the timer pin voltage can be monitored to indicate when the switch is turned off due to current limit. During normal operation (ON or OFF), the timer voltage is 3.5V and only during current limit does the voltage drop below 3V.

The second method shown in Figure 8 uses a quad exclusive-NOR gate to indicate when the output of the switch has not obeyed the input command (i.e., output low when it should be high or vice versa). In addition to current limit, this gives a fault indication if the switch is shorted or if the load is open.

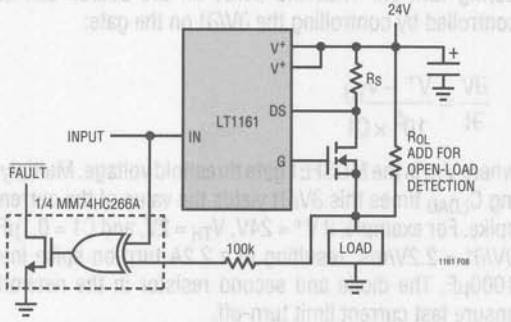


Figure 8. Fault Feedback Using Exclusive-NOR Gate

Low-Side Driving

Although the LT1161 is primarily targeted at high-side (grounded load) switch applications, it can also be used for low-side (supply-connected load), or mixed high- and low-side switch applications. Figures 9a and 9b illustrate LT1161 switch channels driving low-side power MOSFETs. Because the LT1161 charge pump tries to pump the gate of the N-channel MOSFET *above* supply, a clamp zener is required to prevent the V_{GS} (absolute maximum) of the MOSFET from being exceeded. The LT1161 gate drive is current limited for this purpose so that no resistance is needed between the gate pin and zener.

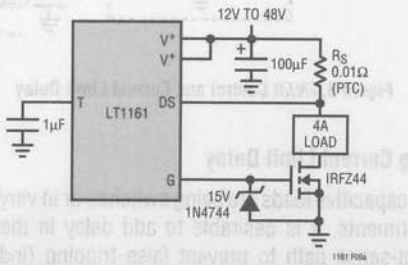


Figure 9a. Low-Side Driver with Load Current Sensing

APPLICATIONS INFORMATION

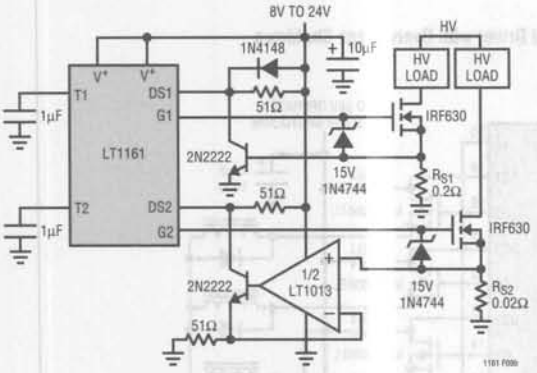


Figure 9b. Low-Side Drivers with Two Approaches for Source Current Sensing

Current sensing for protecting low-side drivers can be done in several different ways. In the Figure 9a circuit, the supply voltage for the load is assumed to be within the supply operating range of the LT1161. This allows the load to be returned to supply through current-sense resistor R_S, providing normal operation of the LT1161 protection circuitry.

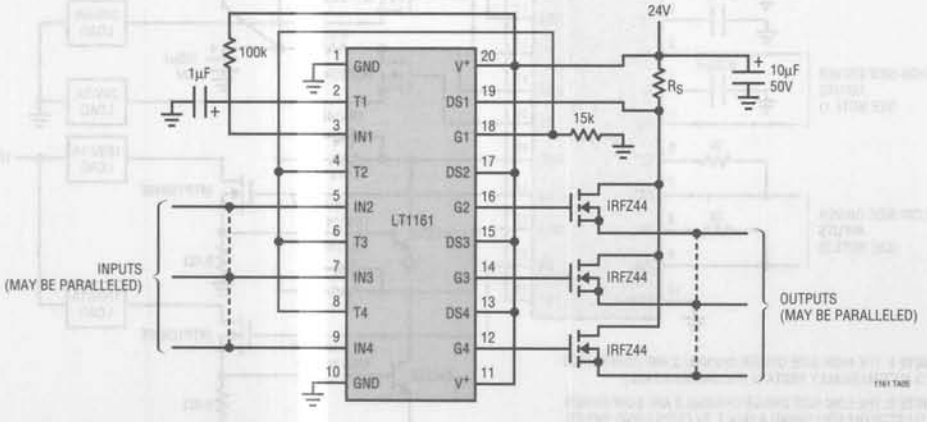
If the load cannot be returned to supply through R_S, or the load supply voltage is higher than the LT1161 supply, the current sense must be moved to the source of the low-side MOSFET. Figure 9b shows two approaches to source sensing. On channel 1, current limit occurs when the voltage across sense resistor R_{S1} thresholds the V_{BE} of the NPN transistor, causing the LT1161 drain sense pin to be pulled down.

The channel 2 circuit of Figure 9b uses an operational amplifier (must common mode to ground) to level shift the voltage across R_{S2} up to the drain sense pin. This approach allows the use of a much smaller sense resistor which could be made from PC trace material. In both cases, the LT1161 restart timers function the same as in high-side switch applications.

4

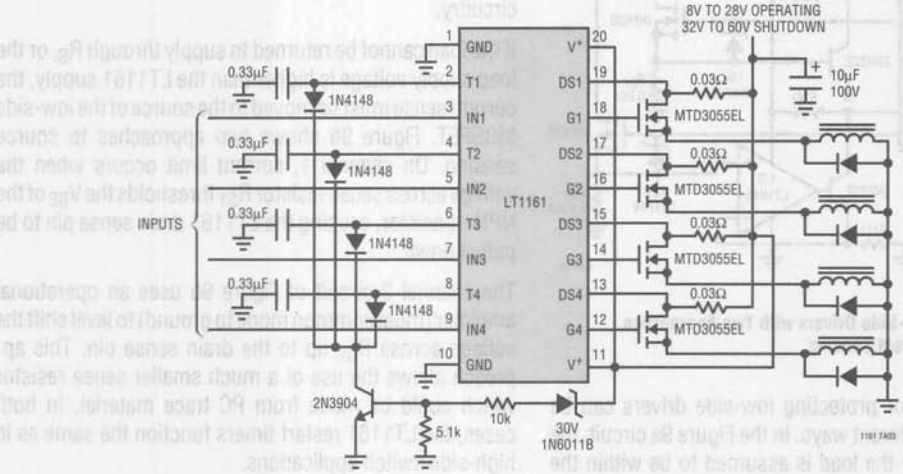
TYPICAL APPLICATIONS

Using an Extra Channel to Do Common Current Limit for Multiple/Paralleled Switches

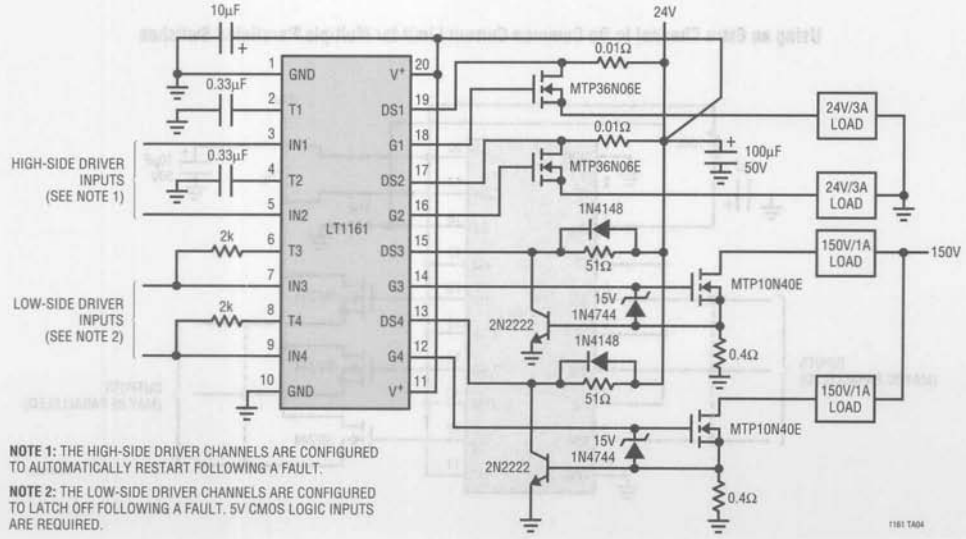


TYPICAL APPLICATIONS

Protected Quad 1A Automotive Solenoid Driver with Overvoltage Shutdown



Protected Quad Switch with Mixed Low- and High-Side Driving

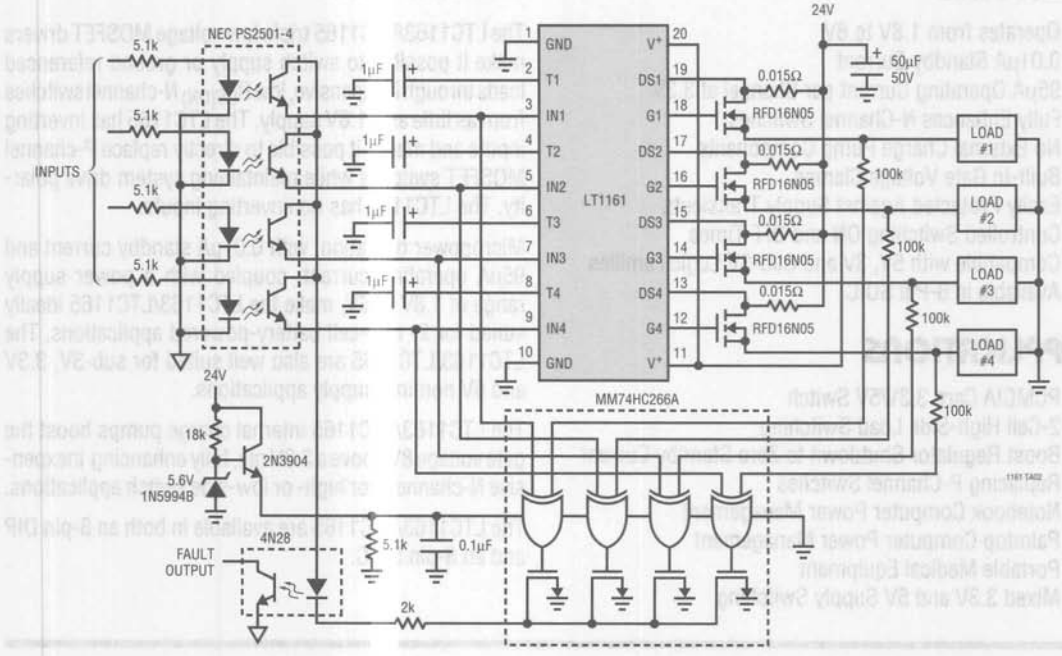


NOTE 1: THE HIGH-SIDE DRIVER CHANNELS ARE CONFIGURED TO AUTOMATICALLY RESTART FOLLOWING A FAULT.

NOTE 2: THE LOW-SIDE DRIVER CHANNELS ARE CONFIGURED TO LATCH OFF FOLLOWING A FAULT. 5V CMOS LOGIC INPUTS ARE REQUIRED.

TYPICAL APPLICATIONS

Protected Quad 2A Industrial Switch with Isolated Inputs and Fault Output



Triple 1.8V to 6V High-Side MOSFET Drivers

FEATURES

- Operates from 1.8V to 6V
- 0.01µA Standby Current
- 95µA Operating Current per Channel at 3.3V
- Fully Enhances N-Channel Switches
- No External Charge Pump Components
- Built-In Gate Voltage Clamps
- Easily Protected Against Supply Transients
- Controlled Switching ON and OFF Times
- Compatible with 5V, 3V and Sub-3V Logic Families
- Available in 8-Pin SOIC

APPLICATIONS

- PCMCIA Card 3.3V/5V Switch
- 2-Cell High-Side Load Switching
- Boost Regulator Shutdown to Zero Standby Current
- Replacing P-Channel Switches
- Notebook Computer Power Management
- Palmtop Computer Power Management
- Portable Medical Equipment
- Mixed 3.3V and 5V Supply Switching

DESCRIPTION

The LTC1163/LTC1165 triple low voltage MOSFET drivers make it possible to switch supply or ground referenced loads through inexpensive, low $R_{DS(ON)}$ N-channel switches from as little as a 1.8V supply. The LTC1165 has inverting inputs and makes it possible to directly replace P-channel MOSFET switches while maintaining system drive polarity. The LTC1163 has noninverting inputs.

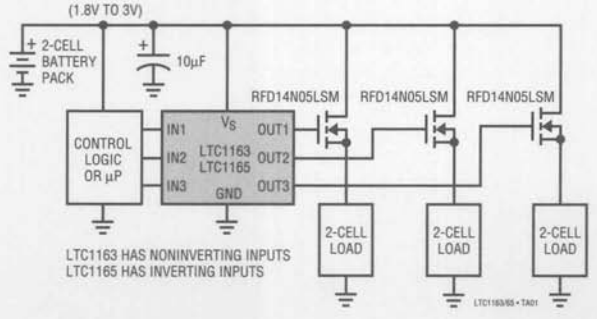
Micropower operation, with 0.01µA standby current and 95µA operating current, coupled with a power supply range of 1.8V to 6V, make the LTC1163/LTC1165 ideally suited for 2- to 4-cell battery-powered applications. The LTC1163/LTC1165 are also well suited for sub-3V, 3.3V and 5V nominal supply applications.

The LTC1163/LTC1165 internal charge pumps boost the gate voltage 8V above a 3.3V rail, fully enhancing inexpensive N-channels for high- or low-side switch applications.

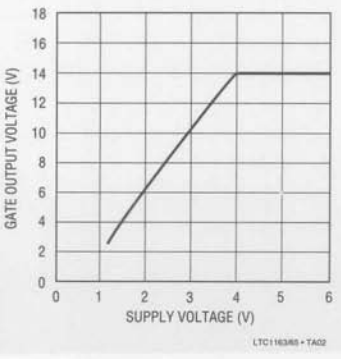
The LTC1163/LTC1165 are available in both an 8-pin DIP and an 8-pin SOIC.

TYPICAL APPLICATION

2-Cell Triple High-Side Switch



MOSFET Switch Gate Voltage

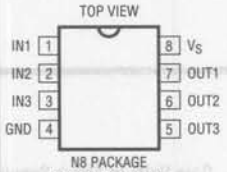


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7V
Any Input Voltage ..... 7V to (GND – 0.3V)
Any Output Voltage ..... 20V to (GND – 0.3V)
Current (Any Pin) 50mA

Operating Temperature Range
LTC1163C/LTC1165C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

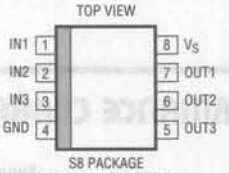


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1163CN8
LTC1165CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1163CS8
LTC1165CS8

S8 PART MARKING

1163
1165

Consult factory for Industrial and Military grade parts.

4

ELECTRICAL CHARACTERISTICS

V_S = 1.8V to 6V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1163C/LTC1165C MIN	TYP	MAX	UNITS
I_Q	Quiescent Current OFF	V_S = 1.8V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
		V_S = 3.3V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
		V_S = 5V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
	Quiescent Current ON	V_S = 1.8V, $V_{IN} = V_{ON}$ (Note 2,3)			60	120	µA
		V_S = 3.3V, $V_{IN} = V_{ON}$ (Note 2,3)			95	200	µA
		V_S = 5V, $V_{IN} = V_{ON}$ (Note 2,3)			180	400	µA
V_{INH}	Input High Voltage	1.8V < V_S < 2.7V	●	80% × V_S			V
		2.7V < V_S < 6V	●	70% × V_S			V
V_{INL}	Input Low Voltage	1.8V < V_S < 6V	●			15% × V_S	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
$V_{GATE} – V_S$	Gate Voltage Above Supply	V_S = 1.8V, $V_{IN} = V_{ON}$ (Note 2)	●	3.5	4.1	6.0	V
		V_S = 2V, $V_{IN} = V_{ON}$ (Note 2)	●	4.0	4.6	7.0	V
		V_S = 2.2V, $V_{IN} = V_{ON}$ (Note 2)	●	4.5	5.2	8.0	V
		V_S = 3.3V, $V_{IN} = V_{ON}$ (Note 2)	●	6.0	8.0	9.5	V
		V_S = 5V, $V_{IN} = V_{ON}$ (Note 2)	●	5.0	9.0	13.0	V
t_{ON}	Turn-ON Time	V_S = 3.3V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		40	120	400	µs
		Time for $V_{GATE} > V_S + 2V$		60	180	600	µs
		V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		30	95	300	µs
		Time for $V_{GATE} > V_S + 2V$		40	130	400	µs

ELECTRICAL CHARACTERISTICS V_S = 1.8V to 6V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1163C/LTC1165C MIN	TYP	MAX	UNITS
t_{OFF}	Turn-OFF Time	V_S = 3.3V, C_{GATE} = 1000pF Time for V_{GATE} < 0.5V	20	65	200	µs
		V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 0.5V	15	45	150	µs

The ● denotes specifications which apply over the full operating temperature range.

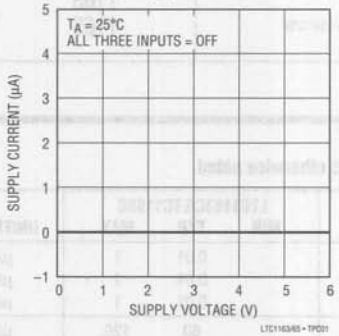
Note 1: Quiescent current OFF is for all channels in OFF condition.

Note 2: LTC1163: V_{OFF} = 0V, V_{ON} = V_S. LTC1165: V_{OFF} = V_S, V_{ON} = 0V

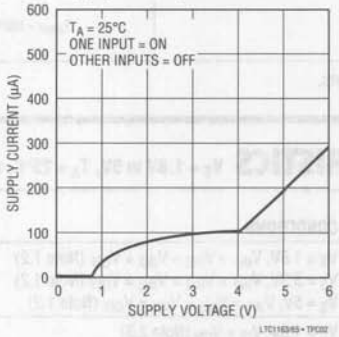
Note 3: Quiescent current ON is per driver and is measured independently.

TYPICAL PERFORMANCE CHARACTERISTICS

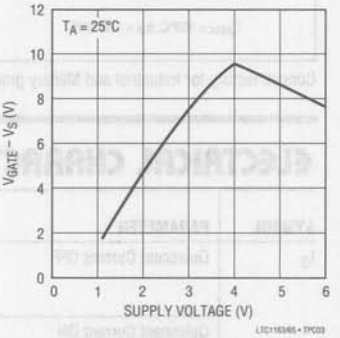
Standby Supply Current



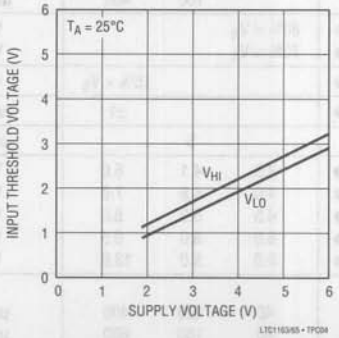
Supply Current per Driver ON



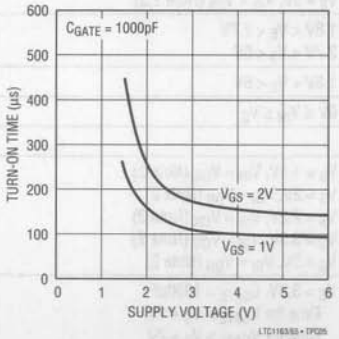
Gate Voltage Above Supply



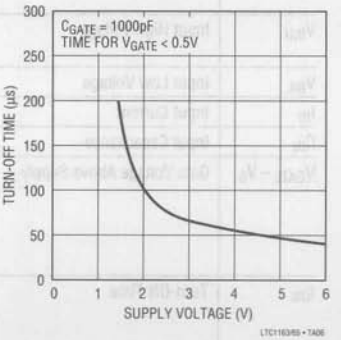
Input Threshold Voltage



Turn-ON Time

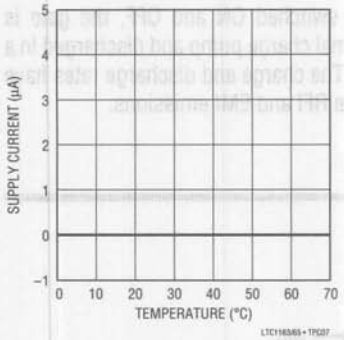


Turn-OFF Time

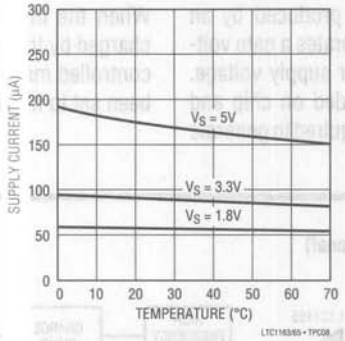


TYPICAL PERFORMANCE CHARACTERISTICS

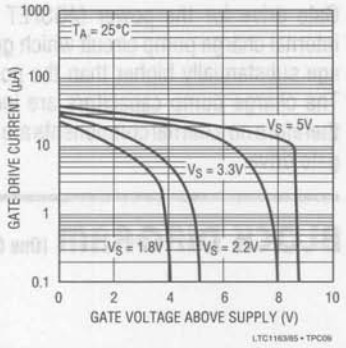
Standby Supply Current



Supply Current per Driver ON



MOSFET Gate Drive Current



PIN FUNCTIONS

Input Pins

The LTC1163 is noninverting; i.e., the MOSFET gate is driven above the supply when the input pin is held high. The LTC1165 is inverting and drives the MOSFET gate high when the input pin is held low. The inverting inputs of the LTC1165 allow P-channel switches to be replaced by lower resistance/cost N-channel switches while maintaining system drive polarity.

The LTC1163/LTC1165 logic inputs are high impedance CMOS gates with ESD protection diodes to ground and therefore should not be forced below ground. The inputs can however, be driven above the power supply rail as there are no clamping diodes connected between the input pins and supply pin. This facilitates operation in mixed 5V/3V systems.

Output Pins

The output pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. The output is clamped to about 14V above ground by a built-in Zener clamp. This pin has a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

A 150Ω resistor should be inserted in series with the ground pin or supply pin if negative supply voltage transients are anticipated. This will limit the current flowing from the power source into the LTC1163/LTC1165 to tens of milliamps during reverse battery conditions.

OPERATION

The LTC1163/LTC1165 are triple micropower MOSFET drivers designed for operation over the 1.8V to 6V supply range and include the following functional blocks:

3V Logic Compatible Inputs

The LTC1163/LTC1165 inputs have been designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is set at roughly 50% of the supply voltage and approximately 200mV of input hysteresis is provided to ensure clean switching.

The input enables all of the following circuit blocks: the bias generator, the high frequency oscillator and gate charge pump. Therefore, when the input is turned off, the entire circuit powers down and the supply current drops below 1µA.

OPERATION

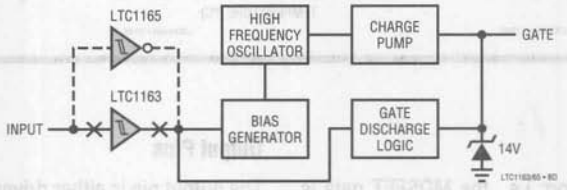
Gate Charge Pump

Gate drive for the power MOSFET is produced by an internal charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and therefore no external components are required to generate gate drive.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

Logic-Level MOSFET Switches

The LTC1163/LTC1165 are designed to operate with logic-level N-channel MOSFET switches. Although there is some variation among manufacturers, logic-level MOSFET switches are typically rated with V_{GS} = 4V with a maximum continuous V_{GS} rating of ±10V. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic-level MOSFETs are frequently designated by an "L" and are usually available in surface mount packaging. Some logic-level MOSFETs are rated with V_{GS} up to ±15V and can be used in applications which require operation over the entire 1.8V to 6V range.

Powering Large Capacitive Loads

Electrical subsystems in portable battery-powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly powered however, these capacitors may themselves become the source of supply glitching.

For example, if a 100µF capacitor is powered through a switch with a slew rate of 0.1V/µs, the current during start-up is:

$$I_{START} = C(\Delta V/\Delta t)$$
$$= (100 \times 10^{-6})(1 \times 10^{5})$$
$$= 10A$$

Obviously, this is too much current for the regulator (or output capacitor) to supply and the output will glitch by as much as a few volts.

The startup current can be substantially reduced by limiting the slew rate at the gate of an N-channel as shown in Figure 1. The gate drive output of the LTC1163/LTC1165 is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately 1.5×10^{-4}V/µs. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the startup current to approximately 15mA which is easily

APPLICATIONS INFORMATION

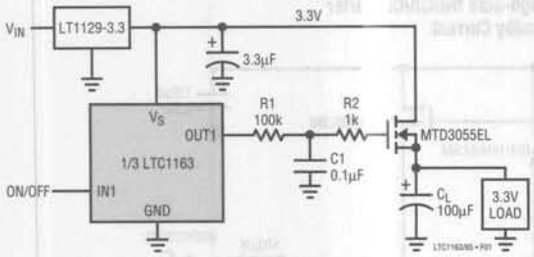


Figure 1. Powering a Large Capacitive Load

managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. It is a good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Mixed 5V/3V Systems

Because the input ESD protection diodes are referenced to ground instead of the supply pin, it is possible to drive the LTC1163/LTC1165 inputs from 5V CMOS or TTL logic even though the LTC1163/LTC1165 are powered from a 3.3V supply as shown in Figure 2. The input threshold voltage is approximately 50% of the supply voltage or 1.6V on a 3.3V supply which is compatible with 5V TTL and CMOS logic. (The LTC1163/LTC1165 cannot however, be driven by 3V logic when powered from a 5V supply because the threshold is approximately 2.5V.)

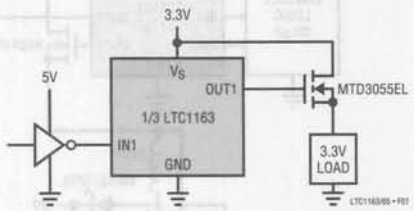


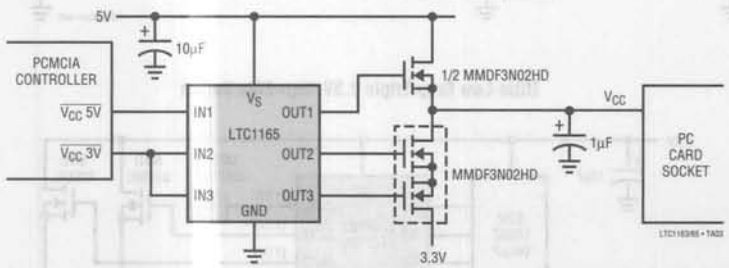
Figure 2. Direct Interface to 5V Logic

Reverse Battery Protection

The LTC1163/LTC1165 can be protected against reverse battery conditions by connecting a 150Ω resistor in series with the ground pin or supply pin. The resistor limits the supply current to less than 24mA with –3.6V applied. Because the LTC1163/LTC1165 draw very little current while in normal operation, the drop across the resistor is minimal. The 3.3V µP (or control logic) can be protected by adding 10k resistors in series with the input pins.

TYPICAL APPLICATIONS

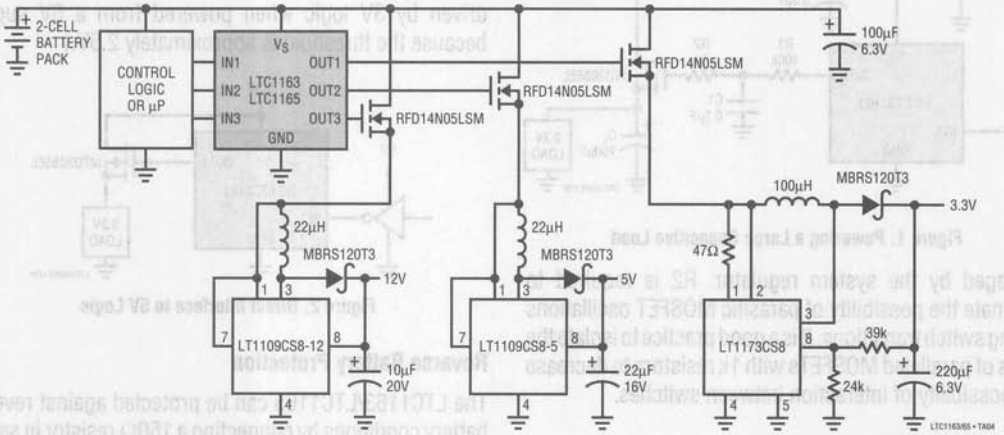
PCMCIA Card 3.3V/5V V_{CC} Switch



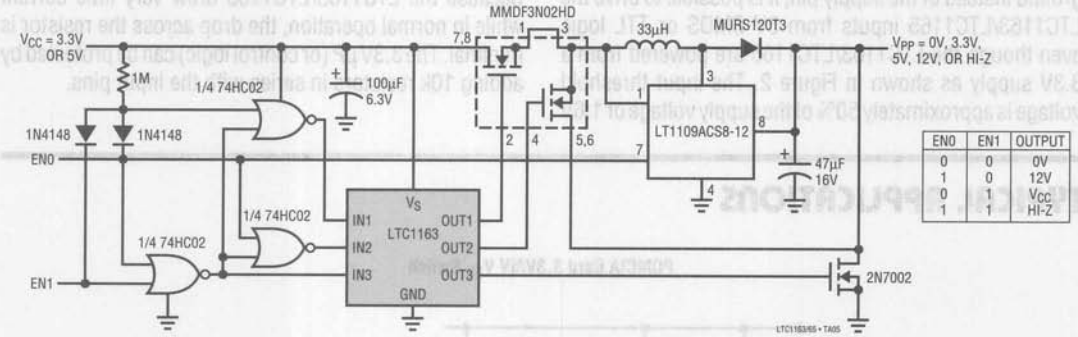
NOTE: USE LTC1163 WITH NONINVERTING PCMCIA CONTROLLERS

TYPICAL APPLICATIONS

2-Cell to 3.3V, 5V and 12V High-Side Switch/Converter with 0.01μA Standby Current

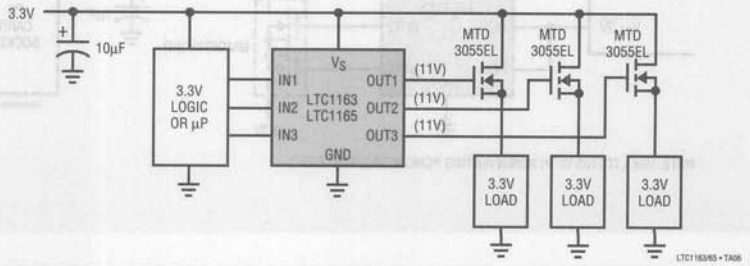


PCMCIA Card Socket V_{PP} Switch/Regulator



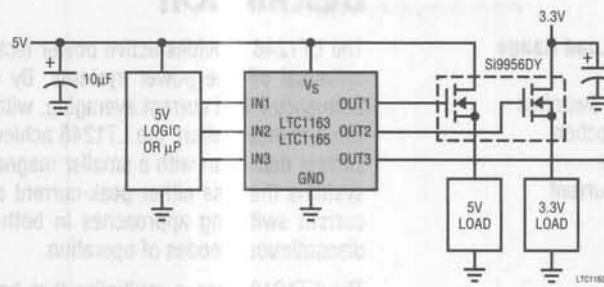
EN0	EN1	OUTPUT
0	0	0V
1	0	12V
0	1	V_{CC}
1	1	HI-Z

Ultra-Low Drop Triple 3.3V High-Side Switch

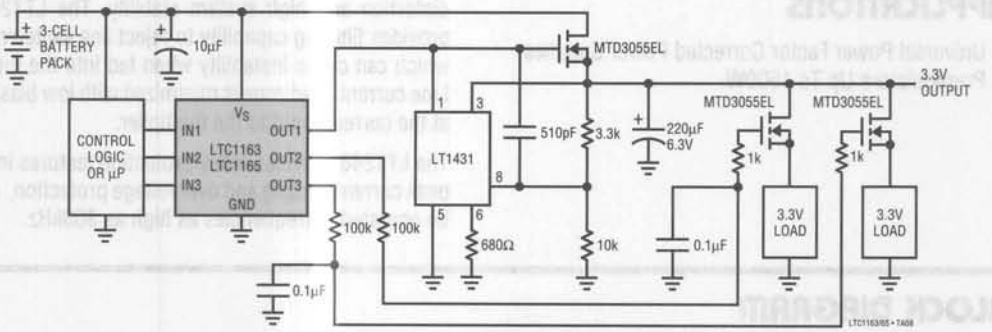


TYPICAL APPLICATIONS

Mixed Voltage High- and Low-Side Switches



3-Cell to 3.3V Ultra-Low Drop Regulator with 2 Ramped Switches



4

Power Factor Controller

FEATURES

- **High Power Factor Over Wide Load Range with Line Current Averaging**
- International Operation Without Switches
- Instantaneous Overvoltage Protection
- Minimal Line Current Dead Zone
- Typical 250µA Startup Supply Current
- Rejects Line Switching Noise
- Synchronization Capability
- Low Quiescent Current: 9mA
- Fast 1.5A Peak Current Gate Driver

APPLICATIONS

- Universal Power Factor Corrected Power Supplies
- Preregulators Up To 1500W

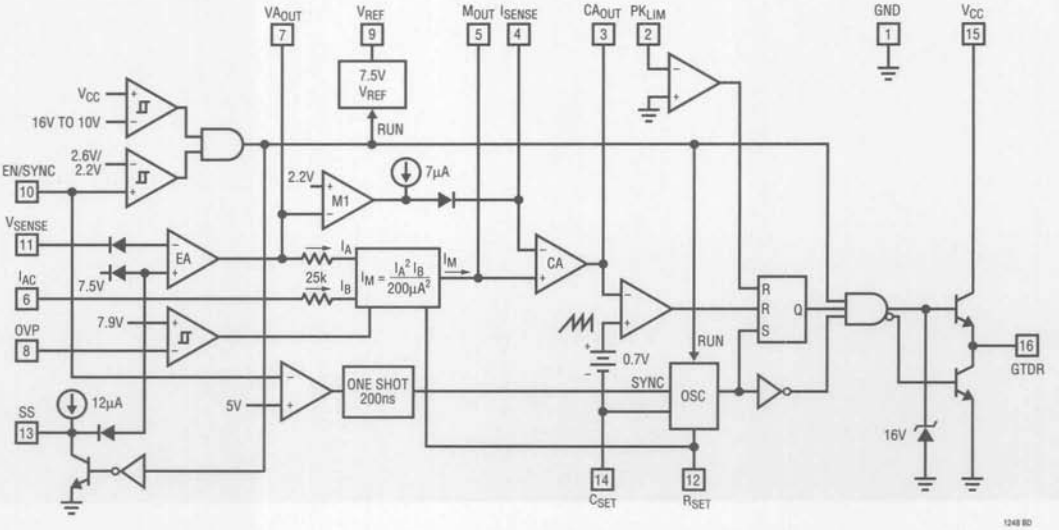
DESCRIPTION

The LT1248 provides active power factor correction for universal off-line power systems. By using fixed high frequency PWM current averaging, without the need for slope compensation, the LT1248 achieves far lower line current distortion with a smaller magnetic element than systems that use either peak-current detection or zero current switching approaches in both continuous and discontinuous modes of operation.

The LT1248 uses a multiplier that has a square gain function from the voltage amplifier to reduce the AC gain at light output load and thus maintains low line current distortion and high system stability. The LT1248 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1248 provides many protection features including peak current limiting and overvoltage protection, and can be operated at frequencies as high as 300kHz.

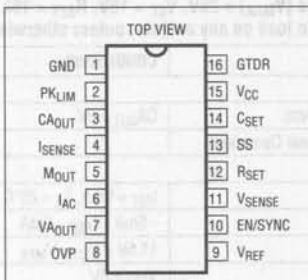
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 27V
GTDR Current Continuous 0.5A
GTDR Output Energy(Per Cycle) 5µJ
I_{AC}, R_{SET}, PK_{LIM} Input Current 20mA
V_{SENSE}, EN/SYNC, OVP Input Voltage ..... V_{MAX}
I_{SENSE}, M_{OUT} Input Current ..... ±5mA
Operating Junction Temperature Range
LT1248C ..... 0°C to 100°C
LT1248I ..... –40°C to 125°C
Thermal Resistance (Junction-to-Ambient)
N Package ..... 100°C/W
S Package ..... 120°C/W
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP
S PACKAGE
16-LEAD NARROW PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S)

ORDER PART NUMBER

LT1248CN
LT1248IN
LT1248CS
LT1248IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = 7.5V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current (V_{CC} in Undervoltage Lockout)	V_{CC} = Lockout Voltage – 0.2V	●		0.25	0.45	mA
Supply Current (Inactive)	EN/SYNC = 0V, $V_{CC} \le V_{MAX}$	●		0.5	1.5	mA
Supply Current, On	11.5V ≤ $V_{CC} \le V_{MAX}$	●		8.5	12.0	mA
V_{CC} Turn-On Threshold (Undervoltage Lockout)		●	15.5	16.5	17.5	V
V_{CC} Turn-Off Threshold		●	9.5	10.5	11.5	V
EN/SYNC Threshold, Rising		●	2.2	2.6	2.85	V
EN/SYNC Threshold Hysteresis				0.40		V
EN/SYNC Input Current	EN/SYNC = 0V	●	–5	–1	5	µA
	3V ≤ EN/SYNC ≤ 7V		–50	–25	50	µA
Voltage Amplifier						
Voltage Amp Offset Voltage	VA_{OUT} = 3.5V	●	–8		8	mV
Input Bias Current	V_{SENSE} = 0V to 7V	●		–25	–250	nA
Voltage Gain			70	100		dB
Voltage Amp Unity-Gain Bandwidth				3		MHz
Voltage Amp Output High (Internally Clamped)		●	11.3	13.3		V
Voltage Amp Output Low		●		1.1	2	V
Voltage Amp Short-Circuit Current	VA_{OUT} = 0V	●	5	14	30	mA
SS Current	SS = 2.5V	●	5	12	30	µA
Current Amplifier						
Current Amp Offset Voltage		●		±1	±4	mV
I_{SENSE} Bias Current		●		–25	–250	nA
Current Amp Voltage Gain			80	110		dB
Current Amp Unity-Gain Bandwidth				3		MHz
Current Amp Output High		●	7.2	8.5		V
Current Amp Output Low		●		1.1	2	V

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = 7.5V. No load on any outputs, unless otherwise noted.

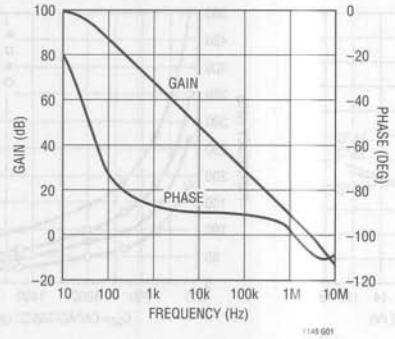
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Amplifier						
Current Amp Short-Circuit Current	CA_{OUT} = 0V	●	5	14	30	mA
Input Range, I_{SENSE}, M_{OUT} (Linear Operation)		●	–0.3		1	V
Reference						
Reference Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.39	7.50	7.60	V
V_{REF} Load Regulation	–5mA < I_{REF} < 0mA			5		mV
V_{REF} Line Regulation	11.5V < V_{CC} < V_{MAX}	●	–20	5	20	mV
V_{REF} Short-Circuit Current	V_{REF} = 0V	●	12	28	50	mA
V_{REF} Worst Case	Load, Line, Temperature	●	7.32	7.5	7.68	V
Current Limit						
PK_{LIM} Offset Voltage		●	–15		15	mV
PK_{LIM} Input Current	PK_{LIM} = –0.1V	●		–50	–100	µA
PK_{LIM} to GTDR Propagation Delay	PK_{LIM} Falling from 50mV to –50mV			400		ns
Multiplier						
Multiplier Output Current	I_{AC} = 100µA, R_{SET} = 15k			35		µA
Multiplier Output Current Offset	R_{AC} = 1M from I_{AC} to GND	●		–0.05	–0.5	µA
Multiplier Maximum Output Current	I_{AC} = 450µA, R_{SET} = 15k, VA_{OUT} = 7V, M_{OUT} = 0V	●	–286	–260	–235	µA
Multiplier Gain Constant (Note 1)				0.035		V^{-2}
I_{AC} Input Resistance	I_{AC} from 50µA to 1mA		15	25	35	kΩ
Oscillator						
Oscillator Frequency	R_{SET} = 15k, C_{SET} = 1000pF	●	85	100	115	kHz
	R_{SET} = 15k, C_{SET} = 1500pF	●	58	68	78	kHz
C_{SET} Ramp Peak-to-Peak Amplitude			4.35	4.7	5.0	V
C_{SET} Ramp Valley Voltage			1.25	1.4	1.55	V
Synchronization Pulse Threshold on EN/SYNC Pin	Pulse Low = 3.5V, High = 7V, Width > 200ns		4.5	5.6	6.5	V
Synchronization Frequency Range	R_{SET} = 15k, C_{SET} = 1000pF	●	1.2		1.6	f_{NOM}
Overvoltage Comparator						
Comparator Trip Voltage Ratio (V_{TRIP}/V_{REF})		●	1.04	1.05	1.06	
Hysteresis				0.35		V
OVP Bias Current	OVP = 7.5V	●		–50	–250	nA
OVP Propagation Delay				100		ns
Gate Driver						
Max GTDR Output Voltage	0mA Load, 18V < V_{CC}	●	12	15	17.5	V
GTDR Output High	–200mA Load, 11.5V ≤ V_{CC} ≤ 15V	●	V_{CC} – 3.0			V
GTDR Output Low (Device Unpowered)	V_{CC} = 0V, 50mA Load (Sinking)	●		0.9	1.5	V
GTDR Output Low (Device Active)	200mA Load (Sinking)	●		0.5	1	V
	10mA Load	●		0.2	0.4	V
Peak GTDR Current	10nF from GTDR to GND			2		A
GTDR Rise and Fall Time	1nF from GTDR to GND			25		ns
GTDR Max Duty Cycle			90	96		%

The ● denotes specifications which apply over the full operating temperature range.

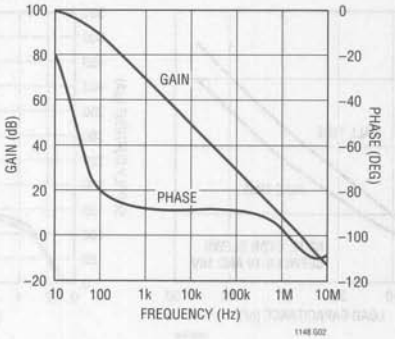
Note 1: Multiplier Gain Constant: $K = \frac{I_M}{I_{AC}(VA_{OUT} - 2)^2}$

TYPICAL PERFORMANCE CHARACTERISTICS

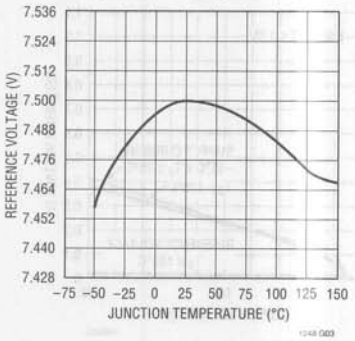
Voltage Amplifier Open-Loop Gain and Phase



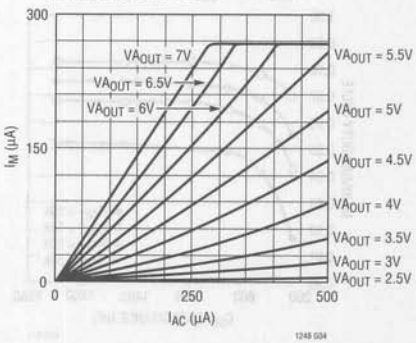
Current Amplifier Open-Loop Gain and Phase



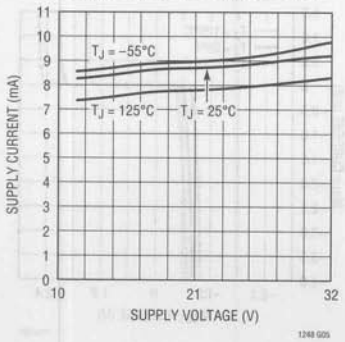
Reference Voltage vs Temperature



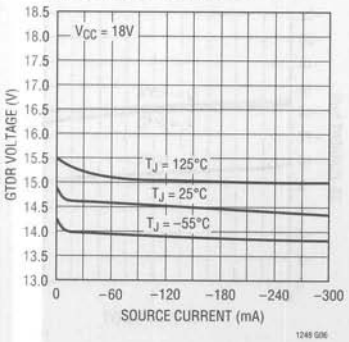
Multiplier Current



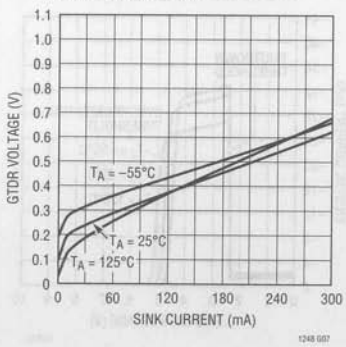
Supply Current vs Supply Voltage



GTDR Source Current



GTDR Sink Current



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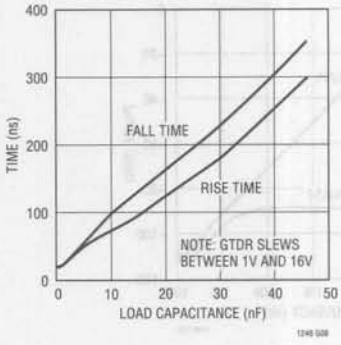
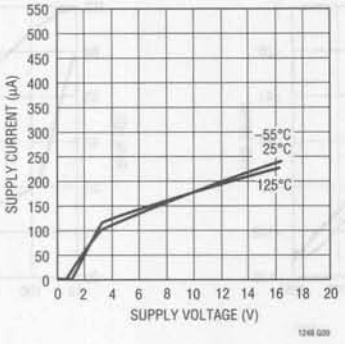
TYPICAL PERFORMANCE CHARACTERISTICS

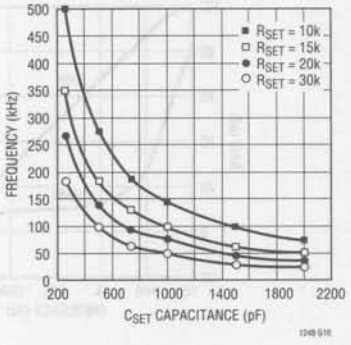
GTDR Rise and Fall Time



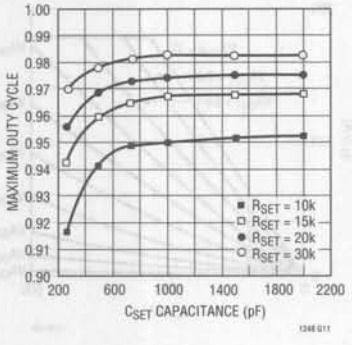
Startup Supply Current vs Supply Voltage



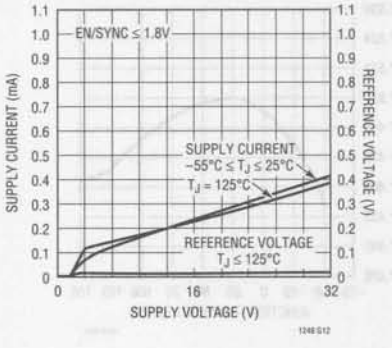
Frequency vs R_{SET} and C_{SET}



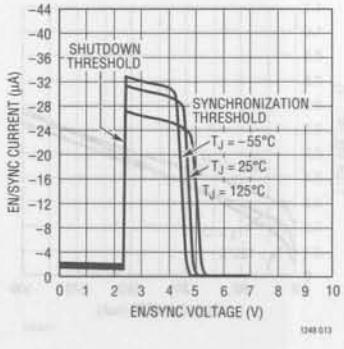
GTDR Maximum Duty Cycle vs R_{SET} and C_{SET}



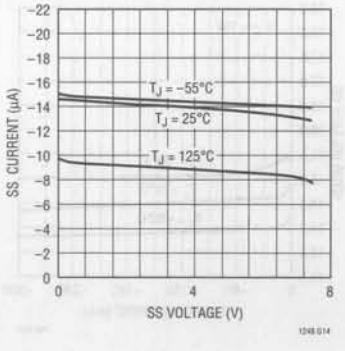
Shutdown Mode Supply Current and Reference Voltage



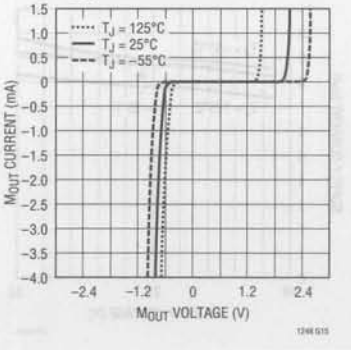
Synchronization and Shutdown Thresholds at EN/SYNC Pin



SS Pin Characteristics

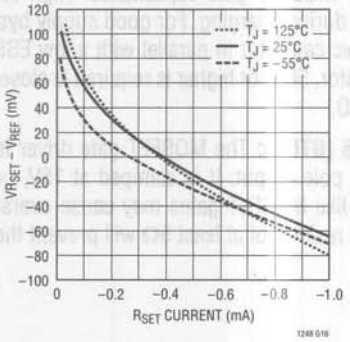


M_{OUT} Pin Characteristics

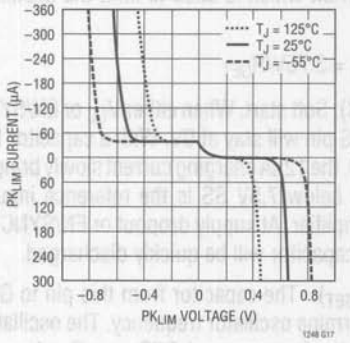


TYPICAL PERFORMANCE CHARACTERISTICS

R_{SET} Voltage vs Current



PK_{LIM} Pin Characteristics



PIN FUNCTIONS

Pin 1 (GND).

Pin 2 (PK_{LIM}): The threshold of the peak current limit comparator is GND. To set current limit, a resistor divider can be connected from V_{REF} to current sense resistor.

Pin 3 (CA_{OUT}): This is the output of the current amplifier that senses and forces the line current to follow the reference signal that comes from the multiplier by commanding the pulse width modulator. When CA_{OUT} is low, the modulator has zero duty cycle.

Pin 4 (I_{SENSE}): This is the inverting input of the current amplifier. This pin is clamped at –0.6V by an ESD protection diode.

Pin 5 (M_{OUT}): This is the multiplier high impedance current output and the noninverting input of the current amplifier. This pin is clamped at –0.6V and 2V.

Pin 6 (I_{AC}): This is the AC line voltage sensing input to the multiplier. It is a current input that is biased at 2V to minimize the crossover dead zone caused by low line voltage. At the pin, a 25k resistor is in series with the current input, so that a lowpass RC can be used to filter out the switching noise from the high impedance lines.

Pin 7 (VA_{OUT}): This is the output of the voltage error amplifier. The output is clamped at 13.5V. When the output goes below 2.5V, the multiplier output current is zero.

Pin 8 (OVP): This is the input to the overvoltage comparator. The threshold is 1.05 times the reference voltage. When the comparator trips, the multiplier is quickly inhibited and outputs no current. Figure 4 in the Applications Information section shows how to set overvoltage threshold with only one additional resistor.

Pin 9 (V_{REF}): This is the 7.5V reference. When either V_{CC} or EN/SYNC goes low, V_{REF} will stay at 0V. V_{REF} biases most of the internal circuitry and can source up to 5mA externally.

Pin 10 (EN/SYNC): This pin has two functions. When it goes below 2.6V, the chip goes into shutdown mode and draws little current. Pulses at this pin that go below the 5V threshold will synchronize the chip. The synchronizing pulses should have an on-time of at least 200ns for the LT1248 resetting circuit to work.

Pin 11 (V_{SENSE}): This is the inverting input to the voltage amplifier.

PIN FUNCTIONS

Pin 12 (R_{SET}): A resistor from R_{SET} to GND sets the oscillator charging current and the maximum multiplier output current which is used to limit the maximum line current.

$$I_{M(MAX)} = 3.75V/R_{SET}$$

Pin 13 (SS): Soft start. When either V_{CC} or EN/SYNC goes low, the SS pin will stay at 0V. With a capacitor from the pin to GND, the 12μA charging current slowly brings up the SS to 8V; below 7.5V SS is the reference input to the voltage amplifier. At supply dropout or EN/SYNC low, the soft start capacitor will be quickly discharged.

Pin 14 (C_{SET}): The capacitor from this pin to GND, and R_{SET}, determine oscillator frequency. The oscillator ramp is 5V, and the frequency = $1.5/(R_{SET} \times C_{SET})$.

Pin 15 (V_{CC}): This is the supply for the chip. The LT1248 has a very fast gate driver required to fast charge high power MOSFET gate capacitance. High current spikes occur during charging. For good supply bypass, a 0.1μF ceramic capacitor in parallel with a low ESR electrolytic capacitor, 56μF or higher is required in close proximity to IC GND.

Pin 16 (GTDR): The MOSFET gate driver is a 1.5A fast totem pole output. It is clamped at 15V, but capacitive loads like MOSFET gates may cause overshoot. A gate series resistor of at least 5Ω will prevent the overshoot.

APPLICATIONS INFORMATION

Error Amplifier

The error amplifier has a 100dB DC gain and 3MHz unity-gain frequency. The output is internally clamped at 13.5V. The noninverting input is tied to the 7.5V V_{REF} through a diode and can be pulled down from the SS (soft start) pin.

Current Amplifier

The current amplifier has a 110dB DC gain, 3MHz unity-gain frequency, and a 2V/μs slew rate. It is internally clamped at 8.5V. Note that in the current averaging operation, high gain at twice the line frequency is necessary to minimize line current distortion. Because CA_{OUT} may need to swing 5V over one line cycle at high line condition, 14mV AC will be needed at the inputs of the current amplifier for a gain of 350 at 120Hz. Especially at light load when the current loop reference signal is small, lower gain will distort the reference signal and line current. If signal gain at switching frequency is too high, the system behaves more like a current mode system and can cause subharmonic oscillation. Therefore, the current amplifier should be compensated to have a gain of less than 15 at the switching frequency, but more than 250 at twice the line frequency.

Multiplier

The multiplier is a current multiplier with high noise immunity in a high power switching environment. The current gain is: $I_M = (I_{AC} \times I_{EA}^2)/(200\mu A)^2$, with $I_{EA} = (VA_{OUT} - 2V)/25k$. With a square function, because of the lower gain at light power load, system stability is maintained and line current distortion caused by the line frequency AC ripple

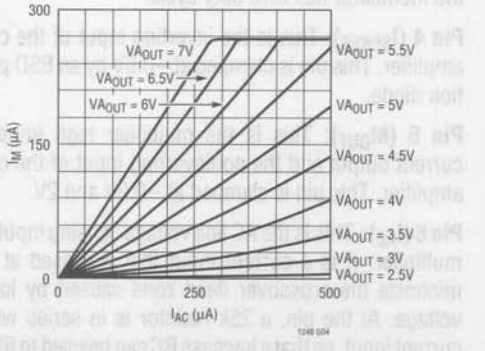


Figure 1. Multiplier Current I_M vs I_{AC} and VA_{OUT}

APPLICATIONS INFORMATION

fed back to the error amplifier is minimized. Note that switching ripple on the high impedance lines could get into the multiplier from the I_{AC} pin and cause instability. The LT1248 provides an internal 25k resistor in series with the low impedance multiplier current input so that only a capacitor from the I_{AC} pin to GND is needed to filter out the noise. The maximum multiplier output current, which limits the system line current, is set by the R_{SET} according to the formula: $I_{M(MAX)} = 3.75V/R_{SET}$.

Oscillator Frequency and Maximum Line Current Settling

Oscillator frequency is set by R_{SET} and C_{SET}. Ramp amplitude is 5V and C_{SET} charging current is set by V_{REF}/R_{SET}. Typical discharging time for C_{SET} = 1nF is 250ns. R_{SET} should always be determined first to set the maximum multiplier output current for system line current limit. For a 300W preregulator, with R_{SET} = 15k, $I_{M(MAX)}$ = 3.75V/15k = 250μA. With a 4k resistor R_{REF} from M_{OUT} to the 0.2Ω line current sense resistor R_S, the line current limit is: $(I_M \times 4k)/R_S$. As a general rule, R_S is chosen according to:

$$R_S = \frac{I_{M(MAX)} \times R_{REF} \times V_{LINE(MIN)}}{K(1.414)P_{OUT(MAX)}}$$

where $P_{OUT(MAX)}$ is the maximum power output and K is usually between 1.1 and 1.3 depending on efficiency and resistor tolerance. With R_{SET} selected, C_{SET} can then be determined by: $C_{SET} = 1.5/(\text{Frequency} \times R_{SET})$. For 100kHz, C_{SET} = 1.5/(100kHz × 15k) = 1nF. For optional double protection, the LT1248 provides a current limit comparator. When the comparator trips at 0V, the GTDR pin quickly goes low to shut off the MOS switch. A resistor divider from V_{REF} to R_S (Figure 2) senses the voltage across the line current sense resistor and the current limit is set by: $I_{LINE} = [(7.5V/R1) + 50\mu A](R2/R_S)$, where 50μA is I_{PKLIM}.

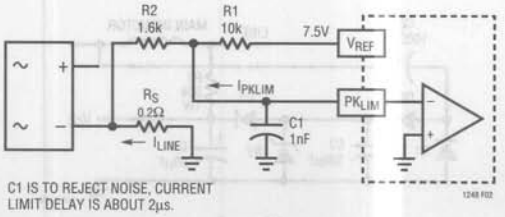


Figure 2.

With I_{LINE} and R_S chosen, let R1 = 10k, then R2 = $(I_{LINE} \times R_S)/0.8mA$.

Always use R_{SET} to set the primary line current limit. The PK_{LIM} comparator is only for secondary protection. The secondary limit should be higher than the primary limit; 6.5A is good (5A for primary limit) for a 300W regulator. When line current reaches the primary limit, V_{OUT} drops to keep the line current constant, and system stability is still maintained by the current loop which is controlled by the current amplifier. When line current reaches the secondary limit, the comparator controls the system and loop hysteresis may occur and can cause audible noise.

Synchronization

The LT1248 can be synchronized to a frequency that is up to 1.6 times the natural frequency. With a 200ns one-shot timer on-chip, the LT1248 provides flexibility on the synchronizing pulse width. Because the EN/SYNC pin also serves the chip shutdown function, the pulses at the pin should not go below 3V and must go below 5V with widths greater than 200ns. The Figure 3 circuit will synchronize the LT1248.

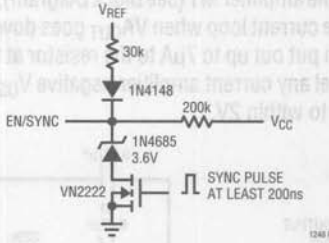


Figure 3.

Overvoltage Protection

Because of the slow loop response necessary for power factor correction, output overshoot can occur with sudden load removal or reduction. To protect the power components and output load, the LT1248 provides an overvoltage comparator which senses the output voltage and quickly shuts off the current switch. In Figure 4, because there is no DC current going through R3, R1 and R2 set the regulator output DC level: $V_{OUT} = V_{REF}[(R1 + R2)/R2]$, with R1 = 1M, R2 = 20k, V_{OUT} is 382V.

APPLICATIONS INFORMATION

Note that V_{SENSE} is the summing node and it stays at 7.5V. When overshoot occurs on V_{OUT}, the overcurrent from R1 will go through R2 as well as R3. Amplifier feedback will keep V_{SENSE} locked at 7.5V. The equivalent AC resistance, seen by the comparator input pin OVP, is R2 in parallel with R3, which is 10k. Therefore, with the comparator trip level of $1.05V_{REF}$ and R3 of 20k, the comparator trips when V_{OUT} overshoot exceeds 10%. Overvoltage trip level:

$$\%V_{OUT} = 5\%\left(\frac{R2+R3}{R3}\right)$$

M_{OUT} is a high impedance current output. In the current loop, offset line current is determined by multiplier offset current and input offset voltage of the current amplifier. A −4mV current amplifier V_{OS} translates into 20mA line current and 5W input power for 250V line if 0.2Ω sense resistor is used. Under no load or when the load power is less than this offset input power, V_{OUT} would slowly charge up to an overvoltage state because the overvoltage comparator can only reduce multiplier output current to zero. This does not guarantee zero output current if the current amplifier has offset. To regulate V_{OUT} under this condition, the amplifier M1 (see Block Diagram), becomes active in the current loop when VA_{OUT} goes down to 2.2V. The M1 can put out up to 7μA to the resistor at the I_{SENSE} pin to cancel any current amplifier negative V_{OS} and keep V_{OUT} error to within 2V.

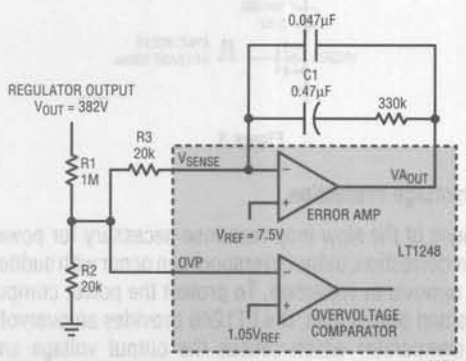


Figure 4.

Undervoltage Lockout

The LT1248 turns on when V_{CC} is higher than 16V and remains on until V_{CC} falls below 10V, whereupon the chip enters the lockout state. In the lockout state, the LT1248 only draws 250μA, the oscillator is off, and the V_{REF} and the GTDR pins remain low to keep the power MOSFET off.

Start-Up and Supply Voltage

The LT1248 draws only 250μA before the chip starts at 16V on V_{CC}. To trickle start, a 90k resistor from the power line to V_{CC} supplies the trickle current and C4 holds the V_{CC} up while switching starts. Then the auxiliary winding takes over and supplies the operating current. Note that D3 and the large value C3, in both Figures 5 and 6, are only necessary for systems that have sudden large load variation down to minimum load and/or very light load conditions. Under these conditions, the loop may exhibit a start/restart mode because switching remains off long enough for C4 to discharge below 10V. The C3 will hold V_{CC} up until switching resumes. For less severe load variations, D3 is replaced with a short and C3 is omitted. The turns ratio between the primary winding and the auxiliary winding determines V_{CC} according to:

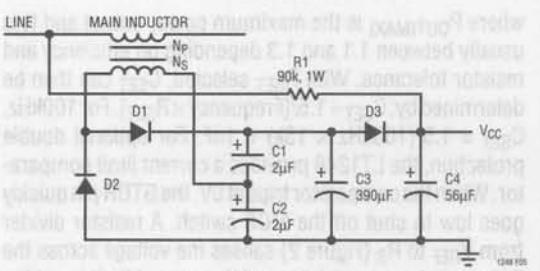


Figure 5.

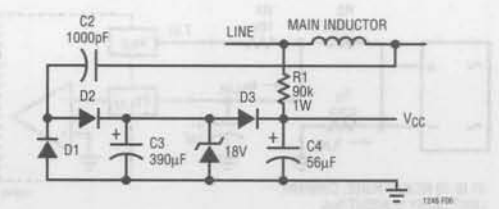


Figure 6.

APPLICATIONS INFORMATION

$V_{OUT}/(V_{CC} - 2V) = N_P/N_S$.

For 382V V_{OUT} and 18V V_{CC}, Np/Ns ≈ 19.

In Figure 6, a new technique for supply voltage eliminates the need for an extra inductor winding. It uses capacitor charge transfer to generate a constant current source which feeds a Zener diode. Current to the Zener is equal to $(V_{OUT} - V_Z)(C)(f)$, where V_Z is Zener voltage and f is switching frequency. For V_{OUT} = 382V, V_Z = 18V, C = 1000pF, and f = 100kHz, Zener current will be 36mA. This is enough to operate the LT1248, including the FET gate drive. Normally soft start is not needed because the LT1248 has overcurrent limit and overvoltage protection. If soft start is used with a 0.01µF capacitor on SS pin, V_{OUT} ramps up slower during startup. Then C4 has to hold V_{CC} longer, and the circuit may not start. Increasing C4 to 100µF ensures startup, but startup time will be extended if the same 90k trickle charge resistor is used.

Output Capacitor

The peak-to-peak 120Hz output ripple is determined by:

$V_{P-P} = (2)\ (I_{LOAD(DC)})(Z)$

where $I_{LOAD(DC)}$: DC load current.

Z: capacitor impedance at 120Hz.

For 180µF at 300W load, $I_{LOAD(DC)}$ = 300W/385V = 0.78A, $V_{PP} = 2 \times 0.78A \times 7.4\Omega = 11.5V$. If less ripple is desired, higher capacitance should be used. The selection of the output capacitor should also be based on the operating ripple current through the capacitor. The ripple current can be divided into three major components. The first is at 120Hz; it's RMS value is related to the DC load current as follows,

$I_{1RMS} \approx 0.71 \times I_{LOAD(DC)}$

The second component contains the PF switching frequency ripple current and its harmonics. Analysis of the ripple is complicated because it is modulated with a 120Hz signal. However computer numerical integration and Fourier analysis approximate the RMS value reasonably close to the bench measurements. The RMS value is about 0.82A at a typical condition of 120VAC, 200W load. This ripple is line-voltage dependent, and the worst case is at low line.

I_{2RMS} = 0.82A at 120VAC, 200W

The third component is the switching ripple from the load, if the load is a switching regulator.

$I_{3RMS} \approx I_{LOAD(DC)}$

For the United Chemicon KMH 400V capacitor series, ripple current multiplier for currents at 100kHz is 1.43. The equivalent 120Hz ripple current can be then found:

$$I_{RMS} = \sqrt{(I_{1RMS})^2 + (I_{2RMS}/1.43)^2 + (I_{3RMS}/1.43)^2}$$

For a typical system that runs at an average load of 200W and 385V output:

$I_{LOAD(DC)} = 0.52A$

$I_{1RMS} \approx 0.71 \times 0.52A = 0.37A$

$I_{2RMS} \approx 0.82A$ at 120VAC

$I_{3RMS} \approx I_{LOAD(DC)} = 0.52A$

$$I_{RMS} = \sqrt{(0.37A)^2 + (0.82A/1.43)^2 + (0.52A/1.43)^2} = 0.77A$$

The 120Hz ripple current rating at 105°C ambient is 0.95A for the 180µF KMH 400V capacitor. The expected life of the output capacitor may be calculated from the thermal stress analysis:

$$L = L_0 \times 2^{\frac{(105°C + \Delta TK) - (TA + \Delta TO)}{10}}$$

where:

L: expected life time

L_0: hours of load life at rated ripple current and rated ambient temperature.

ΔT_K: Capacitor internal temperature rise at rated condition. $\Delta T_K = (I^2R)/(KA)$. Where I is the rated current, R is capacitor ESR, and KA is a volume constant.

T_A: Operating ambient temperature.

ΔT_O: Capacitor internal temperature rise at operating condition.

In our example L_0 = 2000 hours and ΔT_K = 10°C at rated 0.95A. ΔT_O can then be calculated from:

$$\Delta T_K = (I_{RMS}/0.95A)^2 \times \Delta T_K = (0.77A/0.95A)^2 \times 10°C = 6.6°C$$

Assuming the operating ambient temperature is 60°C, the approximate life time is:

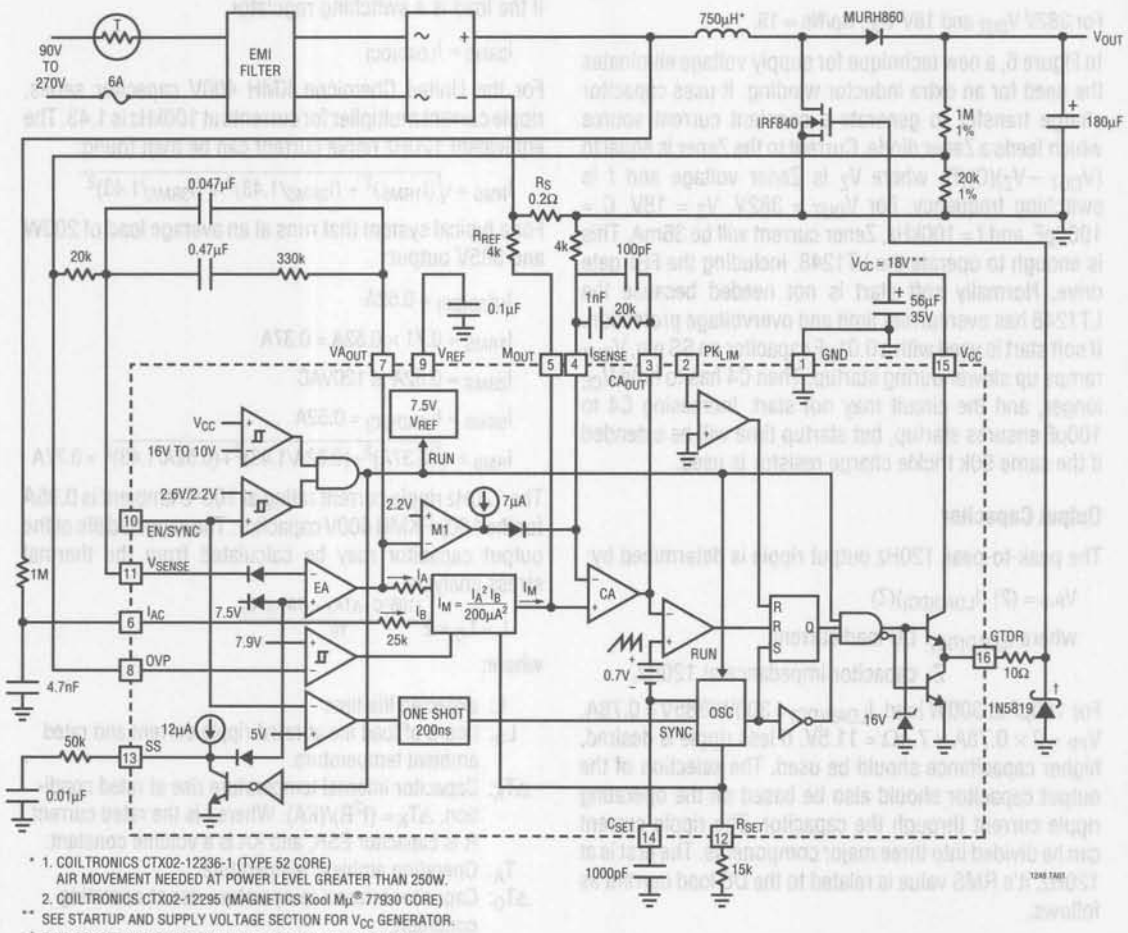
$$L_0 \approx 2000 \times 2^{\frac{(105°C + 10°C) - (60° + 6.6°C)}{10}} \approx 57{,}000 \text{ hours}$$

For longer life, a capacitor with a higher ripple current rating or parallel capacitors should be used.

4

TYPICAL APPLICATION

300W, 382V Preregulator



* 1. COILTRONICS CTX02-12236-1 (TYPE 52 CORE)
AIR MOVEMENT NEEDED AT POWER LEVEL GREATER THAN 250W.
2. COILTRONICS CTX02-12295 (MAGNETICS Kool Mµ® 77930 CORE)

** SEE STARTUP AND SUPPLY VOLTAGE SECTION FOR V_{CC} GENERATOR.

† THIS SCHOTTKY DIODE IS TO CLAMP GTDR WHEN MOS SWITCH TURNS OFF. PARASITIC INDUCTANCE AND GATE CAPACITANCE MAY TURN ON CHIP SUBSTRATE DIODE AND CAUSE ERRATIC OPERATIONS IF GTDR IS NOT CLAMPED.

Kool Mµ is a registered trademark of Magnetics, Inc.

Power Factor Controller

FEATURES

- **Standard 8-Pin Packages**
- **High Power Factor Over Wide Load Range with Line Current Averaging**
- International Operation Without Switches
- Instantaneous Overvoltage Protection
- Minimal Line Current Dead Zone
- Typical 250µA Start-Up Supply Current
- Rejects Line Switching Noise
- Synchronization Capability
- Low Quiescent Current: 9mA
- Fast 1.5A Peak Current Gate Driver

APPLICATIONS

- Universal Power Factor Corrected Power Supplies
- Preregulators up to 1500W

DESCRIPTION

The 8-pin LT1249 provides active power factor correction for universal off-line power systems with very few external parts. By using fixed high frequency PWM current averaging without the need for slope compensation, the LT1249 achieves far lower line current distortion, with a smaller magnetic element than systems that use either peak current detection or zero current switching approach, in both continuous and discontinuous modes of operation.

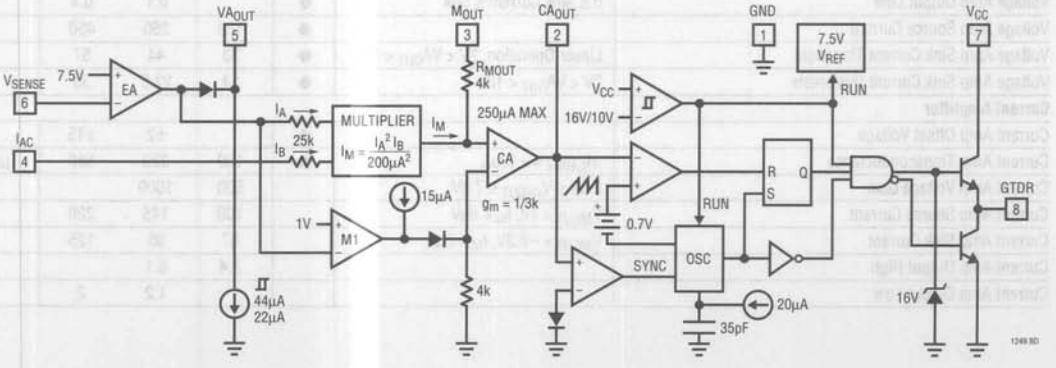
The LT1249 uses a multiplier that has a square gain function from the voltage amplifier to reduce the AC gain at light output load and thus maintains low line current distortion and high system stability. The LT1249 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1249 provides many protection features including peak current limiting and overvoltage protection. The switching frequency is internally set at 100kHz.

While the LT1249 simplifies PFC design with minimal parts count, the LT1248 provides flexibilities in switching frequency, overvoltage, and current limit.

4

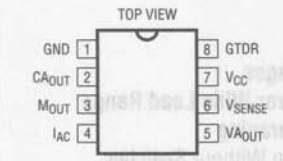
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 27V
GTDR Current Continuous 0.5A
GTDR Output Energy(Per Cycle) 5µJ
I_{AC} Input Current 20mA
V_{SENSE} Input Voltage ..... V_{MAX}
M_{OUT} Input Current ..... ±5mA
Operating Junction Temperature Range
LT1249C ..... 0°C to 100°C
LT1249I ..... –40°C to 125°C
Thermal Resistance (Junction-to-Ambient)
N Package ..... 100°C/W
S Package ..... 120°C/W
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S)

ORDER PART NUMBER
LT1249CN8 LT1249IN8 LT1249CS8 LT1249IS8
S8 PART MARKING
1249 1249I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, I_{AC} = 100µA, CA_{OUT} = 3.5V, VA_{OUT} = 5V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current (V_{CC} in Undervoltage Lockout)	V_{CC} = Lockout Voltage – 0.2V	●		0.25	0.45	mA
Supply Current, On	11.5V ≤ V_{CC} ≤ V_{MAX}	●		8	12	mA
V_{CC} Turn-On Threshold		●	15.5	16.5	17.5	V
V_{CC} Turn-Off Threshold		●	9.5	10.5	11.5	V
Voltage Amplifier						
V_{SENSE} Bias Current	V_{SENSE} = 0V to 7V	●		–25	–250	nA
Voltage Amp Gain			70	100		dB
Voltage Amp Unity-Gain Bandwidth				1.5		MHz
Voltage Amp Output High	0 ≤ Source Current ≤ 50µA	●	10	12		V
Voltage Amp Output Low	0 ≤ Sink Current ≤ 5µA	●		0.1	0.4	V
Voltage Amp Source Current		●	130	260	450	µA
Voltage Amp Sink Current Threshold	Linear Operation, 2V < VA_{OUT} < 10V	●	33	44	57	µA
Voltage Amp Sink Current Hysteresis	2V < VA_{OUT} < 10V	●	14	22.5	30	µA
Current Amplifier						
Current Amp Offset Voltage		●		±2	±15	mV
Current Amp Transconductance	ΔI_{CAOUT} = ±40µA	●	150	320	550	µmho
Current Amp Voltage Gain	2.5V ≤ V_{CAOUT} ≤ 7.5V		500	1000		V/V
Current Amp Source Current	V_{MOUT} = 1V, I_M = 0µV		100	145	220	µA
Current Amp Sink Current	V_{MOUT} = –0.3V, I_M = 0µA		67	95	125	µA
Current Amp Output High			7.4	8.1		V
Current Amp Output Low				1.2	2	V

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, I_{AC} = 100µA, CA_{OUT} = 3.5V, VA_{OUT} = 5V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Output Voltage	T_A = 25°C, Measured at V_{SENSE} Pin		7.39	7.5	7.6	V
Reference Output Voltage Worst Case	All Line, Temperature	●	7.32	7.5	7.68	V
Reference Output Voltage Line Regulation	$V_{LOCKOUT} < V_{CC} < V_{MAX}$	●	−20	5	20	mV
Multiplier						
Multiplier Output Current	I_{AC} = 100µA, VA_{OUT} = 5V			35		µA
Multiplier Output Current Offset	R_{AC} = 1M from I_{AC} to GND	●		−0.05	−0.5	µA
Multiplier Max Output Current ($I_{M(MAX)}$)	I_{AC} = 450µA, VA_{OUT} = 7V (Note 1)	●	−375	−250	−150	µA
Multiplier Max Output Voltage ($I_{M(MAX)} \times R_{MOUT}$)	I_{AC} = 450µA, VA_{OUT} = 7V (Note 1)	●	−1.25	−1.1	−0.96	V
Multiplier Gain Constant (Note 2)				0.035		V^{-2}
I_{AC} Input Resistance	I_{AC} from 50µA to 1mA		15	25	35	kΩ
Oscillator						
Oscillator Frequency		●	75	100	125	kHz
Control Pin (CA_{OUT}) Threshold	Duty Cycle = 0	●	1.3	1.8	2.3	V
Synchronization Frequency Range	Synchronizing Pulse Low ≤ 0.35V on CA_{OUT}	●	127		160	kHz
Gate Driver						
Max GTDR Output Voltage	0mA Load, 18V < V_{CC} < V_{MAX} (Note 3)	●	12	15	17.5	V
GTDR Output High	−200mA Load, 11.5V ≤ V_{CC} ≤ 15V	●	V_{CC} − 3.0			V
GTDR Output Low (Device Unpowered)	V_{CC} = 0V, 50mA Load (Sinking)	●		0.9	1.5	V
GTDR Output Low (Device Active)	200mA Load (Sinking)	●		0.5	1	V
Peak GTDR Current	10nF from GTDR to GND			2		A
GTDR Rise and Fall Time	1nF from GTDR to GND			25		ns
GTDR Max Duty Cycle			90	96		%

The ● denotes specifications which apply over the operating temperature range.

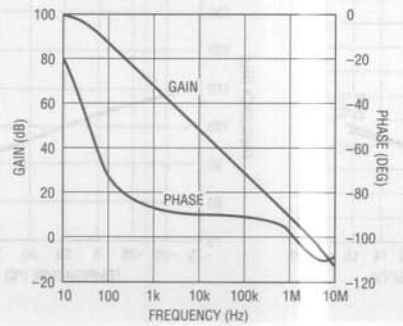
Note 1: Current amplifier is in linear mode with 0V input common mode.

Note 2: Multiplier Gain Constant: $K = \frac{I_M}{I_{AC}(VA_{OUT} - 1.5)^2}$

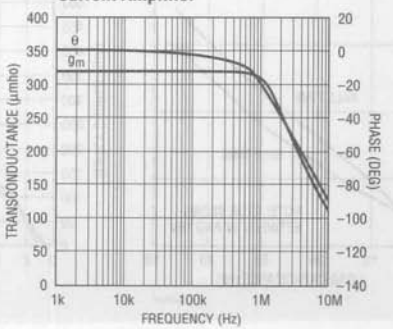
Note 3: Maximum GTDR output voltage is internally clamped for higher V_{CC} voltages.

TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Amplifier Open-Loop Gain and Phase

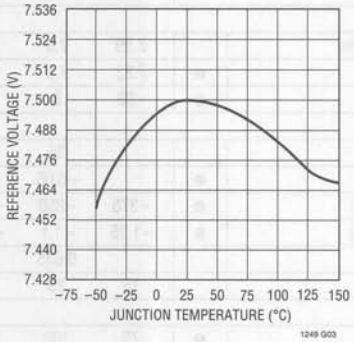


Transconductance of Current Amplifier

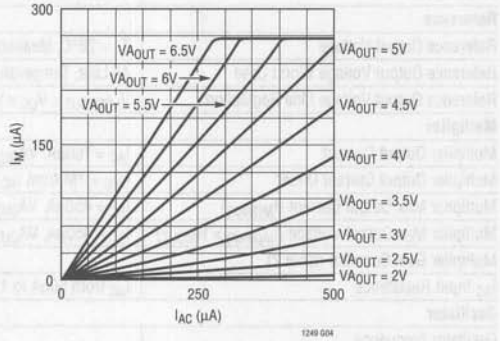


TYPICAL PERFORMANCE CHARACTERISTICS

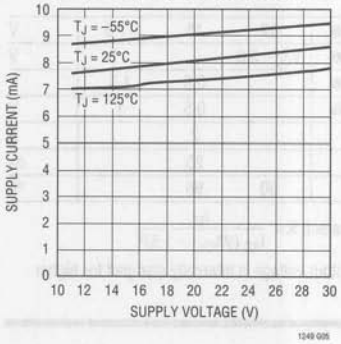
Reference Voltage vs Temperature



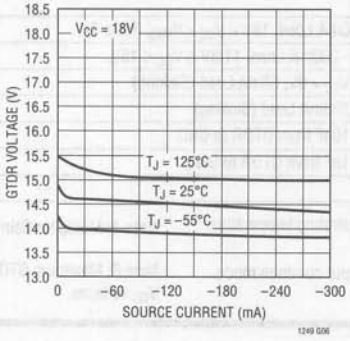
Multiplier Current



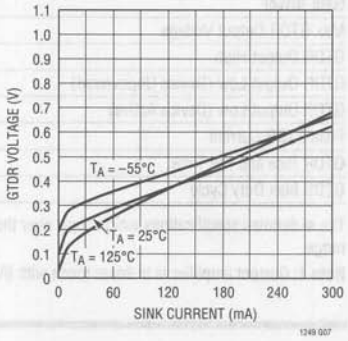
Supply Current vs Supply Voltage



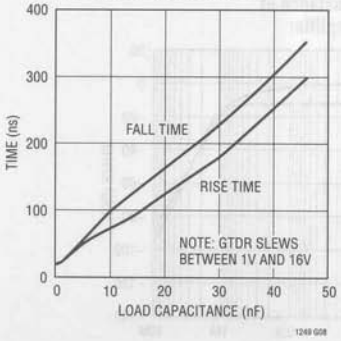
GTDR Source Current



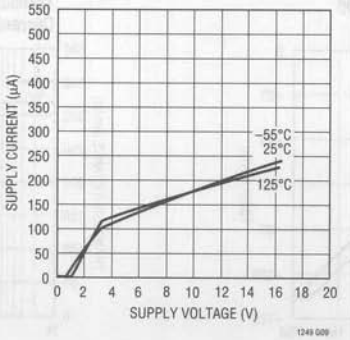
GTDR Sink Current



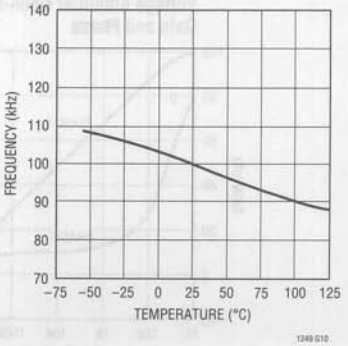
GTDR Rise and Fall Time



Start-Up Supply Current vs Supply Voltage

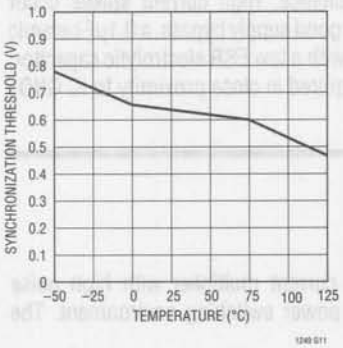


Switching Frequency

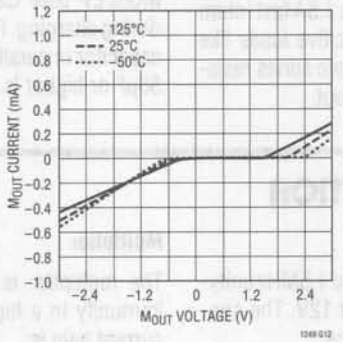


TYPICAL PERFORMANCE CHARACTERISTICS

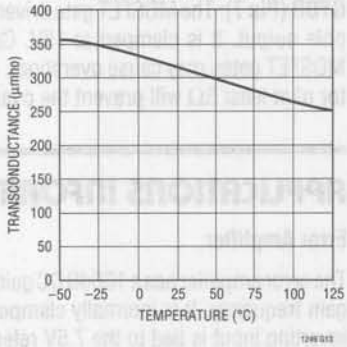
Synchronization Threshold at CA_{OUT}



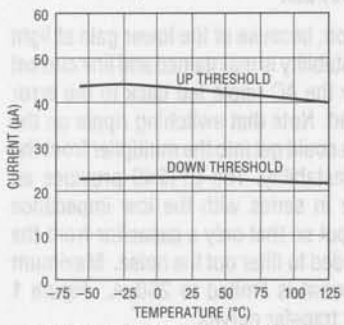
M_{OUT} Pin Characteristics



Transconductance of Current Amplifier Over Temperature

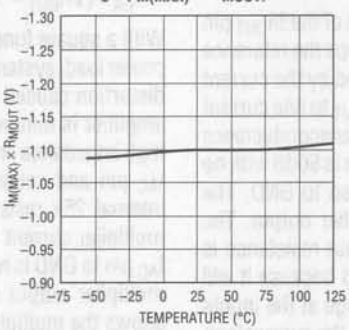


Voltage Amp Sink Current Limits (Threshold)

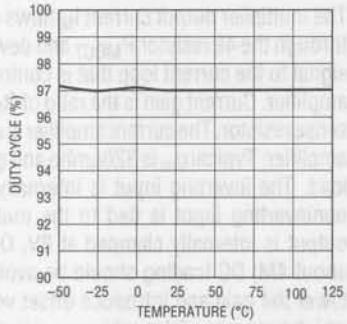


NOTE: THESE SINK CURRENT THRESHOLDS ARE FOR OVERVOLTAGE PROTECTION FUNCTION. 1249 G14

Maximum Multiplier Output Voltage ($I_{M(MAX)} \times R_{MOUT}$)



Maximum Duty Cycle



4

PIN FUNCTIONS

GND (Pin 1): Ground.

CA_{OUT} (Pin 2): This is the output of the current amplifier that senses and forces the line current to follow the reference signal that comes from the multiplier by commanding the pulse width modulator. When CA_{OUT} is low, the modulator has zero duty cycle.

M_{OUT} (Pin 3): The multiplier current goes out of this pin through the 4k resistor R_{MOUT}. The voltage developed across R_{MOUT} is the reference voltage of the current loop and it is limited to 1.1V. The noninverting input of the current amplifier is also tied to R_{MOUT}. In operation, M_{OUT} is normally at negative potential and only AC signals appear at the noninverting input of the current amplifier.

I_{AC} (Pin 4): This is the AC line voltage sensing input to the multiplier. It is a current input that is biased at 2V to minimize the crossover dead zone caused by low line voltage. A 25k resistor is in series with the current input, so that a small external capacitor can be used to filter out the switching noise from the high impedance lines.

VA_{OUT} (Pin 5): This is the output of the voltage error amplifier. The output is clamped at 12V. When the output goes below 1.5V, the multiplier output current is zero.

PIN FUNCTIONS

V_{SENSE} (Pin 6): This is the inverting input to the voltage amplifier.

GTDR (Pin 7): The MOSFET gate driver is a 1.5A fast totem pole output. It is clamped at 15V. Capacitive loads like MOSFET gates may cause overshoot. A gate series resistor of at least 5Ω will prevent the overshoot.

V_{CC} (Pin 8): This is the supply of the chip. The LT1249 has a very fast gate driver required to fast charge high power MOSFET gate capacitance. High current spikes occur during charging. For good supply bypass, a 0.1µF ceramic capacitor in parallel with a low ESR electrolytic capacitor, 56µF or higher is required in close proximity to IC GND.

APPLICATIONS INFORMATION

Error Amplifier

The error amplifier has a 100dB DC gain and 1.5MHz unity-gain frequency. It is internally clamped at 12V. The non-inverting input is tied to the 7.5V reference.

Current Amplifier

The multiplier output current I_M flows out of the M_{OUT} pin through the 4k resistor R_{MOUT} and develops the reference signal to the current loop that is controlled by the current amplifier. Current gain is the ratio of R_{MOUT} to line current sense resistor. The current amplifier is a transconductance amplifier. Typical g_m is 320µmho and gain is 60dB with no load. The inverting input is internally tied to GND. The noninverting input is tied to the multiplier output. The output is internally clamped at 8V. Output resistance is about 4M; DC loading should be avoided because it will lower the gain and introduce offset voltage at the inputs which becomes a false reference signal to the current loop and can distort line current. Note that in the current averaging operation, high gain at twice the line frequency is necessary to minimize line current distortion. Because CA_{OUT} may need to swing 5V over one line cycle at high line condition, 11mV will be present at the inputs of the current amplifier if gain is rolled off to 450 at 120Hz (1nF in series with 10k at CA_{OUT}). At light load, when $(I_M)(R_{MOUT})$ can be less than 100mV, lower gain will distort the current loop reference signal and line current. If signal gain at the 100kHz switching frequency is too high, the system behaves more like a current mode system and can cause subharmonic oscillation. Therefore, the current amplifier should be compensated to have a gain of less than 15 at 100kHz and more than 300 at 120Hz.

Multiplier

The multiplier is a current multiplier with high noise immunity in a high power switching environment. The current gain is:

$$I_M = (I_{AC} \times I_{EA}^2)/(200\mu A)^2, \text{ and}$$
$$I_{EA} = (VA_{OUT} - 1.5V)/25k$$

With a square function, because of the lower gain at light power load, system stability is maintained and line current distortion caused by the AC ripple fed back to the error amplifier is minimized. Note that switching ripple on the high impedance lines could get into the multiplier from the I_{AC} pin and cause instability. The LT1249 provides an internal 25k resistor in series with the low impedance multiplier current input so that only a capacitor from the I_{AC} pin to GND is needed to filter out the noise. Maximum multiplier output current is limited to 250µA. Figure 1 shows the multiplier transfer curves.

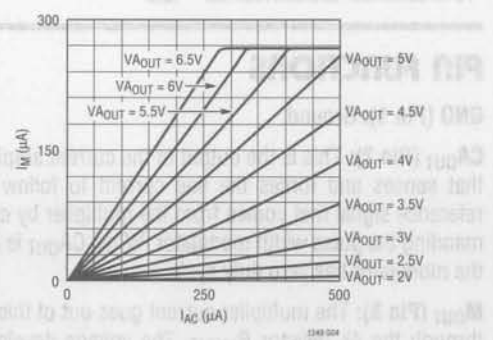


Figure 1. Multiplier Current I_M vs I_{AC} and VA_{OUT}

APPLICATIONS INFORMATION

Line Current Limiting

Maximum voltage across R_{MOUT} is internally limited to 1.1V. Therefore, line current limit is 1.1V divided by the sense resistor R_S. With a 0.2Ω sense resistor R_S line current limit is 5.5A. As a general rule, R_S is chosen according to:

$$R_S = \frac{I_{M(MAX)} \times R_{MOUT} \times V_{LINE(MIN)}}{K(1.414)P_{OUT(MAX)}}$$

where $P_{OUT(MAX)}$ is the maximum power output and K is usually between 1.1 and 1.3 depending on efficiency and resistor tolerance. When the output is overloaded and line current reaches limit, output voltage V_{OUT} will drop to keep line current constant. System stability is still maintained by the current loop which is controlled by the current amplifier. Further load current increase results in further V_{OUT} drop and clipping of the line current, which degrades power factor.

Synchronization

The LT1249 can be externally synchronized in a frequency range of 127kHz to 160kHz. Figure 2 shows the synchronizing circuit. Synchronizing occurs when CA_{OUT} pin is pulled below 0.5V with an external transistor and a Schottky diode. The Schottky diode and the 10k pull-up resistor are necessary for the required fast slewing back up to the normal operating voltage on CA_{OUT} after the transistor is turned off. Positive slewing on CA_{OUT} should be faster than the oscillator ramp rate of 0.5V/μs.

The width of the synchronizing pulse should be under 60ns. The synchronizing pulses introduce an offset voltage on the current amplifier inputs, according to:

$$\Delta V_{OS} = \frac{(ts)(fs)\left(I_C + \frac{V_C - 0.5}{R2}\right)}{g_m}$$

ts = pulse width
fs = pulse frequency
I_C = CA_{OUT} source current (≈ 150μA)
V_C = CA_{OUT} operating voltage (1.8V to 6.8V)
R2 = resistor for the mid-frequency "zero" in the current loop
g_m = current amplifier transconductance (≈ 320μmho)

With ts = 30ns, fs = 130kHz, V_C = 3V, and R2 = 10k, offset voltage shift is ≈5mV. Note that this offset voltage will add slight distortion to line current at light load.

Figure 2. Synchronizing the LT1249

Overvoltage Protection

In Figure 3, R1 and R2 set the regulator output DC level: $V_{OUT} = V_{REF}[(R1 + R2)/R2]$. With R1 = 1M, R2 = 20k, V_{OUT} is 382V.

Because of the slow loop response necessary for power factor correction, output overshoot can occur with sudden load removal or reduction. To protect the power components and output load, the LT1249 voltage error amplifier senses the output voltage and quickly shuts off the current switch when overvoltage occurs. When overshoot occurs on V_{OUT}, the overcurrent from R1 will go through VA_{OUT} because amplifier feedback keeps V_{SENSE} locked at 7.5V. When this overcurrent reaches 44μA amplifier sinking limit, the amplifier loses feedback and its output snaps low to turn the multiplier off.

Overvoltage trip level: $\Delta V_{OUT} = 44\mu A \times R1$

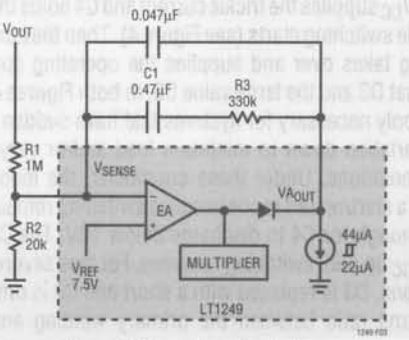


Figure 3. Overvoltage Protection

APPLICATIONS INFORMATION

The Figure 3 circuit therefore has 382V on V_{OUT}, and an overvoltage level = (V_{OUT} + 44V), or 426V. With a 22µA hysteresis, V_{OUT} then has to drop 22V to 404V before feedback recovers and the switch turns back on.

M_{OUT} is a high impedance current output. In the current loop, offset line current is determined by multiplier offset current and input offset voltage of the current amplifier. A negative 4mV current amplifier V_{OS} translates into 20mA line current and 5W input power for 250V line if 0.2Ω sense resistor is used. Under no load or when the load power is less than this offset input power, V_{OUT} would slowly charge up to an overvoltage state because the overvoltage comparator can only reduce multiplier output current to zero. This does not guarantee zero output current if the current amplifier has offset. To regulate V_{OUT} under this condition, the amplifier M1 (see Block Diagram), becomes active in the current loop when VA_{OUT} goes down to 1V. The M1 can put out up to 15µA to the 4k resistor at the inverting input to cancel the current amplifier negative V_{OS} and keep V_{OUT} error to within 2V.

Undervoltage Lockout

The LT1249 turns on when V_{CC} is higher than 16V and remains on until V_{CC} falls below 10V, whereupon the chip enters the lockout state. In the lockout state, the LT1249 only draws 250µA, the oscillator is off, the V_{REF} and the GTDR pins remain low to keep the power MOSFET off.

Start-Up and Supply Voltage

The LT1249 draws only 250µA before the chip starts at 16V on V_{CC}. To trickle start, a 90k resistor from the power line to V_{CC} supplies the trickle current and C4 holds the V_{CC} up while switching starts (see Figure 4). Then the auxiliary winding takes over and supplies the operating current. Note that D3 and the large value C3, in both Figures 4 and 5, are only necessary for systems that have sudden large load variation down to minimum load and/or very light load conditions. Under these conditions, the loop may exhibit a start/restart mode because switching remains off long enough for C4 to discharge below 10V. The C3 will hold V_{CC} up until switching resumes. For less severe load variations, D3 is replaced with a short and C3 is omitted. The turns ratio between the primary winding and the

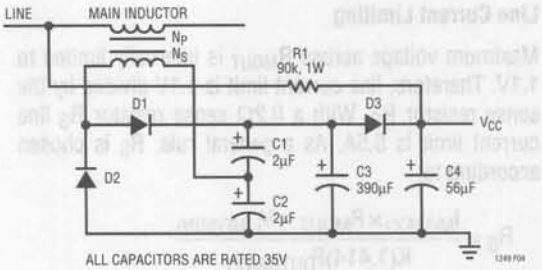


Figure 4. Power Supply for LT1249

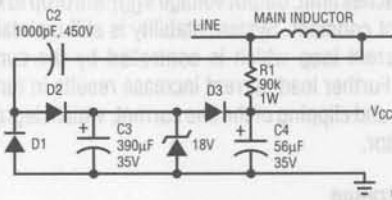


Figure 5. Power Supply for LT1249

auxiliary winding determines V_{CC} according to: $V_{OUT}/(V_{CC} - 2V) = N_P/N_S$. For 382V V_{OUT} and 18V V_{CC}, $N_P/N_S \approx 19$.

In Figure 5 a new technique for supply voltage eliminates the need for an extra inductor winding. It uses capacitor charge transfer to generate a constant current source which feeds a Zener diode. Current to the Zener is equal to $(V_{OUT} - V_Z)(C)(f)$, where V_Z is Zener voltage and f is switching frequency. For V_{OUT} = 382V, V_Z = 18V, C = 1000pF, and f = 100kHz, Zener current will be 36mA. This is enough to operate the LT1249, including the FET gate drive.

Output Capacitor

The peak-to-peak 120Hz output ripple is determined by:

$V_{P-P} = (2)(I_{LOAD}DC)(Z)$

where $I_{LOAD}DC$: DC load current
Z: capacitor impedance at 120Hz

For 180µF at 300W load, $I_{LOAD}DC$ = 300W/385V = 0.78A,

APPLICATIONS INFORMATION

$V_{P-P} = 2 \times 0.78A \times 7.4\Omega = 11.5V$. If less ripple is desired, higher capacitance should be used.

The selection of the output capacitor should also be based on the operating ripple current through the capacitor.

The ripple current can be divided into three major components. The first is at 120Hz whose RMS value is related to the DC load current as follows:

$$I_{1RMS} \approx 0.71 \times I_{LOAD}DC$$

The second component contains the PF switching frequency ripple current and its harmonics. Analysis of this ripple is complicated because it is modulated with a 120Hz signal. However, computer numerical integration and Fourier analysis approximate the RMS value reasonably close to the bench measurements. The RMS value is about 0.82A at a typical condition of 120VAC, 200W load. This ripple is line voltage dependent, and the worst case is at low line.

I_{2RMS} = 0.82A at 120VAC, 200W

The third component is the switching ripple from the load, if the load is a switching regulator.

$$I_{3RMS} \approx I_{LOAD}DC$$

For United Chemicon KMH 400V capacitor series, ripple current multiplier for currents at 100kHz is 1.43. The equivalent 120Hz ripple current can then be found:

$$I_{RMS} = \sqrt{(I_{1RMS})^2 + \left(\frac{I_{2RMS}}{1.43}\right)^2 + \left(\frac{I_{3RMS}}{1.43}\right)^2}$$

For a typical system that runs at an average load of 200W and 385V output:

$I_{LOAD}DC = 0.52A$

$I_{1RMS} \approx 0.71 \times 0.52A = 0.37A$

$I_{2RMS} \approx 0.82A$ at 120VAC

$I_{3RMS} \approx I_{LOAD}DC = 0.52A$

$$I_{RMS} = \sqrt{(0.37A)^2 + \left(\frac{0.82A}{1.43}\right)^2 + \left(\frac{0.52A}{1.43}\right)^2} = 0.77A$$

The 120Hz ripple current rating at 105°C ambient is 0.95A for the 180µF KMH 400V capacitor. The expected life of the output capacitor may be calculated from the thermal stress analysis:

$$L = L_0 \times 2^{\frac{(105°C+\Delta T_K)-(T_{AMB}+\Delta T_0)}{10}}$$

where

L = expected life time

L_0 = hours of load life at rated ripple current and rated ambient temperature

ΔT_K = capacitor internal temperature rise at rated condition. $\Delta T_K = (I^2R)/(KA)$, where I is the rated current, R is capacitor ESR, and KA is a volume constant.

T_{AMB} = operating ambient temperature

ΔT_0 = capacitor internal temperature rise at operating condition

In our example, L_0 = 2000 hours and ΔT_K = 10°C at rated 0.95A. ΔT_0 can then be calculated from:

$$\Delta T_0 = \left(\frac{I_{RMS}}{0.95A}\right)^2 \times \Delta T_K = \left(\frac{0.77A}{0.95A}\right)^2 \times 10°C = 6.6°C$$

Assuming the operating ambient temperature is 60°C, the approximate life time is:

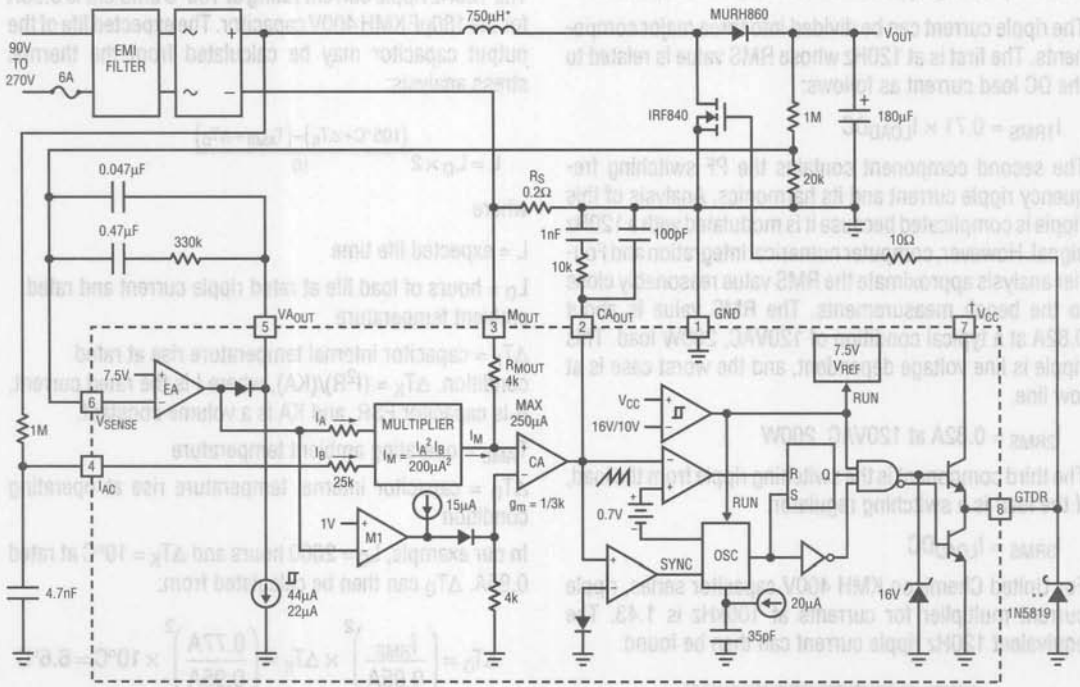
$$L_0 \approx 2000 \times 2^{\frac{(105°C+10°C)-(60°C+6.6°C)}{10}} \approx 57{,}000 \text{ Hrs.}$$

For longer life, capacitor with higher ripple current rating or parallel capacitors should be used.

4

TYPICAL APPLICATION

300W, 382V Preregulator



* 1. COILTRONICS CTX02-12236 (TYPE 52 CORE)
AIR MOVEMENT NEEDED AT POWER LEVEL GREATER THAN 250W.
2. COILTRONICS CTX02-12295 (MAGNETICS Kool Mµ® 77930 CORE)

** THIS SCHOTTKY DIODE IS TO CLAMP GTDR WHEN MOS SWITCH TURNS OFF. PARASITIC INDUCTANCE AND GATE CAPACITANCE MAY TURN ON CHIP SUBSTRATE DIODE AND CAUSE ERRATIC OPERATIONS IF GTDR IS NOT CLAMPED.

† SEE APPLICATIONS INFORMATION SECTION FOR CIRCUITRY TO SUPPLY POWER TO V_{CC}.

Kool Mµ is a registered trademark of Magnetics, Inc.

Dual 24V High-Side MOSFET Driver

FEATURES

- Fully Enhances N-Channel Power MOSFETs
- 12μA Standby Current
- Operates at Supply Voltages from 9V to 24V
- Short Circuit Protection
- Easily Protected Against Supply Transients
- Controlled Switching ON and OFF Times
- No External Charge Pump Components
- Compatible With Standard Logic Families
- Available in 8-Pin SOIC

APPLICATIONS

- Solenoid Drivers
- DC Motor Drivers
- Stepper Motor Drivers
- Lamp Drivers/Dimmers
- Relay Drivers
- Low Frequency H-Bridge
- P-Channel Switch Replacement

DESCRIPTION

The LTC1255 dual high-side driver allows using low cost N-channel FETs for high-side industrial and automotive switching applications. An internal charge pump boosts the gate drive voltage above the positive rail, fully enhancing an N-channel MOS switch with no external components. Low power operation, with 12μA standby current, allows use in virtually all systems with maximum efficiency.

Included on-chip is independent overcurrent sensing to provide automatic shutdown in case of short circuits. A time delay can be added to the current sense to prevent false triggering on high in-rush current loads.

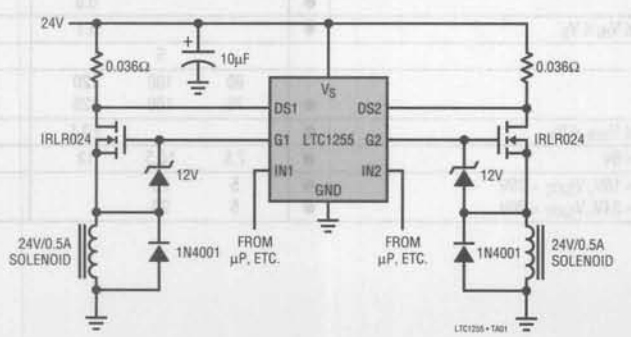
The LTC1255 operates from 9V to 24V supplies and is well suited for industrial and automotive applications.

The LTC1255 is available in both an 8-pin DIP and an 8-pin SOIC.

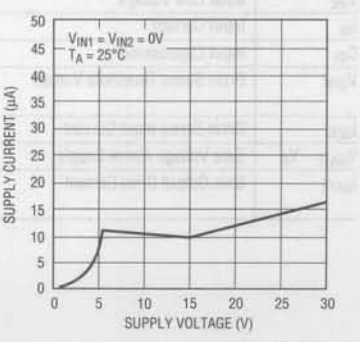
4

TYPICAL APPLICATION

Dual 24V High-Side Switch with Overcurrent Protection



Standby Supply Current

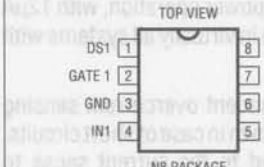


ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.3V to 30V
Transient Supply Voltage (<10ms) 40V
Input Voltage ..... (V_S + 0.3V) to (GND − 0.3V)
Gate Voltage ..... (V_S + 20V) to (GND − 0.3V)
Current (Any Pin) 50mA

Operating Temperature Range
LTC1255C ..... 0°C to 70°C
LTC1255I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

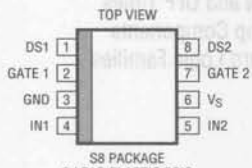


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1255CN8
LTC1255IN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1255CS8
LTC1255IS8

S8 PART MARKING

1255
1255I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 9V to 24V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current OFF	V_S = 10V, V_{IN} = 0V (Note 1)			12	40	µA
		V_S = 18V, V_{IN} = 0V (Note 1)			12	40	µA
		V_S = 24V, V_{IN} = 0V (Note 1)			12	40	µA
	Quiescent Current ON	V_S = 10V, V_{GATE} = 22V, V_{IN} = 5V (Note 2)			160	400	µA
		V_S = 18V, V_{GATE} = 30V, V_{IN} = 5V (Note 2)			350	800	µA
		V_S = 24V, V_{GATE} = 36V, V_{IN} = 5V (Note 2)			600	1200	µA
V_{INH}	Input High Voltage		●	2			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
V_{SEN}	Drain Sense Threshold Voltage			80	100	120	mV
			●	75	100	125	mV
I_{SEN}	Drain Sense Input Current	0V ≤ V_{SEN} ≤ V_S	●			±0.1	µA
$V_{GATE} - V_S$	Gate Voltage Above Supply	V_S = 9V	●	7.5	10.5	12	V
I_{GATE}	Gate Output Drive Current	V_S = 18V, V_{GATE} = 30V	●	5	20		µA
		V_S = 24V, V_{GATE} = 36V	●	5	23		µA

ELECTRICAL CHARACTERISTICS

V_S = 9V to 24V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	Turn-ON Time	V_S = 10V, C_{GATE} = 1000pF (Note 3)				
		Time for $V_{GATE} > V_S + 2V$	30	100	300	µs
		Time for $V_{GATE} > V_S + 5V$	75	250	750	µs
		V_S = 18V, C_{GATE} = 1000pF (Note 3)				
		Time for $V_{GATE} > V_S + 5V$	40	120	400	µs
		Time for $V_{GATE} > V_S + 10V$	75	250	750	µs
		V_S = 24V, C_{GATE} = 1000pF (Note 3)				
		Time for $V_{GATE} > V_S + 10V$	50	180	500	µs
t_{OFF}	Turn-OFF Time	V_S = 10V, C_{GATE} = 1000pF, (Note 3, 4)	10	24	60	µs
		V_S = 18V, C_{GATE} = 1000pF, (Note 3, 4)	10	21	60	µs
		V_S = 24V, C_{GATE} = 1000pF, (Note 3, 4)	10	19	60	µs
t_{SC}	Short-Circuit Turn-OFF Time	V_S = 10V, C_{GATE} = 1000pF, (Note 3, 4)	5	16	30	µs
		V_S = 18V, C_{GATE} = 1000pF, (Note 3, 4)	5	16	30	µs
		V_S = 24V, C_{GATE} = 1000pF, (Note 3, 4)	5	16	30	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Quiescent current OFF is for both channels in OFF condition.

Note 2: Quiescent current ON is per driver and is measured independently. The gate voltage is clamped to 12V above the rail to simulate the effects of protection clamps connected across the GATE-SOURCE of the power MOSFET.

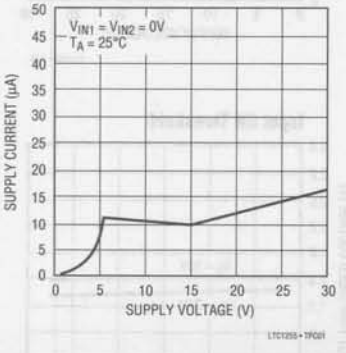
Note 3: Zener diode clamps must be connected across the GATE-SOURCE of the power MOSFET to limit V_{GS}. 1N5242A (through hole) or MMBZ5242A (surface mount) 12V Zener diodes are recommended. All Turn-ON and Turn-OFF tests are performed with a 12V Zener clamp in series with a small-signal diode connected between V_S and the GATE output to simulate the effects of a 12V protection Zener clamp connected across the GATE-SOURCE of the power MOSFET.

Note 4: Time for V_{GATE} to drop below 1V.

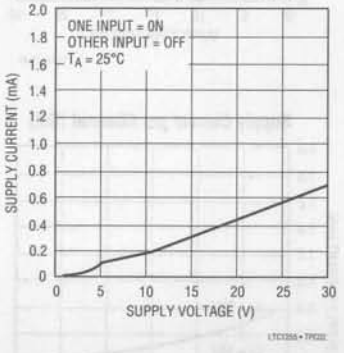
4

TYPICAL PERFORMANCE CHARACTERISTICS

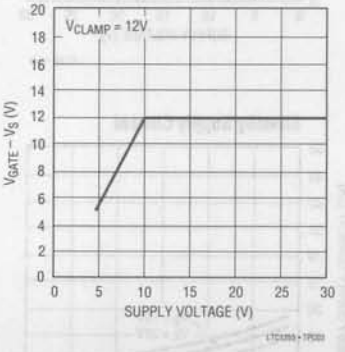
Standby Supply Current



Supply Current per Driver (ON)

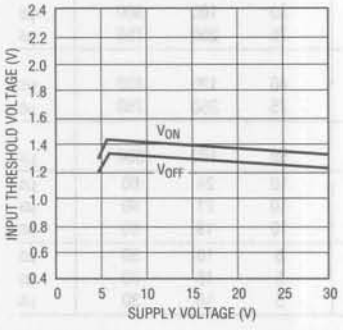


Gate Voltage Above Supply

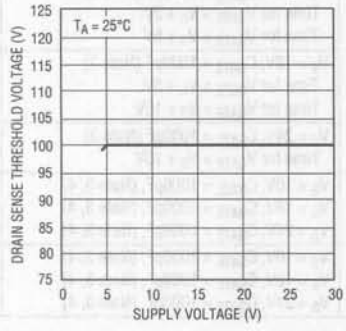


TYPICAL PERFORMANCE CHARACTERISTICS

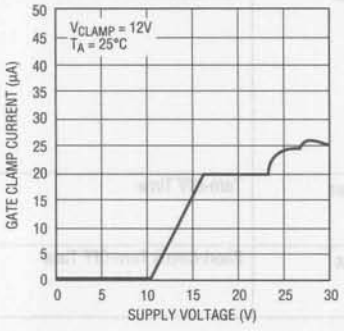
Input Threshold Voltage



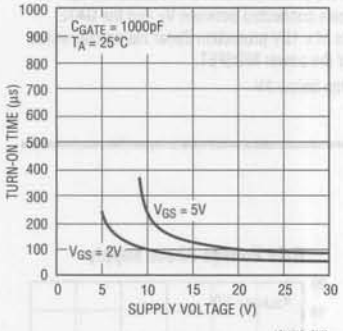
Drain Sense Threshold Voltage



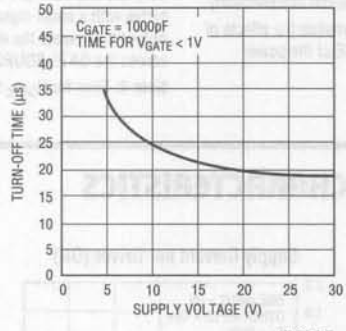
Gate Clamp Current



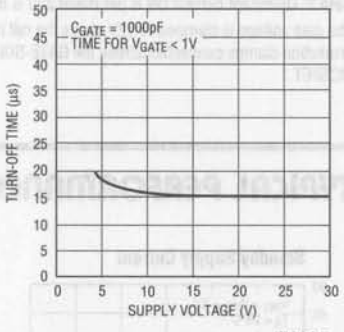
Turn-ON Time



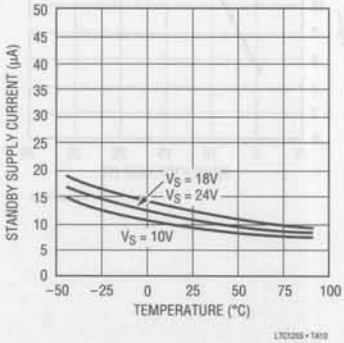
Turn-OFF Time



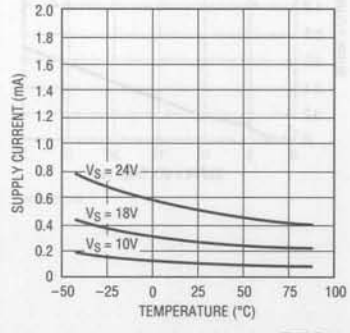
Short-Circuit Turn-OFF Delay Time



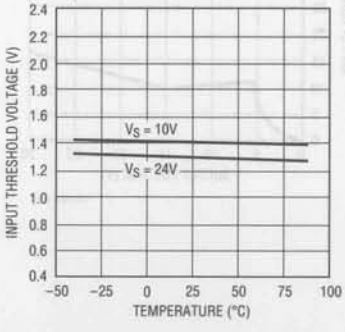
Standby Supply Current



Supply Current per Channel (ON)



Input ON Threshold



PIN FUNCTIONS

Input Pin

The LTC1255 input pin is active high and activates all of the protection and charge pump circuitry when switched ON. The LTC1255 logic and shutdown inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails. The input pin should be held low during the application of power to properly set the input latch.

Gate Drive Pin

The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is of relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1255 serves two vital purposes. The first is obvious; it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious; it provides a Kelvin connection to the top of the drain sense resistor for the internal 100mV reference.

The supply pin of the LTC1255 should never be forced below ground as this may result in permanent damage to the device. A 100Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

The LTC1255 is designed to be continuously powered so that the gate of the MOSFET is actively driven at all times. If it is necessary to remove power from the supply pin and then reapply it, the input pin should be cycled (low to high) a few milliseconds *after* the power is reapplied to reset the input latch and protection circuitry. Also, the input pin should be isolated from the controlling logic by a 10k resistor if there is a possibility that the input pin will be held high after the supply has been removed.

Drain Sense Pin

The drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input to reset the short-circuit latch and turn the MOSFET back on.

This pin is also a high impedance CMOS gate with ESD protection and therefore should not be forced outside of the power supply rails. To defeat the overcurrent protection, short the drain sense pin to the supply pin.

Some loads, such as large supply capacitors, lamps or motors require high in-rush currents. An RC time delay can be added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false trigger during startup. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET at risk of being destroyed by a short-circuit condition (see Applications Information section).

4

OPERATION

The LTC1255 is a dual 24V MOSFET driver with built-in protection and gate charge pump. The LTC1255 consists of the following functional blocks:

TTL and CMOS Compatible Inputs and Latches

The LTC1255 inputs have been designed to accommodate a wide range of logic families. Both input thresholds are set at about 1.3V with approximately 100mV of hysteresis. A low standby current regulator provides continuous bias for the TTL-to-CMOS converter.

The input/protection latch should be set after initial power-up, or after reapplication of power, by cycling the input low to high.

OPERATION

Internal Voltage Regulation

The output of the TTL-to-CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the power MOSFET is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and therefore no external components are required to generate the gate drive. The charge pump is designed to drive a 12V Zener diode clamp connected across the gate and source of the MOSFET switch.

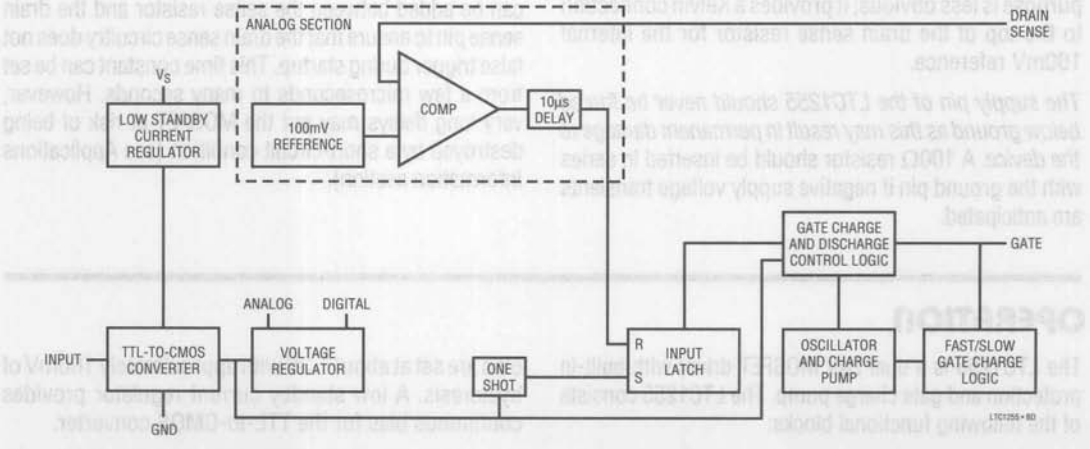
Drain Current Sense

The LTC1255 is configured to sense the current flowing into the drain of the power MOSFET in a high-side application. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.10Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged via a relatively large N-channel transistor.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions in normal operation. If a short circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

MOSFET AND LOAD PROTECTION

The LTC1255 protects the power MOSFET switch by removing drive from the gate as soon as an overcurrent condition is detected. Resistive and inductive loads can be protected with no external time delay in series with the drain sense pin. Lamp loads, however, require that the overcurrent protection be delayed long enough to start the lamp but short enough to ensure the safety of the MOSFET.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10µs to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to "mask" short load current transients and the starting of a small capacitor (<1µF) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 1.

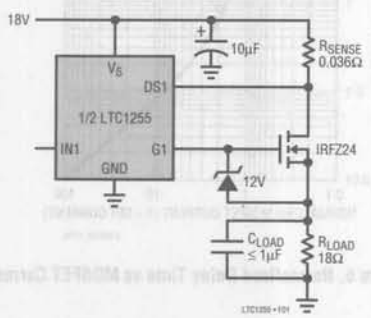


Figure 1. Protecting Resistive Loads

Inductive Loads

Loads that are primarily inductive, such as relays, solenoids and stepper motor windings, should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The built-in 10µs delay will ensure that the overcurrent protection is not false triggered by a supply or load transient. No external delay components are required as shown in Figure 2.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 2, to safely divert the stored energy.

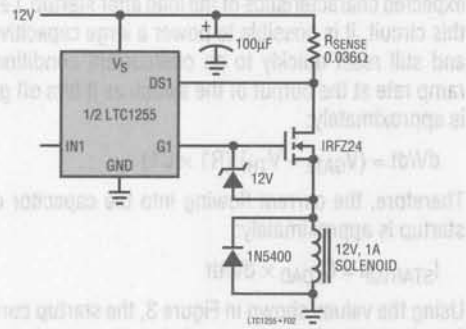


Figure 2. Protecting Inductive Loads

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 3. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn-on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the startup current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation

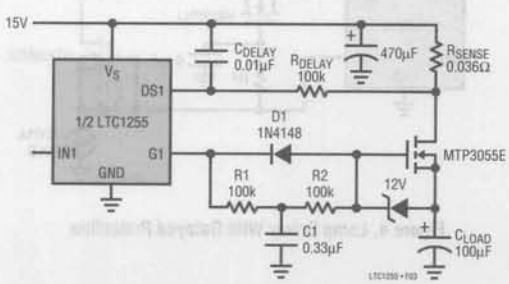


Figure 3. Powering Large Capacitive Loads

of sensitive electrical loads. (Resistor R2, and the diode D1, provide a direct path for the LTC1255 protection circuitry to quickly discharge the gate in the event of an overcurrent condition.)

The RC network, R_{DELAY} and C_{DELAY}, in series with the drain sense input should be set to trip based on the expected characteristics of the load after startup, i.e., with this circuit, it is possible to power a large capacitive load and still react quickly to an overcurrent condition. The ramp rate at the output of the switch as it lifts off ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH})/(R1 \times C1)$$

Therefore, the current flowing into the capacitor during startup is approximately:

$$I_{STARTUP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 3, the startup current is less than 100mA and does not false trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

Lamp Loads

The in-rush current created by a lamp during turn-on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 4 shifts the current limit threshold up by a factor of 11:1 (to 30A) for a short period of time while the bulb is turned on. The current limit then drops down to 2.7A after the in-rush current has subsided.

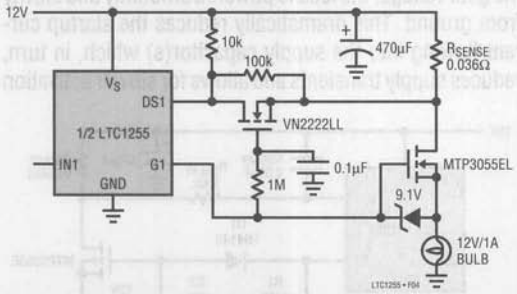


Figure 4. Lamp Driver With Delayed Protection

Selecting R_{DELAY} and C_{DELAY}

Figure 5 is a graph of normalized overcurrent shutdown time versus normalized MOSFET current. This graph is used to select the two delay components, R_{DELAY} and C_{DELAY}, which make up a simple RC delay between the drain sense input and the drain sense resistor.

The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the set current. (The set current is defined as the current required to develop 100mV across the drain sense resistor.)

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the manufacturer for safe operation. (See MOSFET data sheet for further S.O.A. information.)

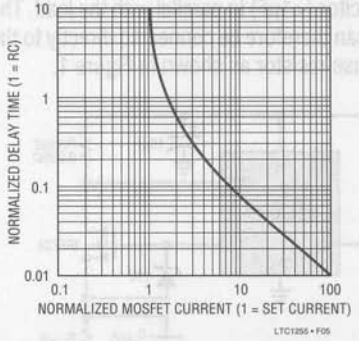


Figure 5. Normalized Delay Time vs MOSFET Current

Using a Speed-Up Diode

Another way to reduce the amount of time that the power MOSFET is in a short-circuit condition is to "bypass" the delay resistor with a small signal diode as shown in Figure 6. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 4A.

APPLICATIONS INFORMATION

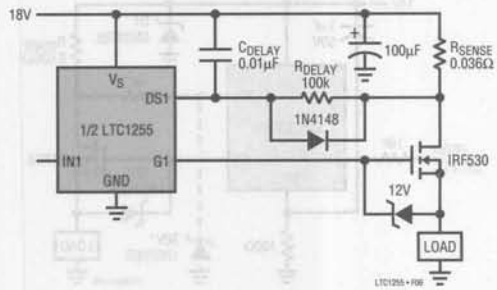


Figure 6. Using a Speed-Up Diode

Current Limited Power Supplies

The LTC1255 requires at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply to the LTC1255 be held higher than 3.5V at all times, even when the output of the switch is short circuited to ground. The output voltage of a current limited regulator may drop very quickly during short circuit and pull the supply pin of the LTC1255 below 3.5V before the shutdown circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should be added as shown in Figure 7 which holds the supply pin of the LTC1255 high long enough for the overcurrent shutdown circuitry to respond and fully discharge the gate.

Linear regulators with small output capacitors are the most difficult to protect as they can "switch" from a voltage mode to a current limited mode very quickly.

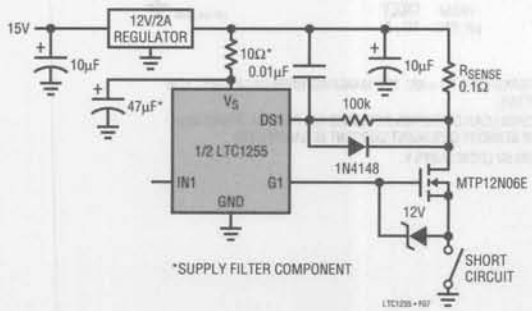


Figure 7. Supply Filter for Current Limited Supplies

The large output capacitors on many switching regulators, on the other hand, may be able to hold the supply pin of the LTC1255 above 3.5V sufficiently long that this extra filtering is not required.

Because the LTC1255 is micropower in both the standby and ON state, the voltage drop across the supply filter is very small (typically <6mV) and does not significantly alter the accuracy of the drain sense threshold voltage which is typically 100mV.

AUTOMOTIVE APPLICATIONS

Reverse Battery Protection

The LTC1255 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 8. The resistor limits the supply current to less than 120mA with –12V applied. Since the LTC1255 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V µP (or controlling logic) is protected by the 10k resistors in series with the input.

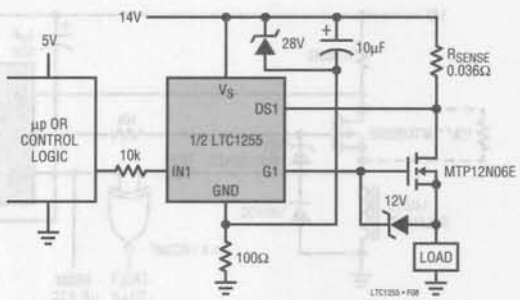


Figure 8. Reverse Battery Protection

Transient Overvoltage Protection

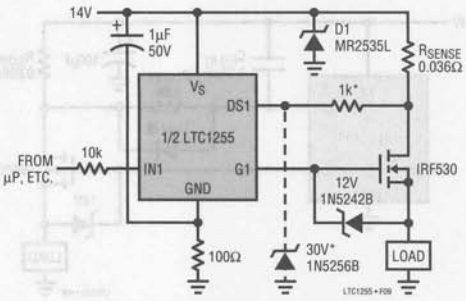
A common scheme used to limit overvoltage transients on a 14V nominal automotive power bus is to clamp the supply to the module containing the high-side MOSFET switches with a large transient suppressor diode, D1 in Figure 9. This diode limits the supply voltage to 40V under worse case conditions. The LTC1255 is designed to survive short (10ms) 40V transients and return to normal operation after the transient has passed.

APPLICATIONS INFORMATION

The switches can either be turned OFF by the controlling logic during these transients or latched OFF above 30V by holding the drain sense pin low as shown in Figure 9.

Switch status can be ascertained by means of an XNOR gate connected to the input and switch output through 100k current limiting resistors (see Typical Applications section for more detail on this scheme). The switch is reset after the overvoltage event by cycling the input low and then high again.

The power MOSFET switch should be selected to have a breakdown voltage sufficiently higher than the 40V supply clamp voltage to ensure that no current is conducted to the load during the transient.

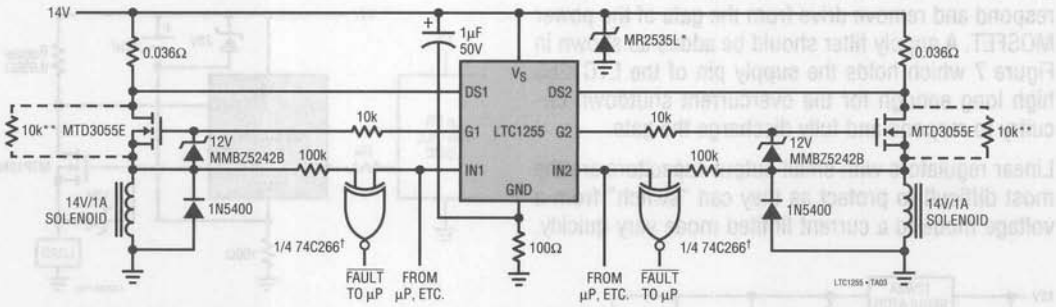


*OPTIONAL OVERVOLTAGE (30V) LATCH-OFF COMPONENTS

Figure 9. Overvoltage Transient Protection

TYPICAL APPLICATIONS

Dual Automotive High-Side Switch with Overvoltage Protection, XNOR Status and 12µA Standby Current



TRUTH TABLE

IN	OUT	CONDITION	FAULT
0	0	SWITCH OFF	1
1	0	OVERCURRENT	0
0	1	OPEN LOAD**	0
1	1	SWITCH ON	1

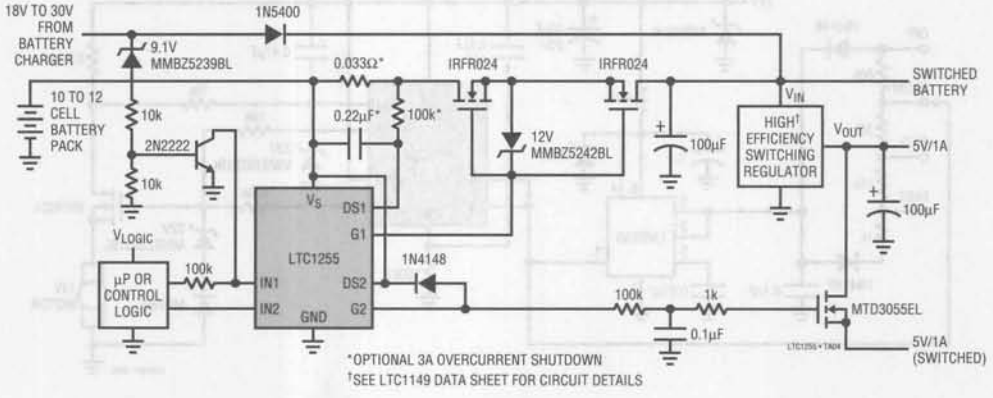
*LIMITS V_S TRANSIENTS TO <40V. SEE MANUFACTURER DATA SHEET FOR FURTHER DETAIL.

**OPTIONAL OPEN LOAD DETECTION REQUIRES 10k PULL-UP RESISTORS. (ULTRA LOW STANDBY QUIESCENT CURRENT IS SACRIFICED)

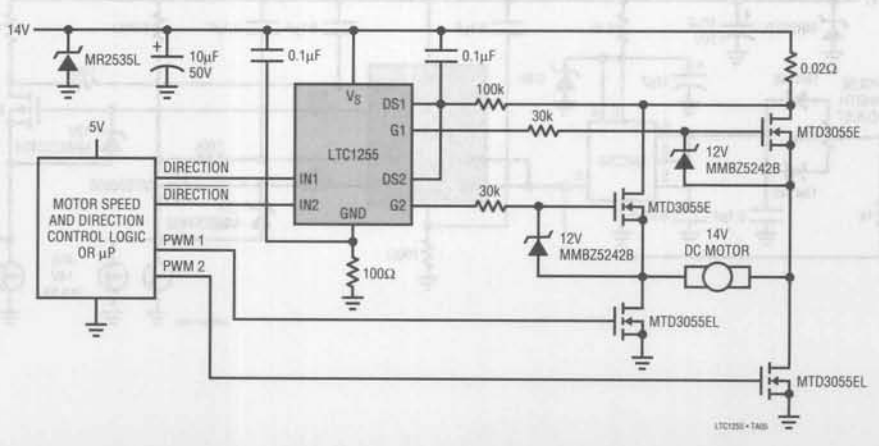
†POWER FROM 5V LOGIC SUPPLY.

TYPICAL APPLICATIONS

10 to 12 Cell Battery Switch and 5V Ramped Load Switch with 12μA Standby Current and Optional 3A Overcurrent Shutdown

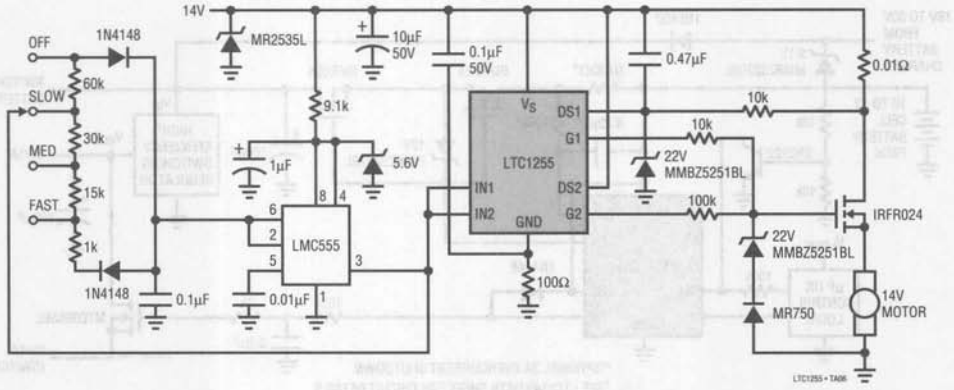


Automotive Motor Direction and Speed Control with Stall-Current Shutdown

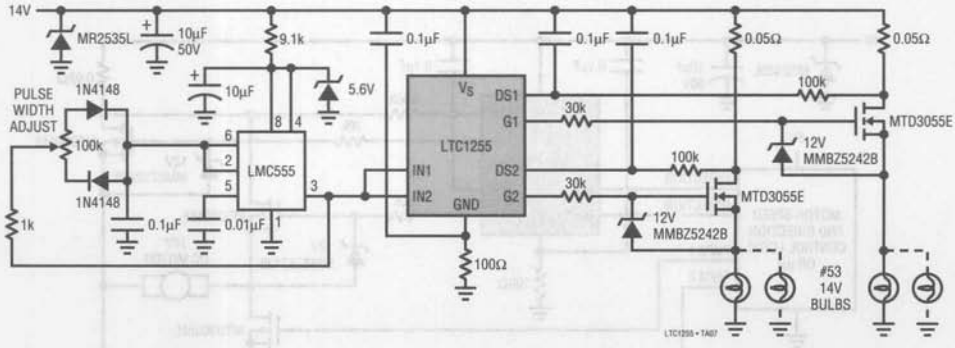


TYPICAL APPLICATIONS

Low Frequency (f_O = 100Hz) PWM Motor Speed Control with Current Limit and 22V Overvoltage Shutdown

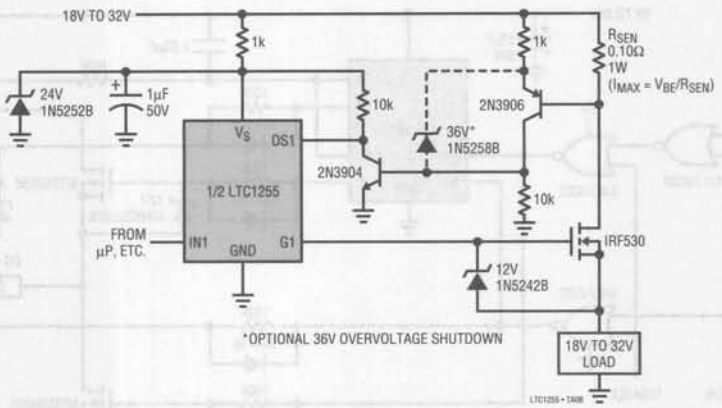


Dual Automotive Lamp Dimmer with Controlled Rise and Fall Times and Short-Circuit Protection



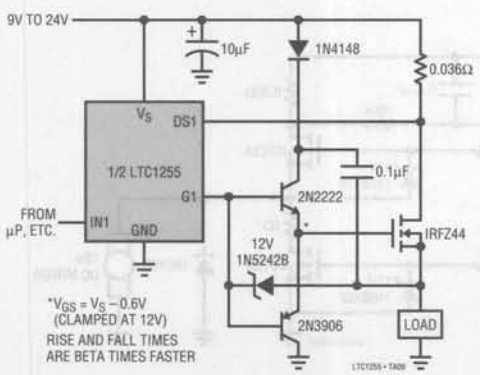
TYPICAL APPLICATIONS

18V to 32V Operation with Overcurrent Shutdown and Optional Overvoltage Shutdown

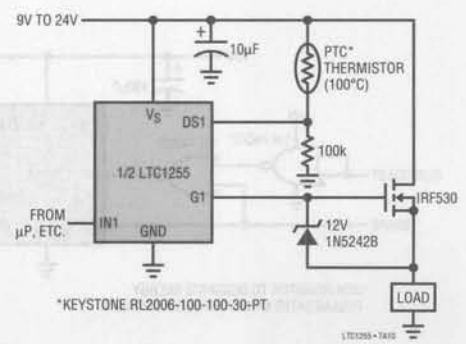


4

Bootstrapped Gate Driver (100Hz < f_O < 10kHz)

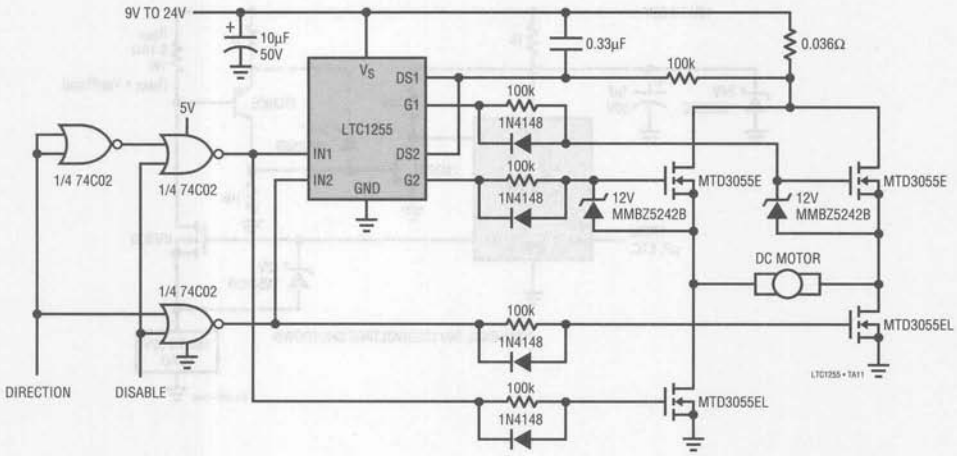


High-Side Switch with Thermal Shutdown (PTC Thermistor)

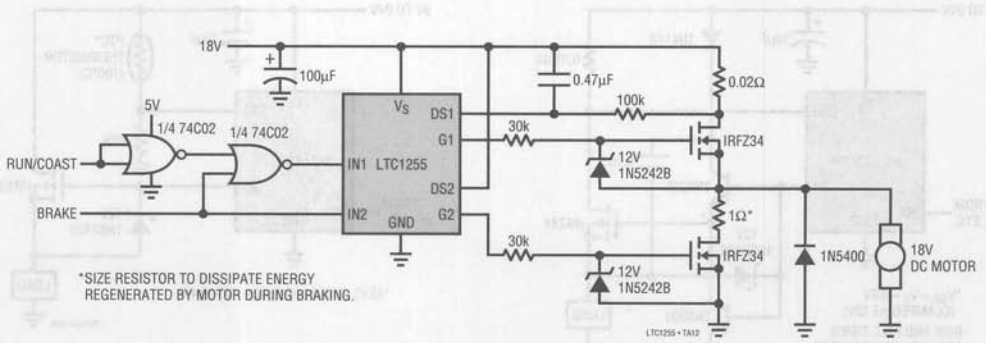


TYPICAL APPLICATIONS

H-Bridge DC Motor Driver
(Direction and ON/OFF Control)

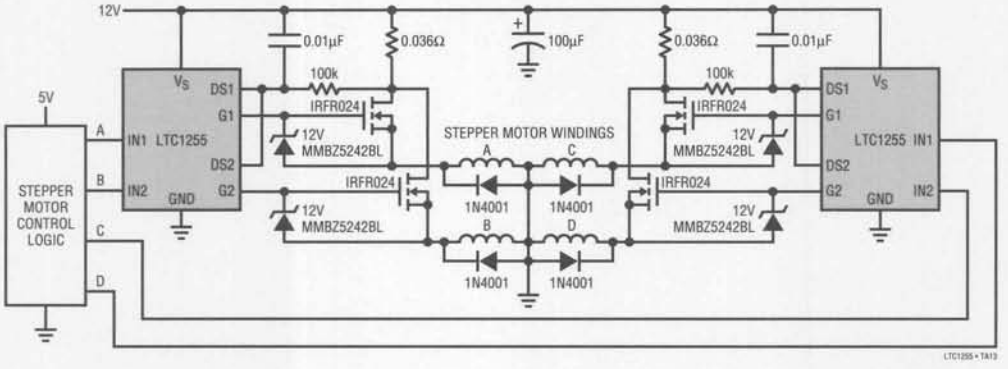


High-Side DC Motor Driver With Electronic Braking and Stalled Motor Shutdown



TYPICAL APPLICATIONS

Stepper Motor Driver with Overcurrent Protection



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SECTION 4—POWER PRODUCTS

SWITCHING REGULATORS

LT1072, 1.25A High Efficiency Switching Regulator 4-232
LT1074/LT1076, Step-Down Switching Regulator 4-243
LT1082, 1A High Voltage, Efficiency Switching Voltage Regulator 4-257
LT1103/LT1105, Offline Switching Regulator 4-267
LT1107, Micropower DC/DC Converter Adjustable and Fixed 5V, 12V 4-294
LT1108, Micropower DC/DC Converter Adjustable and Fixed 5V, 12V 4-306
LT1109, Micropower Low Cost DC/DC Converter Adjustable and Fixed 5V, 12V 4-318
LT1109A, Micropower DC/DC Converter Flash Memory VPP Generator Adjustable and Fixed 5V, 12V 4-325
LT1111, Micropower DC/DC Converter Adjustable and Fixed 5V, 12V 4-331
LTC1142/LTC1142-ADJ, Dual High Efficiency Synchronous Step-Down Switching Regulators 4-346
LTC1143, Dual High Efficiency Step-Down Switching Regulator Controller 4-365
LTC1147-3.3/LTC1147-5, High Efficiency Step-Down Switching Regulator Controllers 4-380
LTC1148/LTC1148-3.3/LTC1148-5, High Efficiency Synchronous Step-Down Switching Regulators 4-395
LTC1149/LTC1149-3.3/LTC1149-5, High Efficiency Synchronous Step-Down Switching Regulators 4-414
LTC1159/LTC1159-3.3/LTC1159-5, High Efficiency Synchronous Step-Down Switching Regulators 13-11
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LT1176/LT1176-5, Step-Down Switching Regulator 4-462
LT1182/LT1183, CCFL/LCD Contrast Dual Switching Regulator 13-27
LT1268B/LT1268, 7.5A, 150kHz Switching Regulators 4-466
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LT1300, Micropower High Efficiency 3.3/5V Step-Up DC/DC Converter 4-478
LT1301, Micropower High Efficiency 5V12V Step-Up DC/DC Converter with Flash Memory 4-486
LT1302/LT1302-5, Micropower High Output Current Step-Up Adjustable and Fixed 5V DC/DC Converter 13-47
LT1303/LT1303-5, Micropower High Efficiency DC/DC Converter with Low-Battery Detector Adjustable and Fixed 5V 13-51
LT1309, 500kHz Micropower DC/DC Converter for Flash Memory 13-55
LT1372, 500kHz High Efficiency 1.5A Switching Regulator 13-120
LT1376, 1.5A, 500kHz Step-Down Switching Regulator 13-121

1.25A High Efficiency Switching Regulator

FEATURES

- Available in MiniDIP, TO-220, and TO-3 Packages
- Wide Input Voltage Range 3V–60V
- Low Quiescent Current—6mA
- Internal 1.25A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Can be Externally Synchronized

APPLICATIONS

- Logic Supply 5V @ 2.5A
- 5V Logic to ±15V Op Amp Supply
- Offline Converter up to 50W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs
- Driver for High Current Supplies

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1072. Application circuits are included to show the capability of the LT1072. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1072 by factoring in the lower switch current rating.

DESCRIPTION

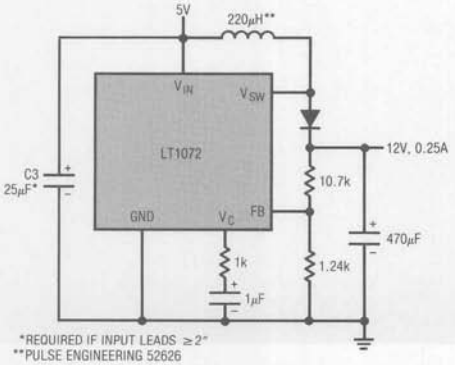
The LT1072 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1072 to be built in a standard 5-pin TO-3 or TO-220 power package as well as the 8-pin miniDIP. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1072 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 20 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1072 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1072, without the need for optocouplers or extra transformer windings.

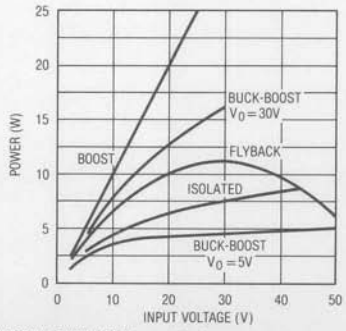
TYPICAL APPLICATION

Boost Converter (5V to 12V)



*REQUIRED IF INPUT LEADS ≥2"
**PULSE ENGINEERING 52626

Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 1A \times V_{OUT}$.
MINIDIP OUTPUT POWER MAY BE LIMITED BY PACKAGE TEMPERATURE RISE AT HIGH INPUT VOLTAGES OR HIGH DUTY CYCLES.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1072HV (See Note 1) 60V
- LT1072 (See Note 1) 40V

Switch Output Voltage
- LT1072HV 75V
- LT1072 ..... 65V
- LT1072S8 ..... 60V

Feedback Pin Voltage (Transient, 1ms) ..... ±15V

Operating Junction Temperature Range
- LT1072HVM, LT1072M ..... −55°C to +150°C
- LT1072HVC, LT1072C (Oper.)* ..... 0°C to +100°C
- LT1072HVC, LT1072C (Sh. Ckt.)* ..... 0°C to +125°C

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

*Includes LT1072S8

Note 1: Minimum switch "on" time for the LT1072 in current limit is ≈0.7μsec. This limits the maximum input voltage during short circuit conditions, *in the buck and inverting modes only*, to ≈40V. Normal (unshorted) conditions are not affected. If the LT1072 is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

The value of the resistor is given by: $R = \frac{(t)(f)(V_{IN}) - V_f}{I_{(LIMIT)}} - R_L$

t = Minimum "on" time of LT1072 in current limit, ≈0.7μs

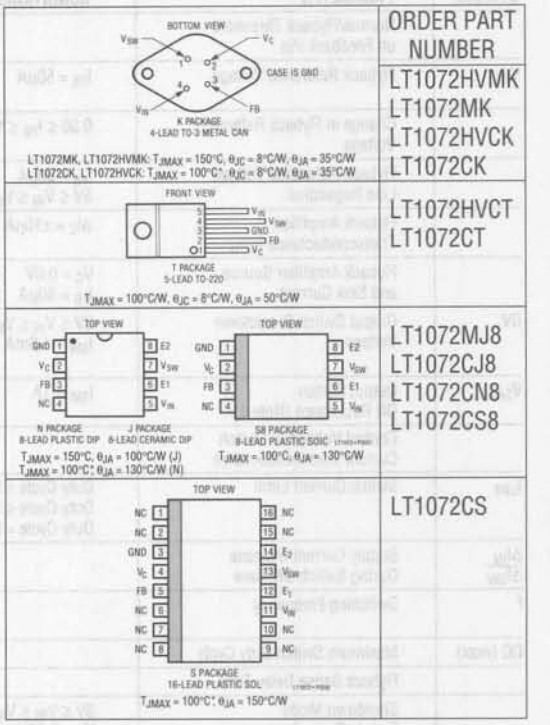
f = Operating frequency (40kHz)

V_f = Forward voltage of external catch diode at $I_{(LIMIT)}$

$I_{(LIMIT)}$ = Current limit of LT1072 (2A)

R_L = Internal series resistance of inductor

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1072HVMK LT1072MK LT1072HVCK LT1072CK
LT1072HVCT LT1072CT
LT1072MJ8 LT1072CJ8 LT1072CN8 LT1072CS8
LT1072CS

All Thermal Information is based on continuous operation.
*T_{JMAX} = 125°C for intermittent fault conditions.
Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin V_C = 0.8V	 ●	1.224 1.214	1.244 1.244	1.264 1.274	V V
I_B	Feedback Input Current	V_{FB} = V_{REF}	 ●		350	750 1100	nA nA
gm	Error Amplifier Transconductance	ΔI_C = ±25μA	 ●	3000 2400	4400	6000 7000	μmho μmho
	Error Amplifier Source or Sink Current	V_C = 1.5V	 ●	150 120	200	350 400	μA μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V Lo Clamp, V_{FB} = 1.5V		1.8 0.25	 0.38	2.3 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX} V_C = 0.8V	●			0.03	%/V %/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0	 ●	0.8 0.6	0.9	1.08 1.25	V V

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	I_{FB} = 50µA	 ●	15 14	16.3	17.6 18	V V
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50µA 3V ≤ V_{IN} ≤ V_{MAX} (Note 3)			0.01	0.03	%/V %/V
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10µA		150	300	500	µmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V Source I_{FB} = 50µA Sink	● ●	15 25	32 40	70 70	µA µA
BV	Output Switch Breakdown Voltage	3V ≤ V_{IN} ≤ V_{MAX} LT1072 I_{SW} = 1.5mA LT1072HV LT1072S8	● ● ●	65 75 60	90 90 80		V V V
V_{SAT}	Output Switch ON Resistance (Note 1)	I_{SW} = 1A	●		0.6	1	Ω
	Control Voltage to Switch Current Transconductance				2		A/V
I_{LIM}	Switch Current Limit	Duty Cycle ≤ 50% $T_J \geq 25°C$ Duty Cycle ≤ 50% $T_J < 25°C$ Duty Cycle = 80% (Note 2)	● ● ●	1.25 1.25 1		3 3.5 2.5	A A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch ON Time				25	35	mA/A
f	Switching Frequency		 ●	35 33	40	45 47	kHz kHz
DC (max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX} V_C = 0.05V			100	250	µA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}	 ●	100 50	150	250 300	mV mV

The ● denotes the specifications which apply over the full operating temperature range.

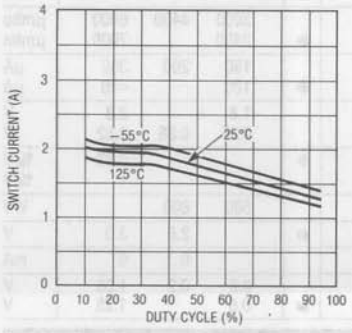
Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 0.833 (2 – DC).

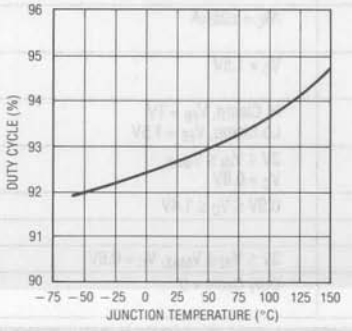
Note 3: V_{MAX} = 55V for HV grade to avoid switch breakdown.

TYPICAL PERFORMANCE CHARACTERISTICS

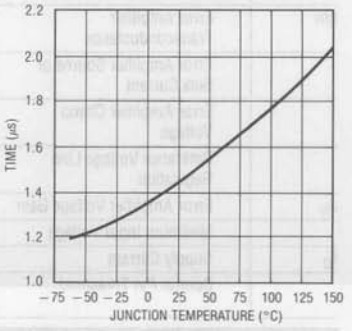
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

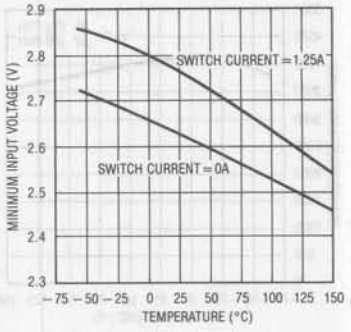


Flyback Blanking Time

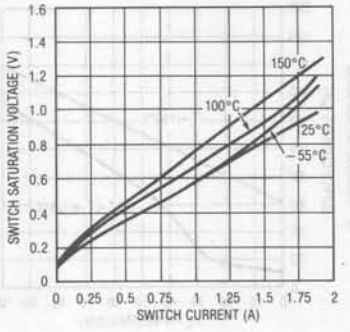


TYPICAL PERFORMANCE CHARACTERISTICS

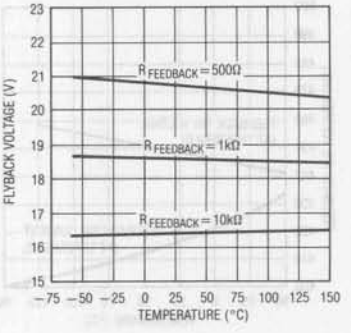
Minimum Input Voltage



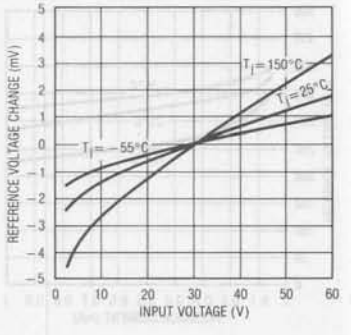
Switch Saturation Voltage



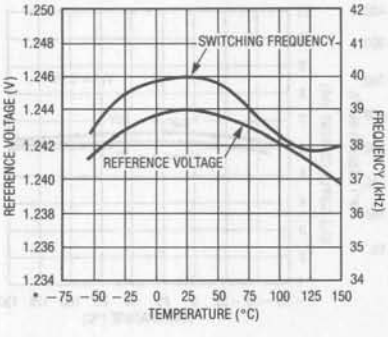
Isolated Mode Flyback Reference Voltage



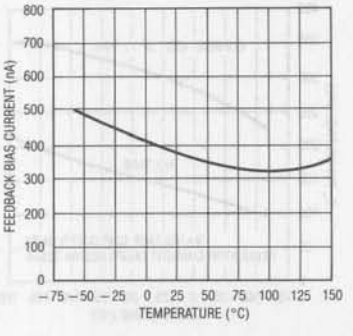
Line Regulation



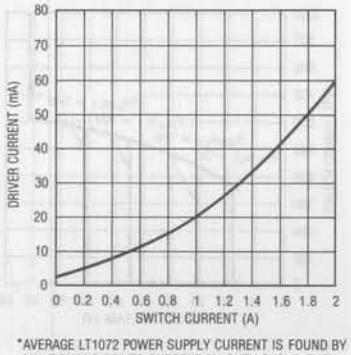
Reference Voltage and Switching Frequency vs Temperature



Feedback Bias Current vs Temperature

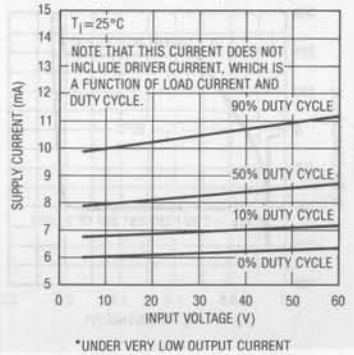


Driver Current* vs Switch Current



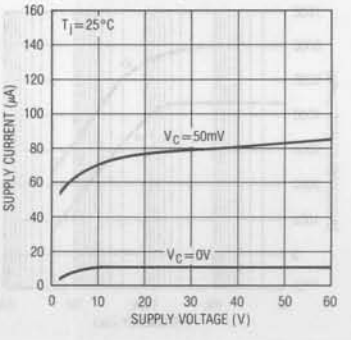
*AVERAGE LT1072 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Supply Current vs Supply Voltage (Shutdown Mode)



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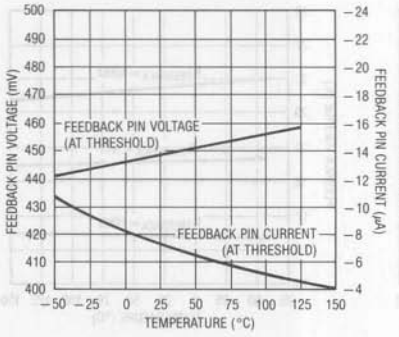
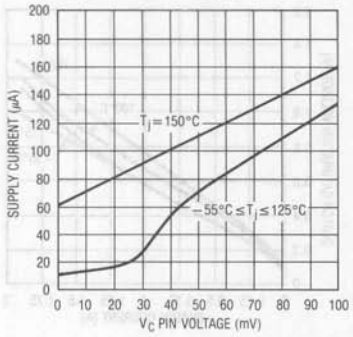
TYPICAL PERFORMANCE CHARACTERISTICS

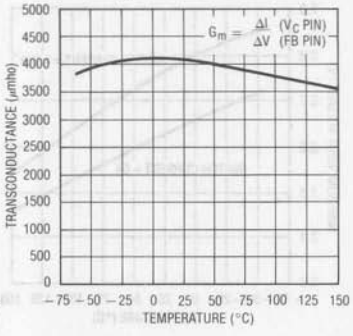
Normal/Flyback Mode Threshold on Feedback Pin



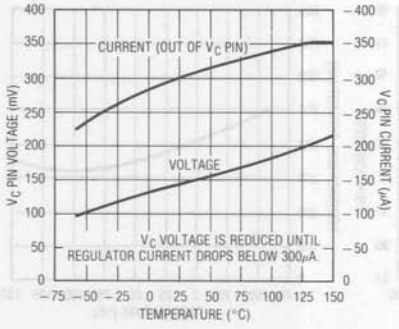
Shutdown Mode Supply Current



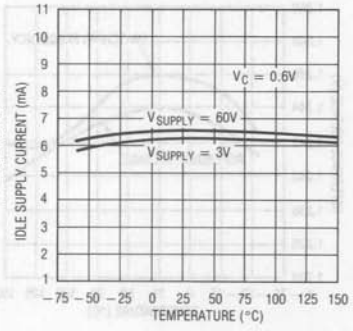
Error Amplifier Transconductance



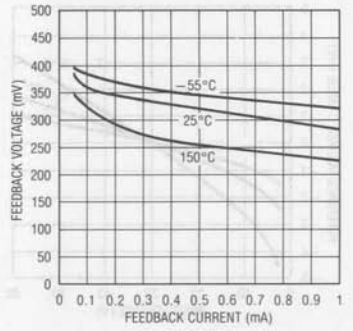
Shutdown Thresholds



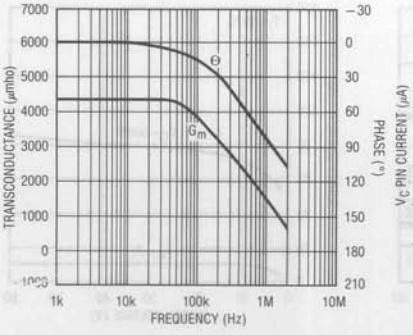
Idle Supply Current vs Temperature



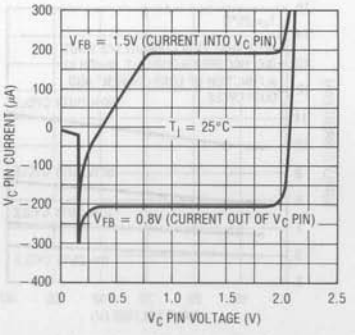
Feedback Pin Clamp Voltage



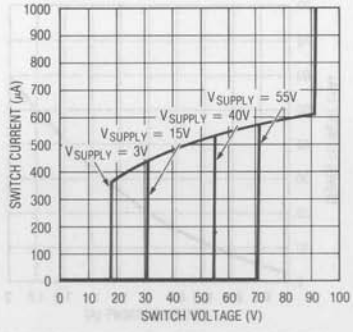
Transconductance of Error Amplifier



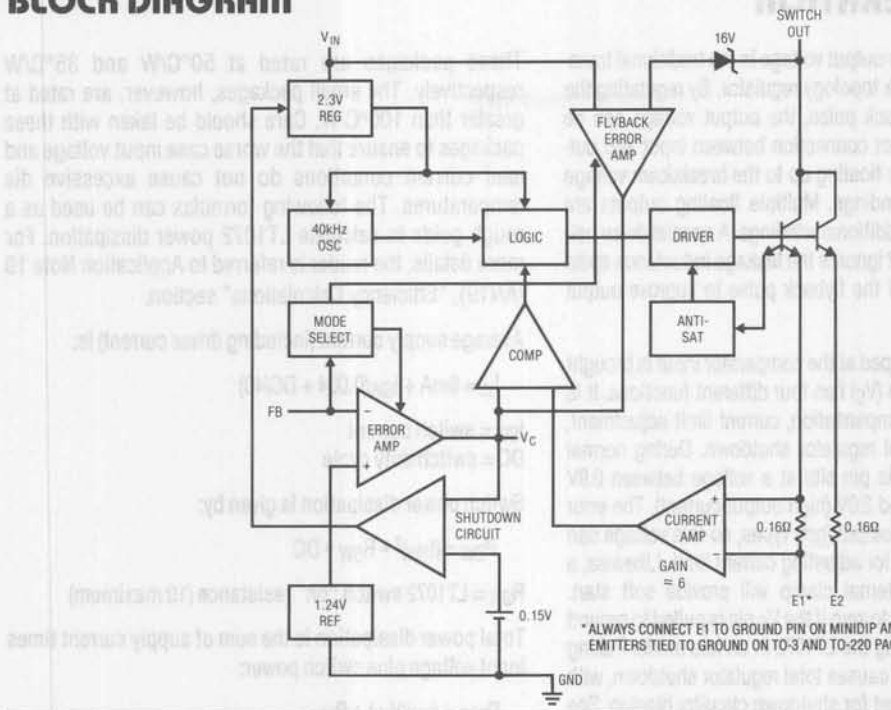
V_C Pin Characteristics



Switch "Off" Characteristics



BLOCK DIAGRAM



LT1072 OPERATION

The LT1072 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1072. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1072 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1072 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is

LT1072 OPERATION

directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1072 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1072 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing. See AN-19 for full application details.

Extra Pins on the MiniDIP and Surface Mount Packages

The 8 and 16-pin versions of the LT1072 have the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 100mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*. See "Thermal Considerations."

Thermal Considerations When Using Small Packages

The low supply current and high switch efficiency of the LT1072 allow it to be used without a heat sink in most applications when the TO-220 or TO-3 package is selected. These packages are rated at 50°C/W and 35°C/W respectively. The small packages, however, are rated at greater than 100°C/W. Care should be taken with these packages to ensure that the worse case input voltage and load current conditions do not cause excessive die temperatures. The following formulas can be used as a rough guide to calculate LT1072 power dissipation. For more details, the reader is referred to Application Note 19 (AN19), "Efficiency Calculations" section.

Average supply current (including driver current) is:

$$I_{IN} \approx 6mA + I_{SW}(0.004 + DC/40)$$

I_{SW} = switch current
DC = switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2 \bullet R_{SW} \bullet DC$$

R_{SW} = LT1072 switch "on" resistance (1Ω maximum)

Total power dissipation is the sum of supply current times input voltage plus switch power:

$$P_{TOT} = (I_{IN})(V_{IN}) + P_{SW}$$

In a typical example, using a boost convertor to generate +12V@0.12A from a +5V input, duty cycle is approximately 60%, and switch current is about 0.65A, yielding:

$$I_{IN} = 6mA + 0.65(0.004 + DC/40) = 18mA$$

$$P_{SW} = (0.65)^2 \bullet 1\Omega \bullet (0.6) = 0.25W$$

$$P_{TOT} = (5V)(0.018A) + 0.25 = 0.34W$$

Temperature rise in a plastic miniDIP would be 130°C/W times 0.34W, or approximately 44°C. The maximum ambient temperature would be limited to 100°C (commercial temperature limit) minus 44°C, or 56°C.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, four approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1072 will protect the die in most applications by shutting off switch

LT1072 OPERATION

current. *Thermal limit is not a tested parameter*, however, and should be considered only for non-critical applications with temporary overloads. A second approach is to use the larger TO-220 (T) or TO-3 (K) package which, even without a heat sink, may limit die temperatures to safe levels under overload conditions. In critical situations, heat sinking of these packages is required; especially if overload conditions must be tolerated for extended periods of time.

The third approach for lower current applications is to leave the second switch emitter open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The fourth approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1072 switch current limit is zero at approximately 1V on the V_C pin and 2A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN-19 for details.

LT1072 Synchronizing

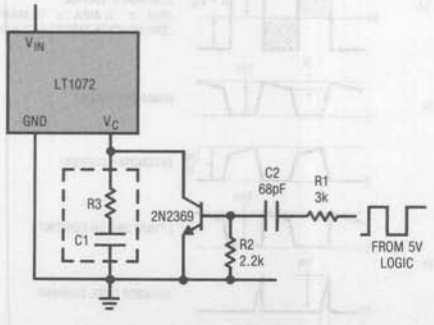
The LT1072 can be externally synchronized in the frequency range of 48kHz to 70kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under 1μs. C2 sets the pulse width at ≈0.35μs. The effect of a synchronizing pulse on the LT1072 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right)(t_S)(f_S)\left(I_C + \frac{V_C}{R3}\right)}{I_C}$$

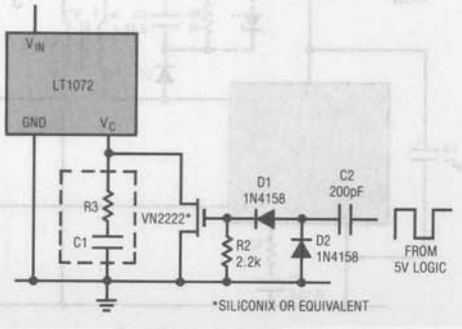
$\frac{KT}{q}$ = 26mV@25°C
t_S = pulse width
f_S = pulse frequency
I_C = LT1072 V_C source current (≈200μA)
V_C = LT1072 operating V_C voltage (1V–2V)
R3 = resistor used to set mid-frequency "zero" in LT1072 frequency compensation network.

With t_S = 0.35μs, f_S = 50kHz, V_C = 1.5V, and R3 = 2KΩ, offset voltage shift is ≈2.2mV. This is not particularly bothersome, but note that high offsets could result if R3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R3, so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor

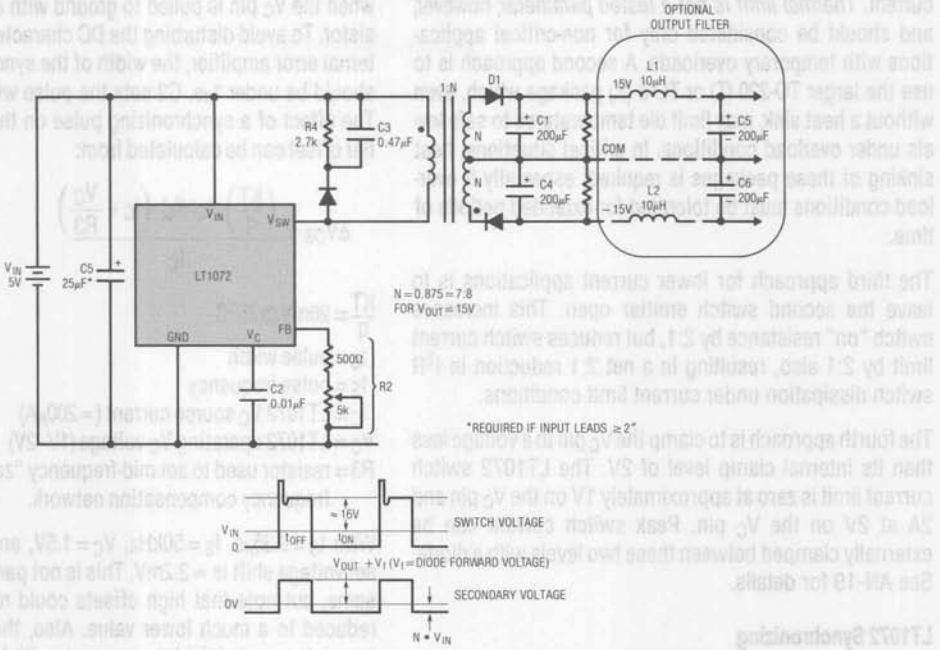


Synchronizing with MOS Transistor

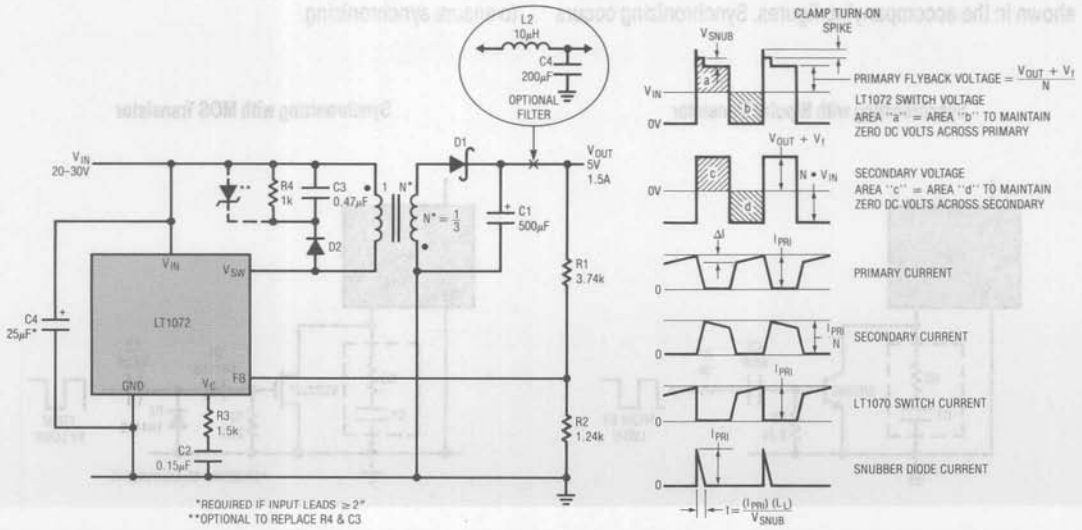


TYPICAL APPLICATIONS

Totally Isolated Converter

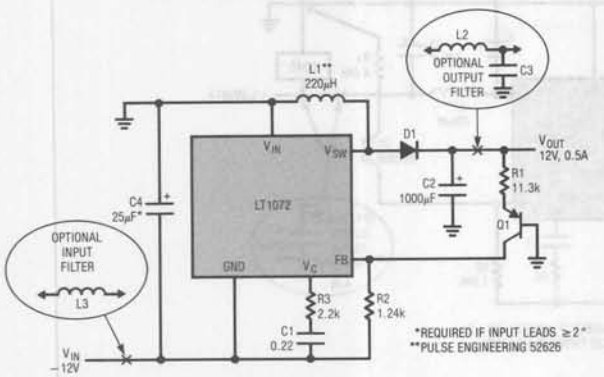


Flyback Converter

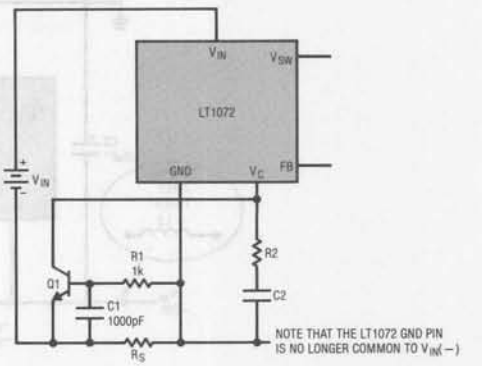


TYPICAL APPLICATIONS

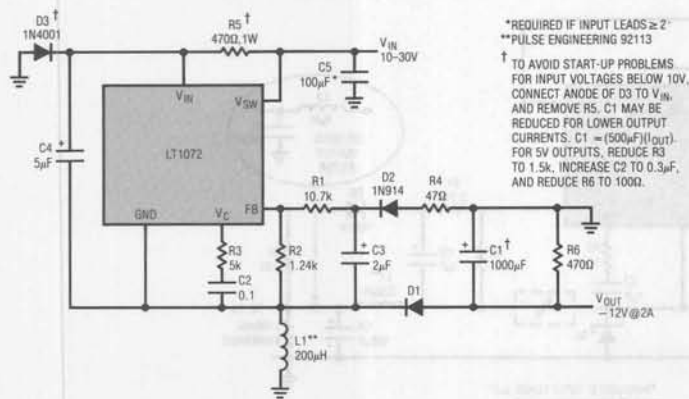
Negative to Positive Buck-Boost Converter



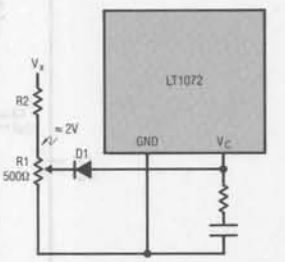
External Current Limit



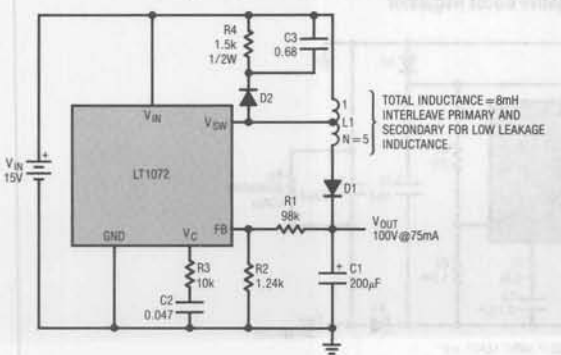
Positive to Negative Buck-Boost Converter



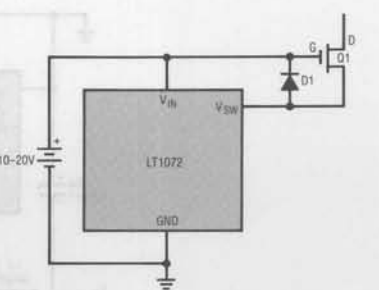
External Current Limit



Voltage Boosted Boost Converter

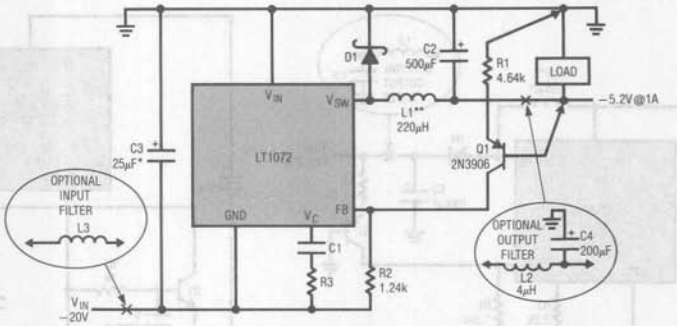


Driving High Voltage FET (for Offline Applications, See AN-25)



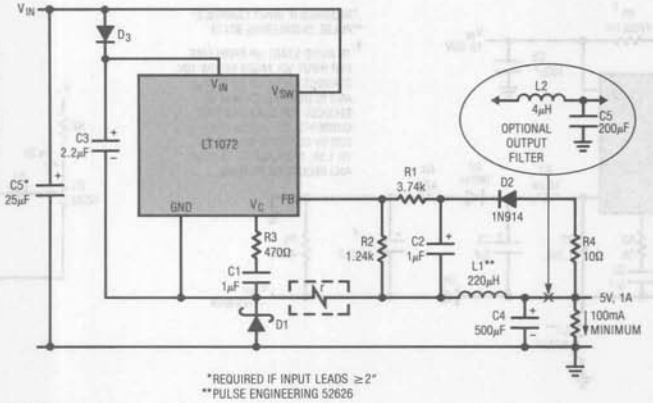
TYPICAL APPLICATIONS

Negative Buck Converter



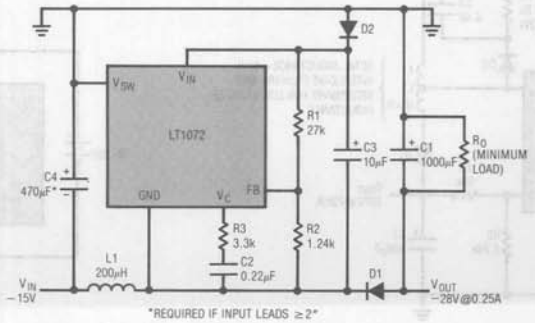
*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 52626

Positive Buck Converter



*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 52626

Negative Boost Regulator



*REQUIRED IF INPUT LEADS ≥ 2"

Step-Down Switching Regulator

FEATURES

- 5A On-Board Switch (LT1074)
- 100kHz Switching Frequency
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5 and 7-Lead Packages
- Only 8.5mA Quiescent Current
- Programmable Current Limit
- Operates Up to 60V Input
- Micropower Shutdown Mode

APPLICATIONS

- Buck Converter with Output Voltage Range of 2.5V to 50V
- Tapped-Inductor Buck Converter with 10A Output at 5V
- Positive-to-Negative Converter
- Negative Boost Converter
- Multiple Output Buck Converter

DESCRIPTION

The LT1074 is a 5A (LT1076 is rated at 2A) monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, and all current limit components, are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive-to-negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing 40V below ground, allowing the LT1074 to drive a tapped-inductor in the buck mode with output currents up to 10A.

The LT1074 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

On-chip pulse by pulse current limiting makes the LT1074 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

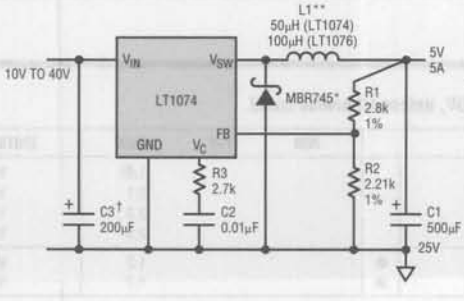
The LT1074 is available in low cost TO-220 or TO-3 packages with frequency pre-set at 100kHz and current limit at 6.5A (LT1076 = 2.6A). A 7-pin TO-220 package is also available which allows current limit to be adjusted down to zero. In addition, full micropower shutdown can be programmed. See Application Note 44 for design details.

A fixed 5V output, 2A version is also available. See LT1076-5.

4

TYPICAL APPLICATION

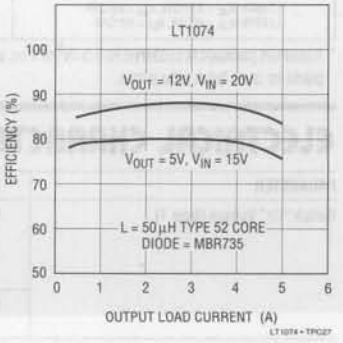
Basic Positive Buck Converter



*USE MBR340 FOR LT1076
**COILTRONICS #50-2-52 (LT1074)
#100-1-52 (LT1076)
PULSE ENGINEERING, INC.
#PE-92114 (LT1074)
#PE-92102 (LT1076)
HURRICANE #HL-AK147QQ (LT1074)
#HL-AG210LL (LT1076)
†RIPPLE CURRENT RATING ≥ I_{OUT} / 2

LT1074 • TA01

Buck Converter Efficiency



LT1074 • TPC27

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1074/ LT1076 ..... 45V
- LT1074HV/76HV 64V

Switch Voltage with Respect to Input Voltage
- LT1074/ 76 ..... 64V
- LT1074HV/76HV 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1074/76 (Note 6) 35V
- LT1074HV/76HV (Note 6) 45V

Feedback Pin Voltage ..... –2V, +10V

Shutdown Pin Voltage (Not to Exceed V_{IN}) 40V

I_{LIM} Pin Voltage (Forced) 5.5V

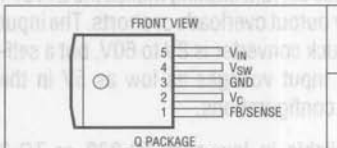
Maximum Operating Ambient Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 70°C
- LT1074I/76I, LT1074HVI/76HVI ..... –40°C to 85°C
- LT1074M/76M, LT1074HVM/76HVM ..... –55°C to 125°C

Maximum Operating Junction Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 125°C
- LT1074I/76I, LT1074HVI/76HVI ..... –40°C to 125°C
- LT1074M/76M, LT1074HVM/76HVM ..... –55°C to 150°C

Maximum Storage Temperature ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

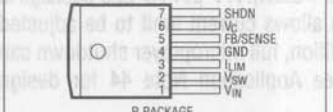
PACKAGE/ORDER INFORMATION



Q PACKAGE
5-LEAD PLASTIC DD
LT1076: θ_{JC} = 4°C/W, θ_{JA} = 30°C/W*

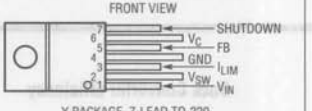
ORDER PART NUMBER

LT1076CQ



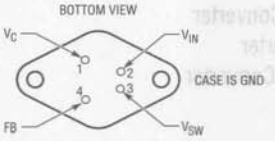
R PACKAGE
7-LEAD PLASTIC DD
LT1076: θ_{JC} = 4°C/W, θ_{JA} = 30°C/W*

LT1076CR
LT1076HVCR



Y PACKAGE, 7-LEAD TO-220
LT1074: θ_{JC} = 2.5°C/W, θ_{JA} = 50°C/W
LT1076: θ_{JC} = 4°C/W, θ_{JA} = 50°C/W

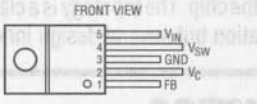
LT1074CY
LT1074HVCY
LT1074IY
LT1074HVIY
LT1076CY
LT1076HVCY



K PACKAGE, 4-LEAD TO-3 METAL CAN
LT1074: θ_{JC} = 2.5°C/W, θ_{JA} = 35°C/W
LT1076: θ_{JC} = 4°C/W, θ_{JA} = 35°C/W

ORDER PART NUMBER

LT1074CK
LT1074HVCK
LT1074MK
LT1074HVMK
LT1076CK
LT1076HVCK
LT1076MK
LT1076HVMK



T PACKAGE, 5-LEAD TO-220
LEADS ARE FORMED STANDARD FOR STRAIGHT LEADS, ORDER FLOW 06
LT1074: θ_{JC} = 2.5°C/W, θ_{JA} = 50°C/W
LT1076: θ_{JC} = 4°C/W, θ_{JA} = 50°C/W

LT1074CT
LT1074HVCT
LT1074IT
LT1074HVIT
LT1076CT
LT1076HVCT
LT1076IT

* Assumes package is soldered to 0.5 IN^2 of 1 oz. copper over internal ground plane or over back side plane.

ELECTRICAL CHARACTERISTICS T_j = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	LT1074 I_{SW} = 1A, $T_j \geq 0°C$				1.85	V
	I_{SW} = 1A, $T_j < 0°C$				2.1	V
	I_{SW} = 5A, $T_j \geq 0°C$				2.3	V
	I_{SW} = 5A, $T_j < 0°C$				2.5	V
	LT1076 I_{SW} = 0.5A	●			1.2	V
	I_{SW} = 2A	●			1.7	V

ELECTRICAL CHARACTERISTICS $T_j = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "Off" Leakage	LT1074 $V_{IN} \leq 25V$, $V_{SW} = 0$			5	300	µA
	$V_{IN} = V_{MAX}$, $V_{SW} = 0$ (Note 7)			10	500	µA
	LT1076 $V_{IN} = 25V$, $V_{SW} = 0$				150	µA
	$V_{IN} = V_{MAX}$, $V_{SW} = 0$ (Note 7)				250	µA
Supply Current (Note 2)	$V_{FB} = 2.5V$, $V_{IN} \leq 40V$	●		8.5	11	mA
	$40V < V_{IN} < 60V$	●		9	12	mA
	$V_{SHUT} = 0.1V$ (Device Shutdown) (Note 8)	●		140	300	µA
Minimum Supply Voltage	Normal Mode	●		7.3	8	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)	LT1074 I_{LIM} Open	●	5.5	6.5	8.5	A
	$R_{LIM} = 10k$ (Note 5)			4.5		A
	$R_{LIM} = 7k$ (Note 5)			3		A
	LT1076 I_{LIM} Open	●	2	2.6	3.2	A
	$R_{LIM} = 10k$ (Note 5)			1.8		A
	$R_{LIM} = 7k$ (Note 5)			1.2		A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
	$T_j \leq 125°C$	●	85		120	kHz
	$T_j > 125°C$	●	85		125	kHz
	$V_{FB} = 0V$ through $2k\Omega$ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 6)	$1V \leq V_C \leq 4V$			2000		V/V
Error Amplifier Transconductance			3700	5000	8000	µmho
Error Amplifier Source and Sink Current	Source ($V_{FB} = 2V$)		100	140	225	µA
	Sink ($V_{FB} = 2.5V$)		0.7	1	1.6	mA
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	µA
Reference Voltage	$V_C = 2V$	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	V_{REF} (Nominal) = 2.21V			±0.5	±1.5	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1	±2.5	%
Reference Voltage Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		−4		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	$V_{SH} = 5V$	●	5	10	20	µA
	$V_{SH} \leq V_{THRESHOLD}$ (≅2.5V)	●			50	µA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.2	2.45	2.7	V
	Fully Shut Down	●	0.1	0.3	0.5	V
Thermal Resistance Junction to Case	LT1074				2.5	°C/W
	LT1076				4.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of 1µs.

Note 5: $I_{LIM} \approx \frac{R_{LIM} - 1k}{2k}$ (LT1074), $I_{LIM} \approx \frac{R_{LIM} - 1k}{5.5k}$ (LT1076).

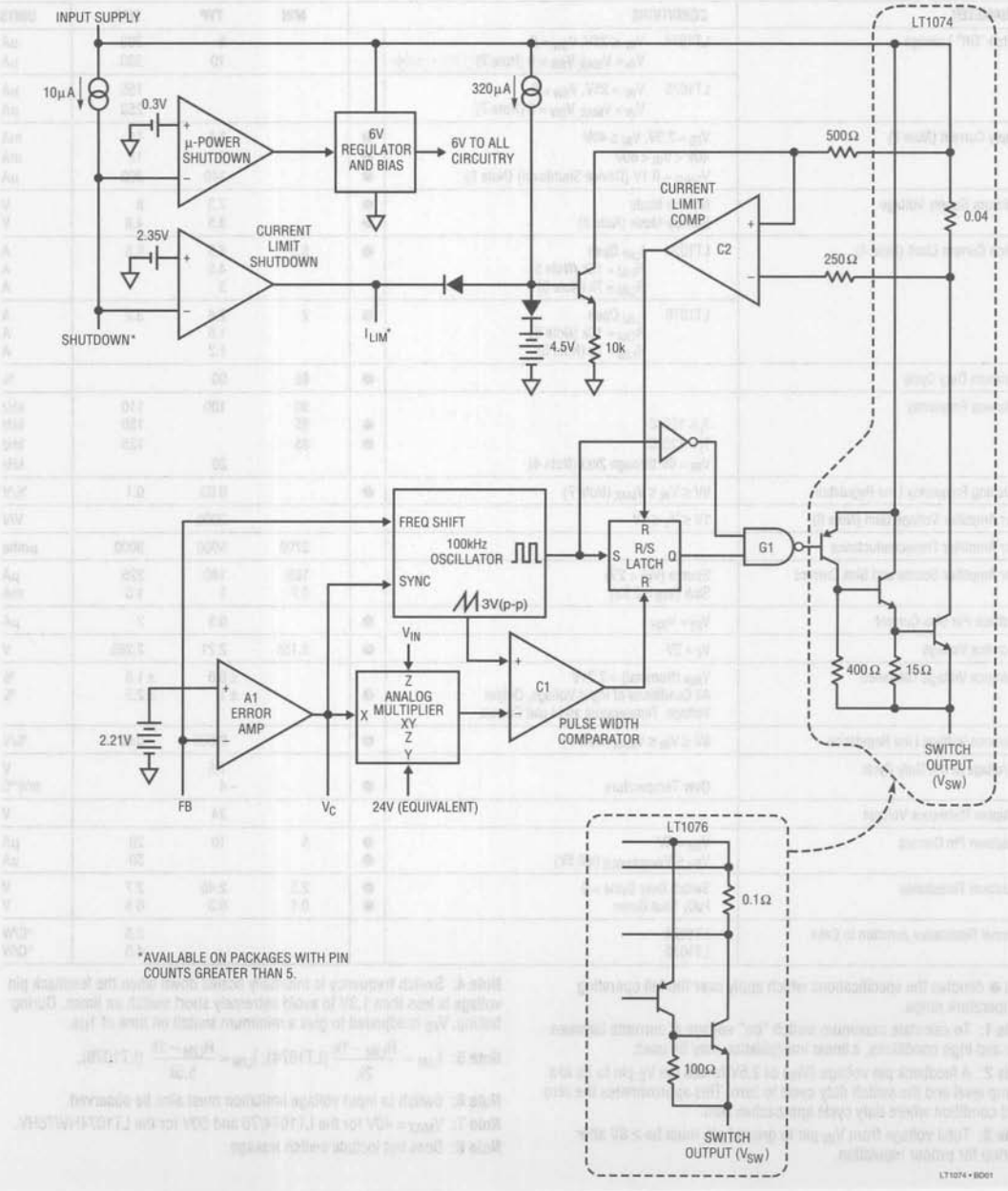
Note 6: Switch to input voltage limitation must also be observed.

Note 7: V_{MAX} = 40V for the LT1074/76 and 60V for the LT1074HV/76HV.

Note 8: Does not include switch leakage.

4

BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 5000μmho. Slew current going positive is 140μA, while negative slew current is about 1.1mA. This asymmetry helps prevent overshoot on start-up. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

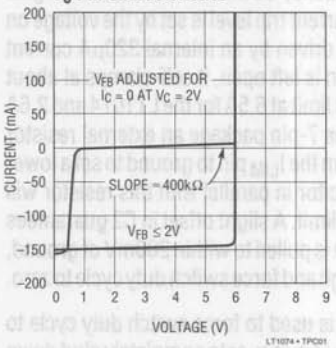
Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn off is approximately 600ns. So minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1.3V. Current trip level is set by the voltage on the I_{LIM} pin which is driven by an internal 320μA current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A for the LT1074 and 2.6A for the LT1076. In the 7-pin package an external resistor can be connected from the I_{LIM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft start the current limit. A slight offset in C2 guarantees that when the I_{LIM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LIM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 150μA. A 10μA pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed start-up. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

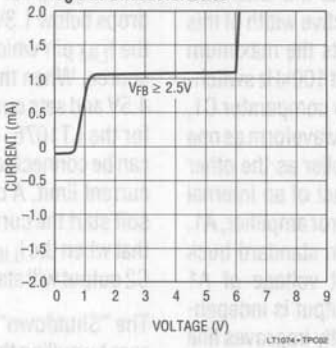
The switch used in the LT1074 is a Darlington NPN (single NPN for LT1076) driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

TYPICAL PERFORMANCE CHARACTERISTICS

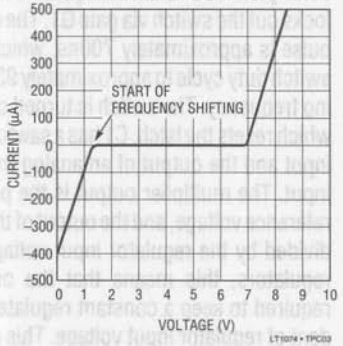
V_C Pin Characteristics



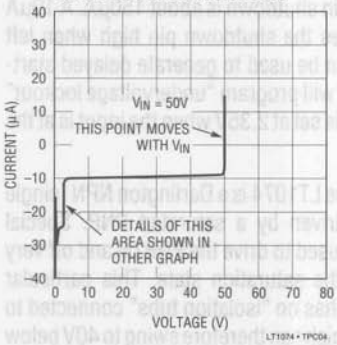
V_C Pin Characteristics



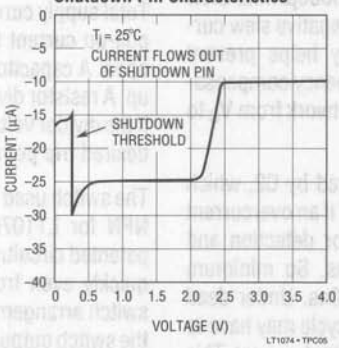
Feedback Pin Characteristics



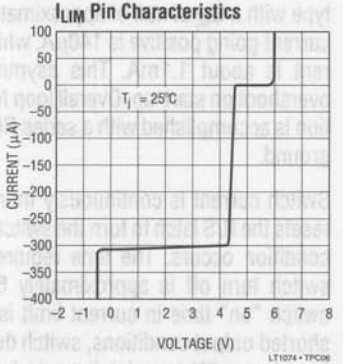
Shutdown Pin Characteristics



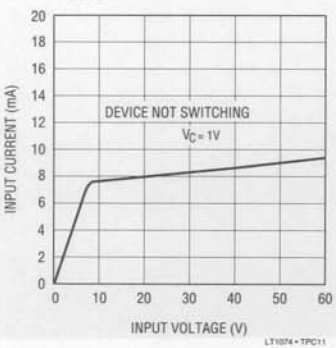
Shutdown Pin Characteristics



I_{LIM} Pin Characteristics

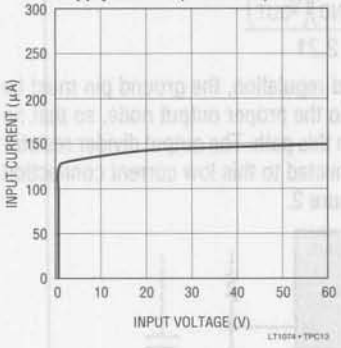


Supply Current

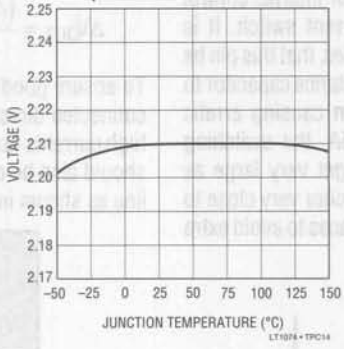


TYPICAL PERFORMANCE CHARACTERISTICS

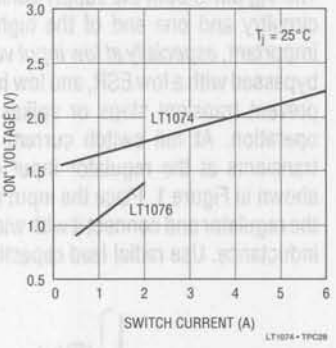
Supply Current (Shutdown)



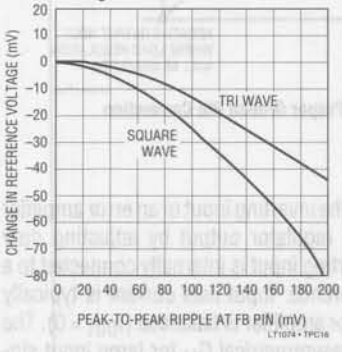
Reference Voltage vs Temperature



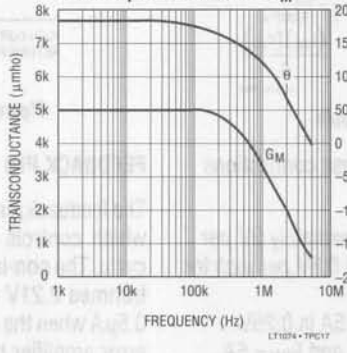
Switch "On" Voltage



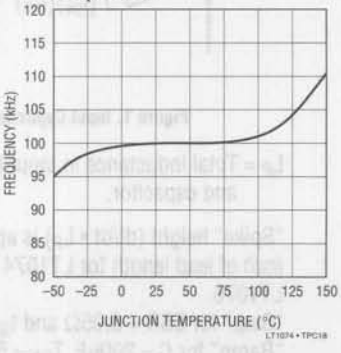
Reference Shift with Ripple Voltage



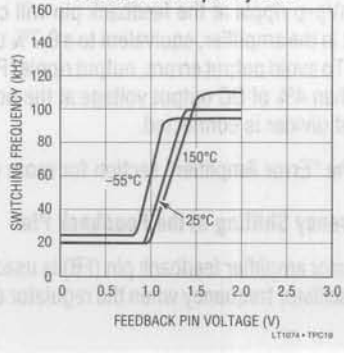
Error Amplifier Phase and G_M



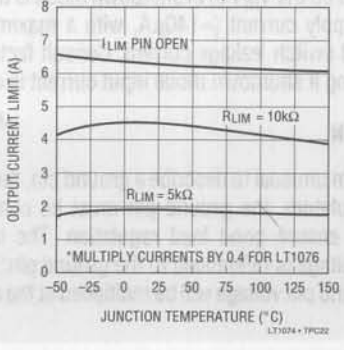
Switching Frequency vs Temperature



Feedback Pin Frequency Shift



Current Limit vs Temperature*



4

PIN DESCRIPTIONS

V_{IN} PIN

The V_{IN} pin is both the supply voltage for internal control circuitry and one end of the high current switch. It is important, *especially at low input voltages*, that this pin be bypassed with a low ESR, and low inductance capacitor to prevent transient steps or spikes from causing erratic operation. At full switch current of 5A, the switching transients at the regulator input can get very large as shown in Figure 1. Place the input capacitor very close to the regulator and connect it with wide traces to avoid extra inductance. Use radial lead capacitors.

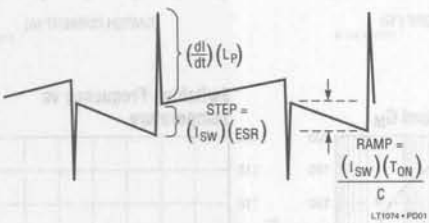


Figure 1. Input Capacitor Ripple

L_P = Total inductance in input bypass connections and capacitor.

"Spike" height (dI/dt • L_P) is approximately 2V *per inch* of lead length for LT1074 and 0.8V *per inch* for LT1076.
"Step" for ESR = 0.05Ω and I_{SW} = 5A is 0.25V.
"Ramp" for C = 200µF, T_{ON} = 5µs, and I_{SW} = 5A, is 0.12V.

Input current on the V_{IN} Pin in shutdown mode is the sum of actual supply current (≈140µA, with a maximum of 300µA), and switch leakage current. Consult factory for special testing if shutdown mode input current is critical.

GROUND PIN

It might seem unusual to describe a ground pin, but in the case of regulators, the ground pin must be connected properly to ensure good load regulation. The internal reference voltage is referenced to the ground pin; so any error in ground pin voltage will be multiplied at the output;

$$\Delta V_{OUT} = \frac{(\Delta V_{GND})(V_{OUT})}{2.21}$$

To ensure good load regulation, the ground pin must be connected directly to the proper output node, so that no high currents flow in this path. The output divider resistor should also be connected to this low current connection line as shown in Figure 2.

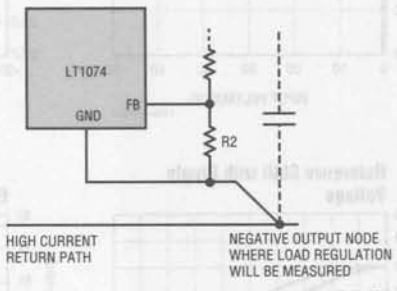


Figure 2. Proper Ground Pin Connection

FEEDBACK PIN

The feedback pin is the inverting input of an error amplifier which controls the regulator output by adjusting duty cycle. The non-inverting input is internally connected to a trimmed 2.21V reference. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0). The error amplifier has asymmetrical G_M for large input signals to reduce startup overshoot. This makes the amplifier more sensitive to large ripple voltages at the feedback pin. 100mVp-p ripple at the feedback pin will create a 14mV offset in the amplifier, equivalent to a 0.7% output voltage shift. To avoid output errors, output ripple (P-P) should be less than 4% of DC output voltage at the point where the output divider is connected.

See the "Error Amplifier" section for more details.

Frequency Shifting at the Feedback Pin

The error amplifier feedback pin (FB) is used to downshift the oscillator frequency when the regulator output voltage

PIN DESCRIPTIONS

is low. This is done to guarantee that output short circuit current is well controlled even when switch duty cycle must be extremely low. Theoretical switch "on" time for a buck converter in continuous mode is;

$$t_{ON} = \frac{V_{OUT} + V_D}{V_{IN} \bullet f}$$

V_D = Catch diode forward voltage (≈ 0.5V)
f = Switching frequency

At f = 100kHz, t_{ON} must drop to 0.2µs when V_{IN} = 25V and the output is shorted (V_{OUT} = 0V). In current limit, the LT1074 can reduce t_{ON} to a minimum value of ≈ 0.6µs, much too long to control current correctly for V_{OUT} = 0. To correct this problem, switching frequency is lowered from 100kHz to 20kHz as the FB pin drops from 1.3V to 0.5V. This is accomplished by the circuitry shown in Figure 3.

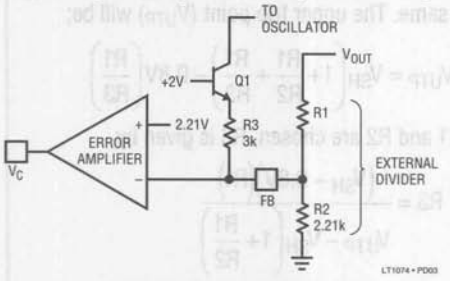


Figure 3. Frequency Shifting

Q1 is off when the output is regulating (V_{FB} = 2.21V). As the output is pulled down by an overload, V_{FB} will eventually reach 1.3V, turning on Q1. As the output continues to drop, Q1 current increases proportionately and lowers the frequency of the oscillator. Frequency shifting starts when the output is ≈ 60% of normal value, and is down to its minimum value of ≅ 20kHz when the output is ≅ 20% of normal value. The rate at which frequency is shifted is determined by both the internal 3k resistor R3 and the external divider resistors. For this reason, R2 should not be increased to more than 4kΩ, if the LT1074 will be subjected to the simultaneous conditions of high input voltage and output short circuit.

SHUTDOWN PIN

The shutdown pin is used for undervoltage lockout, micropower shutdown, soft start, delayed start, or as a general purpose on/off control of the regulator output. It controls switching action by pulling the I_{LIM} pin low, which forces the switch to a continuous "off" state. Full micropower shutdown is initiated when the shutdown pin drops below 0.3V.

The V/I characteristics of the shutdown pin are shown in Figure 4. For voltages between 2.5V and ≈V_{IN}, a current of 10µA flows *out* of the shutdown pin. This current increases to ≈25µA as the shutdown pin moves through the 2.35V threshold. The current increases further to ≈ 30µA at the 0.3V threshold, then drops to ≈15µA as the shutdown voltage falls below 0.3V. The 10µA current source is included to pull the shutdown pin to its high or default state when left open. It also provides a convenient pullup for delayed start applications with a capacitor on the shutdown pin.

When activated, the typical collector current of Q1 in Figure 5, is ≈ 2mA. A soft start capacitor on the I_{LIM} pin will delay regulator shutdown in response to C1, by ≈(5V)(C_{LIM})/2mA. Soft start after full micropower shutdown is ensured by coupling C2 to Q1.

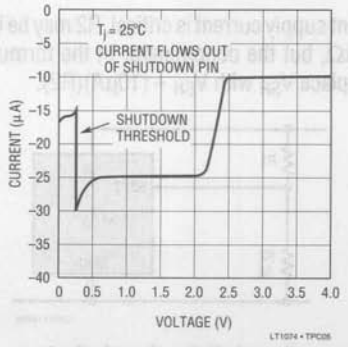


Figure 4. Shutdown Pin Characteristics

PIN DESCRIPTIONS

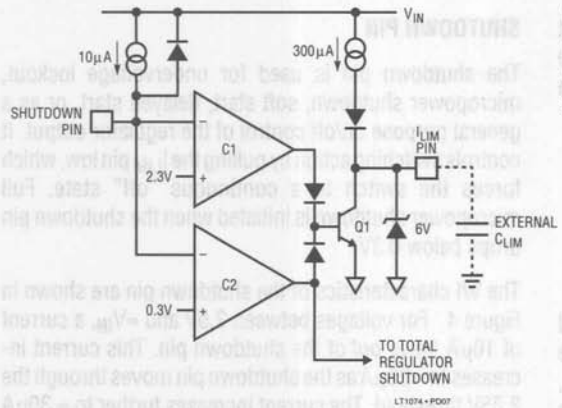


Figure 5. Shutdown Circuitry

Undervoltage Lockout

Undervoltage lockout point is set by R1 and R2 in Figure 6. To avoid errors due to the 10μA shutdown pin current, R2 is usually set at 5k, and R1 is found from:

$$R1 = R2\frac{(V_{TP} - V_{SH})}{V_{SH}}$$

V_{TP} = Desired undervoltage lockout voltage.

V_{SH} = Threshold for lockout on the shutdown pin = 2.45V.

If quiescent supply current is critical, R2 may be increased up to 15kΩ, but the denominator in the formula for R2 should replace V_{SH} with $V_{SH} - (10\mu A)(R2)$.

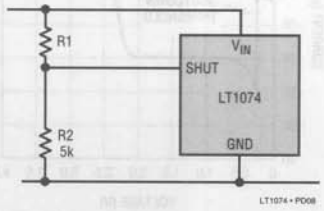


Figure 6. Undervoltage Lockout

Hysteresis in undervoltage lockout may be accomplished by connecting a resistor (R3) from the I_{LIM} pin to the shutdown pin as shown in Figure 7. D1 prevents the shutdown divider from altering current limit.

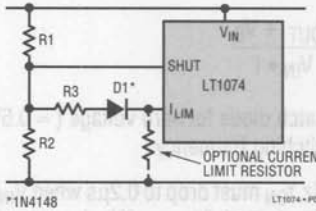


Figure 7. Adding Hysteresis

$$\text{Trip Point} = V_{TP} = 2.35V\left(1 + \frac{R1}{R2}\right)$$

If R3 is added, the lower trip point (V_{IN} descending) will be the same. The upper trip point (V_{UTP}) will be;

$$V_{UTP} = V_{SH}\left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right) - 0.8V\left(\frac{R1}{R3}\right)$$

If R1 and R2 are chosen, R3 is given by

$$R3 = \frac{(V_{SH} - 0.8V)(R1)}{V_{UTP} - V_{SH}\left(1 + \frac{R1}{R2}\right)}$$

Example: An undervoltage lockout is required such that the output will not start until V_{IN} = 20V, but will continue to operate until V_{IN} drops to 15V. Let R2 = 2.32k.

$$R1 = (2.32k)\frac{(15V - 2.35V)}{2.35V} = 12.5k$$

$$R3 = \frac{(2.35 - 0.8)(12.5)}{20 - 2.35\left(1 + \frac{12.5}{2.32}\right)} = 3.9k$$

PIN DESCRIPTIONS

I_{LIM} PIN

The I_{LIM} pin is used to reduce current limit below the preset value of 6.5A. The equivalent circuit for this pin is shown in Figure 8.

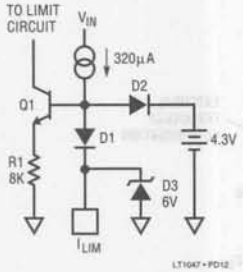


Figure 8. I_{LIM} Pin Circuit

When I_{LIM} is left open, the voltage at Q1 base clamps at 5V through D2. Internal current limit is determined by the current through Q1. If an external resistor is connected between I_{LIM} and ground, the voltage at Q1 base can be reduced for lower current limit. The resistor will have a voltage across it equal to (320µA) (R), limited to ≈ 5V when clamped by D2. Resistance required for a given current limit is

$$R_{LIM} = I_{LIM}\ (2k\Omega) + 1k\Omega\ (LT1074)$$

$$R_{LIM} = I_{LIM}\ (5.5k\Omega) + 1k\Omega\ (LT1076)$$

As an example, a 3A current limit would require 3A (2k) + 1k = 7kΩ for the LT1074. The accuracy of these formulas is ±25% for $2A \le I_{LIM} \le 5A$ (LT1074) and $0.7A \le I_{LIM} \le 1.8A$ (LT1076), so I_{LIM} should be set at least 25% above the *peak* switch current required.

Foldback current limiting can be easily implemented by adding a resistor from the output to the I_{LIM} pin as shown in Figure 9. This allows full desired current limit (with or without R_{LIM}) when the output is regulating, but reduces current limit under short circuit conditions. A typical value for R_{FB} is 5kΩ, but this may be adjusted up or down to set the amount of foldback. D2 prevents the output voltage from forcing current back into the I_{LIM} pin. To calculate a value for R_{FB}, first calculate R_{LIM}, then R_{FB}:

$$R_{FB} = \frac{\left(I_{SC} - 0.44^*\right)\left(R_L\right)}{0.5^*\left(R_L - 1k\Omega\right) - I_{SC}}\left(R_L \text{ in } k\Omega\right)$$

*Change 0.44 to 0.16, and 0.5 to 0.18 for LT1076.

Example: I_{LIM} = 4A, I_{SC} = 1.5A, R_{LIM} = (4)(2k) + 1k = 9k

$$R_{FB} = \frac{(1.5 - 0.44)(9k\Omega)}{0.5(9k - 1k) - 1.5}$$

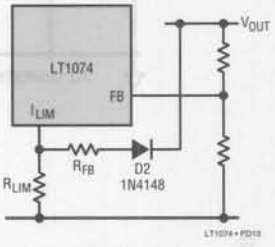


Figure 9. Foldback Current Limit

ERROR AMPLIFIER

The error amplifier in Figure 10 is a single stage design with added inverters to allow the output to swing above and below the common mode input voltage. One side of the amplifier is tied to a trimmed internal reference voltage of 2.21V. The other input is brought out as the FB (feedback) pin. This amplifier has a G_M (voltage "in" to current "out") transfer function of ≈5000µmho. Voltage gain is determined by multiplying G_M times the total equivalent output loading, consisting of the output resistance of Q4 and Q6 in parallel with the series RC external frequency compensation network. At DC, the external RC is ignored, and with a parallel output impedance for Q4 and Q6 of 400kΩ, voltage gain is ≈ 2000. At frequencies above a few hertz, voltage gain is determined by the external compensation, R_C and C_C.

4

PIN DESCRIPTIONS

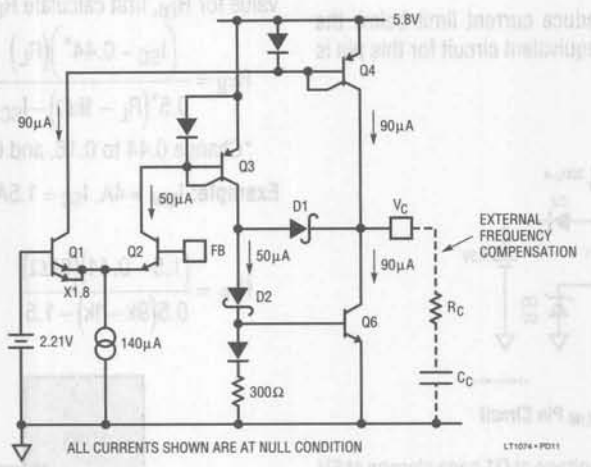


Figure 10. Error Amplifier

$$A_V = \frac{G_m}{2\pi \bullet f \bullet C_C} \text{ at midfrequencies}$$

$$A_V = G_m \bullet R_C \text{ at highfrequencies}$$

Phase shift from the FB pin to the V_C pin is 90° at mid-frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. The low frequency "pole" where the reactance of C_C is equal to the output impedance of Q4 and Q6 (r_O), is

$$f_{POLE} = \frac{1}{2\pi \bullet r_O \bullet C} \quad r_O \approx 400k\Omega$$

Although f_{POLE} varies as much as 3:1 due to r_O variations, mid-frequency gain is dependent only on G_M, which is specified much tighter on the data sheet. The higher frequency "zero" is determined solely by R_C and C_C.

$$f_{ZERO} = \frac{1}{2\pi \bullet R_C \bullet C_C}$$

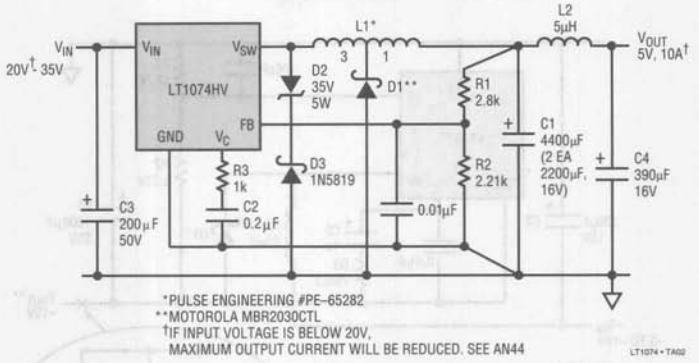
The error amplifier has *asymmetrical* peak output current. Q3 and Q4 current mirrors are unity gain, but the Q6 mirror has a gain of 1.8 at output null and a gain of 8 when the FB pin is high (Q1 current = 0). This results in a maximum positive output current of 140µA and a maximum negative (sink) output current of ≅ 1.1mA. The asymmetry is deliberate—it results in much less regulator output overshoot during rapid start-up or following the release of an output overload. Amplifier offset is kept low by area scaling Q1 and Q2 at 1.8:1.

Amplifier swing is limited by the internal 5.8V supply for positive outputs and by D1 and D2 when the output goes low. Low clamp voltage is approximately one diode drop (≈ 0.7V – 2mV/°C).

Note that both the FB pin and the V_C pin have other internal connections. Refer to the frequency shifting and sychronizing discussions.

TYPICAL APPLICATIONS

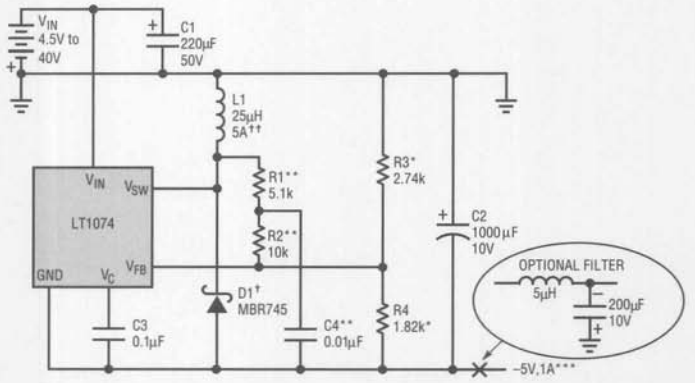
Tapped-Inductor Buck Converter



*PULSE ENGINEERING #PE–65282
**MOTOROLA MBR2030CTL
†IF INPUT VOLTAGE IS BELOW 20V,
MAXIMUM OUTPUT CURRENT WILL BE REDUCED. SEE AN44

LT1074 • TA02

Positive-to-Negative Converter with 5V Output



* = 1% FILM RESISTORS
D1 = MOTOROLA-MBR745
C1 = NICHICON-UPL1C221MRH6
C2 = NICHICON-UPL1A102MRH6
L1 = COILTRONICS-CTX25-5-52

† LOWER REVERSE VOLTAGE RATING MAY BE USED FOR LOWER INPUT VOLTAGES. LOWER CURRENT RATING IS ALLOWED FOR LOWER OUTPUT CURRENT. SEE AN44.

†† LOWER CURRENT RATING MAY BE USED FOR LOWER OUTPUT CURRENT. SEE AN44.

** R1, R2, AND C4 ARE USED FOR LOOP FREQUENCY COMPENSATION WITH LOW INPUT VOLTAGE, BUT R1 AND R2 MUST BE INCLUDED IN THE CALCULATION FOR OUTPUT VOLTAGE DIVIDER VALUES. FOR HIGHER OUTPUT VOLTAGES, INCREASE R1, R2, AND R3 PROPORTIONATELY. FOR INPUT VOLTAGE > 10V, R1, R2, AND C4 CAN BE ELIMINATED, AND COMPENSATION IS DONE TOTALLY ON THE V_C PIN.
R3 = V_{OUT} –2.37 (KΩ)
R1 = (R3) (1.86)
R2 = (R3) (3.65)

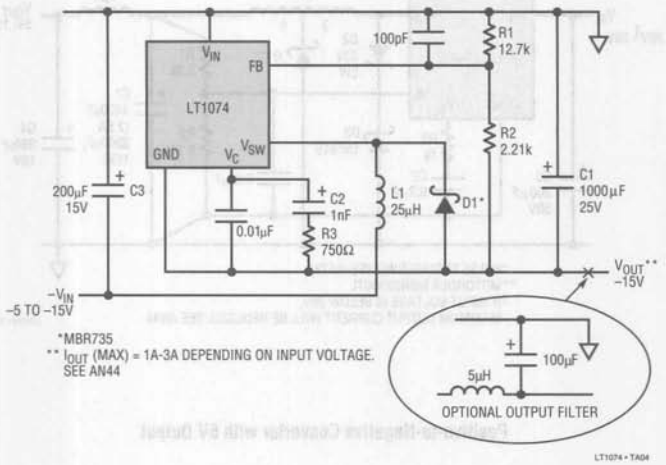
*** MAXIMUM OUTPUT CURRENT OF 1A IS DETERMINED BY MINIMUM INPUT VOLTAGE OF 4.5V. HIGHER MINIMUM INPUT VOLTAGE WILL ALLOW MUCH HIGHER OUTPUT CURRENTS. SEE AN44.

LT1074 • TA03

4

TYPICAL APPLICATIONS

Negative Boost Converter



*MBR735
** I_{OUT} (MAX) = 1A-3A DEPENDING ON INPUT VOLTAGE. SEE AN44

1A High Voltage, Efficiency Switching Voltage Regulator

FEATURES

- Wide Input Voltage Range: 3V to 75V
- High Switch Voltage: 100V
- Low Quiescent Current: 4.5mA
- Internal 1A Switch
- Shutdown Mode Draws Only 120µA Supply Current
- Isolated Flyback Regulation Mode for Fully Floating Outputs
- Can Be Externally Synchronized
- Available in MiniDIP and TO-220 Packages
- Same Pinout as LT1072

APPLICATIONS

- Telecom 5V Supply at 0.7A from –48V
- 90V Supply at 120mA from 15V
- All Applications Using LT1072 (See Below for Specification Differences)

LT1082 and LT1072 Major Specification Differences

	LT1082C	LT1072HV
V_{IN}	3V to 75V	3V to 60V
V_{SW}	100V	75V
Switch Current Limit	1A	1.25A
Quiescent Current	4.5mA	6mA
Operating Frequency	60kHz	40kHz
Flyback Reference Voltage	16.2 + 0.6 (35kΩ/R_{FB})	16 + 0.35 (7kΩ/R_{FB})

USER NOTE: This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1082. Application circuits are included to show the capability of the LT1082. A complete design manual (AN19) and Switcher CAD (LTC Switching Power Supply Design Program) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1082 by factoring in the lower switch current rating.

DESCRIPTION

The LT1082 is a monolithic high voltage switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, and inverting. A 1A high efficiency switch is included on the die along with all oscillator, control, and protection circuitry.

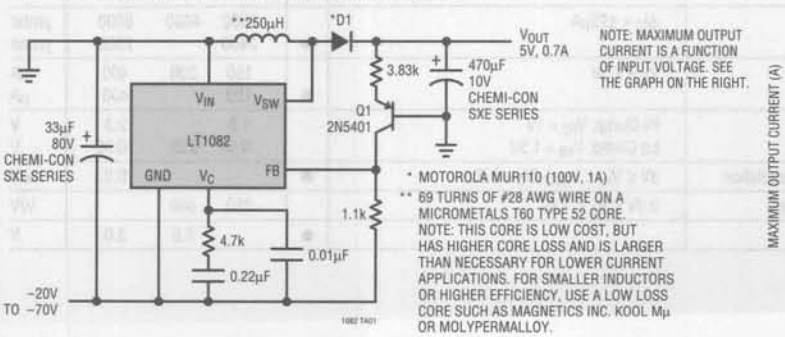
The LT1082 operates with supply voltages from 3V to 75V, switch voltage up to 100V and draws only 4.5mA quiescent current. It can deliver load power up to 20W with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

An externally activated shutdown mode reduces total supply current to 120µA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "isolated flyback regulation mode" built into the LT1082, without the need for optocouplers or extra transformer windings.

The LT1082 has a unique feature to provide high voltage short-circuit protection. When the FB pin is pulled down to 0.6V and the current out of the pin reaches approximately 350µA, the switching frequency will shift down from 60kHz to 12kHz.

The LT1082 is nearly identical to the lower voltage LT1072. For the major differences in specifications, see the table on the left.

Negative-to-Positive Telecom 5V Supply

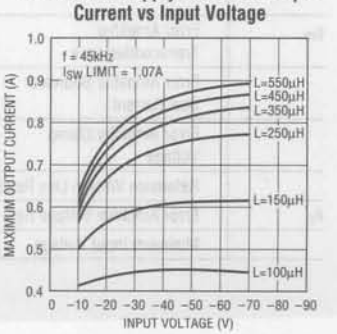


NOTE: MAXIMUM OUTPUT CURRENT IS A FUNCTION OF INPUT VOLTAGE. SEE THE GRAPH ON THE RIGHT.

* MOTOROLA MUR110 (100V, 1A)

** 69 TURNS OF #28 AWG WIRE ON A MICROMETALS T60 TYPE 52 CORE. NOTE: THIS CORE IS LOW COST, BUT HAS HIGHER CORE LOSS AND IS LARGER THAN NECESSARY FOR LOWER CURRENT APPLICATIONS. FOR SMALLER INDUCTORS OR HIGHER EFFICIENCY, USE A LOW LOSS CORE SUCH AS MAGNETICS INC. KOOL Mµ OR MOLYPERMALLOY.

Telecom 5V Supply Maximum Output Current vs Input Voltage

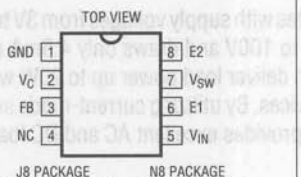


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 75V
Switch Output Voltage 100V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Junction Temperature Range
LT1082M ..... – 55°C to 150°C
LT1082I ..... – 40°C to 125°C
LT1082C ..... 0°C to 100°C

PACKAGE/ORDER INFORMATION

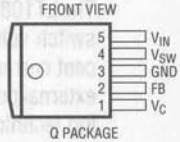


J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (MJ8)
T_{JMAX} = 100°C, θ_{JA} = 90°C/W (CN8)
T_{JMAX} = 125°C, θ_{JA} = 90°C/W (IN8)

ORDER PART NUMBER

LT1082MJ8
LT1082CN8
LT1082IN8



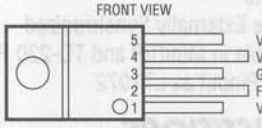
Q PACKAGE
5-LEAD DD

T_{JMAX} = 100°C, θ_{JA} = 40°C/W (CQ)
T_{JMAX} = 125°C, θ_{JA} = 40°C/W (IQ)

NOTE: θ_{JA} VARIES FROM 25°C/W TO 50°C/W DEPENDING ON BOARD COMPOSITION.

ORDER PART NUMBER

LT1082CQ
LT1082IQ



T PACKAGE
5-LEAD TO-220

T_{JMAX} = 100°C, θ_{JA} = 75°C/W, θ_{JC} = 8°C/W (CT)
T_{JMAX} = 125°C, θ_{JA} = 75°C/W, θ_{JC} = 8°C/W (IT)

ORDER PART NUMBER

LT1082CT
LT1082IT

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		V_C = 0.8V	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	nA
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		3000	4400	6000	µmho
			●	2400		7000	µmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	400	µA
			●	120		400	µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.12	0.22	0.36	V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		350	650		V/V
	Minimum Input Voltage		●		2.6	3.0	V

ELECTRICAL CHARACTERISTICS V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.6V			4.5	7.0	mA
	Control Pin Threshold	Duty Cycle = 0		0.7	0.9	1.1	V
			●	0.5		1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.58	0.67	0.8	V
f	Switching Frequency			50	60	70	kHz
			●	45		75	kHz
		$800\mu A \ge I_{FB} \ge 450\mu A$			12		kHz
BV	Output Switch Breakdown Voltage	$3V \le V_{IN} \le V_{MAX}$, I_{SW} = 1.5mA	●	100	115		V
	Control Voltage to Switch Current Transconductance				1.5		A/V
V_{FB}	Flyback Reference Voltage	I_{FB} = 60µA		17	18.6	20.5	V
			●	16		21.5	V
	Change in Flyback Reference Voltage	$60\mu A \le I_{FB} \le 200\mu A$		3.5	4.6	6.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 60µA, $3V \le V_{IN} \le V_{MAX}$			0.01	0.03	%/V
	Flyback Amplifier Transconductance (g_m)	$\Delta I_C = \pm 10\mu A$		150	300	850	µmho
	Flyback Amplifier Source	V_C = 0.6V Source	●	15	32	70	µA
	and Sink Current	I_{FB} = 60µA Sink	●	30	50	90	µA
V_{SAT}	Output Switch "On" Resistance (Note 1)	I_{SW} = 0.7A (LT1082C), I_{SW} = 0.5A (LT1082M)	●		0.8	1.2	Ω
I_{LIM}	Switch Current Limit (LT1082C)	Duty Cycle = 20%	●	1.07		2.6	A
		Duty Cycle ≤ 50%	●	1.0		2.6	A
		Duty Cycle = 80% (Note 2)	●	0.8		2.4	A
	Switch Current Limit (LT1082I)	Duty Cycle = 20%	●	0.85		2.8	A
		Duty Cycle ≤ 50%	●	0.8		2.8	A
		Duty Cycle = 80% (Note 2)	●	0.65		2.6	A
	Switch Current Limit (LT1082M)	Duty Cycle = 20%	●	0.75		3.0	A
		Duty Cycle ≤ 50%	●	0.7		3.0	A
		Duty Cycle = 80% (Note 2)	●	0.6		2.8	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch-On Time				35	45	mA/A
DC_{MAX}	Maximum Switch Duty Cycle			85	92	97	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.05V			120	350	µA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$		70	150	250	mV
			●	50		300	mV

The ● denotes the specifications which apply over the operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current decreases linearly.

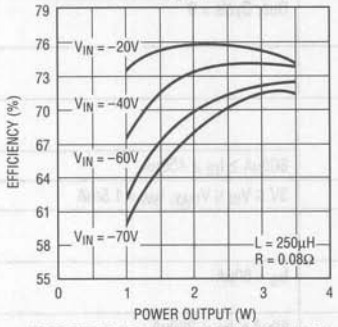
TYPICAL PERFORMANCE CHARACTERISTICS

Suggested Core Size and Inductance for Telecom 5V Supply

LOAD CURRENT	TYPE 52 POWDERED IRON	KOOL Mμ OR MOLY-PERMALLOY
100mA	T38 250μH	T38 200μH
200mA	T50 250μH	T38 150μH
400mA	T60 250μH	T50 150μH
600mA	T60 250μH	T50 200μH
800mA	T80 350μH	T80 350μH

1082 GA

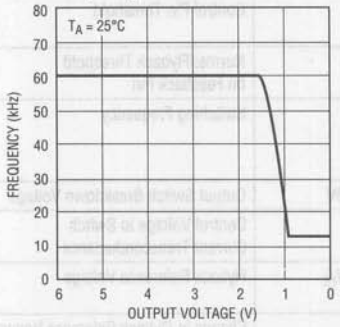
Telecom 5V Supply Efficiency



NOTE: THIS GRAPH IS BASED ON LOW CORE LOSS PERMALLOY INDUCTOR. IF POWDERED IRON CORE INDUCTOR IS USED, THE CORE LOSS IS TYPICALLY 100mW HIGHER.

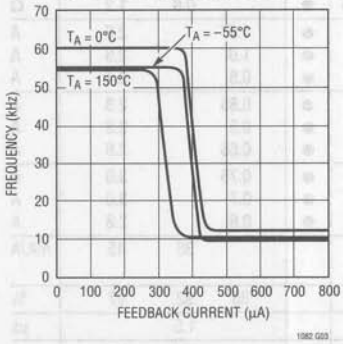
1082 G01

Telecom 5V Supply Short-Circuit Frequency Shift-Down



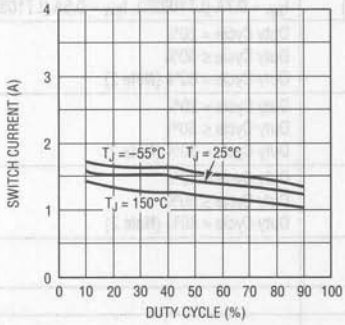
1082 G02

Short-Circuit Frequency Shift-Down vs Feedback Current



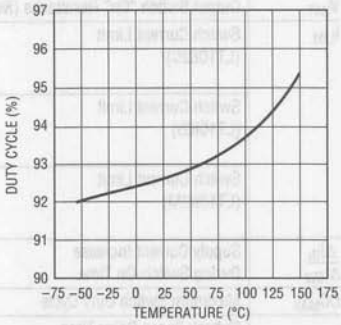
1082 G03

Switch Current Limit



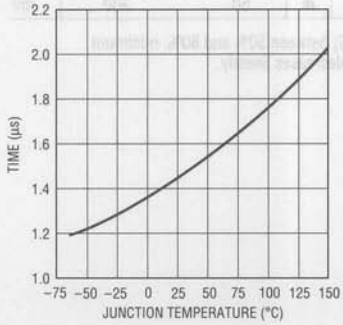
1082 G04

Maximum Duty Cycle



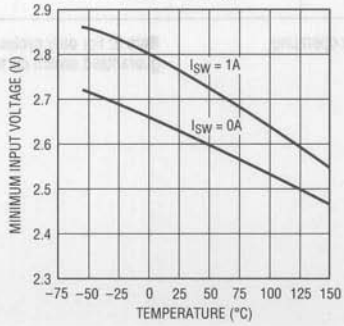
1082 G05

Flyback Blanking Time



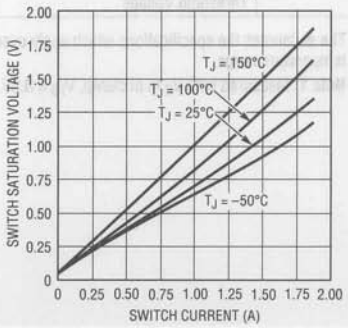
1082 G06

Minimum Input Voltage



1082 G07

Switch Saturation Voltage

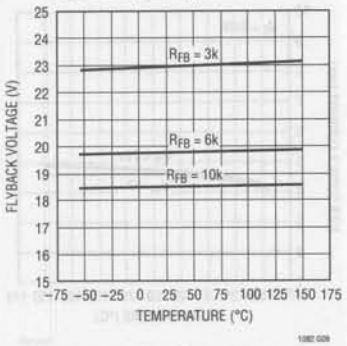


1082 G08

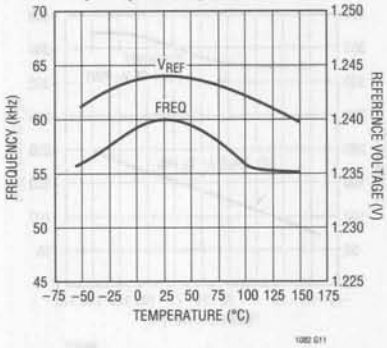
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

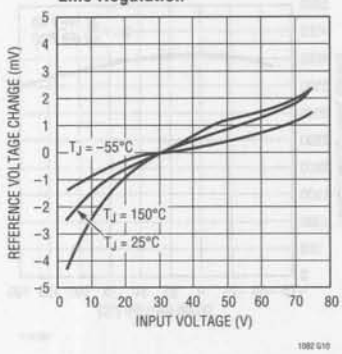
Isolated Mode Flyback Reference Voltage



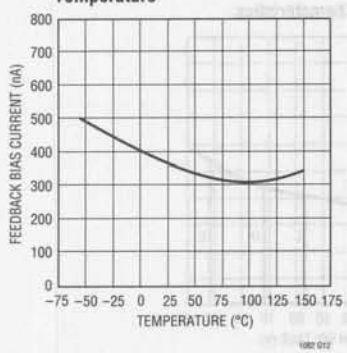
Reference Voltage and Switching Frequency vs Temperature



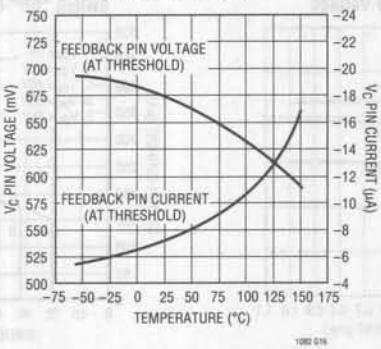
Line Regulation



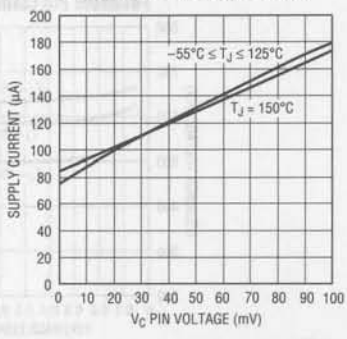
Feedback Bias Current vs Temperature



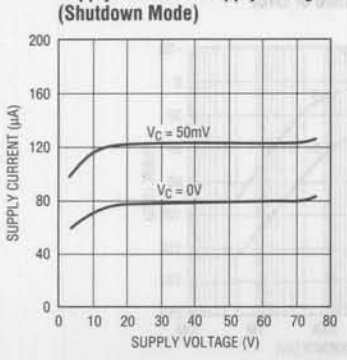
Normal/Feedback Mode Threshold on Feedback Pin



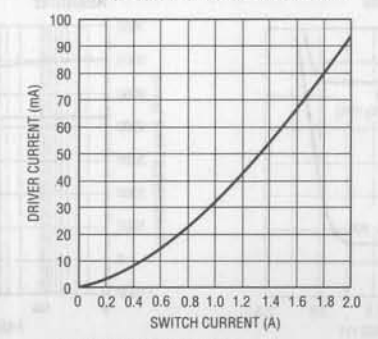
Shutdown Mode Supply Current



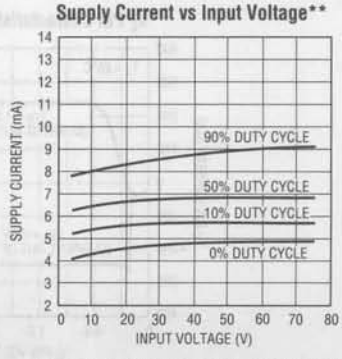
Supply Current vs Supply Voltage (Shutdown Mode)



Driver Current* vs Switch Current



Supply Current vs Input Voltage**



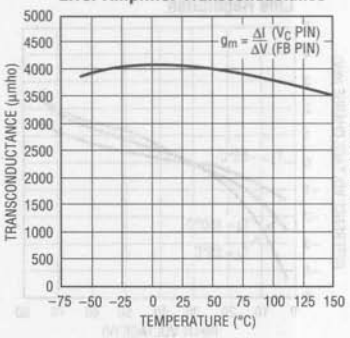
* AVERAGE SUPPLY CURRENT
$= I_Q + DC(2.9 + 10^{-2}I_{SW} + 10^{-5}I_{SW}^2)$
I_Q = QUIESCENT CURRENT, DC = DUTY CYCLE,
I_{SW} = SWITCH CURRENT
1082 G13

** UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

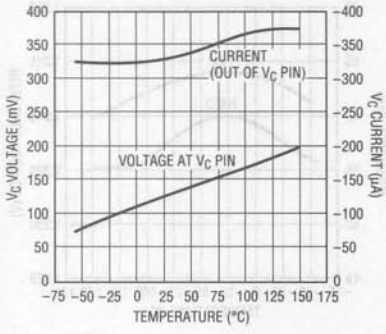
4

TYPICAL PERFORMANCE CHARACTERISTICS

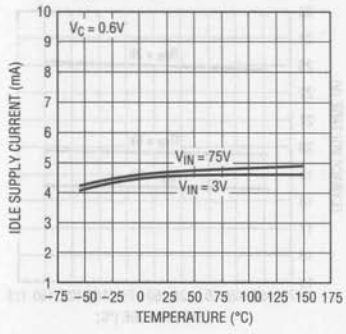
Error Amplifier Transconductance



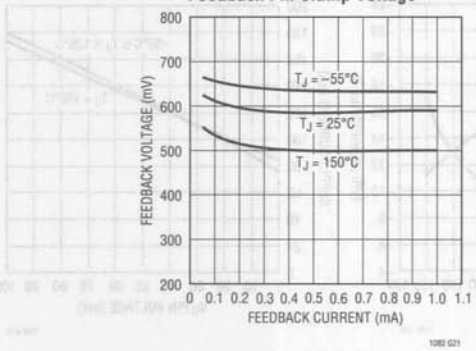
Shutdown Thresholds



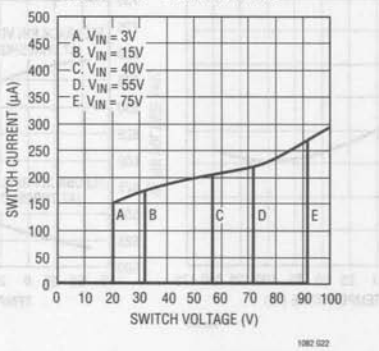
Idle Supply Current vs Temperature



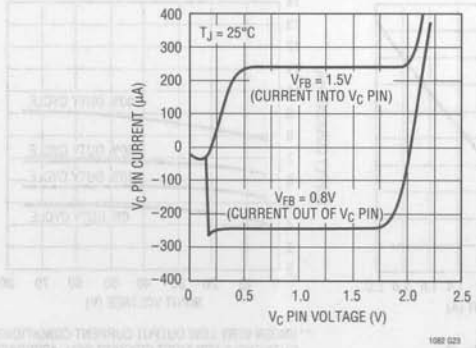
Feedback Pin Clamp Voltage



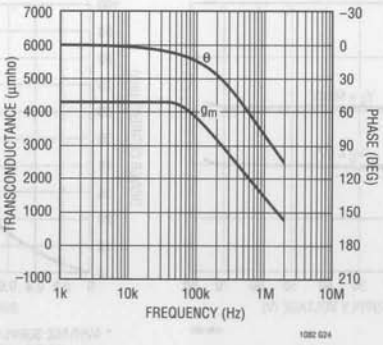
Switch "Off" Characteristics



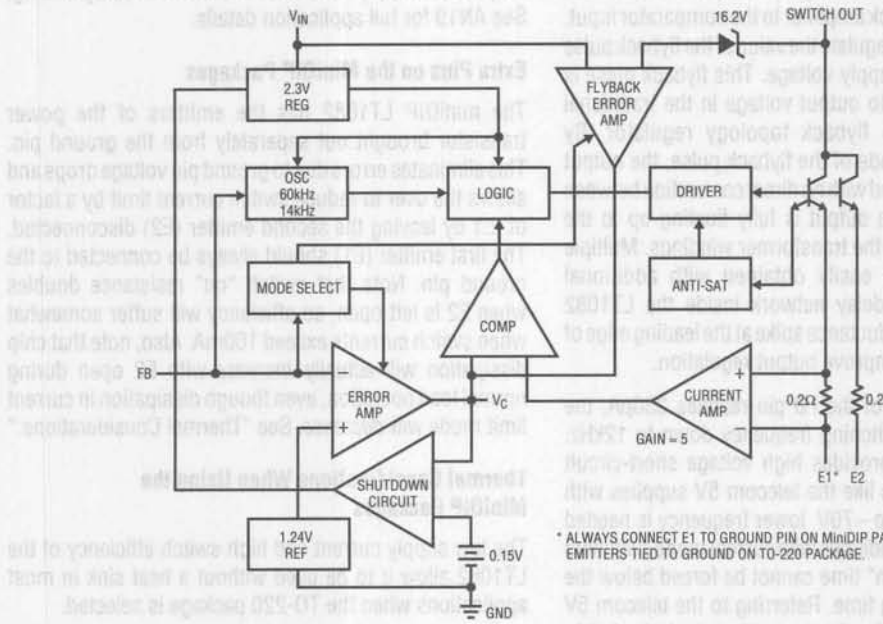
V_C Pin Characteristics



Transconductance of Error Amplifier



BLOCK DIAGRAM



OPERATION

The LT1082 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1082. This low dropout design allows input voltage to vary from 3V to 75V with virtually no change in device performance. A 60kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function: when pulled low with an external resistor and with I_{FB} of 60μA to 200μA, it programs the LT1082 to

4

OPERATION

disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1082 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1082 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

When I_{FB} drawn out of the FB pin reaches 350μA, the LT1082 shifts the switching frequency down to 12kHz. This unique feature provides high voltage short-circuit protection in systems like the telecom 5V supplies with input voltages down to –70V; lower frequency is needed under short-circuit conditions with current mode switchers because minimum "on" time cannot be forced below the internally set blanking time. Referring to the telecom 5V supply circuit on the front page, with output shorted to ground, the V_{FB} stays at 0.6V when sourcing I_{FB} up to 1mA. If the FB pin is forced to source more than 1mA, the frequency shifting function may be defeated. Therefore, the minimum suggested value for R_{FB} is 1k and the maximum suggested value is 1.2k. Also, no capacitance more than 1nF should be used on the FB pin, because it may cause unstable switching frequency in this low frequency mode.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2V (high output current). The error amplifiers are current output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1082 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 120μA supply current for shutdown circuitry biasing. See AN19 for full application details.

Extra Pins on the MiniDIP Packages

The miniDIP LT1082 has the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit by a factor of 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 100mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*. See "Thermal Considerations."

Thermal Considerations When Using the MiniDIP Packages

The low supply current and high switch efficiency of the LT1082 allow it to be used without a heat sink in most applications when the TO-220 package is selected.

This package is rated at 50°C/W. The miniDIPs, however, are rated at 100°C/W in ceramic (J) and 90°/W in plastic (N).

Care should be taken for miniDIP applications to ensure that the worst case input voltage and load current conditions do not cause excessive die temperatures. The following formulas can be used as a rough guide to calculate LT1082 power dissipation. For more details, the reader is referred to Application Note 19 (AN19), "Efficiency Calculations" section.

Average supply current (including driver current) is:

$$I_{IN} \approx 4.5mA + I_{SW}\,(0.004 + DC/28)$$

I_{SW} = switch current
DC = switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2 \bullet R_{SW} \bullet DC$$

R_{SW} = LT1082 switch "on" resistance (1.2Ω maximum)

OPERATION

Total power dissipation is the sum of supply current times input voltage plus switch power:

$$P_{TOT} = (I_{IN})(V_{IN}) + P_{SW}$$

In a typical example, using negative-to-positive converter to generate 5V at 0.5A from a –45V input, duty cycle is approximately 12%, and switch current is about 0.5A, yielding:

$$I_{IN} = 4.5mA + 0.5(0.004 + DC/28) = 8.7mA$$

$$P_{SW} = (0.5)^2 \bullet 1.2\Omega \bullet (0.12) = 0.036W$$

$$P_{TOT} = (45V)(8.7mA) + 0.036 = 0.43W$$

Temperature rise in a plastic miniDIP would be 90°C/W times 0.43W, or approximately 39°C. The maximum ambient temperature would be limited to 100°C (commercial temperature limit) minus 39°C, or 61°C.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, four approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1082 will protect the die in most applications by shutting off switch current. *Thermal limit* is not a tested parameter, however, and should be considered only for noncritical applications with temporary overloads. A second approach is to use the larger TO-220 (T) package which, even without a heat sink, may limit die temperatures to safe levels under overload conditions. In critical situations, heat sinking of these packages is required; especially if overload conditions must be tolerated for extended periods of time.

The third approach for lower current applications is to leave the second switch emitter (miniDIP only) open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The fourth approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1082 switch current limit is zero at approximately 1V on the V_C pin and 1.6A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN19 for details.

LT1082 Synchronizing

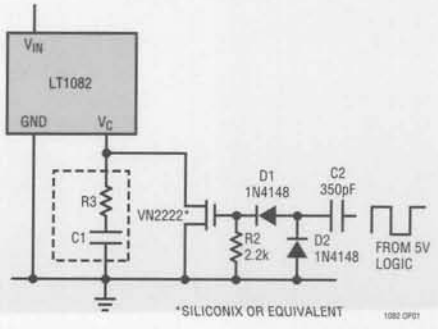
The LT1082 can be externally synchronized in the frequency range of 75kHz to 90kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under 1µs. C2 sets the pulse width at ≈ 0.6µs. The effect of a synchronizing pulse on the LT1082 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right)(t_S)(f_S)\left(I_C + \frac{V_C}{R3}\right)}{I_C}$$

KT/q = 26mV at 25°C
t_S = pulse width
f_S = pulse frequency
I_C = LT1082 V_C source current (≈ 200µA)
V_C = LT1082 operating V_C voltage (1V to 2V)
R3 = resistor used to set mid-frequency "zero" in LT1082 frequency compensation network.

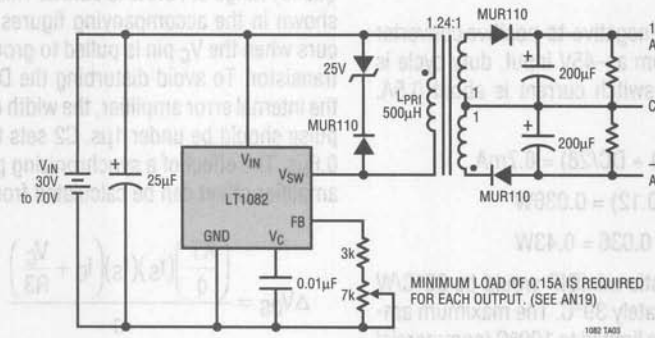
With t_S = 0.6µs, f_S = 80kHz, V_C = 1.5V, and R3 = 2k, offset voltage shift is ≈ 5mV. This is not particularly bothersome, but note that high offset could result if R3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R3, so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 100mV of ground to ensure synchronizing.

Synchronizing the LT1082

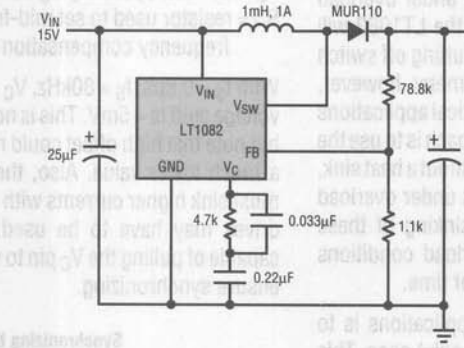


TYPICAL APPLICATIONS

Totally Isolated Converter



Boost Converter



Offline Switching Regulator

FEATURES

- ±1% Line and Load Regulation with No Opto-Coupler
- Switch Frequency up to 200kHz
- Internal 2A Switch and Current Sense (LT1103)
- Internal 1A Totem Pole Driver (LT1105)
- Start-Up Mode Draws Only 200µA
- Fully Protected Against Overloads
- Overvoltage Lockout of Main Supply
- Protected Against Underdrive or Overdrive to FET
- Operates in Continuous or Discontinuous Mode
- Ideal for Flyback and Forward Topologies
- Isolated Flyback Mode Has Fully Floating Outputs

APPLICATIONS

- Up to 250W Isolated Mains Converter
- Up to 50W Isolated Telecom Converter
- Fully Isolated Multiple Outputs
- Distributed Power Conversion Networks

DESCRIPTION

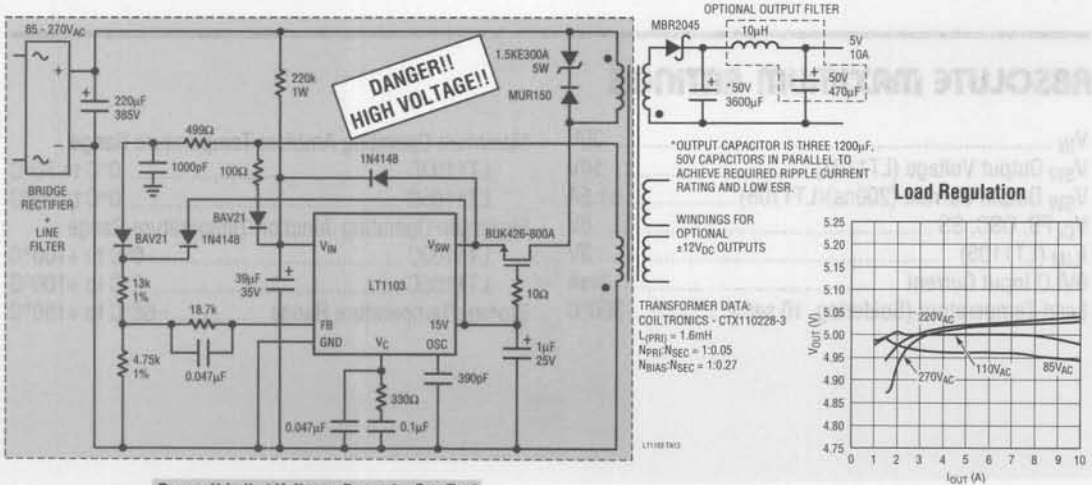
The LT1103 Offline Switching Regulator is designed for high input voltage applications using an external FET switch whose source is driven by the open collector output of the LT1103. The LT1103 is optimized for 15W–100W applications. For higher power applications or additional switch current flexibility, the LT1105 is available and its totem pole output drives the gate of an external FET. Unique design of the LT1103/LT1105 eliminates the need for an opto-coupler while still providing ±1% load and line regulation in a magnetic flux-sensed converter. This significantly simplifies the design of offline power supplies and reduces the number of components which must cross the isolation barrier to one, the transformer.

The LT1103/LT1105 current mode switching techniques are well suited to transformer-isolated flyback and forward topologies while providing ease of frequency compensation with a minimum of external components. Low external part count for a typical application combines with

4

TYPICAL APPLICATION

Fully-Isolated Flyback 100kHz 50W Converter with Load Regulation Compensation



Danger!! Lethal Voltages Present – See Text

DESCRIPTION

a 200kHz maximum switching frequency to achieve high power density. Performance at switching frequencies above 100kHz may be degraded due to internal timing constraints associated with fully-isolated flyback mode.

Included are the oscillator, control, and protection circuitry such as current limit and overvoltage lockout. Switch frequency and maximum duty cycle are adjustable. Bootstrap circuitry draws 200µA for startup of isolated topologies. A 5V reference as well as a 15V gate bias are available to power external primary-side circuitry. No external current sense resistor is necessary with LT1103 because it is integrated with the high current switch. The LT1105 brings out the input to the current limit amplifier and requires the use of an external sense resistor.

The LT1103/LT1105 have unique features not found on other offline switching regulators. Adaptive anti-sat switch drive allows wide-ranging load currents while maintaining high efficiency. The external FET is protected from insufficient or excessive gate drive voltage with a drive detection circuit. An externally activated shutdown mode reduces total supply current to less than 200µA, typical for standby operation. Fully isolated and regulated outputs can be generated in the optional isolated flyback mode without the need for opto-couplers or other isolated feedback paths.

WARNING!

DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS!

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

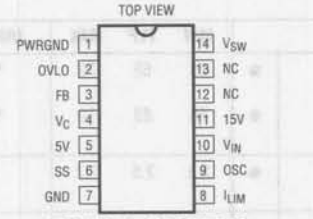
ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

ABSOLUTE MAXIMUM RATINGS

V_{IN} 30V
V_{SW} Output Voltage (LT1103) 50V
V_{SW} Output Current (200ns)(LT1105) ..... ±1.5A
V_C, FB, OSC, SS 6V
I_{LIM} (LT1105) 3V
OVLO Input Current 1mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Maximum Operating Ambient Temperature Range
LT1103C ..... 0°C to 70°C
LT1105C ..... 0°C to 70°C
Maximum Operating Junction Temperature Range
LT1103C ..... 0°C to +100°C
LT1105C ..... 0°C to +100°C
Storage Temperature Range ..... –65°C to +150°C

PACKAGE/ORDER INFORMATION



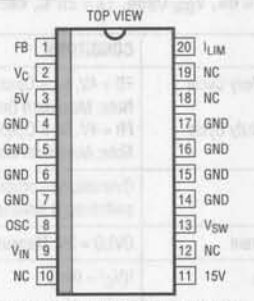
N PACKAGE, 14-LEAD PLASTIC DIP

PINS 1 AND 7 MUST BE TIED TOGETHER

T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1105CN

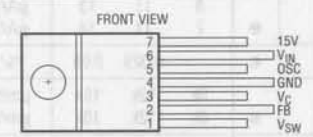


S PACKAGE, 20-LEAD (FUSED) PLASTIC SOL

T_{JMAX} = 100°C, θ_{JA} = 45°C/W

ORDER PART NUMBER

LT1105CS



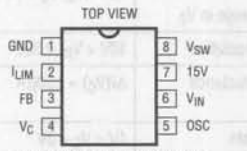
Y PACKAGE
7-LEAD TO-220

CASE IS CONNECTED TO GROUND. LEADS ARE FORMED.

T_{JMAX} = 100°C, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1103CY



N8 PACKAGE, 8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1105CN8

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	8V < V_{IN} < 30V, After device has started	●	10	20	30	mA
I_{START}	Start-Up Current	V_{IN} < V_{IN} Start Threshold	●		200	400	µA
	V_{IN} Start Threshold		●	14.5	16.0	17.5	V
	V_{IN} Shutdown Threshold	Note: Switching stops when V_{SW} < 10V (LT1103) Note: Switching stops when V_{GATE} < 10V (LT1105)	●	5.0	7.0	8.0	V
V_{REF}	5V Reference Voltage		●	4.80	4.95	5.20	V
	V_{REF} Line Regulation	10V < V_{IN} < 30V	●		0.025	0.075	%/V
	V_{REF} Load Regulation	0mA < I_L < 20mA	●		0.025	0.05	%/mA
	V_{REF} Short Circuit Current		●	25	60	110	mA
V_{GATE}	15V Gate Bias Reference	17 < V_{IN} < 30V, 0mA < I_L < 30mA	●	13.8	15.0	16.2	V
	15V Dropout Voltage	V_{IN} = 15V, I_L = 30mA	●		2.0	2.5	V
	15V Short Circuit Current		●	30	70	130	mA
SF	Oscillator Scaling Factor	FB = 4V, V_C = Open, Measured at V_{SW}, I_{SW} = 25mA, OVLO = 5V, F_{OSC} = SF/C_{OSC}, 40kHz < F_{OSC} < 200kHz	●	36 32	40 40	44 48	Hz • µF Hz • µF
	Oscillator Valley Voltage				2.0		V
	Oscillator Peak Voltage				4.5		V

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ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
DC	Preset Max. Switch Duty Cycle (LT1103)	FB = 4V, V_C = Open, F_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle can be altered at OSC pin	●	58	65	72	%
	Preset Max. Switch Duty Cycle (LT1105)	FB = 4V, V_C = Open, F_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle can be altered at OSC pin	●	56	63	70	%
	OVLO Threshold	Overvoltage Lockout Threshold at which switching is inhibited	●	2.3	2.5	2.7	V
	OVLO Input Bias Current	OVLO = 2V, Measured out of pin (Note 1)	●		1.0	3.0	µA
V_{FB}	FB Threshold Voltage	$I(V_C)$ = 0mA	 ●	4.425 4.400	4.50 4.50	4.575 4.600	V V
	FB Input Bias Current	FB = V_{FB} (Note 2)	●	5	10	20	µA
	Change in FB Input Bias Current with Change in V_C	FB = V_{FB}, V_C = 1V to 4V (Note 2)	 ●	8 7	11 11	13 14	µA/V µA/V
	FB Threshold Line Regulation	10V < V_{IN} < 30V	●		0.025	0.05	%/V
gm	Error Amp Transconductance	$\Delta I(V_C)$ = ±50µA	 ●	9k 6k	12k 12k	16k 18k	µmho µmho
A_V	Error Amp Voltage Gain	1V < V_C < 3V	●	500	1250		V/V
	V_C Switching Threshold	Switch Duty Cycle = 0%	●	0.85	1.25	1.4	V
	Shutdown Threshold Voltage		●	50	150	250	mV
	Error Amp Source Current		●	150	275		µA
	Error Amp Sink Current		●	1.5	3	4.5	mA
	Error Amp Clamp Voltage	FB = 4.75V FB = 4.0V	● ●	0.3 4.2	0.7 4.4	0.9 4.6	V V
	Soft-Start Charging Current	SS = 0V	●	25	40	60	µA
	Soft-Start Reset Current	V_{IN} = 6V, SS = 0.3V	●	1	2		mA
	Output Switch Leakage (LT1103)	V_{SW} = 45V V_{SW} = 15V	● ●			500 200	µA µA
BV	Switch Breakdown Voltage (LT1103)	I_{SW} = 5mA	●	50	70		V
	V_{SW} Current Limit (LT1103)	Duty Cycle = 25% (Note 3)	●	2.0	2.5	3.0	A
	Output Switch ON Resistance (LT1103)		●		0.4	0.75	Ω
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	I_Q Increase During Switch ON Time (LT1103)	I_{SW} = 0.5A to 1.5A	●		30	50	mA/A
	Switch Output High Level (LT1105)	I_{SW} =200mA, V_{GATE} = 15V I_{SW} = 750mA, V_{GATE} = 15V	● ●	13.0 12.5	13.5 13.2		V V
	Switch Output Low Level (LT1105)	I_{SW} = 200mA I_{SW} = 750mA	● ●		0.25 0.75	0.50 1.50	V V
	Rise Time (LT1105)	CL = 1000pF			50		ns
	Fall Time (LT1105)	CL = 1000pF			20		ns

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
	I_{LIM} Threshold Voltage (LT1105)	Duty Cycle = 25% (Note 4)	●	300	375	450	mV
	Low Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	9.0	9.5	10.5	V
	High Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	17.0	18.5	20.0	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The OVLO pin is clamped with a 5.5V Zener and can sink a maximum input current of 1mA.

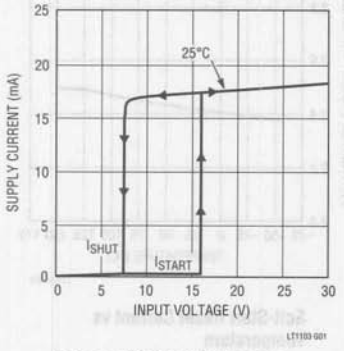
Note 2: FB input bias current changes as a function of the V_C pin voltage. Rate of change of FB input bias current is 11µA/V of change on V_C. By including a resistor in series with the FB pin, load regulation can be set to zero.

Note 3: Current limit on V_{SW} is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuity. The LT1103 switch current limit is given by I_{LIM} = 1.76 (1.536 – DC) above 35% duty cycle.

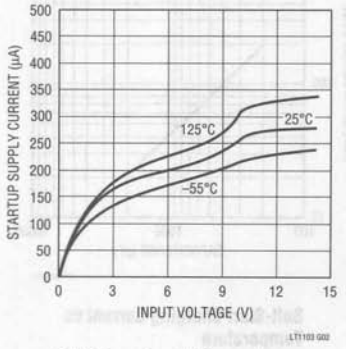
Note 4: The current limit threshold voltage is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuitry. The LT1105 switch current limit threshold voltage is given by V_{LIM} = 0.225 (1.7 – DC) above 35% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

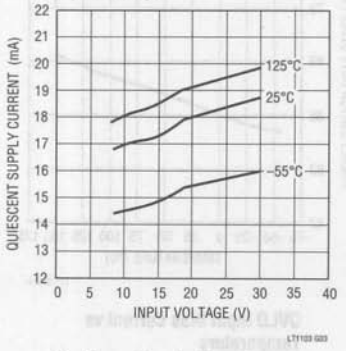
Supply Current vs Input Voltage



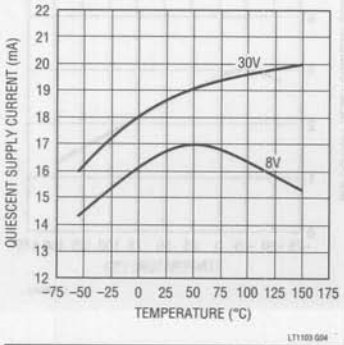
Startup Supply Current vs Input Voltage



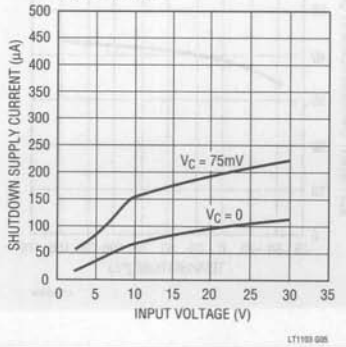
Quiescent Supply Current vs Input Voltage



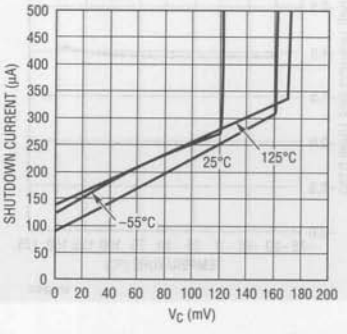
Quiescent Supply Current vs Temperature



Shutdown Supply Current vs Input Voltage

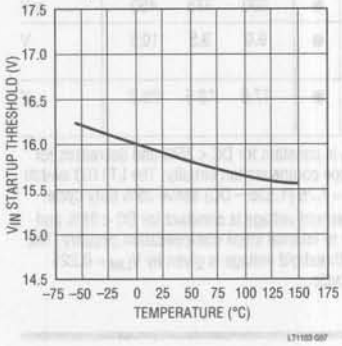


Shutdown Supply Current vs V_C Voltage

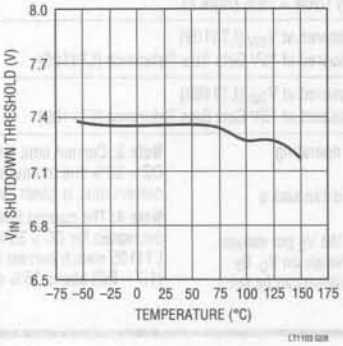


TYPICAL PERFORMANCE CHARACTERISTICS

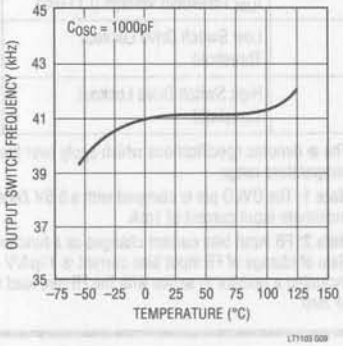
V_{IN} Start-Up Threshold vs Temperature



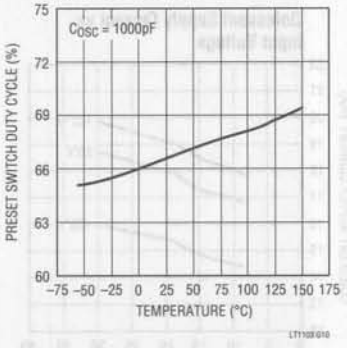
V_{IN} Shutdown Threshold vs Temperature



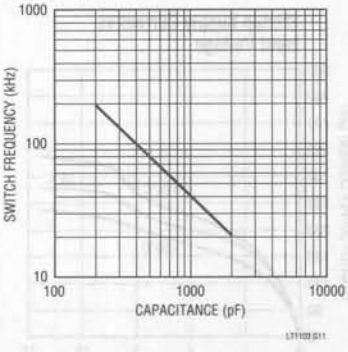
Output Switch Frequency vs Temperature



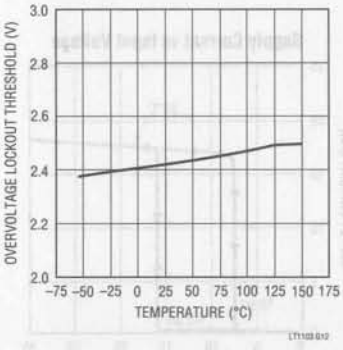
Preset Switch Maximum Duty Cycle vs Temperature



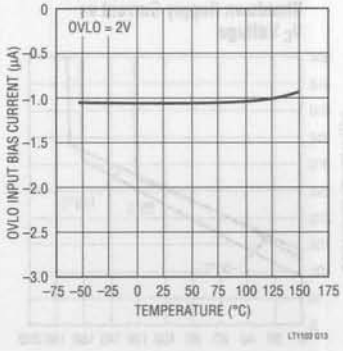
Switch Oscillator Frequency vs Capacitance



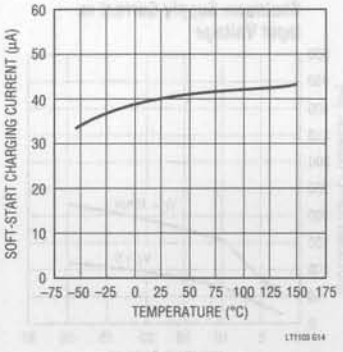
Overvoltage Lockout Threshold vs Temperature



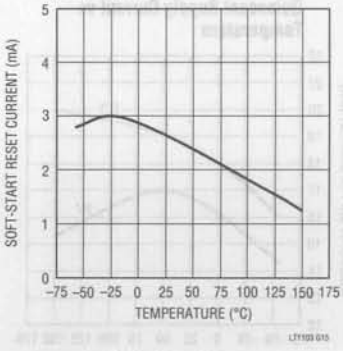
OVLO Input Bias Current vs Temperature



Soft-Start Charging Current vs Temperature

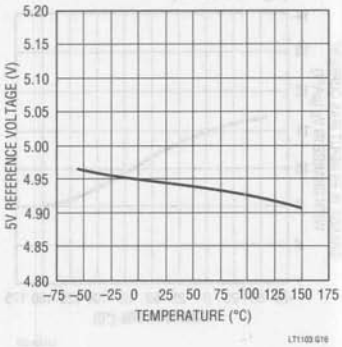


Soft-Start Reset Current vs Temperature

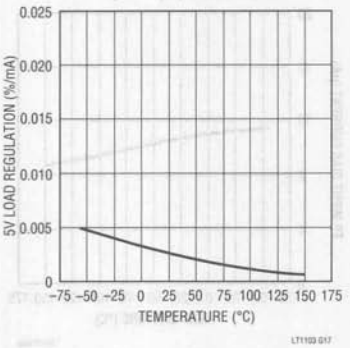


TYPICAL PERFORMANCE CHARACTERISTICS

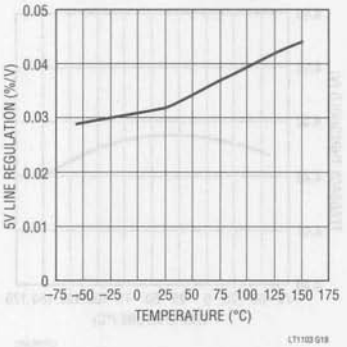
5V Reference Voltage vs Temperature



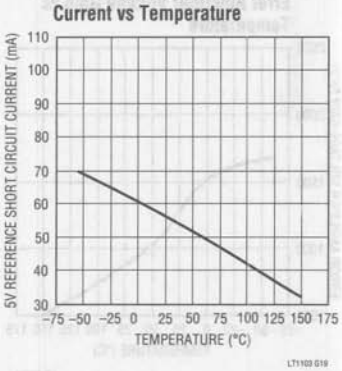
5V Load Regulation vs Temperature



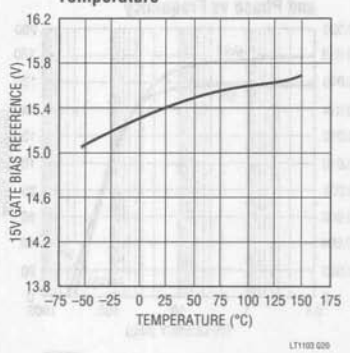
5V Line Regulation vs Temperature



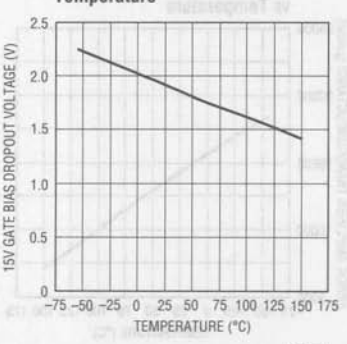
5V Reference Short Circuit Current vs Temperature



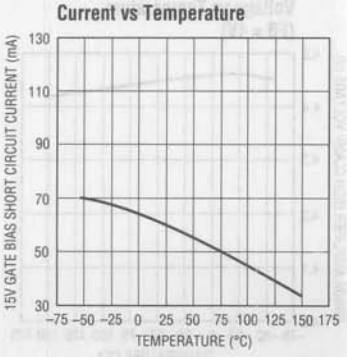
15V Gate Bias Reference vs Temperature



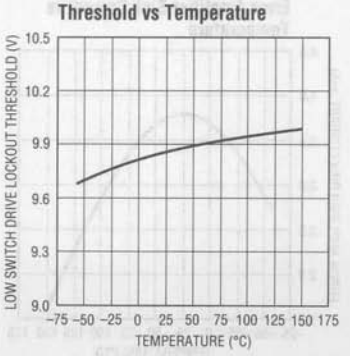
15V Gate Bias Dropout Voltage vs Temperature



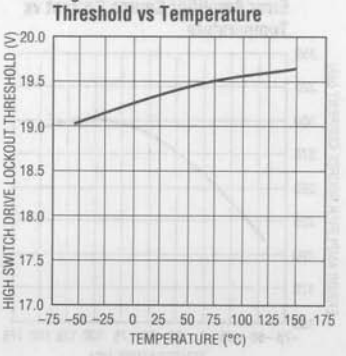
15V Gate Bias Short Circuit Current vs Temperature



Low Switch Drive Lockout Threshold vs Temperature



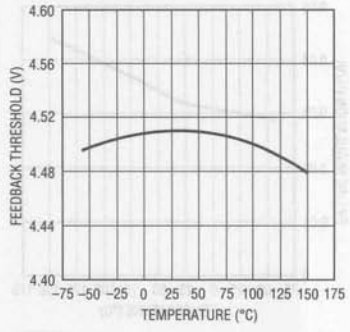
High Switch Drive Lockout Threshold vs Temperature



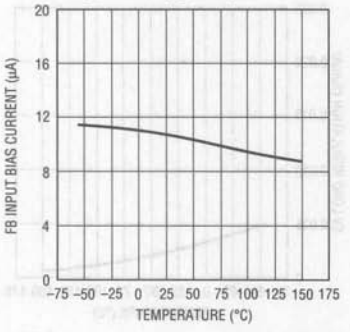
4

TYPICAL PERFORMANCE CHARACTERISTICS

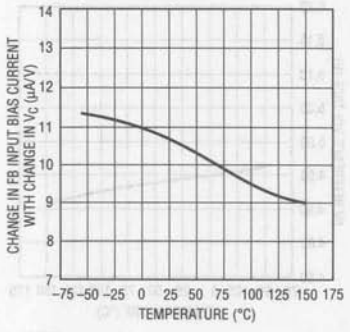
Feedback Threshold vs Temperature



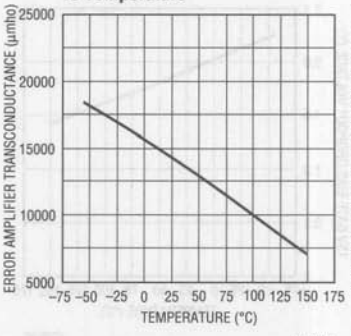
FB Input Bias Current vs Temperature (V_C = 1V)



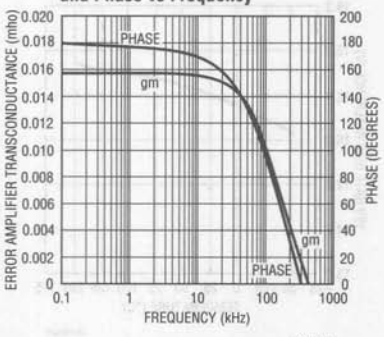
Change in FB Input Bias Current with Change in V_C vs Temperature (V_C = 1V to 4V)



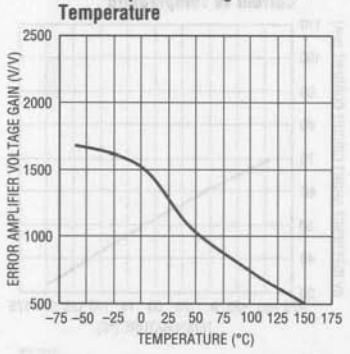
Error Amplifier Transconductance vs Temperature



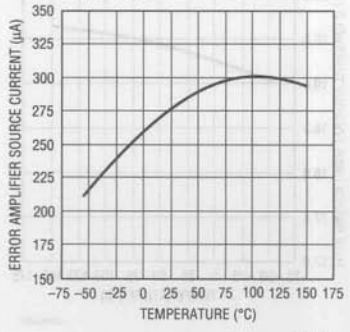
Error Amplifier Transconductance and Phase vs Frequency



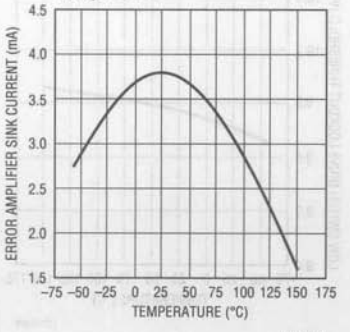
Error Amplifier Voltage Gain vs Temperature



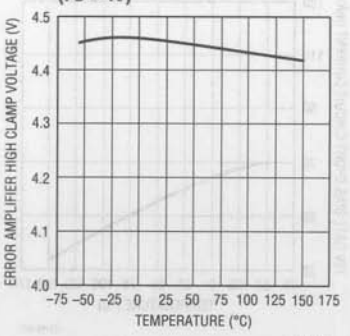
Error Amplifier Source Current vs Temperature



Error Amplifier Sink Current vs Temperature

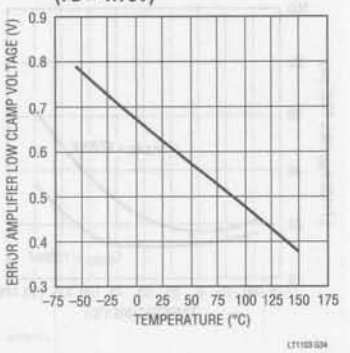


Error Amplifier High Clamp Voltage vs Temperature (FB = 4V)

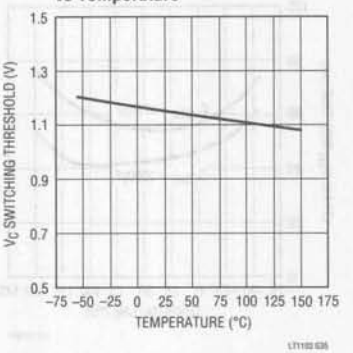


TYPICAL PERFORMANCE CHARACTERISTICS

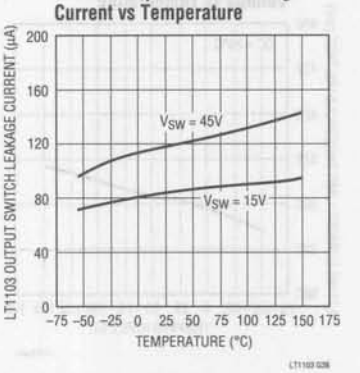
Error Amplifier Low Clamp Voltage vs Temperature (FB = 4.75V)



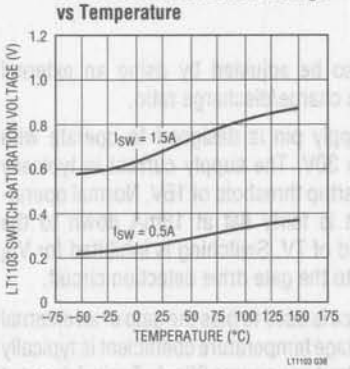
V_C Switching Threshold Voltage vs Temperature



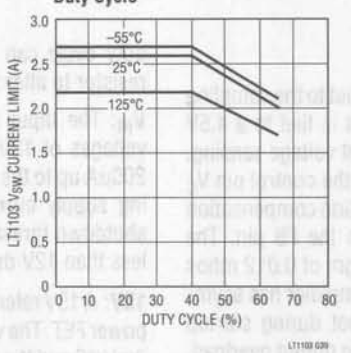
LT1103 Output Switch Leakage Current vs Temperature



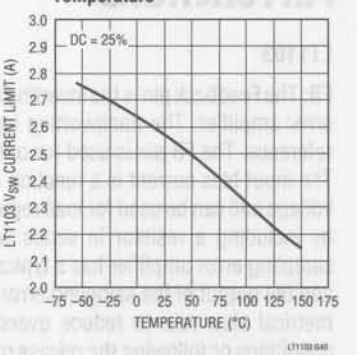
LT1103 Switch Saturation Voltage vs Temperature



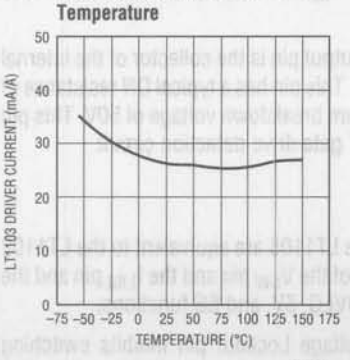
LT1103 V_{SW} Current Limit vs Duty Cycle



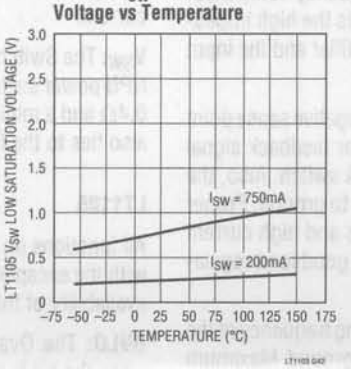
LT1103 V_{SW} Current Limit vs Temperature



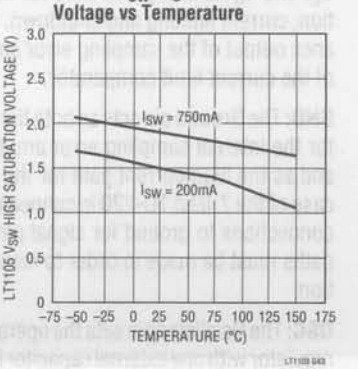
LT1103 Driver Current vs Temperature



LT1105 V_{SW} Low Saturation Voltage vs Temperature



LT1105 V_{SW} High Saturation Voltage vs Temperature



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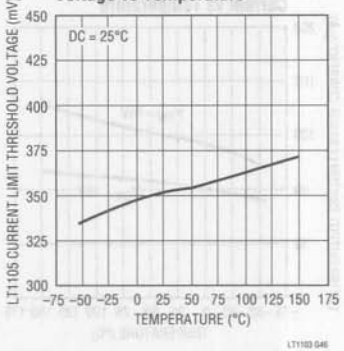
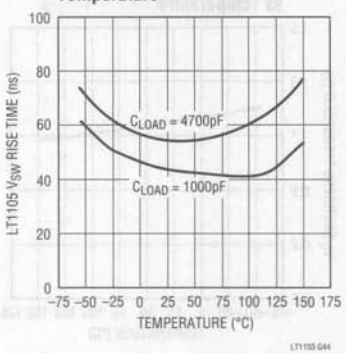
TYPICAL PERFORMANCE CHARACTERISTICS

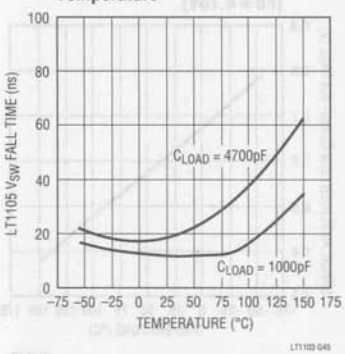
LT1105 Current Limit Threshold Voltage vs Temperature



LT1105 V_{SW} Rise Time vs Temperature



LT1105 V_{SW} Fall Time vs Temperature



PIN FUNCTIONS

LT1103

FB: The Feedback pin is the inverting input to the sampling error amplifier. The noninverting input is tied to a 4.5V reference. The FB pin is used for output voltage sensing. The input bias current is a function of the control pin V_C voltage and can be used for load regulation compensation by including a resistor in series with the FB pin. The sampling error amplifier has a typical gm of 0.012 mhos and the output of the sampling error amplifier has asymmetrical slew rate to reduce overshoot during startup conditions or following the release of an output overload.

V_C: The V_C control pin is used for frequency compensation, current limiting and shutdown. It is the high impedance output of the sampling error amplifier and the input of the current limit comparator.

GND: The Ground pin acts as both the negative sense point for the internal sampling error amplifier feedback signal and as the high current path for the 2A switch. Also, the case of the 7-lead TO-220 is connected to ground. Proper connections to ground for signal paths and high current paths must be made in order to insure good load regulation.

OSC: The Oscillator pin sets the operating frequency of the regulator with one external capacitor to ground. Maximum duty cycle can also be adjusted by using an external resistor to alter the charge/discharge ratio.

V_{IN}: The Input Supply pin is designed to operate with voltages of 12V to 30V. The supply current is typically 200μA up to the startup threshold of 16V. Normal operating supply current is fairly flat at 18mA down to the shutdown threshold of 7V. Switching is inhibited for V_{IN} less than 12V due to the gate drive detection circuit.

15V: A 15V reference is used to bias the gate of an external power FET. The voltage temperature coefficient is typically 3mV/°C and the output can source 30mA. Typical dropout voltage is 1.5V for V_{IN} less than 17V and 30mA of load current.

V_{SW}: The Switch Output pin is the collector of the internal NPN power switch. This pin has a typical ON resistance of 0.4Ω and a minimum breakdown voltage of 50V. This pin also ties to the FET gate drive detection circuit.

LT1105

All functions on the LT1105 are equivalent to the LT1103 with the exception of the V_{SW} pin and the I_{LIM} pin and the availability of the OVLO, 5V, and SS functions.

OVLO: The Overvoltage Lockout pin inhibits switching when the pin is pulled above its threshold voltage of 2.5V.

PIN FUNCTIONS

OVLO is implemented with a resistor divider network from the rectified DC line and is used to protect the external FET from an overvoltage condition in the off state. This function is only available on the 14-lead DIP.

5V: A 5V reference is available to power primary-side circuitry. The temperature coefficient is typically 50ppm/°C and the output can source 25mA. This function is available on the 14-lead DIP and the 20-pin fused SO.

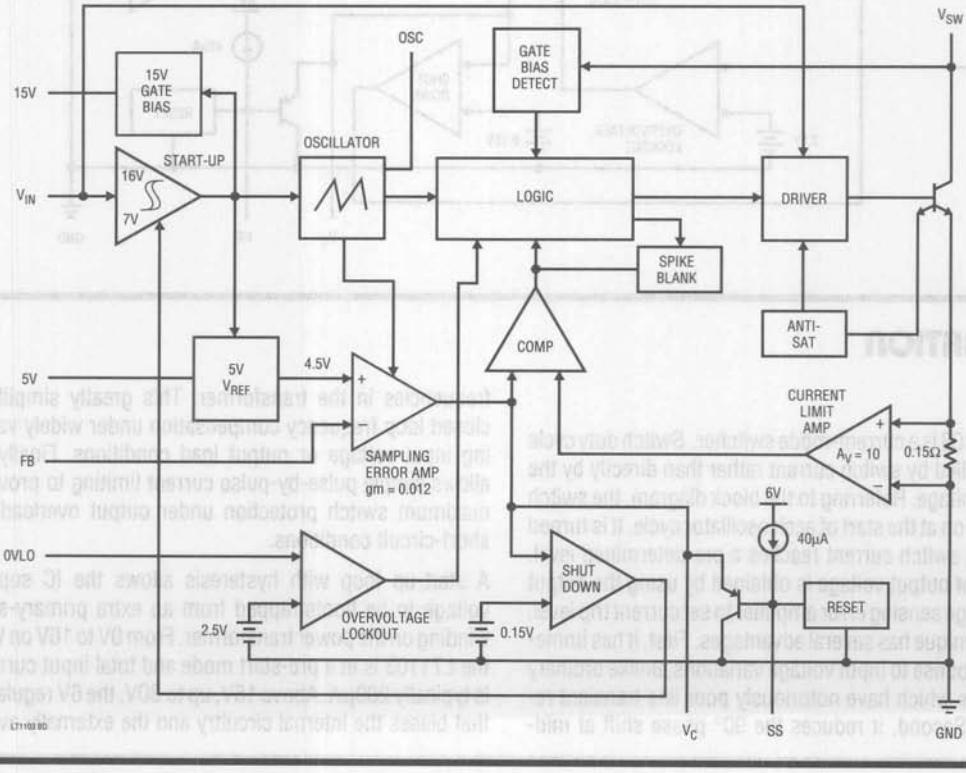
SS: The Soft-start pin is used to either program start-up time with a capacitor to ground or to set external current limit with a resistor divider. The SS pin has a 40µA pullup current and is reset to 0V by a 1mA pulldown current during startup and shutdown. This function is only available on the 14-lead DIP.

V_{SW}: The Switch Output pin is the output of a 1A NPN totem pole stage. The V_{SW} pin turns the external FET on by pulling its gate high. Break-Before-Make action of 200ns on each switch edge is built in to eliminate cross-conduction currents.

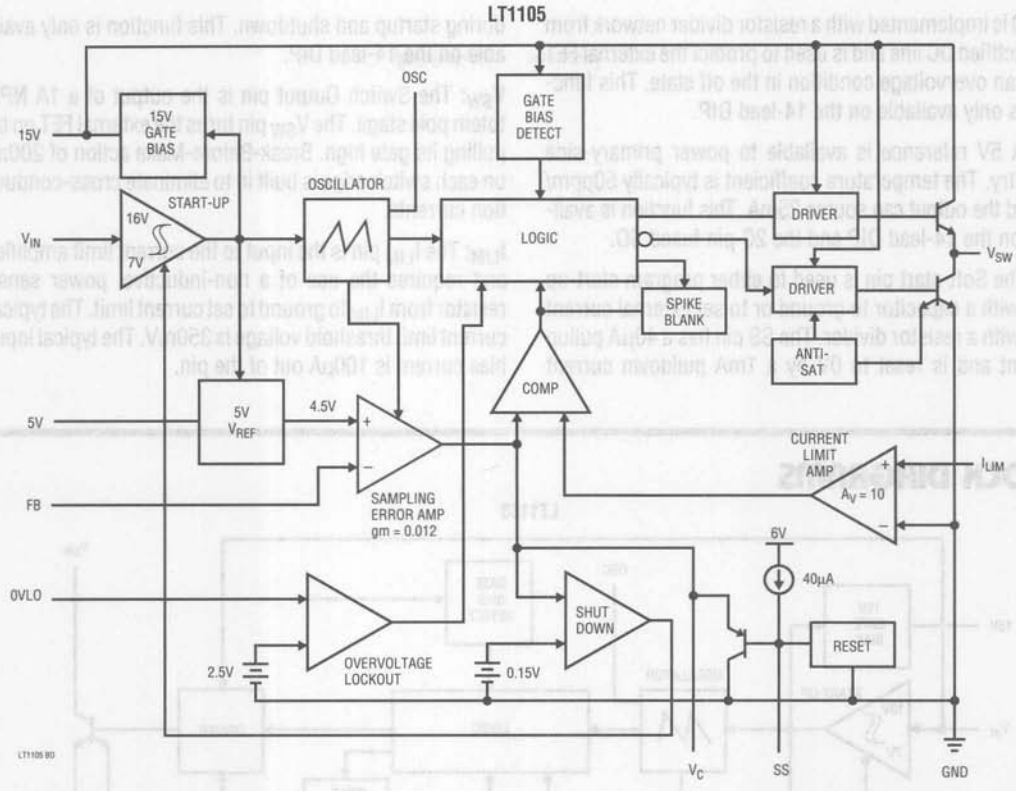
I_{LIM}: The I_{LIM} pin is the input to the current limit amplifier and requires the use of a non-inductive, power sense resistor from I_{LIM} to ground to set current limit. The typical current limit threshold voltage is 350mV. The typical input bias current is 100µA out of the pin.

BLOCK DIAGRAMS

LT1103



BLOCK DIAGRAMS



OPERATION

LT1103

The LT1103 is a current-mode switcher. Switch duty cycle is controlled by switch current rather than directly by the output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a pre-determined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the transformer. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary-side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1103 is in a pre-start mode and total input current is typically 200µA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally avail-

OPERATION

able 15V regulator is turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to the pre-start mode. Output switching stops when the V_{SW} drive is less than 10V corresponding to V_{IN} of about 12V.

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

The LT1103 is designed to drive the source of an external power FET in common-gate configuration. The 15V regulator biases the gate to guarantee the FET is on when the switch is on. Special drive detection circuitry senses the gate bias voltage and prevents the output switch from turning on if the gate voltage is less than 10V or greater than 20V, the industry standards for power MOSFET operation.

The switch current is sensed internally and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

The 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1103 to operate in fully-isolated flyback mode by regulating from the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in a transformer-coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. This V_C pin has three functions including frequency compensation, current limit adjustment, and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (gm) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1103 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1103 in a pre-start mode.

LT1105

The LT1105 is a current-mode switcher. Switch duty cycle is controlled by switch current rather than directly by output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a pre-determined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the transformer. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary-side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1105 is in pre-start mode and total input current is typically 200μA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally available 5V and 15V regulators are turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to pre-start mode. Output switching stops when the 15V gate bias reference is less than 10V corresponding to V_{IN} of about 12V.

OPERATION

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry.

The LT1105 is designed to drive the gate of an external power FET in common-source configuration. The drivers and the 1A maximum totem-pole output stage are biased from the 15V gate bias reference. Special drive detection circuitry senses the gate bias reference voltage and prevents the output switch from turning on if this voltage is less than 10V or greater than 20V. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross conduction currents.

Switch current is sensed externally through a precision, power resistor. This allows for greater flexibility in switch current and output power than allowed by the LT1103. The voltage across the sense resistor is fed into the I_{LIM} pin and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

A 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1105 to operate in fully-isolated flyback mode by regulating the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in the transformer-coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. The V_C pin has three functions including frequency compensation, current limit adjustment, and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (gm) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1105 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1105 in pre-start mode.

The SS pin implements soft-start with one external capacitor to ground. The internal pullup current and clamp transistor limit the voltage at V_C to one diode drop above the voltage at the SS pin, thereby controlling the rate of rise of switch current in the regulator. The SS pin is reset to 0V when the LT1105 is in pre-start mode.

A final protection feature includes overvoltage lockout monitoring of the main supply voltage on the OVLO pin. If the OVLO pin is greater than 2.5V, the output switch is prevented from turning on. This function can be disabled by grounding the OVLO pin.

APPLICATIONS INFORMATION

Bootstrap Start

It is inefficient as well as impractical to power a switching regulator control IC from the rectified DC input as this voltage is several hundred volts. Self-biased switching regulator topologies take advantage of a lower voltage auxiliary winding on the power transformer or inductor to power the regulator, but require a startup cycle to begin regulation.

Start-up circuitry with hysteresis built into the LT1103/LT1105 allows the input voltage to increase from 0V to 16V before the regulator tries to start. During this time the startup current of the switching regulator is typically 200μA and all internal voltage regulators are off. The low quiescent current allows the input voltage to be trickled up with only 500μA of current from the rectified DC line voltage, thereby minimizing power dissipation in the startup resistor. At 16V, the internal voltage regulators are turned

APPLICATIONS INFORMATION

on and switching begins. If enough power feeds back through the auxiliary winding to keep the input voltage to the switching regulator above 12V, then switching continues and a bootstrap start is accomplished. If the input voltage drops below 12V, then the FET drive detection circuit locks out switching. The input voltage continues to fall as the V_{IN} bypass capacitor is discharged by the normal quiescent current of the LT1103/LT1105. Once the input voltage falls below 7V, the internal voltage regulators are turned off and the switching regulator returns to the low startup current state. A continuous "burp start" mode indicates a fault condition or an incomplete power loop.

The trickle current required to bootstrap the regulator input voltage is typically generated with a resistor from the rectified DC input voltage. When combined with the regulator input bypass capacitor, the startup resistor creates a ramp whose slope governs the turn-on time of the regulator as well as the period of the "burp start" mode. The design trade-offs are power dissipated in the trickle resistor, the turn-on time of the regulator, and the hold-up time of the regulator input bypass capacitor. The value of the startup resistor is set by the minimum rectified DC input voltage to guarantee sufficient startup current. The recommended minimum trickle current is 500μA. The power rating of the startup resistor is set by the maximum rectified DC input voltage. A final consideration for the startup resistor is to insure that the maximum voltage rating of the resistor is not exceeded. Typical carbon film resistors have a voltage rating of 250V. The most reliable and economical solution for the startup resistor is generally provided by placing several 0.25W resistor in series.

The LT1103/LT1105 is designed to operate with supply pin voltages up to 30V. However, the auxiliary bias winding should be designed for a typical output voltage of 17V to minimize IC power dissipation and efficiency loss. Allowances must also be made for cross regulation of the bias voltage due to variations in the rectified DC line voltage and output load current.

Soft-Start

Soft-start refers to the controlled increase of switch current from a startup or shutdown state. This allows the power supply to come up to voltage in a controlled manner and charge the output capacitor without activating current limit. In general, soft-start is not required on the LT1105 due to the design of the sampling error amplifier gm stage which generates asymmetrical slew capability on the V_C pin.

This feature exhibits itself as a typical 3mA sink current capability on the V_C pin whereas source current is only 275μA. The low gm of the error amplifier allows small-valued compensation capacitors to be used on V_C. This allows the sink current to slew the compensation capacitor quickly. Therefore, overshoot of the output voltage on startup sequences and recovery from overload or short circuit conditions is prevented. However, if a longer startup period is required, the soft-start function can be used.

Soft-start is implemented with an internal 40μA pullup and a transistor clamp on the V_C pin so that a single external capacitor from SS ground can define the linear ramp function. The voltage at V_C is limited to one V_{BE} above the Soft-start pin (SS). The time to maximum switch current is defined as the capacitance on SS multiplied by the active range in volts of the V_C pin divided by the pullup current:

$$T = \frac{C \bullet (3.2V)}{40\mu A}$$

SS is reset to 0V whenever V_{IN} is less than 7V (pre-start mode) or when shutdown is activated by pulling V_C below 0.15V. The SS pin has a guaranteed reset sink current of 1mA when either the regulator supply voltage V_{IN} falls below 7V or the regulator is placed in shutdown.

Shutdown

The LT1103/LT1105 can be put in a low quiescent current shutdown mode by pulling V_C below 150mV. In the shutdown mode the internal voltage regulators are turned off, SS is reset to 0V and the part draws less than 200μA. To initiate shutdown, about 400μA must be pulled out of V_C until the internal voltage regulators turn off. Then, less than 50μA pulldown current is required to maintain shutdown. The shutdown function has about 60mV of hysteresis on the V_C pin before the part returns to normal

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operation. Soft-start, if used, controls the recovery from shutdown.

5V Reference

A 5V reference output is available for the user's convenience to power primary-side circuitry or to generate a clamp voltage for switch current limiting. The output will source 25mA and the voltage temperature coefficient is typically 50ppm/°C. If bypassing of the 5V reference is required, a 0.1µF is recommended. Values of capacitance greater than 1µF may be susceptible to ringing due to decreased phase margin. In such cases, the capacitive load can be isolated from the reference output with a small series resistor at the expense of load regulation performance.

Overvoltage Lockout

The switching supply and primarily the external power MOSFET can be protected from an extreme surge of the input line voltage with the overvoltage lockout feature implemented on the OVLO pin. If the voltage on OVLO rises above its typical threshold voltage of 2.5V, output switching is inhibited. This feature can be implemented with a resistive divider off of the rectified DC input voltage. This feature is only available on the LT1105 in the 14-lead DIP and must be tied to ground if left unused.

Ground (LT1103)

The ground pin of the LT1103 is important because it acts as the negative sense point for the internal error amplifier feedback signal, the negative sense point for the current limit amplifier and as the high current path for the 2A switch. The tab of the 7-lead TO-220 is internally connected to ground (pin 4).

To avoid degradation of load regulation, the feedback resistor divider string and the reference side of the bias winding should be directly connected to the ground pin on the package. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and low resistance for best performance. The case of the LT1103 package is desirable to use as the high current ground return path as this is a lower resistive and inductive path than that of the actual package pin and will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Ground (LT1105)

The ground pin of the LT1105 is important because it acts as the negative sense point for the internal error amplifier feedback signal and as the negative sense point for the current limit amplifier. The LT1105 8-pin MiniDIP has pin 1 as its ground. The LT1105 14-pin DIP has pin 1 and pin 7 as grounds and must be tied together for proper operation.

To avoid degradation of load regulation, the feedback resistor divider should be directly connected to the package ground pin. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and low resistance for best performance. This will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Oscillator

The oscillator of the LT1103/LT1105 is a linear ramp type powered from the internal 6V bias line. The charging currents and voltage thresholds are generated internally so that only one external capacitor is required to set the frequency. The 150µA pullup current, which is on all the time, sets the preset maximum on-time of the switch and

APPLICATIONS INFORMATION

the 450μA pulldown current which is turned on and off, sets the dead time. The threshold voltages are typically 2V and 4.5V, so for a 400pF capacitor the ramp-up time of the voltage on the OSC pin is 6.67μs and the ramp-down time is 3.3μs, resulting in an operating frequency of 100kHz. Although the oscillator, as well as the rest of the switching regulator, will function at higher frequencies, 200kHz is the practical upper limit that will allow control range for line and load regulation. The lowest operating frequency is limited by the sampling error amplifier to about 10kHz.

The frequency temperature coefficient is typically –80ppm/°C with a good low T.C. capacitor. This means that with a low temperature coefficient capacitor, the temperature coefficient of the currents and the temperature coefficient of the thresholds sum to –80ppm/°C over the commercial temperature range. Bowing in the temperature coefficient of the currents affects the frequency about ±3% at the extremes of the military temperature range. The capacitor type chosen will have a direct effect on the frequency tempco.

Maximum duty cycle is set internally by the pullup and pulldown currents, independent of frequency. It can be adjusted externally by modifying the fixed pullup current with an additional resistor. In practice, one resistor from the OSC pin to the 5V reference or to ground does the job. Note that the capacitor value must change to maintain the same frequency. For example, a 24k resistor from 5V to OSC and a 440pF capacitor from OSC to ground will yield 100kHz with 50% maximum duty cycle. A 56k resistor and a 280pF capacitor from OSC to ground will yield 100 kHz with 80% maximum duty cycle.

The oscillator can be synchronized to an external clock by coupling a sync pulse into the OSC pin. The width of this pulse should be a minimum of 500ns. The oscillator can only be synchronized up in frequency and the synchronizing frequency must be greater than the maximum possible unsynchronized frequency (for the chosen oscillator capacitor value). The amplitude of the sync pulse must be chosen so that the sum of the oscillator voltage amplitude plus the sync pulse amplitude does not exceed the 6V bias reference. Otherwise, the oscillator pullup current source will saturate and erroneous operation will result. If the LT1103/LT1105 is positioned on the primary side of the transformer and the external clock on the isolated secondary output side, the sync signal must be coupled into the OSC pin using a pulse transformer. The pulse transformer must meet all safety/isolation requirements as it also crosses the isolation boundary. An example of externally synchronizing the oscillator is shown in the Typical Applications section.

Gate Biasing (LT1103)

The LT1103 is designed to drive an external power MOSFET in the common-gate or cascode connection with the V_{SW} pin. The advantage is that the switch current can be sensed internally, eliminating a low-value, power sense resistor. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the open-collector source drive is on. This means 10V as specified in FET data sheets, plus 1V for the typical switch saturation voltage, plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed, the gate capacitance must be charged and discharged quickly with high peak currents. In particular, the turn-off current can be as high as the peak switch current. The switching speed is controlled by the impedance seen by the gate capacitance. Practically speaking, zero impedance is not desirable because of the high frequency noise spikes introduced to the system. The gate bias should be bypassed with a 1μF low ESR capacitor to ground and should have a 5Ω resistor or larger in series with the gate to define the source impedance.

The LT1103 provides a 15V output intended for biasing the gate of the MOSFET. It will source 30mA into a capacitive load with no stability problems. The voltage temperature coefficient is +3mV/°C. If V_{IN} drops below 17V, the 15V output follows about 2.0V below V_{IN} until the part shuts down. If the 15V output is pulled above 17.5V, it will sink 5mA.

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A special circuit in the LT1103 senses the voltage at V_{SW} prior to turning on the switch. V_{SW} is tied to the source of the FET and should represent the bias voltage on the gate when the switch is off. When the switch first turns off, the drain flies back until it is clamped by a snubber network. The source also flies high due to parasitic capacitive coupling on the FET and parasitic inductance of the leads. An extra diode from the source to the gate or V_{IN} will provide insurance against fault conditions that might otherwise damage the FET. The diode clamps the source to one diode drop above the gate or V_{IN}, thereby limiting the gate-source reverse bias. Once the energy in the leakage inductance spike is dissipated and the primary is being regulated to its flyback voltage, the diode shuts off. The source is then floating and its voltage will be close to the gate voltage. If the sensed voltage on V_{SW} is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a non-saturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the startup window is 6V if the gate is biased from V_{IN} and to 4V if the gate is biased from the 15V output. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1103)

The V_{SW} pin of the LT1103 is the collector of an internal NPN power switch. This NPN has a typical on resistance of 0.4Ω and a typical breakdown voltage (BV_{CBO}) of 75V. Fast switching times and high efficiency are obtained by using a special driver loop which automatically adapts base drive current to the minimum required to keep the switch in a quasi-saturated state. The key element in the loop is an extra emitter on the output power transistor as seen in the block diagram. This emitter carries no current when the NPN output transistor collector is high (unsaturated). In this condition, the driver circuit can deliver very high base drive to the switch for fast turn-on. When the switch saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. Very low switch current results in nearly zero driver current and high switch currents automatically increase driver current as necessary. The ratio of switch current to driver current is approximately 30:1. This ratio is determined by the sizing of the extra emitter and the value of the current source feeding the driver circuitry. The quasi-saturation state of the switch permits rapid turn-off without the need for reverse base-emitter voltage drive.

Gate Biasing (LT1105)

The LT1105 is designed to drive an external power MOSFET in the common-source configuration with the totem-pole output V_{SW} pin. The advantage is added switch current flexibility (limited only by the choice of external power FET) and higher output power applications than allowed by LT1103. An external, non-inductive, power sense resistor must be used in series with the source of the FET to detect switch current and must be tied to the input of the current limit amplifier. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the totem-pole gate drive is on. This means 10V as specified in FET data sheets, plus the totem-pole high side saturation voltage plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed, the gate capacitance must be charged and discharged quickly with high peak currents. In particular, the turn-off current can be as high as the peak switch current. The switching speed is controlled by the impedance seen by the gate capacitance. Practically speaking, zero impedance is not desirable because of the high frequency noise spikes introduced to the system. The gate bias supply which drives the totem-pole output stage should be bypassed with a 1μF low ESR capacitor to ground. This capacitor supplies the energy to charge the gate capacitance during gate drive turn-on. The power MOSFET should have a 5Ω

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resistor or larger in series with its gate from the V_{SW} pin to define the source impedance.

The LT1105 provides a 15V regulated output intended for driving the totem-pole output stage. It will source 30mA into a capacitive load with no stability problems. The output voltage temperature coefficient is +3mV/°C. If V_{IN} drops below 17V, the 15V output follows about 2.0V below V_{IN} until the part shuts down. If the 15V output is pulled above 17.5V, it will sink 5mA.

A special circuit in the LT1105 senses the voltage at the 15V regulated output prior to turning on the switch. The 15V regulator drives the totem-pole output stage and the V_{SW} pin will pull the gate of the FET very close to the value of the 15V output when V_{SW} turns on. Therefore, the 15V output represents what the gate bias voltage on the FET will be when the FET is turned on. If the sensed voltage on the 15V output is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a non-saturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the startup window is 4V. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1105)

The V_{SW} pin of the LT1105 is the output of a 1A totem-pole driver stage. This output stage turns an external power MOSFET on by pulling its gate high. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross-conduction currents. Fast switching times and high efficiency are obtained by using a low loss output stage and a special driver loop which automatically adapts base drive current to the totem-pole low-side drive. The key element in the loop is an extra emitter on the output pull-down transistor as seen in the block diagram. This emitter carries no current when the low-side transistor collector is high (unsaturated). In this condition, the driver can deliver very high base drive to the output transistor for fast turn-off. When the low-side transistor saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. This results in nearly zero driver current. The quasi-saturation state of the low-side switch permits rapid turn-on of the external FET when V_{SW} pulls high.

Fully-Isolated Flyback Mode

A unique sampling error amplifier included in the control loop of the LT1103/LT1105 eliminates the need for an opto-isolator while providing ±1% line and load regulation in a magnetic flux-sensed flyback converter. In this mode, the flyback voltage on the primary during "switch off" time is sensed and regulated. It is difficult to derive a feedback signal directly from the primary flyback voltage as this voltage is typically several hundred volts. A dedicated winding is not required because the bias winding for the regulator lends itself to flux-sensing. Flux-sensing made practical simplifies the design of offline power supplies by minimizing the total number of external components and reduces the components which must cross the isolation barrier to one, the transformer. This inherently implies greater safety and reliability. The transformer must be optimized for coupling between the bias winding and the secondary output winding(s) while maintaining the required isolation and minimizing the parasitic leakage inductances.

Although magnetic flux-sensing has been used in the past, the technique has exhibited poor output voltage regulation due to the parasitics present in a transformer-coupled design. Transformers which provide the safety and isolation as required by various international safety/regulatory agencies also provide the poorest output voltage regulation. Solutions to these parasitic elements have been achieved with the novel sampling error amplifier of the LT1103/LT1105. A brief review of flyback converter operation and the problems which create a poorly regulated output will provide insight on how the sampling error amplifier of the LT1103/LT1105 addresses the regulation issue of magnetic flux-sensed converters.

The following figure shows a simplified diagram of a flyback converter using magnetic flux-sensing. The major parasitic elements present in the transformer-coupled

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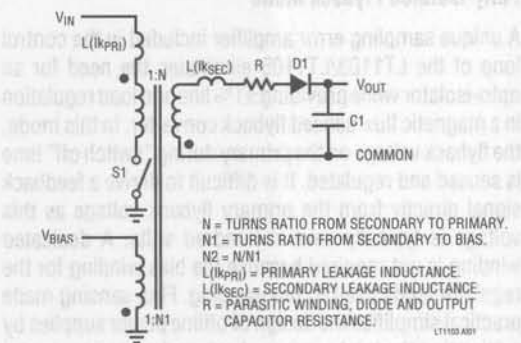
design are indicated. The relationships between the primary voltage, the secondary voltage, the bias voltage and the winding currents are indicated in the figures found on the following page for both continuous and discontinuous modes of operation.

Simplified Flyback Converter



When the switch "turns on," the primary winding sees the input voltage and the secondary and bias windings go to negative voltages as a function of the turns ratio. Current builds in the primary winding as the transformer stores energy. When the switch "turns off," the voltage across the switch flies back to a clamp level as defined by a snubber network until the energy in the leakage inductance of the primary dissipates. Leakage inductance is one of the main parasitic elements in a flux-sensed converter and is modeled as an inductor in series with the primary and secondary of the transformer. These parasitic inductances contribute to changes in the bias winding voltage and thus the output voltage with increasing load current.

The energy stored in the transformer transfers through the secondary and bias windings during "switch off" time. Ideally, the voltage across the bias winding is set by the DC output voltage, the forward voltage of the output diode, and the turns ratio of the transformer after the energy in the leakage inductance spike of the primary is dissipated.

This relationship holds until the energy in the transformer drops to zero (discontinuous mode) or the switch turns on again (continuous mode). Either case results in the voltage across the secondary and bias windings decreasing to zero or changing polarity. Therefore, the voltage on the bias winding is only valid as a representation of the output voltage while the secondary is delivering current.

Although the bias winding flyback voltage is a representation of the output voltage, its voltage is not constant. For a brief period following the leakage inductance spike, the bias winding flyback voltage decreases due to nonlinearities and parasitics present in the transformer. Following this nonlinear behavior is a period where the bias winding flyback voltage decreases linearly. This behavior is easily explained. Current flow in the secondary decreases linearly at a rate determined by the voltage across the secondary and the inductance of the secondary. The parasitic secondary leakage inductance appears as an impedance in series with the secondary winding. In addition, parasitic resistances exist in the secondary winding, the output diode and the output capacitor. These impedances can be combined to form a lumped sum equivalent and which cause a voltage drop as secondary current flows. This voltage drop is coupled from the secondary to the bias winding flyback voltage and becomes more significant as the output is loaded more heavily. This voltage drop is largest at the beginning of "switch off" time and smallest just prior to either all transformer energy being depleted or the switch turning on again.

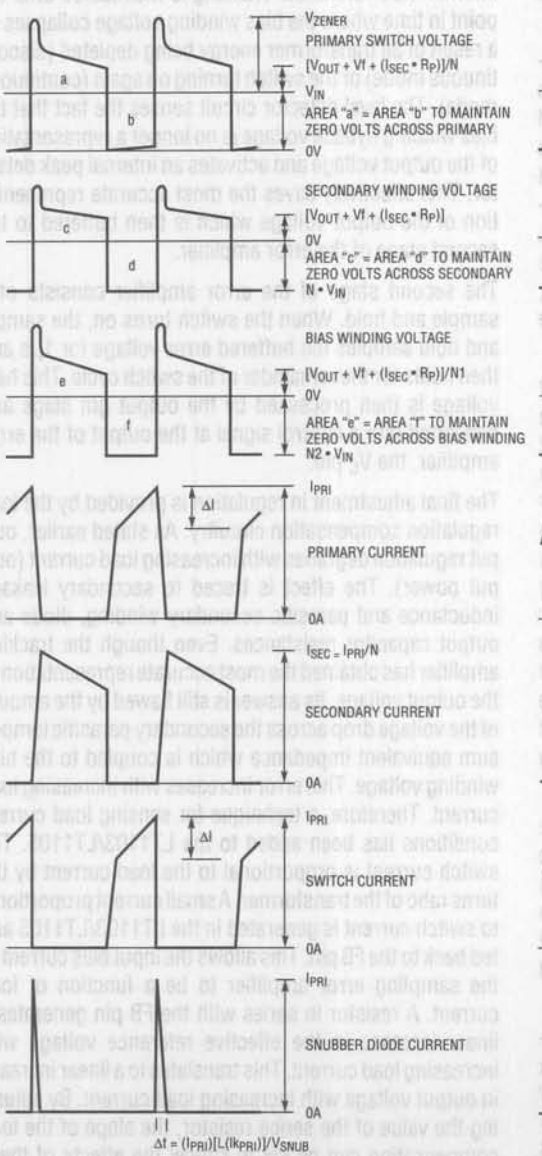
The best representation of the output voltage is just prior to either all transformer energy being used up and the bias winding voltage collapsing to zero or just prior to the switch turning on again and the bias winding going negative. This point in time also represents the smallest forward voltage for the output diode. It is possible to redefine the relationship between the secondary winding voltage and the bias winding voltage as:

$$V_{BIAS} = \frac{\left(V_{OUT} + Vf + I \bullet R_P\right)}{N1}$$

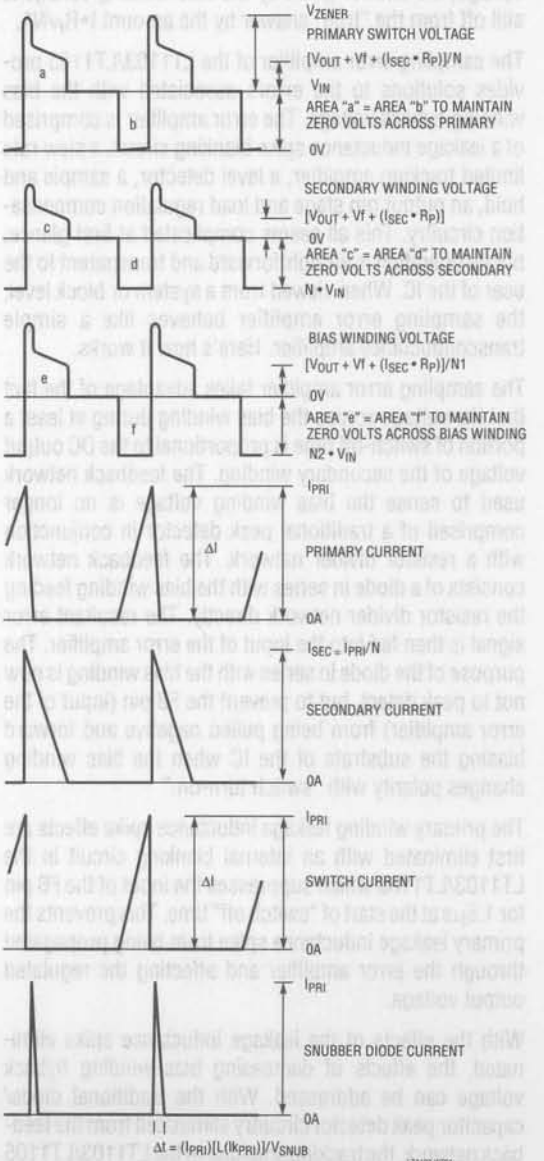
where Vf is the forward voltage of the output diode, I is the current flowing in the secondary, R_P is the lumped sum equivalent secondary parasitic impedance and N1 is thetransformer turns ratio from the secondary to the bias winding. It is apparent that even though the above point in

APPLICATIONS INFORMATION

Flyback Waveform for Continuous Mode Operation



Flyback Waveform for Discontinuous Mode Operation



4

time is the most accurate representation of the output voltage, the answer given by the bias winding voltage is still off from the "true" answer by the amount $I \cdot R_P/N1$.

The sampling error amplifier of the LT1103/LT1105 provides solutions to the errors associated with the bias winding flyback voltage. The error amplifier is comprised of a leakage inductance spike blanking circuit, a slew rate limited tracking amplifier, a level detector, a sample and hold, an output gm stage and load regulation compensation circuitry. This all seems complicated at first glance, but its operation is straightforward and transparent to the user of the IC. When viewed from a system or block level, the sampling error amplifier behaves like a simple transconductance amplifier. Here's how it works.

The sampling error amplifier takes advantage of the fact that the voltage across the bias winding during at least a portion of switch-off time is proportional to the DC output voltage of the secondary winding. The feedback network used to sense the bias winding voltage is no longer comprised of a traditional peak detector in conjunction with a resistor divider network. The feedback network consists of a diode in series with the bias winding feeding the resistor divider network directly. The resultant error signal is then fed into the input of the error amplifier. The purpose of the diode in series with the bias winding is now not to peak detect, but to prevent the FB pin (input of the error amplifier) from being pulled negative and forward biasing the substrate of the IC when the bias winding changes polarity with "switch turn-on."

The primary winding leakage inductance spike effects are first eliminated with an internal blanking circuit in the LT1103/LT1105 which suppresses the input of the FB pin for 1.5μs at the start of "switch off" time. This prevents the primary leakage inductance spike from being propagated through the error amplifier and affecting the regulated output voltage.

With the effects of the leakage inductance spike eliminated, the effects of decreasing bias winding flyback voltage can be addressed. With the traditional diode/capacitor peak detector circuitry eliminated from the feedback network, the tracking amplifier of the LT1103/LT1105 follows the flyback waveform as it changes with time and amplifies the difference between the flyback signal and the internal 4.5V reference. Tracking is maintained until the point in time where the bias winding voltage collapses as a result of all transformer energy being depleted (discontinuous mode) or the switch turning on again (continuous mode). The level detector circuit senses the fact that the bias winding flyback voltage is no longer a representation of the output voltage and activates an internal peak detector. This effectively saves the most accurate representation of the output voltage which is then buffered to the second stage of the error amplifier.

The second stage of the error amplifier consists of a sample and hold. When the switch turns on, the sample and hold samples the buffered error voltage for 1μs and then holds for the remainder of the switch cycle. This held voltage is then processed by the output gm stage and converted into a control signal at the output of the error amplifier, the V_C pin.

The final adjustment in regulation is provided by the load regulation compensation circuitry. As stated earlier, output regulation degrades with increasing load current (output power). The effect is traced to secondary leakage inductance and parasitic secondary winding, diode and output capacitor resistances. Even though the tracking amplifier has obtained the most accurate representation of the output voltage, its answer is still flawed by the amount of the voltage drop across the secondary parasitic lumped sum equivalent impedance which is coupled to the bias winding voltage. This error increases with increasing load current. Therefore, a technique for sensing load current conditions has been added to the LT1103/LT1105. The switch current is proportional to the load current by the turns ratio of the transformer. A small current proportional to switch current is generated in the LT1103/LT1105 and fed back to the FB pin. This allows the input bias current of the sampling error amplifier to be a function of load current. A resistor in series with the FB pin generates a linear increase in the effective reference voltage with increasing load current. This translates to a linear increase in output voltage with increasing load current. By adjusting the value of the series resistor, the slope of the load compensation can be set to cancel the effects of these parasitic voltage drops. The feature can be ignored by

APPLICATIONS INFORMATION

eliminating the series resistor and lowering the equivalent divider impedance to swamp out the effects of the input bias current.

Frequency Compensation

In order to prevent a regulator loop using the LT1103/LT1105 from oscillating, frequency compensation is required. Although the architecture of the LT1103/LT1105 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complication of input/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical approach. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1103/LT1105 is to use transient response techniques and an "R-C" box to quickly iterate toward the final compensation network. Additional information on this technique of frequency compensation can be found in Linear Technology's Application Note 19.

In general, frequency compensation is accomplished with an R-C series network on the V_C pin. The error amplifier has a Gm (voltage "in" to current "out") of ≈ 12000 μmhos. Voltage gain is determined by multiplying Gm times the total equivalent error amplifier output loading, consisting of the error amplifier output impedance in parallel with the series R-C external frequency compensation network. At DC, the external R-C can be ignored. The output impedance of the error amplifier is typically 100kΩ resulting in a voltage gain of ≈ 1200. At frequencies just above DC, the voltage gain is determined by the external compensation, R_C and C_C. The gain at mid frequencies is given by:

$$A_V = \frac{Gm}{2\pi \bullet f \bullet C_C}$$

The gain at high frequencies is given by:

$$A_V = Gm \bullet R_C$$

Phase shift from the FB pin to the V_C pin is 90° at mid frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. Thus, this R-C series network forms a pole-zero pair. The pole is set by the high impedance output of the error amplifier and the value of C_C on the V_C pin. The zero is formed by the value of C_C and the value of R_C in series with C_C on the V_C pin. The R-C series network will have capacitor values in the range of 0.1μF – 1.0μF and series resistor values in the range of 100Ω – 1000Ω.

It is noted that the R-C network on the V_C pin forms the main compensation network for the regulator loop. However, if the load regulation compensation feature is used as explained in the section on fully-isolated flyback mode, additional frequency compensation components are required. The load regulation compensation feature involves the use of local positive feedback from the V_C pin to the FB pin. Thus, it is possible to add enough load regulation compensation to make the loop oscillate. In order to prevent oscillation, it is necessary to roll off this local positive feedback at high frequencies. This is accomplished by placing a capacitor in parallel with the compensation resistor which is in series with the FB pin. A value for this capacitor in the range of 0.01μF to 0.1μF is recommended. The time constant associated with this R/C combination will be longer than that associated with the loop bandwidth. Thus, transient response will be affected in that settling time will be increased. However, this is typically not as important as controlling the absolute under or overshoot amplitude of the system in response to load current changes which could cause deleterious system operation.

Switching Regulator Topologies

Two basic switching regulator topologies are pertinent to the LT1103/LT1105, the flyback and forward converter. The flyback converter employs a transformer to convert one voltage to either a higher or lower output voltage. V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet \frac{DC}{(1-DC)}$$

APPLICATIONS INFORMATION

where N is the transformer turns ratio of secondary to primary and DC is the duty cycle. This formula can be rewritten in terms of duty cycle as:

$$DC = \frac{V_{OUT}}{\left(V_{OUT} + N \bullet V_{IN}\right)}$$

It is important to define the full range of input voltage, the range of output loading conditions and the regulation requirements for a design. Duty cycle should be calculated for both minimum and maximum input voltage.

In many applications, N can vary over a wide range without degrading performance. If maximum output power is desired, N can be optimized:

$$N_{(OPT)} = \frac{V_{OUT} + Vf}{\left(V_M - V_{IN(MAX)} - V_{SNUB}\right)}$$

where Vf = Forward voltage of the output diode
V_M = Maximum switch voltage
V_{SNUB} = Snubber clamp level – primary flyback voltage.

In the isolated flyback mode, the LT1103/LT1105 sense and regulate the transformer primary voltage V_{PRI} during "switch off" time. The secondary output voltage will be regulated if V_{PRI} is regulated. V_{PRI} is related to V_{OUT} by:

$$V_{PRI} = \frac{\left(V_{OUT} + Vf\right)}{N}$$

This allows duty cycle for an isolated flyback converter to be rewritten as:

$$DC = \text{Duty Cycle} = \frac{V_{PRI}}{\left(V_{PRI} + V_{IN}\right)}$$

An important transformer parameter to be determined is the primary inductance L_{PRI}. The value of this inductance is a trade-off between core size, regulation requirements, leakage inductance effects and magnetizing current ΔI. Magnetizing current is the difference between the primary current at the start of "switch on" time and the current at the end of "switch on" time. If maximum output power is needed, a reasonable starting value is found by assigning ΔI a value of 20% of the peak switch current (2A for the LT1103 and set by the external FET rating used with the LT1105). With this design approach, L_{PRI} is defined as:

$$L_{PRI} = \frac{V_{IN}}{(\Delta I)(f)\left(1 + \frac{V_{IN}}{V_{PRI}}\right)}$$

If maximum output power is not required, then ΔI can be increased which results in lower primary inductance and smaller magnetics. Maximum output power with an isolated flyback converter is defined by the primary flyback voltage and the peak allowed switch current and is limited to:

$$P_{OUT(MAX)} = \frac{(V_{PRI})}{(V_{PRI} + V_{IN})}\left[V_{IN}\left(I_P - \frac{\Delta I}{2}\right) - (Ip)^2 R\right]E$$

where R = Total "switch" ON resistance
I_P = Maximum switch current
E = Overall efficiency ≈ 75%

Peak primary current is used to determine core size for the transformer and is found from:

$$I_{PRI} = \frac{(V_{OUT})(I_{OUT})(V_{PRI} + V_{IN})}{E(V_{PRI})(V_{IN})} + \frac{\Delta I}{2}$$

A second consideration on primary inductance is the transition point from continuous mode to discontinuous mode. At light loads, the flyback pulse across the primary will drop to zero before the end of switch "off" time. The load current at which this starts to occur can be calculated from:

$$I_{OUT(TRANSITION)} = \frac{(V_{PRI} \bullet V_{IN})^2}{(V_{PRI} + V_{IN})^2 (2V_{OUT})(f)(L_{PRI})}$$

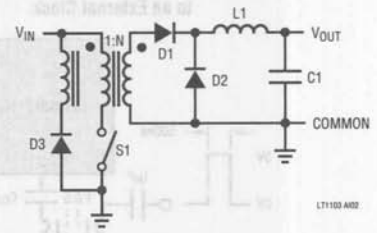
The forward converter as shown below is another transformer-based topology that converts one voltage to either a higher or a lower voltage.

V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet DC$$

APPLICATIONS INFORMATION

Simplified Forward Converter



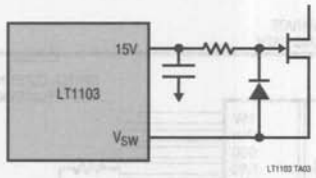
The secondary voltage charges up L1 through D1 when S1 is on. When S1 is off, energy in L1 is transferred through free-wheeling diode D2 to C1. The extra transformer winding and diode D3 are needed in a single switch forward converter to define the switch voltage when S1 is off. This "reset" winding limits the maximum duty cycle allowed for the switch. This topology trades off reduced transformer size for increased complexity and parts count. A separate isolated feedback path is required for full isolation from input to output because voltages on the primary are no longer related to the DC output voltage during switch off time.

The isolated feedback path can take several forms. A second transformer in a modulator/demodulator scheme provides the isolation, but with significant complexity. An opto-isolator can be substituted for the transformer with a savings in volume to be traded off with component variations and possible aging problems with the opto-isolator transfer function. Finally, an extra winding closely coupled to the output inductor L1 can sense the flux in this element and give a representation of the output voltage when S1 is off.

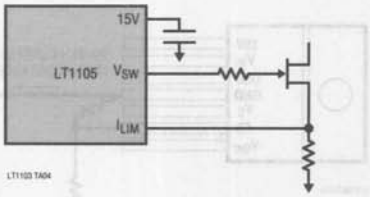
4

TYPICAL APPLICATIONS

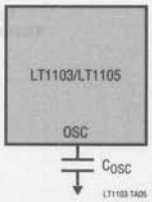
LT1103 FET Connection



LT1105 FET Connection



Setting Oscillator Frequency

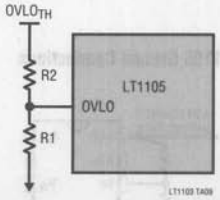


CHOOSE $20kHz \le F_{OSC} \le 200kHz$

$$C_{OSC} = \frac{SF}{F_{OSC}} = \frac{I}{(\Delta V)(F_{OSC})} = \frac{100\mu A}{(2.5V)(F_{OSC})}$$

$DC \equiv 0.66 \Rightarrow 66\%$

Setting Overvoltage Lockout



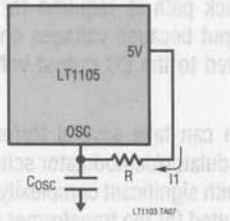
CHOOSE $OVLO_{TH}$

LET R1 = 5k

$$R2 = \left(\frac{OVLO_{TH}}{2.5V} - 1\right) R1$$

TYPICAL APPLICATIONS

Decreasing Oscillator Maximum Duty Cycle



CHOOSE $0 \le DC \le 0.66$

SOLVE FOR $X \Rightarrow X = \dfrac{(6 - 9DC)}{2}$

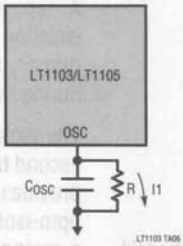
$0 \le X \le 3$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

$\Rightarrow R = \dfrac{1.75V}{I1}$

$C_{OSC} = \dfrac{100\mu A}{(2.5V)(F_{OSC})} \bullet \left[1 + \dfrac{(3X - 2X^2)}{9}\right]$

Increasing Oscillator Maximum Duty Cycle



CHOOSE $0.66 \le DC \le 1.0$

SOLVE FOR $X \Rightarrow X = \dfrac{(9DC - 6)}{2}$

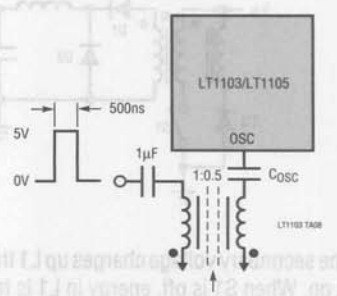
$0 \le X \le 1.5$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

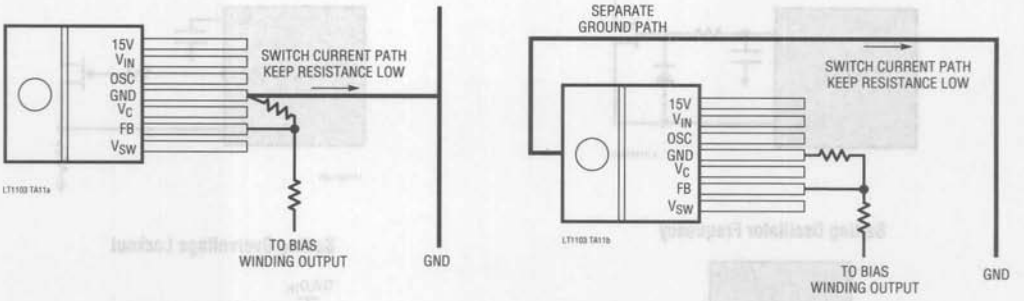
$\Rightarrow R = \dfrac{3.25V}{I1}$

$C_{OSC} = \dfrac{100\mu A}{(2.5V)(F_{OSC})} \bullet \left[1 - \dfrac{(3X + 2X^2)}{9}\right]$

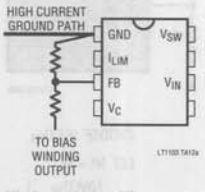
Synchronizing Oscillator Frequency to an External Clock



LT1103 Ground Connections

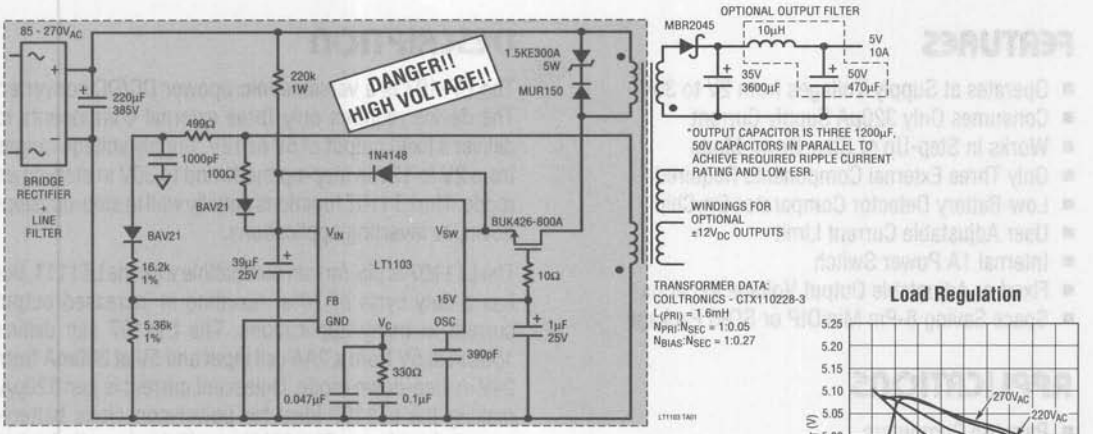


1105 Ground Connections



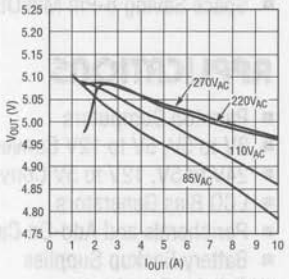
TYPICAL APPLICATIONS

Minimum Parts Count Fully-Isolated Flyback 100kHz 50W Converter



Danger!! Lethal Voltages Present – See Text

Load Regulation



4

LINEAR TECHNOLOGY

LT1107

Micropower DC/DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages from 2V to 30V
- Consumes Only 320µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Three External Components Required
- Low-Battery Detector Comparator On-Chip
- User Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or SO-8 Package

APPLICATIONS

- Palmtop Computers
- 3V to 5V, 5V to 12V Converters
- 24V to 5V, 12V to 5V Converters
- LCD Bias Generators
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Cellular Telephones
- Portable Instruments

DESCRIPTION

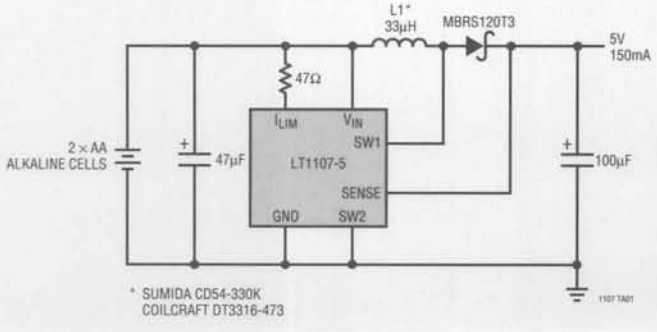
The LT1107 is a versatile micropower DC/DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2V to 12V in step-up mode and to 30V in step-down mode. The LT1107 functions equally well in step-up, step-down, or inverting applications.

The LT1107 is pin-for-pin compatible with the LT1111, but has a duty cycle of 70%, resulting in increased output current in many applications. The LT1107 can deliver 150mA at 5V from a 2AA cell input and 5V at 300mA from 24V in step-down mode. Quiescent current is just 320µA, making the LT1107 ideal for power-conscious battery-operated systems. The 63kHz oscillator is optimized to work with surface mount inductors and capacitors.

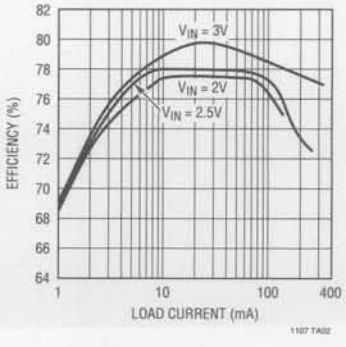
Switch current limit can be programmed with a single resistor. An auxiliary gain block can be configured as a low-battery detector, linear post regulator, undervoltage lock-out circuit, or error amplifier.

TYPICAL APPLICATION

Palmtop Computer Logic Supply



Efficiency

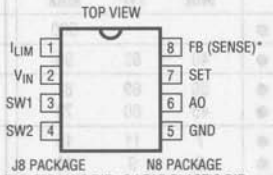


LINEAR TECHNOLOGY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 36V
SW1 Pin Voltage (V_{SW1}) 50V
SW2 Pin Voltage (V_{SW2}) ..... −0.5V to V_{IN}
Feedback Pin Voltage (LT1107) 5V
Sense Pin Voltage (LT1107-5, LT1107-12) 36V
Maximum Power Dissipation 500mW
Set Pin Voltage 5.5V
Maximum Switch Current 1.5A
Operating Temperature Range
LT1107C ..... 0°C to 70°C
LT1107M ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



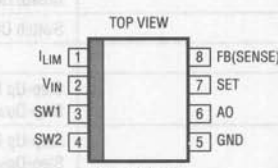
J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

* FIXED VERSIONS

T_{JMAX} = 150°C, θ_{JA} = 120°C/W (J)
T_{JMAX} = 90°C, θ_{JA} = 130°C/W (N)

ORDER PART NUMBER

LT1107CN8
LT1107CN8-5
LT1107CN8-12
LT1107MJ8
LT1107MJ8-5
LT1107MJ8-12



S8 PACKAGE
8-LEAD PLASTIC SO

*FIXED VERSIONS

T_{JMAX} = 90°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1107CS8
LT1107CS8-5
LT1107CS8-12

S8 PART MARKING

1107
11075
110712

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3V, military or commercial version, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch OFF				320	450	µA
	Quiescent Current, Step-Up Mode Configuration	No Load	LT1107-5			360		µA
			LT1107-12			550		µA
V_{IN}	Input Voltage	Step-Up Mode		●	2		12.6	V
		Step-Down Mode		●			30.0	V
	Comparator Trip Point Voltage	LT1107 (Note 1)		●	1.2	1.25	1.3	V
V_{OUT}	Output Sense Voltage	LT1107-5 (Note 2)		●	4.75	5	5.25	V
		LT1107-12 (Note 2)		●	11.40	12	12.60	V
	Comparator Hysteresis	LT1107		●		8	12.5	mV
	Output Hysteresis	LT1107-5		●		32	50	mV
		LT1107-12		●		75	120	mV
f_{OSC}	Oscillator Frequency				50	63	77	kHz
	Duty Cycle, Step-Up Mode	Full Load			64	70	76	%
t_{ON}	Switch ON Time, Step-Up Mode	I_{LIM} Tied to V_{IN}			8.8	11	12.7	µs
	Feedback Pin Bias Current	LT1107, V_{FB} = 0V		●		70	120	nA
	Set Pin Bias Current	V_{SET} = V_{REF}		●		70	300	nA
V_{OL}	Gain Block Output Low	I_{SINK} = 300µA, V_{SET} = 1V		●		0.15	0.4	V
	Reference Line Regulation	5V ≤ V_{IN} ≤ 30V		●		0.02	0.075	%/V

ELECTRICAL CHARACTERISTICS

V_{IN} = 3V, military or commercial version, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_V	Gain Block Gain	R_L = 100k (Note 3)	●	1000	6000		V/V
	Current Limit	220Ω to I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coefficient		●		−0.3		%/°C
	Switch OFF Leakage Current	Measured at SW1 Pin, V_{SW1} = 12V			1	10	µA
V_{SW2}	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch OFF			−400	−350	mV

V_{IN} = 3V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1107M MIN	LT1107M TYP	LT1107M MAX	UNITS
I_Q	Quiescent Current	Switch OFF	●			500	µA
f_{OSC}	Oscillator Frequency		●	40	63	95	kHz
DC	Duty Cycle	Step-Up Mode	●	56	69	81	%
		Step-Down Mode, V_{IN} = 12V	●	45	60	73	%
t_{ON}	Switch ON Time	Step-Up Mode	●	7	11	15	µs
		Step-Down Mode, V_{IN} = 12V	●	5	9	13	µs
	Reference Line Regulation	2V ≤ V_{IN} ≤ 5V, 0°C ≤ T_A ≤ 125°C			0.2	0.4	%/V
		2.4V ≤ V_{IN} ≤ 5V, T_A = −55°C				0.8	%/V
V_{SAT}	Switch Saturation Voltage, Step-Up Mode	0°C ≤ T_A ≤ 125°C, I_{SW} = 500mA			0.5	0.65	V
		T_A = −55°C, I_{SW} = 400mA			0.5	0.65	V
	Switch Saturation Voltage, Step-Down Mode	V_{IN} = 12V, I_{SW} = 500mA					
		0°C ≤ T_A ≤ 125°C				1.5	V
		T_A = −55°C				2.0	V

V_{IN} = 3V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1107C MIN	LT1107C TYP	LT1107C MAX	UNITS
I_Q	Quiescent Current	Switch OFF	●			450	µA
f_{OSC}	Oscillator Frequency		●	50	63	88	kHz
DC	Duty Cycle	Step-Up Mode	●	62	69	78	%
		Step-Down Mode, V_{IN} = 12V	●	50	60	70	%
t_{ON}	Switch ON Time	Step-Up Mode	●	8	11	13.5	µs
		Step-Down Mode, V_{IN} = 12V	●	6	9	12.0	µs
	Reference Line Regulation	2V ≤ V_{IN} ≤ 5V	●		0.2	0.7	%/V
V_{SAT}	Switch Saturation Voltage, Step-Up Mode	V_{IN} = 3V, I_{SW} = 650mA	●		0.5	0.65	V
	Switch Saturation Voltage, Step-Down Mode	V_{IN} = 12V, I_{SW} = 650mA	●		1.1	1.5	V

The ● denotes specifications which apply over the full operating temperature range.

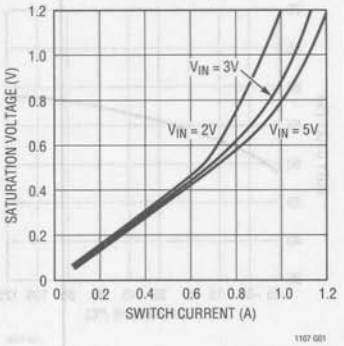
Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.2V to 1.3V range.

Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed-output versions will always be within the specified range.

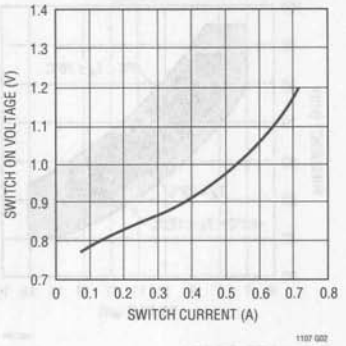
Note 3: 100k resistor connected between a 5V source and the AO pin.

TYPICAL PERFORMANCE CHARACTERISTICS

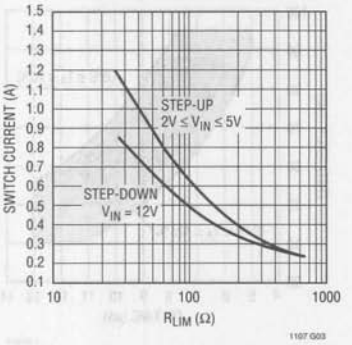
Saturation Voltage, Step-Up Mode (SW2 Pin Grounded)



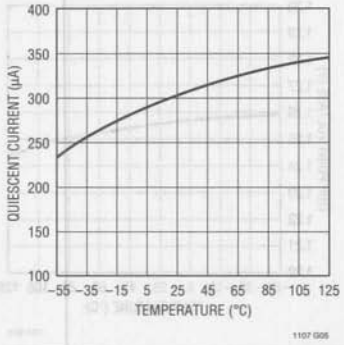
Switch ON Voltage, Step-Down Mode (SW1 Pin Connected to V_{IN})



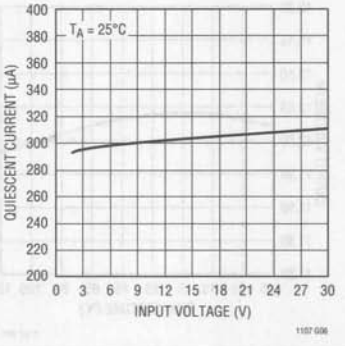
Maximum Switch Current vs R_{LIM}



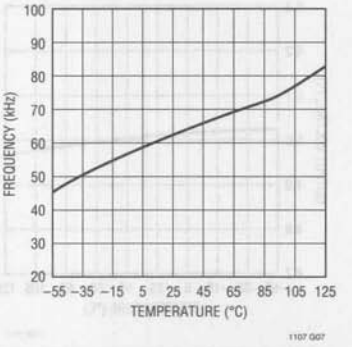
Quiescent Current



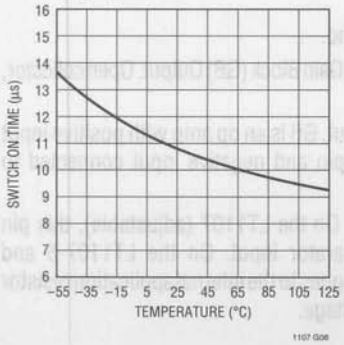
Quiescent Current



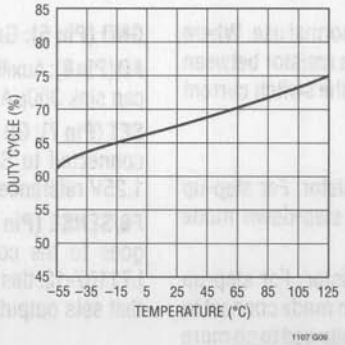
Oscillator Frequency



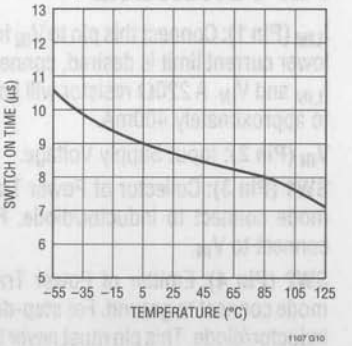
Switch ON Time Step-Up Mode



Duty Cycle Step-Up Mode



Switch ON Time Step-Down Mode



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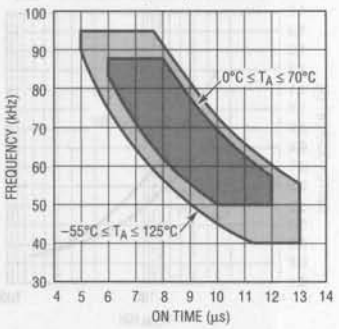
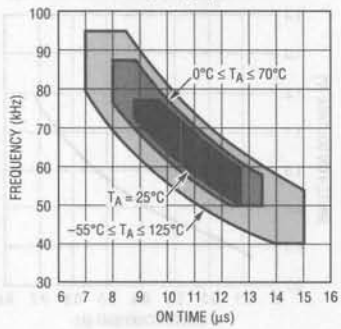
TYPICAL PERFORMANCE CHARACTERISTICS

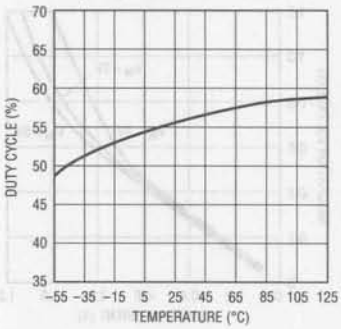
Minimum/Maximum Frequency vs ON Time, Step-Down Mode



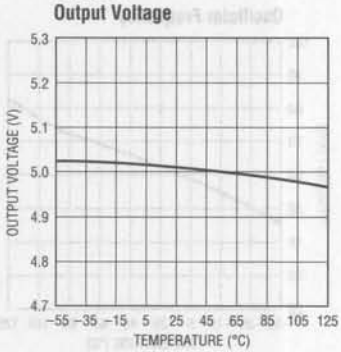
Minimum/Maximum Frequency vs ON Time, Step-Up Mode



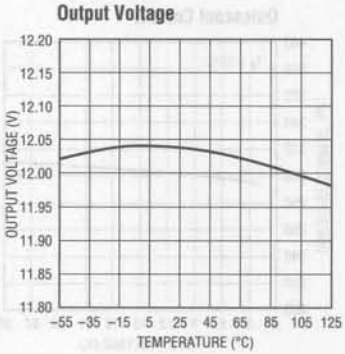
Duty Cycle Step-Down Mode



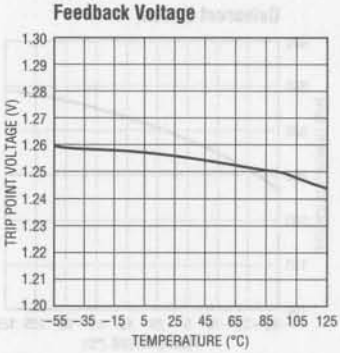
LT1107-5 Output Voltage



LT1107-12 Output Voltage



LT1107 Feedback Voltage



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input Supply Voltage.

SW1 (Pin 3): Collector of Power Transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of Power Transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

GND (Pin 5): Ground.

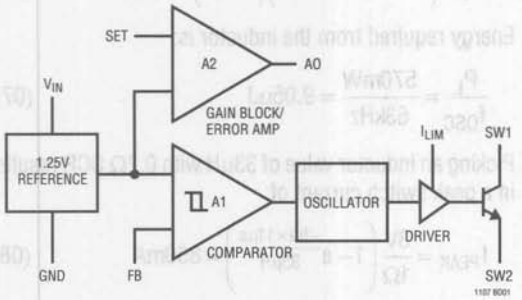
AO (Pin 6): Auxiliary Gain Block (GB) Output. Open collector, can sink 300µA.

SET (Pin 7): GB Input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.25V reference.

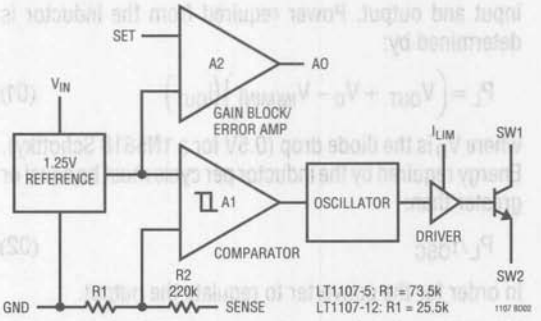
FB/SENSE (Pin 8): On the LT1107 (adjustable), this pin goes to the comparator input. On the LT1107-5 and LT1107-12, this pin goes to the internal application resistor that sets output voltage.

BLOCK DIAGRAMS

LT1107



LT1107-5/LT1107-12



OPERATION

The LT1107 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1107 block diagram. Comparator A1 compares the feedback (FB) pin voltage with the 1.25V reference signal. When FB drops below 1.25V, A1 switches on the 63kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator output is low, the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 300μA.

The oscillator is set internally for 11μs ON time and 5μs OFF time in step-up mode, optimizing the device for converters where $V_{OUT} \approx 3V_{IN}$. The combination of high duty cycle and the current limit feature enables continuous mode operation in many applications, increasing available output power.

Gain block A2 can serve as a low-battery detector. The negative input of A2 is the 1.25V reference. A resistor divider from V_{IN} to GND, with the mid-point connected to the SET pin provides the trip voltage in a low-battery detector application. AO can sink 300μA (use a 22k resistor pull-up to 5V).

A resistor connected between the I_{LIM} pin and V_{IN} sets maximum switch current. When the switch current exceeds the set value, the switch cycle is prematurely terminated. If current limit is not used, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current limit circuitry is approximately 1μs.

In step-up mode the switch emitter (SW2) is connected to ground and the switch collector (SW1) drives the inductor; in step-down mode the collector is connected to V_{IN} and the emitter drives the inductor.

The LT1107-5 and LT1107-12 are functionally identical to the LT1107. The -5 and -12 versions have on-chip voltage setting resistors for fixed 5V or 12V outputs. Pin 8 on the fixed versions should be connected to the output. No external resistors are needed.

4

APPLICATIONS INFORMATION

Inductor Selection — Step-Up Converter

In a step-up, or boost converter (Figure 1), power generated by the inductor makes up the difference between input and output. Power required from the inductor is determined by:

$$P_L = \left(V_{OUT} + V_D - V_{IN(MIN)}\right)\left(I_{OUT}\right) \quad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than:

$$P_L / f_{OSC} \quad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to:

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (03)$$

where R′ is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation:

$$I_L(t) = \frac{V_{IN}}{L}t \quad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch ON time from the LT1107 specification table (typically 11µs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch ON time can be calculated as:

$$E_L = \frac{1}{2}LI_{PEAK}^2 \quad (05)$$

E_L must be greater than P_L/f_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 60mA is to be generated from a 3V to 6V input. Recalling equation (01),

$$P_L = \left(12V + 0.5V - 3V\right)\left(60mA\right) = 570mW \quad (06)$$

Energy required from the inductor is:

$$\frac{P_L}{f_{OSC}} = \frac{570mW}{63kHz} = 9.05\mu J \quad (07)$$

Picking an inductor value of 33µH with 0.2Ω DCR results in a peak switch current of:

$$I_{PEAK} = \frac{3V}{1\Omega}\left(1 - e^{\frac{-1\Omega \times 11\mu s}{33\mu H}}\right) = 850mA \quad (08)$$

Substituting I_{PEAK} into Equation 04 results in:

$$E_L = \frac{1}{2}\left(33\mu H\right)\left(0.85A\right)^2 = 11.91\mu J \quad (09)$$

Since 11.9µJ > 9.05µJ, the 33µH inductor will work. This trial-and-error approach can be used to select the optimum inductor.

A resistor can be added in series with the I_{LIM} pin to invoke switch current limit. The resistor should be picked so the calculated I_{PEAK} at minimum V_{IN} is equal to the Maximum Switch Current (from Typical Performance Characteristic curves). Then, as V_{IN} increases, peak switch current is held constant, resulting in increasing efficiency.

Inductor Selection — Step-Down Converter

The step-down case (Figure 2) differs from the step-up in that the inductor current flows through the load during both the charge and discharge periods of the inductor. Current through the switch should be limited to ~650mA in this mode. Higher current can be obtained by using an external switch (see LT1111 and LT1110 data sheets). The I_{LIM} pin is the key to successful operation over varying inputs.

After establishing output voltage, output current and input voltage range, peak switch current can be calculated by the formula:

$$I_{PEAK} = \frac{2I_{OUT}}{DC}\left[\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right] \quad (10)$$

APPLICATIONS INFORMATION

where DC = duty cycle (0.50 in step-down mode)
V_{SW} = switch drop in step-down mode
V_D = diode drop (0.5V for a 1N5818)
I_{OUT} = output current
V_{OUT} = output voltage
V_{IN} = minimum input voltage

V_{SW} is actually a function of switch current which is in turn a function of V_{IN}, L, time, and V_{OUT}. To simplify, 1.5V can be used for V_{SW} as a very conservative value.

Once I_{PEAK} is known, inductor value can be derived from:

$$L = \frac{V_{IN(MIN)} - V_{SW} - V_{OUT}}{I_{PEAK}} \times t_{ON} \quad (11)$$

where t_{ON} = switch ON time (7µs).

Next, the current limit resistor R_{LIM} is selected to give I_{PEAK} from the Maximum Switch Current vs R_{LIM} curve. The addition of this resistor keeps maximum switch current constant as the input voltage is increased.

As an example, suppose 5V at 300mA is to be generated from a 12V to 24V input. Recalling Equation (10):

$$I_{PEAK} = \frac{2(300mA)}{0.50}\left[\frac{5+0.5}{12-1.5+0.5}\right] = 600mA \quad (12)$$

Next, inductor value is calculated using Equation (11):

$$L = \frac{12-1.5-5}{600mA} 7\mu s = 64\mu H \quad (13)$$

Use the next lowest standard value (56µH).

Then pick R_{LIM} from the curve. For I_{PEAK} = 600mA, R_{LIM} = 56Ω.

Inductor Selection — Positive-to-Negative Converter

Figure 4 shows hookup for positive-to-negative conversion. All of the output power must come from the inductor. In this case,

$$P_L = \left(|V_{OUT}| + V_D\right)\left(I_{OUT}\right) \quad (14)$$

In this mode the switch is arranged in common collector or step-down mode. The switch drop can be modeled as a 0.75V source in series with a 0.65Ω resistor. When the switch closes, current in the inductor builds according to:

$$I_L(t) = \frac{V_L}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (15)$$

where $R' = 0.65\Omega + DCR_L$
$V_L = V_{IN} - 0.75V$

As an example, suppose –5V at 50mA is to be generated from a 4.5V to 5.5V input. Recalling Equation (14),

$$P_L = \left(|-5V| + 0.5V\right)(50mA) = 275mW \quad (16)$$

Energy required from the inductor is:

$$\frac{P_L}{f_{OSC}} = \frac{275mW}{63kHz} = 4.4\mu J \quad (17)$$

Picking an inductor value of 100µH with 0.2Ω DCR results in a peak switch current of:

$$I_{PEAK} = \frac{(4.5V - 0.75V)}{(0.65\Omega + 0.2\Omega)}\left(1 - e^{\frac{-0.85\Omega \times 9\mu s}{100\mu H}}\right) = 325mA \quad (18)$$

Substituting I_{PEAK} into Equation (04) results in:

$$E_L = \frac{1}{2}(100\mu H)(0.325A)^2 = 5.28\mu J \quad (19)$$

Since 5.28µJ > 3.82µJ, the 100µH inductor will work.

With this relatively small input range, R_{LIM} is not usually necessary and the I_{LIM} pin can be tied directly to V_{IN}. As in the step-down case, peak switch current should be limited to ~650mA.

Step-Up (Boost Mode) Operation

A step-up DC/DC converter delivers an output voltage higher than the input voltage. Step-up converters are *not* short-circuit protected since there is a DC path from input to output.

APPLICATIONS INFORMATION

The usual step-up configuration for the LT1107 is shown in Figure 1. The LT1107 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1. At the end of the switch ON time the current in L1 is[1]:

$$I_{PEAK} = \frac{V_{IN}}{L} t_{ON} \quad (20)$$

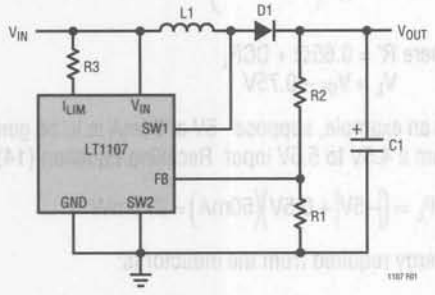


Figure 1. Step-Up Mode Hookup

Immediately after switch turn-off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1107 to keep V_{FB} at the internal reference voltage of 1.25V. R1 and R2 set the output voltage according to the formula:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V) \quad (21)$$

Step-Down (Buck Mode) Operation

A step-down DC/DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1107 based step-down converter is shown in Figure 2.

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to:

$$I_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON} \quad (22)$$

Note 1: This simple expression neglects the effects of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

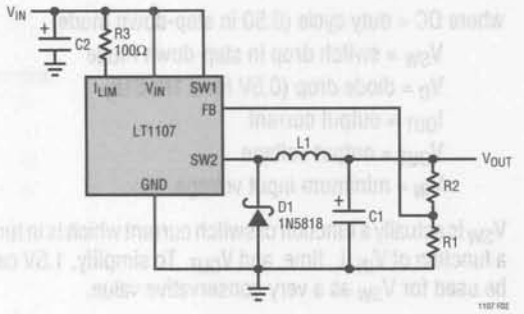


Figure 2. Step-Down Mode Hookup

When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below –0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to –0.8V, causing potentially destructive power dissipation inside the LT1107. Output voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V) \quad (23)$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 100Ω resistor programs the switch to turn off when the current reaches approximately 700mA. When using the LT1107 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

Inverting Configurations

The LT1107 can be configured as a positive-to-negative converter (Figure 3), or a negative-to-positive converter (Figure 4). In Figure 3, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode,

APPLICATIONS INFORMATION

and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accommodated as in the prior section.

In Figure 4, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

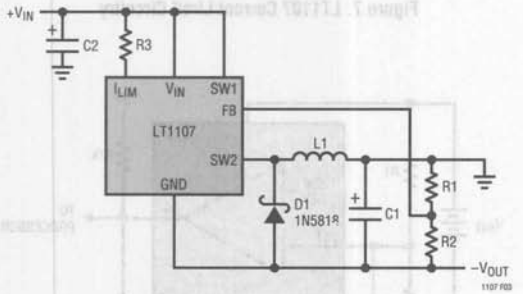


Figure 3. Positive-to-Negative Converter

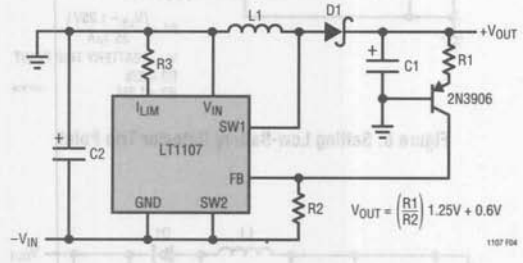


Figure 4. Negative-to-Positive Converter

Using the I_{LIM} Pin

The LT1107 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1107 must operate at an 800mA peak switch current with a 2V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs R_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when:

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC} \quad (24)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn-on. As shown in Figure 5, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, the switch turns off at the programmed current as shown in Figure 6, keeping output ripple to a minimum.

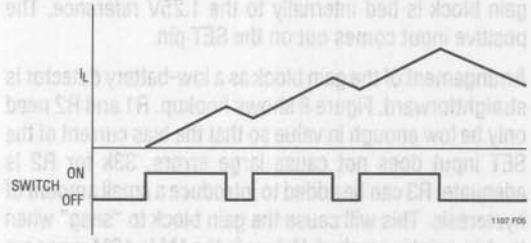


Figure 5. No Current Limit Causes Large Inductor Current Build-Up

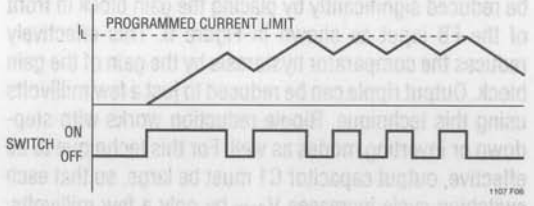


Figure 6. Current Limit Keeps Inductor Current Under Control

APPLICATIONS INFORMATION

Figure 7 details current limit circuitry. Sense transistor A1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current is passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} sets the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 800ns. The current trip point becomes less accurate for switch ON times less than 3µs. Resistor values programming switch ON time for 800ns or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

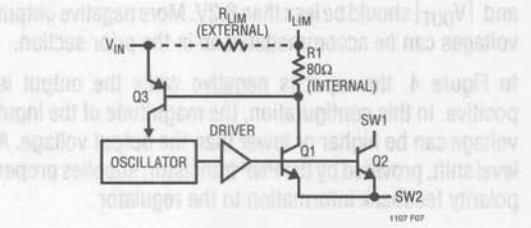


Figure 7. LT1107 Current Limit Circuitry

Using the Gain Block

The gain block (GB) on the LT1107 can be used as an error amplifier, low-battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 1.25V reference. The positive input comes out on the SET pin.

Arrangement of the gain block as a low-battery detector is straightforward. Figure 8 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 33k for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M to 10M range are optimal. The addition of R3 will change the trip point, however.

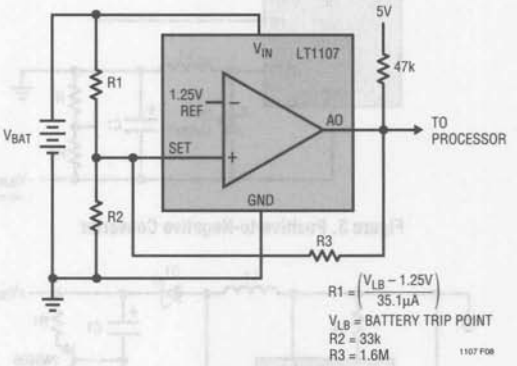


Figure 8. Setting Low-Battery Detector Trip Point

Output ripple of the LT1107, normally 50mV at $5V_{OUT}$ can be reduced significantly by placing the gain block in front of the FB input as shown in Figure 9. This effectively reduces the comparator hysteresis by the gain of the gain block. Output ripple can be reduced to just a few millivolts using this technique. Ripple reduction works with step-down or inverting modes as well. For this technique to be effective, output capacitor C1 must be large, so that each switching cycle increases V_{OUT} by only a few millivolts. 1000µF is a good starting value. C1 should be a low ESR type as well.

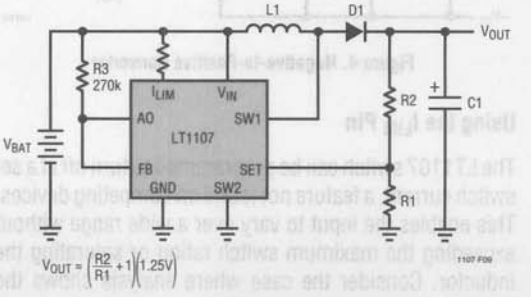
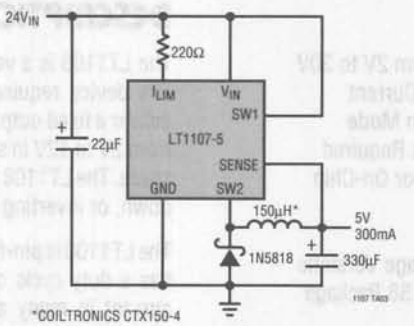


Figure 9. Output Ripple Reduction Using Gain Block

TYPICAL APPLICATION

24V-to-5V Step-Down Converter



*COILTRONICS CTX150-4

Micropower DC/DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages from 2V to 30V
- Consumes Only 110µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Four External Components Required
- Low Battery Detector Comparator On-Chip
- User Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or S8 Package

APPLICATIONS

- Palmtop Computers
- 3V to 5V, 5V to 12V Converters
- 9V to 5V, 12V to 5V Converters
- LCD Bias Generators
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Cellular Telephones
- Portable Instruments

DESCRIPTION

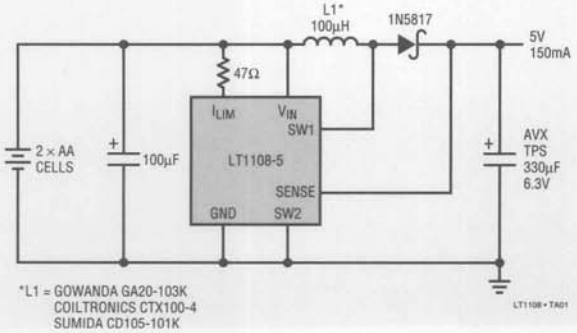
The LT1108 is a versatile micropower DC/DC converter. The device requires only four external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2V to 12V in step-up mode and to 30V in step-down mode. The LT1108 functions equally well in step-up, step-down, or inverting applications.

The LT1108 is pin-for-pin compatible with the LT1173, but has a duty cycle of 70%, resulting in increased output current in many applications. The LT1108 can deliver 150mA at 5V from a 2 AA cell input and 5V at 300mA from 9V in step-down mode. Quiescent current is just 110µA, making the LT1108 ideal for power conscious battery-operated systems.

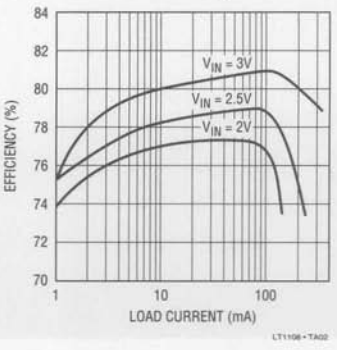
Switch current limit can be programmed with a single resistor. An auxiliary gain block can be configured as a low battery detector, linear post regulator, undervoltage lock-out circuit, or error amplifier.

TYPICAL APPLICATION

Palmtop Computer Logic Supply



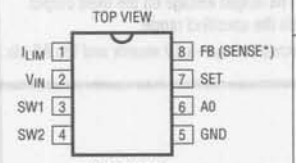
Efficiency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 36V
SW1 Pin Voltage (V_{SW1}) 50V
SW2 Pin Voltage (V_{SW2}) ..... −0.5V to V_{IN}
Feedback Pin Voltage (LT1108) 5.5V
Sense Pin Voltage (LT1108, -5, -12) 36V
Maximum Power Dissipation 500mW
Maximum Switch Current 1.5A
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



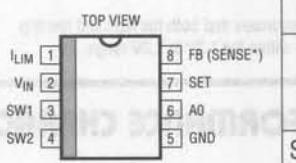
N8 PACKAGE
8-LEAD PLASTIC DIP

*FIXED VERSIONS

T_{JMAX} = 90°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1108CN8
LT1108CN8-5
LT1108CN8-12



S8 PACKAGE
8-LEAD PLASTIC SOIC

*FIXED VERSIONS

T_{JMAX} = 90°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1108CS8
LT1108CS8-5
LT1108CS8-12

S8 PART MARKING

1108
11085
11081

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch OFF	●		110	150	µA
	Quiescent Current, Boost Mode Configuration	No Load LT1108-5 LT1108-12			135 250		µA µA
V_{IN}	Input Voltage	Step-Up Mode Step-Down Mode	● ●	2		12.6 30.0	V V
	Comparator Trip Point Voltage	LT1108 (Note 1)	●	1.2	1.245	1.3	V
V_{OUT}	Output Sense Voltage	LT1108-5 (Note 2) LT1108-12 (Note 2)	● ●	4.75 11.4	5 12	5.25 12.6	V V
	Comparator Hysteresis	LT1108	●		5	10	mV
	Output Hysteresis	LT1108-5 LT1108-12	● ●		20 50	40 100	mV mV
f_{OSC}	Oscillator Frequency		●	14	19	25	kHz
	Duty Cycle	Full Load, Step-Up Mode	●	63	70	78	%
t_{ON}	Switch-ON Time	I_{LIM} Tied to V_{IN}, Step-Up Mode	●	28	36	48	µs
	Feedback Pin Bias Current	LT1108, $V_{FB} \approx 0V$	●		10	50	nA
	Set Pin Bias Current	$V_{SET} = V_{REF}$	●		20	100	nA
V_{OL}	Gain Block Output Low	I_{SINK} = 100µA, V_{SET} = 1V	●		0.15	0.4	V
	Reference Line Regulation	2V ≤ V_{IN} ≤ 5V 5V ≤ V_{IN} ≤ 30V	● ●		0.20 0.02	0.400 0.075	%/V %/V
V_{SAT}	SW_{SAT} Voltage, Step-Up Mode	V_{IN} = 3V, I_{SW} = 650mA V_{IN} = 5V, I_{SW} = 1A	●		0.5 0.8	0.65 1.00	V V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	SW_{SAT} Voltage, Step-Down Mode	V_{IN} = 12V, I_{SW} = 650mA			1.1	1.5	V
			●			1.7	V
A_V	Gain Block Gain	R_L = 100k (Note 3)	●	400	1000		V/V
	Current Limit	220Ω from I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coefficient		●		−0.3		%/°C
	Switch OFF Leakage Current	Measured at SW1 Pin			1	10	µA
V_{SW2}	Maximum Excursion Below GND	I_{SW1} ≤ 10µA, Switch OFF			−400	−350	mV

The ● denotes specifications which apply over the full operating temperature range.

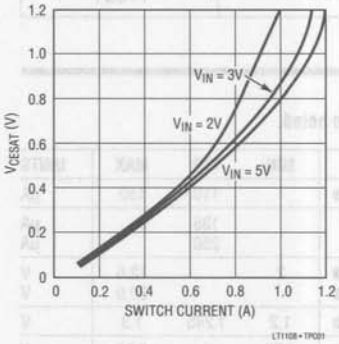
Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.2V to 1.3V range.

Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

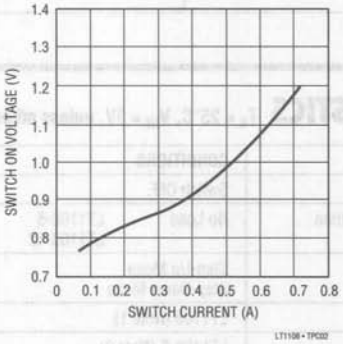
Note 3: 100k resistor connected between a 5V source and the A0 pin.

TYPICAL PERFORMANCE CHARACTERISTICS

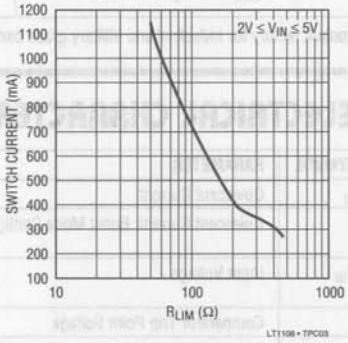
Saturation Voltage Step-Up Mode (SW2 Pin Grounded)



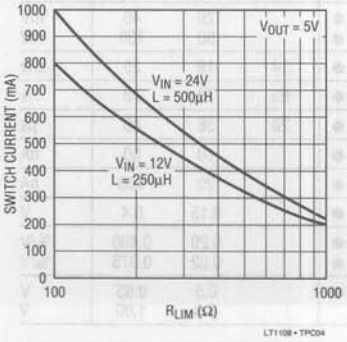
Switch ON Voltage Step-Down Mode (SW1 Pin Connected to V_{IN})



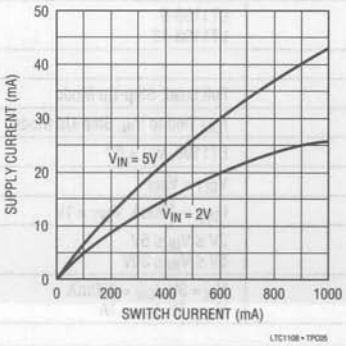
Maximum Switch Current vs R_{LIM}



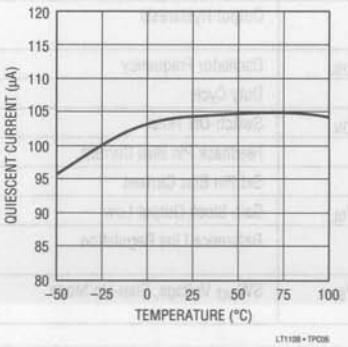
Saturation Voltage Step-Up Mode (SW2 Pin Grounded)



Supply Current vs Switch Current

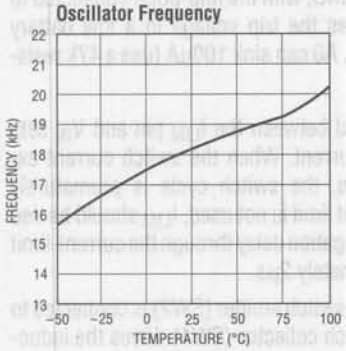


Quiescent Current

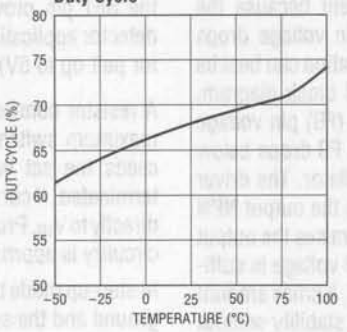


TYPICAL PERFORMANCE CHARACTERISTICS

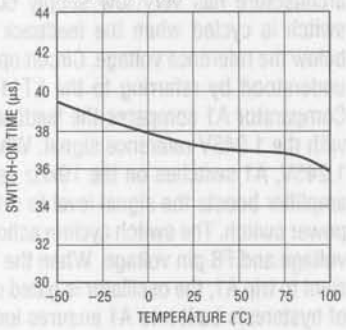
Oscillator Frequency



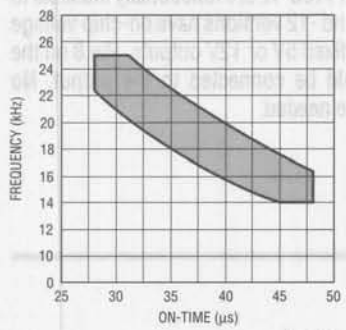
Duty Cycle



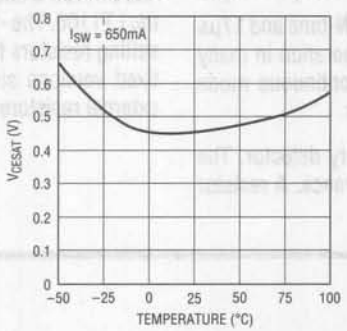
Switch-ON Time



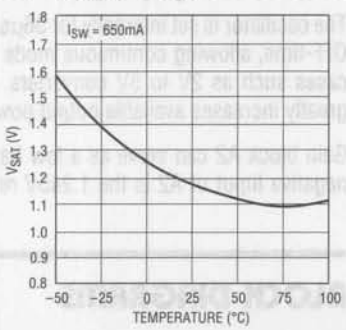
Minimum/Maximum Frequency vs ON-Time



Switch Saturation Voltage Step-Up Mode



Switch Saturation Voltage Step-Down Mode



4

PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

GND (Pin 5): Ground.

AO (Pin 6): Auxiliary gain block (GB) output. Open collector, can sink 100µA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.245V reference.

FB/SENSE (Pin 8): On the LT1108 (adjustable) this pin goes to the comparator input. On the LT1108-5 and LT1108-12, this pin goes to the internal application resistor that sets output voltage.

OPERATION

The LT1108 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1108 block diagram. Comparator A1 compares the feedback (FB) pin voltage with the 1.245V reference signal. When FB drops below 1.245V, A1 switches on the 19kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator output is low, the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 110µA.

The oscillator is set internally for 36µs ON-time and 17µs OFF-time, allowing continuous mode operation in many cases such as 2V to 5V converters. Continuous mode greatly increases available output power.

Gain block A2 can serve as a low battery detector. The negative input of A2 is the 1.245V reference. A resistor divider from V_{IN} to GND, with the mid-point connected to the SET pin provides the trip voltage in a low battery detector application. A0 can sink 100µA (use a 47k resistor pull-up to 5V).

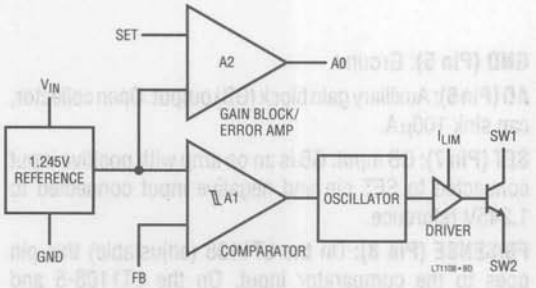
A resistor connected between the I_{LIM} pin and V_{IN} sets maximum switch current. When the switch current exceeds the set value, the switch cycle is prematurely terminated. If current limit is not used, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current-limit circuitry is approximately 2µs.

In step-up mode the switch emitter (SW2) is connected to ground and the switch collector (SW1) drives the inductor; in step-down mode the collector is connected to V_{IN} and the emitter drives the inductor.

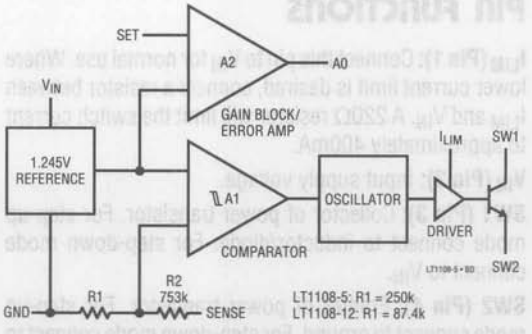
The LT1108-5 and LT1108-12 are functionally identical to the LT1108. The -5 and -12 versions have on-chip voltage setting resistors for fixed 5V or 12V outputs. Pin 8 on the fixed versions should be connected to the output. No external resistors are needed.

BLOCK DIAGRAMS

LT1108



LT1108-5/LT1108-12



APPLICATIONS INFORMATION

INDUCTOR SELECTION

General

A DC/DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology.

To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch-ON time. The inductance must also be high enough so maximum current ratings of the LT1108 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON-time.

Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1108 based designs, small surface mount ferrite core units with saturation current ratings in the 300mA to 1A range and DCR less than 0.4Ω (depending on application) are adequate.

Lastly, the inductor must have sufficiently low DC resistance so excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem. Minimum and maximum input voltage, output voltage and output current must be established before an inductor can be selected.

Step-Up Converter

In a step-up, or boost converter (Figure 1), power generated by the inductor makes up the difference between input and output. Power required from the inductor is determined by

$$P_L = (V_{OUT} + V_D - V_{IN\,MIN})(I_{OUT}) \quad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than

$$P_L / f_{OSC} \quad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (03)$$

where R' is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L} t \quad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch-ON time from the LT1108 specification table (typically 36µs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch-ON time can be calculated as

$$E_L = \frac{1}{2} L I_{PEAK}^2 \quad (05)$$

E_L must be greater than P_L/f_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 30mA is to be generated from a 2V to 3V input. Recalling equation (01),

$$P_L = (12V + 0.5V - 2V)(30mA) = 315mW \quad (06)$$

APPLICATIONS INFORMATION

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{315mW}{19kHz} = 16.6\mu J \quad (07)$$

Picking an inductor value of 100µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{2V}{1.0\Omega}\left(1 - e^{\frac{-1.0\Omega \times 36\mu s}{100\mu H}}\right) = 605mA \quad (08)$$

Substituting I_{PEAK} into Equation 04 results in

$$E_L = \frac{1}{2}(100\mu H)(6.605A)^2 = 18.3\mu J \quad (09)$$

Since 18.3µJ > 16.6µJ, the 100µH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.5A. If the calculated peak current exceeds this, an external power transistor can be used.

A resistor can be added in series with the I_{LIM} pin to invoke switch current limit. The resistor should be picked so the calculated I_{PEAK} at minimum V_{IN} is equal to the Maximum Switch Current (from Typical Performance Characteristic curves). Then, as V_{IN} increases, switch current is held constant, resulting in increasing efficiency.

Step-Down Converter

The step-down case (Figure 2) differs from the step-up in that the inductor current flows through the load during both the charge and discharge periods of the inductor. Current through the switch should be limited to ~650mA in this mode. Higher current can be obtained by using an external switch (see Figure 3). The I_{LIM} pin is the key to successful operation over varying inputs.

After establishing output voltage, output current and input voltage range, peak switch current can be calculated by the formula:

$$I_{PEAK} = \frac{2I_{OUT}}{DC}\left[\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right] \quad (10)$$

where DC = duty cycle (0.60)
V_{SW} = switch drop in step-down mode
V_D = diode drop (0.5V for a 1N5818)
I_{OUT} = output current
V_{OUT} = output voltage
V_{IN} = minimum input voltage

V_{SW} is actually a function of switch current which is in turn a function of V_{IN}, L, time, and V_{OUT}. To simplify, 1.5V can be used for V_{SW} as a very conservative value.

Once I_{PEAK} is known, inductor value can be derived from

$$L = \frac{V_{IN\,MIN} - V_{SW} - V_{OUT}}{I_{PEAK}} \times t_{ON} \quad (11)$$

where t_{ON} = switch-ON time (36µs).

Next, the current limit resistor R_{LIM} is selected to give I_{PEAK} from the R_{LIM} Step-Down Mode curve. The addition of this resistor keeps maximum switch current constant as the input voltage is increased.

As an example, suppose 5V at 300mA is to be generated from a 12V to 24V input. Recalling Equation (10),

$$I_{PEAK} = \frac{2(300mA)}{0.60}\left[\frac{5 + 0.5}{12 - 1.5 + 0.5}\right] = 500mA \quad (12)$$

Next, inductor value is calculated using Equation (11)

$$L = \frac{12 - 1.5 - 5}{500mA}\,36\mu s = 396\mu H \quad (13)$$

Use the next lowest standard value (330µH).

Then pick R_{LIM} from the curve. For I_{PEAK} = 500mA, R_{LIM} = 220Ω.

Positive-to-Negative Converter

Figure 4 shows hookup for positive-to-negative conversion. All of the output power must come from the inductor. In this case,

$$P_L = (|V_{OUT}| + V_D)(I_{OUT}) \quad (14)$$

APPLICATIONS INFORMATION

In this mode the switch is arranged in common collector or step-down mode. The switch drop can be modeled as a 0.75V source in series with a 0.65Ω resistor. When the switch closes, current in the inductor builds according to

$$I_L(t) = \frac{V_L}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (15)$$

where: $R' = 0.65\Omega + DCR_L$

$V_L = V_{IN} - 0.75V$

As an example, suppose –5V at 100mA is to be generated from a 4.5V to 5.5V input. Recalling Equation (14),

$$P_L = (|-5V| + 0.5V)(100mA) = 550mW. \quad (16)$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{550mW}{19kHz} = 28.9\mu J \quad (17)$$

Picking an inductor value of 220µH with 0.3Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{(4.5V - 0.75V)}{(0.65\Omega + 0.3\Omega)}\left(1 - e^{\frac{-0.95\Omega \times 36\mu s}{220\mu H}}\right) \quad (18)$$

$$= 568mA$$

Substituting I_{PEAK} into Equation (04) results in

$$E_L = \frac{1}{2}(220\mu H)(0.568A)^2 = 35.5\mu J \quad (19)$$

Since 35.5µJ > 28.9µJ, the 220µH inductor will work.

Finally, R_{LIM} should be selected by looking at the Switch Current vs R_{LIM} curve. In this example, $R_{LIM} = 150\Omega$.

STEP-UP (BOOST MODE) OPERATION

A step-up DC/DC converter delivers an output voltage higher than the input voltage. Step-up converters are not short-circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1108 is shown in Figure 1. The LT1108 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1. At the end of the switch-ON time the current in L1 is

$$I_{PEAK} = \frac{V_{IN}}{L} t_{ON}^{*} \quad (20)$$

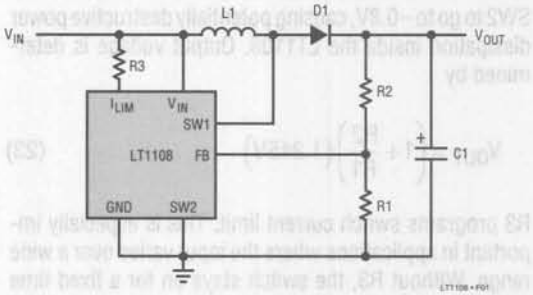


Figure 1. Step-Up Mode Hookup

Immediately after switch turn-off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1108 to keep V_{FB} at the internal reference voltage of 1.245V. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.245V) \quad (21)$$

STEP-DOWN (BUCK MODE) OPERATION

A step-down DC/DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1108 based step-down converter is shown in Figure 2.

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch-ON time, the current in L1 is equal to

*Expression 20 neglects the effect of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

APPLICATIONS INFORMATION

$$I_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON} \quad (22)$$

When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below –0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to –0.8V, causing potentially destructive power dissipation inside the LT1108. Output voltage is determined by

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.245V) \quad (23)$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 100Ω resistor programs the switch to turn off when the current reaches approximately 700mA. When using the LT1108 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

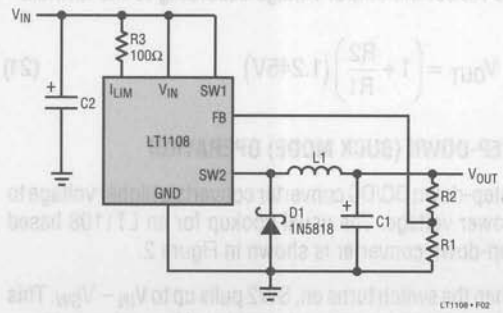


Figure 2. Step-Down Mode Hookup

HIGHER CURRENT STEP-DOWN OPERATION

Output current can be increased by using a discrete PNP pass transistor as shown in Figure 3. R1 serves as a current limit sense. When the voltage drop across R1 equals $0.5V_{BE}$, the switch turns off. As shown, switch current is limited to 2A. Inductor value can be calculated based on formulas in the Inductor Selection Step-Down Converter section with the following conservative expression for V_{SW}:

$$V_{SW} = V_{R1} + V_{Q1SAT} \approx 1.0V \quad (24)$$

R2 provides a current path to turn off Q1. R3 provides base drive to Q1. R4 and R5 set output voltage. A PMOS FET can be used in place of Q1 when V_{IN} is between 10V and 20V.

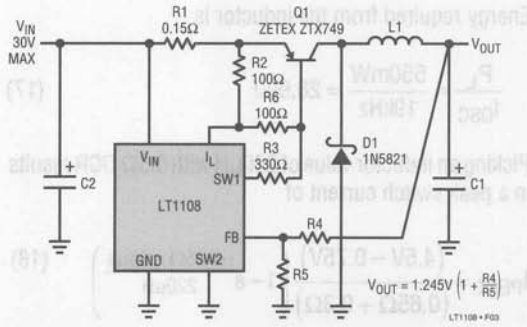


Figure 3. Q1 Permits Higher Current Switching The LT1108 Functions as Controller

INVERTING CONFIGURATIONS

The LT1108 can be configured as a positive-to-negative converter (Figure 4), or a negative-to-positive converter (Figure 5). In Figure 4, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accommodated as in the prior section.

In Figure 5, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A

APPLICATIONS INFORMATION

level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

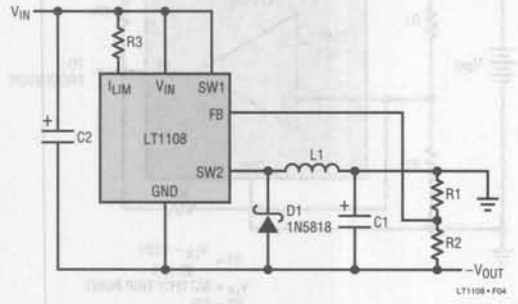


Figure 4. Positive-to-Negative Converter

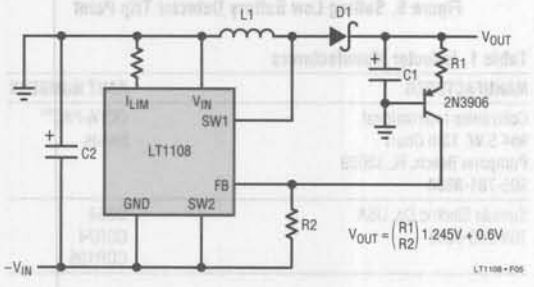


Figure 5. Negative-to-Positive Converter

USING THE I_{LIM} PIN

The LT1108 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1108 must operate at an 800mA peak switch current with a 2.0V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs R_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC} \quad (25)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch-OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn-on. As shown in Figure 6, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 7, keeping output ripple to a minimum.

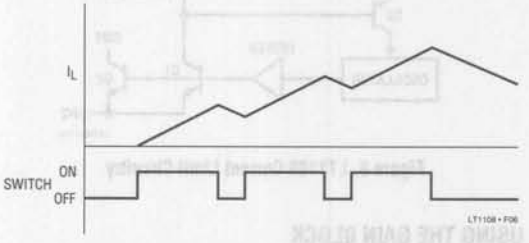


Figure 6. No Current Limit Causes Large Inductor Current Build-Up

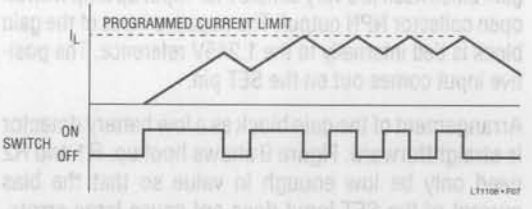


Figure 7. Current Limit Keeps Inductor Current Under Control

4

APPLICATIONS INFORMATION

Figure 8 details current limit circuitry. Sense transistor Q1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} sets the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 2µs. The current trip point becomes less accurate for switch-ON times less than 5µs. Resistor values programming switch-ON time for 2µs or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

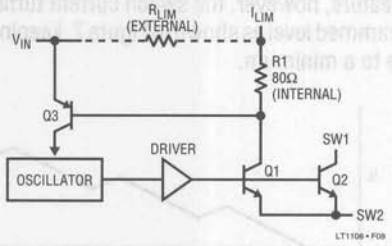


Figure 8. LT1108 Current Limit Circuitry

USING THE GAIN BLOCK

The gain block (GB) on the LT1108 can be used as an error amplifier, low battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 1.245V reference. The positive input comes out on the SET pin.

Arrangement of the gain block as a low battery detector is straightforward. Figure 9 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 33k for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M to 10M range are optimal. The addition however, of R3 will change the trip point.

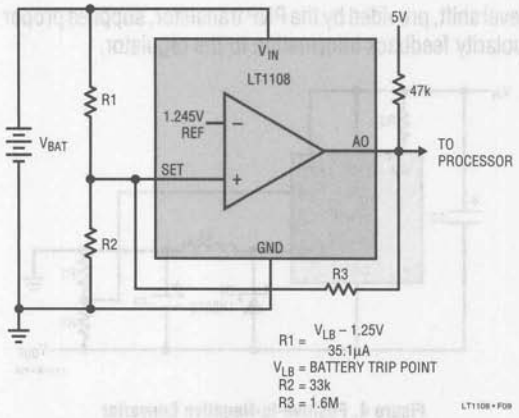


Figure 9. Setting Low Battery Detector Trip Point

Table 1. Inductor Manufacturers

MANUFACTURER	PART NUMBERS
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	OCTA-PAC™ Series
Sumida Electric Co. USA 708-956-0666	CD54 CDR74 CDR105

Table 2. Capacitor Manufacturers

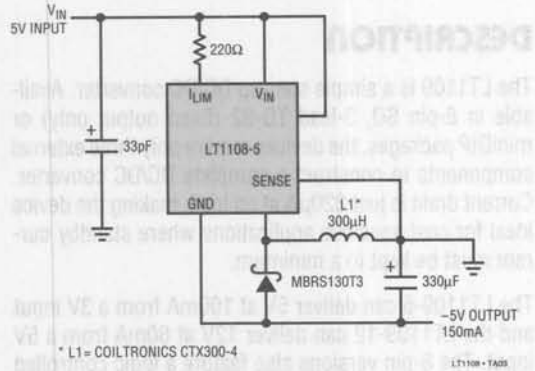
MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
AVX Corporation Myrtle Beach, SC 803-946-0690	TPS Series

Table 3. Transistor Manufacturers

MANUFACTURER	PART NUMBERS
Zetex Inc. 87 Modular Avenue Commack, NY 11725 516-543-7100	ZTX 749 (NPN) ZTX 849 (NPN) ZTX 949 (PNP)

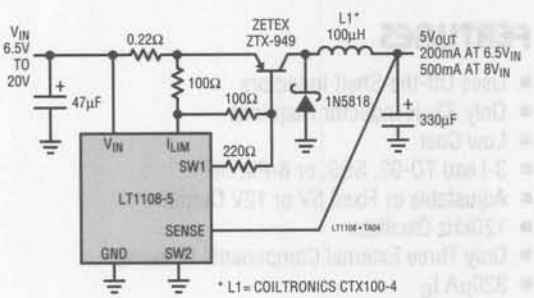
TYPICAL APPLICATIONS

5V to –5V Converter



* L1 = COILTRONICS CTX300-4

6.5V-20V to 5V Step-Down Converter



* L1 = COILTRONICS CTX100-4

4

Micropower Low Cost DC/DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Uses Off-the-Shelf Inductors
- Only 33µH Inductor Required
- Low Cost
- 3-Lead TO-92, SO8, or 8-Pin DIP
- Adjustable or Fixed 5V or 12V Output
- 120kHz Oscillator
- Only Three External Components Required
- 320µA I_Q
- 1.6V Minimum Start-Up Voltage
- Logic Controlled Shutdown

APPLICATIONS

- Flash Memory VPP Generators
- 3V to 5V Converters
- 5V to 12V Converters
- Disk Drives
- PC Plug-In Cards
- Peripherals
- Battery-Powered Equipment

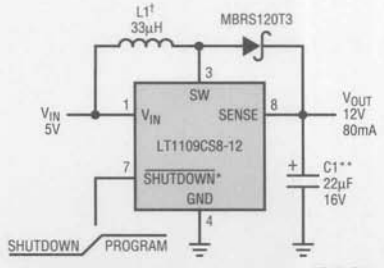
DESCRIPTION

The LT1109 is a simple step-up DC/DC converter. Available in 8-pin SO, 3-lead TO-92 (fixed output only) or miniDIP packages, the devices require only three external components to construct a complete DC/DC converter. Current drain is just 320µA at no load, making the device ideal for cost-sensitive applications where standby current must be kept to a minimum.

The LT1109-5 can deliver 5V at 100mA from a 3V input and the LT1109-12 can deliver 12V at 60mA from a 5V input. The 8-pin versions also feature a logic controlled $\overline{\text{SHUTDOWN}}$ pin that turns off the oscillator when taken low. The gated-oscillator design requires no frequency compensation components. The high frequency 120kHz oscillator permits the use of small surface mount inductors and capacitors. For a 5V to 12V at 120mA converter, see the LT1109A. Foa a 5V to 12V at 200mA converter with 20µA shutdown current, see the LT1301.

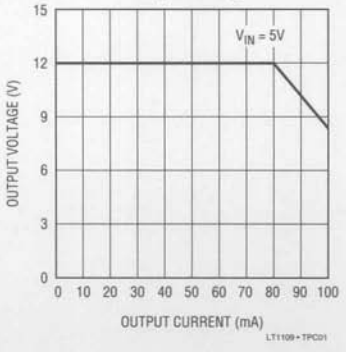
TYPICAL APPLICATION

All Surface Mount Flash Memory VPP Generator

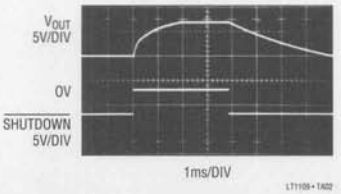


* 8-PIN PACKAGE ONLY
† L1 = SUMIDA CD54-330LC (I_{OUT} = 80mA)
COILTRONICS CTX33-1 (80mA)
MURATA-ERIE LQH4N330K (I_{OUT} = 50mA)
ISI LCS2414-330K (I_{OUT} = 50mA)
**C1 = MATSUO 267M1602226 OR EQUIVALENT

Output Voltage



Flash Memory Program Output



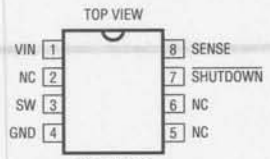
ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin)

Supply Voltage (V_{OUT}) ..... −0.4V to 20V
SW Pin Voltage ..... −0.4V to 50V
SHUTDOWN Pin Voltage 6.0V
Maximum Power Dissipation 300mW

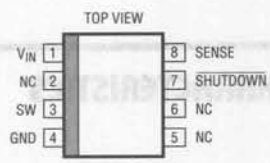
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Switch Current 1.2A

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

Z PACKAGE
3-LEAD TO-92 PLASTIC

T_{JMAX} = 100°C, θ_{JA} = 160°C/W

ORDER PART NUMBER	ORDER PART NUMBER	S8 PART MARKING	ORDER PART NUMBER
LT1109CN8 LT1109CN8-5 LT1109CN8-12	LT1109CS8 LT1109CS8-5 LT1109CS8-12	1109 10905 10912	LT1109CZ-5 LT1109CZ-12

Consult factory for Industrial and Military grade parts.

4

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{IN} = 3V (LT1109CN8, LT1109CS8), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off	●		320	550	µA
	Minimum Start-Up Voltage at V_{OUT} Pin (Z Package)			1.6			V
V_{IN}	Input Voltage (N8, S8 Package)		●	3			V
	Comparative Trip Point Voltage	LT1109	●	1.20	1.25	1.30	V
V_{OUT}	Output Voltage	LT1109-5; 3V ≤ V_{IN} ≤ 5V	●	4.75	5.00	5.25	V
		LT1109-12; 3V ≤ V_{IN} ≤ 12V	●	11.52	12.00	12.55	V
	Comparator Hysteresis	LT1109	●		8	12.5	mV
	Output Voltage Ripple	LT1109-5	●		25	50	mV
		LT1109-12	●		60	120	mV
f_{OSC}	Oscillator Frequency			100	120	140	kHz
			●	90		150	kHz
t_{ON}	Switch ON Time			3.3	4.2	5.3	µs
			●	3.0		5.5	µs
DC	Duty Cycle	Full Load	●	45	50	60	%
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 500mA			0.4	0.7	V
		LT1109-5: V_{IN} = 3V; LT1109-12: V_{IN} = 5V	●		0.5	0.8	V

ELECTRICAL CHARACTERISTICS

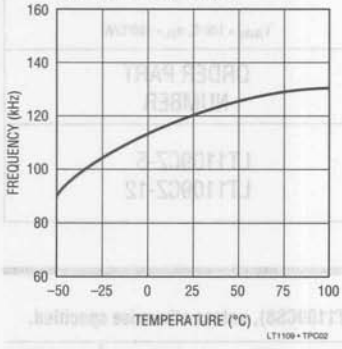
T_A = 25°C, V_{IN} = 3V (LT1109CN8, LT1109CS8), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Switch Leakage Current	V_{SW} = 12V			1	10	µA
V_{IH}	$\overline{\text{SHUTDOWN}}$ Pin High	N8, S8 Package	●	2.0			V
V_{IL}	$\overline{\text{SHUTDOWN}}$ Pin Low	N8, S8 Package	●			0.8	V
I_{IH}	$\overline{\text{SHUTDOWN}}$ Pin Input Current	N8, S8 Package, $V_{\overline{\text{SHUTDOWN}}}$ = 4V	●			10	µA
I_{IL}	$\overline{\text{SHUTDOWN}}$ Pin Input Current	N8, S8 Package, $V_{\overline{\text{SHUTDOWN}}}$ = 0V	●			20	µA

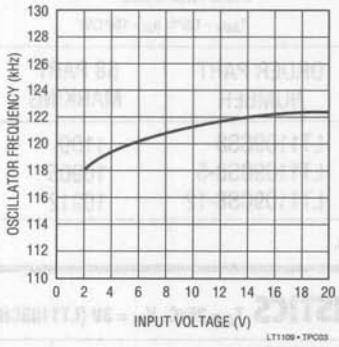
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

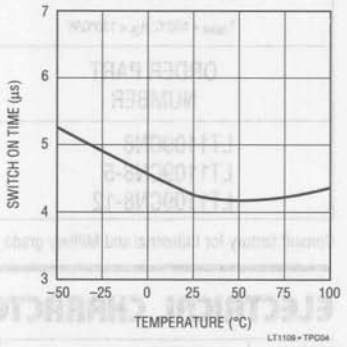
Oscillator Frequency



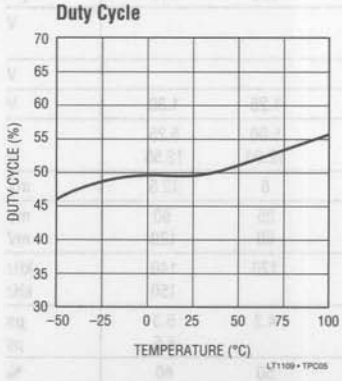
Oscillator Frequency



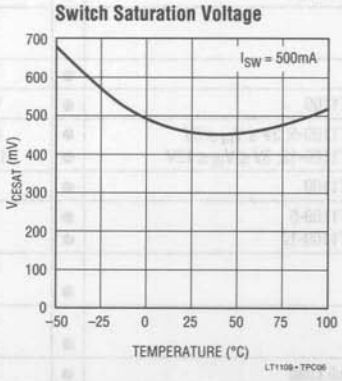
Switch ON Time



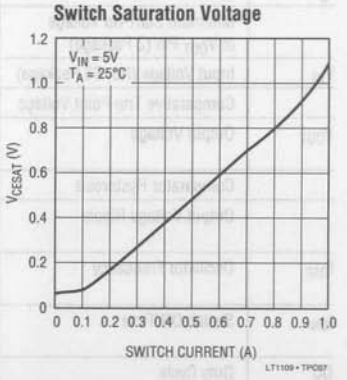
Duty Cycle



Switch Saturation Voltage

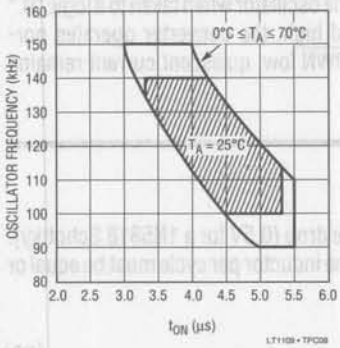


Switch Saturation Voltage

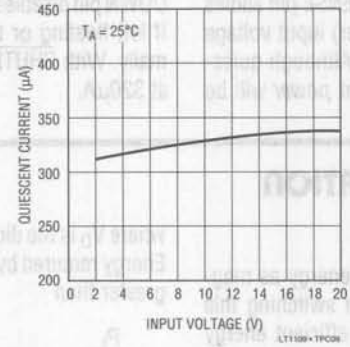


TYPICAL PERFORMANCE CHARACTERISTICS

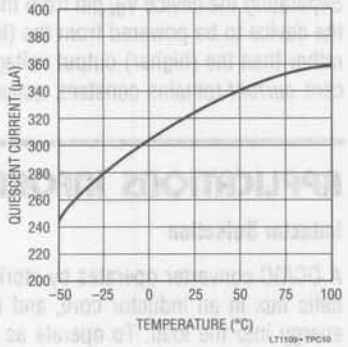
Minimum/Maximum Oscillator Frequency vs t_{ON}



Quiescent Current

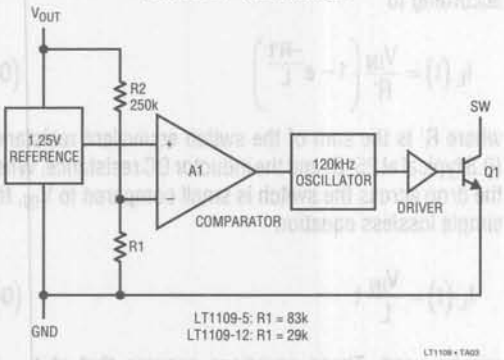


Quiescent Current

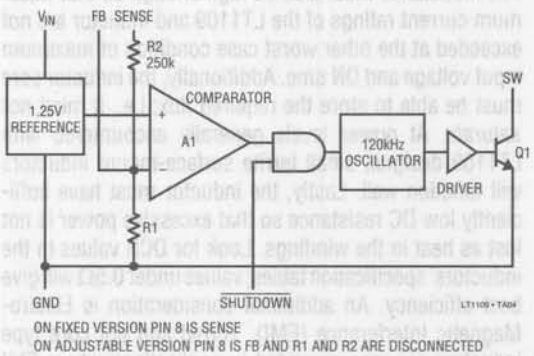


BLOCK DIAGRAMS

LT1109-5, -12 Z Package



LT1109-5, -12 N8, S8 Package



ON FIXED VERSION PIN 8 IS SENSE
ON ADJUSTABLE VERSION PIN 8 IS FB AND R1 AND R2 ARE DISCONNECTED

LT1109Z OPERATION

The LT1109Z-5 and LT1109Z-12 are fixed output voltage step-up DC/DC converters in a 3-pin TO-92 package. Power for internal regulator circuitry is taken from the V_{OUT} pin, a technique known as "bootstrapping." Circuit operation can be best understood by referring to the block diagram. V_{OUT}, attenuated by R1 and R2, is applied to the negative input of comparator A1. When this voltage falls below the 1.25V reference voltage, the oscillator is turned on and the power switch Q1 cycles at the oscillator frequency of 120kHz. Switch cycling alternately builds current in the inductor, then dumps it into the output capacitor, increasing the output voltage. When A1's negative input rises above 1.25V, it turns off the oscillator. A small amount of hysteresis in A1 obviates the need for frequency compensation circuitry. When Q1 is off, current into the V_{OUT} pin drops to just 320µA. Quiescent current from the battery will be higher because the device operates off the *stepped-up* voltage.

LT1109 S8 AND N8 OPERATION

The 8-pin versions of the LT1109 have separate pins for V_{IN} and SENSE or FB and also have a SHUTDOWN pin. Separating the device V_{IN} pin from the SENSE pin allows the device to be powered from the (lower) input voltage rather than the (higher) output voltage. Although quiescent *current* remains constant, quiescent *power* will be reduced by using the 8-pin version since the quiescent current flows from a lower voltage source. The SHUTDOWN pin disables the oscillator when taken to a logic "0." If left floating or tied high, the converter operates normally. With SHUTDOWN low, quiescent current remains at 320μA.

APPLICATIONS INFORMATION

Inductor Selection

A DC/DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch-ON time. The inductance must also be high enough so that maximum current ratings of the LT1109 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1109 designs, small ferrite surface-mount inductors will function well. Lastly, the inductor must have sufficiently low DC resistance so that excessive power is not lost as heat in the windings. Look for DCR values in the inductors' specification tables; values under 0.5Ω will give best efficiency. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem.

Specifying a proper inductor for an application requires first establishing minimum and maximum input voltage, output voltage, and output current. In a step-up converter, the inductive events add to the input voltage to produce the output voltage. Power required from the inductor is determined by

$$P_L = (V_{OUT} + V_D - V_{IN})\,(I_{OUT}) \qquad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than

$$\frac{P_L}{F_{OSC}} \qquad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \qquad (03)$$

where R' is the sum of the switch equivalent resistance (0.8 typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L}\,t \qquad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch-ON time from the LT1109 specification table (typically 4.2μs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch-ON time can be calculated as

$$E_L = \frac{1}{2}LI_{PEAK}^2 \qquad (05)$$

E_L must be greater than P_L/F_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be

APPLICATIONS INFORMATION

kept to 600mA or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 60mA is to be generated from a 4.5V input. Recalling Equation 01,

$$P_L = (12V + 0.5V - 4.5V)(60mA) = 480mW. \quad (06)$$

Energy required from the inductor is

$$\frac{P_L}{F_{OSC}} = \frac{480mW}{120kHz} = 4.0\mu J. \quad (07)$$

Picking an inductor value of 33µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{4.5V}{1.0\Omega}\left(1 - e^{\frac{-1.0 \bullet 4.2\mu s}{33\mu H}}\right) = 538mA. \quad (08)$$

Substituting I_{PEAK} into Equation 03 results in

$$E_L = \frac{1}{2}(33\mu H)(0.538A)^2 = 4.77\mu J. \quad (09)$$

Since 4.77µJ > 4µJ the 33µH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.2A. If the calculated peak current exceeds this, the input voltage must be increased or the load decreased.

Capacitor Selection

The output capacitor should be chosen on the basis of its equivalent series resistance (ESR). Surface-mount tantalum electrolytics can be used provided the ESR value is sufficiently low. An ESR of 0.1Ω will result in a 50mV step at the output of the converter when the peak inductor current is 500mA. Physically larger capacitors have lower ESR.

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1109 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10µs-50µs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1109 circuits will be well served by a 1N5818 Schottky diode. The combination of 500mV forward drop at 1A current, fast turn-ON and turn-OFF time, and 4µA to 10µA leakage current fit nicely with LT1109 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA to 5nA range at 25°C and lower cost than a 1N5818.

Table 1. Inductor Manufacturers

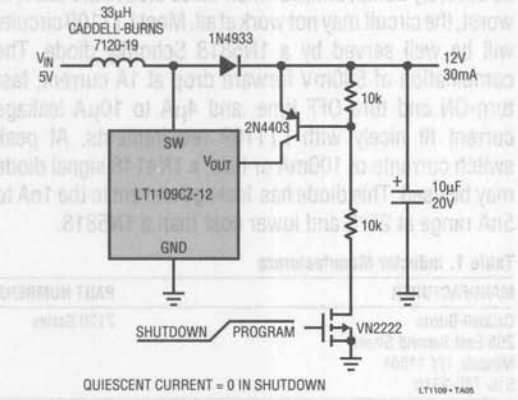
MANUFACTURER	PART NUMBERS
Caddell-Burns 258 East Second Street Mineola, NY 11501 516-746-2310	7120 Series
Coiltronics Incorporated 6000 Park of Commerce Blvd. Boca Raton, FL 33487 407-241-7876	Surface Mount CTX33-1
Coilcraft 1102 Silver Lake Road Cary, IL 60013 708-639-6400	DT3316 Series
Sumida Electric Co., Ltd. 637 E. Golf Road, Suite 209 Arlington Heights, IL 60005 708-956-0666	CD54 CD105 Surface Mount

Table 2. Capacitor Manufacturers

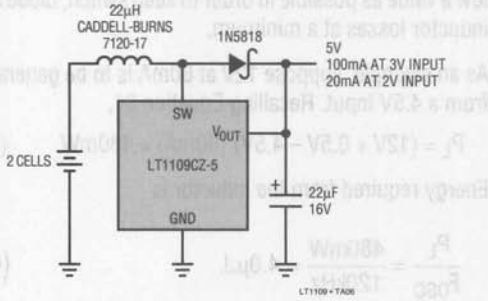
MANUFACTURER	PART NUMBERS
Sanyo Video Components 2001 Sanyo Avenue San Diego, CA 92173 619-661-6835	OS-CON Series
Matsuo Electronics 2134 Main Street, Suite 200 Huntington Beach, CA 92648 714-969-2491	267 Series
Kemet Electronics Corporation Box 5928 Greenville, SC 29606 803-963-6621	T491 Series
Philips Components 2001 W. Blue Heron Blvd. P.O. Box 10330 Riviera Beach, FL 33404 407-881-3200	49MC Series

TYPICAL APPLICATIONS

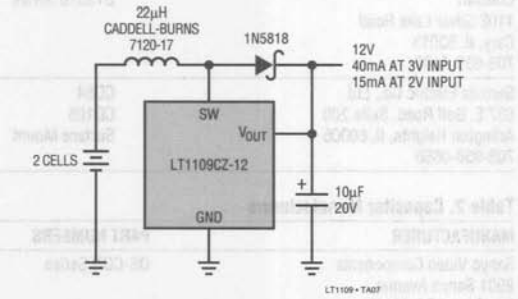
3-Pin Package Flash Memory VPP Generator



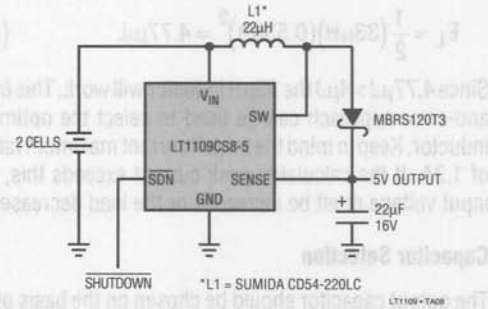
3V to 5V Converter



3V to 12V Converter



3V to 5V Converter with Shutdown



Micropower DC/DC Converter Flash Memory VPP Generator Adjustable and Fixed 5V, 12V

FEATURES

- Uses Off-the-Shelf Inductors
- Low Cost
- 8-Pin DIP or SO Package
- Fixed 5V or 12V Output or Adjustable Version
- Only Four External Components Required
- 360µA Standby Current
- Logic-Controlled Shutdown

APPLICATIONS

- Flash Memory VPP Generators
- 5V to 12V Converters
- 3.3V to 12V Converters
- Disk Drives
- PC Plug-In Cards
- Peripherals
- Battery-Powered Equipment

DESCRIPTION

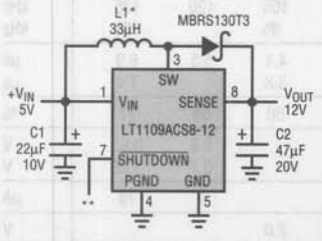
The LT1109A is a simple step-up DC/DC converter. The 8-pin DIP or SOIC devices require only four external components to construct a complete DC/DC converter. Current drain is just 360µA at no load, making the device ideal for cost-sensitive applications where standby current must be kept to a minimum.

The LT1109A-12 can deliver 12V at over 150mA from a 5V supply, enough power to program four flash memory chips simultaneously. The LT1109A-5 can deliver 5V at up to 110mA from a 2V input. The devices feature a shutdown pin that turns off the oscillator when taken low. The gated-oscillator design requires no frequency compensation components. High frequency 120kHz operation permits the use of small surface mount inductors and capacitors.

4

TYPICAL APPLICATION

All Surface Mount Flash Memory VPP Generator

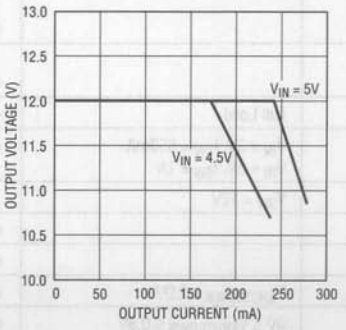


* COILTRONICS CTX33-2
SUMIDA CD54-330LC

** 1 = PROGRAM
0 = SHUTDOWN

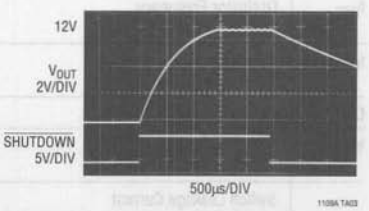
1109A TA01

Output Current



1109A TA02

Output Voltage

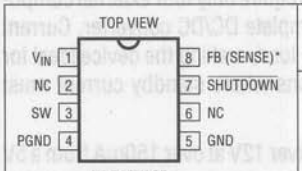


1109A TA03

ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin)
Supply Voltage (V_{IN}) ..... −0.4V to 20V
SW Pin Voltage ..... −0.4V to 50V
Feedback Pin Voltage (LT1109A) 5.5V
Shutdown Pin Voltage 5.5V
Switch Current 2A
Maximum Power Dissipation 300mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

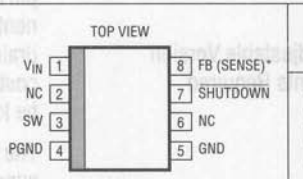


N8 PACKAGE
8-LEAD PLASTIC DIP
*FIXED VERSIONS

T_{JMAX} = 90°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1109ACN8
LT1109ACN8-5
LT1109ACN8-12



S8 PACKAGE
8-LEAD PLASTIC SO
*FIXED VERSIONS

T_{JMAX} = 90°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	S8 PART MARKING
LT1109ACS8	1109A
LT1109ACS8-5	1109A5
LT1109ACS8-12	1109A1

Consult factory for Industrial and Military grade parts.

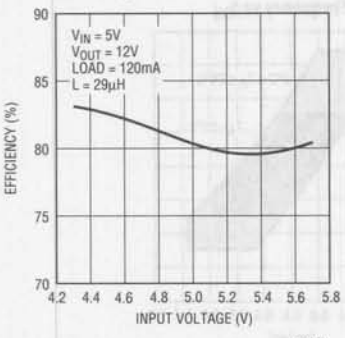
ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{IN} = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off	●		360	500	µA
V_{IN}	Input Voltage		●	2		9	V
	Comparator Trip Point Voltage	LT1109A	●	1.20	1.25	1.30	V
V_{OUT}	Output Sense Voltage	LT1109A-5; 2V ≤ V_{IN} ≤ 5V	●	4.75	5.00	5.25	V
		LT1109A-12; 2V ≤ V_{IN} ≤ 12V	●	11.52	12.00	12.55	V
	Comparator Hysteresis	LT1109A	●		8	12.5	mV
	Output Voltage Ripple	LT1109A-5	●		25	50	mV
		LT1109A-12	●		60	120	mV
f_{OSC}	Oscillator Frequency			105	120	135	kHz
			●	95		155	kHz
t_{ON}	Switch On Time			4.1	5.5	6.9	µs
			●	3.8		7.4	µs
DC	Duty Cycle	Full Load	●	60	68	77	%
V_{CESAT}	Switch Saturation Voltage	V_{IN} = 3V, I_{SW} = 650mA	●		0.5	0.65	V
		V_{IN} = 5V, I_{SW} = 1A			0.7	1.00	V
	Switch Leakage Current	V_{SW} = 12V			1	10	µA
V_{IH}	$\overline{\text{SHUTDOWN}}$ Pin High		●	2.0			V
V_{IL}	$\overline{\text{SHUTDOWN}}$ Pin Low		●			0.8	V
I_{IH}	$\overline{\text{SHUTDOWN}}$ Pin Input Current	$V_{\overline{\text{SHUTDOWN}}}$ ≥ 2.0V	●			10	µA
I_L	$\overline{\text{SHUTDOWN}}$ Pin Input Current	0V ≤ $V_{\overline{\text{SHUTDOWN}}}$ ≤ 0.8V	●			20	µA

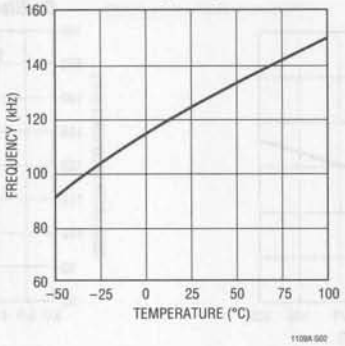
The ● denotes specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

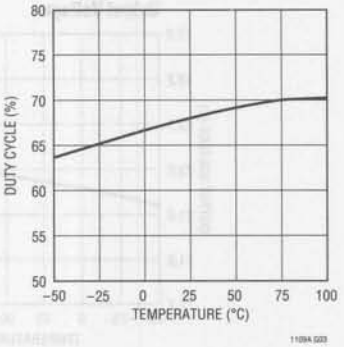
Efficiency



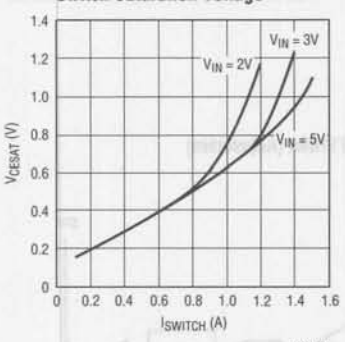
Oscillator Frequency



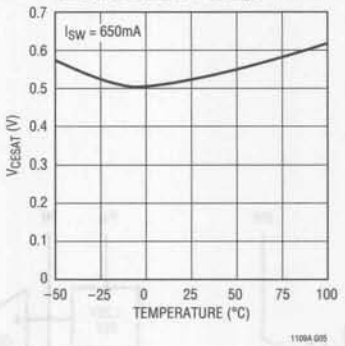
Duty Cycle



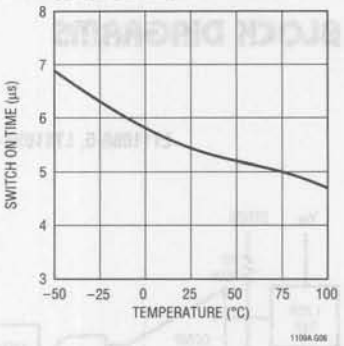
Switch Saturation Voltage



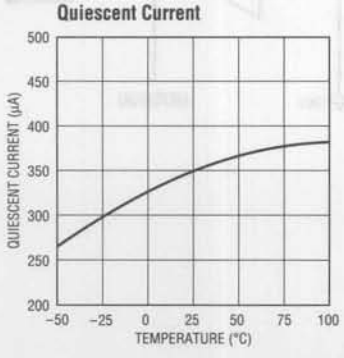
Switch Saturation Voltage



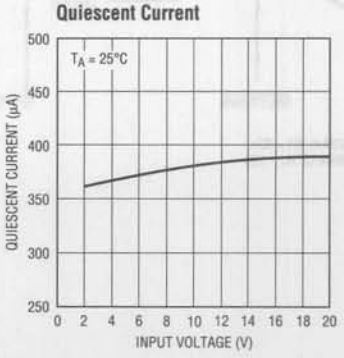
Switch On Time



Quiescent Current



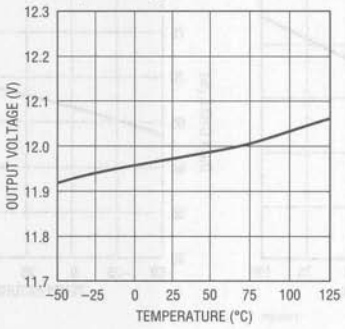
Quiescent Current



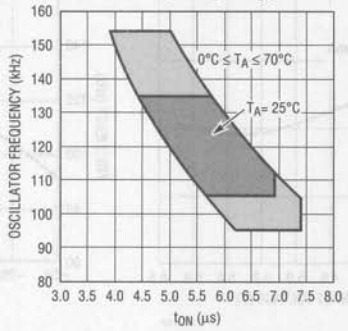
4

TYPICAL PERFORMANCE CHARACTERISTICS

LT1109A-12
Output Voltage

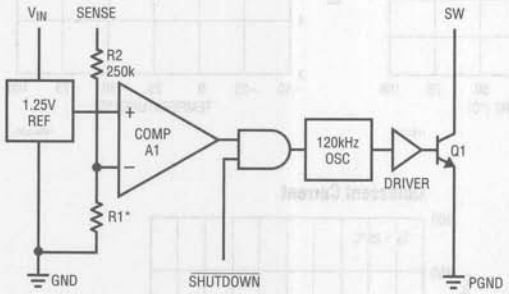


Minimum/Maximum
Oscillator Frequency vs t_{ON}



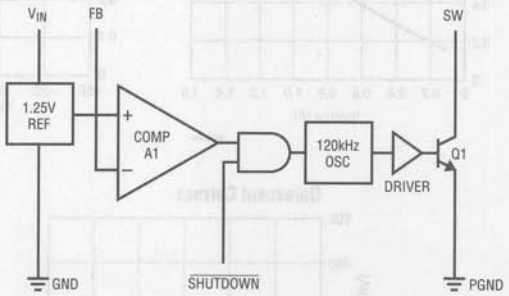
BLOCK DIAGRAMS

LT1109A-5, LT1109A-12



*LT1109A-5: R1 = 83k
LT1109A-12: R1 = 29k

LT1109A (Adjustable)



OPERATION

The LT1109A is a micropower step-up DC/DC converter. It uses Burst Mode™ operation to achieve micropower operation yet still deliver more than 2W of output power from a 5V supply. Circuit operation can be best understood by referring to the LT1109A block diagram. With SHUTDOWN high, comparator A1 compares the feedback (FB) pin voltage with the 1.25V reference signal. When FB drops below 1.25V, A1 switches on the 120kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. When the FB voltage is sufficient to trip A1, the oscillator is turned off. A low signal on the shutdown pin gates off the oscillator, overriding A1. With SHUTDOWN low, quiescent current remains at 360μA.

Burst Mode™ is a trademark of Linear Technology Corporation

APPLICATIONS INFORMATION

Inductor Selection

A DC/DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. To operate as an efficient energy transfer element, the inductor must fulfill three requirements: inductance value, saturation current and DC resistance. A fourth requirement is physical size. The inductors recommended with the LT1109A circuits are small, surface-mountable and are designed for switch-mode applications. Avoid using RF chokes or air core units since they have very low peak current ratings. The LT1109A works best in situations where the input voltage does not vary much since the device has no internal switch current limit function. For situations where the input voltage varies, such as battery inputs, the LT1107 or LT1111 is suggested instead.

Capacitor Selection

The output capacitor should be chosen on the basis of its equivalent series resistance (ESR) and capacitance value. Low ESR tantalum surface-mountable capacitors such as those made by AVX are well-suited for DC/DC converter applications. Inexpensive aluminum electrolytics may have excessive ESR, resulting in high output ripple. These should be avoided.

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a diode for LT1109A converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10μs to 50μs range. At best, efficiency will be severely compromised if this diode is used; at worst, the circuit may not work at all. The 1N5818 is an ideal choice for LT1109A circuits. Surface-mountable versions, such as the MBRS130T3, are available as well.

Table 1. Inductor Manufacturers

MANUFACTURER	PART NUMBERS
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	Surface Mount OCTA-PAC™ Series
Sumida Electric Co., Ltd. 637 E. Golf Road, Suite 209 Arlington Heights, IL 60005 708-956-0666	CD54 CD105 Surface Mount

OCTA-PAC™ is a trademark of Coiltronics International

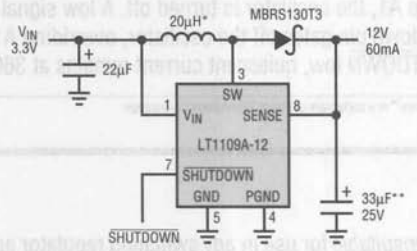
Table 2. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
AVX Myrtle Beach, SC 29578 803-946-0690	TPS Series
Philips Components 2001 W. Blue Heron Blvd. P.O. Box 10330 Riviera Beach, FL 33404 407-881-3200	49MC Series
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series

4

TYPICAL APPLICATIONS

3.3V Powered Flash Memory VPP Generator

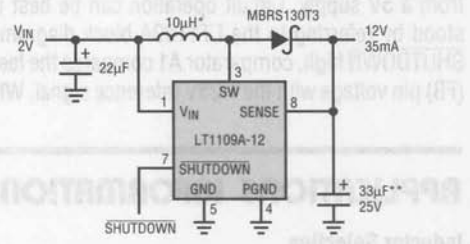


* COILTRONICS CTX20-1
SUMIDA CD54-220LC

** AVX TPS SERIES

1109A TA04

2V Powered Flash Memory VPP Generator

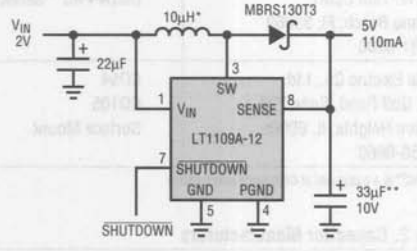


* COILTRONICS CTX10-1
SUMIDA CD54-100LC

** AVX TPS SERIES

1109A TA05

2V to 5V Converter

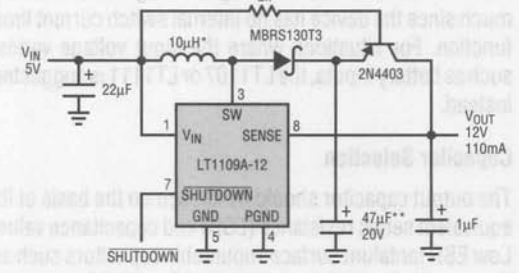


* COILTRONICS CTX10-1
SUMIDA CD54-100LC

** AVX TPS SERIES

1109A TA06

5V to 12V Converter with Shutdown to 0V at Output



* COILTRONICS CTX33-2
SUMIDA CD54-330LC

** AVX TPS SERIES

1109A TA07

Micropower DC/DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- **Operates at Supply Voltages from 2V to 30V**
- 72kHz Oscillator
- **Works with Surface Mount Inductors**
- Only Three External Components Required
- Step-Up or Step-Down Mode
- Low-Battery Detector Comparator On-Chip
- User Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or SO-8 Package

APPLICATIONS

- 3V to 5V, 5V to 12V Converters
- 9V to 5V, 12V to 5V Converters
- Remote Controls
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Uninterruptible Supplies
- Laptop and Palmtop Computers
- Cellular Telephones
- Portable Instruments
- Flash Memory VPP Generators

DESCRIPTION

The LT1111 is a versatile micropower DC/DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2V to 12V in step-up mode and to 30V in step-down mode. The LT1111 functions equally well in step-up, step-down, or inverting applications.

The LT1111 oscillator is set at 72kHz, optimizing the device to work with off-the-shelf surface mount inductors. The device can deliver 5V at 100mA from a 3V input in step-up mode or 5V at 200mA from a 12V input in step-down mode.

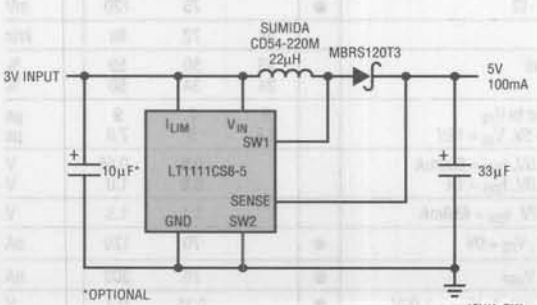
Switch current limit can be programmed with a single resistor. An auxiliary open-collector gain block can be configured as a low-battery detector, linear post regulator, undervoltage lock-out circuit, or error amplifier.

For input sources of less than 2V use the LT1110.

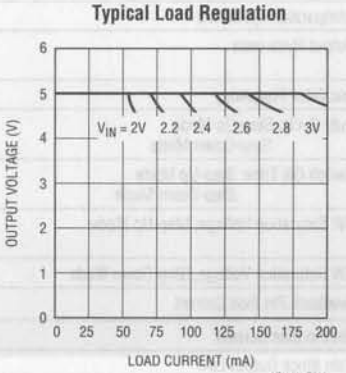
4

TYPICAL APPLICATION

All Surface Mount 3V to 5V Step-Up Converter



Typical Load Regulation

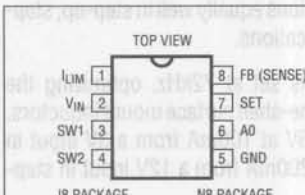


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 36V
SW1 Pin Voltage (V_{SW1}) 50V
SW2 Pin Voltage (V_{SW2}) ..... −0.5V to V_{IN}
Feedback Pin Voltage (LT1111) 5.5V
Switch Current 1.5A
Maximum Power Dissipation 500mW

Operating Temperature Range
LT1111C ..... 0°C to 70°C
LT1111I ..... −40°C to 105°C
LT1111M ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

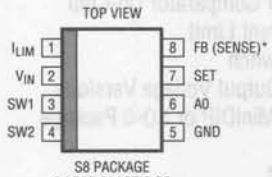


J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

*FIXED VERSIONS

T_{JMAX} = 150°C, θ_{JA} = 120°C/W (J)
T_{JMAX} = 90°C, θ_{JA} = 130°C/W (N)

ORDER PART NUMBER
LT1111CN8
LT1111CN8-5
LT1111CN8-12
LT1111MJ8
LT1111MJ8-5
LT1111MJ8-12



S8 PACKAGE
8-LEAD PLASTIC SO

*FIXED VERSION

T_{JMAX} = 90°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1111CS8
LT1111CS8-5
LT1111CS8-12
LT1111IS8
S8 PART MARKING
1111
11115
11111
1111I

ELECTRICAL CHARACTERISTICS V_{IN} = 3V, Military or Commercial Version

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch OFF			300	400	µA
V_{IN}	Input Voltage	Step-Up Mode Step-Down Mode	● ●	2.0		12.6 30.0	V V
	Comparator Trip Point Voltage	LT1111 (Note 1)	●	1.20	1.25	1.30	V
V_{OUT}	Output Sense Voltage	LT1111-5 (Note 2) LT1111-12 (Note 2)	● ●	4.75 11.40	5.00 12.00	5.25 12.60	V V
	Comparator Hysteresis	LT1111	●		8	12.5	mV
	Output Hysteresis	LT1111-5 LT1111-12	● ●		32 75	50 120	mV mV
f_{OSC}	Oscillator Frequency			54	72	88	kHz
DC	Duty Cycle: Step-Up Mode Step-Down Mode	Full Load		43 24	50 34	59 50	% %
t_{ON}	Switch ON Time: Step-Up Mode Step-Down Mode	I_{LIM} Tied to V_{IN} V_{OUT} = 5V, V_{IN} = 12V		5 3.3	7 5	9 7.8	µs µs
V_{SAT}	SW Saturation Voltage, Step-Up Mode	V_{IN} = 3.0V, I_{SW} = 650mA V_{IN} = 5.0V, I_{SW} = 1A			0.5 0.8	0.65 1.0	V V
	SW Saturation Voltage, Step-Down Mode	V_{IN} = 12V, I_{SW} = 650mA			1.1	1.5	V
I_{FB}	Feedback Pin Bias Current	LT1111, V_{FB} = 0V	●		70	120	nA
I_{SET}	Set Pin Bias Current	V_{SET} = V_{REF}	●		70	300	nA
V_{OL}	Gain Block Output Low	I_{SINK} = 300µA, V_{SET} = 1.00V	●		0.15	0.4	V

ELECTRICAL CHARACTERISTICS V_{IN} = 3V, Military or Commercial Version

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Reference Line Regulation	5V ≤ V_{IN} ≤ 30V 2V ≤ V_{IN} ≤ 5V	● ●		0.02 0.20	0.075 0.400	%/V %/V
A_V	Gain Block Gain	R_L = 100k (Note 3)	●	1000	6000		V/V
I_{LIM}	Current Limit	220Ω from I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coefficient		●		−0.3		%/°C
	Switch OFF Leakage Current	Measured at SW1 Pin, V_{SW1} = 12V			1	10	µA
	Maximum Excursion Below GND	I_{SW1} ≤ 10µA, Switch OFF			−400	−350	mV

V_{IN} = 3V, −55°C ≤ T_A ≤ 125°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1111M MIN	LT1111M TYP	LT1111M MAX	UNITS
I_Q	Quiescent Current	Switch OFF	●		300	500	µA
f_{OSC}	Oscillator Frequency		●	45	72	100	kHz
DC	Duty Cycle: Step-Up Mode Step-Down Mode	Full Load	● ●	40 20	50	62 55	% %
t_{ON}	Switch ON Time: Step-Up Mode Step-Down Mode	I_{LIM} Tied to V_{IN} V_{OUT} = 5V, V_{IN} = 12V	● ●	5 3	7	11 9	µs µs
	Reference Line Regulation	2V ≤ V_{IN} ≤ 5V, 25°C ≤ T_A ≤ 125°C 2.4V ≤ V_{IN} ≤ 5V, T_A = −55°C			0.2	0.4 0.8	%/V %/V
V_{SAT}	SW Saturation Voltage, Step-Up Mode	0°C ≤ T_A ≤ 125°C, I_{SW} = 500mA, T_A = −55°C, I_{SW} = 400mA			0.5	0.65	V
	SW Saturation Voltage, Step-Down Mode	V_{IN} = 12V, 0°C ≤ T_A ≤ 125°C I_{SW} = 500mA T_A = −55°C				1.5 2.0	V V

V_{IN} = 3V, 0°C ≤ T_A ≤ 70°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1111C MIN	LT1111C TYP	LT1111C MAX	UNITS
I_Q	Quiescent Current	Switch OFF	●	300		450	µA
f_{OSC}	Oscillator Frequency		●	54	72	95	kH
DC	Duty Cycle: Step-Up Mode Step-Down Mode	Full Load	● ●	43 24	50 34	59 50	% %
t_{ON}	Switch ON Time: Step-Up Mode Step-Down Mode	I_{LIM} Tied to V_{IN} V_{OUT} = 5V, V_{IN} = 12V	● ●	5.0 3.3	7 5	9.0 7.8	µs µs
	Reference Line Regulation	2V ≤ V_{IN} ≤ 5V	●		0.2	0.7	%/V
V_{SAT}	SW Saturation Voltage, Step-Up Mode SW Saturation Voltage, Step-Down Mode	V_{IN} = 3V, I_{SW} = 650mA V_{IN} = 12V, I_{SW} = 650mA	● ●		0.5 1.1	0.65 1.50	V V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.20V to 1.30V range.

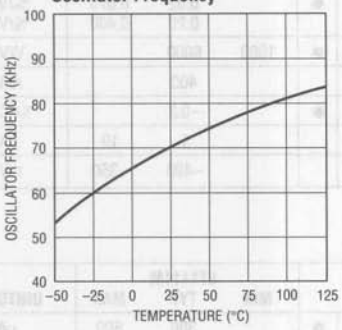
Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

Note 3: 100k resistor connected between a 5V source and the A0 pin.

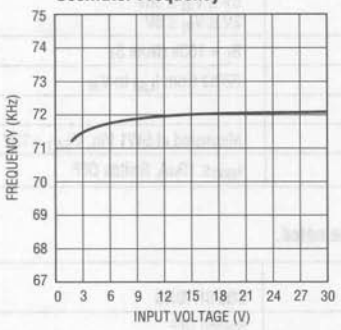
4

TYPICAL PERFORMANCE CHARACTERISTICS

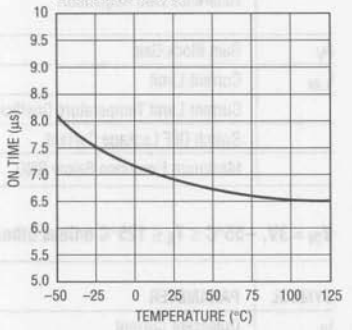
Oscillator Frequency



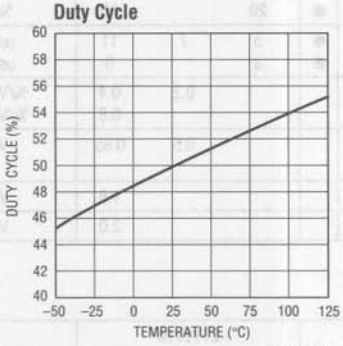
Oscillator Frequency



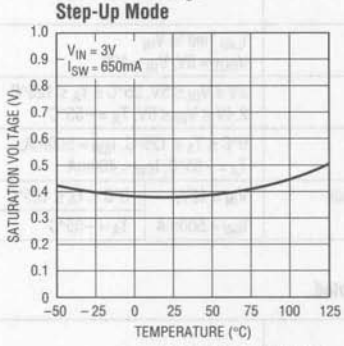
Switch ON Time



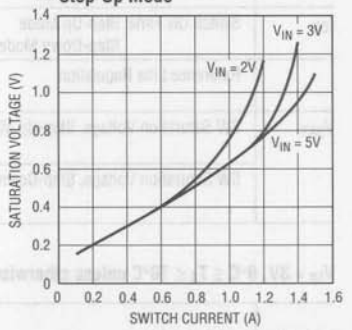
Duty Cycle



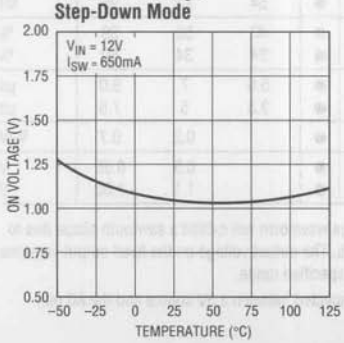
Saturation Voltage Step-Up Mode



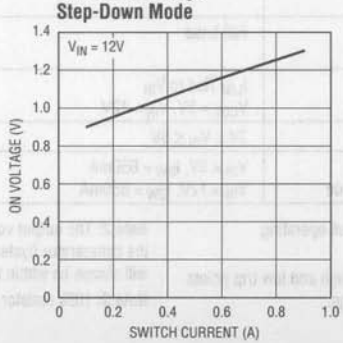
Saturation Voltage Step-Up Mode



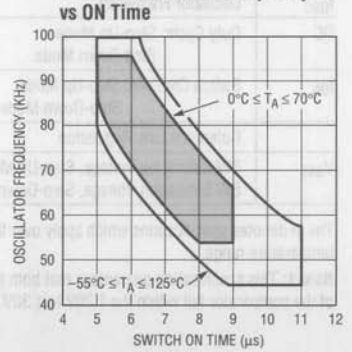
Switch ON Voltage Step-Down Mode



Switch ON Voltage Step-Down Mode

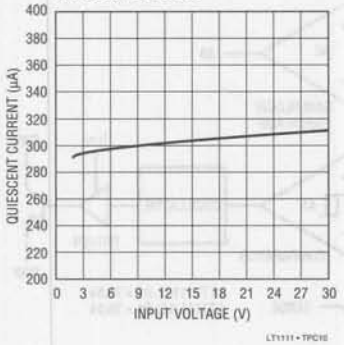


Minimum/Maximum Frequency vs ON Time

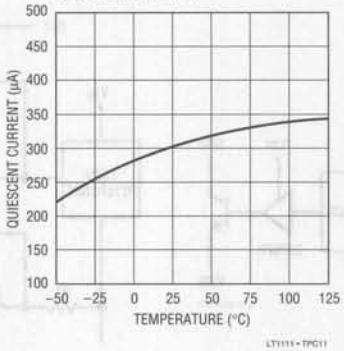


TYPICAL PERFORMANCE CHARACTERISTICS

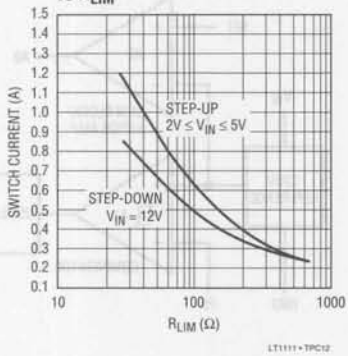
Quiescent Current



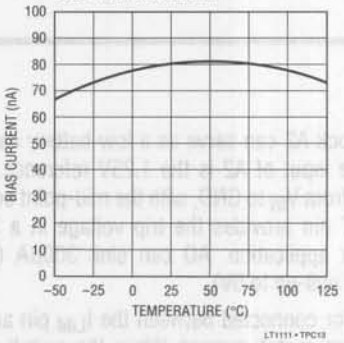
Quiescent Current



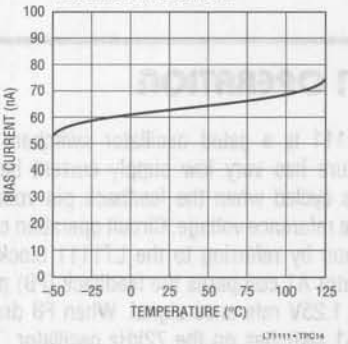
Maximum Switch Current vs R_{LIM}



Set Pin Bias Current



Feedback Bias Current



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input Supply Voltage.

SW1 (Pin 3): Collector of Power Transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of Power Transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

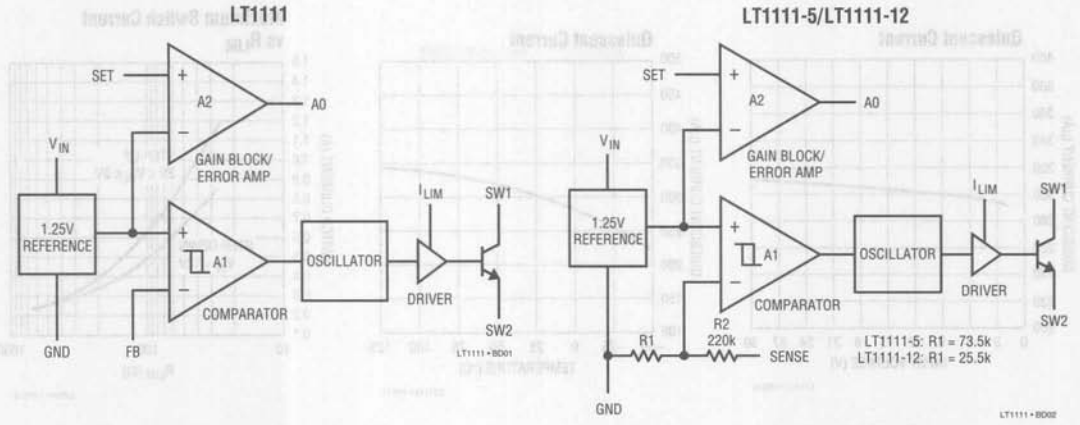
GND (Pin 5): Ground.

A0 (Pin 6): Auxiliary Gain Block (GB) Output. Open collector, can sink 300µA.

SET (Pin 7): GB Input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.25V reference.

FB/SENSE (Pin 8): On the LT1111 (adjustable) this pin goes to the comparator input. On the LT1111-5 and LT1111-12, this pin goes to the internal application resistor that sets output voltage.

BLOCK DIAGRAMS



LT1111 OPERATION

The LT1111 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1111 block diagram. Comparator A1 compares the feedback (FB) pin voltage with the 1.25V reference signal. When FB drops below 1.25V, A1 switches on the 72kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator output is low, the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 300µA.

The oscillator is set internally for 7µs ON time and 7µs OFF time, optimizing the device for circuits where V_{OUT} and V_{IN} differ by roughly a factor of 2. Examples include a 3V to 5V step-up converter or a 9V to 5V step-down converter.

Gain block A2 can serve as a low-battery detector. The negative input of A2 is the 1.25V reference. A resistor divider from V_{IN} to GND, with the mid-point connected to the SET pin provides the trip voltage in a low-battery detector application. AO can sink 300µA (use a 22k resistor pull-up to 5V).

A resistor connected between the I_{LIM} pin and V_{IN} sets maximum switch current. When the switch current exceeds the set value, the switch cycle is prematurely terminated. If current limit is not used, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current limit circuitry is approximately 1µs.

In step-up mode the switch emitter (SW2) is connected to ground and the switch collector (SW1) drives the inductor; in step-down mode the collector is connected to V_{IN} and the emitter drives the inductor.

The LT1111-5 and LT1111-12 are functionally identical to the LT1111. The -5 and -12 versions have on-chip voltage setting resistors for fixed 5V or 12V outputs. Pin 8 on the fixed versions should be connected to the output. No external resistors are needed.

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Inductor Selection — General

A DC/DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch-on time. The inductance must also be high enough so maximum current ratings of the LT1111 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not saturate. At power levels generally encountered with LT1111 based designs, small surface mount ferrite core units with saturation current ratings in the 300mA to 1A range and DCR less than 0.4Ω (depending on application) are adequate. Lastly, the inductor must have sufficiently low DC resistance so excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem. Minimum and maximum input voltage, output voltage and output current must be established before an inductor can be selected.

Inductor Selection — Step-Up Converter

In a step-up, or boost converter (Figure 4), power generated by the inductor makes up the difference between input and output. Power required from the inductor is determined by:

$$P_L = (V_{OUT} + V_D - V_{IN\ MIN})(I_{OUT}) \quad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than:

$$P_L/f_{OSC} \quad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to:

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (03)$$

where R′ is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation:

$$I_L(t) = \frac{V_{IN}}{L}t \quad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch-on time from the LT1111 specification table (typically 7µs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch-on time can be calculated as:

$$E_L = \frac{1}{2}LI_{PEAK}^2 \quad (05)$$

E_L must be greater than P_L/f_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 60mA is to be generated from a 4.5V to 8V input. Recalling equation (01),

$$P_L = (12V + 0.5V - 4.5V)(60mA) = 480mW \quad (06)$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{480mW}{72kHz} = 6.7\mu J \quad (07)$$

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Picking an inductor value of 47µH with 0.2Ω DCR results in a peak switch current of:

$$I_{PEAK} = \frac{4.5V}{1.0\Omega}\left(1 - e^{\frac{-1.0\Omega \times 7\mu s}{47\mu H}}\right) = 623mA. \quad (08)$$

Substituting I_{PEAK} into Equation 04 results in:

$$E_L = \frac{1}{2}(47\mu H)(0.623A)^2 = 9.1\mu J \quad (09)$$

Since 9.1µJ > 6.7µJ, the 47µH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.5A. If the calculated peak current exceeds this, consider using the LT1110. The 70% duty cycle of the LT1110 allows more energy per cycle to be stored in the inductor, resulting in more output power.

A resistor can be added in series with the I_{LIM} pin to invoke switch current limit. The resistor should be picked so the calculated I_{PEAK} at minimum V_{IN} is equal to the Maximum Switch Current (from Typical Performance Characteristic curves). Then, as V_{IN} increases, switch current is held constant, resulting in increasing efficiency.

Inductor Selection — Step-Down Converter

The step-down case (Figure 5) differs from the step-up in that the inductor current flows through the load during both the charge and discharge periods of the inductor. Current through the switch should be limited to ~650mA in this mode. Higher current can be obtained by using an external switch (see Figure 6). The I_{LIM} pin is the key to successful operation over varying inputs.

After establishing output voltage, output current and input voltage range, peak switch current can be calculated by the formula:

$$I_{PEAK} = \frac{2I_{OUT}}{DC}\left[\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right] \quad (10)$$

where DC = duty cycle (0.50)

V_{SW} = switch drop in step-down mode

V_D = diode drop (0.5V for a 1N5818)

I_{OUT} = output current

V_{OUT} = output voltage

V_{IN} = minimum input voltage

V_{SW} is actually a function of switch current which is in turn a function of V_{IN}, L, time, and V_{OUT}. To simplify, 1.5V can be used for V_{SW} as a very conservative value.

Once I_{PEAK} is known, inductor value can be derived from:

$$L = \frac{V_{IN\,MIN} - V_{SW} - V_{OUT}}{I_{PEAK}} \times t_{ON} \quad (11)$$

where t_{ON} = switch-on time (7µs).

Next, the current limit resistor R_{LIM} is selected to give I_{PEAK} from the R_{LIM} Step-Down Mode curve. The addition of this resistor keeps maximum switch current constant as the input voltage is increased.

As an example, suppose 5V at 300mA is to be generated from a 12V to 24V input. Recalling Equation (10),

$$I_{PEAK} = \frac{2(300mA)}{0.50}\left[\frac{5 + 0.5}{12 - 1.5 + 0.5}\right] = 600mA \quad (12)$$

Next, inductor value is calculated using Equation (11):

$$L = \frac{12 - 1.5 - 5}{600mA} 7\mu s = 64\mu H. \quad (13)$$

Use the next lowest standard value (56µH).

Then pick R_{LIM} from the curve. For I_{PEAK} = 600mA, R_{LIM} = 56Ω.

Inductor Selection — Positive-to-Negative Converter

Figure 7 shows hookup for positive-to-negative conversion. All of the output power must come from the inductor. In this case,

$$P_L = (|V_{OUT}| + V_D)(I_{OUT}) \quad (14)$$

In this mode the switch is arranged in common collector or step-down mode. The switch drop can be modeled as a 0.75V source in series with a 0.65Ω resistor. When the

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switch closes, current in the inductor builds according to

$$I_L(t) = \frac{V_L}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \quad (15)$$

where $R' = 0.65\Omega + DCR_L$

$V_L = V_{IN} - 0.75V$

As an example, suppose –5V at 50mA is to be generated from a 4.5V to 5.5V input. Recalling Equation (14),

$$P_L = (|-5V| + 0.5V)(50mA) = 275mW \quad (16)$$

Energy required from the inductor is:

$$\frac{P_L}{f_{OSC}} = \frac{275mW}{72kHz} = 3.8\mu J. \quad (17)$$

Picking an inductor value of 56µH with 0.2Ω DCR results in a peak switch current of:

$$I_{PEAK} = \frac{(4.5V - 0.75V)}{(0.65\Omega + 0.2\Omega)}\left(1 - e^{\frac{-0.85\Omega \times 7\mu s}{56\mu H}}\right) = 445mA. \quad (18)$$

Substituting I_{PEAK} into Equation (04) results in:

$$E_L = \frac{1}{2}(56\mu H)(0.445A)^2 = 5.54\mu J. \quad (19)$$

Since 5.54µJ > 3.82µJ, the 56µH inductor will work.

With this relatively small input range, R_{LIM} is not usually necessary and the I_{LIM} pin can be tied directly to V_{IN}. As in the step-down case, peak switch current should be limited to ~650mA.

Capacitor Selection

Selecting the right output capacitor is almost as important as selecting the right inductor. A poor choice for a filter capacitor can result in poor efficiency and/or high output ripple. Ordinary aluminum electrolytics, while inexpensive and readily available, may have unacceptably poor Equivalent Series Resistance (ESR) and ESL (inductance). There are low ESR aluminum capacitors on the market specifically designed for switch mode DC/DC converters which work much better than general-purpose units. Tantalum capacitors provide still better performance at more expense. We recommend OS-CON capacitors from Sanyo Corporation (San Diego, CA). These units are physically quite small and have extremely low ESR. To illustrate, Figures 1, 2, and 3 show the output voltage of an LT1111 based converter with three 100µF capacitors. The peak switch current is 500mA in all cases. Figure 1 shows a Sprague 501D, 25V aluminum capacitor. V_{OUT} jumps by over 120mV when the switch turns off, followed by a drop in voltage as the inductor dumps into the capacitor. This works out to be an ESR of over 0.24Ω. Figure 2 shows the same circuit, but with a Sprague 150D, 20V tantalum capacitor replacing the aluminum unit. Output jump is now about 35mV, corresponding to an ESR of 0.07Ω. Figure 3 shows the circuit with a 16V OS-CON unit. ESR is now only 0.02Ω.

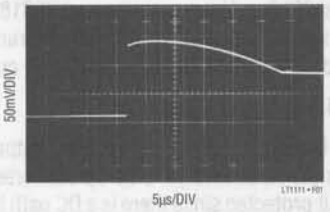

Figure 1. Aluminum

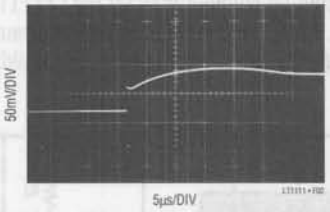

Figure 2. Tantalum

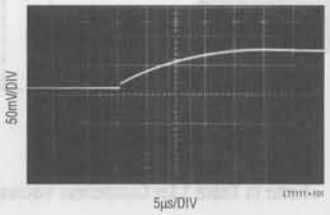

Figure 3. OS-CON

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Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1111 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10μs to 50μs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1111 circuits will be well served by a 1N5818 Schottky diode, or its surface mount equivalent, the MBRS130T3. The combination of 500mV forward drop at 1A current, fast turn ON and turn OFF time, and 4μA to 10μA leakage current fit nicely with LT1111 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA to 5nA range at 25°C and lower cost than a 1N5818. (You can also use them to get your circuit up and running, but beware of destroying the diode at 1A switch currents.)

Step-Up (Boost Mode) Operation

A step-up DC/DC converter delivers an output voltage higher than the input voltage. Step-up converters are not short-circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1111 is shown in Figure 4. The LT1111 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1.

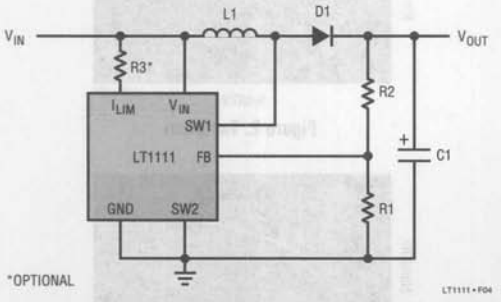

Figure 4. Step-Up Mode Hookup. Refer to Table 1 for Component Values.

At the end of the switch ON time the current in L1 is[1]:

$$I_{PEAK} = \frac{V_{IN}}{L} t_{ON} \quad (20)$$

Immediately after switch turn-off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1111 to keep V_{FB} at the internal reference voltage of 1.25V. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V) \quad (21)$$

Step-Down (Buck Mode) Operation

A step-down DC/DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1111 based step-down converter is shown in Figure 5.

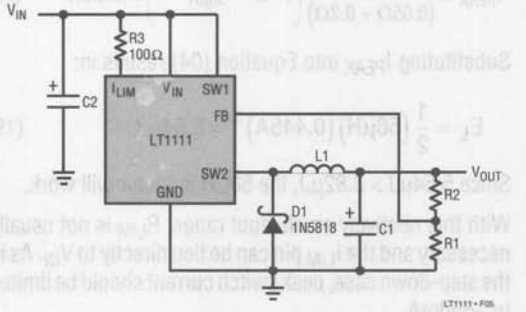

Figure 5. Step-Down Mode Hookup

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to:

$$I_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON} \quad (22)$$

Note 1: This simple expression neglects the effect of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

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When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE*. The voltage at SW2 must never be allowed to go below –0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to –0.8V, causing potentially destructive power dissipation inside the LT1111. Output voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V) \qquad (23)$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 100Ω resistor programs the switch to turn off when the current reaches approximately 700mA. When using the LT1111 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

Higher Current Step-Down Operation

Output current can be increased by using a discrete PNP pass transistor as shown in Figure 6. R1 serves as a current limit sense. When the voltage drop across R1 equals a V_{BE}, the switch turns off. For temperature compensation a Schottky diode can be inserted in series with the I_{LIM} pin. This also lowers the maximum drop across R1 to $V_{BE} - V_D$, increasing efficiency. As shown, switch current is limited to 2A. Inductor value can be calculated based on formulas in the "Inductor Selection — Step-Down Converter" section with the following conservative expression for V_{SW}:

$$V_{SW} = V_{R1} + V_{Q1SAT} \approx 1.0V \qquad (24)$$

R2 provides a current path to turn off Q1. R3 provides base drive to Q1. R4 and R5 set output voltage. A PMOS FET can be used in place of Q1 when V_{IN} is between 10V and 20V.

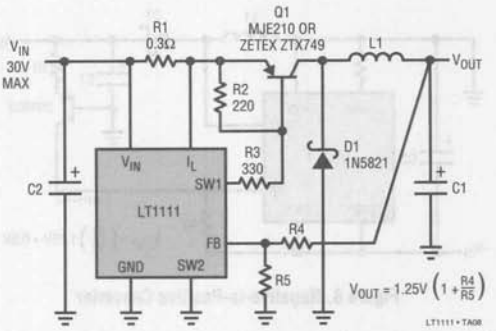


Figure 6. Q1 Permits Higher Current Switching. LT1111 Functions as Controller.

Inverting Configurations

The LT1111 can be configured as a positive-to-negative converter (Figure 7), or a negative-to-positive converter (Figure 8). In Figure 7, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accommodated as in the prior section.

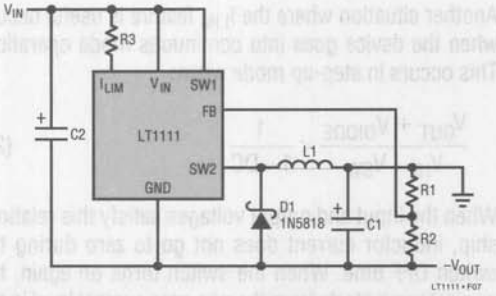


Figure 7. Positive-to-Negative Converter

In Figure 8, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

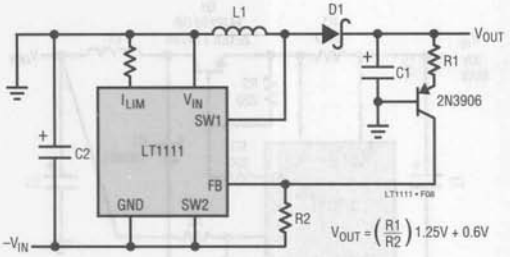


Figure 8. Negative-to-Positive Converter

Using the I_{LIM} Pin

The LT1111 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case wh ere analysis shows the LT1111 must operate at an 800mA peak switch current with a 2V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs I_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when:

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC} \qquad (25)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn-on. As shown in Figure 9, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 10, keeping output ripple to a *minimum*.

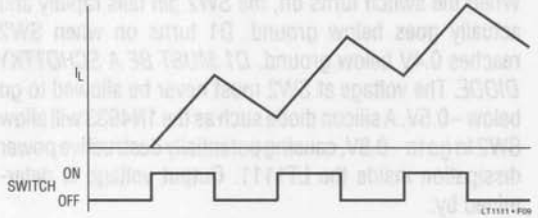


Figure 9. No Current Limit Causes Large Inductor Current Build-Up

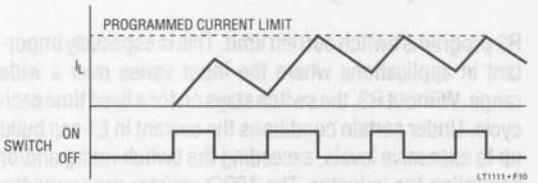


Figure 10. Current Limit Keeps Inductor Current Under Control

Figure 11 details current limit circuitry. Sense transistor Q1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current is passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} sets the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 1µs. The current trip point becomes less accurate for switch ON times less than 3µs. Resistor values programming switch ON time for 1µs or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

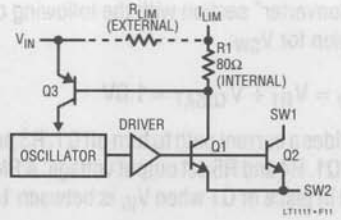


Figure 11. LT1111 Current Limit Circuitry

APPLICATIONS INFORMATION

Using the Gain Block

The gain block (GB) on the LT1111 can be used as an error amplifier, low-battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 1.25V reference. The positive input comes out on the SET pin.

Arrangement of the gain block as a low-battery detector is straightforward. Figure 12 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 33k for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M to 10M range are optimal. However, the addition of R3 will change the trip point.

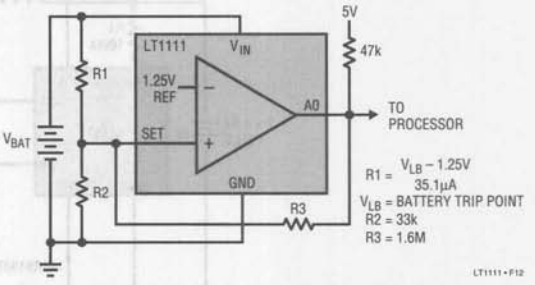


Figure 12. Setting Low-Battery Detector Trip Point

Table 1. Component Selection for Common Converters

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT (MIN)	CIRCUIT FIGURE	INDUCTOR VALUE	INDUCTOR PART NUMBER	CAPACITOR VALUE	NOTES
2 to 3.1	5	90mA	4	15µH	S CD75-750K	33µF	*
2 to 3.1	5	10mA	4	47µH	S CD54-470K, C CTX50-1	10µF	
2 to 3.1	12	30mA	4	15µH	S CD75-150K	22µF	
2 to 3.1	12	10mA	4	47µH	S CD54-470K, C CTX50-1	10µF	
5	12	90mA	4	33µH	S CD75-330K	22µF	
5	12	30mA	4	47µH	S CD75-470K, C CTX50-1	15µF	
6.5 to 11	5	50mA	5	15µH	S CD54-150K	47µF	**
12 to 20	5	300mA	5	56µH	S CD105-560K, C CTX50-4	47µF	**
20 to 30	5	300mA	5	120µH	S CD105-121K, C CTX100-4	47µF	**
5	–5	75mA	6	56µH	S CD75-560K, C CTX50-4	47µF	
12	–5	250mA	6	120µH	S CD105-121K, C CTX100-4	100µF	**

S = Sumida
C = Coiltronics
* Add 47Ω from I_{LIM} to V_{IN}
** Add 220Ω from I_{LIM} to V_{IN}

Table 2. Inductor Manufacturers

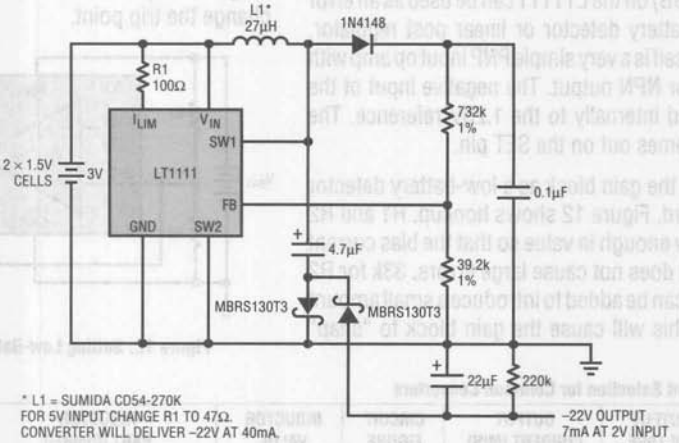
MANUFACTURER	PART NUMBERS
Coiltronics Incorporated 6000 Park of Commerce Blvd. Boca Raton, FL 33487 407-241-7876	CTX100-4 Series Surface Mount
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Sumida Electric Co. USA 708-956-0666	CD54 CDR74 CDR105 Surface Mount

Table 3. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
Sprague Electric Company Lower Main Street Sanford, ME 04073 207-324-4140	150D Solid Tantalums 550D Tantalex
Matsuo 714-969-2491	267 Series Surface Mount

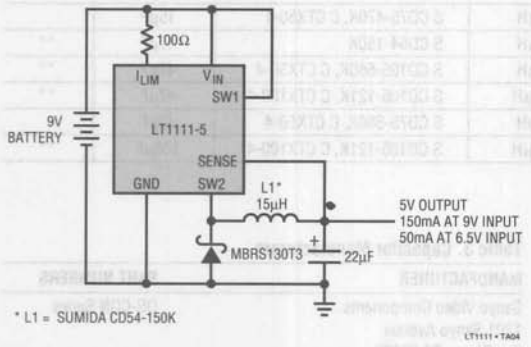
TYPICAL APPLICATIONS

3V to –22V LCD Bias Generator



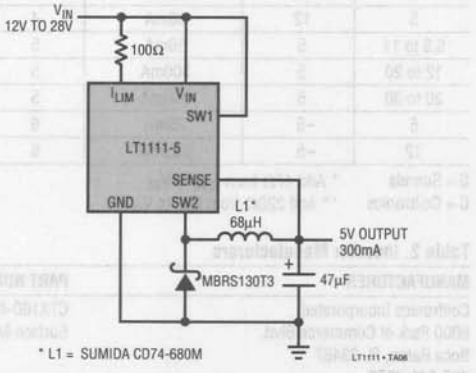
* L1 = SUMIDA CD54-270K
FOR 5V INPUT CHANGE R1 TO 47Ω.
CONVERTER WILL DELIVER –22V AT 40mA.

9V to 5V Step-Down Converter



* L1 = SUMIDA CD54-150K

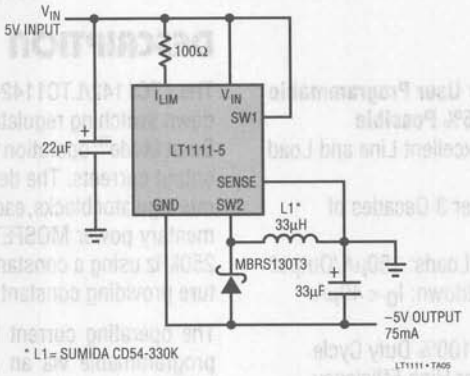
20V to 5V Step-Down Converter



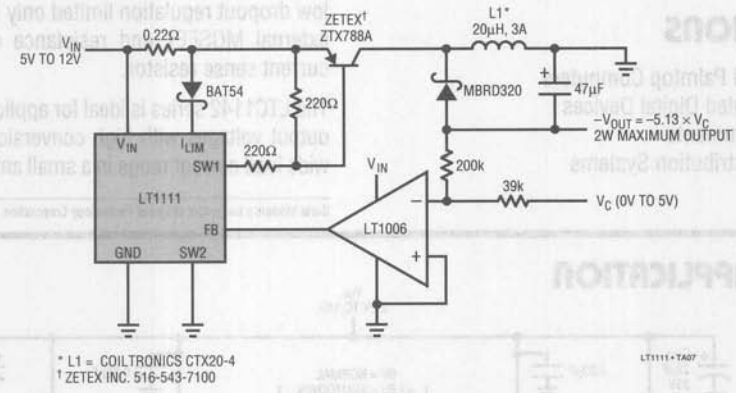
* L1 = SUMIDA CD74-680M

TYPICAL APPLICATIONS

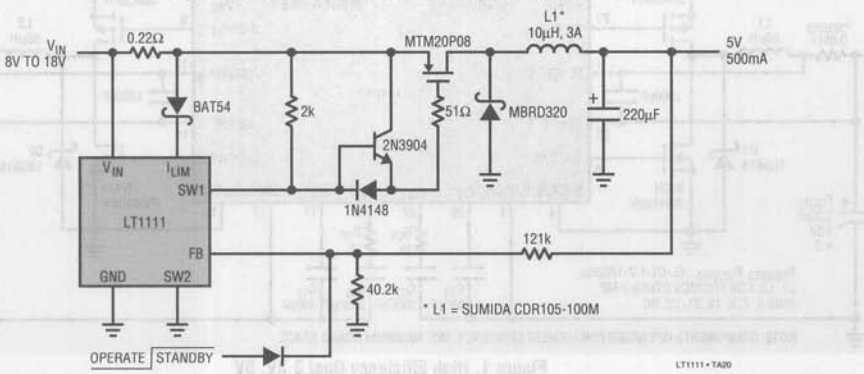
5V to –5V Converter



Voltage Controlled Positive-to-Negative Converter



High Power, Low Quiescent Current Step-Down Converter



Dual High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Dual Outputs: 3.3V and 5V or User Programmable**
- **Ultra-High Efficiency: Over 95% Possible**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over 3 Decades of Output Current
- Low Standby Current at Light Loads: 160μA/Output
- Independent Micropower Shutdown: I_Q < 40μA
- Wide V_{IN} Range: 4V to 20V
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Available in Standard 28-Pin SSOP

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC1142/LTC1142-ADJ are dual synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. The devices are composed of two separate regulator blocks, each driving a pair of external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current mode architecture providing constant ripple current in the inductor.

The operating current level for both regulators is user programmable via an external current sense resistor. Wide input supply range allows operation from 4V to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1142 series is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

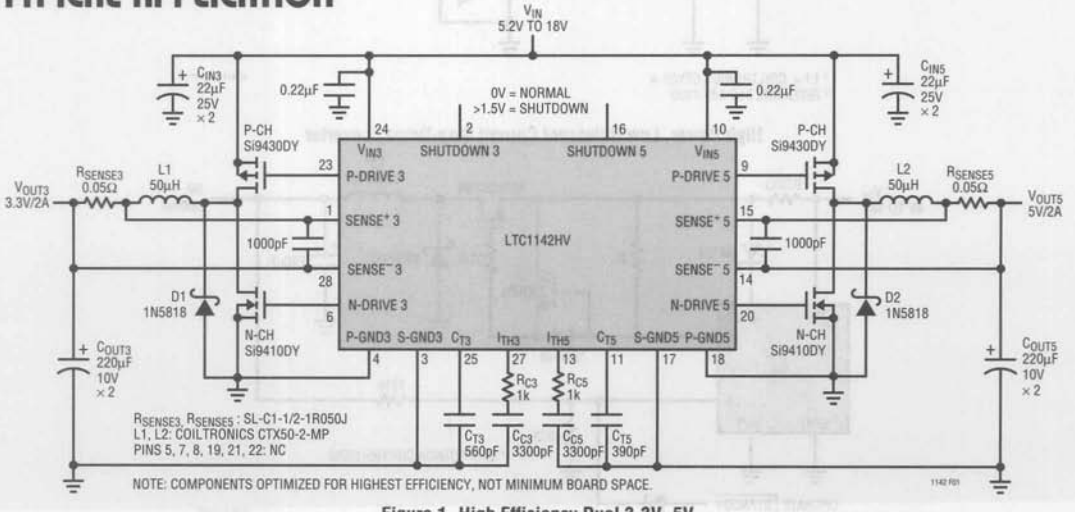


Figure 1. High Efficiency Dual 3.3V, 5V

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pins 10, 24)
- LTC1142 ..... 16V to –0.3V
- LTC1142HV, LTC1142HV-ADJ ..... 20V to –0.3V

Continuous Output Current (Pins 6, 9, 20, 23) 50mA
Sense Voltages (Pins 1, 14, 15, 28)..... 13V to –0.3V
Operating Ambient Temperature Range..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1)..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

G PACKAGE, 28-LEAD SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1142CG
LTC1142HVCG

G PACKAGE, 28-LEAD SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1142HVCG-ADJ

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{10} = V_{24} = 10V, $V_{SHUTDOWN}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_2, V_{16}	Feedback Voltage	LTC1142HV-ADJ Only: V_{10}, V_{24} = 9V	●	1.21	1.25	1.29	V
I_2, I_{16}	Feedback Current	LTC1142HV-ADJ Only	●		0.2	1	µA
V_{OUT}	Regulated Output Voltage	LTC1142, LTC1142HV					
	3.3V Output	I_{LOAD} = 700mA, V_{24} = 9V	●	3.23	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA, V_{10} = 9V	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{10}, V_{24} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation	Figure 1 Circuit					
	3.3V Output	5mA < I_{LOAD} < 2A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2A	●		60	100	mV
	Output Ripple (Burst Mode)	I_{LOAD} = 0A			50		mV_{P-P}
I_{10}, I_{24}	Input DC Supply Current (Note 2)	LTC1142					
	Normal Mode	4V < V_{10}, V_{24} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{24} < 12V, 6V < V_{10} < 12V			160	230	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 4V < V_{10}, V_{24} < 12V			10	20	µA
	Input DC Supply Current (Note 2)	LTC1142HV, LTC1142HV-ADJ					
	Normal Mode	4V < V_{10}, V_{24} < 18V			1.6	2.3	mA
	Sleep Mode	4V < V_{24} < 18V, 6V < V_{10} < 18V			160	250	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 4V < V_{10}, V_{24} < 18V			10	22	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{10} = V_{24}$ = 10V, $V_{SHUTDOWN}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_1 - V_{28}$ $V_{15} - V_{14}$	Current Sense Threshold Voltage	LTC1142HV-ADJ $V_{14} = V_{28}$ = 5V, $V_2 = V_{16} = V_{OUT}/4$ + 25mV (Forced) $V_{14} = V_{28}$ = 5V, $V_2 = V_{16} = V_{OUT}/4$ – 25mV (Forced)	 ●	 130	25 150	 170	mV mV
		LTC1142, LTC1142HV $V_{28} = V_{OUT}$ + 100mV (Forced) $V_{28} = V_{OUT}$ – 100mV (Forced)	 ●	 130	25 150	 170	mV mV
		LTC1142, LTC1142HV $V_{14} = V_{OUT}$ + 100mV (Forced) $V_{14} = V_{OUT}$ – 100mV (Forced)	 ●	 130	25 150	 170	mV mV
$V_{SHUTDOWN}$	Shutdown Pin Threshold			0.6	0.8	2	V
$I_{SHUTDOWN}$	Shutdown Pin Input Current	0V < $V_{SHUTDOWN}$ < 8V, V_{10}, V_{24} = 16V			1.2	5	µA
I_{11}, I_{24}	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT} V_{OUT} = 0V		50	70 2	110 10	µA µA
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 6, 9, 20, 23), V_{10}, V_{24} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_A ≤ 85°C (Note 4), $V_{10} = V_{24}$ = 10V, unless otherwise noted.

V_2, V_{16}	Feedback Voltage	LTC1142HV-ADJ Only: V_{10}, V_{24} = 9V		1.21	1.25	1.29	V
I_2, I_{16}	Feedback Current	LTC1142HV-ADJ Only			0.2	1	µA
V_{OUT}	Regulated Output Voltage 3.3V Output 5V Output	LTC1142, LTC1142HV I_{LOAD} = 700mA, V_{24} = 9V I_{LOAD} = 700mA, V_{10} = 9V		 3.17 4.85	 3.33 5.05	 3.40 5.20	 V V
I_{10}, I_{24}	Input DC Supply Current (Note 2) Normal Mode Sleep Mode Shutdown	LTC1142 4V < V_{10}, V_{24} < 12V 4V < V_{24} < 12V, 6V < V_{10} < 12V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{10}, V_{24} < 12V			 1.6 160 10	 2.4 260 22	 mA µA µA
	Input DC Supply Current (Note 2) Normal Mode Sleep Mode Shutdown	LTC1142HV-ADJ, LTC1142HV 4V < V_{10}, V_{24} < 18V 4V < V_{24} < 18V, 6V < V_{10} < 18V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{10}, V_{24} < 12V			 1.6 160 10	 2.6 280 24	 mA µA µA
$V_1 - V_{28}$ $V_{15} - V_{14}$	Current Sense Threshold Voltage	LTC1142HV-ADJ $V_{14} = V_{28}$ = 5V, $V_2 = V_{16} = V_{OUT}/4$ + 25mV (Forced) $V_{14} = V_{28}$ = 5V, $V_2 = V_{16} = V_{OUT}/4$ – 25mV (Forced)		 130	25 150	 170	mV mV
		LTC1142, LTC1142HV $V_{28} = V_{OUT}$ + 100mV (Forced) $V_{28} = V_{OUT}$ – 100mV (Forced)		 125	25 150	 175	mV mV
		LTC1142, LTC1142HV $V_{14} = V_{OUT}$ + 100mV (Forced) $V_{14} = V_{OUT}$ – 100mV (Forced)		 125	25 150	 175	mV mV
$V_{SHUTDOWN}$	Shutdown Pin Threshold			0.55	0.8	2	V
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA		3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1142CG: $T_J = T_A + (P_D \times 95°C/W)$

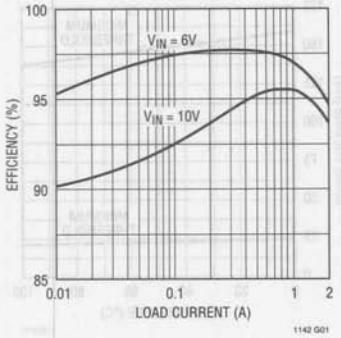
Note 2: This current is for one regulator block. Total supply current is the sum of pins 10 and 24 currents. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

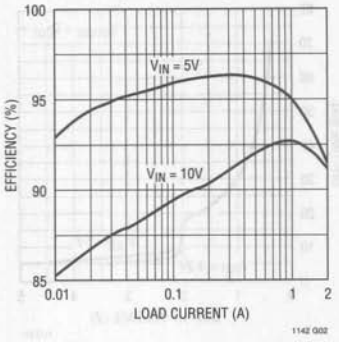
Note 4: The LTC1142/LTC1142JV-ADJ/LTC1142HV are not tested and quality-assurance sampled at –40°C to 85°C. These specifications are guaranteed by design and/or correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

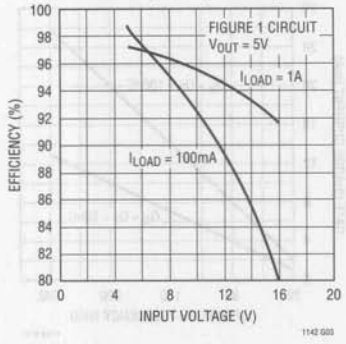
5V Output Efficiency



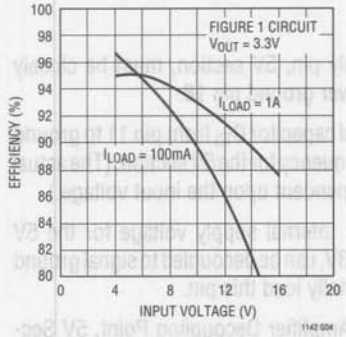
3.3V Output Efficiency



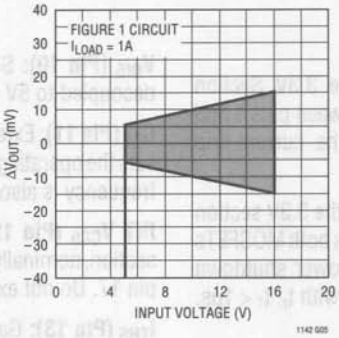
5V Efficiency vs Input Voltage



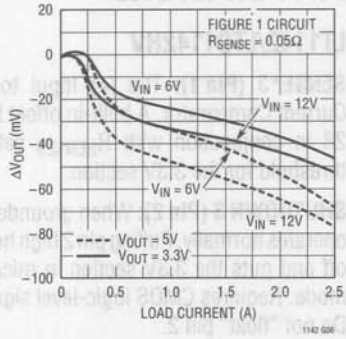
3.3V Efficiency vs Input Voltage



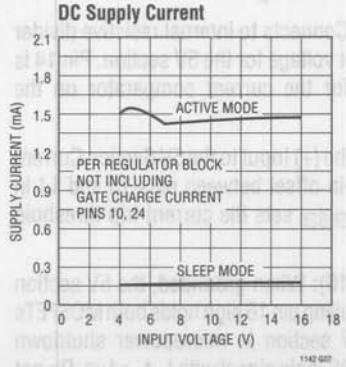
Line Regulation



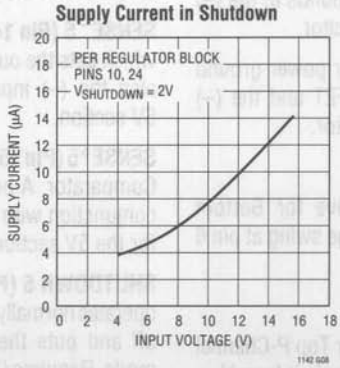
Load Regulation



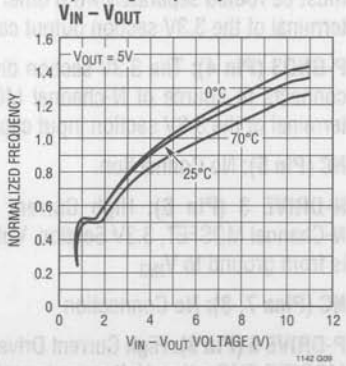
DC Supply Current



Supply Current in Shutdown



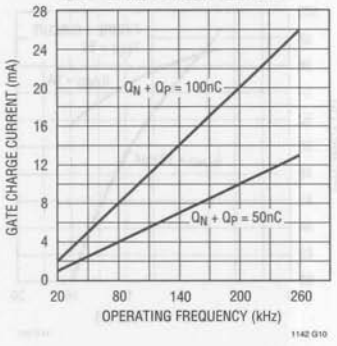
Operating Frequency vs $V_{IN} - V_{OUT}$



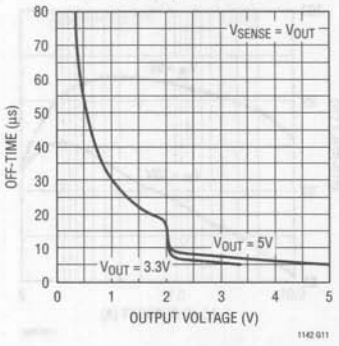
4

TYPICAL PERFORMANCE CHARACTERISTICS

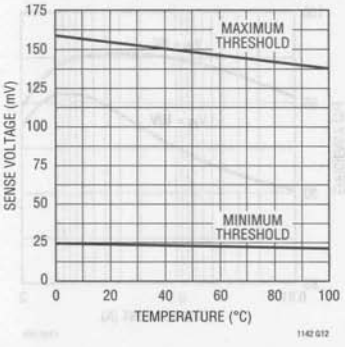
Gate Charge Supply Current



Off-Time vs Output Voltage



Current Sense Threshold Voltage



PIN FUNCTIONS

LT1142/LTC1142HV

SENSE⁺3 (Pin 1): The (+) Input to the 3.3V Section Current Comparator. A built-in offset between pins 1 and 28 in conjunction with R_{SENSE3} sets the current trip threshold for the 3.3V section.

SHUTDOWN 3 (Pin 2): When grounded, the 3.3V section operates normally. Pulling pin 2 high holds both MOSFETs off and puts the 3.3V section in micropower shutdown mode. Requires CMOS logic-level signal with t_r, $t_f < 1\mu s$. Do not "float" pin 2.

S-GND3 (Pin 3): The 3.3V section small-signal ground must be routed separately from other grounds to the (–) terminal of the 3.3V section output capacitor.

P-GND3 (Pin 4): The 3.3V section driver power ground connects to source of N-channel MOSFET and the (–) terminal of the 3.3V section input capacitor.

NC (Pin 5): No Connection.

N-DRIVE 3 (Pin 6): High Current Drive for Bottom N-Channel MOSFET, 3.3V Section. Voltage swing at pin 6 is from ground to V_{IN3}.

NC (Pins 7, 8): No Connection.

P-DRIVE 5 (Pin 9): High Current Drive for Top P-Channel MOSFET, 5V Section. Voltage swing at this pin is from V_{IN5} to ground.

V_{IN5} (Pin 10): Supply pin, 5V section, must be closely decoupled to 5V power ground pin 18.

C_{T5} (Pin 11): External capacitor C_{T5} from pin 11 to ground sets the operating frequency for the 5V section. (The actual frequency is also dependent upon the input voltage.)

INT V_{CC5} (Pin 12) : Internal supply voltage for the 5V section, nominally 3.3V, can be decoupled to signal ground pin 17. Do not externally load this pin.

I_{TH5} (Pin 13): Gain Amplifier Decoupling Point, 5V Section. The 5V section current comparator threshold increases with the pin 13 voltage.

SENSE⁻5 (Pin 14): Connects to internal resistive divider which sets the output voltage for the 5V section. Pin 14 is also the (–) input for the current comparator on the 5V section.

SENSE⁺5 (Pin 15): The (+) Input to the 5V Section Current Comparator. A built-in offset between pins 15 and 14 in conjunction with R_{SENSE5} sets the current trip threshold for the 5V section.

SHUTDOWN 5 (Pin 16): When grounded, the 5V section operates normally. Pulling pin 16 high holds both MOSFETs off and puts the 5V section in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not "float" pin 16.

PIN FUNCTIONS

S-GND5 (Pin 17): The 5V section small-signal ground must be routed separately from other grounds to the (–) terminal of the 5V section output capacitor.

P-GND5 (Pin 18): The 5V section driver power ground connects to source of N-channel MOSFET and the (–) terminal of the 5V section input capacitor.

NC (Pin 19): No Connection.

N-DRIVE 5 (Pin 20): High Current Drive for Bottom N-Channel MOSFET, 5V Section. Voltage swing at pin 20 is from ground to V_{IN5}.

NC (Pins 21, 22): No Connection.

P-DRIVE 3 (Pin 23): High Current Drive for Top P-Channel MOSFET, 3.3V Section. Voltage swing at this pin is from V_{IN3} to ground.

V_{IN3} (Pin 24): Supply pin, 3.3V section, must be closely decoupled to 3.3V power ground pin 4.

C_{T3} (Pin 25): External capacitor C_{T3} from pin 25 to ground sets the operating frequency for the 3.3V section. (The actual frequency is also dependent upon the input voltage.)

INT V_{CC3} (Pin 26): Internal supply voltage for the 3.3V section, nominally 3.3V, can be decoupled to signal ground pin 3. Do not externally load this pin.

I_{TH3} (Pin 27): Gain Amplifier Decoupling Point, 3.3V Section. The 3.3V section current comparator threshold increases with the pin 27 voltage.

SENSE$^-$3 (Pin 28): Connects to internal resistive divider which sets the output voltage for the 3.3V section. Pin 28 is also the (–) input for the current comparator on the 3.3V section.

LT1142HV-ADJ

SENSE$^+$1 (Pin 1): The (+) Input to the Section 1 Current Comparator. A built-in offset between pins 1 and 28 in conjunction with R_{SENSE1} sets the current trip threshold for this section.

V_{FB1} (Pin 2): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 1.

SHUTDOWN 1 (Pin 3): When grounded, the section 1 regulator operates normally. Pulling pin 3 high holds both MOSFETs off and puts this section in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not "float" pin 3.

S-GND1 (Pin 4): The section 1 small-signal ground must be routed separately from other grounds to the (–) terminal of the section 1 output capacitor.

P-GND1 (Pin 5): The section 1 driver power ground connects to source of N-channel MOSFET and the (–) terminal of the section 1 input capacitor.

N-DRIVE 1 (Pin 6): High Current Drive for Bottom N-Channel MOSFET, Section 1. Voltage swing at pin 6 is from ground to V_{IN1}.

NC (Pins 7, 8): No Connection.

P-DRIVE 2 (Pin 9): High Current Drive for Top P-Channel MOSFET, Section 2. Voltage swing at this pin is from V_{IN2} to ground.

V_{IN2} (Pin 10): Supply pin, section 2, must be closely decoupled to section 2 power ground pin 19.

C_{T2} (Pin 11): External capacitor C_{T2} from pin 11 to ground sets the operating frequency for the section 2. (The actual frequency is also dependent upon the input voltage.)

INT V_{CC2} (Pin 12) : Internal supply voltage for section 2, nominally 3.3V, can be decoupled to signal ground pin 18. Do not externally load this pin.

I_{TH2} (Pin 13): Gain Amplifier Decoupling Point, Section 2. The section 2 current comparator threshold increases with the pin 13 voltage.

SENSE$^-$2 (Pin 14): Connects (–) input for the current comparator on section 2.

SENSE$^+$2 (Pin 15): The (+) Input to the Section 2 Current Comparator. A built-in offset between pins 15 and 14 in conjunction with R_{SENSE2} sets the current trip threshold for this section.

V_{FB2} (Pin 16): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 2.

PIN FUNCTIONS

SHUTDOWN 2 (Pin 17): When grounded, the section 2 regulator operates normally. Pulling pin 17 high holds both MOSFETs off and puts section 2 in micropower shutdown mode. Requires CMOS logic signal with t_r, t_f < 1µs. Do not "float" pin 17.

S-GND2 (Pin 18): The section 2 small-signal ground must be routed separately from other grounds to the (–) terminal of the section 2 output capacitor.

P-GND2 (Pin 19): The section 2 driver power ground connects to source of the N-channel MOSFET and the (–) terminal of the section 2 input capacitor.

N-DRIVE 2 (Pin 20): High Current Drive for Bottom N-Channel MOSFET, Section 2. Voltage swing at pin 20 is from ground to V_{IN2}.

NC (Pins 21, 22): No Connection.

P-DRIVE 1 (Pin 23): High Current Drive for Top P-Channel MOSFET, Section 1. Voltage swing at this pin is from V_{IN1} to ground.

V_{IN1} (Pin 24): Supply Pin, Section 1. Must be closely decoupled to section 1 power ground pin 5.

C_{T1} (Pin 25): External capacitor C_{T1} from pin 25 to ground sets the operating frequency for section 1. (The actual frequency is also dependent upon the input voltage.)

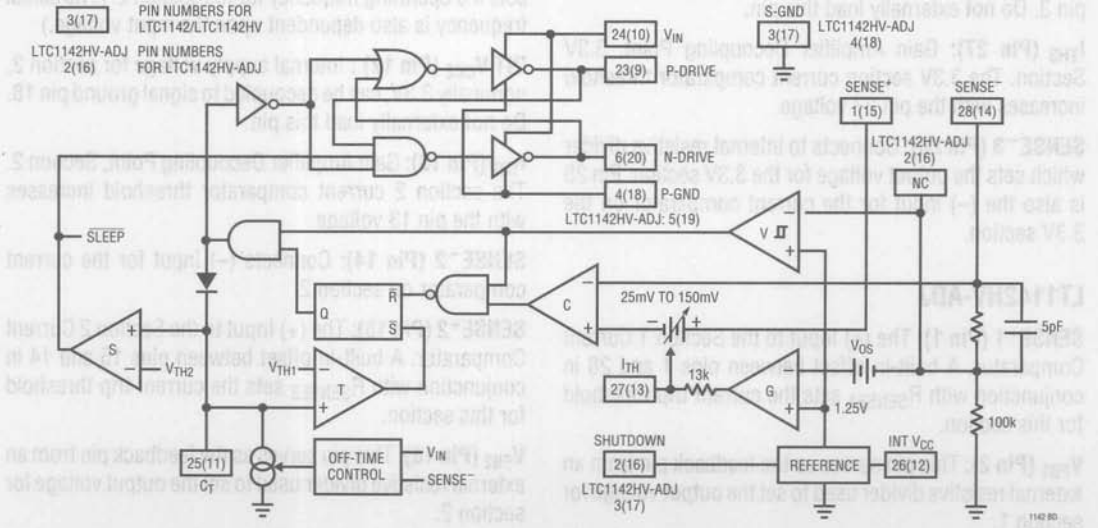
INT V_{CC1} (Pin 26): Internal supply voltage for section 1, nominally 3.3V, can be decoupled to signal ground pin 4. Do not externally load this pin.

I_{TH1} (Pin 27): Gain Amplifier Decoupling Point, Section 1. The section 1 current comparator threshold increases with the pin 27 voltage.

SENSE⁻1 (Pin 28): Connects to the (–) input for the current comparator on section 1.

FUNCTIONAL DIAGRAM

Only one regulator block shown. Pin numbers are for 3.3V (5V) sections for LTC1142, and V_{OUT1} (V_{OUT2}) for LTC1142HV-ADJ.



OPERATION Refer to Functional Diagram

The LTC1142 series consists of two individual regulator blocks, each using current mode, constant off-time architectures to synchronously switch an external pair of complementary power MOSFETs. The two regulators are internally set to provide output voltages of 3.3V and 5V for the LTC1142. The LTC1142HV-ADJ is configured to provide two user selectable output voltages, each set by external resistor dividers. Operating frequency is individually set on each section by the external capacitors at C_T pins 11 and 25.

The output voltage is sensed by an internal voltage divider connected to Sense$^-$ pin 28 (14) (LTC1142) or external divider returned to V_{FB} pin 2 (16) (LTC1142HV-ADJ). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1142 series automatically switches between two modes of operation, Burst Mode and continuous mode. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 1 (15) and 28 (14) connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 25 (11) is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage [measured by pin 28 (14)] to model the inductor current, which decays at a rate that is also proportional to the output voltage. While the timing capacitor is discharging, the N-drive output goes to V_{IN}, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-drive output to go low (turning off the N-channel MOSFET) and the P-drive output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage [pin 27(13)] to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160μA (for one regulator block). The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-drive output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low while the N-drive output is high.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle) providing low dropout operation with $V_{OUT} \sim V_{IN}$.

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The basic LTC1142 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the 3.3V and 5V sections in the LTC1142 are identical and similarly section 1 and section 2 in the LTC1142HV-ADJ are identical, the process of component selection is the same for both sections. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 20V.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1142 current comparators have a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency section). Solving for R_{SENSE} and allowing a margin for variations in the LTC1142 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1142 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

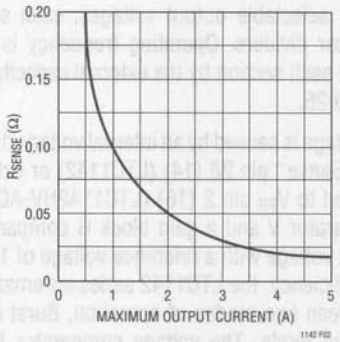

Figure 2. Selecting R_{SENSE}

L and C_T Selection for Operating Frequency

Each regulator section of the LTC1142 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{2.6 \times 10^4 \times f}$$

Assumes $V_{IN} = 2V_{OUT}$, Figure 1 circuit.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations section). The complete expression for operating frequency of the circuit in Figure 1 is given by:

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$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input-to-output voltage differential drops below 1.5V for a particular section, the LTC1142 reduces t_{OFF} in that section by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

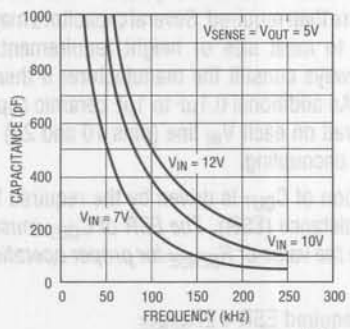

Figure 3. Timing Capacitor Value

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1142 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, molypermalloy (MPP), or Kool Mμ® cores. Lower cost powdered iron cores provide suitable performance, but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies, but it is quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corporation which do not increase the height significantly.

Power MOSFET and D1, D2 Selection

Two external power MOSFETs must be selected for use with each section of the LTC1142: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on-resistance $R_{DS(ON)}$.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8V, standard threshold MOSFETs

Kool Mμ is a registered trademark of Magnetics, Inc.

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($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are strongly recommended. When logic-level MOSFETs are used, the LTC1142 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1142 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_P}{V_{OUT} \times I_{MAX}^2 \times (1+\delta_P)}$$

$$\text{N-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_N}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times (1+\delta_N)}$$

where P_P and P_N are the allowable power dissipations and δ_P and δ_N are the temperature dependencies of $R_{DS(ON)}$. P_P and P_N will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but δ = 0.007/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diodes D1 and D2 shown in Figure 1 only conduct during the dead-time between the conduction of the respective power MOSFETs. The sole purpose of D1 and D2 is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 and D2 are omitted). Therefore, D1 and D2 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case conditon is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on each V_{IN} line (pins 10 and 24) for high frequency decoupling.

The selection of C_{OUT} is driven by the required Effective Series Resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1142:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

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In surface mount applications multiple capacitors may have to be parallel to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1142 would normally be in continuous operation. The output remains in regulation at all times.

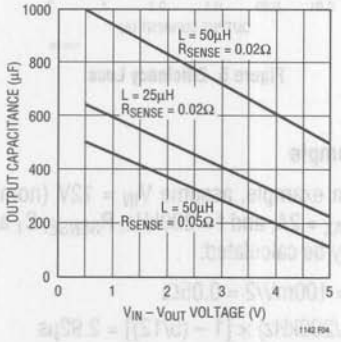

Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The pin 27 (13) external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1142 circuits:

1. LTC1142 DC bias current
2. MOSFET gate charge current
3. I^2R losses

1. The DC supply current is the current which flows into V_{IN} (pin 24 for the 3.3V section, pin 10 for the 5V section) less the gate charge current. For V_{IN} = 10V the LTC1142 DC supply current for each section is 160µA with no load, and increases proportionally with load up

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to a constant 1.6mA after the LTC1142 has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATE(CHG)} = f(Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATE(CHG)}$ = 7.5mA in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.1\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

Figure 5 shows how the efficiency losses in one section of a typical LTC1142 regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

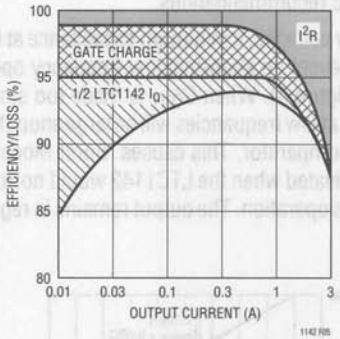

Figure 5. Efficiency Loss

Design Example

As a design example, assume V_{IN} = 12V (nominal), 5V section, I_{MAX} = 2A, and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/2 = 0.05\Omega$

$t_{OFF} = (1/200kHz) \times [1 - (5/12)] = 2.92\mu s$

$C_{T5} = 2.92\mu s/(1.3 \times 10^4) = 220pF$

$L2_{MIN} = 5.1 \times 10^5 \times 0.05\Omega \times 220pF \times 5V = 28\mu H$

Assume that the MOSFET dissipations are to be limited to $P_N = P_P$ = 250mW.

If T_A = 50°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = \delta_N = 0.007(63 - 25) = 0.27$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

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$$\text{P-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2(1.27)} = 0.12\Omega$$

$$\text{N-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2(1.27)} = 0.085\Omega$$

The P-channel requirement can be met by a Si9430DY, while the N-channel requirement is exceeded by a Si9410DY. Note that the most stringent requirement for the N-channel MOSFET is with $V_{OUT} = 0$ (i.e., short circuit). During a continuous short circuit, the worst case N-channel dissipation rises to:

$$P_N = I_{SC(AVG)}{}^2 \times R_{DS(ON)} \times (1 + \delta_N)$$

With the 0.05Ω sense resistor, $I_{SC(AVG)}$ = 2A will result, increasing the 0.085Ω N-channel dissipation to 450mW at a die temperature of 73°C.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V:

$$f_{MIN} = (1/2.92\mu s)[1 - (5V/7V)] = 98kHz$$

$$P_P = \frac{5V(0.12\Omega)(2A)^2(1.27)}{7V} = 435mV$$

A similar calculation for the 3.3V section results in the component values shown in Figure 16.

LTC1142HV-ADJ Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1142A adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} pin 2 (16). The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1142HV-ADJ as in Figure 6. The external divider network must be placed across C_{OUT} with the negative plate of C_{OUT} returned to signal ground. Refer to the Board Layout Checklist.

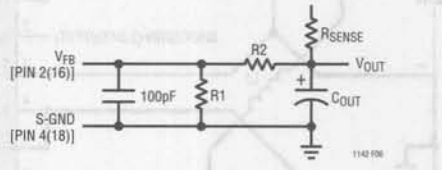

Figure 6. LTC1142HV-ADJ External Feedback Network

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1142. These items are also illustrated graphically in the layout diagram of Figure 7. In general each block should be self-contained with little cross coupling for best performance. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1142 signal ground [pin 3 (17) for the LTC1142, pin 4 (18) for LTC1142HV-ADJ] must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1142 Sense$^-$ pin 28 (14) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between pins 1 (15) and 28 (14) should be as close as possible to the LTC1142.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the input decoupling capacitor (1μF/0.22μF) connected closely between pin 24 (10) and power ground [pin 4 (18) for the LTC1142, pin 5 (19) for the LTC1142HV-ADJ]? This capacitor carries the MOSFET driver peak currents.

4

APPLICATIONS INFORMATION

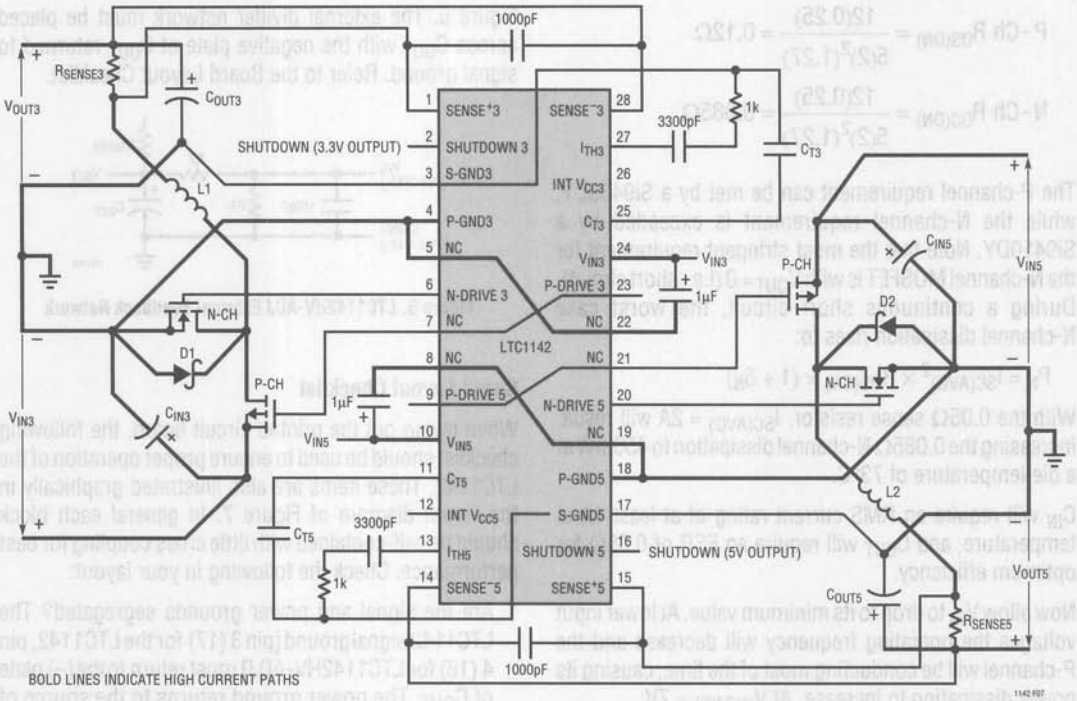

Figure 7. LTC1142 Layout Diagram (see Board Layout Checklist)

6. Are the shutdown pins 2 and 16 for the LTC1142 (pins 3 and 17 for the LTC1142HV-ADJ) actively pulled to ground during normal operation? Both shutdown pins are high impedance and must not be allowed to float. Both pins can be driven by the same external signal if needed.
7. For the LTC1142HV-ADJ adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the C_T pin 25 (11) above 1.5V when the output voltage is greater than the desired regulated value will turn "on" the N-channel MOSFET for that regulator section.

A fault condition which causes the output voltage to go above a maximum allowable value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will cause large currents to flow and blow the system fuse.

The N-channel MOSFET needs to be sized so it will safely handle this overcurrent condition. The typical delay from pulling the C_T pin high and the N-drive pin 6 (20) going high is 250ns. Note: Under shutdown conditions, the N-channel is held OFF and pulling the C_T pin high will not cause the N-channel MOSFET to crowbar the output.

A simple N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1142 as shown in Figure 8.

APPLICATIONS INFORMATION

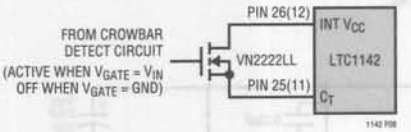

Figure 8. Output Crowbar Interface

Troubleshooting Hints

Since efficiency is critical to LTC1142 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pins 25 and 11.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 9b.

Inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

If pin 25 or pin 11 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

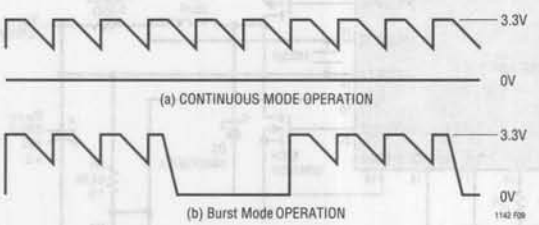

Figure 9. C_T Waveforms

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current ($I_{OUT} > 5A$) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 10. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

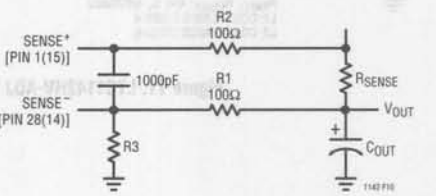

Figure 10. Suppression of Burst Mode Operation

With the addition of R3 a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3} \right)$$

If $V_{OFFSET} > 25mV$, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 1 (15) and 28 (14).

TYPICAL APPLICATIONS

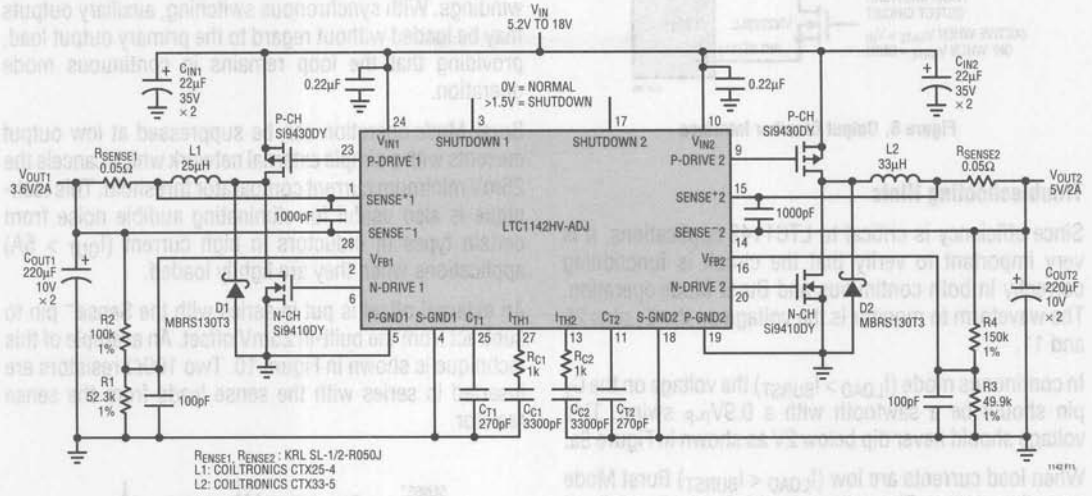

Figure 11. LTC1142HV-ADJ Dual Regulator with 3.6V/2A and 5V/2A Outputs

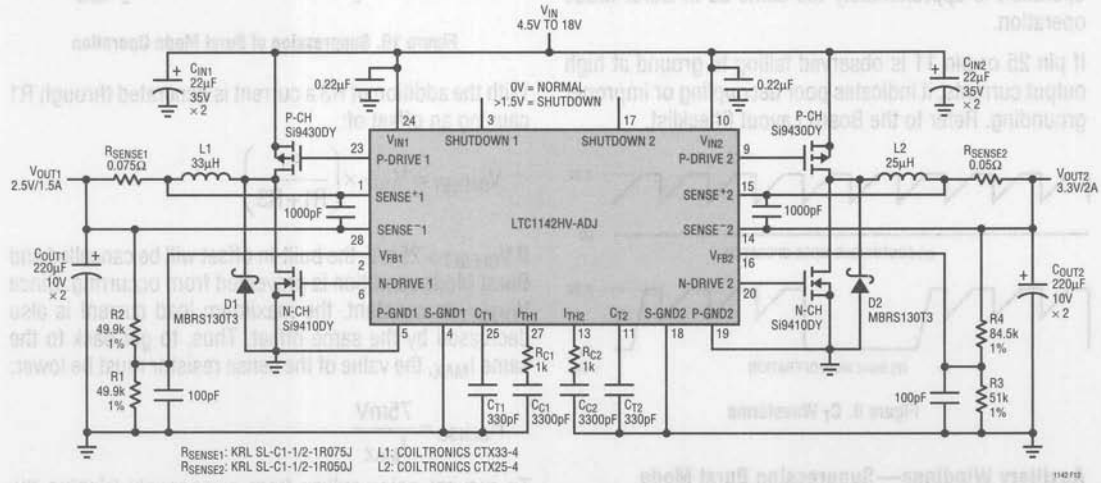

Figure 12. LTC1142HV-ADJ High Efficiency Regulator with 3.3V/2A and 2.5V/1.5A Outputs

TYPICAL APPLICATIONS

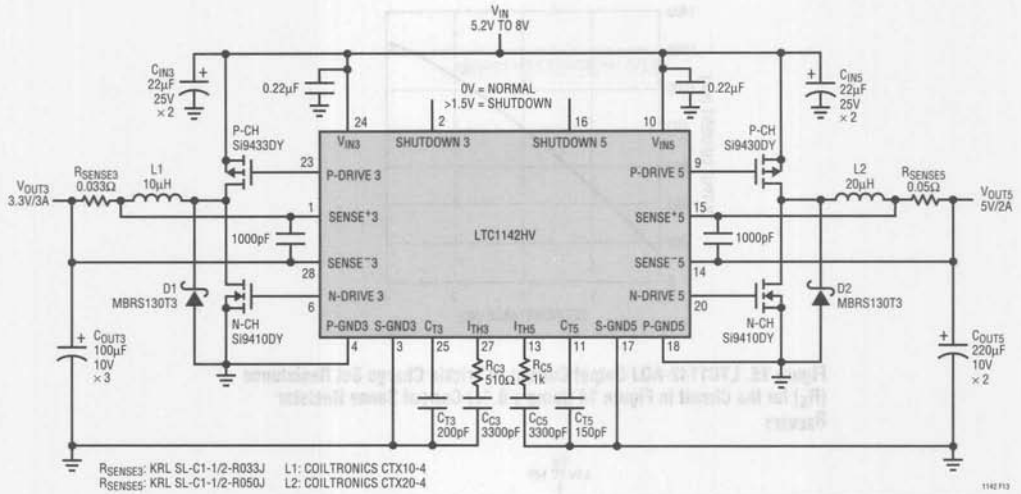

Figure 13. LTC1142 High Efficiency Regulator with 3.3V/3A and 5V/2A Outputs

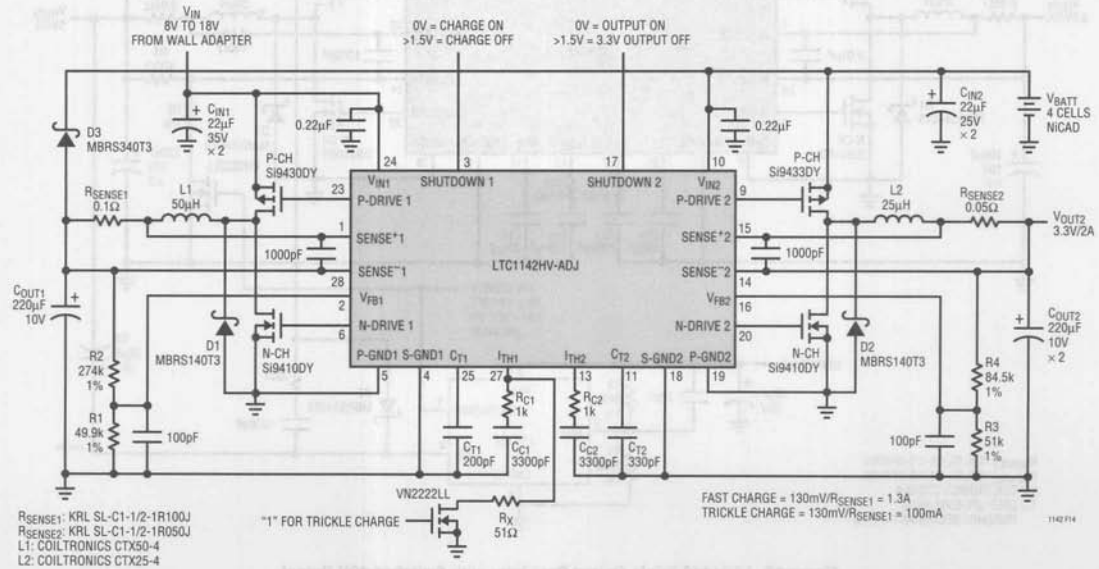

Figure 14. LTC1142HV-ADJ High Efficiency Power Supply Providing 3.3V/2A with Built-In Battery Charger

TYPICAL APPLICATIONS

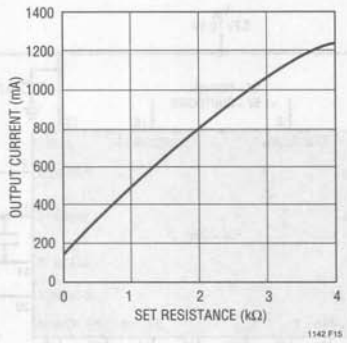

Figure 15. LTC1142-ADJ Output Current vs Trickle Charge Set Resistance (R_X) for the Circuit in Figure 14 Using a 0.1Ω Current Sense Resistor R_{SENSE1}

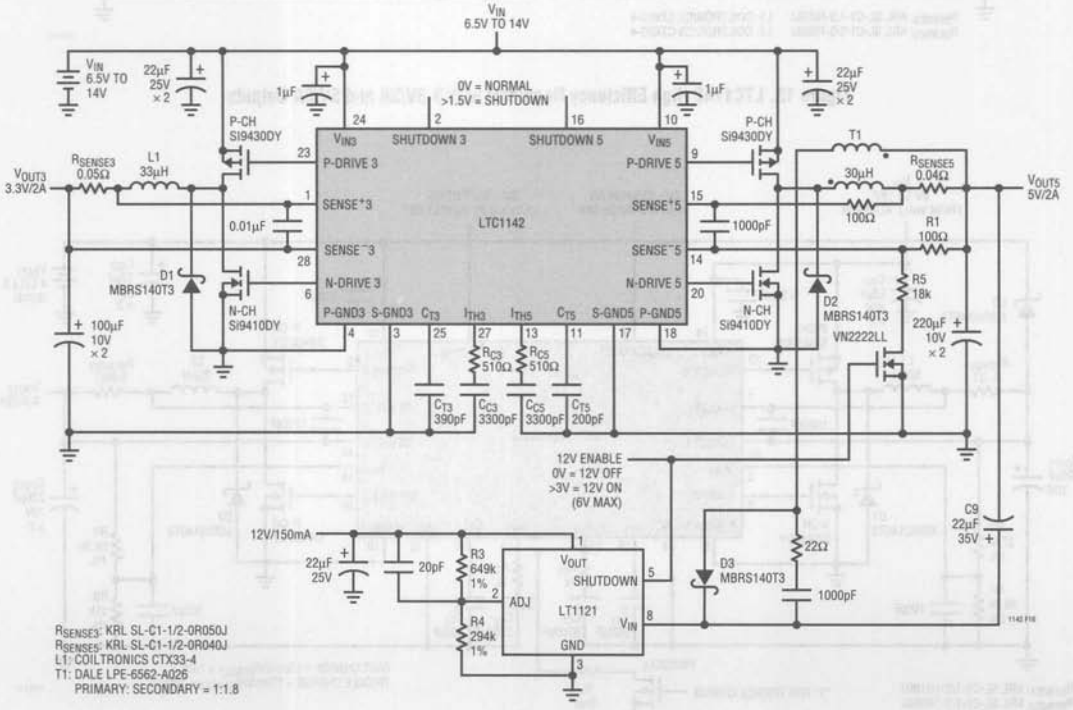

Figure 16. LTC1142 Triple Output Regulator with Switched 12V Output

Note: For additional higher efficiency circuits, see Application Note 54.

Dual High Efficiency Step-Down Switching Regulator Controller

FEATURES

- **Dual Outputs: 3.3V and 5.0V**
- **Very High Efficiency: Over 95% Possible**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over 3 Decades of Output Current
- Low Standby Current at Light Loads: 160µA/Output
- Independent Micropower Shutdown: I_Q < 40µA
- Wide V_{IN} Range: 4V to 16V
- Very Low Dropout Operation: 100% Duty Cycle
- Available in Narrow 16-Pin SOIC Package

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC1143 is a dual step-down switching regulator controller featuring automatic **Burst Mode**™ operation to maintain high efficiencies at low output currents. This device is composed of two separate regulator blocks, each driving an external power MOSFET at switching frequencies exceeding 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor.

The operating current level for both regulators is user-programmable via an external current sense resistor. Wide input supply range allows operation from 4V to 14V (16V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1143 is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

Burst Mode is a trademark of Linear Technology Corporation.

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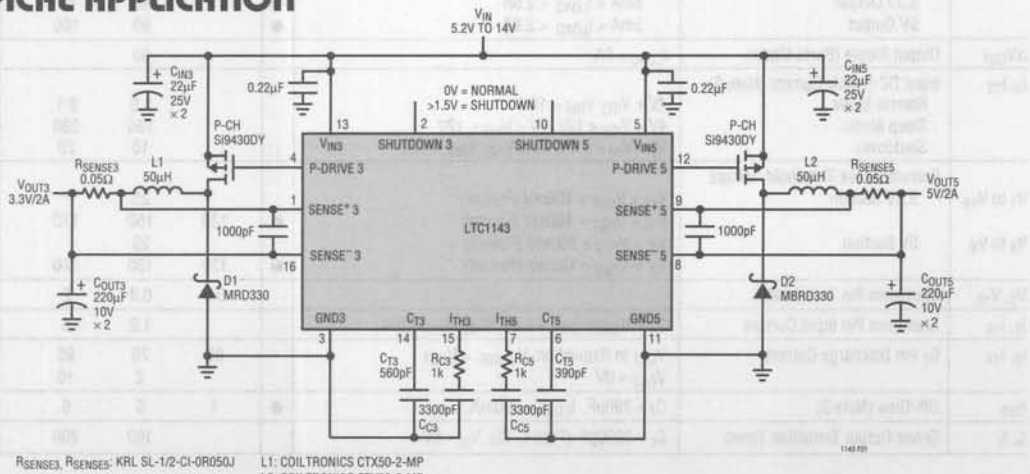
TYPICAL APPLICATION



RSENSE3, RSENSE5: KRL SL-1/2-CI-0R050J L1: COILTRONICS CTX50-2-MP
L2: COILTRONICS CTX50-2-MP

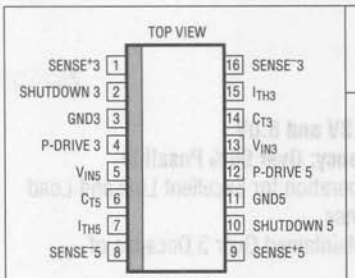
NOTE: COMPONENTS OPTIMIZED FOR HIGHEST EFFICIENCY, NOT MINIMUM BOARD SPACE.

Figure 1. High Efficiency Dual 3.3V/5V

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pins 5,13) ..... 16V to –0.3V
Continuous Output Current (Pins 4,12) 50mA
Sense Voltages (Pins 1, 8, 9, 16) ..... 13V to –0.3V
Operating Ambient Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1143CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN3} = V_{IN5} = 10V, V_2 = V_{10} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Output Voltage	V_{IN3}, V_{IN5} = 9V					
	3.3V Output	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN3}, V_{IN5} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
ΔV_{OUT}	Output Voltage Load Regulation	Figure 1 Circuit					
	3.3V Output	5mA < I_{LOAD} < 2.0A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2.0A	●		60	100	mV
ΔV_{OUT}	Output Ripple (Burst Mode)	I_{LOAD} = 0A			50		mV_{P-P}
I_5, I_{13}	Input DC Supply Current (Note 2)						
	Normal Mode	4V < V_{IN3}, V_{IN5} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{IN3} < 12V, 6V < V_{IN5} < 12V			160	230	µA
	Shutdown	V_2 = V_{10} = 2.1V, 4V < V_{IN3}, V_{IN5} < 12V			10	20	µA
	Current-Sense Threshold Voltage						
V_1 to V_{16}	3.3V Section	V_{16} = V_{OUT} + 100mV (Forced)			25		mV
		V_{16} = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
V_8 to V_9	5V Section	V_8 = V_{OUT} + 100mV (Forced)			25		mV
		V_8 = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
V_2, V_{10}	Shutdown Pin Threshold			0.6	0.8	2	V
I_2, I_{10}	Shutdown Pin Input Current	0V < $V_{SHUTDOWN}$ = < 8V, V_{IN3}, V_{IN5} = 16V			1.2	5	µA
I_6, I_{14}	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE-} = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 4, 12), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$ (Note 4), $V_{IN3} = V_{IN5} = 10V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Output Voltage	$V_{IN3}, V_{IN5} = 9V$				
	3.3V Output	$I_{LOAD} = 700mA$	3.17	3.33	3.4	V
	5V Output	$I_{LOAD} = 700mA$	4.85	5.05	5.2	V
I_5, I_{13}	Input DC Supply Current (Note 2)					
	Normal Mode	$4V < V_{IN3}, V_{IN5} < 12V$		1.6	2.4	mA
	Sleep Mode	$4V < V_{IN3}, V_{IN5} < 12V$		160	260	µA
	Shutdown	$V_2 = V_{10} = 2.1V$, $4V < V_{IN3}, V_{IN5} < 12V$		10	22	µA
	Current Sense Threshold Voltage					
V_1 to V_{16}	3.3V Section	$V_{16} = V_{OUT} + 100mV$ (Forced)		25		mV
		$V_{16} = V_{OUT} - 100mV$ (Forced)	125	150	175	mV
V_8 to V_9	5V Section	$V_8 = V_{OUT} + 100mV$ (Forced)		25		mV
		$V_8 = V_{OUT} - 100mV$ (Forced)	125	150	175	mV
V_2, V_{10}	Shutdown Pin Threshold		0.55	0.8	2	V
t_{OFF}	Off-Time (Note 3)	$C_T = 390pF$, $I_{LOAD} = 700mA$	3.8	5	6	µs

The ● denotes specifications which apply over the operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1143CS: $T_J = T_A + (P_D \times 120°C/W)$

Note 2: This supply current is for one regulator block. Total supply current is the sum of pin 5 and pin 13 currents. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 4: The LTC1143 is not tested and quality assurance sampled at –40°C to 85°C. These specifications are guaranteed by design and/or correlation.

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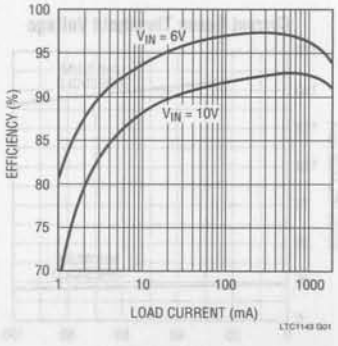
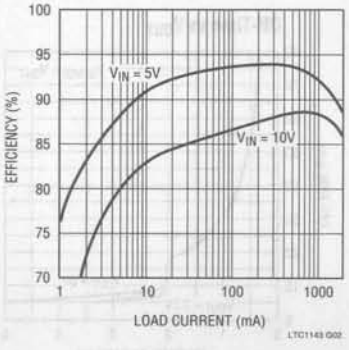
TYPICAL PERFORMANCE CHARACTERISTICS

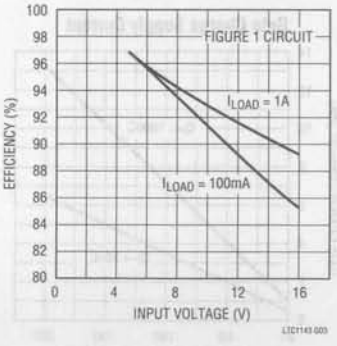
5V Output Efficiency



3.3V Output Efficiency

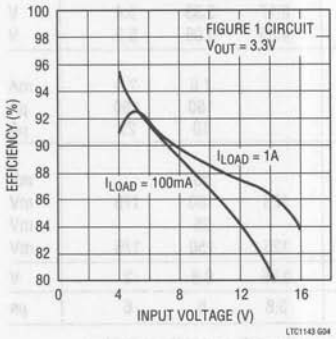


5V Efficiency vs Input Voltage

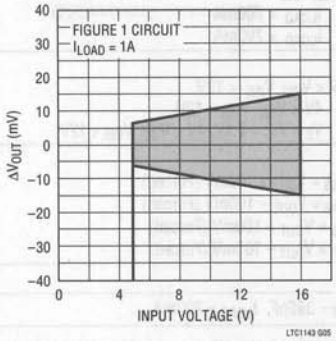


TYPICAL PERFORMANCE CHARACTERISTICS

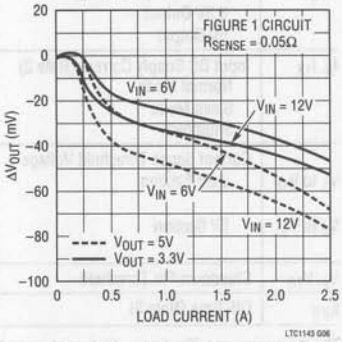
3.3V Efficiency vs Input Voltage



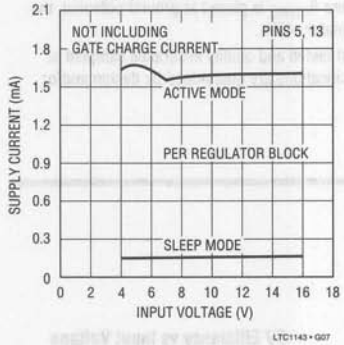
Line Regulation



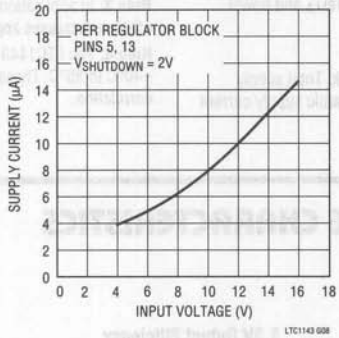
Load Regulation



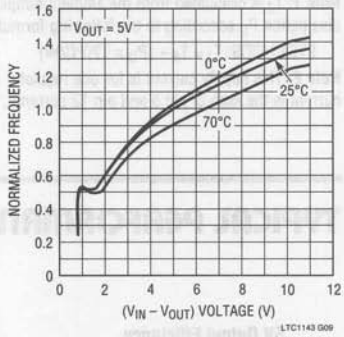
DC Supply Current



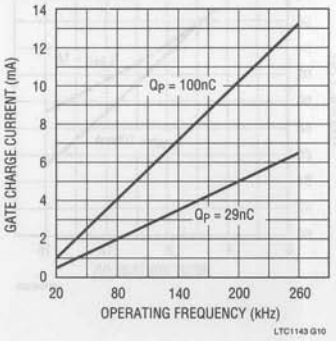
Supply Current in Shutdown



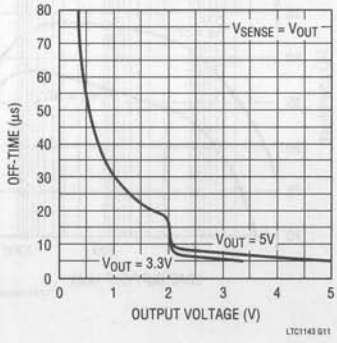
Operating Frequency vs $V_{IN} - V_{OUT}$



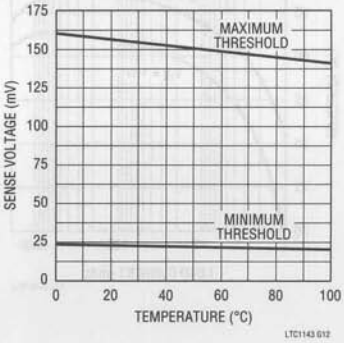
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

SENSE+3 (Pin 1): The (+) Input to the 3.3V Section Current Comparator. A built in offset between pins 1 and 16 in conjunction with $R_{SENSE\ 3}$ sets the current trip threshold for the 3.3V section.

SHUTDOWN 3 (Pin 2): When grounded, the 3.3V section operates normally. Pulling pin 2 high holds the MOSFET off and puts the 3.3V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" pin 2.

GND3 (Pin 3): 3.3V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 3.3V section output capacitor, and 2) the cathode of the Schottky diode D1 and (–) terminal of C_{IN3} (See Figures 1 and 9).

P-DRIVE 3 (Pin 4): High Current Drive for Top P-Channel MOSFET, 3.3V Section. Voltage swing at this pin is from V_{IN3} to ground.

V_{IN5} (Pin 5): Supply Pin, 5V Section. Must be closely decoupled to 5V power ground pin 11.

C_{T5} (Pin 6): External capacitor C_{T5} from pin 6 to ground sets the operating frequency for the 5V section. (The actual frequency is also dependent upon the input voltage.)

I_{TH5} (Pin 7): Gain Amplifier Decoupling Point, 5V Section. The 5V section current comparator threshold increases with the pin 7 voltage.

SENSE– 5 (Pin 8): Connects to internal resistive divider which sets the output voltage for the 5V section. Pin 8 is also the (–) input for the current comparator on the 5V section.

SENSE+ 5 (Pin 9): The (+) Input to the 5V Section Current Comparator. A built-in offset between pins 9 and 8 in conjunction with $R_{SENSE\ 5}$ sets the current trip threshold for the 5V section.

SHUTDOWN 5 (Pin 10): When grounded, the 5V section operates normally. Pulling pin 10 high holds the 5V section MOSFET off and puts the 5V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" pin 10.

GND5 (Pin 11): 5V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 5V section output capacitor, and 2) the cathode of the Schottky diode D2 and (–) terminal of C_{IN5} (See Figures 1 and 9).

P-DRIVE 5 (Pin 12): High Current Drive for Top P-Channel MOSFET, 5V Section. Voltage swing at this pin is from V_{IN5} to ground.

V_{IN3} (Pin 13): Supply Pin, 3.3V Section. Must be closely decoupled to 3.3V power ground pin 3.

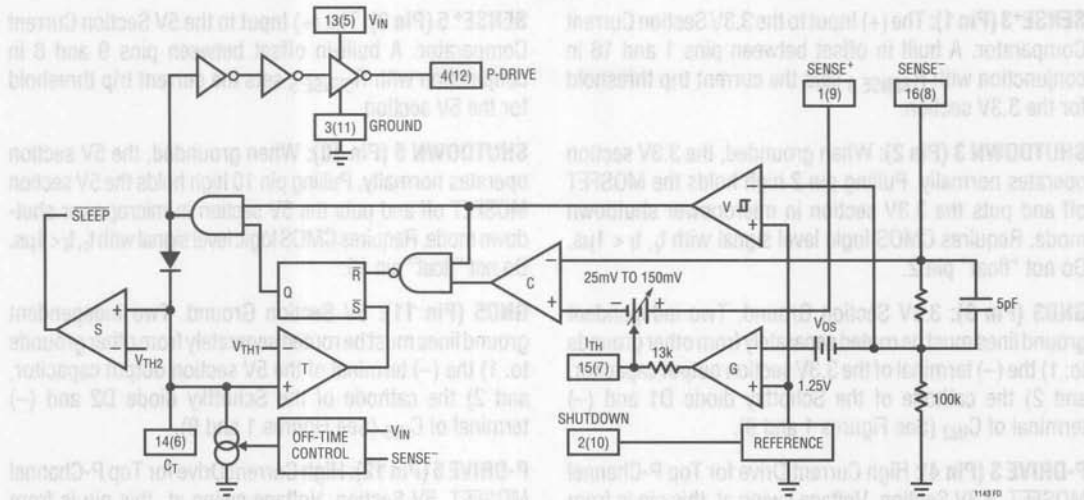
C_{T3} (Pin 14): External capacitor C_{T3} from pin 14 to ground sets the operating frequency for the 3.3V section. (The actual frequency is also dependent upon the input voltage.)

I_{TH3} (Pin 15): Gain Amplifier Decoupling Point, 3.3V Section. The 3.3V section current comparator threshold increases with the pin 15 voltage.

SENSE– 3 (Pin 16): Connects to internal resistive divider which sets the output voltage for the 3.3V section. Pin 16 is also the (–) input for the current comparator on the 3.3V section.

FUNCTIONAL DIAGRAM

Only one regulator block shown. Pin numbers are for 3.3V (5V) sections.



OPERATION

Refer to Functional Diagram and Figure 1.

The LTC1143 consists of two individual regulator blocks each using current mode, constant off-time architectures to switch an external power MOSFET. The two regulators are internally set to provide output voltages of 3.3V and 5V. Operating frequency is individually set on each section by external capacitors at the timing capacitor pins 6 and 14.

The output voltage is sensed by an internal voltage divider connected to Sense$^-$ pin 16 (8). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1143 automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 1 (9) and 16 (8) connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 14 (6) is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage [measured by pin 16 (8)] to model the inductor current, which decays at a rate which is also proportional to the output voltage.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the P-drive output to go low turning the P-channel MOSFET back on. The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage [pin 15 (7)] to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{\text{sleep}}$ line to go low.

The circuit now enters sleep mode with the power MOSFET turned off. In sleep mode a majority of the circuitry is

OPERATION Refer to Functional Diagram and Figure 1

turned off, dropping the quiescent current from 1.6mA to 160μA (for one regulator block). The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and the process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset (V_{OS}) is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing extremely low dropout operation.

APPLICATIONS INFORMATION

The basic LTC1143 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFET and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the 3.3V and 5V sections are identical, the process of component selection is the same for both sections. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 16V.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1143 current comparators have a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE}. (See C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1143 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

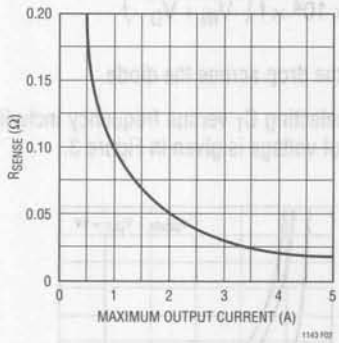


Figure 2. Selecting R_{SENSE}

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1143 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

APPLICATIONS INFORMATION

L and C_T Selection for Operating Frequency

Each regulator section of LTC1143 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3 \times 10^4 \times f}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)$$

Where V_D is the drop across the diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

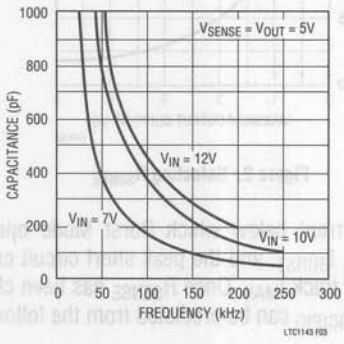


Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V for a particular section, the LTC1143 reduces t_{OFF} in that section by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used the inductor current will become discontinuous before the LTC1143 enters Burst Mode operation. A consequence of this is that the LTC1143 will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using Ferrite, Kool Mμ® or Molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance, but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (> 200 kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corporation which do not increase the height significantly.

Power MOSFET Selection

An external power MOSFET must be selected for use with each section of the LTC1143. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage determines whether a standard threshold or logic-level threshold MOSFET must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. When logic-level MOSFETs are used, the LTC1143 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFET.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1143 is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Schottky Diode Duty Cycle} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_P}{V_{OUT} \times I_{MAX}^2 \times (1 + \delta_P)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependencies of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1+d) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but $\delta = 0.007/°C$ can be used as an approximation for low voltage MOSFETs.

Output Diode Selection (D1, D2)

The Schottky diodes D1 and D2 shown in Figure 1 conduct during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

The most stressful condition for the output diode is under short circuit ($V_{OUT}=0$). Under this condition the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions the average current conducted by the diode is:

$$I_{DIODE} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}} (I_{LOAD})$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(PK)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency Considerations).

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APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on each V_{IN} line (pin 5, pin 13) for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1143:*

$$C_{OUT} \text{ required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$ the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon, should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR size/ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be parallel to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, (2) AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

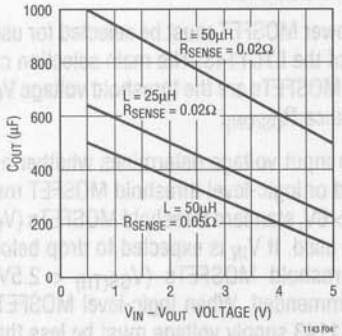

Figure 4. Minimum Value of C_{OUT}

At low supply voltages a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1143 would normally be in continuous operation. The output remains in regulation at all times.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The pin 15(7) external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT} causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1143 circuits:

1) LTC1143 DC bias current
2) MOSFET gate charge current
3) I^2R losses
4) Voltage drop of the Schottky diode.

1) The DC supply current is the current which flows into V_{IN} (pin 13 for the 3.3V section, pin 5 for the 5V section) less the gate charge current. For V_{IN} = 10V the LTC1143 DC supply current for each section is 160µA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1143 has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN}=10V the DC bias losses are generally less than 1% for load currents over 30mA. However at very low load currents the DC bias current accounts for nearly all of the loss.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_P)$. The typical gate charge for a 125mΩ P-channel power MOSFET is 40nC. This results in $I_{GATECHG}$ = 4mA in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3) I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel MOSFET and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if the $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 10% as the output

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current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4) The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A. If Schoky diode losses routinely exceed 5% consider using the synchronously switched LTC1142.

Figure 5 shows how the efficiency losses in one section of a typical LTC1143 regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses and Schottky diode loss dominate at high load currents.

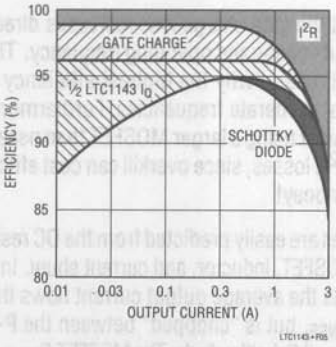

Figure 5. Efficiency Loss

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 12V(nominal), 5V section, I_{MAX} = 2A, and f = 200kHz, R_{SENSE}, C_T, and L can immediately be calculated:

$$R_{SENSE5} = 100mV / 2 = 0.05\Omega$$

$$t_{OFF} = (1/200kHz) \times [1 - (5/12)] = 2.92\mu s$$

$$C_{T5} = 2.92\mu s/(1.3 \times 10^4) = 220pF$$

$$L2_{MIN} = 5.1 \times 10^5 \times 0.05\Omega \times 220pF \times 5V = 28\mu H$$

Assume that the MOSFET dissipation is to be limited to P_P = 250mW.

If T_A = 50°C and the thermal resistance of the MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = \delta_N = 0.007(63\text{-}25) = 0.27$. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2\,(1.27)} = 0.12\Omega$$

The P-channel requirement can be met by a Si9430DY. Note that the most stringent requirement for the Schottky diode is with V_{OUT} = 0 (i.e. short circuit). During a continuous short circuit, the worst case Schottky diode dissipation rises to:

$$P_D = I_{SC(AVG)} \times V_D \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

With the 0.05Ω sense resistor $I_{SC(AVG)}$ = 2A will result, increasing the 0.4V Schottky diode dissipation to 0.8W.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V, the frequency shifts to 49kHz and the P-channel power dissipation increases to 435mW. Check to assure the maximum temperature of the P-channel is not exceeded.

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Troubleshooting Hints

Since efficiency is critical to LTC1143 applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor pin 14 and pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 7a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 7b.

If pin 14 or pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

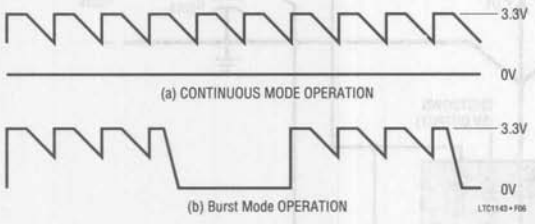


Figure 7. C_T Waveforms

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1143 being a nonsynchronous switch has the normal limitation that the power drawn from the inductor primary winding must not be less than twice the power drawn from the auxiliary windings. (With synchronous switching, using the LTC1142, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.)

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT}>5A) applications when they are lightly loaded.

An external offset is put in series with the Sense⁻ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 8. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

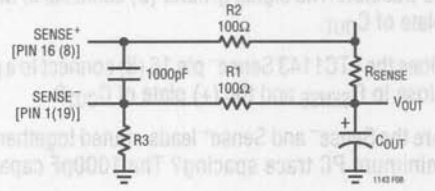


Figure 8. Suppression of Burst Mode Operation

With the addition of R3 a current is generated though R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 1 (16) and 9 (8).

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1143. These items are also illustrated graphically in the layout diagram of Figure 9. In general each block

APPLICATIONS INFORMATION

should be self-contained with little cross coupling for best performance. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1143 ground pin 3 (11) must return separately to: a) the power, and b) the signal grounds. The power ground returns to the anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible. The signal ground (b) connects to the (–) plate of C_{OUT}.

2) Does the LTC1143 Sense⁻ pin 16 (8) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?

3) Are the Sense⁻ and Sense⁺ leads routed together with minimum PC trace spacing? The 1000pF capacitor between pins 1 (9) and 16 (8) should be as close as possible to the LTC1143.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-Channel MOSFET.

5) Is the V_{IN} decoupling capacitor (1µF, 0.1µF) connected closely between pin 13 (5) and ground pin 3 (11)? This capacitor carries the MOSFET driver peak currents.

6) Are the Shutdown pins 2 and 10 actively pulled to ground during normal operation? Both shutdown pins are high impedance and must not be allowed to float. Both pins can be driven by the same external signal if needed.

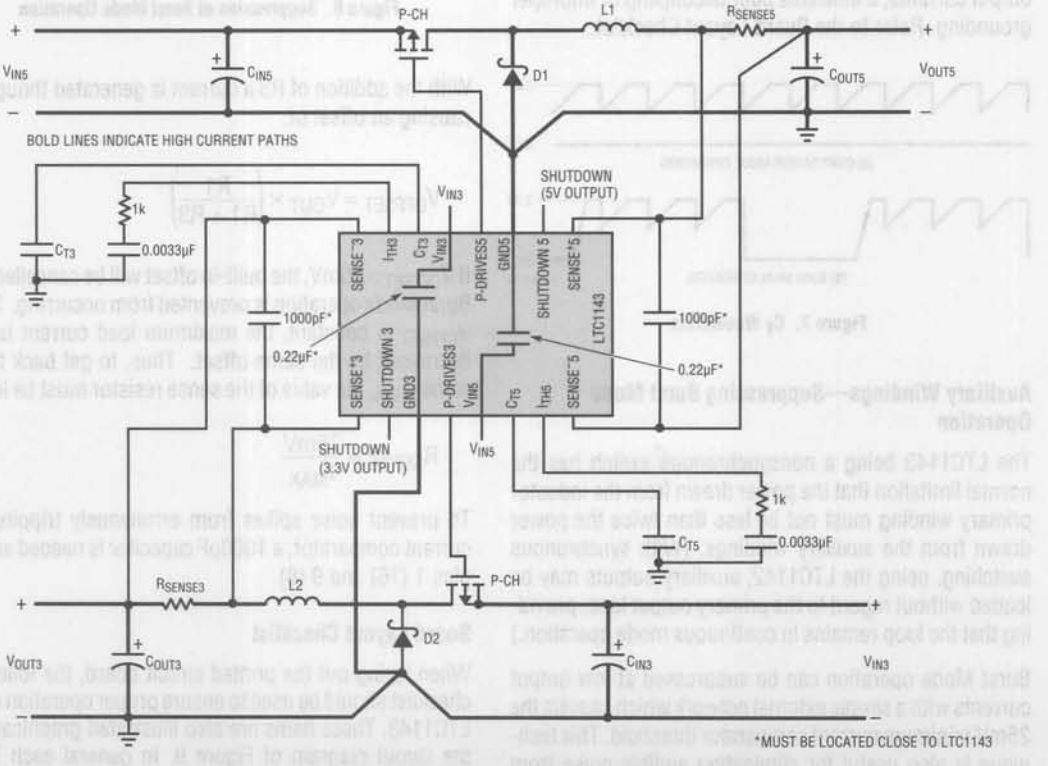
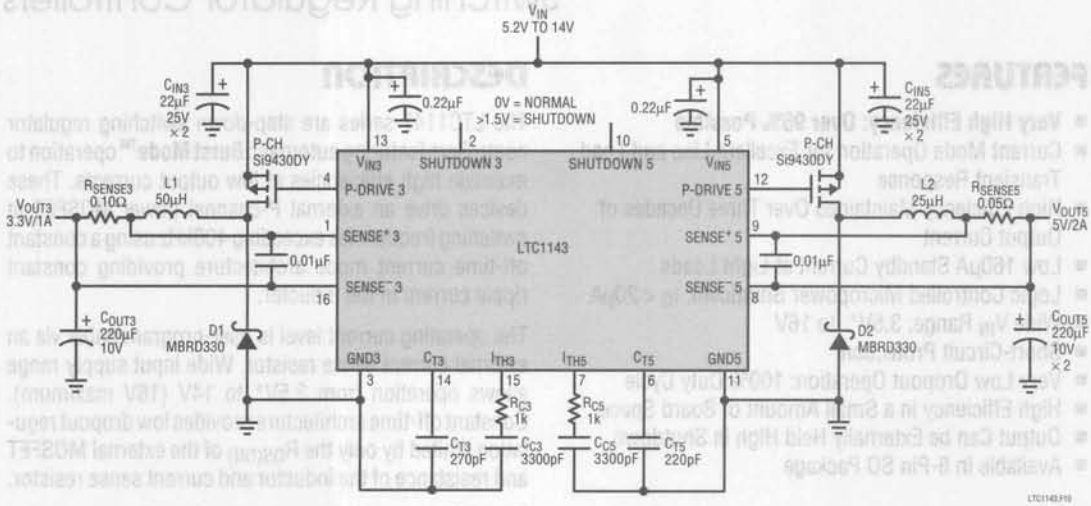


Figure 9. LTC1143 Layout Diagram (see Board Layout Checklist)

TYPICAL APPLICATIONS

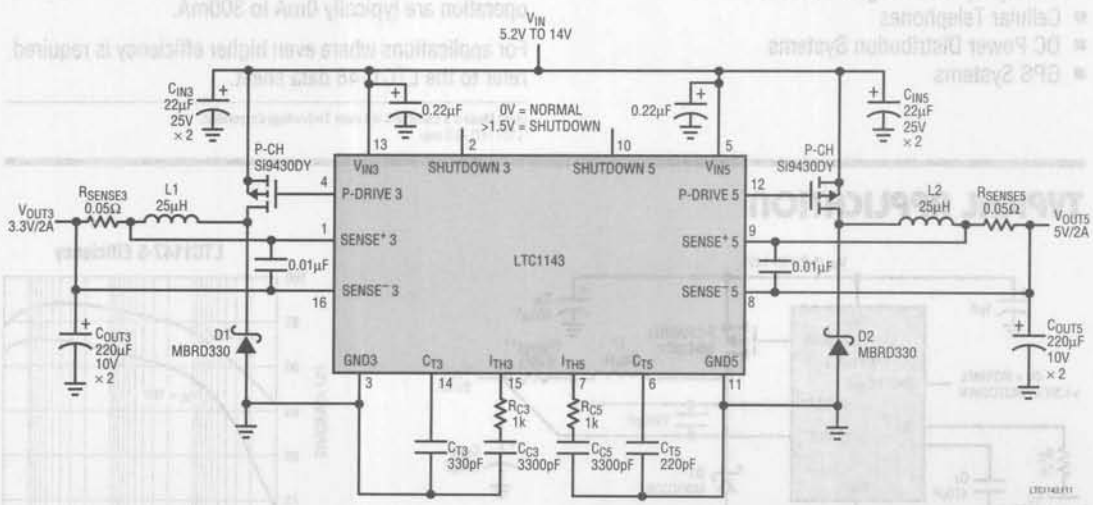


RSENSE3: IRC LR2512-01-0R100G
RSENSE5: IRC LR2512-01-0R050G

CIN3, CIN5: AVX (TA) TPSD226K025R0200
COUT3, COUT5: AVX (TA) TPSE227K010R0080

L2: COILTRONICS CTX50-4
L2: COILTRONICS CTX25-4

Figure 10. All Surface Mount Dual 5V/2A, 3.3V/1A Converter



RSENSE3: KRL SL-1/2-C1-0R050J
RSENSE5: KRL SL-1/2-C1-0R050J

CIN3, CIN5: AVX (TA) TPSD226K025R0200
COUT3, COUT5: AVX (TA) TPSE227K010R0080

L1: COILTRONICS CTX25-4
L2: COILTRONICS CTX25-4

Figure 11. All Surface Mount Dual 5V/2A, 3.3V/2A Converter

High Efficiency Step-Down Switching Regulator Controllers

FEATURES

- **Very High Efficiency: Over 95% Possible**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Three Decades of Output Current
- Low 160µA Standby Current at Light Loads
- Logic Controlled Micropower Shutdown: I_Q < 20µA
- Wide V_{IN} Range: 3.5V* to 16V
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- High Efficiency in a Small Amount of Board Space
- Output Can be Externally Held High in Shutdown
- Available in 8-Pin SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC1147 series are step-down switching regulator controllers featuring automatic **Burst Mode™** operation to maintain high efficiencies at low output currents. These devices drive an external P-channel power MOSFET at switching frequencies exceeding 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V* to 14V (16V maximum). Constant off-time architecture provides low dropout regulation limited by only the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1147 series incorporate automatic power saving **Burst Mode** operation to reduce switching losses when load currents drop below the level required for continuous operation. Standby power is reduced to only 2mW at V_{IN} = 10V (at I_{OUT} = 0). Load currents in **Burst Mode** operation are typically 0mA to 300mA.

For applications where even higher efficiency is required, refer to the LTC1148 data sheet.

Burst Mode is a trademark of Linear Technology Corporation.
*LTC1147L-3.3 only.

TYPICAL APPLICATION

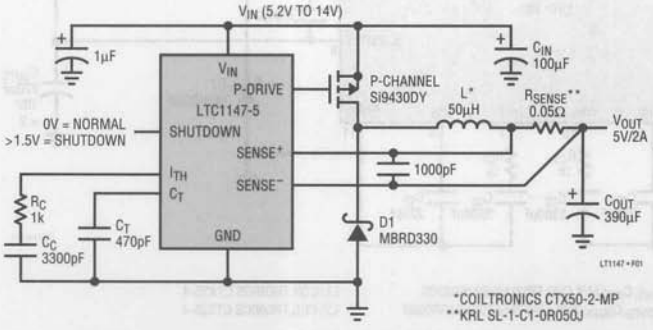
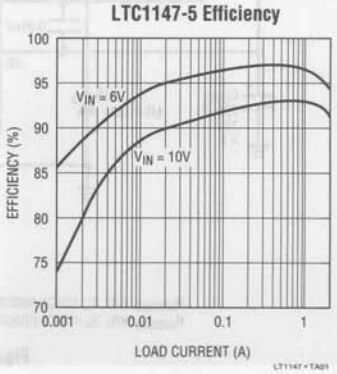


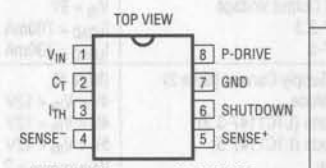
Figure 1. High Efficiency Step-Down Converter



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 1) ..... 16V to –0.3V
Continuous Output Current (Pin 8) 50mA
Sense Voltages (Pins 4, 5) ..... 10V to –0.3V
Operating Ambient Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 110°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC1147CN8-3.3
LTC1147CN8-5
LTC1147CS8-3.3
LTC1147LCS8-3.3
LTC1147CS8-5
S8 PART MARKING
11473
11475

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1147-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1147-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1147-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1147-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Burst Mode™ Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_Q	Input DC Supply Current (Note 2)	(Note 5)					
	Normal Mode	4V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode (LTC1147-3.3)	4V < V_{IN} < 12V			160	230	µA
	Sleep Mode (LTC1147-5)	5V < V_{IN} < 12V			160	230	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 12V			10	20	µA
$V_5 - V_4$	Current Sense Threshold Voltage						
	LTC1147-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
	LTC1147-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
V_6	Shutdown Pin Threshold			0.6	0.8	2	V
I_6	Shutdown Pin Input Current	0V < $V_{SHUTDOWN}$ < 8V, V_{IN} = 16V			1.2	5	µA
I_2	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 8), V_{IN} = 6V			100	200	ns

4

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$ (Note 4), $V_{IN} = 10V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Output Voltage	$V_{IN} = 9V$					
	LTC1147-3.3	$I_{LOAD} = 700mA$	●	3.17	3.33	3.4	V
	LTC1147-5	$I_{LOAD} = 700mA$	●	4.85	5.05	5.2	V
I_Q	Input DC Supply Current (Note 2)	(Note 5)					
	Normal Mode	$4V < V_{IN} < 12V$			1.6	2.4	mA
	Sleep Mode (LTC1147-3.3)	$4V < V_{IN} < 12V$			160	260	µA
	Sleep Mode (LTC1147-5)	$5V < V_{IN} < 12V$			160	260	µA
	Shutdown	$V_{SHUTDOWN} = 2.1V$, $4V < V_{IN} < 12V$			10	22	µA
$V_5 - V_4$	Current Sense Threshold Voltage						
	LTC1147-3.3	$V_{SENSE}^- = V_{OUT} + 100mV$ (Forced)			25		mV
		$V_{SENSE}^- = V_{OUT} - 100mV$ (Forced)	●	125	150	175	mV
	LTC1147-5	$V_{SENSE}^- = V_{OUT} + 100mV$ (Forced)			25		mV
		$V_{SENSE}^- = V_{OUT} - 100mV$ (Forced)	●	125	150	175	mV
V_6	Shutdown Pin Threshold			0.55	0.8	2	V
t_{OFF}	Off-Time (Note 3)	$C_T = 390pF$, $I_{LOAD} = 700mA$	●	3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1147CN8-3.3, LTC1147CN8-5: $T_J = T_A + (P_D \times 110°C/W)$

LTC1147CS8-3.3, LTC1147CS8-5: $T_J = T_A + (P_D \times 150°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. **See Applications Information.**

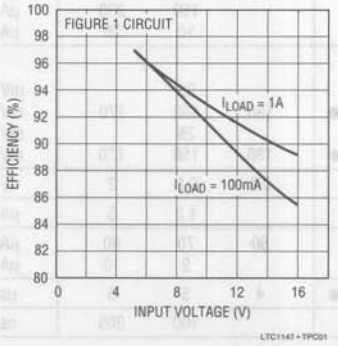
Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 4: The LTC1147-3.3/LTC1147-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

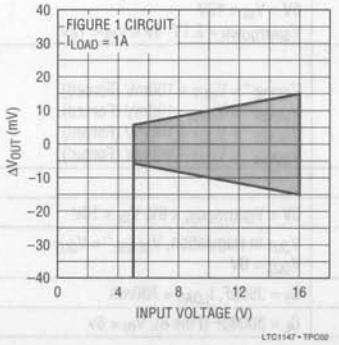
Note 5: The LTC1147L-3.3 allows operation to $V_{IN} = 3.5V$.

TYPICAL PERFORMANCE CHARACTERISTICS

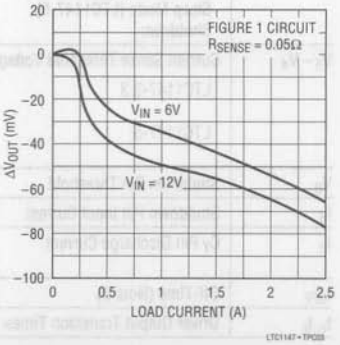
Efficiency vs Input Voltage



Line Regulation

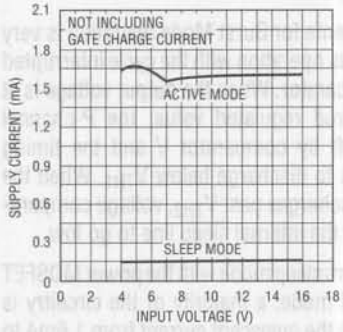


Load Regulation

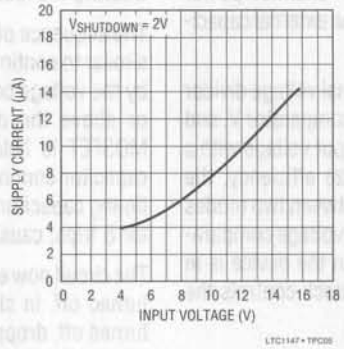


TYPICAL PERFORMANCE CHARACTERISTICS

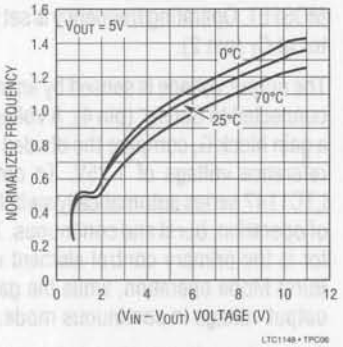
DC Supply Current



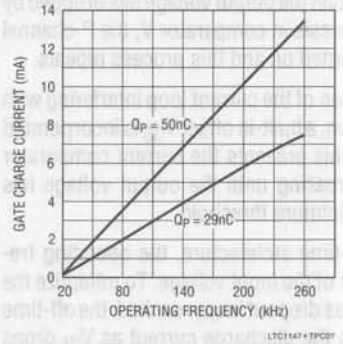
Supply Current in Shutdown



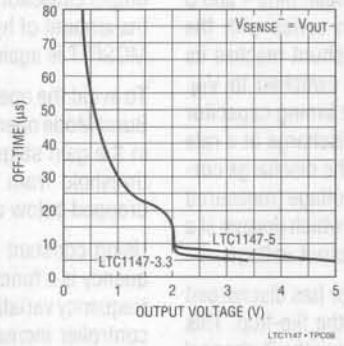
Operating Frequency vs ($V_{IN} - V_{OUT}$)



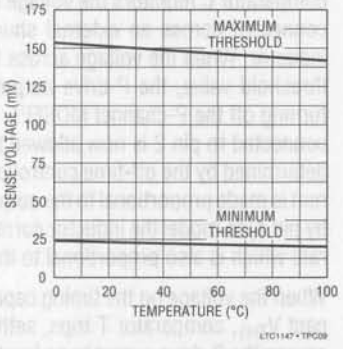
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

Pin 1 (V_{IN}): Main supply pin. Must be closely decoupled to ground pin 7.

Pin 2 (C_T): External capacitor C_T from pin 2 to ground sets the operating frequency. The actual frequency is also dependent upon the input voltage.

Pin 3 (I_{TH}): Gain amplifier decoupling point. The current comparator threshold increases with the pin 3 voltage.

Pin 4 (Sense⁻): Connects to internal resistive divider which sets the output voltage. Pin 4 is also the (–) input for the current comparator.

Pin 5 (Sense⁺): The (+) input to the current comparator. A built-in offset between pins 4 and 5 in conjunction with R_{SENSE} sets the current trip threshold.

Pin 6 (Shutdown): When grounded, the LTC1147 operates normally. Pulling pin 6 high holds the P-channel MOSFET off and puts the LTC1147 in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not leave this pin floating.

Pin 7 (Ground): Two independent ground lines must be routed separately to: 1) the (–) terminal of C_{OUT}, and 2) the cathode of the Schottky diode and (–) terminal of C_{IN}.

Pin 8 (P-Channel Drive): High current drive for the P-channel MOSFET. Voltage swing at this pin is from V_{IN} to ground.

OPERATION (Refer to Functional Diagram)

The LTC1147 series use a current mode, constant off-time architecture to switch an external P-channel power MOSFET. Operating frequency is set by an external capacitor at C_T (pin 2).

The output voltage is sensed by an internal voltage divider connected to Sense$^-$ (pin 4). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1147 series automatically switch between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "on" cycle in continuous mode, current comparator C monitors the voltage between pins 4 and 5 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 2 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by pin 4) to model the inductor current, which decays at a rate which is also proportional to the output voltage.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the P-drive output to go low turning the P-channel MOSFET back on. The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (pin 3) to increase the current comparator threshold, thus tracking the load current.

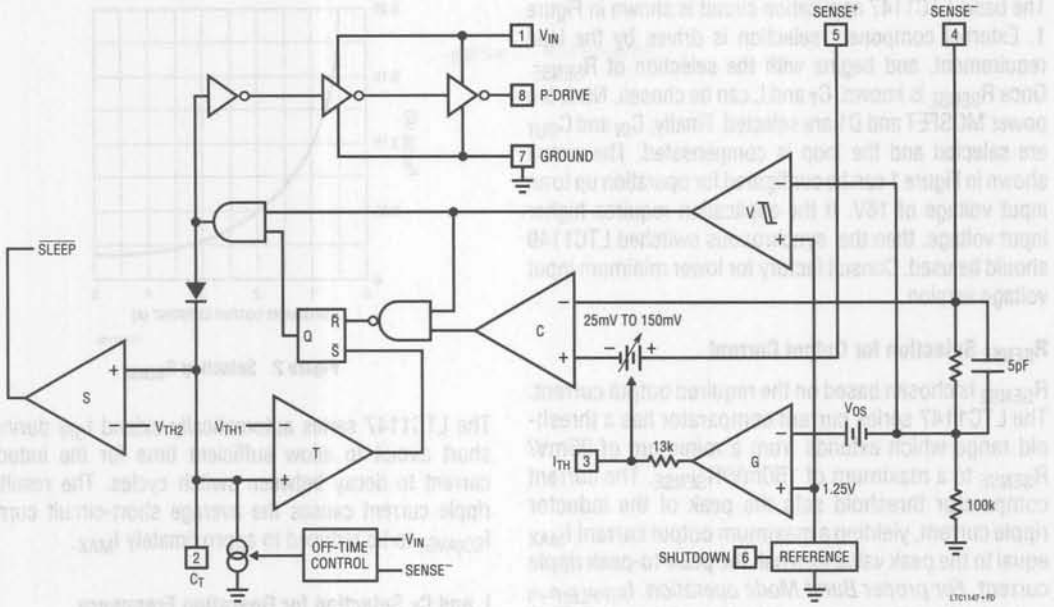
The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{\text{sleep}}$ line to go low.

The circuit now enters sleep mode with the power MOSFET turned off. In sleep mode, a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160μA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

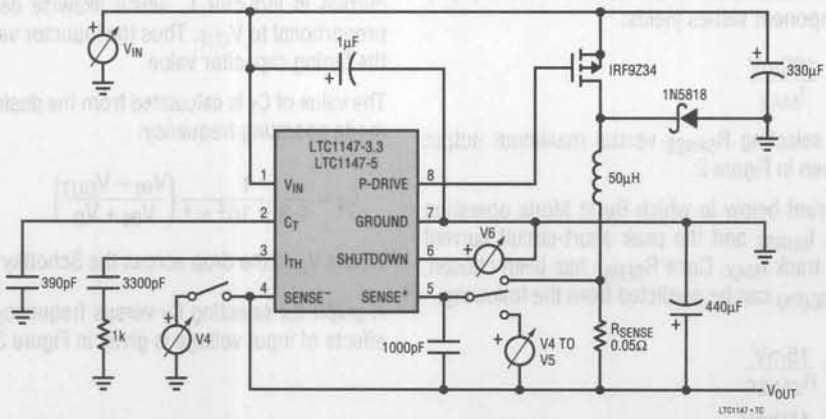
To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing low dropout operation with $V_{OUT} \approx V_{IN}$.

FUNCTIONAL DIAGRAM



TEST CIRCUIT



4

APPLICATIONS INFORMATION

The basic LTC1147 application circuit is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFET and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 16V. If the application requires higher input voltage, then the synchronous switched LTC1149 should be used. Consult factory for lower minimum input voltage version.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1147 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 25mV/R_{SENSE}$ (See **C_T and L Selection for Operating Frequency**). Solving for R_{SENSE} and allowing a margin for variations in the LTC1147 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

The load current below in which Burst Mode operation commences, I_{BURST} and the peak short-circuit current $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

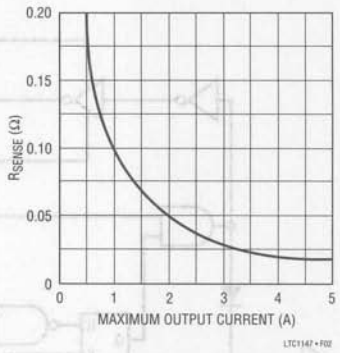


Figure 2. Selecting R_{SENSE}

The LTC1147 series automatically extend t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1147 series use a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3 \times 10^4 \times f}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)$$

Where V_D is the drop across the Schottky diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

APPLICATIONS INFORMATION

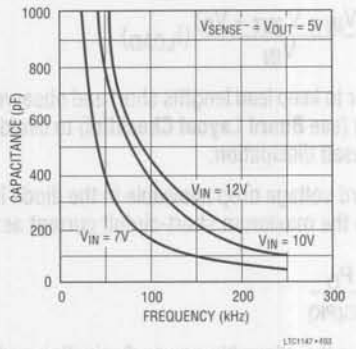


Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will reduce efficiency (see **Efficiency Considerations**). The complete expression for operating frequency is given by:

$$f \approx \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1147 reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $25mV/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will become discontinuous before the LTC1147 series enters Burst Mode operation. A consequence of this is that the LTC1147 series will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. Highest efficiency will be obtained using ferrite, Kool Mμ® (from Magnetics, Inc.) or molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 5%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1147. Do not allow the core to saturate!

Kool Mμ is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics, Sumida and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC1147 series. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and "on" resistance $R_{DS(ON)}$.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

The minimum input voltage determines whether a standard threshold or logic-level threshold MOSFET must be used. For $V_{IN} > 8V$, a standard threshold MOSFET ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, a logic-level threshold MOSFET ($V_{GS(TH)} < 2.5V$) is strongly recommended. When a logic-level MOSFET is used, the LTC1147 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFET.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the power MOSFET. When the LTC1147 series is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Schottky Diode Duty Cycle} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}}$$

From the duty cycle the required $R_{DS(ON)}$ for the MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_P}{V_{OUT} \times I_{MAX}^2 \times (1 + \delta_P)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependency of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see **Efficiency Considerations**). $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.007/°C$ can be used as an approximation for low voltage MOSFETs.

Output Diode Selection (D1)

The Schottky diode D1 shown in Figure 1 only conducts during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

The most stressful condition for the output diode is under short circuit ($V_{OUT} = 0$). Under this condition the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions the average current conducted by the diode is:

$$I_{D1} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}} (I_{LOAD})$$

Remember to keep lead lengths short and observe proper grounding (see **Board Layout Checklist**) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(PK)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see **Efficiency Considerations**).

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic decoupling capacitor is also required on V_{IN} (pin 1) for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1147 :*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

APPLICATIONS INFORMATION

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1147 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

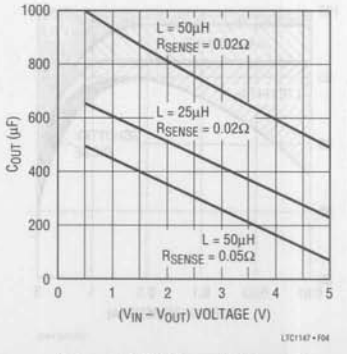


Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

APPLICATIONS INFORMATION

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power).

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1147 circuits: 1) LTC1147 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) voltage drop of the Schottky diode.

1. The DC supply current is the current which flows into V_{IN} (pin 1) less the gate charge current. For V_{IN} = 10V the LTC1147 series DC supply current is 160µA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1147 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_P)$. The typical gate charge for a 0.135Ω P-channel power MOSFET is 40nC. This results in $I_{GATECHG}$ = 4mA in 100kHz continuous operation for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control I^2R losses, since overkill can cost efficiency as well as money!
3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω at $V_{IN} \approx 2V_{OUT}$. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.
4. The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A.

Figure 5 shows how the efficiency losses in a typical LTC1147 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses and Schottky diode loss dominate at high load currents.

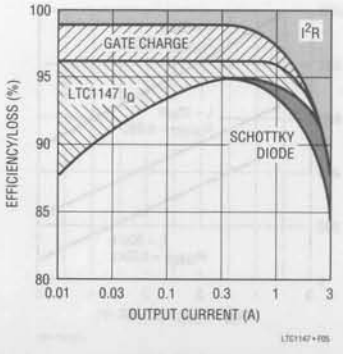


Figure 5. Efficiency Loss

APPLICATIONS INFORMATION

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{OUT} = 3.3V, I_{MAX} = 1A, and f = 130kHz; R_{SENSE}, C_T and L can immediately be calculated:

$$R_{SENSE} = 100mV/1A = 0.1\Omega$$

$$t_{OFF} = (1/130kHz) \times [1 - (3.3/5)] = 2.61\mu s$$

$$C_T = 2.61\mu s/(1.3 \times 10^4) = 220pF$$

$$L = 5.1 \times 10^5 \times 0.1\Omega \times 220pF \times 3.3V = 33\mu H$$

Assume that the MOSFET dissipation is to be limited to P_P = 250mW.

If T_A = 50°C and the thermal resistance of the MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = 0.007(63 - 25) = 0.27$. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{5(0.25)}{3.3(1)^2\,(1.27)} = 0.3\Omega$$

The P-channel requirement can be met by a Si9430DY. Note that the most stringent requirement for the Schottky diode is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst case Schottky diode dissipation rises to:

$$P_D = I_{SC(AVG)} \times V_D$$

With the 0.1Ω sense resistor $I_{SC(AVG)}$ = 1A will result, increasing the 0.4V Schottky diode dissipation to 0.4W.

C_{IN} will require an RMS current rating of at least 0.5A at temperature, and C_{OUT} will require an ESR of 0.1Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing the power dissipation to increase. At $V_{IN(MIN)}$ = 4.5V, the frequency will decrease and the P-channel will be conducting most of the time causing its power dissipation to increase. At $V_{IN(MIN)}$ = 4.5V:

$$f_{MIN} = \frac{1}{2.61\mu s}\left(1 - \frac{3.3}{4.5}\right) = 102kHz$$

$$P_P = \frac{3.3(0.125\Omega)(1A)^2(1.27)}{4.5} = 116mW$$

This last step is necessary to assure that the power dissipation and junction temperature of the P-channel are not exceeded.

Troubleshooting Hints

Since efficiency is critical to LTC1147 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor pin 2.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 6a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 6b. During this time the LTC1147 series are in sleep mode with the quiescent current reduced to 160μA.

The inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

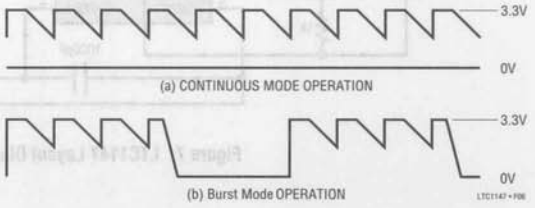


Figure 6. C_T Waveforms

If pin 2 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the **Board Layout Checklist**.

APPLICATIONS INFORMATION

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1147 series. These items are also illustrated graphically in the layout diagram of Figure 7. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1147 ground (pin 7) must return separately to a) the power and b) signal grounds. The power ground (a) returns to the source anode of the Schottky diode, and (–) plate of C_{IN}, which should have lead lengths as short as possible. The signal ground (b) connects to the (–) plate of C_{OUT}.
2. Does the LTC1147 Sense$^-$ (pin 4) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between pins 4 and 5 should be as close as possible to the LTC1147.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the input decoupling capacitor (0.1µF/1µF) connected closely between V_{IN} (pin 1) and ground (pin 7)? This capacitor carries the MOSFET driver peak currents.
6. Is the Shutdown (pin 6) actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

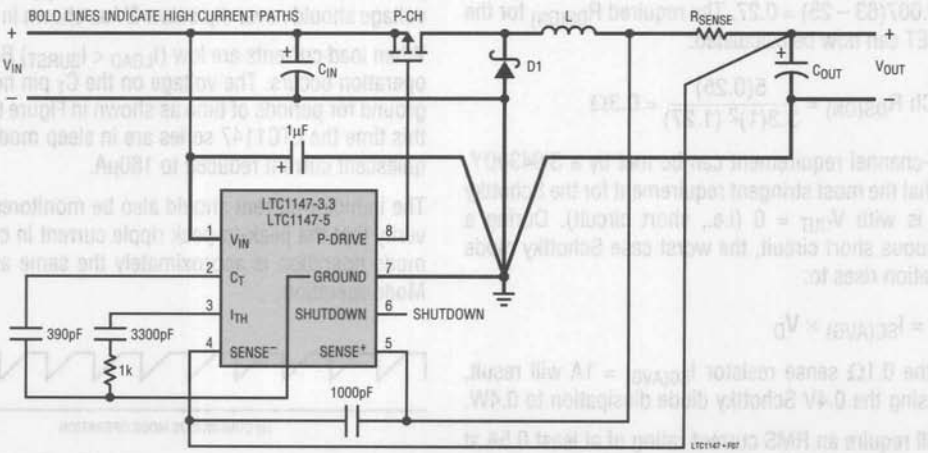


Figure 7. LTC1147 Layout Diagram (See Board Layout Checklist)

For additional High Efficiency application circuits see Application Note 54.

TYPICAL APPLICATIONS

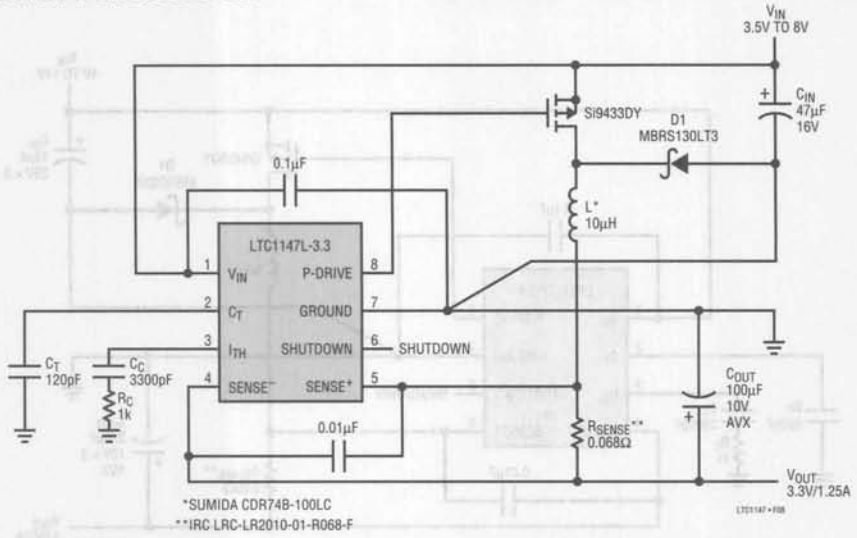


Figure 8. Low Dropout, 3.3V High Efficiency Regulator

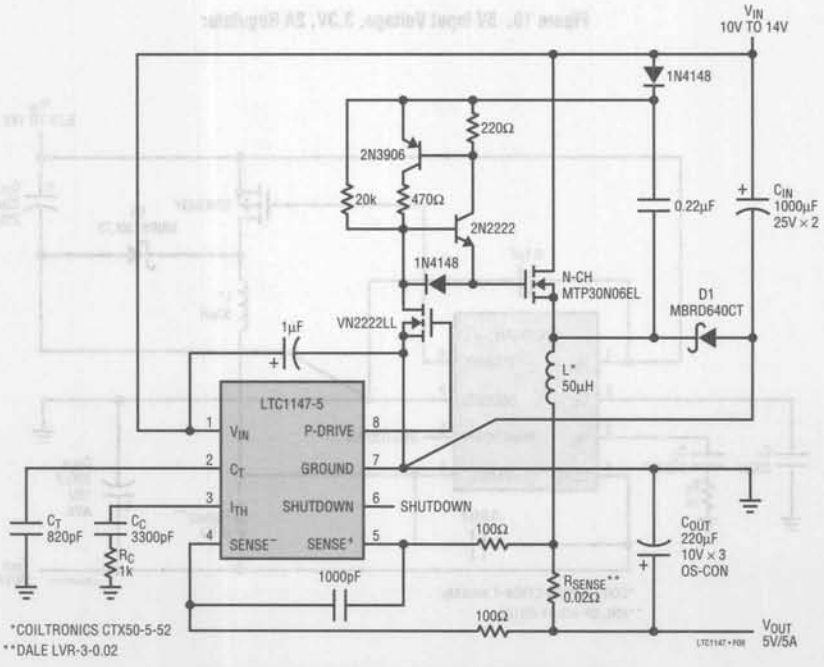


Figure 9. 5V Step-Down Regulator with N-Channel

TYPICAL APPLICATIONS

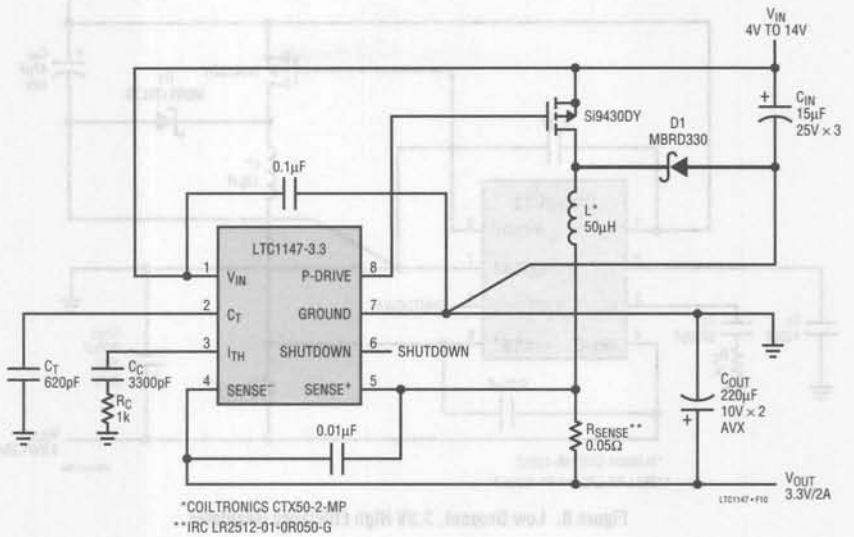


Figure 10. 5V Input Voltage, 3.3V, 2A Regulator

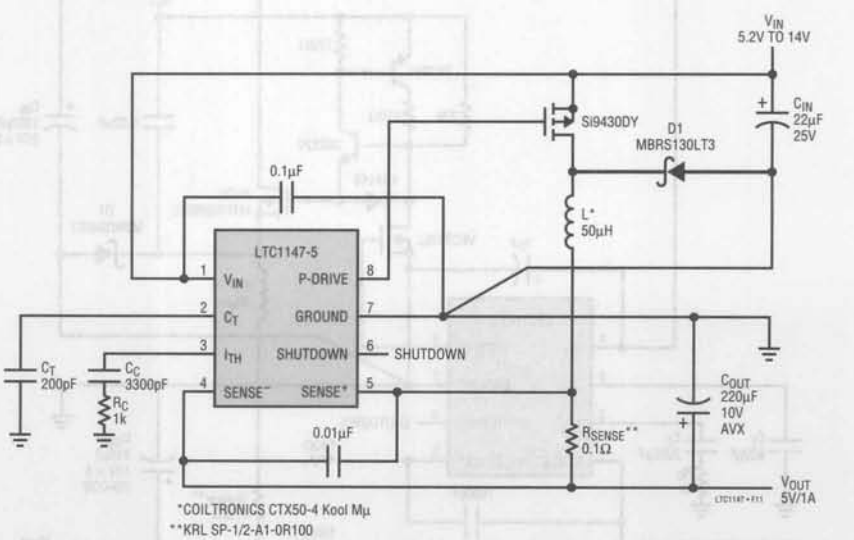


Figure 11. 5V, 1A Output High Efficiency Regulator

High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Ultra-High Efficiency: Over 95% Possible**
- Current-Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Three Decades of Output Current
- Low 160μA Standby Current at Light Loads
- Logic Controlled Micropower Shutdown: I_Q < 20μA
- Wide V_{IN} Range: 3.5V* to 20V
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Adaptive Non-Overlap Gate Drives
- Output Can be Externally Held High in Shutdown
- Available in 14-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC1148 series is a family of synchronous step-down switching regulator controllers featuring automatic **Burst Mode™** operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture providing constant ripple current in the inductor.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V* to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited by only the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

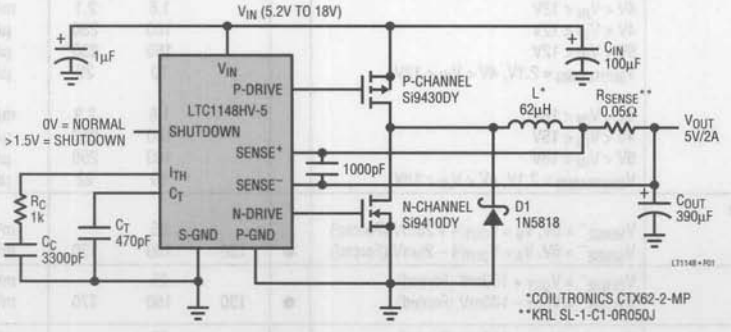
The LTC1148 series combines synchronous switching for maximum efficiency at high currents with an automatic low current operating mode, called **Burst Mode** operation which reduces switching losses. Standby power is reduced to only 2mW at V_{IN} = 10V (at I_{OUT} = 0). Load currents in **Burst Mode** operation are typically 0mA to 300mA.

For operation up to 48V input, see the LTC1149 and LTC1159 data sheest and Application Note 54.

Burst Mode is a trademark of Linear Technology Corporation.
* LTC1148L-3.3 only.

4

TYPICAL APPLICATION



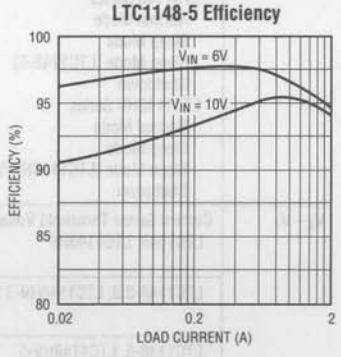


Figure 1. High Efficiency Step-Down Converter

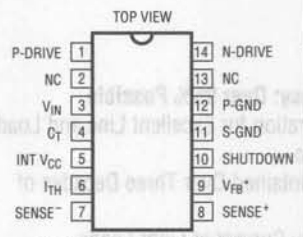
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 3)
- LTC1148 Series ..... 16V to –0.3V
- LTC1148HV Series ..... 20V to –0.3V

Continuous Output Current (Pins 1, 14) 50mA
Sense Voltages (Pins 7, 8)
- LTC1148HV (Adjustable only) ..... 13V to –0.3V
- All Others ..... 10V to –0.3V

Operating Ambient Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 14-LEAD PLASTIC DIP
S PACKAGE 14-LEAD PLASTIC SOIC

*FIXED OUTPUT VERSIONS = NC

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LTC1148CN
LTC1148HVCN
LTC1148CN-3.3
LTC1148HVCN-3.3
LTC1148CN-5
LTC1148HVCN-5
LTC1148CS
LTC1148HVCS
LTC1148CS-3.3
LTC1148LCS-3.3
LTC1148HVCS-3.3
LTC1148CS-5
LTC1148HVCS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_9	Feedback Voltage (LTC1148, LTC1148HV)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_9	Feedback Current (LTC1148, LTC1148HV)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1148-3.3, LTC1148HV-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1148-5, LTC1148HV-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1148-3.3, LTC1148HV-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1148-5, LTC1148HV-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Output Ripple (Burst Mode™)	I_{LOAD} = 0A			50		mV_{P-P}
I_Q	Input DC Supply Current (Note 2)	(Note 6)					
	LTC1148 Series						
	Normal Mode	4V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{IN} < 12V			160	230	µA
	Sleep Mode (LTC1148-5)	6V < V_{IN} < 12V			160	230	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 12V			10	20	µA
	LTC1148HV Series						
	Normal Mode	4V < V_{IN} < 18V			1.6	2.3	mA
	Sleep Mode	4V < V_{IN} < 18V			160	250	µA
	Sleep Mode (LTC1148HV-5)	6V < V_{IN} < 18V			160	250	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 18V			10	22	µA
$V_8 - V_7$	Current Sense Threshold Voltage						
	LTC1148, LTC1148HV	V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 – 25mV (Forced)	●	130	150	170	mV
	LTC1148-3.3, LTC1148HV-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
	LTC1148-5, LTC1148HV-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	130	150	170	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Shutdown Pin Threshold			0.6	0.8	2	V
I_{10}	Shutdown Pin Input Current	0V < $V_{SHUTDOWN}$ < 8V, V_{IN} = 16V			1.2	5	µA
I_4	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT} V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_R, t_F	Driver Output Transition Times	C_L = 3000pF (Pins 1, 14), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_A ≤ 85°C (Note 4), V_{IN} = 10V, unless otherwise noted.

V_9	Feedback Voltage (LTC1148, LTC1148HV)	V_{IN} = 9V		1.20	1.25	1.30	V
ΔV_{OUT}	Regulated Output Voltage LTC1148-3.3, LTC1148HV-3.3 LTC1148-5, LTC1148HV-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA		 3.17 4.85	 3.33 5.05	 3.4 5.2	 V V
I_Q	Input DC Supply Current (Note 2) LTC1148 Series Normal Mode Sleep Mode Sleep Mode Shutdown LTC1148HV Series Normal Mode Sleep Mode Sleep Mode Shutdown	(Note 6) 4V < V_{IN} < 12V 4V < V_{IN} < 12V 6V < V_{IN} < 12V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 12V 4V < V_{IN} < 18V 4V < V_{IN} < 18V 6V < V_{IN} < 18V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 18V		 	 1.6 160 160 10 1.6 160 160 10	 2.4 260 260 22 2.6 280 280 24	 mA µA µA µA mA µA µA µA
$V_8 - V_7$	Current Sense Threshold Voltage LTC1148, LTC1148HV (Note 3)	V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 – 25mV (Forced) V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 + 25mV (Forced)		 125	25 150	 175	mV mV
	LTC1148-3.3, LTC1148HV-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)		 125	25 150	 175	mV mV
	LTC1148-5, LTC1148HV-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)		 125	25 150	 175	mV mV
V_{10}	Shutdown Pin Threshold			0.55	0.8	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA		3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1148CN, LTC1148CN-3.3, LTC1148CN-5: $T_J = T_A + (P_D \times 70°C/W)$
LTC1148CS, LTC1148CS-3.3, LTC1148CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. **See Applications Information.**

Note 3: The LTC1148 and LTC1148HV versions are tested with external feedback resistors resulting in a nominal output voltage of 5V.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

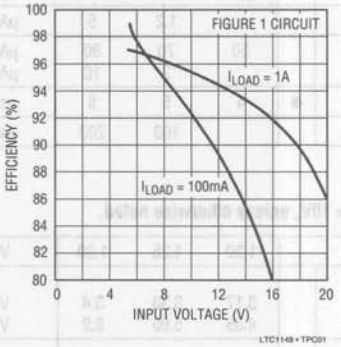
Note 5: The LTC1148 and LTC1148HV series are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

Note 6: The LTC1148L-3.3 allows operation to V_{IN} = 3.5V.

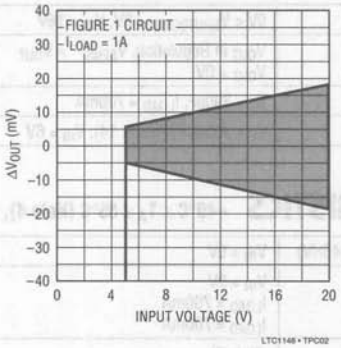
4

TYPICAL PERFORMANCE CHARACTERISTICS

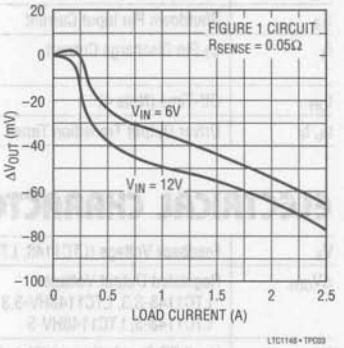
Efficiency vs Input Voltage



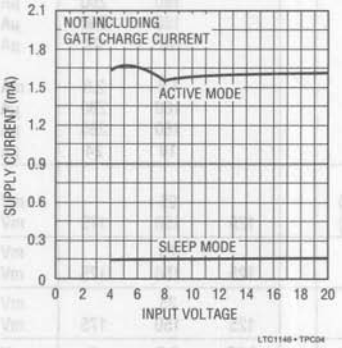
Line Regulation



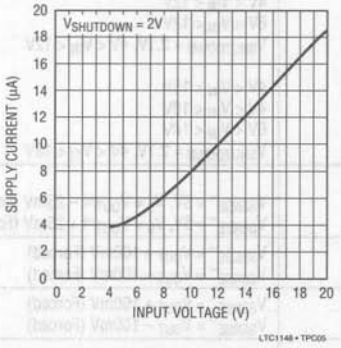
Load Regulation



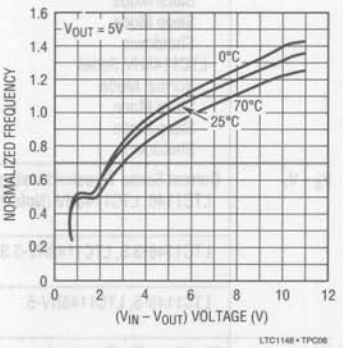
DC Supply Current



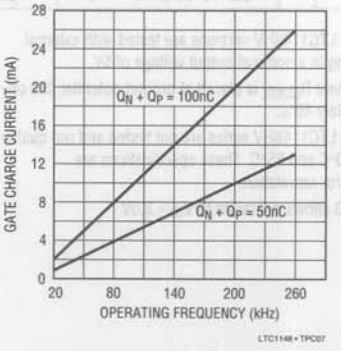
Supply Current in Shutdown



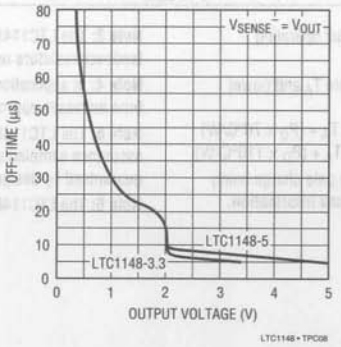
Operating Frequency vs (V_{IN} – V_{OUT})



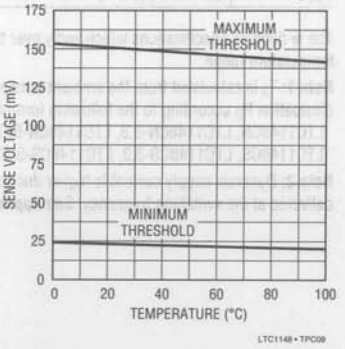
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

Pin 1 (P-Channel Drive): High current drive for top P-channel MOSFET. Voltage swing at this pin is from V_{IN} to ground.

Pin 2 (NC): No connection. Can connect to power ground.

Pin 3 (V_{IN}): Main supply pin. Must be closely decoupled to power ground pin 12.

Pin 4 (C_T): External capacitor C_T from pin 4 to ground sets the operating frequency. The actual frequency is also dependent upon the input voltage.

Pin 5 (Int V_{CC}): Internal supply voltage, nominally 3.3V. Can be decoupled to signal ground. Do not externally load this pin.

Pin 6 (I_{TH}): Gain amplifier decoupling point. The current comparator threshold increases with the pin 6 voltage.

Pin 7 (Sense$^-$): Connects to internal resistive divider which sets the output voltage in LTC1148-3.3 and LTC1148-5 versions. Pin 7 is also the (–) input for the current comparator.

Pin 8 (Sense$^+$): The (+) input to the current comparator. A built in offset between pins 7 and 8 in conjunction with R_{SENSE} sets the current trip threshold.

Pin 9 (V_{FB}): For the LTC1148 adjustable version, pin 9 serves as the feedback pin from an external resistive divider used to set the output voltage. On LTC1148-3.3 and LTC1148-5 versions this pin is not used.

Pin 10 (Shutdown): When grounded, the LTC1148 series operates normally. Pulling pin 10 high holds both MOSFETs off and puts the LTC1148 series in micropower shutdown mode. Requires CMOS logic signal with t_R, $t_F < 1\mu s$, should not be left floating

Pin 11 (S-Ground): Small signal ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

Pin 12 (P-Ground): Driver power ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

Pin 13 (NC): No connection. Can connect to power ground.

Pin 14 (N-Channel Drive): High current drive for bottom N-channel MOSFET. Voltage swing at pin 14 is from ground to V_{IN}.

4

OPERATION

The LTC1148 series uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the timing cap pin 4.

The output voltage is sensed by an internal voltage divider connected to Sense$^-$ pin 7 (LTC1148-3.3 and LTC1148-5) or external divider returned to V_{FB} pin 9 (LTC1148). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1148 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 7 and 8 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 4 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by pin 7) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-drive output goes to V_{IN}, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-drive output to go low (turning off the N-channel MOSFET) and the P-drive output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

OPERATION

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (pin 6) to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{\text{sleep}}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160µA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and the process repeats.

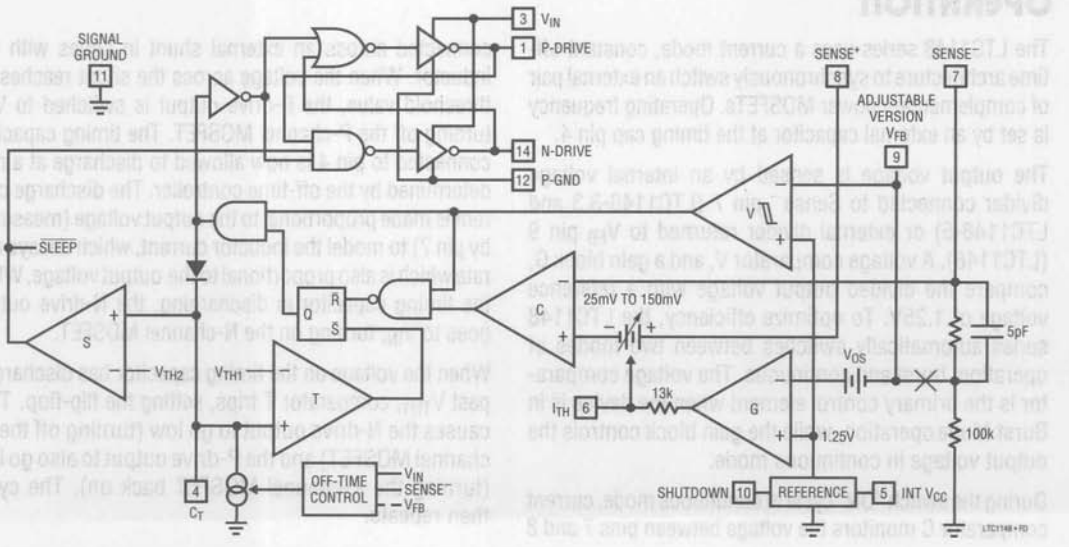
To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset (V_{OS}) is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-drive output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low while the N-drive output is high.

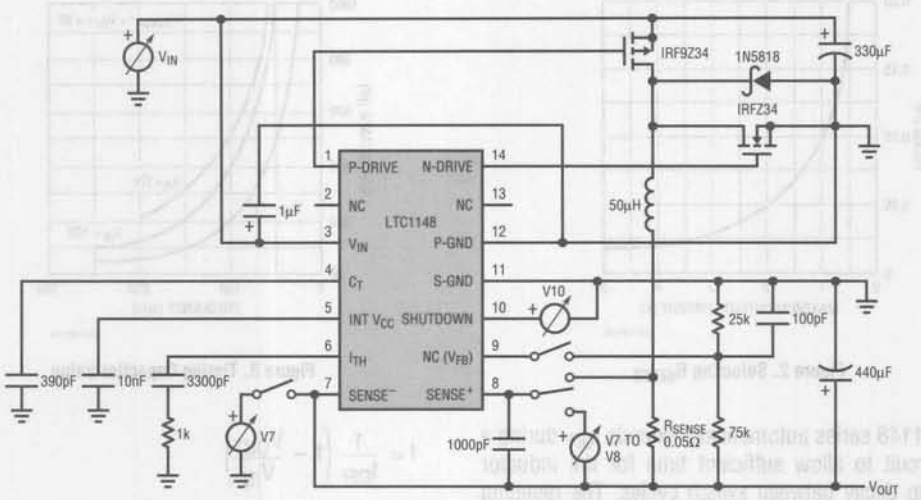
Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing extremely low dropout operation.

FUNCTIONAL DIAGRAM

Pin 9 connection shown for LTC1148-3.3 and LTC1148-5; changes create LTC1148.



TEST CIRCUIT



4

APPLICATIONS INFORMATION

The basic LTC1148 series application circuit (fixed output versions) is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 20V. If the application requires higher input voltage, then the LTC1149 or LTC1159 should be used.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1148 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 25mV/R_{SENSE}$ (See **C_T and L Selection for Operating Frequency**). Solving for R_{SENSE} and allowing a margin for variations in the LTC1148 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

APPLICATIONS INFORMATION

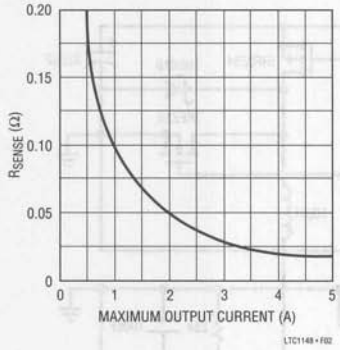


Figure 2. Selecting R_{SENSE}

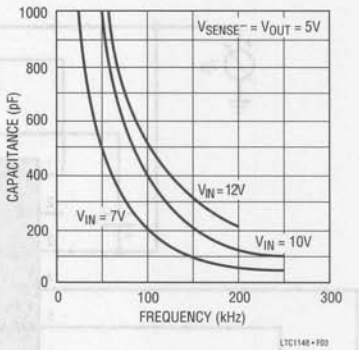


Figure 3. Timing Capacitor Value

The LTC1148 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1148 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{1}{2.6 \times 10^4 \times f}$$

Assumes $V_{IN} = 2V_{OUT}$, Figure 1 circuit.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see **Efficiency Considerations**). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1148 series reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $25mV/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1148 series may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

APPLICATIONS INFORMATION

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, Kool Mμ® on molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids, with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies, but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1148 series: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. The LTC1148/LTC1148HV series supply voltage must always be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1148 series is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_P}{V_{OUT} \times I_{MAX}^2 \times (1 + \delta_P)}$$

$$\text{N-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_N}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times (1 + \delta_N)}$$

where P_P and P_N are the allowable power dissipations and d_P and d_N are the temperature dependencies of $R_{DS(ON)}$. P_P and P_N will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1 + d) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but d = 0.007/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diode D1 shown in Figure 1 only conducts during the dead-time between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large

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APPLICATIONS INFORMATION

voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX}\ \frac{[V_{OUT}(V_{IN}-V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on V_{IN} pin 3 for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1148 series:*

$$C_{OUT}\ \text{Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1148 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

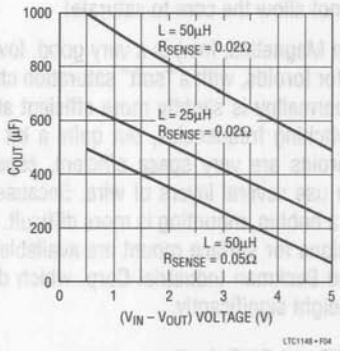


Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability

APPLICATIONS INFORMATION

problem. The pin 6 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power).

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1148 series circuits: 1) LTC1148 DC bias current, 2) MOSFET gate charge current, and 3) I^2R losses.

1. The DC supply current is the current which flows into V_{IN} pin 3 less the gate charge current. For V_{IN} = 10V the LTC1148 DC supply current is 160µA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1148 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATECHG}$ = 7.5mA in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!
3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.

   Figure 5 shows how the efficiency losses in a typical LTC1148 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses dominate at high load currents.

4

APPLICATIONS INFORMATION

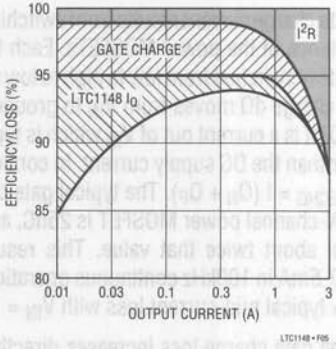


Figure 5. Efficiency Loss

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{OUT} = 5V, I_{MAX} = 2A, and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$$R_{SENSE} = 100mV/2 = 0.05\Omega$$

$$t_{OFF} = (1/200kHz) \times [1 - (5/12)] = 2.92\mu s$$

$$C_T = 2.92\mu s/(1.3 \times 10^4) = 220pF$$

$$L_{MIN} = 5.1 \times 10^5 \times 0.05\Omega \times 220pF \times 5V = 28\mu H$$

Assume that the MOSFET dissipations are to be limited to $P_N = P_P = 250mW$.

If T_A = 50°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = \delta_N = 0.007(63 - 25) = 0.27$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2\,(1.27)} = 0.12\Omega$$

$$\text{N-Ch } R_{DS(ON)} = \frac{12(0.25)}{7(2)^2\,(1.27)} = 0.085\Omega$$

The P-channel requirement can be met by a Si9430DY, while the N-channel requirement is exceeded by a Si9410DY. Note that the most stringent requirement for the N-channel MOSFET is with $V_{OUT} = 0$ (i.e., short circuit). During a continuous short circuit, the worst case N-channel dissipation rises to:

$$P_N = I_{SC(AVG)}{}^2 \times R_{DS(ON)} \times (1 + \delta_N)$$

With the 0.05Ω sense resistor $I_{SC(AVG)}$ = 2A will result, increasing the 0.085Ω N-channel dissipation to 450mW at a die temperature of 73°C.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V:

$$f_{MIN} = (1/2.92\mu s)[1 - (5V/7V)] = 98kHz$$

$$P_P = \frac{5V(0.12\Omega)(2A)^2(1.27)}{7V} = 435mW$$

This last step is necessary to assure that the power dissipation and junction temperature of the P-channel are not exceeded.

LTC1148 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1148 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} pin 9 (see Figure 9). The regulated voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1148.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

APPLICATIONS INFORMATION

Auxiliary Windings – Suppressing Burst Mode Operation

The LTC1148 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 6. Two 100Ω resistors are inserted in series with the leads from the sense resistor.

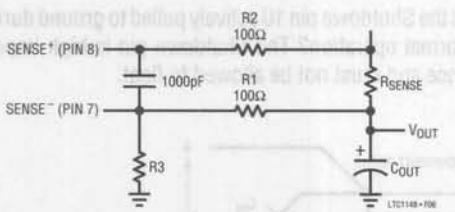


Figure 6. Suppression of Burst Mode™ Operation

With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the minimum threshold will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 7 and 8.

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing cap pin 4 above 1.5V when the output voltage is greater than the desired regulated value will turn "on" the N-channel MOSFET.

A fault condition which causes the output voltage to go above a maximum allowable value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will cause large currents to flow and blow the system fuse.

The N-channel MOSFET needs to be sized so it will safely handle this over current condition. The typical delay from pulling the C_T pin high and the N drive pin 14 going high is 250ns. Note: Under shutdown conditions, the N-channel is held OFF and pulling the C_T pin high will not cause the N-channel MOSFET to crowbar the output.

A simple N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1148 as shown in Figure 7.

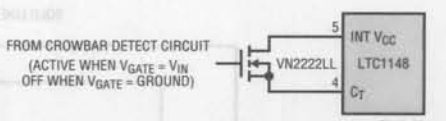


Figure 7. Output Crowbar Interface

Troubleshooting Hints

Since efficiency is critical to LTC1148 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor pin 4.

In continuous mode (I_{LOAD} > I_{BURST}) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 8a.

When load currents are low (I_{LOAD} < I_{BURST}) Burst Mode operation should occur with the C_T pin waveform periodically falling to ground as shown in Figure 8b.

APPLICATIONS INFORMATION

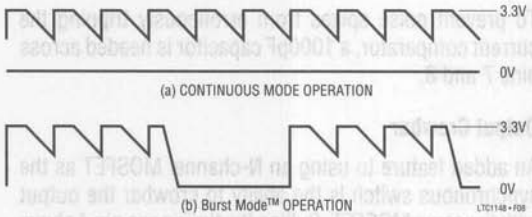


Figure 8. C_T Waveforms

If pin 4 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the **Board Layout Checklist.**

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1148 series. These items are also illustrated graphically in the layout diagram of Figure 9. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1148 signal ground pin 11 must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1148 Sense$^-$ pin 7 connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between pins 7 and 8 should be as close as possible to the LTC1148.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the 1µF V_{IN} decoupling capacitor connected closely between pin 3 and power ground pin 12? This capacitor carries the MOSFET driver peak currents.
6. Is the Shutdown pin 10 actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

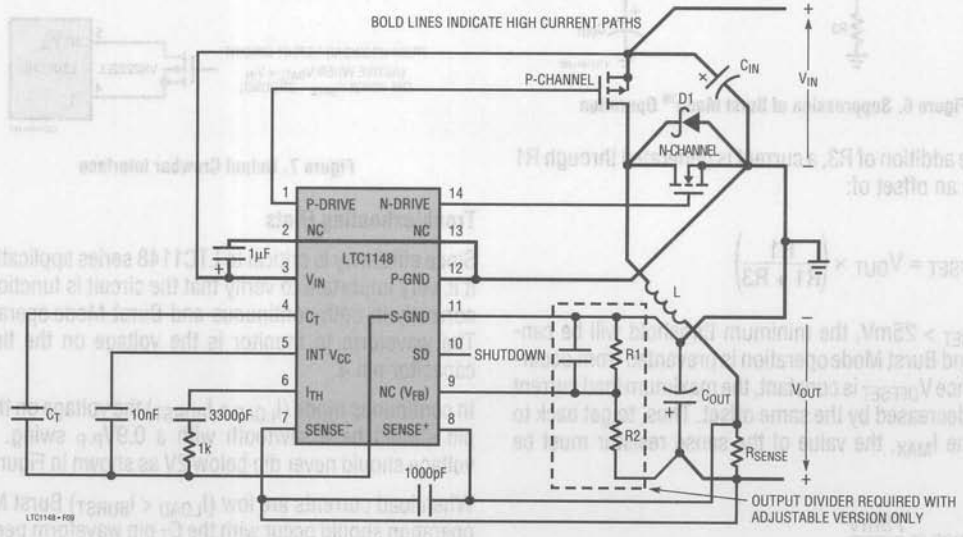


Figure 9. LTC1148 Layout Diagram (See Board Layout Checklist)

TYPICAL APPLICATIONS

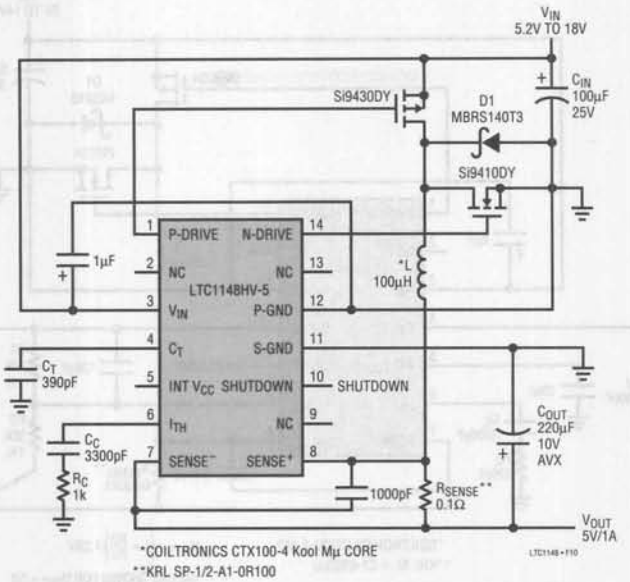


Figure 10. 5V/1A High Efficiency Regulator with Extended Input Voltage Range

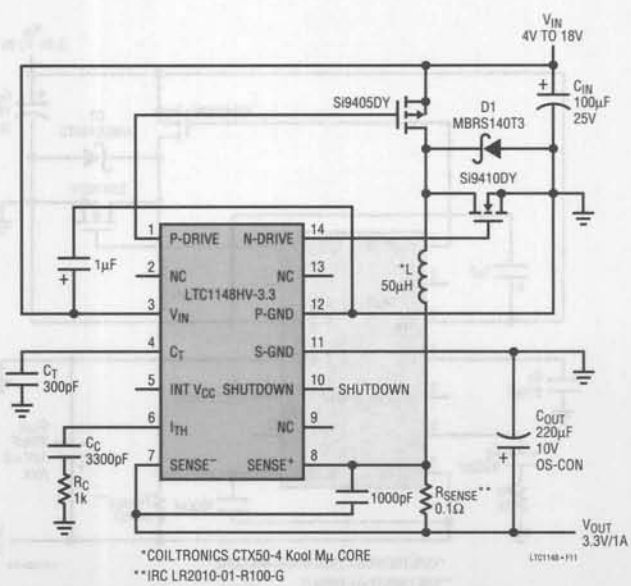


Figure 11. High Efficiency 5V to 3.3V/1A Converter with Extended Input Voltage Range

TYPICAL APPLICATIONS

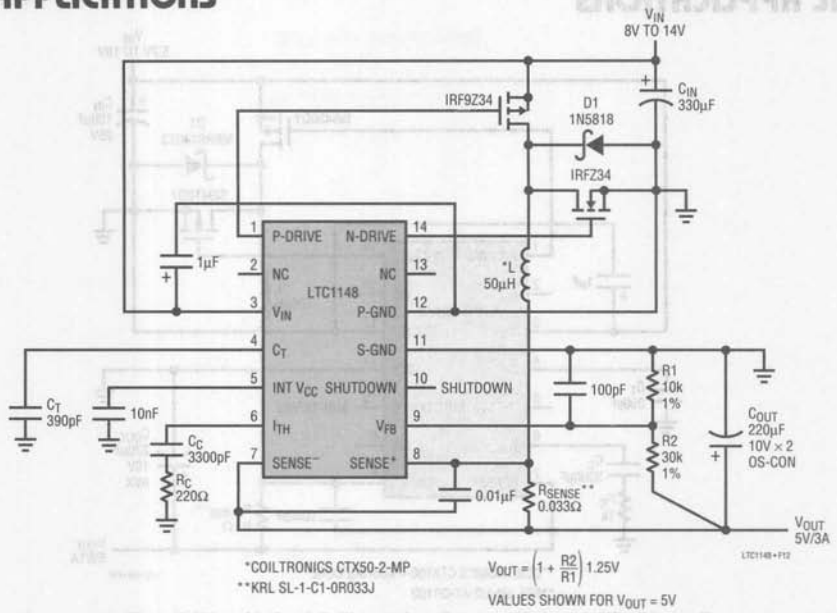


Figure 12. High Efficiency Adjustable 3A Regulator

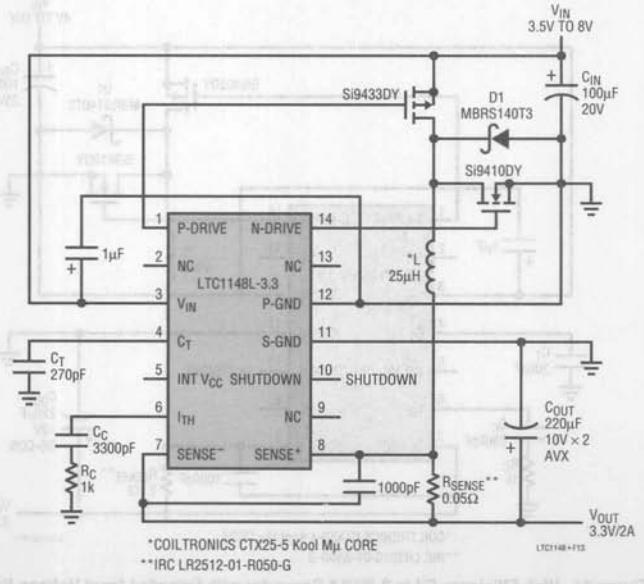


Figure 13. Low Dropout, 3.3V/2A High Efficiency Regulator

TYPICAL APPLICATIONS

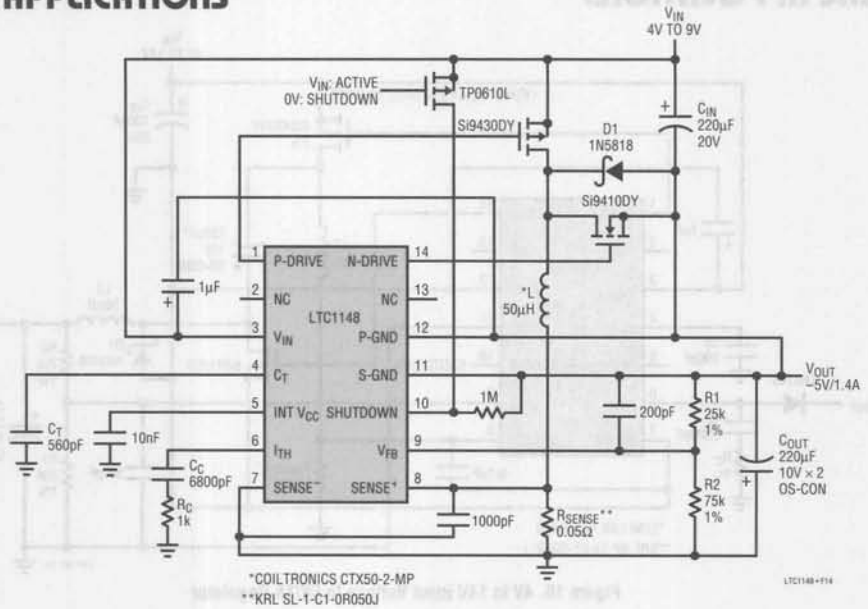


Figure 14. 4V to 9V Input Voltage to –5V/1A Regulator

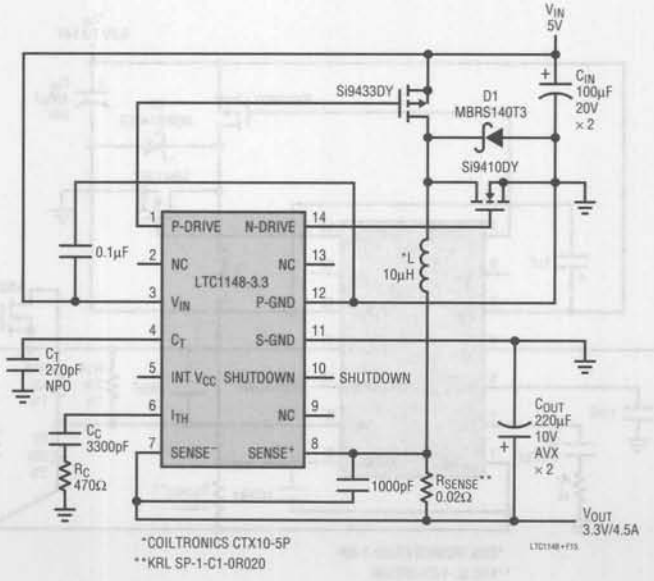


Figure 15. High Efficiency 5V to 3.3V/4.5A Converter

TYPICAL APPLICATIONS

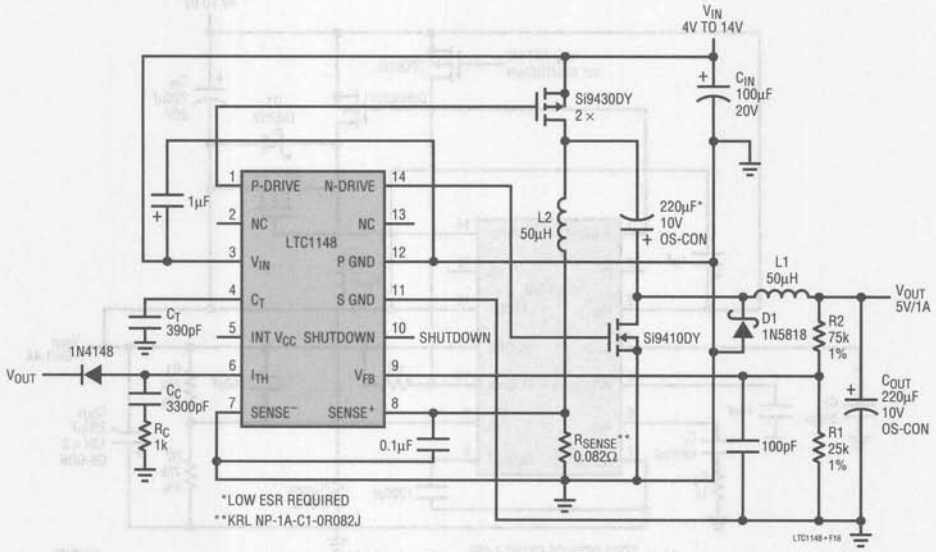


Figure 16. 4V to 14V Input Voltage to 5V/1A Regulator

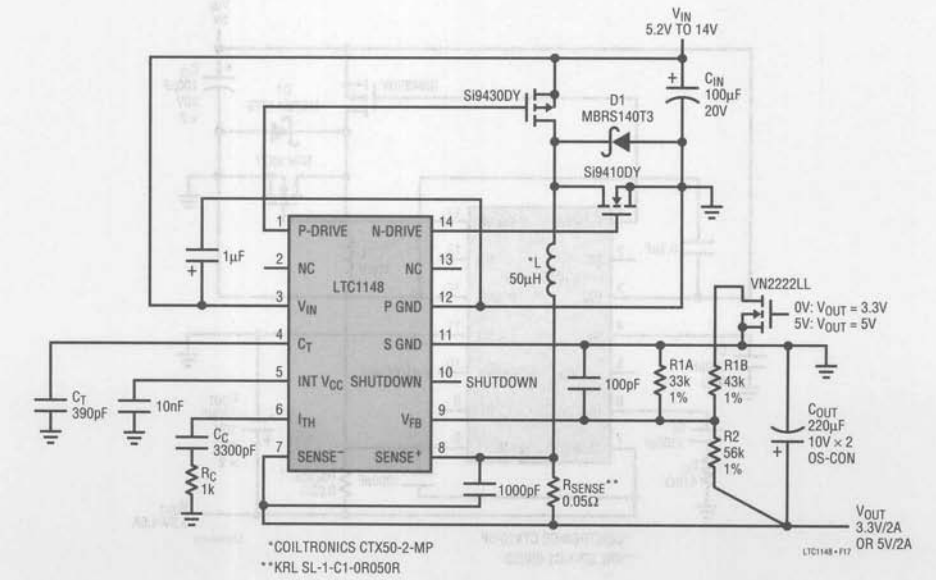


Figure 17. Logic Selectable 5V/1A or 3.3V/1A High Efficiency Regulator

TYPICAL APPLICATIONS

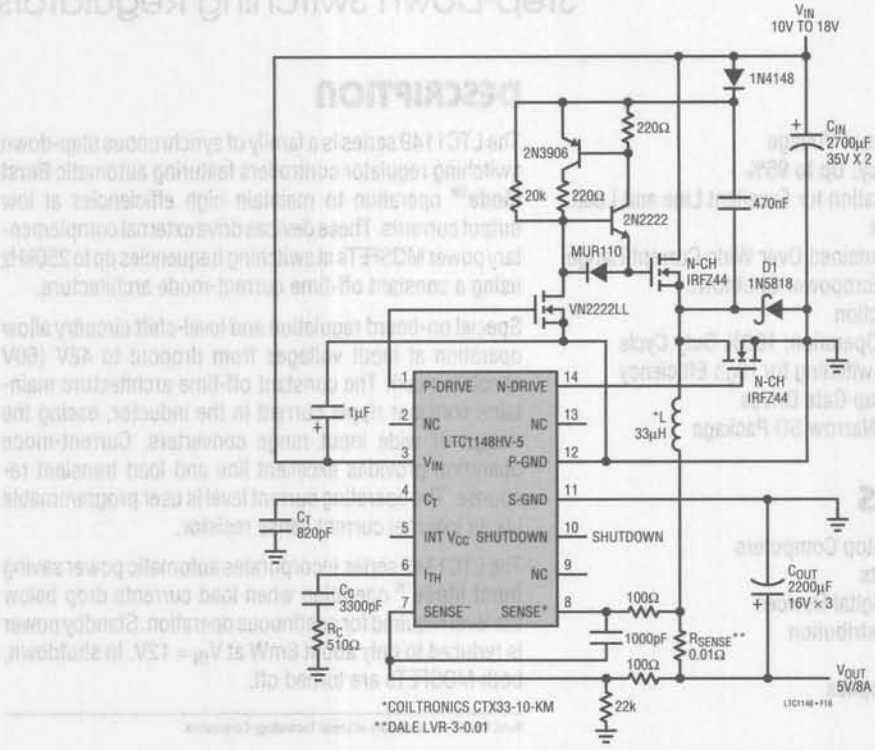
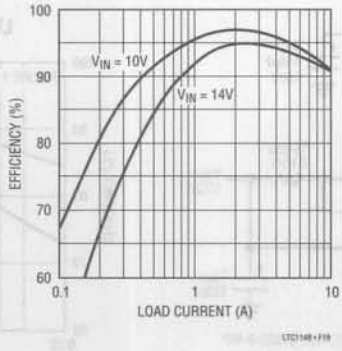


Figure 18. All N-Channel 5V/8A High Efficiency Regulator (Burst Mode™ Operation Suppressed)



For additional high efficiency application circuits, see Application Note 54

Figure 19. All N-Channel 5V/8A Efficiency

High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- Operation to 48V Input Voltage
- **Ultra High Efficiency: Up to 95%**
- Current-Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Wide Current Range
- Logic Controlled Micropower Shutdown
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Adaptive Non-Overlap Gate Drives
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

DESCRIPTION

The LTC1149 series is a family of synchronous step-down switching regulator controllers featuring automatic **Burst Mode™** operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture.

Special on-board regulation and level-shift circuitry allow operation at input voltages from dropout to 48V (60V absolute max). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The LTC1149 series incorporates automatic power saving **Burst Mode™** operation when load currents drop below the level required for continuous operation. Standby power is reduced to only about 8mW at V_{IN} = 12V. In shutdown, both MOSFETs are turned off.

Burst Mode™ is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

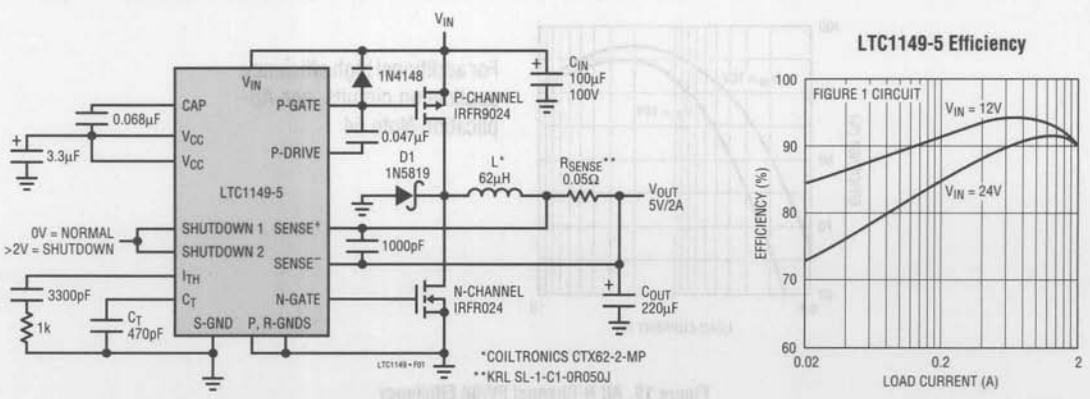
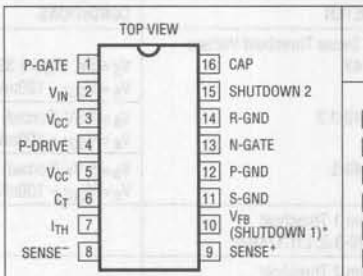


Figure 1. High Efficiency Step-Down Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –15V to 60V
V_{CC} Output Current (Pin 3) 50mA
V_{CC} Input Voltage (Pin 5) 16V
Continuous Output Current (Pins 4, 13) 50mA
Sense Voltages (Pins 8, 9) ..... –0.3V to V_{CC}
Shutdown Voltages (Pins 10, 15) 7V
Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOIC

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LTC1149CN
LTC1149CN-3.3
LTC1149CN-5
LTC1149CS
LTC1149CS-3.3
LTC1149CS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage (LTC1149 Only)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_{10}	Feedback Current (LTC1149 Only)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1149-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1149-5	I_{LOAD} = 700mA	●	4.9	5.05	5.2	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 48V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1149-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1149-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Burst Mode™ Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_2	Input DC Supply Current (Note 3)						
	Normal Mode	V_{IN} = 12V			2.0	2.8	mA
		V_{IN} = 48V			2.2	3.0	mA
	Burst Mode™	V_{IN} = 12V			0.6	0.9	mA
		V_{IN} = 48V			0.8	1.1	mA
	Shutdown	V_{IN} = 12V, V_{15} = 2V			135	170	µA
		V_{IN} = 48V, V_{15} = 2V			300	390	µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V, I_3 = 20mA	●	9.75	10.25	11	V
$V_2 - V_3$	V_{CC} Dropout Voltage	V_{IN} = 5V, I_3 = 10mA			200	250	mV
$V_{IN} - V_1$	P-Gate to Source Voltage (Off)	V_{IN} = 12V	●	–0.2	0		V
		V_{IN} = 48V	●	–0.2	0		V

4

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_9 - V_8$	Current Sense Threshold Voltage LTC1149	V_8 = 5V, V_{10} = 1.32V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	25 150	 170	mV mV
	LTC1149-3.3	V_8 = 3.5V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	25 150	 170	mV mV
	LTC1149-5	V_8 = 5.3V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	25 150	 170	mV mV
V_{10}	Shutdown 1 Threshold LTC1149-3.3, LTC1149-5			0.6	0.8	2	V
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
I_{15}	Shutdown 2 Input Current	V_{15} = 5V			18	25	µA
I_6	C_T Pin Discharge Current	V_{OUT} In Regulation, V_{SENSE}^- = V_{OUT} V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 4, 13), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_A ≤ 85°C (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage LTC1149 Only			1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage LTC1149-3.3 LTC1149-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA		 3.17 4.85	 3.33 5.05	 3.4 5.2	 V V
I_2	Input DC Supply Current (Note 3) Normal Mode	 V_{IN} = 12V V_{IN} = 48V			 2.0 2.2	 3.2 3.5	 mA mA
	Burst Mode™	V_{IN} = 12V V_{IN} = 48V			0.6 0.8	1.05 1.30	mA mA
	Shutdown	V_{IN} = 12V, V_{15} = 2V V_{IN} = 48V, V_{15} = 2V			135 300	230 520	µA µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V I_3 = 20mA		9.75	10.25	11	V
$V_9 - V_8$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)		 125	25 150	 175	mV mV
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1149CN, LTC1149CN-3.3, LTC1149CN-5: $T_J = T_A + (P_D \times 70°C/W)$
LTC1149CS, LTC1149CS-3.3, LTC1149CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: Pin 10 is a shutdown pin on the LTC1149-3.3 and LTC1149-5 fixed output voltage versions and must be at ground potential for testing.

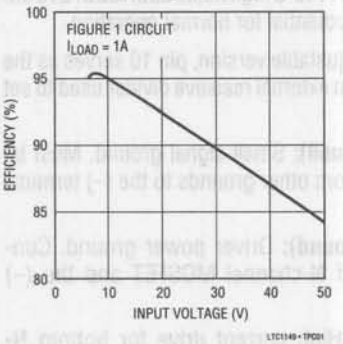
Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages. **See Typical Performance Characteristics and Applications Information.**

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

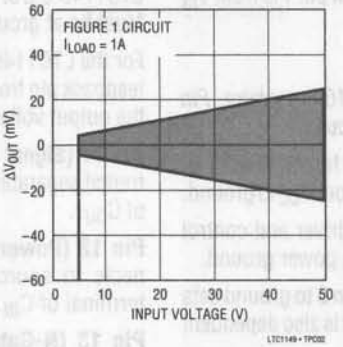
Note 5: The LTC1149, LTC1149-3.3, and LTC1149-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

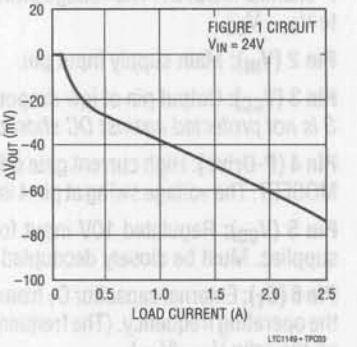
Efficiency vs Input Voltage



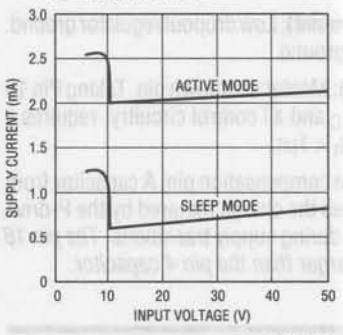
Line Regulation



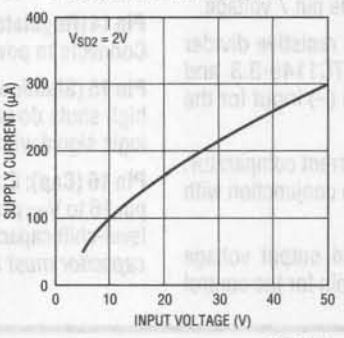
Load Regulation



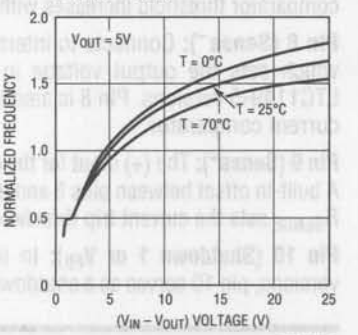
DC Supply Current



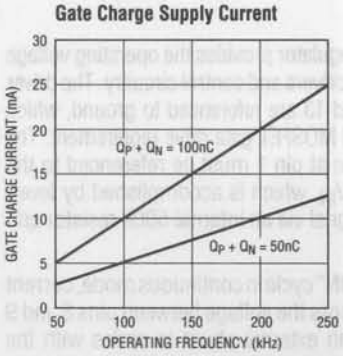
Supply Current in Shutdown



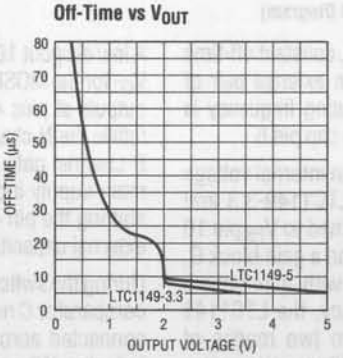
Operating Frequency vs (V_{IN} – V_{OUT})



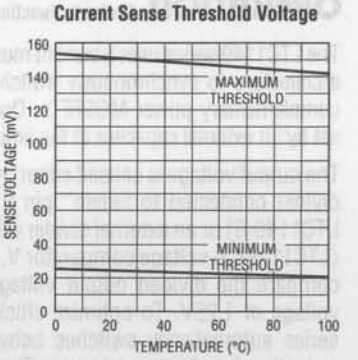
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

Pin 1 (P-Gate): Level-shifted gate drive signal for top P-channel MOSFET. The voltage swing at pin 1 is from V_{IN} to $V_{IN} - V_{CC}$.

Pin 2 (V_{IN}): Main supply input pin.

Pin 3 (V_{CC}): Output pin of low dropout 10V regulator. *Pin 3 is not protected against DC short circuits.*

Pin 4 (P-Drive): High current gate drive for top P-channel MOSFET. The voltage swing at pin 4 is from V_{CC} to ground.

Pin 5 (V_{CC}): Regulated 10V input for driver and control supplies. Must be closely decoupled to power ground.

Pin 6 (C_T): External capacitor C_T from pin 6 to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

Pin 7 (I_{TH}): Gain amplifier decoupling point. The current comparator threshold increases with the pin 7 voltage.

Pin 8 (Sense$^-$): Connects to internal resistive divider which sets the output voltage in LTC1149-3.3 and LTC1149-5 versions. Pin 8 is also the (–) input for the current comparator.

Pin 9 (Sense$^+$): The (+) input for the current comparator. A built-in offset between pins 8 and 9 in conjunction with R_{SENSE} sets the current trip threshold.

Pin 10 (Shutdown 1 or V_{FB}): In fixed output voltage versions, pin 10 serves as a shutdown pin for the control circuitry only (V_{CC} is not affected). Taking pin 10 of the LTC1149-3.3 or LTC1149-5 high holds both MOSFETs off. Must be at ground potential for normal operation.

For the LTC1149 adjustable version, pin 10 serves as the feedback pin from an external resistive divider used to set the output voltage.

Pin 11 (Signal Ground): Small signal ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

Pin 12 (Power Ground): Driver power ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

Pin 13 (N-Gate): High current drive for bottom N-channel MOSFET. The voltage swing at pin 13 is from ground to V_{CC}.

Pin 14 (Regulator Ground): Low dropout regulator ground. Connects to power ground.

Pin 15 (Shutdown 2): Master shutdown pin. Taking Pin 15 high shuts down V_{CC} and all control circuitry; requires a logic signal with t_r, $t_f < 1\mu s$.

Pin 16 (Cap): Charge compensation pin. A capacitor from pin 16 to V_{CC} provides the charge required by the P-drive level-shift capacitor during supply transitions. *The pin 16 capacitor must be larger than the pin 4 capacitor.*

OPERATION (Refer to Functional Diagram)

The LTC1149 series uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the timing cap pin 6.

The output voltage is sensed either by an internal voltage divider connected to Sense$^-$ pin 8 (LTC1149-3.3 and LTC1149-5) or an external divider returned to V_{FB} pin 10 (LTC1149). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1149 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element for Burst Mode™ operation, while the gain block controls the output voltage in continuous mode.

A low dropout 10V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry. The driver outputs at pins 4 and 13 are referenced to ground, which fulfills the N-channel MOSFET gate drive requirement. The P-channel gate drive at pin 1 must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the pin 4 signal via an internal 500k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 8 and 9 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-gate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 6 is now allowed to discharge at a rate

OPERATION (Refer to Functional Diagram)

determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by pin 8) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-gate output is high, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-gate output to go low (turning off the N-channel MOSFET) and the P-gate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode™ operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep bar line to go low and the N-channel MOSFET to turn off.

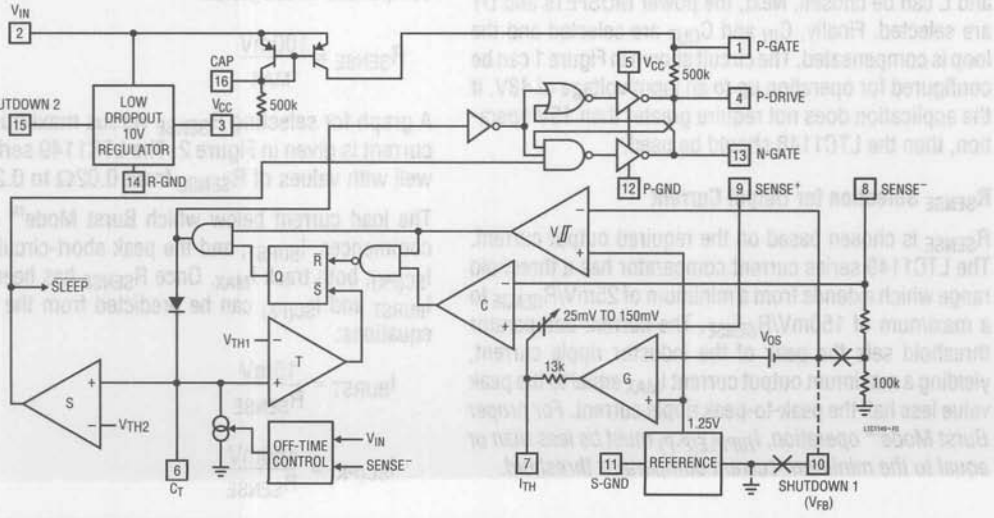
The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several mA (with the MOSFETs switching) to 600µA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode™ operation, a built-in offset is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

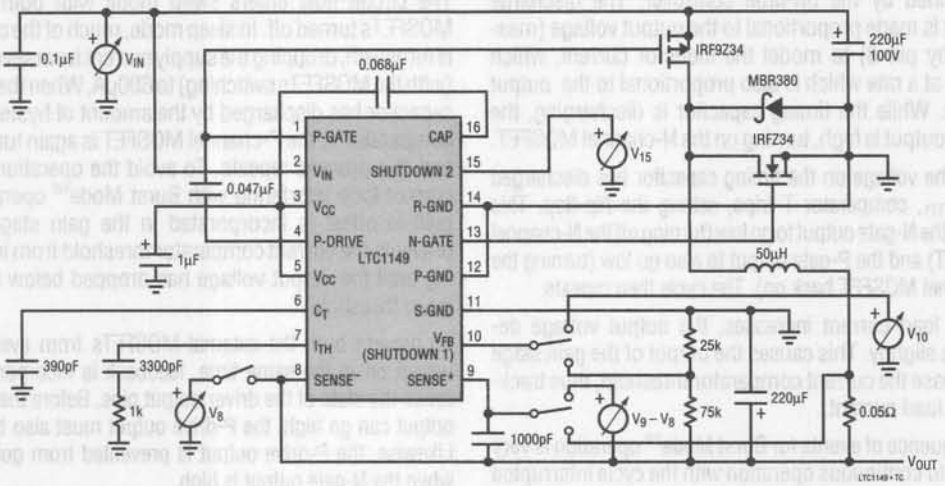
Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously.

4

FUNCTIONAL DIAGRAM Pin 10 connection shown for LTC1149-3.3 and LTC1149-5; changes create LTC1149.



TEST CIRCUIT



APPLICATIONS INFORMATION

Typical Application Circuit

The basic LTC1149 series application circuit is shown in Figure 1. External component selection is driven by the input voltage and output load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 48V. If the application does not require greater than 15V operation, then the LTC1148 should be used.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1149 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode™ operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see **C_T and L Selection for Operating Frequency**). Solving for R_{SENSE} and allowing a margin for variations in the LTC1149 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1149 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode™ operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

APPLICATIONS INFORMATION

The LTC1149 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

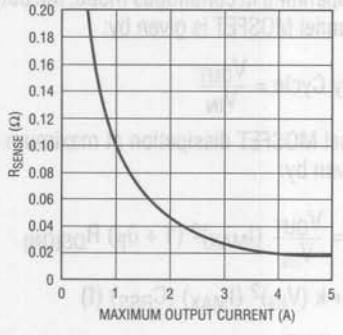


Figure 2. R_{SENSE} vs Maximum Output Current

L and C_T Selection for Operating Frequency

The LTC1149 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{7.8 \times 10^{-5}}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see **Efficiency Considerations**). The complete expression for operating frequency is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V), while V_{OUT} is the actual output voltage. Thus $V_{REG}/V_{OUT} = 1$ when in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1149 series reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1149 series may not enter Burst Mode™ operation and efficiency will be severely degraded at low currents.

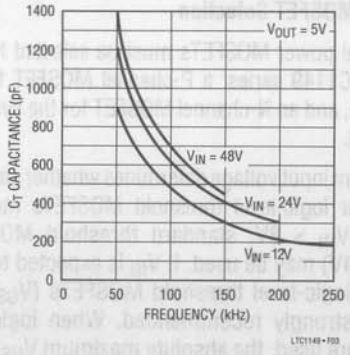


Figure 3. Timing Capacitor Selection

APPLICATIONS INFORMATION

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode™ operation to be falsely triggered in the LTC1149 series. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ®. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

P-Channel MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1149 series: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are strongly recommended. When logic-level MOSFETs are used, the absolute maximum V_{GS} rating for the MOSFETs must be greater than the LTC1149 series internal regulator voltage V_{CC}.

Selection criteria for the P-channel MOSFET include the on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1149 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

The P-channel MOSFET dissipation at maximum output current is given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P) R_{DS(ON)} + k (V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and k is a constant related to the gate drive current. Note the two distinct terms in the equation. The first gives the I^2R losses, which are highest at low input voltages, while the second gives the transition losses, which are highest at high input voltages. For V_{IN} < 24V, the high current efficiency generally improves with larger MOSFETs (although gate charge losses begin eating into the gains. See **Efficiency Considerations**). For V_{IN} > 24V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. This is illustrated in the **Design Example** section.

The term (1 + ∂) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but ∂ = 0.007/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant k is much harder to pin down, but k = 5 can be used for the LTC1149 series to estimate the relative contributions of the two terms in the P-channel dissipation equation.

N-Channel MOSFET and D1 Selection

The same input voltage constraints apply to the N-channel MOSFET as to the P-channel with regard to when logic-

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APPLICATIONS INFORMATION

level devices are required. However, the dissipation calculation is quite different. The duty cycle and dissipation for the N-channel MOSFET operating in continuous mode are given by:

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$. Note that there is no transition loss term in the N-channel dissipation equation because the drain-to-source voltage is always low when the N-channel MOSFET is turning on or off. The remaining I^2R losses are the greatest at high input voltage or during a short circuit, when the N-channel duty cycle is nearly 100%. Fortunately, low $R_{DS(ON)}$ N-channel MOSFETs are readily available which reduce losses to the point that heat sinking is not required, even during continuous short-circuit operation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead-time between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

Finally, both MOSFETs and D1 must be selected for breakdown voltages higher than the maximum V_{IN}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX} [V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1149 series:

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode™ operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon, Chemicon, and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size, at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

APPLICATIONS INFORMATION

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode™ operation to be activated when the LTC1149 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

Checking Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The pin 7 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

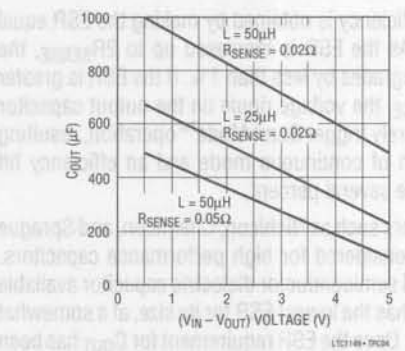

Figure 4. Minimum Suggested C_{OUT}

LTC1149 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1149 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} pin 10. The regulated voltage is determined:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

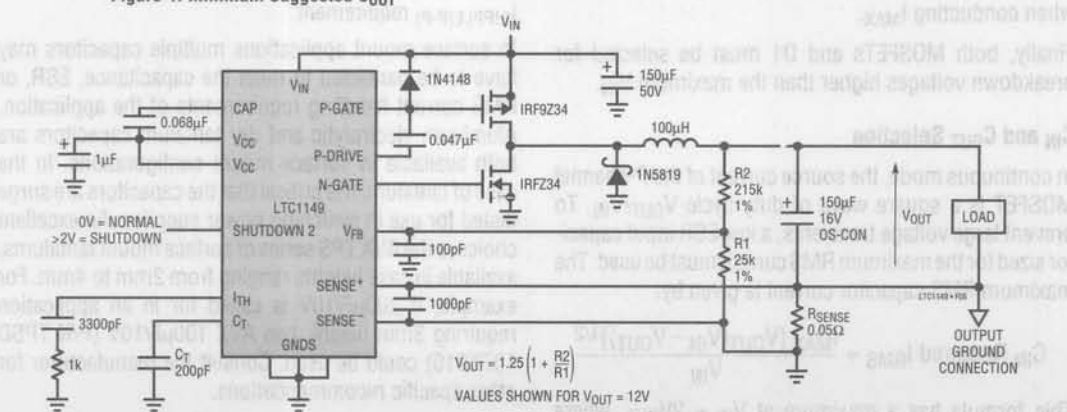

Figure 5. High Efficiency Step-Down Regulator with $V_{OUT} > V_{CC}$

APPLICATIONS INFORMATION

In applications where V_{OUT} is greater than the LTC1149 internally regulated V_{CC} voltage, R_{SENSE} must be moved to the ground side of the output to prevent the absolute maximum voltage ratings of the sense pins from being exceeded. This is shown in Figure 5. When the current sense comparator is operating at 0V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1149 series circuits: 1) LTC1149 DC supply current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) P-channel transition losses.

1) The DC supply current is the current which flows into V_{IN} pin 2 less the gate charge current. For V_{IN} = 12V the LTC1149 DC supply current is 0.6mA for no load, and increases proportionally with load up to 2mA after the LTC1149 series has entered continuous mode. Because the DC supply current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 24V, the DC bias losses are generally less than 3% for load currents over 300mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATECHG}$ = 7.5mA in 100kHz continuous operation, for a 5% to 10% typical mid-current loss with V_{IN} = 24V.

Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3) I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.

4) Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 24V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} \approx 5(V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

For example, if V_{IN} = 48V, I_{MAX} = 2A, C_{RSS} = 300pF (a very large MOSFET), and f = 100kHz, the transition loss is 0.7W. A loss of this magnitude would not only kill efficiency but would probably require additional heat sinking for the MOSFET! See **Design Example** for further guidelines on how to select the P-channel MOSFET.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

LTC1149 Package Dissipation

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maxi-

4

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mum junction temperature rating for the LTC1149 series to be exceeded. The LTC1149 supply current is dominated by the gate charge supply current, which is given as a function of operating frequency in the Typical Performance Characteristics. The LTC1149 series junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LT1149CS is limited to less than 11mA from a 48V supply:

$T_J = 70°C + (11mA \times 48V \times 110°C/W)$
$= 128°C$ exceeds absolute maximum

To prevent the maximum junction temperature from being exceeded, the pin 2 supply current must be checked in continuous mode when operating at the maximum V_{IN}.

Design Example

As a design example, assume V_{IN} = 24V, V_{OUT} = 5V, I_{MAX} = 2.5A, and f = 100kHz. R_{SENSE}, C_T and L can immediately be calculated:

$$R_{SENSE} = \frac{100mV}{2.5} = 0.039\Omega$$

$$C_T = \frac{7.8 \times 10^{-5}}{100kHz}\left(1 - \frac{5V}{24V}\right) = 620pF$$

$$L_{MIN} = 5.1 \times 10^5 \times 0.039\Omega \times 620pF \times 5V = 62\mu H$$

Selection of the P-channel MOSFET involves doing calculations for different sized MOSFETs to determine the relative loss contributions. Taking an International Rectifier IRF9Z34 for example, $R_{DS(ON)}$ = 0.14Ω Max, Q_P = 35nC, and C_{RSS} = 200pF ($V_{DS} = V_{IN}/2$). These values can be used to estimate the I^2R losses, transition losses, and gate charge supply current losses:

Est. I^2R Loss (T_J = 100°C) =
$(5V/24V)\ (2.5)^2\ (1 + 0.5)0.14\Omega = 270mW$

Est. Transition Loss =
$5\ (24V)^2\ (2.5A)\ (200pF)\ (100kHz) = 145mW$

Est. Gate Charge Loss =
$(100kHz)\ (35nC)\ (24V) = 85mW$

The same calculations were repeated for a smaller device, the Motorola MTD2955 ($R_{DS(ON)}$ = 0.3Ω), and a larger one, the Harris RFP30P05 ($R_{DS(ON)}$ = 0.065Ω). The results are summarized in the table.

CONDITIONS V_{IN} = 24V, V_{OUT} = 5V F = 100kHz, I_{OUT} = 2.5A	P-CHANNEL MOSFET		
	MTD2955	IRF9Z34	RFP30P05
Est. I^2R Loss (100°C)	550mW	270mW	120mW
Est. Transition Loss	110mW	145mW	290mW
Est. Gate Charge Loss	60mW	85mW	240mW
Est. Total Loss	720mW	500mW	650mW

For this set of conditions, the mid-sized P-channel MOSFET actually produces the lowest total losses at I_{MAX}. The resulting efficiency differences will be even more pronounced at lower output currents. Note that only the I^2R and transition losses are dissipated in the MOSFET; the gate charge supply current loss is dissipated by the LTC1149 series.

Selection of the N-channel MOSFET is somewhat easier; it need only be sized for the anticipated I^2R losses at 100% duty cycle (worst case assumption for short circuit.) The Siliconix Si9410, for example, has $R_{DS(ON)}$ = 0.03Ω Max and Q_N = 30nC. This will produce an I^2R loss of 250mW at 100°C and a gate charge supply current loss of 75mW. As with the P-channel device, the use of a larger MOSFET may actually result in lower mid-current efficiency

C_{IN} will require an RMS current rating of at least 1.25A at temperature, and C_{OUT} will require an ESR of 0.04Ω for optimum efficiency. The output capacitor ESR requirement can be fulfilled by a single OS-CON or by two or more surface mount tantalums in parallel.

Auxiliary Windings – Suppressing Burst Mode™ Operation

The LTC1149 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode™ operation can be suppressed at low output currents with a simple external network which cancels the

APPLICATIONS INFORMATION

25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 6. Two 100Ω resistors are inserted in series with the leads from the sense resistor.

With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the minimum threshold will be cancelled and Burst Mode™ operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 8 and 9.

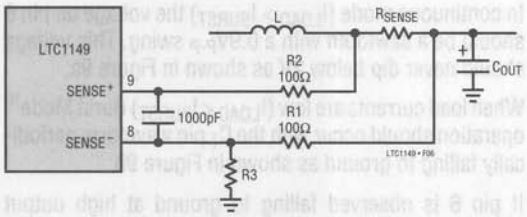


Figure 6. Suppressing Burst Mode™ Operation

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing cap pin 6 above 1.5V when the output voltage is greater than the desired regulated value, will turn on the N-channel MOSFET.

A fault condition which causes the output voltage to go above a maximum value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will then force the system fuse to blow.

The N-channel MOSFET needs to be sized so it will safely handle this over current condition. The typical delay from pulling the C_T pin 6 high to when the N-gate pin 13 goes high is 250ns. *Under shutdown conditions, the N-channel is held off and pulling pin 6 high will not cause the output to be crowbarred.*

A small N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1149 as shown in Figure 7.

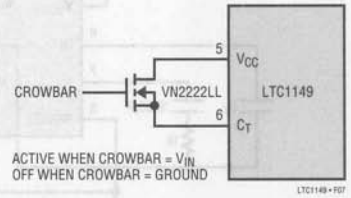


Figure 7. Output Crowbar Interface

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1149 series. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1149 signal ground pin 11 must connect separately to the (–) plate of C_{OUT}. The other ground pins 12 and 14 should return to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.

2) Does the LTC1149 Sense$^-$ pin 8 connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

3) Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between pins 8 and 9 should be as close as possible to the LTC1149. Up to 100Ω may be placed in series with each sense lead to help decouple pins 8

4

APPLICATIONS INFORMATION

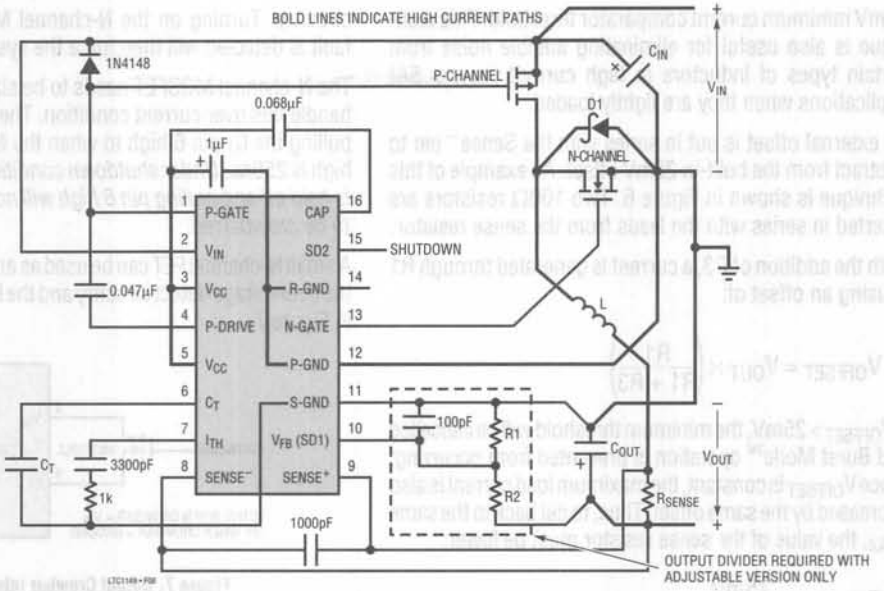


Figure 8. LTC1149 Series Layout Diagram (see Layout Checklist)

and 9. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.

5) Is the V_{CC} decoupling capacitor connected closely between pin 5 of the LTC1149 and power ground? This capacitor carries the MOSFET driver peak currents.

6) Is the shutdown 1 pin 10 (fixed output versions only) actively pulled to ground during normal operation? The shutdown 1 pin is high impedance and must not be allowed to float. In adjustable versions, pin 10 is the feedback pin and is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.

Troubleshooting Hints

Since efficiency is critical to LTC1149 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode™ operation. The waveform to monitor is the voltage on the timing capacitor pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on pin 6 should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode™ operation should occur with the C_T pin waveform periodically falling to ground as shown in Figure 9b.

If pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the **Board Layout Checklist**.

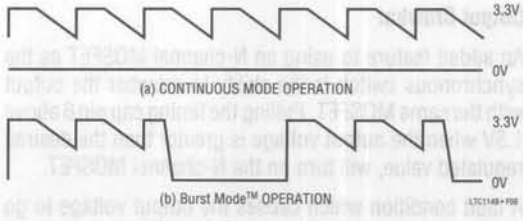


Figure 9. C_T Pin 6 Waveforms

TYPICAL APPLICATIONS

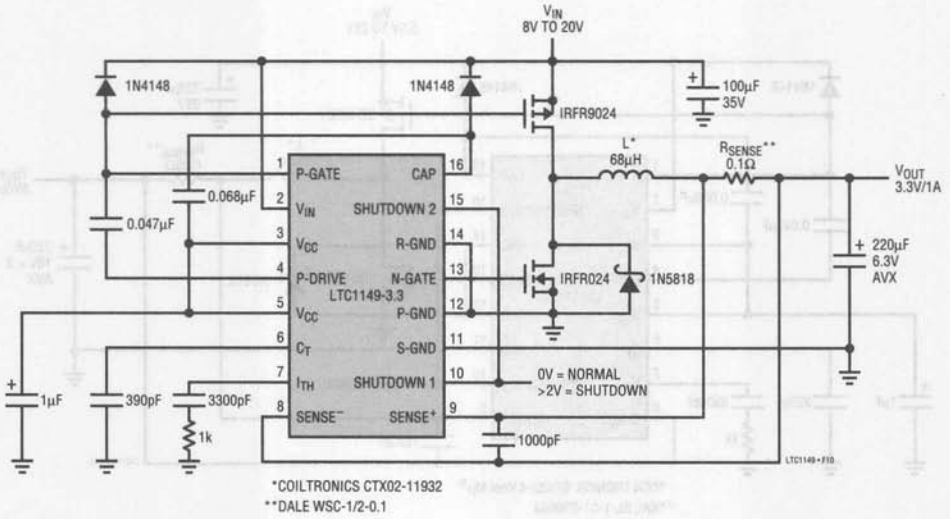


Figure 10. High Efficiency 8V to 20V Input 3.3V/1A Output Regulator

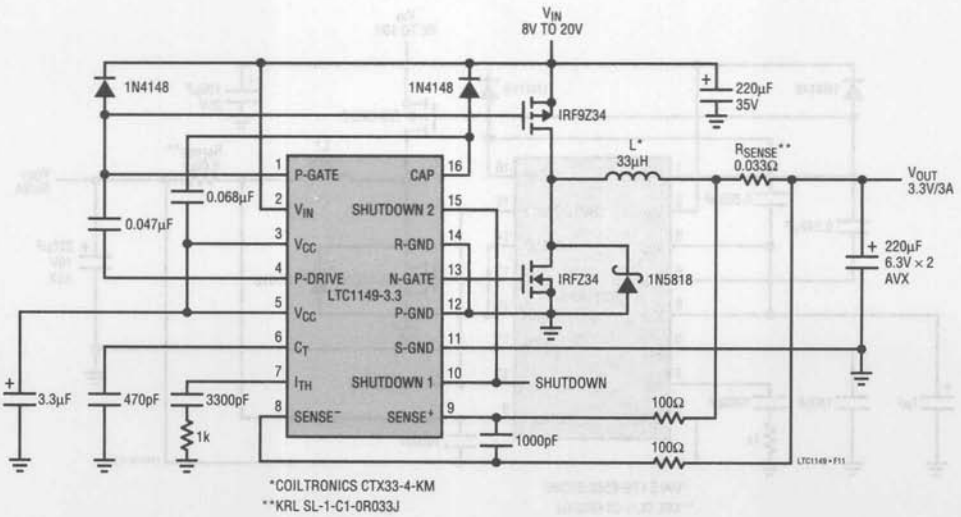


Figure 11. High Efficiency 8V to 20V Input 3.3V/3A Output Regulator

TYPICAL APPLICATIONS

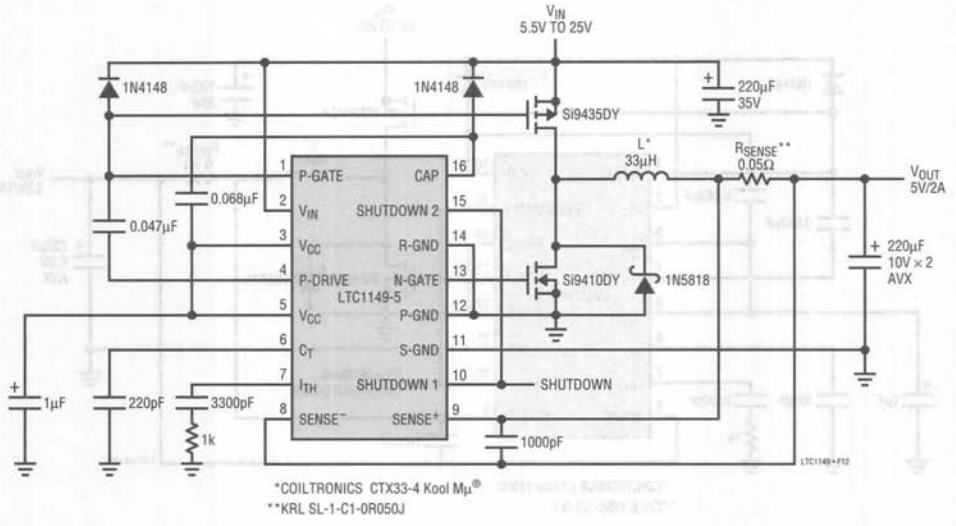


Figure 12. Ultra Wide Input Range (5.5V to 25V) High Efficiency 5V Regulator

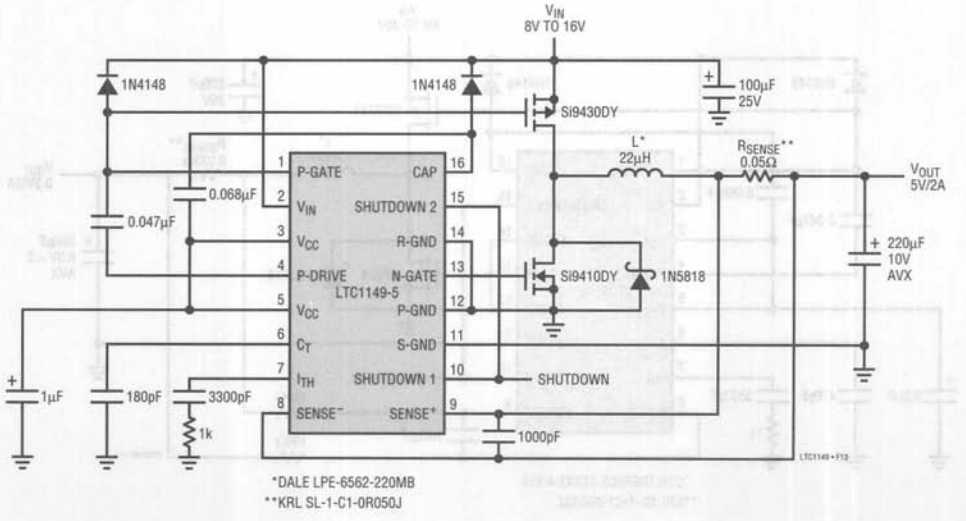


Figure 13. 250kHz High Efficiency 12V Input 5V/2A Output Regulator

TYPICAL APPLICATIONS

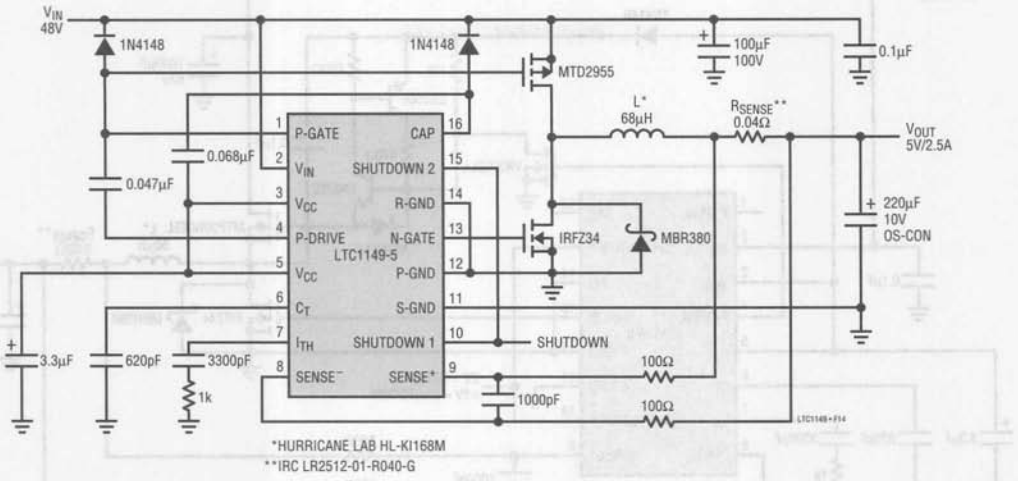


Figure 14. High Efficiency 48V Input 5V/2.5A Output Regulator

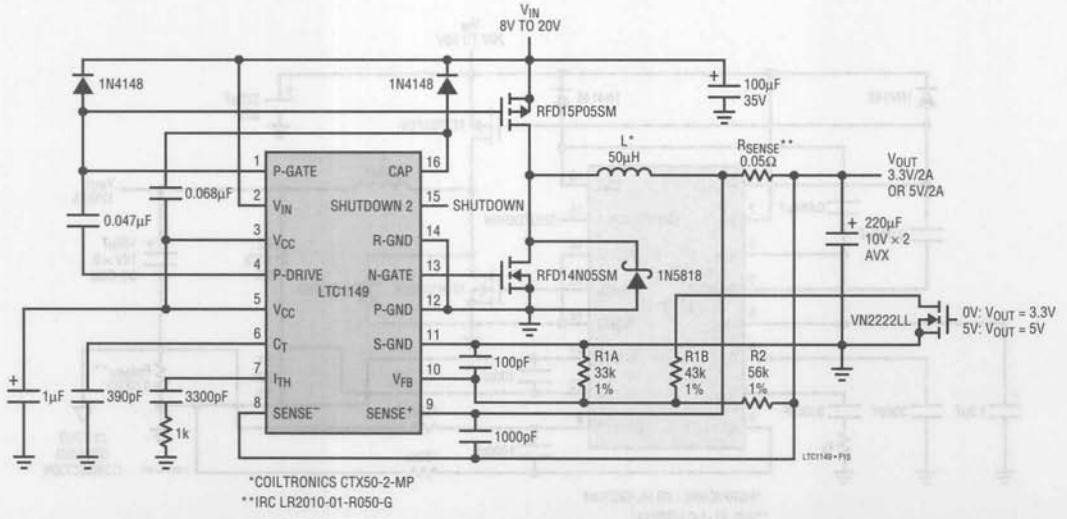


Figure 15. Logic Selectable 5V/2A or 3.3V/2A High Efficiency Regulator

TYPICAL APPLICATIONS

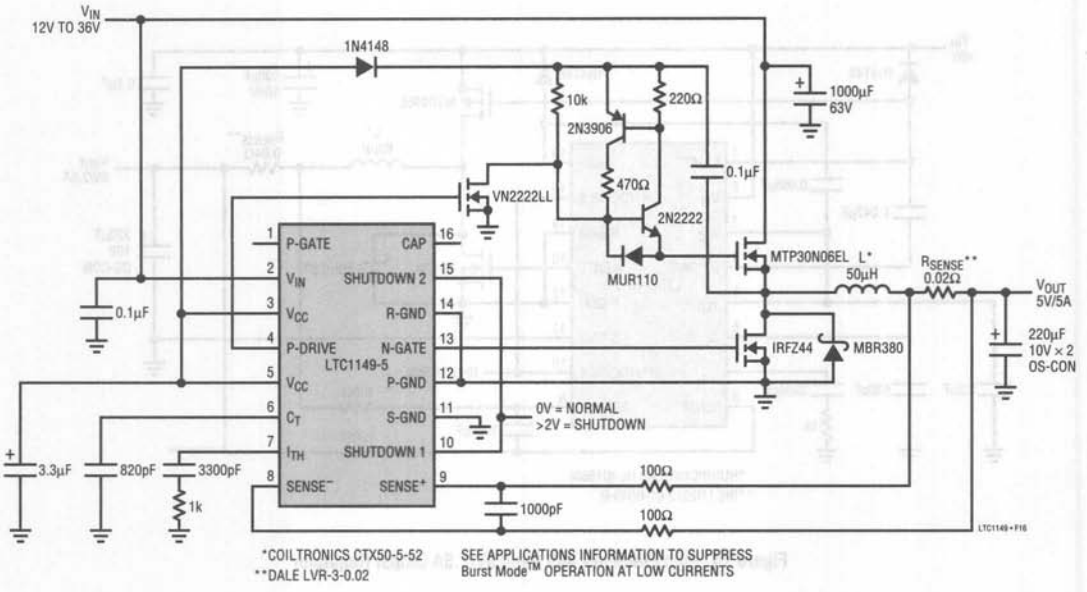


Figure 16. 25W High Efficiency Regulator Using N-Channel MOSFET Switches

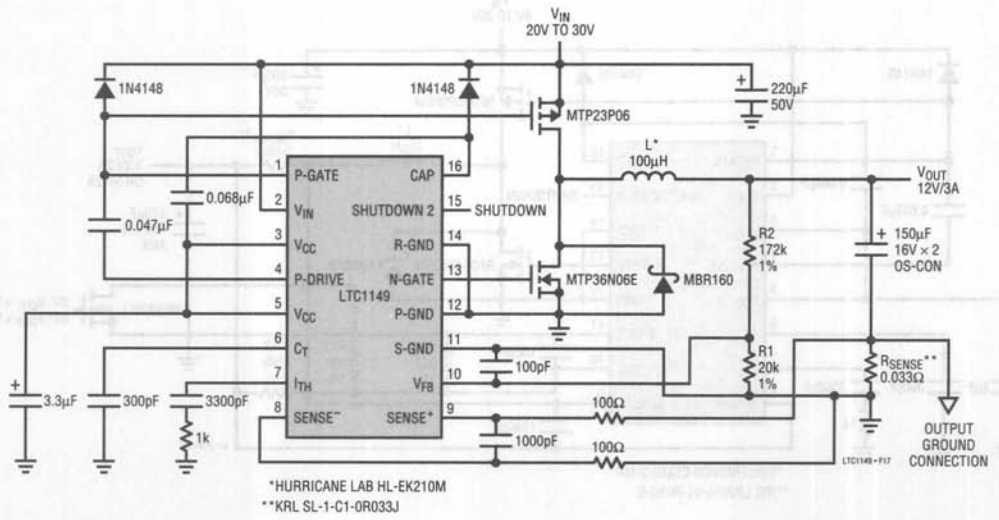


Figure 17. High Efficiency 24V Input 12V/3A Output Regulator

100kHz, 5A, 2.5A and 1.25A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range: 3V to 60V
- Low Quiescent Current: 6mA
- Internal 5A Switch (2.5A for LT1171, 1.25A forLT1172)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode Has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- LT1172 Available in 8-Pin MiniDIP and Surface Mount Packages
- Can Be Externally Synchronized

APPLICATIONS

- Logic Supply 5V at 10A
- 5V Logic to ±15V Op Amp Supply
- Battery Upconverter
- Power Inverter (+ to –) or (– to +)
- Fully Floating Multiple Outputs

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1170/LT1171/LT1172. Application circuits are included to show the capability of the LT1170/LT1171/LT1172. A complete design manual (AN19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1170/LT1171/LT1172 by factoring in the higher frequency. A CAD design program called SwitcherCAD is also available.

DESCRIPTION

The LT1170/LT1171/LT1172 are monolithic high power switching regulators. They can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk." A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1170/LT1171/LT1172 to be built in a standard 5-pin TO-3 or TO-220 power package as well as the 8-pin packages (LT1172). This makes them extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

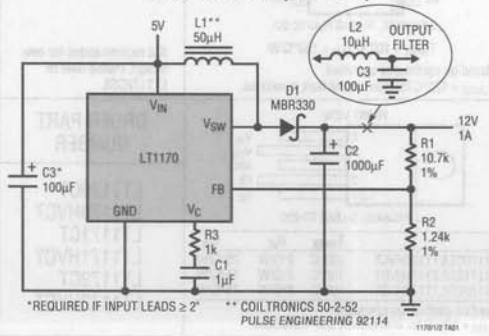
The LT1170/LT1171/LT1172 operate with supply voltages from 3V to 60V, and draw only 6mA quiescent current. They can deliver load power up to 100W with no external power devices. By utilizing current-mode switching techniques, they provide excellent AC and DC load and line regulation.

The LT1170/LT1171/LT1172 have many unique features not found even on the vastly more difficult to use low power control chips presently available. They use adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typically for standby operation.

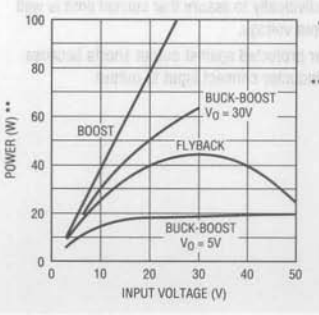
4

TYPICAL APPLICATION

Boost Converter (5V to 12V)



Maximum Output Power*



* ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 5A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.

** DIVIDE VERTICAL POWER SCALE BY TWO FOR LT1171, BY FOUR FOR LT1172.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1170/71/72HV 60V
- LT1170/71/72 (See Note 1) 40V

Switch Output Voltage
- LT1170/71/72HV 75V
- LT1170/71/72 ..... 65V
- LT1172S8 ..... 60V

Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Operating Junction Temperature Range
- LT1170/71/72M ..... −55°C to 150°C
- LT1170/71/72HVC, LT1170/71/72C (Oper.) ..... 0°C to 100°C
- LT1170/71/72HVC, LT1170/71/72C (Sh. Ckt.) ..... 0°C to 125°C
- LT1170/71/72I (Oper.) ..... −40°C to 100°C
- LT1170/71/72I (Sh. Ckt.) ..... −40°C to 125°C

Note 1: Minimum effective switch "on" time for the LT1170/71/72 (in current limit only) is ≈ 0.6µs. This limits the maximum safe input voltage during an output shorted condition. Buck mode and inverting mode input voltage during an output shorted condition is limited to:

$$V_{IN}\ (\text{max, output shorted}) = 15V + \frac{R \bullet I_L + Vf}{t \bullet f}$$

buck and inverting mode

R = Inductor DC resistance

I_L = 10A for LT1170, 5A for LT1171, and 2.5A for LT1172

Vf = Output catch diode forward voltage at I_L

t = 0.6µs, f = 100kHz switching frequency

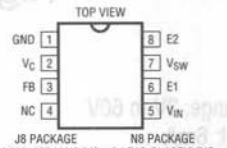
Maximum input voltage can be increased by increasing R or Vf.

External current limiting such as that shown in AN19, Figure 39, will provide protection up to the full supply voltage rating. C1 in Figure 39 should be reduced to 200pF.

Transformer designs will tolerate much higher input voltages because leakage inductance limits rate of rise of current in the switch. These designs must be evaluated individually to assure that current limit is well controlled up to maximum input voltage.

Boost mode designs are never protected against output shorts because the external catch diode and inductor connect input to output.

PACKAGE/ORDER INFORMATION



J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE, 8-LEAD PLASTIC SOIC

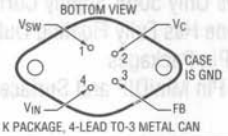
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 100°C, θ_{JA} = 120°C/W (S)

ORDER PART NUMBER

LT1172MJ8
LT1172CJ8
LT1172CN8
LT1172IN8
LT1172CS8
LT1172IS8

S8 PART MARKING

1172
1172I



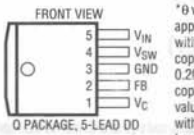
K PACKAGE, 4-LEAD TO-3 METAL CAN

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1170MK	150°C	2°C/W	35°C/W
LT1170CK	100°C	2°C/W	35°C/W
LT1171MK	150°C	4°C/W	35°C/W
LT1171CK	100°C	4°C/W	35°C/W
LT1172MK/LT1172HVMK	150°C	8°C/W	35°C/W
LT1172CK/LT1172HVCK	150°C	8°C/W	35°C/W

Based on continuous operation.
T_{JMAX} = 125°C for intermittent fault conditions.

ORDER PART NUMBER

LT1170MK
LT1170CK
LT1171MK
LT1171CK
LT1172MK
LT1172CK



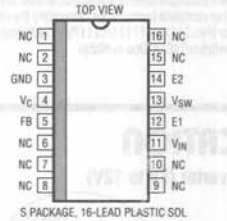
Q PACKAGE, 5-LEAD DD

T_{JMAX} = 100°C, θ_{JA} = *°C/W

*θ will vary from approximately 25°C/W with 2.8 sq. in. of 1oz. copper to 45°C/W with 0.20 sq. in. of 1oz. copper. Somewhat lower values can be obtained with additional copper layers in multilayer boards.

ORDER PART NUMBER

LT1170CQ
LT1171CQ



S PACKAGE, 16-LEAD PLASTIC SOL

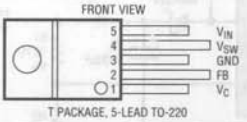
T_{JMAX} = 100°C, θ_{JA} = 150°C/W

Based on continuous operation.
T_{JMAX} = 125°C for intermittent fault conditions.

ORDER PART NUMBER

LT1172CS

Not recommended for new design. Please refer to LT1172CS8.



T PACKAGE, 5-LEAD TO-220

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1170CT/LT1170HVCT	100°C	2°C/W	75°C/W
LT1171CT/LT1171HVCT	100°C	4°C/W	75°C/W
LT1172CT/LT1172HVCT	100°C	8°C/W	75°C/W

Based on continuous operation.
T_{JMAX} = 125°C for intermittent fault conditions.

ORDER PART NUMBER

LT1170CT
LT1170HVCT
LT1171CT
LT1171HVCT
LT1172CT
LT1172HVCT

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage		Measured at Feedback Pin			1.224	1.244	1.264	V
			V_C = 0.8V		●	1.214	1.244	1.274	V
I_B	Feedback Input Current		V_{FB} = V_{REF}				350	750	nA
					●			1100	nA
g_m	Error Amplifier Transconductance		ΔI_C = ±25µA			3000	4400	6000	µmho
					●	2400		7000	µmho
	Error Amplifier Source or Sink Current		V_C = 1.5V			150	200	350	µA
					●	120		400	µA
	Error Amplifier Clamp Voltage		Hi Clamp, V_{FB} = 1V			1.80		2.30	V
			Lo Clamp, V_{FB} = 1.5V			0.25	0.38	0.52	V
	Reference Voltage Line Regulation		3V ≤ V_{IN} ≤ V_{MAX}		●			0.03	%/V
			V_C = 0.8V						
A_V	Error Amplifier Voltage Gain		0.9V ≤ V_C ≤ 1.4V			500	800		V/V
	Minimum Input Voltage (Note 3)				●		2.6	3.0	V
I_Q	Supply Current		3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V				6	9	mA
	Control Pin Threshold		Duty Cycle = 0			0.8	0.9	1.08	V
					●	0.6		1.25	V
	Normal/Flyback Threshold on Feedback Pin					0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage (Note 3)		I_{FB} = 50µA			15.0	16.3	17.6	V
					●	14.0		18.0	V
	Change in Flyback Reference Voltage		0.05 ≤ I_{FB} ≤ 1mA			4.5	6.8	9	V
	Flyback Reference Voltage Line Regulation (Note 3)		I_{FB} = 50µA				0.01	0.03	%/V
			7V ≤ V_{IN} ≤ V_{MAX}						
	Flyback Amplifier Transconductance (g_m)		ΔI_C = ±10µA			150	300	500	µmho
	Flyback Amplifier Source and Sink Current		V_C = 0.6V	Source	●	15	32	70	µA
			I_{FB} = 50µA	Sink	●	25	40	70	µA
BV	Output Switch Breakdown Voltage		3V ≤ V_{IN} ≤ V_{MAX},	LT1170/LT1171/LT1172	●	65	90		V
			I_{SW} = 1.5mA	LT1170HV/LT1171HV/LT1172HV	●	75	90		V
				LT1172S8	●	60	80		V
V_{SAT}	Output Switch "On" Resistance (Note 1)		LT1170		●		0.15	0.24	Ω
			LT1171		●		0.30	0.50	Ω
			LT1172		●		0.60	1.00	Ω
	Control Voltage to Switch Current Transconductance		LT1170				8		A/V
			LT1171				4		A/V
			LT1172				2		A/V
I_{LIM}	Switch Current Limit	(LT1170)	Duty Cycle = 50%	T_J ≥ 25°C	●	5		10	A
			Duty Cycle = 50%	T_J < 25°C	●	5		11	A
			Duty Cycle = 80% (Note 2)		●	4		10	A
		(LT1171)	Duty Cycle = 50%	T_J ≥ 25°C	●	2.5		5.0	A
			Duty Cycle = 50%	T_J < 25°C	●	2.5		5.5	A
			Duty Cycle = 80% (Note 2)		●	2.0		5.0	A
		(LT1172)	Duty Cycle = 50%	T_J ≥ 25°C	●	1.25		3.0	A
			Duty Cycle = 50%	T_J < 25°C	●	1.25		3.5	A
			Duty Cycle = 80% (Note 2)		●	1.00		2.5	A

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ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency			88	100	112	kHz
			●	85		115	kHz
DC_{MAX}	Maximum Switch Duty Cycle		●	80	90	95	%
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$ V_C = 0.05V			100	250	µA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$		100	150	250	mV
			●	50		300	mV
	Flyback Sense Delay Time (Note 3)				1.5		µs

The ● denotes the specifications which apply over the full operating temperature range.

V_{MAX} = 40V for LT1170/71/72 and 60V for LT1170/71/72HV.

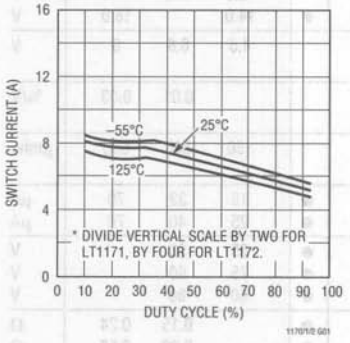
Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V. I_{SW} = 4A for LT1170, 2A for LT1171, and 1A for LT1172.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 3.33 (2 – DC) for the LT1170, I_{LIM} = 1.67 (2 – DC) for the LT1171, and I_{LIM} = 0.833 (2 – DC) for the LT1172.

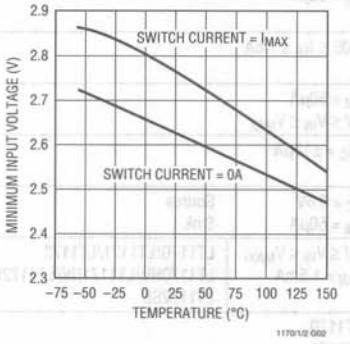
Note 3: Minimum input voltage for isolated flyback mode is 7V. V_{MAX} = 55V for HV grade in fully isolated mode to avoid switch breakdown.

TYPICAL PERFORMANCE CHARACTERISTICS

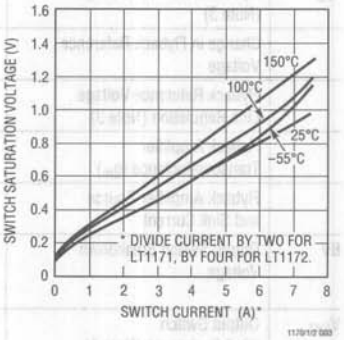
Switch Current Limit vs Duty Cycle*



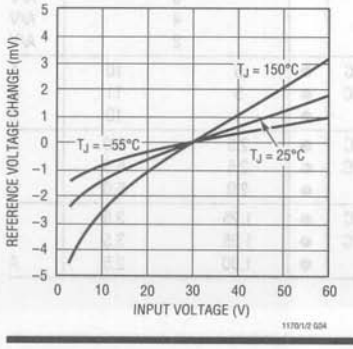
Minimum Input Voltage



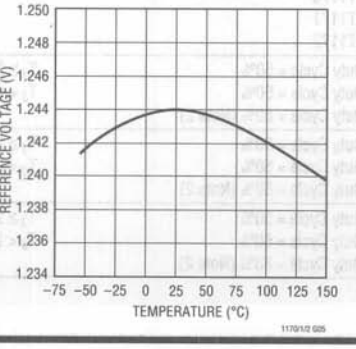
Switch Saturation Voltage



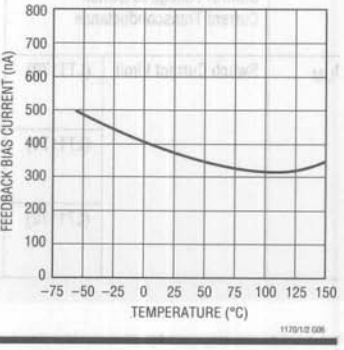
Line Regulation



Reference Voltage vs Temperature

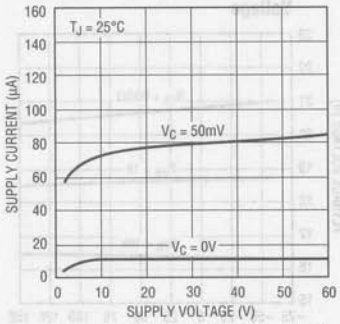


Feedback Bias Current vs Temperature

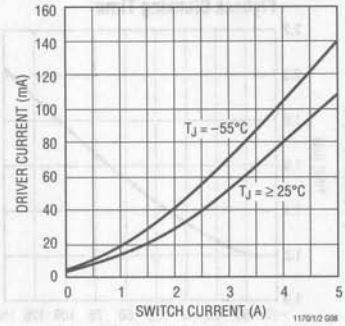


TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage (Shutdown Mode)

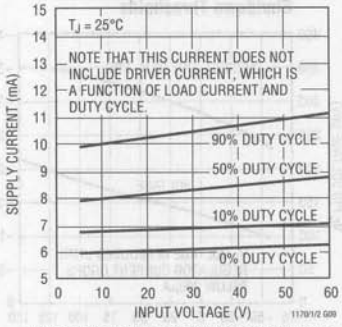


Driver Current* vs Switch Current



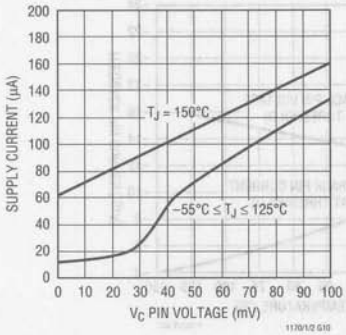
* AVERAGE LT1170 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*

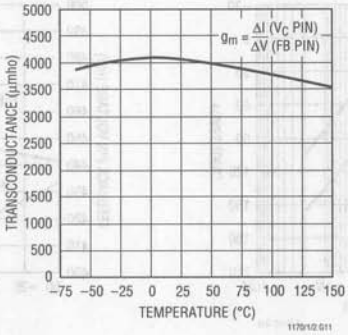


* UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

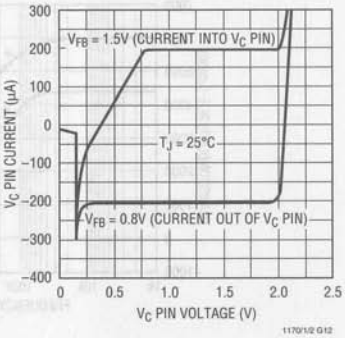
Shutdown Mode Supply Current



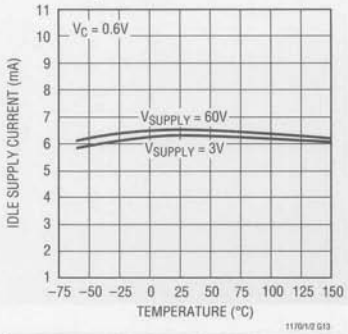
Error Amplifier Transconductance



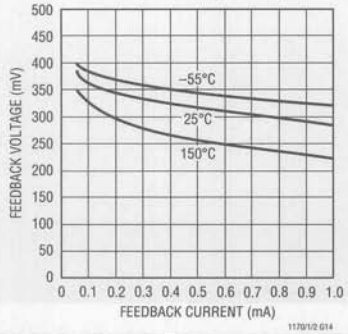
V_C Pin Characteristics



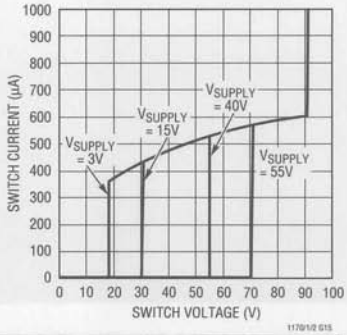
Idle Supply Current vs Temperature



Feedback Pin Clamp Voltage



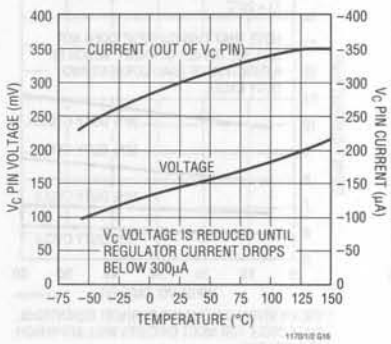
Switch "Off" Characteristics



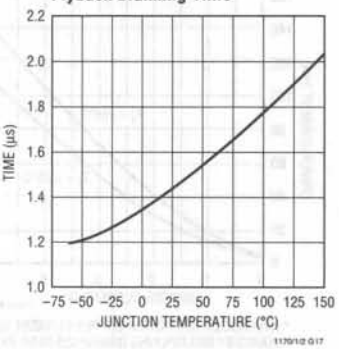
4

TYPICAL PERFORMANCE CHARACTERISTICS

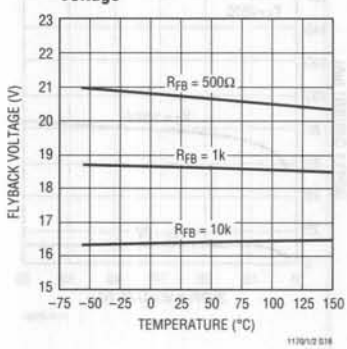
Shutdown Thresholds



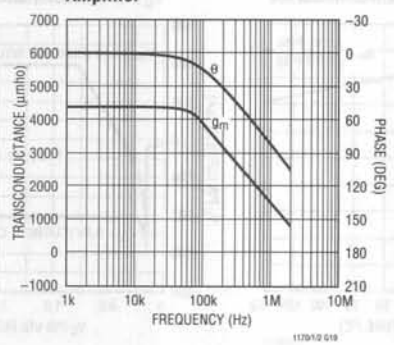
Flyback Blanking Time



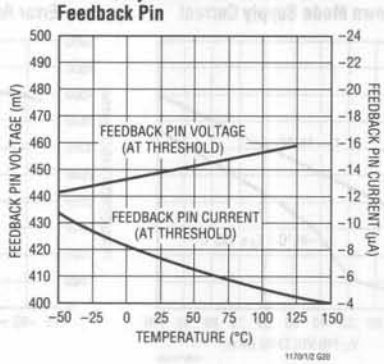
Isolated Mode Flyback Reference Voltage



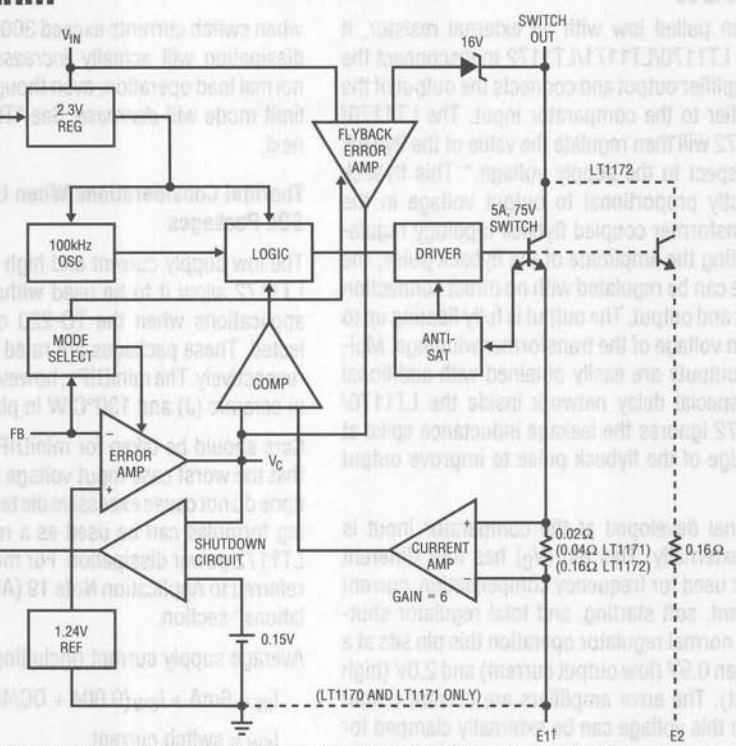
Transconductance of Error Amplifier



Normal/Flyback Mode Threshold on Feedback Pin



BLOCK DIAGRAM



†ALWAYS CONNECT E1 TO THE GROUND PIN ON MINIDIP, 8- AND 16-PIN SURFACE MOUNT PACKAGES.
E1 AND E2 INTERNALLY TIED TO GROUND ON TO-3 AND TO-220 PACKAGES.

1170/1/2 BD

OPERATION

The LT1170/LT1171/LT1172 are current mode switchers. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1170/LT1171/LT1172. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 100kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second

OPERATION

function; when pulled low with an external resistor, it programs the LT1170/LT1171/LT1172 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1170/LT1171/LT1172 will then regulate the value of the flyback pulse with respect to the supply voltage.* This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1170/LT1171/LT1172 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1170/LT1171/LT1172 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing. See AN19 for full application details.

Extra Pins on the MiniDIP and Surface Mount Packages

The 8- and 16-pin versions of the LT1172 have the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 300mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*. See "Thermal Considerations" next.

*See note under block diagram.

Thermal Considerations When Using the MiniDIP and SOL Packages

The low supply current and high switch efficiency of the LT1172 allow it to be used without a heat sink in most applications when the TO-220 or TO-3 package is selected. These packages are rated at 50°C/W and 35°C/W respectively. The miniDIPs, however, are rated at 100°C/W in ceramic (J) and 130°C/W in plastic (N).

Care should be taken for miniDIP applications to ensure that the worst case input voltage and load current conditions do not cause excessive die temperatures. The following formulas can be used as a rough guide to calculate LT1172 power dissipation. For more details, the reader is referred to Application Note 19 (AN19), "Efficiency Calculations" section.

Average supply current (including driver current) is:

$$I_{IN} \approx 6mA + I_{SW}(0.004 + DC/40)$$

I_{SW} = switch current
DC = switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2 \bullet R_{SW} \bullet DC$$

R_{SW} = LT1172 switch "on" resistance (1Ω maximum)

Total power dissipation is the sum of supply current times input voltage plus switch power:

$$P_{D(TOT)} = (I_{IN})(V_{IN}) + P_{SW}$$

In a typical example, using a boost converter to generate 12V at 0.12A from a 5V input, duty cycle is approximately 60%, and switch current is about 0.65A, yielding:

$$I_{IN} = 6mA + 0.65(0.004 + DC/40) = 18mA$$

$$P_{SW} = (0.65)^2 \bullet 1\Omega \bullet (0.6) = 0.25W$$

$$P_{D(TOT)} = (5V)(0.018A) + 0.25 = 0.34W$$

OPERATION

Temperature rise in a plastic miniDIP would be 130°C/W times 0.34W, or approximately 44°C. The maximum ambient temperature would be limited to 100°C (commercial temperature limit) minus 44°C, or 56°C.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, four approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1172 will protect the die in most applications by shutting off switch current. *Thermal limit is not a tested parameter*, however, and should be considered only for noncritical applications with temporary overloads. A second approach is to use the larger TO-220 (T) or TO-3 (K) package which, even without a heat sink, may limit die temperatures to safe levels under overload conditions. In critical situations, heat sinking of these packages is required; especially if overload conditions must be tolerated for extended periods of time.

The third approach for lower current applications is to leave the second switch emitter (miniDIP only) open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The fourth approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1172 switch current limit is zero at approximately 1V on the V_C pin and 2A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN19 for details.

LT1170/LT1171/LT1172 Synchronizing

The LT1170/LT1171/LT1172 can be externally synchronized in the frequency range of 120kHz to 160kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under 0.3µs. C2 sets the pulse width at ≅ 0.2µs. The effect of a synchronizing pulse on the LT1170/LT1171/LT1172 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right)(t_S)(f_S)\left(I_C + \frac{V_C}{R3}\right)}{I_C}$$

$\frac{KT}{q}$ = 26mV at 25°C

t_S = pulse width

f_S = pulse frequency

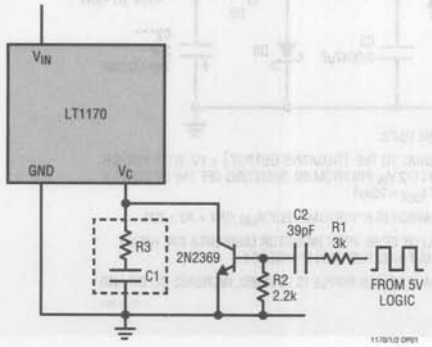
I_C = V_C source current (≈200µA)

V_C = operating V_C voltage (1V to 2V)

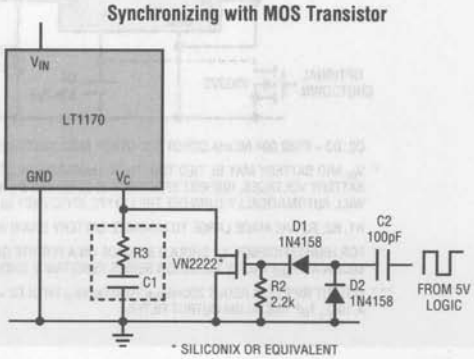
R3 = resistor used to set mid-frequency "zero" in frequency compensation network.

With t_S = 0.2µs, f_S = 150kHz, V_C = 1.5V, and R3 = 2k, offset voltage shift is ≈3.8mV. This is not particularly bothersome, but note that high offsets could result if R3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R3, so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor



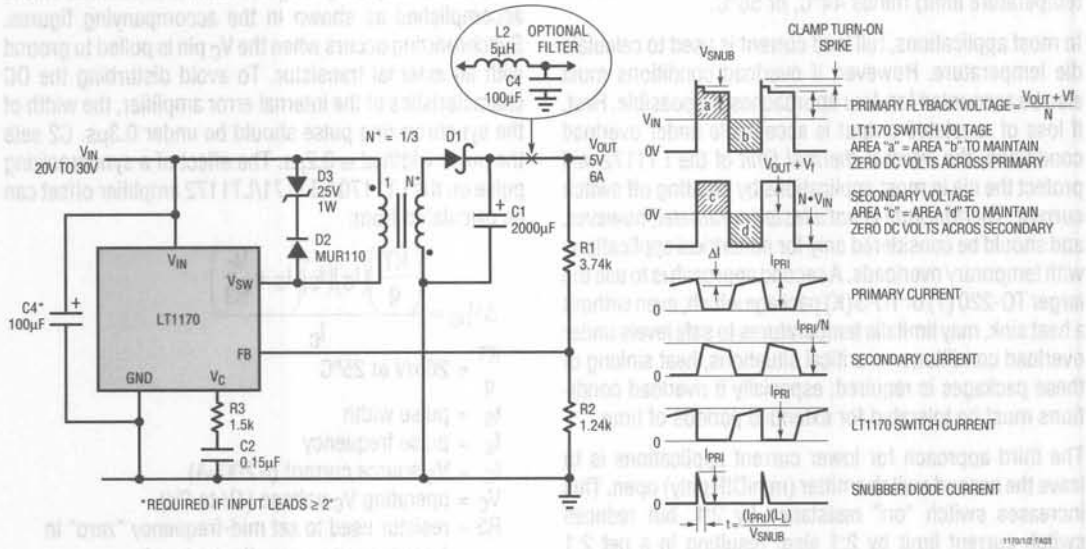
Synchronizing with MOS Transistor



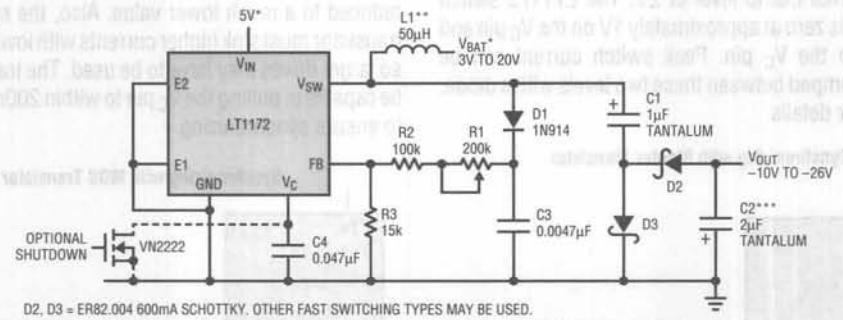
* SILICONIX OR EQUIVALENT

TYPICAL APPLICATIONS

Flyback Converter



LCD Contrast Supply



D2, D3 = ER82.004 600mA SCHOTTKY. OTHER FAST SWITCHING TYPES MAY BE USED.

* V_{IN} AND BATTERY MAY BE TIED TOGETHER. MAXIMUM VALUE FOR V_{BAT} IS EQUAL TO THE |NEGATIVE OUTPUT| + 1V. WITH HIGHER BATTERY VOLTAGES, HIGHEST EFFICIENCY IS OBTAINED BY RUNNING THE LT1172 V_{IN} PIN FROM 5V. SHUTTING OFF THE 5V SUPPLY WILL AUTOMATICALLY TURN OFF THE LT1172. EFFICIENCY IS ABOUT 80% AT I_{OUT} = 25mA.

R1, R2, R3 ARE MADE LARGE TO MINIMIZE BATTERY DRAIN IN SHUTDOWN, WHICH IS APPROXIMATELY V_{BAT} /(R1 + R2 + R3).

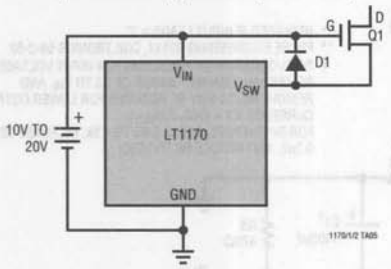
** FOR HIGH EFFICIENCY, L1 SHOULD BE MADE ON A FERRITE OR MOLYPERMALLOY CORE. PEAK INDUCTOR CURRENTS ARE ABOUT 600mA AT P_{OUT} = 0.7Ω. INDUCTOR SERIES RESISTANCE SHOULD BE LESS THAN 0.4Ω FOR HIGH EFFICIENCY.

*** OUTPUT RIPPLE IS ABOUT 200mV$_{P-P}$ TO 400mV$_{P-P}$ WITH C2 = 2μF TANTALUM. IF LOWER RIPPLE IS DESIRED, INCREASE C2, OR ADD A 10Ω , 1μF TANTALUM OUTPUT FILTER.

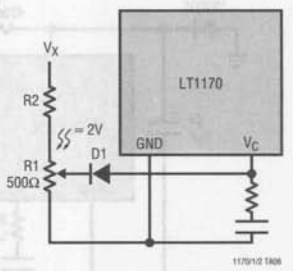
1170/1/2 TA04

TYPICAL APPLICATIONS (Note that maximum output currents are divided by 2 for LT1171, by 4 for LT1172.)

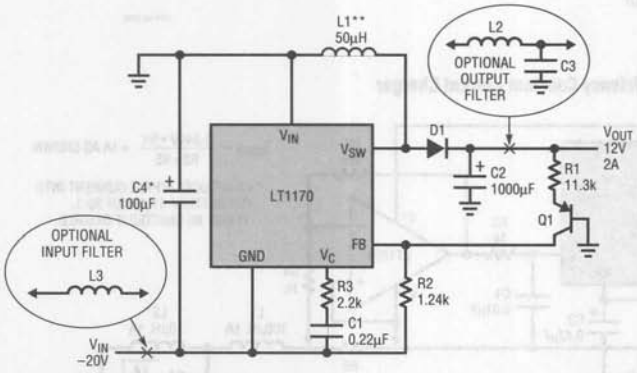
Driving High Voltage FET (for Off-Line Applications, See AN25)



External Current Limit



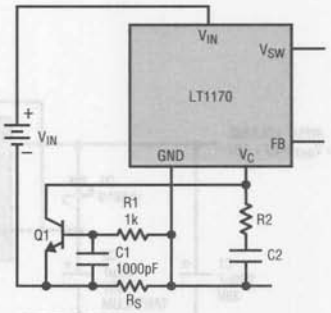
Negative-to-Positive Buck-Boost Converter†



* REQUIRED IF INPUT LEADS ≥ 2"
** PULSE ENGINEERING 92114, COILTRONICS 50-2-52
† THIS CIRCUIT IS OFTEN USED TO CONVERT –48V TO 5V. TO GUARANTEE FULL SHORT-CIRCUIT PROTECTION, THE CURRENT LIMIT CIRCUIT SHOWN IN AN19, FIGURE 39, SHOULD BE ADDED WITH C1 REDUCED TO 200pF.

1170/1/2 TA07

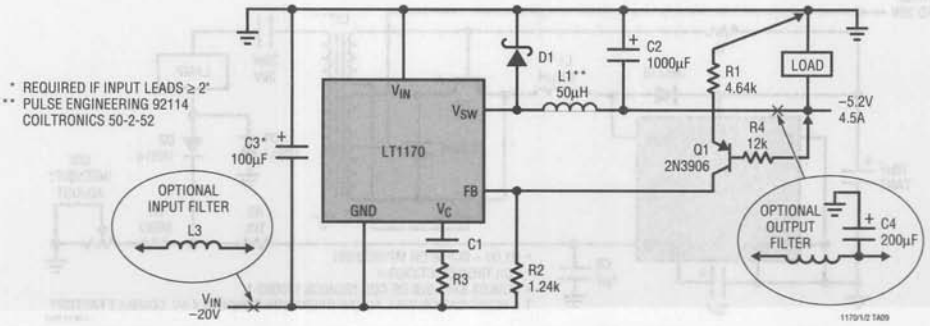
External Current Limit



NOTE THAT THE LT1170 GND PIN IS NO LONGER COMMON TO V_{IN}^-.

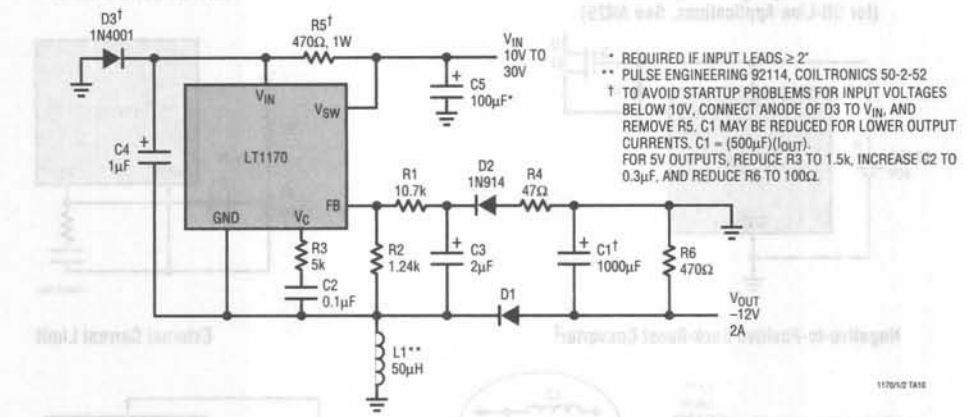
1170/1/2 TA08

Negative Buck Converter

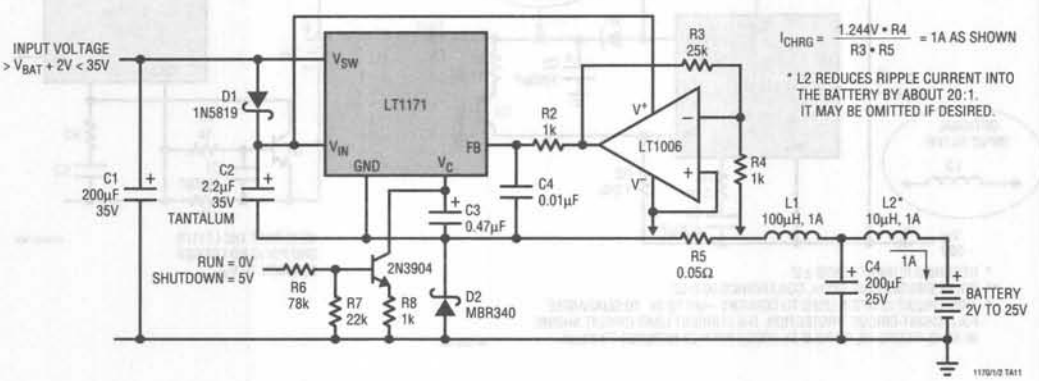


TYPICAL APPLICATIONS

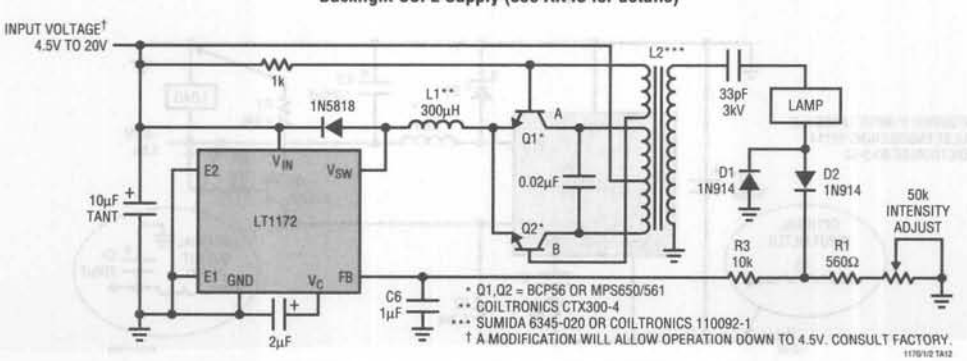
Positive-to-Negative Buck-Boost Converter



High Efficiency Constant Current Charger

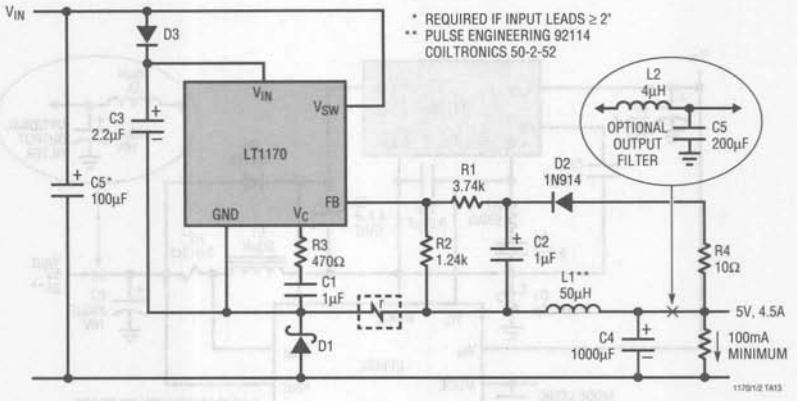


Backlight CCFL Supply (see AN45 for details)

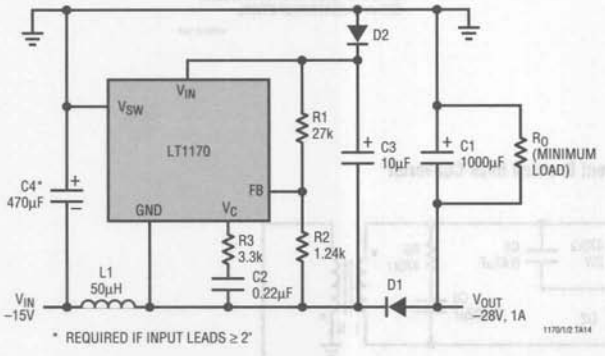


TYPICAL APPLICATIONS

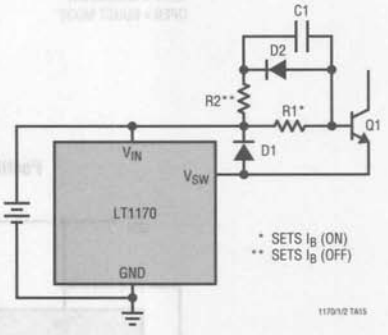
Positive Buck Converter



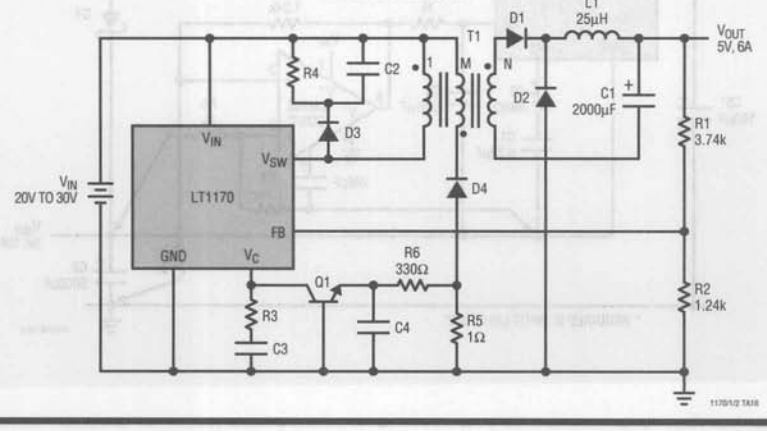
Negative Boost Regulator



Driving High Voltage NPN

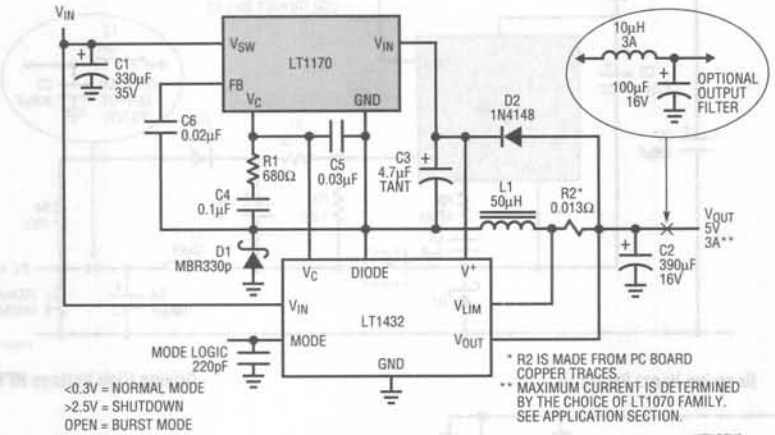


Forward Converter

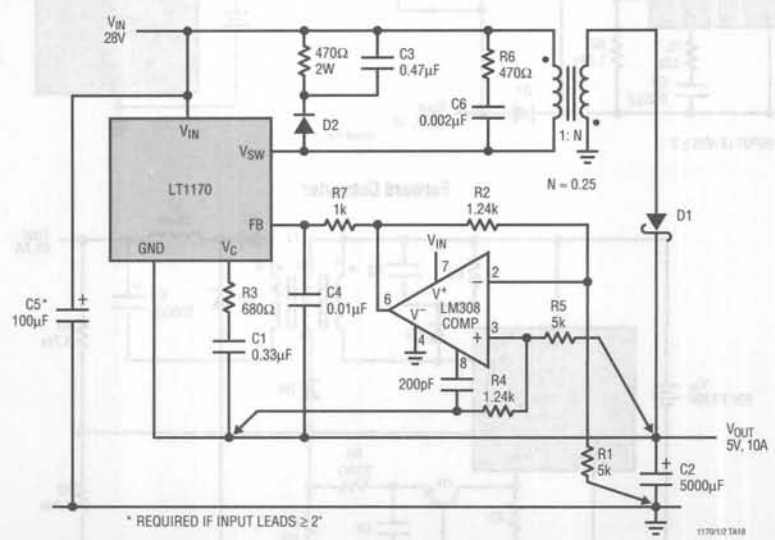


TYPICAL APPLICATIONS

High Efficiency 5V Buck Converter



Positive Current Boosted Buck Converter



High Efficiency Step-Down and Inverting DC/DC Converter

FEATURES

- **High Efficiency: Up to 94%**
- Usable in Noise-Sensitive Products*
- Short-Circuit Protection
- Optimized for 5V to –5V Applications
- Wide V_{IN} Range: 4V to 18.5V
- Low Dropout Operation
- Low-Battery Detector
- Pin Selectable Current Limit
- Internal 0.9Ω Power Switch: V_{IN} = 9V
- Only Four External Components Required
- 130μA Standby Current
- Active Low Micropower Shutdown

APPLICATIONS

- Cellular Phones
- Step-Down Converters
- Inverting Converters
- Memory Backup Supply
- Portable Instruments
- Battery-Powered Equipment

DESCRIPTION

The LTC1174 is a simple current mode DC/DC converter ideally suited for 9V to 5V, 5V to 3.3V, or 5V to –5V operation. With an internal 0.9Ω switch (at a supply voltage of 9V), the LTC1174 requires only four external components to construct a complete high efficiency DC/DC converter.

Under a no load condition the LT1174 draws only 130μA. In shutdown, it draws a mere 1μA making this converter ideal for current sensitive applications. In dropout, the internal P-channel MOSFET switch is turned on continuously allowing the user to maximize the life of the battery source.

The maximum inductor current of the LTC1174 family is pin selectable to either 340mA or 600mA, optimizing efficiency for a wide range of applications. Operation up to 200kHz permits the use of small surface mount inductors and capacitors.

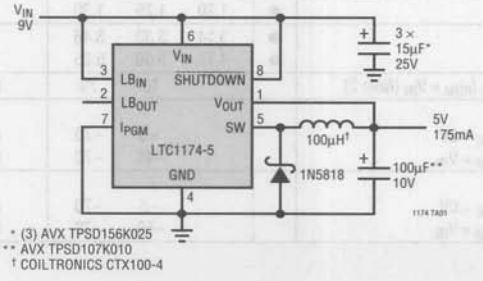
For applications requiring higher output current or ultra-high efficiency, see the LTC1148 data sheet.

* Consult factory Applications Engineering for techniques to manage the output spectrum.

4

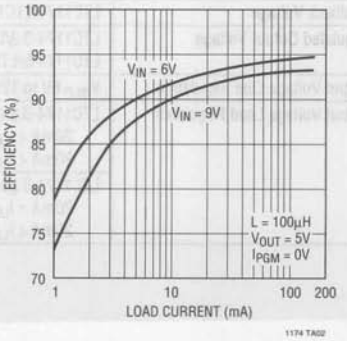
TYPICAL APPLICATION

High Efficiency Step-Down Converter



* (3) AVX TPSD156K025
** AVX TPSD107K010
† COILTRONICS CTX100-4

LTC1174-5 Efficiency

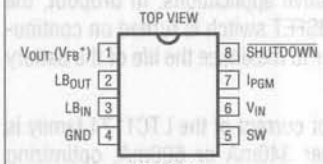


ABSOLUTE MAXIMUM RATINGS

(Voltage Referred to GND Pin)
Input Supply Voltage (Pin 6)
LTC1174 ..... −0.3V to 13.5V
LTC1174HV ..... −0.3V to 18.5V
Switch Current (Pin 5) 1A
Switch Voltage (Pin 5)
LTC1174 ..... V_{IN} − 13.5V
LTC1174HV ..... V_{IN} − 18.5V

Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... −40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

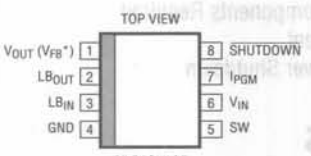


N8 PACKAGE
8-LEAD PLASTIC DIP

* ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1174CN8
LTC1174CN8-3.3
LTC1174CN8-5
LTC1174HVCN8
LTC1174HVCN8-3.3
LTC1174HVCN8-5
LTC1174IN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

* ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1174CS8
LTC1174CS8-3.3
LTC1174CS8-5
LTC1174IS8
LTC1174HVCS8
LTC1174HVCS8-3.3
LTC1174HVCS8-5

S8 PART MARKING	
1174	1174HV
117433	1174H3
117450	1174H5
1174I	

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 9V, $V_{\overline{SHUTDOWN}}$ = V_{IN}, I_{PGM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	Feedback Current	LTC1174/LTC1174HV				1	µA
V_{FB}	Feedback Voltage	LTC1174/LTC1174HV	●	1.20	1.25	1.30	V
V_{OUT}	Regulated Output Voltage	LTC1174-3.3/LTC1174HV-3.3	●	3.14	3.30	3.46	V
		LTC1174-5/LTC1174HV-5	●	4.75	5.00	5.25	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 6V to 12V, I_{LOAD} = 100mA, I_{PGM} = V_{IN} (Note 2)			10	70	mV
	Output Voltage Load Regulation	LTC1174-3.3 (Note 2)					
		20mA < I_{LOAD} < 175mA, I_{PGM} = 0V			−5	−70	mV
		20mA < I_{LOAD} < 400mA, I_{PGM} = V_{IN}			−45	−70	mV
		LTC1174-5 (Note 2)					
		20mA < I_{LOAD} < 175mA, I_{PGM} = 0V			−5	−70	mV
		20mA < I_{LOAD} < 400mA, I_{PGM} = V_{IN}			−50	−70	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 9V, $V_{\overline{SHUTDOWN}}$ = V_{IN}, I_{PGM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Input DC Supply Current (Note 3)	Active Mode					
		LTC1174: 4V < V_{IN} < 12V, I_{PGM} = 0V			450	600	µA
		LTC1174HV: 4V < V_{IN} < 16V, I_{PGM} = 0V			450	600	µA
		Sleep Mode					
		LTC1174: 4V < V_{IN} < 12V			130	180	µA
		LTC1174HV: 4V < V_{IN} < 16V			130	180	µA
		$\overline{SHUTDOWN}$ (Note 4)					
		LTC1174: $V_{\overline{SHUTDOWN}}$ = 0V, 4V < V_{IN} < 12V			1	10	µA
		LTC1174HV: $V_{\overline{SHUTDOWN}}$ = 0V, 4V < V_{IN} < 16V			2	25	µA
V_{LBTRIP}	Low-Battery Trip Point				1.25	1.4	V
I_{LBIN}	Current into Pin 3					0.5	µA
I_{LBOUT}	Current Sunk by Pin 2	LTC1174: V_{LBOUT} = 0.4V		1.0	1.2	1.5	mA
		LTC1174HV: V_{LBOUT} = 0.4V		0.6	0.8	1.5	mA
V_{HYST}	Comparator Hysteresis	LTC1174/LTC1174HV		7.5	15	30	mV
I_{PEAK}	Current Limit	I_{PGM} = V_{IN}, V_{OUT} = 0V	●	0.54	0.60	0.78	A
		I_{PGM} = 0V, V_{OUT} = 0V	●	0.27	0.34	0.50	A
R_{ON}	ON Resistance of Switch	LTC1174	●		0.75	1.30	Ω
		LTC1174HV	●		0.90	1.55	Ω
t_{OFF}	Switch Off-Time (Note 5)	V_{OUT} at Regulated Value		3	4	5	µs
V_{IH}	$\overline{SHUTDOWN}$ Pin High	Minimum Voltage at Pin 8 for Device to Be Active		1.2			V
V_{IL}	$\overline{SHUTDOWN}$ Pin Low	Maximum Voltage at Pin 8 for Device to Be in Shutdown				0.75	V
I_{IH}	$\overline{SHUTDOWN}$ Pin Input Current	LTC1174: $V_{\overline{SHUTDOWN}}$ = 12V				0.5	µA
		LTC1174HV: $V_{\overline{SHUTDOWN}}$ = 16V				2.0	
I_{IL}	$\overline{SHUTDOWN}$ Pin Input Current	0 ≤ $V_{\overline{SHUTDOWN}}$ ≤ 0.8V				0.5	µA

–40°C ≤ T_A ≤ 85°C (Note 6), for LTC1174I only.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage	LTC1174I		1.18	1.25	1.31	V
I_{LBOUT}	Current Sunk by Pin 2	V_{LBOUT} = 0.4		0.75	1.2	2	mA
I_{PEAK}	Current Limit	I_{PGM} = V_{IN}, V_{OUT} = 0V		0.54	0.60	0.78	A
		I_{PGM} = 0V, V_{OUT} = 0V			0.34		A
t_{OFF}	Switch Off-Time (Note 5)	V_{OUT} at Regulated Value		2	4	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1174CN8, LTC1174CN8-3.3, LTC1174CN8-5:
$T_J = T_A + (P_D \times 110°C/W)$

LTC1174CS8, LTC1174CS8-3.3, LTC1174CS8-5:
$T_J = T_A + (P_D \times 150°C/W)$

Note 2: Guaranteed by design.

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 4: Current into pin 6 only, measured without electrolytic input capacitor.

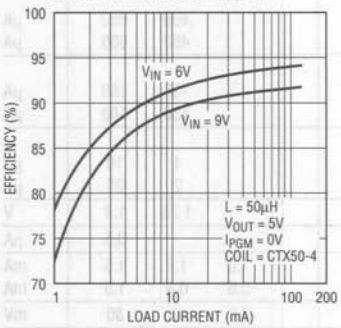
Note 5: The off-time is wafer-sort trimmed.

Note 6: The LTC1174I is not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

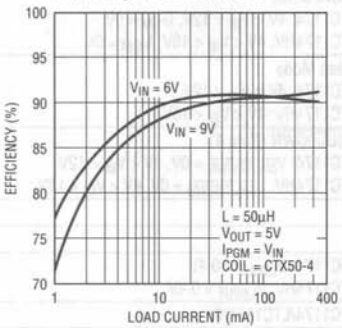
4

TYPICAL PERFORMANCE CHARACTERISTICS

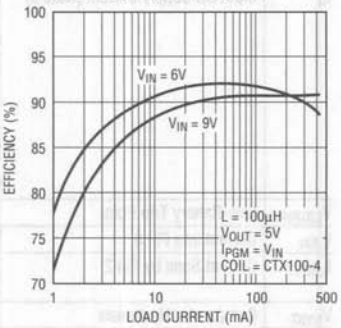
Efficiency vs Load Current



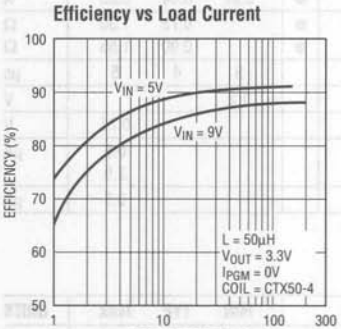
Efficiency vs Load Current



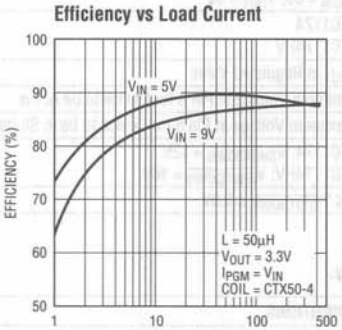
Efficiency vs Load Current



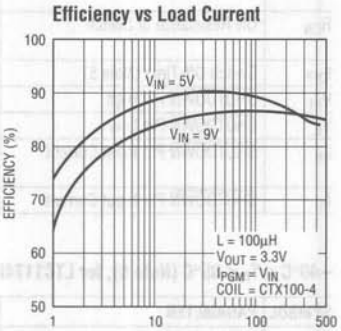
Efficiency vs Load Current



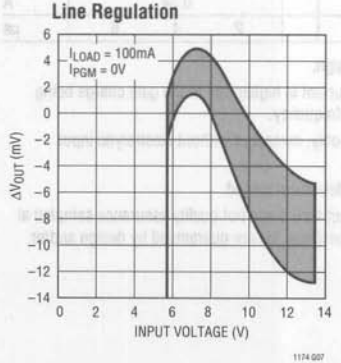
Efficiency vs Load Current



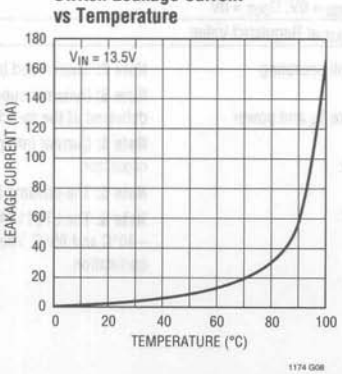
Efficiency vs Load Current



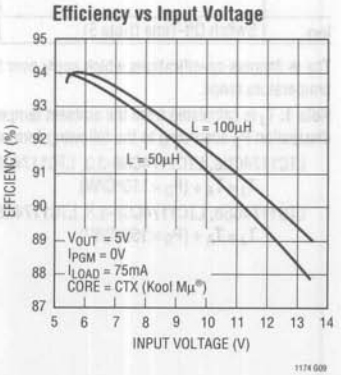
Line Regulation



Switch Leakage Current vs Temperature



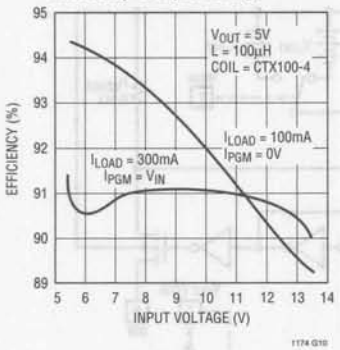
Efficiency vs Input Voltage



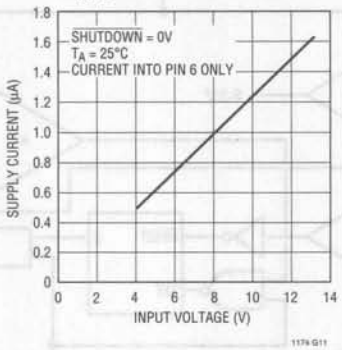
Kool Mµ® is a registered trademark of Magnetics, Inc.

TYPICAL PERFORMANCE CHARACTERISTICS

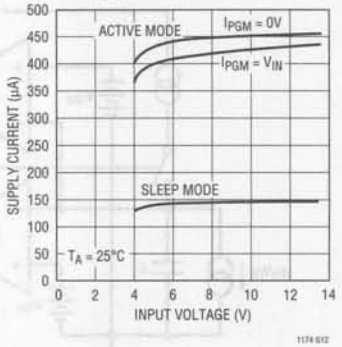
Efficiency vs Input Voltage



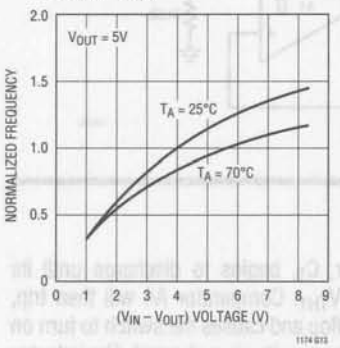
Supply Current in Shutdown



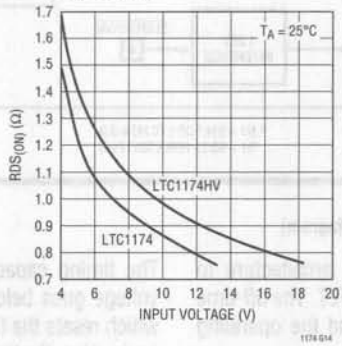
DC Supply Current



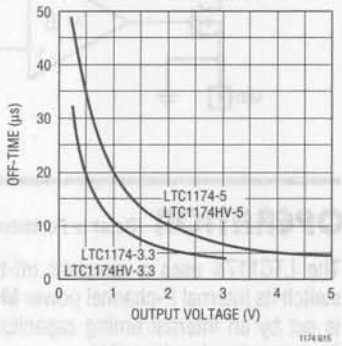
Operating Frequency vs $V_{IN} - V_{OUT}$



Switch Resistance vs Input Voltage



Off-Time vs Output Voltage



4

PIN FUNCTIONS

V_{OUT} (V_{FB}) (Pin 1): For the LTC1174, this pin connects to the main voltage comparator's input. On the LTC1174-3.3 and LTC1174-5 this pin goes to an internal resistive divider which sets the output voltage.

LB_{OUT} (Pin 2): Open Drain of an N-Channel Pull-Down. This pin will sink current when pin 3 (LB_{IN}) goes below 1.25V. During shutdown this pin goes to high impedance.

LB_{IN} (Pin 3): The "–" Input of the Low-Battery Voltage Comparator. The "+" input is connected to a reference voltage of 1.25V.

GND (Pin 4): Ground Pin.

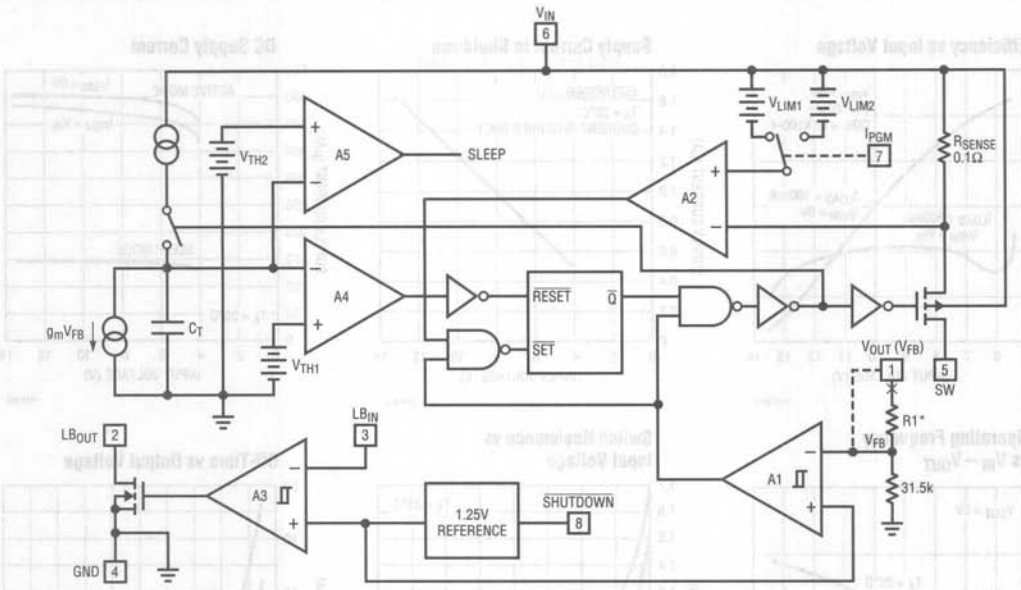
SW(Pin5): Drain of the P-Channel MOSFET Switch. Cathode of Schottky diode must be closely connected to this pin.

V_{IN} (Pin 6): Input Supply Voltage. It must be decoupled close to ground pin 4.

I_{PGM} (Pin 7): Selects the Current Limit of the P-Channel Switch. With $I_{PGM} = V_{IN}$, the current trip point is 600mA and with $I_{PGM} = 0V$, the current trip value is reduced to 340mA.

$\overline{\text{SHUTDOWN}}$ (Pin 8): Pulling this pin to ground keeps the internal switch off and puts the LTC1174 in micropower shutdown.

FUNCTIONAL DIAGRAM (Pin 1 connection shown for LTC1174-3.3 and LTC1174-5, changes create LTC1174)



* R1 = 51k FOR LTC1174-3.3
R1 = 93.5k FOR LTC1174-5

OPERATION (Refer to Functional Diagram)

The LTC1174 uses a constant off-time architecture to switch its internal P-channel power MOSFET. The off-time is set by an internal timing capacitor and the operating frequency is a function of V_{IN}.

The output voltage is set by an internal resistive divider (LTC1174-3.3 and LTC1174-5) or an external divider returned to V_{FB} pin 1 (LTC1174). A voltage comparator A1 compares the divided output voltage to a reference voltage of 1.25V.

To optimize efficiency, the LTC1174 automatically switches between continuous and Burst Mode™ operation. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the current comparator controls the output voltage in continuous mode.

During the switch "ON" time, switch current flows through the 0.1Ω sense resistor. When this current reaches the threshold of the current comparator A2, its output signal will change state, setting the flip-flop and turning the switch off.

The timing capacitor, C_T, begins to discharge until its voltage goes below V_{TH1}. Comparator A4 will then trip, which resets the flip-flop and causes the switch to turn on again. Also, the timing capacitor is recharged. The inductor current will again ramp up until the current comparator A2 trips. The cycle then repeats.

When the load is relatively light, the LTC1174 automatically goes into Burst Mode operation. The current mode loop is interrupted when the output voltage reaches the desired regulated value. The hysteretic voltage comparator A1 trips when V_{OUT} is above the desired output voltage, shutting off the switch and causing the timing capacitor to discharge. This capacitor discharges past V_{TH1} until its voltage drops below V_{TH2}. Comparator A5 then trips and a sleep signal is generated.

In sleep mode, the LTC1174 is in standby and the load current is supplied by the output capacitor. All unused

Burst Mode™ is a trademark of Linear Technology Corporation.

OPERATION (Refer to Functional Diagram)

circuitry is shut off, reducing quiescent current from 0.45mA to 0.13mA. When the output capacitor discharges by the amount of the hysteresis of the comparator A1, the P-channel switch turns on again and the process repeats itself.

Operating Frequency and Inductor

Since the LTC1174 utilizes a constant off-time architecture, its operating frequency is dependent on the value of V_{IN}. The frequency of operation can be expressed as:

$$f = \frac{1}{t_{OFF}}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) \text{(Hz)}$$

where $t_{OFF} = 4\mu s$ and V_D is the voltage drop across the diode. Note that the operating frequency is a function of the input and ouput voltage.

Although the size of the inductor does not affect the frequency, it does affect the ripple current. The peak-to-peak ripple current is given by:

$$I_{RIPPLE} = 4 \times 10^{-6}\left(\frac{V_{OUT} + V_D}{L}\right) (A_{P-P})$$

By choosing a smaller inductor, a low ESR output filter capacitor has to be used (see C_{IN} and C_{OUT}). Moreover, core loss will also increase (see Inductor Core Selection section) due to higher ripple current.

APPLICATIONS INFORMATION

Inductor Core Selection

With the value of L selected, the type of inductor must be chosen. Basically there are two kinds of losses in an inductor, core and copper

Core losses are dependent on the peak-to-peak ripple current and the core material. However it is independent of the physical size of the core. By increasing the inductance the inductor's peak-to-peak ripple current will decrease, therefore reducing core loss. Utilizing low core loss material, such as molypermalloy or Kool Mμ will allow users to concentrate on reducing copper loss and preventing saturation. Figure 1 shows the effect of different core material on the efficiency of the LTC1174. The CTX core is Kool Mμ and the CTXP core is powdered iron (material 52).

Although higher inductance reduces core loss, it increases copper loss as it requires more windings. When space is not a premium larger gauge wire can be used to reduce the wire resistance. This also prevents excessive heat dissipation.

C_{IN}

In continuous mode the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for

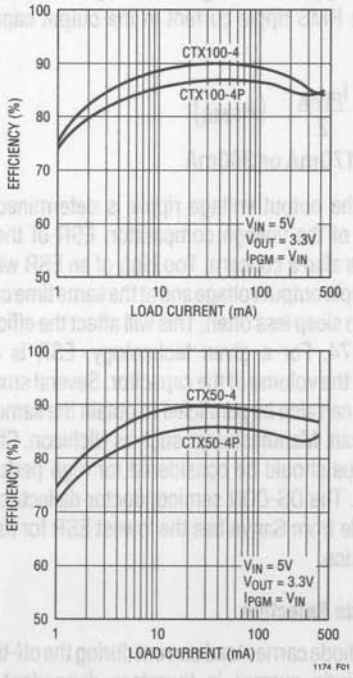


Figure 1. Efficiency Using Different Types of Inductor Core Material

APPLICATIONS INFORMATION

the maximum RMS current must be used. The C_{IN} RMS current is given by:

$$I_{RMS} \approx \frac{I_{OUT}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}} \left(A_{RMS}\right)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used for design because even significant deviations do not offer much relief. Note that ripple current directly affects capacitor's lifetime. DO NOT UNDERSPECIFY THIS COMPONENT. An additional 0.1µF ceramic capacitor is also required on V_{IN} for high frequency decoupling.

C_{OUT}

To avoid overheating, the output capacitor must be sized to handle the ripple current generated by the inductor. The worst case RMS ripple current in the output capacitor is given by:

$$I_{RMS} \approx \frac{I_{PEAK}}{2} \left(A_{RMS}\right)$$
$$= 170\text{mA or } 300\text{mA}$$

Although the output voltage ripple is determined by the hysteresis of the voltage comparator, ESR of the output capacitor is also a concern. Too high of an ESR will create a higher ripple output voltage and at the same time cause the LTC1174 to sleep less often. This will affect the efficiency of the LTC1174. For a given technology, ESR is a direct function of the volume of the capacitor. Several small-sized capacitors can also be paralleled to obtain the same ESR as one large can. Manufacturers such as Nichicon, Chemicon and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size, at a higher price.

Catch Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Most LTC1174 circuits will be well served by either a 1N5818, an MBRS140T3 or an MBR0520L Schottky diode.

Short-Circuit Protection

The LTC1174 is protected from output short by its internal current limit. Depending on the condition of I_{PGM} pin, the limit is either set to 340mA or 600mA. In addition, the off-time of the switch is increased to allow the inductor's current to decay far enough to prevent any current build-up (see Figure 2).

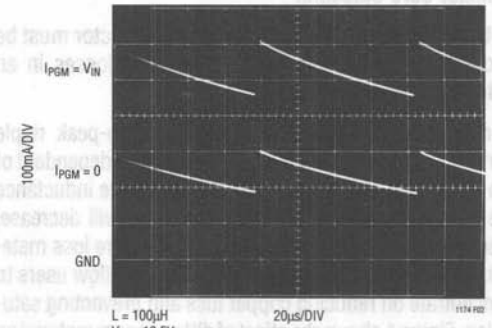


Figure 2. Inductor's Current with Output Shorted

Low-Battery Detector

The low-battery indicator senses the input voltage through an external resistive divider. This divided voltage connects to the "–" input of a voltage comparator (pin 3) which is compared with a 1.25V reference voltage. With the current going into pin 3 being negligible, the following expression is used for setting the trip limit:

$$V_{LBTRIP} = 1.25\left(1 + \frac{R4}{R3}\right)$$

APPLICATIONS INFORMATION

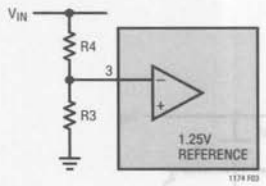


Figure 3. Low-Battery Comparator

LTC1174 Adjustable Applications

The LTC1174 develops a 1.25V reference voltage between the feedback (pin 1) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

For most applications, a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1174.

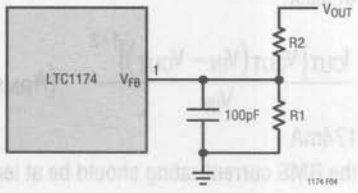


Figure 4. LTC1174 Adjustable Configuration

Inverting Applications

The LTC1174 can easily be set up for a negative output voltage. If –5V is desired, the LTC1174-5 is ideal for this application as it requires the least components. Figure 5 shows the schematic for this application. Note that the output voltage is now taken off the GND pin. Therefore, the maximum input voltage is now determined by the difference between the absolute maximum voltage rating and the output voltage. A maximum of 12V is specified in Figure 5, giving the circuit a 1.5V of headroom for V_{IN}. Note that the circuit can operate from a minimum of 4V, making it ideal for a 4 NiCad cell application. For a higher output current circuit, please refer to the Typical Applications section.

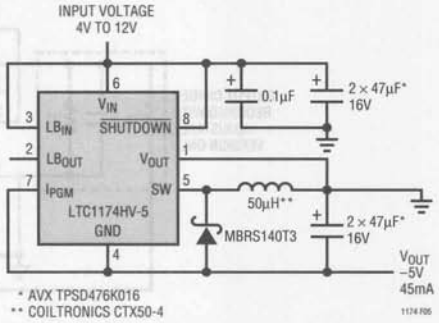


Figure 5. Positive-to-Negative 5V Converter

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1174. These items are also illustrated graphically in the layout diagram in Figure 6. Check the following in your layout:

1. Is the Schottky catch diode *closely* connected between ground (pin 4) and switch (pin 5)?
2. Is the "+" plate of C_{IN} *closely* connected to V_{IN} (pin 6)? This capacitor provides the AC current to the internal P-channel MOSFET.
3. Is the 0.1µF V_{IN} decoupling capacitor *closely* conected between V_{IN} (pin 6) and ground (pin 4)? This capacitor carries the high frequency peak currents.
4. Is the $\overline{\text{SHUTDOWN}}$ (pin 8) actively pulled to V_{IN} during normal operation? The $\overline{\text{SHUTDOWN}}$ pin is high impedance and must not be allowed to float.
5. Is the I_{PGM} (pin 7) pulled either to V_{IN} or ground? The I_{PGM} pin is high impedance and must not be allowed to float.

APPLICATIONS INFORMATION

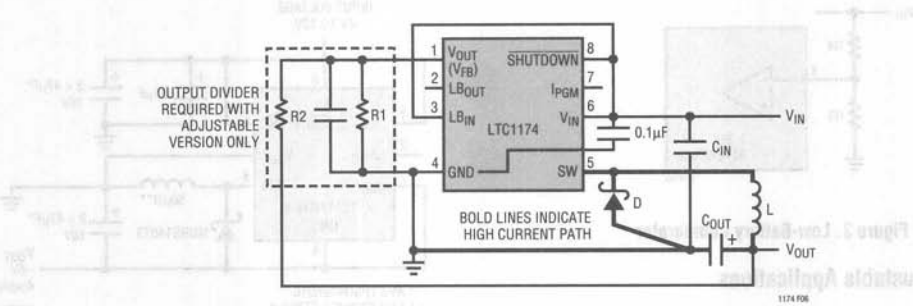


Figure 6. LTC1174 Layout Diagram (See Board Layout Checklist)

DESIGN EXAMPLE

As a design example, assume V_{IN} = 9V (nominal), V_{OUT} = 5V, and I_{OUT} = 350mA maximum. The LTC1174-5 is used for this application, with I_{PGM} (pin 7) connected to V_{IN}. The minmum value of L is determined by assuming the LTC1174-5 is operating in continuous mode.

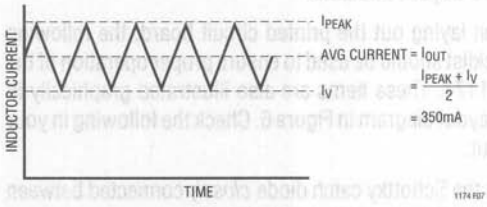


Figure 7. Continuous Inductor Current

With I_{OUT} = 350mA and I_{PEAK} = 0.6A (I_{PGM} = V_{IN}), I_V = 0.1A.The peak-to-peak ripple inductor current, I_{RIPPLE}, is 0.5A and is also equal to:

$$I_{RIPPLE} = 4 \times 10^{-6}\left(\frac{V_{OUT} + V_D}{L}\right) \quad (A_{P-P})$$

Solving for L in the above equation and with V_D = 0.6V, L = 44.8µH. The next higher standard value of L is 50µH (example: Coiltronics CTX50-4). The operating frequency, neglecting voltage across diode V_D is:

$$f \approx 2.5 \times 10^5\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 111kHz$$

With the value of L determined, the requirements for C_{IN} and C_{OUT} are calculated. For C_{IN}, its RMS current rating should be at least:

$$I_{RMS} = \frac{I_{OUT}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}} \quad (A_{RMS})$$

$$= 174mA$$

For C_{OUT}, the RMS current rating should be at least:

$$I_{RMS} \approx \frac{I_{PEAK}}{2} \quad (A_{RMS})$$

$$= 300mA$$

Now allow V_{IN} to drop to 6V. At this minimum input voltage the operating frequency will decrease. The new frequency is 42kHz.

APPLICATIONS INFORMATION

Table 1. Inductor Manufacturers

MANUFACTURER	PART NUMBER
Coilcraft 1102 Silver Lake Road Cary, IL 60013 (708) 639-2361	DT3316 Series
Coiltronics Inc. 6000 Park of Commerce Blvd. Boca Raton, FL 33487 (407) 241-7876	Econo-Pac Octa-Pac
Gowanda Electronics Corporation 1 Industrial Place Gowanda, NY 14070 (716) 532-2234	GA10 Series
Sumida Electric Co. Ltd. 637 E. Golf Road, Suite 209 Arlington Heights, IL 60005 (708) 956-0666/7	CD 54 Series CD 75 Series

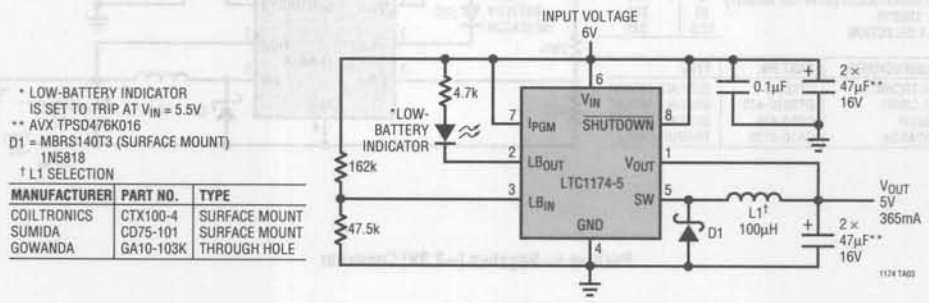
Table 2. Capacitor Manufacturers

MANUFACTURER	PART NUMBER
AVX Corporation P.O. Box 887 Myrtle Beach, SC 29578 (803) 448-9411	TPS Series TAJ Series
Nichicon America Corporation 927 East State Parkway Schaberg, IL 60173 (708) 843-7500	PL Series
Sanyo Video Components 2001 Sanyo Avenue San Diego, CA 92173 (619) 661-6385 Attn: Sales Dept.	OS-CON Series

TYPICAL APPLICATIONS

4

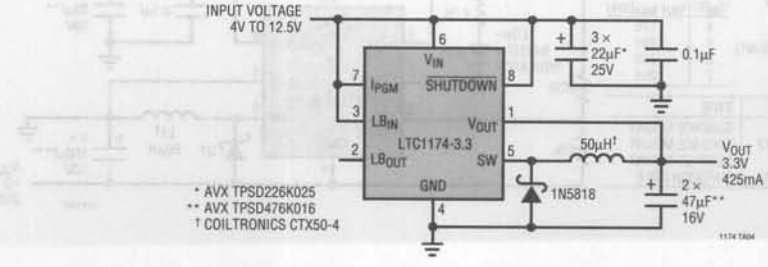
6V to 5V Step-Down Regulator with Low-Battery Detection



* LOW-BATTERY INDICATOR IS SET TO TRIP AT V_{IN} = 5.5V
** AVX TPSD476K016
D1 = MBRS140T3 (SURFACE MOUNT)
1N5818
† L1 SELECTION

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX100-4	SURFACE MOUNT
SUMIDA	CD75-101	SURFACE MOUNT
GOWANDA	GA10-103K	THROUGH HOLE

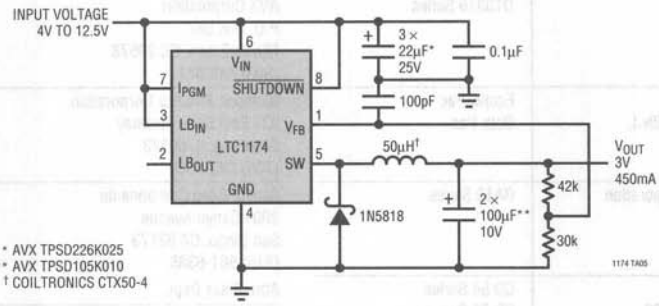
High Efficiency 3.3V Regulator



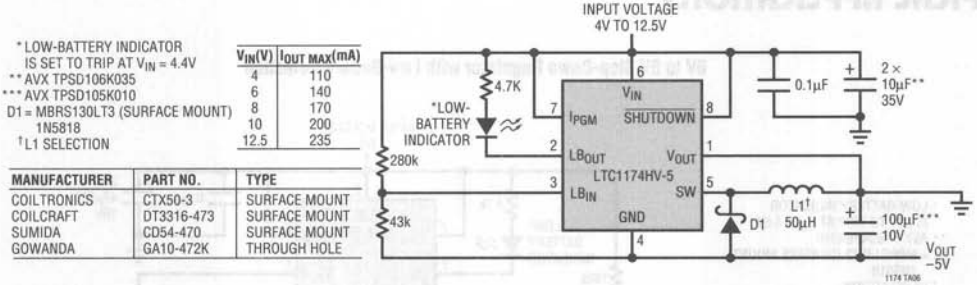
* AVX TPSD226K025
** AVX TPSD476K016
† COILTRONICS CTX50-4

TYPICAL APPLICATIONS

High Efficiency 3V Regulator



Positive-to-Negative (–5V) Converter

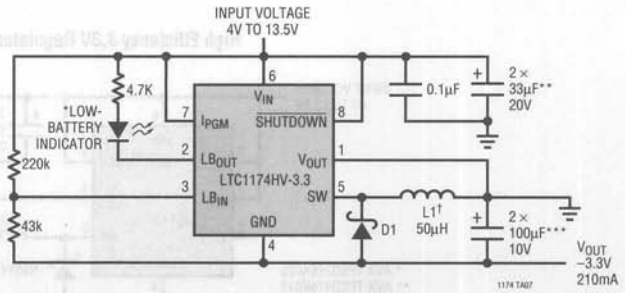


* LOW-BATTERY INDICATOR IS SET TO TRIP AT V_{IN} = 4.4V
** AVX TPSD106K035
*** AVX TPSD105K010
D1 = MBRS130LT3 (SURFACE MOUNT) 1N5818
† L1 SELECTION

V_{IN}(V)	$I_{OUT\ MAX}$(mA)
4	110
6	140
8	170
10	200
12.5	235

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-3	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

Positive-to-Negative (–3.3V) Converter



* LOW-BATTERY INDICATOR IS SET TO TRIP AT V_{IN} = 4.4V
** AVX TPSD336K020
*** AVX TPSD105K010
D1 = MBRS140T3 (SURFACE MOUNT) 1N5818
† L1 SELECTION

V_{IN}(V)	$I_{OUT\ MAX}$(mA)
4	175
5	205
6	230
7	255

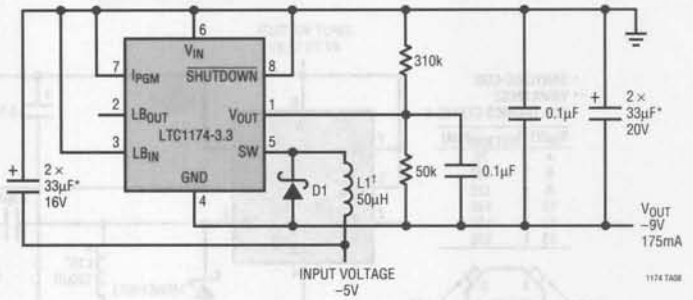
MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-3	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

TYPICAL APPLICATIONS

Negative Boost Converter

* AVX TPSD336K020
D1 = MBRS140T3 (SURFACE MOUNT)
1N5818
† L1 SELECTION

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-3	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

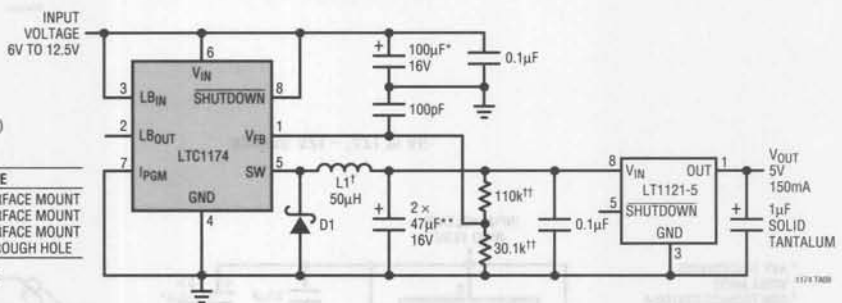


9V to 5V Pre-Post Regulator

* SANYO OS-CON
** AVX TPSD476K016
D1 = MBRS140T3 (SURFACE MOUNT)
1N5818
† L1 SELECTION

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-3	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

†† USE 1% METAL FILM RESISTORS



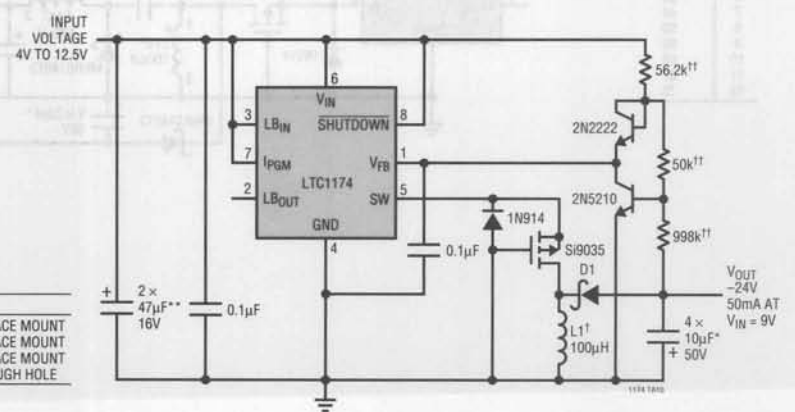
LCD Display Power Supply

V_{IN}(V)	$I_{OUT\ MAX}$(mA)
4	20
5	25
6	30
7	35
8	43
9	50
10	55
11	60
12	65

* AVX TAJE106K050
** AVX TPSD476K016
D1 = MBRS140T3 (SURFACE MOUNT)
1N5818
† L1 SELECTION

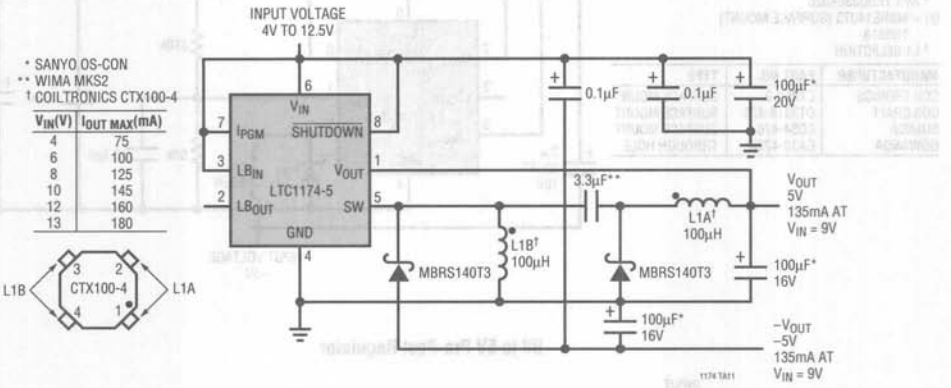
MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX100-3	SURFACE MOUNT
COILCRAFT	DT3316-104	SURFACE MOUNT
SUMIDA	CD75-101	SURFACE MOUNT
GOWANDA	GA10-103K	THROUGH HOLE

†† USE 1% METAL FILM RESISTORS

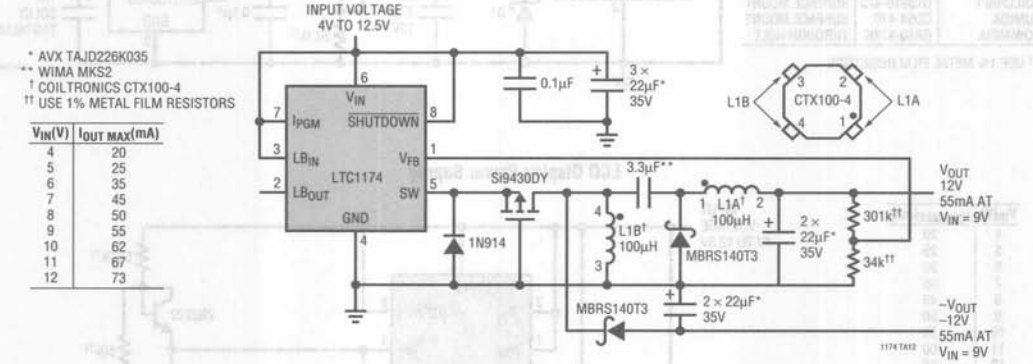


TYPICAL APPLICATIONS

9V to 5V, –5V Outputs

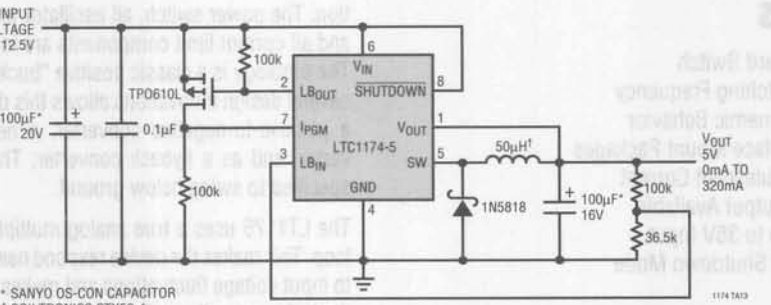


9V to 12V, –12V Outputs

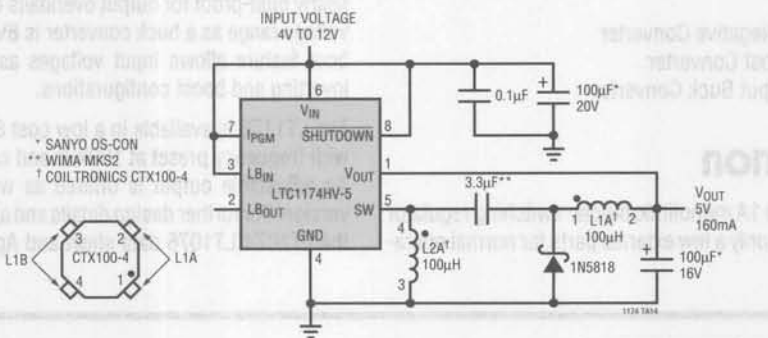


TYPICAL APPLICATIONS

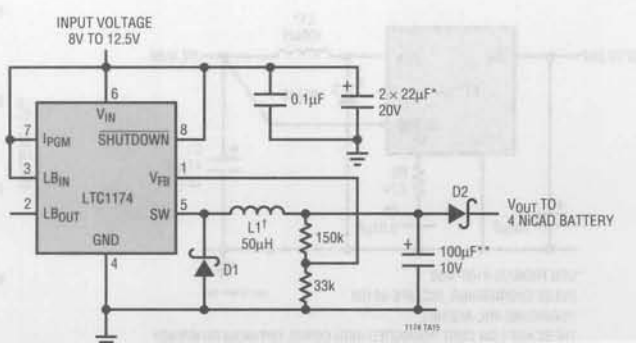
Automatic Current Selection



Buck-Boost Converter



Battery Charger



V_{IN}(V)	$I_{OUT\ MAX}$(mA)
8	320
9	325
10	330
11	335
12	335

* AVX TAJD226K020
** AVX TAJD107K010
D1, D2 = MBRS140T3 (SURFACE MOUNT) 1N5818
† L1 SELECTION

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-2P	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

Step-Down Switching Regulator

FEATURES

- 1.2A On-Board Switch
- 100kHz Switching Frequency
- Excellent Dynamic Behavior
- DIP and Surface Mount Packages
- Only 8mA Quiescent Current
- Preset 5V Output Available
- Operates Up to 35V Input
- Micropower Shutdown Mode

APPLICATIONS

- Buck Converter with Output Voltage Range of 2.5V to 30V
- Positive-to-Negative Converter
- Negative Boost Converter
- Mulitple Output Buck Converter

DESCRIPTION

The LT1176 is a 1A monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, and all current limit components are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allows this device to be used as a positive-to-negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing below ground.

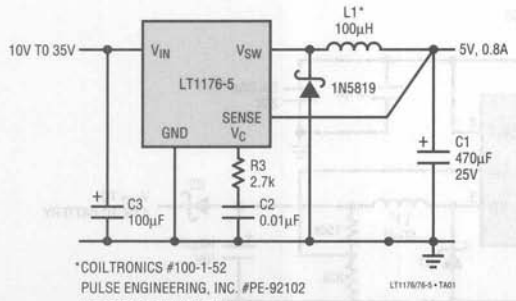
The LT1176 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

On-chip pulse by pulse current limiting makes the LT1176 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 35V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

The LT1176 is available in a low cost 8-lead DIP package with frequency preset at 100kHz and current limit at 1.7A An adjustable output is offered as well as a preset 5V version. For further design details and application help, see the LT1074/LT1076 data sheet and Application Note 44.

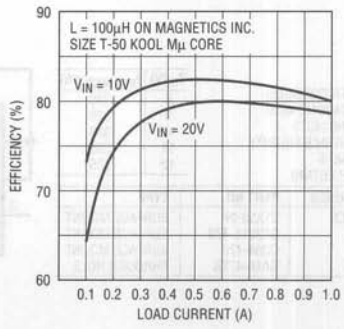
TYPICAL APPLICATION

Basic 5V Positive Buck Converter



*COILTRONICS #100-1-52
PULSE ENGINEERING, INC. #PE-92102
HURRICANE #HL-AG210LL
THESE ARE LOW COST POWDERED IRON CORES. OPTIMUM EFFICIENCY AND SMALLEST SIZE IS OBTAINED BY USING A LOW LOSS CORE SUCH AS MAGNETICS INC. KOOL Mµ. SEE EFFICIENCY GRAPH.

5V Buck Converter Efficiency

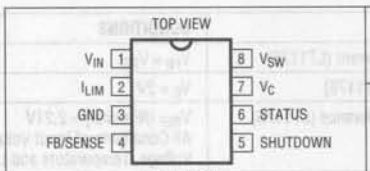


ABSOLUTE MAXIMUM RATINGS

Input Voltage 38V
Switch Voltage With Respect to Input Voltage..... 50V
Switch Voltage With Respect to Ground Pin
(V_{SW} Negative) (Note 6) 20V
Feedback Pin Voltage.....–2V, 10V
Shutdown Pin Voltage (Not to Exceed V_{IN}) 35V
Status Pin Voltage
(Current Must Be Limited to 5mA When Status Pin Switches "ON") 30V
I_{LIM} Pin Voltage (Forced)..... 5.5V
Maximum Operating Ambient Temperature Range
LT1176C/LT1176C-5 ..... 0°C to 70°C
Maximum Operating Junction Temperature Range
LT1176C/LT1176C-5 ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) 300°C

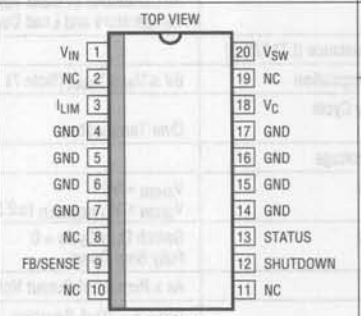
*These thermal resistance numbers are for typical mounting technique. Lower thermal resistance can be obtained with large copper lands, thermal glues or heatsinks.

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 125°C, θ_{JA} = 90°C/W*

ORDER PART NUMBER
LT1176CN8
LT1176CN8-5



S PACKAGE
20-LEAD PLASTIC SOL
T_{JMAX} = 125 °C, θ_{JA} = 50°C/W*

ORDER PART NUMBER
LT1176CS
LT1176CS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 25V, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "ON" Voltage (Note 1)	I_{SW} = 0.2A				1.1	V
	I_{SW} = 1A	●			1.4	V
Switch "OFF" Leakage	V_{IN} = 25V, V_{SW} = 0				150	µA
	V_{IN} = V_{MAX}, V_{SW} = 0 (Note 7)				250	µA
Supply Current (Note 2)	V_{FB} = 2.5V, V_{IN} ≤ 35V	●		7.5	10	mA
	V_{SHDN} = 0.1V (Device Shutdown) (Note 8)	●		140.0	300	µA
Minimum Supply Voltage	Normal Mode	●		7.3	8.0	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)	I_{LIM} Open	●	1.2	1.7	2.2	A
	R_{LIM} = 10k (Note 5)			1.2		A
	R_{LIM} = 7k (Note 5)			0.8		A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
		●	85		120	kHz
	V_{FB} = 0V Through 2k (Note 4) (LT1176)			20		kHz
	V_{SENSE} = 0V (Note 4) (LT1176-5)			20		kHz
Switching Frequency Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 9)	1V ≤ V_C ≤ 4V			2000		V/V
Error Amplifier Transconductance (Note 9)			3700	5000	8000	µmho
Error Amplifier Source and Sink Current	Source (V_{FB} = 2V or V_{SENSE} = 4V)		100.0	140.0	225.0	µA
	Sink (V_{FB} = 2.5V or V_{SENSE} = 5.5V)		0.7	1.0	1.6	mA

4

ELECTRICAL CHARACTERISTICS $T_J = 25°C$, $V_{IN} = 25V$, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Pin Bias Current (LT1176)	$V_{FB} = V_{REF}$	●		0.5	2	µA
Reference Voltage (LT1176)	$V_C = 2V$	●	2.155	2.21	2.265	V
Reference Voltage Tolerance (LT1176)	V_{REF} (Nominal) = 2.21V			±0.5	±1.5	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1.0	±2.5	%
Sense Voltage (LT1176-5)	$V_C = 2V$	●	4.85	5	5.15	V
Sense Voltage Tolerance (LT1176-5)	V_{OUT} (Nominal) = 5V			±0.5	±2	%
	All Conditions of Input Voltage, Temperature and Load Current	●		±1.0	±3	%
Sense Pin Divider Resistance (LT1176-5)			3	5	8	kΩ
Output Voltage Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		–4.0		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	$V_{SHDN} = 5V$	●	5	10	20	µA
	$V_{SHDN} \le V_{THRESHOLD}$ (≅2.5V)	●			50	µA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.2	2.45	2.7	V
	Fully Shut Down	●	0.1	0.30	0.5	V
Status Window	As a Percent of Output Voltage		±4	±5	±6	%
Status High Level	I_{STATUS} = 10µA Sourcing	●	3.5	4.5	5.0	V
Status Low Level	I_{STATUS} = 1.6mA Sinking	●		0.25	0.4	V
Status Delay Time				9		µs
Status Minimum Width				30		µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "ON" voltage at current between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero. The LT1176-5 has $V_{SENSE} = 5.5V$.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥8V after start-up for proper regulation.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch-on times. During testing, V_{FB} or V_{SENSE} is adjusted to give a minimum switch-on time of 1µs.

Note 5: $I_{LM} = (R_{LIM} – 1k)/7.65k$

Note 6: Switch to input voltage limitation must also be observed.

Note 7: $V_{MAX} = 35V$

Note 8: Does not include switch leakage.

Note 9: Error amplifier voltage gain and transconductance are specified relative to the internal feedback node. To calculate gain and transconductance from the sense pin (Output) to the V_C pin on the LT1176-5, multiply by 0.44.

Application Hints

Although the LT1176 has a peak switch rating of 1.2A and a maximum duty cycle of 85%, it must be used cautiously in applications which require high switch current and high duty cycle simultaneously, to avoid excessive chip temperature. Thermal resistance is 90°C/W for the 8-pin DIP package and 50°C/W for the 20-pin SO. This limits continuous chip power dissipation to the 0.5W to 1W range. These numbers assume typical mounting techniques. Extra or thick copper connected to the leads can reduce thermal resistance. Bonding the package to the board or using a clip style heatsink can also help. The following formulas will give chip power dissipation and peak switch current for the standard buck converter. Note that surges less than 30 seconds do not need to be considered from a thermal standpoint, but for proper regulation, they must not result in peak switch currents exceeding the 1.2A limit.

$$\text{Power} = I_{LOAD}(V_{OUT}/V_{IN}) + V_{IN}[7mA + 3mA(V_{OUT}/V_{IN}) + 0.012(I_{LOAD})]$$

$$I_{PEAK} = I_{LOAD(PEAK)} + [V_{OUT}(V_{IN} – V_{OUT})]/2E^5(V_{IN})(L)$$

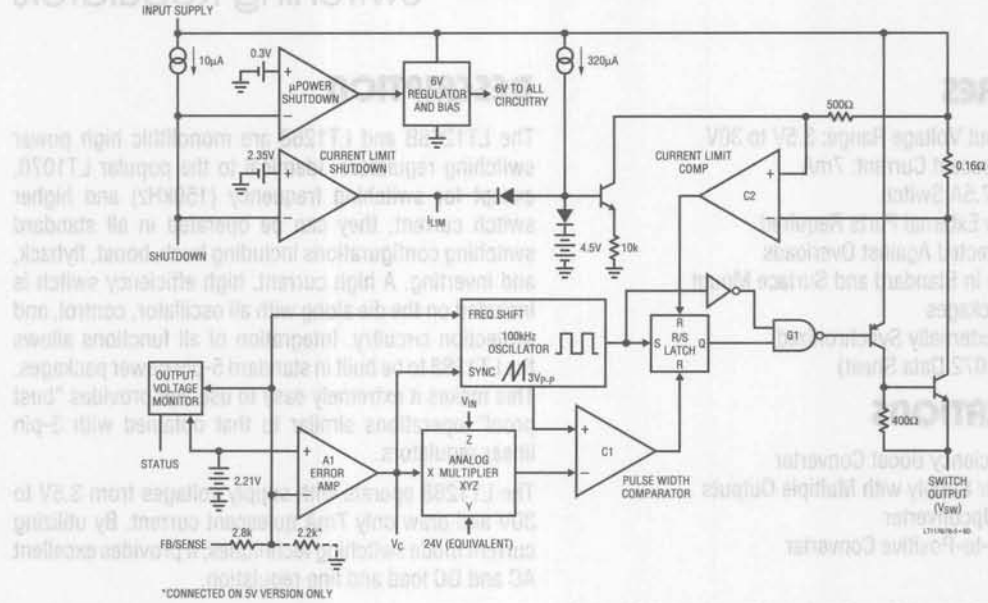
Example: $V_{IN} = 15V$, $V_{OUT} = 5V$, $I_{LOAD} = 0.5A$ Continuous, 0.8A Peak, $L = 100\mu H$

Power ($I_{LOAD} = 0.5A$) = 0.38W

I_{PEAK} ($I_{LOAD} = 0.8A$) = 0.97A

Where component size or height is critical, we suggest using solid tantalum capacitors (singly or in parallel), but be sure to use units rated for switching applications. Coiltronics is a good source for low profile surface mount inductors and AVX makes high quality surface mount tantalum capacitors. For further help, use Application Notes 19 and 44, LTC's SwitcherCAD computer design program, and our knowledgeable application department.

BLOCK DIAGRAM



4

7.5A, 150kHz Switching Regulators

FEATURES

- Wide Input Voltage Range: 3.5V to 30V
- Low Quiescent Current: 7mA
- Internal 7.5A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Available in Standard and Surface Mount 5-Pin Packages
- Can Be Externally Synchronized (See LT1072 Data Sheet)

APPLICATIONS

- High Efficiency Boost Converter
- PC Power Supply with Multiple Outputs
- Battery Upconverter
- Negative-to-Positive Converter

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1268B/LT1268. Application circuits are included to show the capability of the LT1268B/LT1268. A complete design manual (AN19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1268B/LT1268 factoring in the higher switch current rating and higher operating frequency.

DESCRIPTION

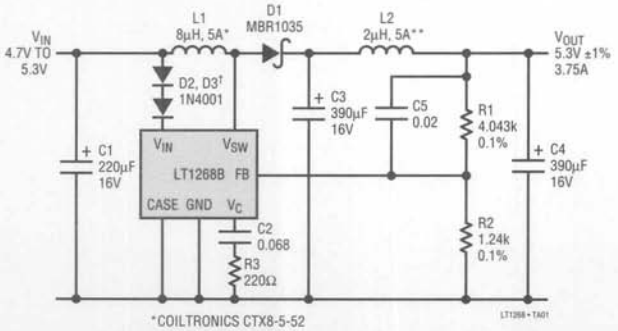
The LT1268B and LT1268 are monolithic high power switching regulators. Identical to the popular LT1070, except for switching frequency (150kHz) and higher switch current, they can be operated in all standard switching configurations including buck, boost, flyback, and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1268 to be built in standard 5-pin power packages. This makes it extremely easy to use and provides "bust proof" operations similar to that obtained with 3-pin linear regulators.

The LT1268 operate with supply voltages from 3.5V to 30V and draw only 7mA quiescent current. By utilizing current mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1268 use an adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 100μA typical for standby operation.

TYPICAL APPLICATION

Boost Regulator with 5.3V ±1% Output

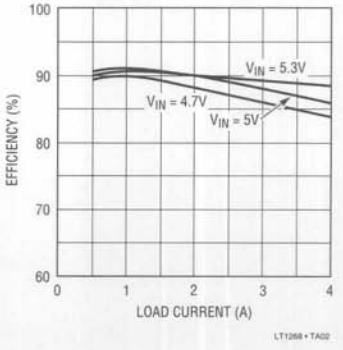


*COILTRONICS CTX8-5-52

**COILTRONICS CTX2-5-52

†OPTIONAL. D2 AND D3 ARE USED TO INCREASE UNDERVOLTAGE LOCKOUT FROM 2.7V TO ≈4V.

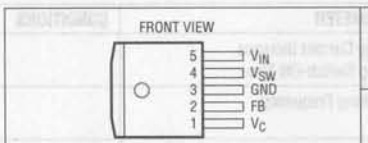
Efficiency of 5.3V Boost Converter



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Output Voltage 60V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Junction Temperature Range
Operating ..... 0°C to 125°C
Short-Circuit ..... 0°C to 140°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

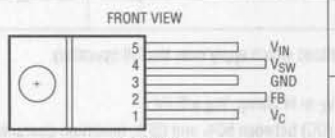


Q PACKAGE
5-LEAD DD

T_{JMAX} = 125°C, θ_{JC} = 2°C/W, θ_{JA} = See Notes 5 and 6

ORDER PART NUMBER

LT1268CQ
LT1268BCQ



T PACKAGE
5-LEAD TO-220

T_{JMAX} = 125°C, θ_{JC} = 2°C/W, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1268CT
LT1268BCT

Consult factory for Industrial and Military parts

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage Measured at Feedback Pin (Note 4)	LT1268B		1.235	1.244	1.253	V
			●	1.224	1.244	1.264	V
	Reference Voltage	LT1268		1.224	1.244	1.264	V
			●	1.214	1.244	1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	nA
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		3000	4400	6000	µmho
			●	2400		7000	µmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	µA
			●	120		400	µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.80		2.30	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage		●		2.8	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			7	10	mA
	Control Pin Threshold	Duty Cycle = 0		0.7	0.9	1.08	V
			●	0.5		1.25	V
BV	Output Switch Breakdown Voltage	3V ≤ V_{IN} ≤ V_{MAX}, I_{SW} = 5mA	●	60	75		V
V_{SAT}	Output Switch-ON Resistance (Note 1, 3)	T_J ≤ 100°C			0.12	0.18	Ω
		T_J ≤ 125°C				0.22	Ω
	Control Voltage to Switch Current Transconductance				12		A/V
I_{LIM}	Switch Current Limit (Note 3, 6)	Duty Cycle = 50%, T_J ≤ 100°C	●	7.50		15	A
		Duty Cycle = 65%, T_J ≤ 100°C	●	6.50		14	A

4

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch-ON Time				25	45	mA/A
f	Switching Frequency			120	150	180	kHz
			●	120		180	kHz
DC_{MAX}	Maximum Switch Duty Cycle			65	85	92	%
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.05V			100	500	µA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$		100	150	250	mV
			●	50		300	mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 65%, minimum guaranteed switch current is given by I_{LIM} = 6.25 (1.7 – DC).

Note 3: Minimum current limit is reduced by 0.5A at 125°C. 100°C test limits are guaranteed by correlation to 125°C tests.

Note 4: LT1268B reference voltage is specified at ±9mV to guarantee ±1% output voltage accuracy when 0.1% external resistors are used to set output voltage. To maintain output accuracy under load, load current should be taken from the case and the ground pin should be connected separately to output ground. See AN19 for details.

Note 5: The Q package is intended for surface mount without a separate heat sink. See graph for thermal resistance as a function of the mounting area. This curve assumes no other heat dissipators adjacent to package.

Note 6: Maximum switch current may be limited by package power dissipation, especially for the surface mount (Q) package. This package has a thermal resistance of 20°C/W to 50°C/W (see graph). The following formula will allow an estimate of maximum continuous switch current as a function of power loss and duty cycle. See AN19 for more details.

$$I_{MAX} = \sqrt{\frac{P}{R_{SW} \times DC}}$$

P = Power dissipation due to switch current

R_{SW} = Switch-ON resistance ≈0.15Ω

DC = Switch duty cycle

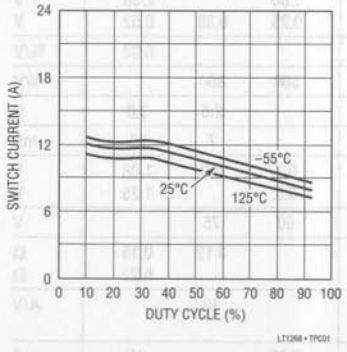
In a typical application where thermal resistance is 30°C/W, maximum power might be limited to 2W and power allocated to switch loss is 1.5W. For a duty cycle of 40%, this yields

$$I_{MAX} = \sqrt{\frac{1.5}{0.15 \times 0.4}} = 5A$$

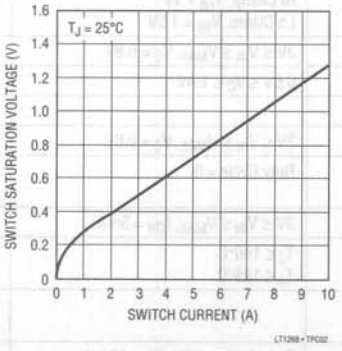
Obviously, a combination of high thermal resistance and high duty cycle may restrict switch current to a value well below the 7.5A electrical limit.

TYPICAL PERFORMANCE CHARACTERISTICS

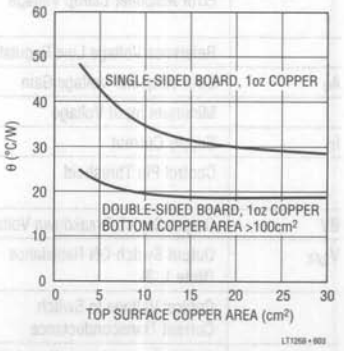
Switch Current Limit vs Duty Cycle



Switch Saturation Voltage

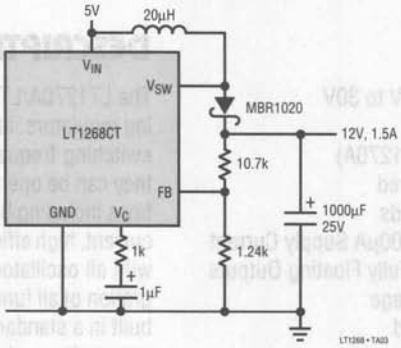


Q Package Thermal Resistance



TYPICAL APPLICATION

Boost Converter (5V TO 12V)



4

8A and 10A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range: 3.5V to 30V
- Low Quiescent Current: 7mA
- Internal 8A Switch (10A for LT1270A)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Shutdown Mode Draws Only 100μA Supply Current
- Flyback-Regulated Mode Has Fully Floating Outputs
- Comes in Standard 5-Pin Package
- Can be Externally Synchronized (See LT1072 Data Sheet)

APPLICATIONS

- High Efficiency Buck Converter
- PC Power Supply with Multiple Outputs
- Battery Upconverter
- Negative-to-Positive Converter

USER NOTE:

This data sheet is only intended to provide specifications, graphs and a general functional description of the LT1270A/LT1270. Application circuits are included to show the capability of the LT1270A/LT1270. A complete design manual (AN-19) should be obtained to assist in developing new designs. AN-19 contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. AN-19 can also be used for the LT1270A/LT1270 by factoring in the higher switch current rating and higher operating frequency.

A comprehensive CAD program called SwitcherCad is also available. Contact the local sales office in your area or the factory direct.

DESCRIPTION

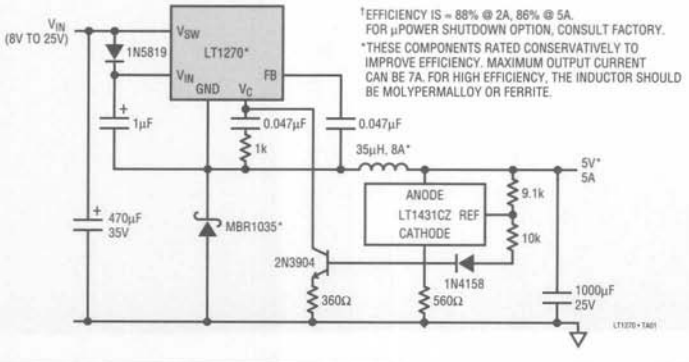
The LT1270A/LT1270 are monolithic high power switching regulators. Identical to the popular LT1070, except for switching frequency (60kHz) and higher switch current, they can be operated in all standard switching configurations including buck, boost, flyback, and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1270A/LT1270 to be built in a standard TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1270A/LT1270 operate with supply voltages from 3.5V to 30V, and draw only 7mA quiescent current. By utilizing current-mode switching techniques, they provide excellent AC and DC load and line regulation.

The LT1270A/LT1270 use adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 100μA typical for standby operation.

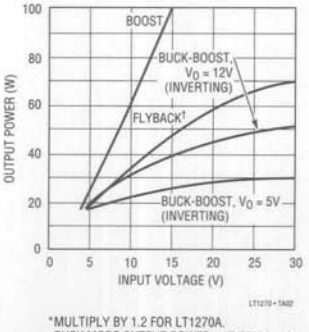
TYPICAL APPLICATION

High Efficiency† Buck Converter



†EFFICIENCY IS ≈ 88% @ 2A, 86% @ 5A.
FOR μPOWER SHUTDOWN OPTION, CONSULT FACTORY.
*THESE COMPONENTS RATED CONSERVATIVELY TO IMPROVE EFFICIENCY. MAXIMUM OUTPUT CURRENT CAN BE 7A. FOR HIGH EFFICIENCY, THE INDUCTOR SHOULD BE MOLYPERMALLOY OR FERRITE.

Maximum Output Power*

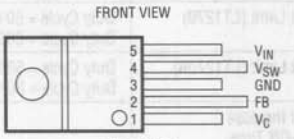


*MULTIPLY BY 1.2 FOR LT1270A.
BUCK MODE OUTPUT POWER ≈ (7.5A)(VOUT)
† TRANSFORMER TURNS RATIO MUST BE OPTIMUM TO ACHIEVE FULL POWER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Output Voltage 60V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Junction Temperature Range
LT1270AC/LT1270C (Oper.) ..... 0°C to 125°C
LT1270AC/LT1270C (Short-Ckt) ..... 0°C to 140°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



T PACKAGE
5-LEAD TO-220

T_{JMAX} = 100°C, θ_{JA} = 2°C/W, θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1270CT
LT1270ACT

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin V_C = 0.8V	 ●	1.224 1.214	1.244 1.244	1.264 1.274	V V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750 1100	nA nA
gm	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	3000 2400	4400	6000 7000	µmho µmho
	Error Amplifier Source of Sink Current	V_C = 1.5V	 ●	150 120	200	350 400	µA µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V Lo Clamp, V_{FB} = 1.5V		1.80 0.25	 0.38	2.30 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage		●		2.8	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			7	10	mA
	Control Pin Threshold	Duty Cycle = 0	 ●	0.70 0.50	0.90	1.08 1.25	V V
	Normal/Flyback Threshold on Feedback Pin			0.40	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	I_{FB} = 50µA	 ●	15.0 14.0	16.3	17.6 18.0	V V
V_{FB}	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50µA 3V ≤ V_{IN} ≤ V_{MAX}			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10µA		150	300	650	µmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V Source I_{FB} = 50µA Sink	● ●	15 25	32 40	70 70	µA µA
BV	Output Switch Breakdown Voltage	3V ≤ V_{IN} ≤ V_{MAX} I_{SW} = 1.5mA	●	60	75		V
V_{SAT}	Output Switch ON Resistance (Note 1, 3)	T_J ≤ 100°C T_J ≤ 125°C			0.12	0.18 0.22	Ω Ω
	Control Voltage to Switch Current Transconductance				12		A/V

4

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIM}	Switch Current Limit (LT1270) (Note 3)	Duty Cycle = 50%, $T_J \le 100°C$		8		16	A
		Duty Cycle = 80%, $T_J \le 100°C$	●	6		14	A
I_{LIM}	Switch Current Limit (LT1270A) (Note 3)	Duty Cycle = 50%, $T_J \le 100°C$		10.0		16.0	A
		Duty Cycle = 80%, $T_J \le 100°C$	●	7.5		14.0	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch-ON Time				25	40	mA/A
f	Switching Frequency			50	60	70	kHz
			●	50		70	kHz
DC_{MAX}	Maximum Switch Duty Cycle			80	92	95	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.05V			100	400	µA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$		100	150	250	mV
			●	50		300	mV

The ● denotes specifications which apply over the full operating temperature range.

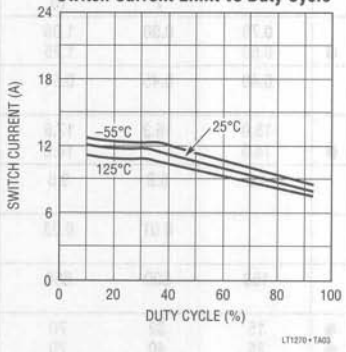
Note 1: Measured with V_C in Hi Clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 6.67 (1.7 – DC) for the LT1270 and I_{LIM} = 8.33 (1.7 – DC) for the LT1270A.

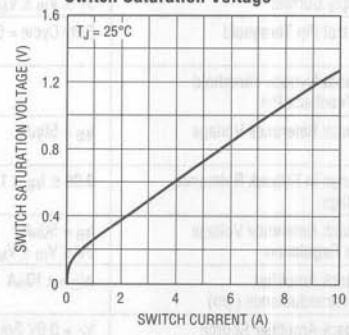
Note 3: Minimum current limit is reduced by 0.5A at 125°C. 100°C test limits are guaranteed by correlation to 125°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle

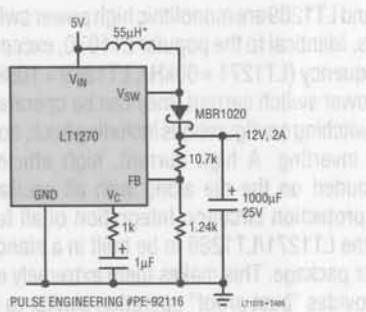


Switch Saturation Voltage

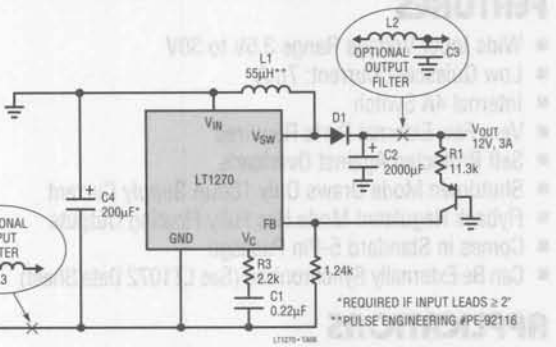


TYPICAL APPLICATIONS

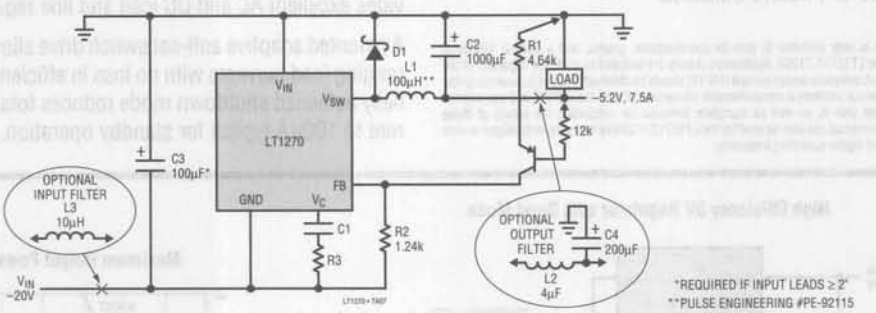
Boost Converter (5V to 12V)



Negative-to-Positive Buck-Boost Converter



Negative Buck Converter



4

4A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range 3.5V to 30V
- Low Quiescent Current: 7mA
- Internal 4A Switch
- Very Few External Parts Required
- Self Protected Against Overloads
- Shutdown Mode Draws Only 100μA Supply Current
- Flyback Regulated Mode Has Fully Floating Outputs
- Comes in Standard 5-Pin Package
- Can Be Externally Synchronized (See LT1072 Data Sheet)

APPLICATIONS

- Boost Converter
- High Efficiency Buck Converter
- PC Power Supply with Multiple Outputs
- Battery Up-Converter
- Negative-to-Positive Converter

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1271/LT1269. Application circuits are included to show the capability of the LT1271/LT1269. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1271/LT1269 by factoring in the higher switch current rating and higher operating frequency.

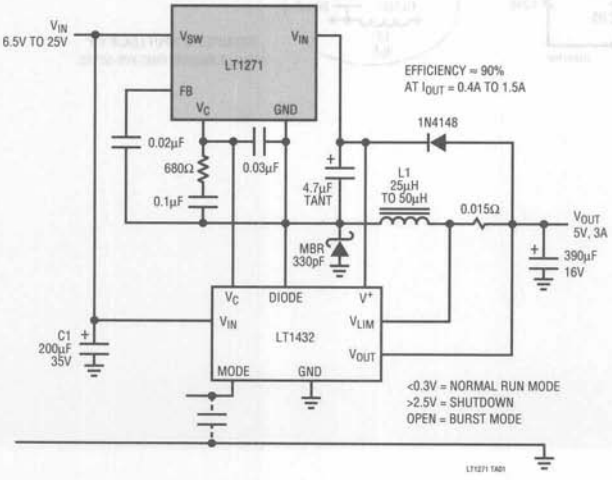
DESCRIPTION

The LT1271 and LT1269 are monolithic high power switching regulators. Identical to the popular LT1070, except for switching frequency (LT1271 = 60kHz, LT1269 = 100kHz) and slightly lower switch current, they can be operated in all standard switching configurations including buck, boost, flyback, and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1271/LT1269 to be built in a standard TO-220 power package. This makes them extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

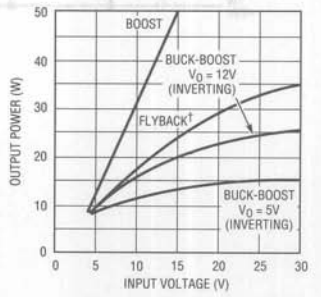
The LT1271/LT1269 operate with supply voltages from 3.5V to 30V, and draw only 7mA quiescent current. By utilizing current mode switching techniques, they provides excellent AC and DC load and line regulation.

A patented adaptive anti-sat switch drive allows very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 100μA typical for standby operation.

High Efficiency 5V Regulator with Burst Mode



Maximum Output Power



† BUCK MODE OUTPUT POWER ≈ (3.5A)(VOUT)
TRANSFORMER TURNS RATIO MUST BE OPTIMUM TO ACHIEVE FULL POWER.

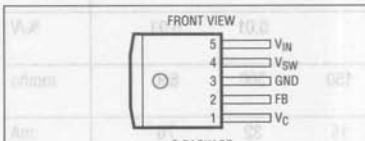
LT1271 TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Output Voltage 60V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V

Operating Junction Temperature Range
(Oper.) ..... 0°C to +100°C
(Short Ckt.) ..... 0°C to +125°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

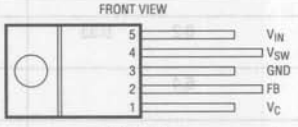
PACKAGE/ORDER INFORMATION



Q PACKAGE
5-LEAD PLASTIC DD

$T_{J\,MAX}$ = 100°C, θ_{JC} = 4°C/W, θ_{JA} = 30°C/W*

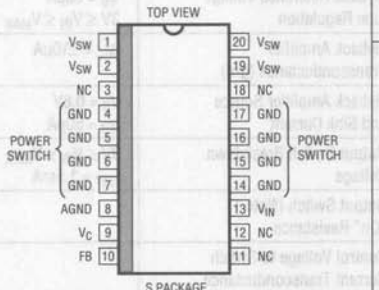
ORDER PART NUMBER
LT1271CQ
LT1269CQ



T PACKAGE
5-LEAD TO-220

$T_{J\,MAX}$ = 100°C, θ_{JC} = 4°C/W, θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1271CT
LT1269CT



S PACKAGE
20-LEAD PLASTIC SOL

$T_{J\,MAX}$ = 100°C, θ_{JC} = 4°C/W, θ_{JA} = 50°C/W**

ORDER PART NUMBER
LT1269CS

* With device soldered to 1/2 square inch of 1oz copper over backside or internal layer ground plane.

Consult factory for Industrial and Military grade parts.

** θ will vary from approximately 40°C/W with 0.75 sq. in. of 1oz copper to 46°C/W with 0.33 sq. in. of 1oz copper

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		V_C = 0.8V	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	nA
gm	Error Amplifier Transconductance	ΔI_C = ±25µA		3000	4400	6000	µmho
			●	2400		7000	µmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	µA
			●	120		400	µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage (Note 3)		●		2.8	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			7	10	mA

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	Control Pin Threshold	Duty Cycle = 0			0.7	0.9	1.08	V
				●	0.5		1.25	V
	Normal/Flyback Threshold on Feedback Pin				0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	I_{FB} = 50µA			15	16.3	17.6	V
				●	14		18	V
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1µA			4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50µA 3V ≤ V_{IN} ≤ V_{MAX}				0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10µA			150	300	650	mmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V I_{FB} = 50µA	Source Sink	● ●	15 25	32 40	70 70	mA mA
BV	Output Switch Breakdown Voltage	3V ≤ V_{IN} ≤ V_{MAX} I_{SW} = 1.5mA		●	60	75		V
V_{SAT}	Output Switch (Note 1) "On" Resistance			●		0.2	0.33	Ω
	Control Voltage to Switch Current Transconductance					6.4		A/V
I_{LIM}	Switch Current Limit (Note 2)	Duty Cycle = 50% Duty Cycle = 80%		● ●	4 3.2		8 8	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time					25	40	mA/A
f	Switching Frequency	LT1271 LT1269		● ●	50 85	60 100	70 115	kHz kHz
DC (max)	Maximum Switch Duty Cycle	LT1271 LT1269			85 80	92 90	95 95	% %
	Flyback Sense Delay Time					1.5		µs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.05V				100	400	µA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}			100	150	250	mV
				●	50		300	mV

The ● denotes the specifications which apply over the full operating temperature range.

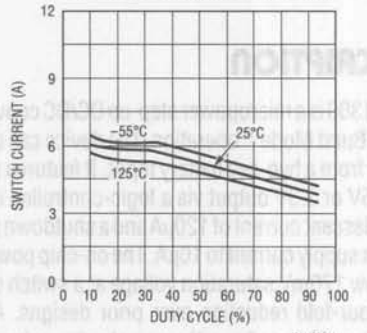
Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by I_{LIM} = 2.67 (2 – DC).

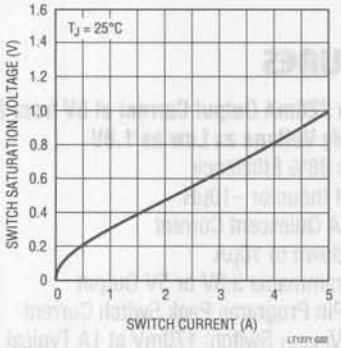
Note 3: Minimum input voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle

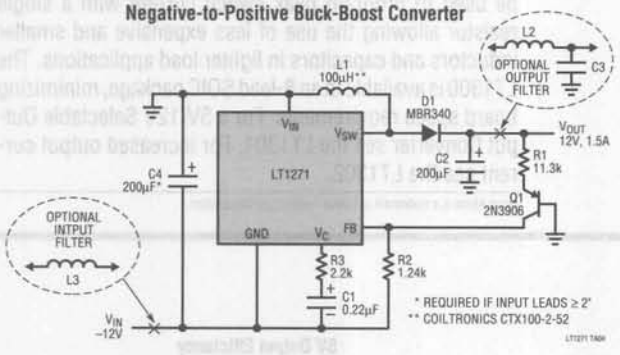


Switch Saturation Voltage

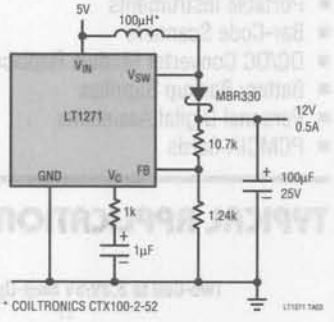


TYPICAL APPLICATIONS

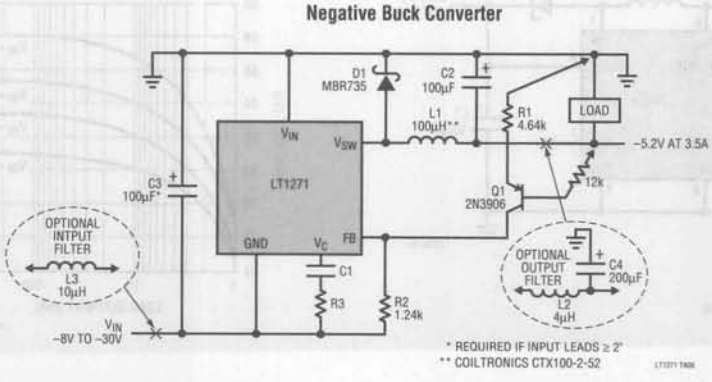
Negative-to-Positive Buck-Boost Converter



Boost Converter (5V to 12V)



Negative Buck Converter



Micropower High Efficiency 3.3/5V Step-Up DC/DC Converter

FEATURES

- **Up to 220mA Output Current at 5V from 2V Supply**
- **Supply Voltage as Low as 1.8V**
- Up to 88% Efficiency
- Small Inductor –10µH
- 120µA Quiescent Current
- Shutdown to 10µA
- Programmable 3.3V or 5V Output
- I_{LIM} Pin Programs Peak Switch Current
- Low V_{CESAT} Switch: 170mV at 1A Typical
- Uses Inexpensive Surface Mount Inductors
- 8-Lead DIP or SOIC Package

APPLICATIONS

- Palmtop Computers
- Portable Instruments
- Bar-Code Scanners
- DC/DC Converter Module Replacements
- Battery Backup Supplies
- Personal Digital Assistants
- PCMCIA Cards

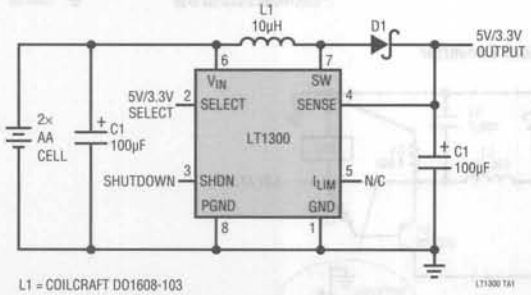
DESCRIPTION

The LT1300 is a micropower step-up DC/DC converter that utilizes Burst Mode™ operation. The device can deliver 5V or 3.3V from a two-cell battery input. It features programmable 5V or 3.3V output via a logic-controlled input, no-load quiescent current of 120µA and a shutdown pin which reduces supply current to 10µA. The on-chip power switch has a low 170mV saturation voltage at a switch current of 1A, a four-fold reduction over prior designs. A 155kHz internal oscillator allows the use of extremely small surface mount inductors and capacitors. Operation is guaranteed at 1.8V input. This allows more energy to be extracted from the battery increasing operating life. The I_{LIM} pin can be used to program peak switch current with a single resistor allowing the use of less expensive and smaller inductors and capacitors in lighter load applications. The LT1300 is available in an 8-lead SOIC package, minimizing board space requirements. For a 5V/12V Selectable Output Converter see the LT1301. For increased output current see the LT1302.

Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATIONS

Two-Cell to 3.3V/5V Step-Up Converter

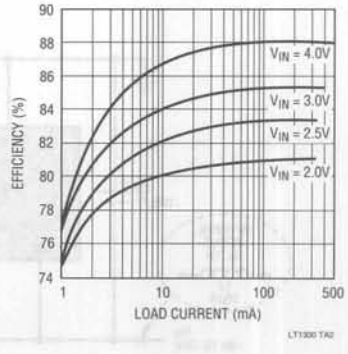


L1 = COILCRAFT DO1608-103
OR SUMIDA CD54-100

C1 = AVX TPSD107M010R0100
OR SANYO OS-CON 16SA100M

D1 = MBRS130LT3
OR 1N5817

5V Output Efficiency



ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 20V
Sense Voltage 10V
SHUTDOWN Voltage 10V
SELECT Voltage 10V
I_{LIM} Voltage 0.5V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1300CN8 LT1300CS8
S8 PART MARKING
1300

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2V unless otherwise noted.

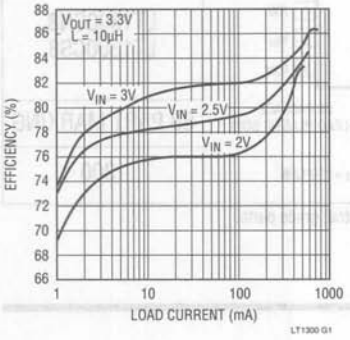
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{SEL} = 5V, V_{SENSE} = 5.5V	●		120	200	µA
		V_{SHDN} = 1.8V	●		7	15	µA
V_{IN}	Input Voltage Range			1.8			V
			●	2.0			V
V_{OUT}	Output Sense Voltage	V_{SEL} = 5V	●	4.80	5.0	5.20	V
		V_{SEL} = 0V	●	3.15	3.3	3.45	V
	Output Referred Comparator Hysteresis	V_{SEL} = 5V (Note 1)	●		22	50	mV
		V_{SEL} = 0V (Note 1)	●		14	35	mV
	Oscillator Frequency	Current Limit not Asserted. See Test Circuit.		120	155	185	kHz
	Oscillator TC				0.2		%/°C
DC	Maximum Duty Cycle			75	86	95	%
t_{ON}	Switch On Time	Current Limit not Asserted.			5.6		µs
	Output Line Regulation	1.8V < V_{IN} < 6V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 700mA	●		130	200	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Peak Switch Current (Internal Trip Point)	I_{LIM} Floating (See Typical Application)		0.75	1.0	1.25	A
		I_{LIM} Grounded			0.4		A
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low					0.5	V
V_{SELH}	Select Pin High		●	1.5			V
V_{SELL}	Select Pin Low		●			0.8	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		9	20	µA
		V_{SHDN} = 2V	●		3		µA
		V_{SHDN} = 0V	●		0.1	1	µA
I_{SEL}	Select Pin Bias Current	0V < V_{SEL} < 5V	●		1	3	µA

The ● denotes specifications which apply over the 0°C to 70°C temperature range.

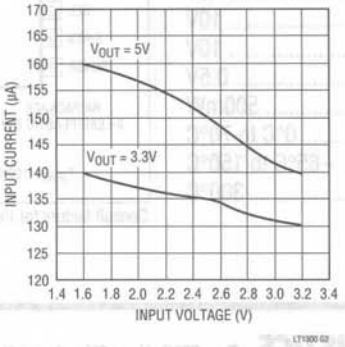
Note 1: Hysteresis specified is DC. Output ripple may be higher if output capacitance is insufficient or capacitor ESR is excessive. See applications section.

TYPICAL PERFORMANCE CHARACTERISTICS

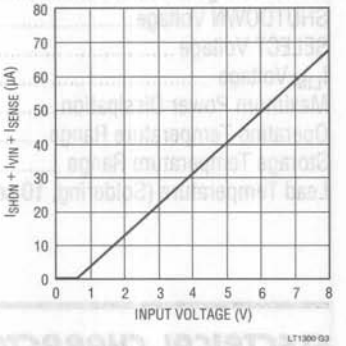
Efficiency



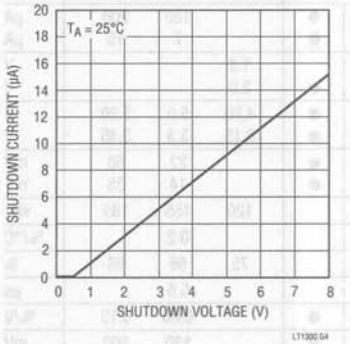
No-Load Battery Current



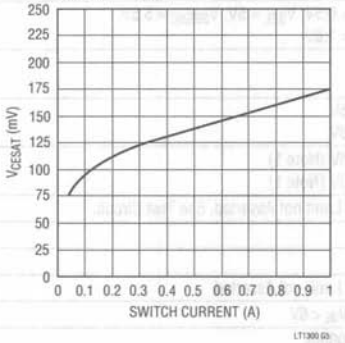
Total Quiescent Current in Shutdown



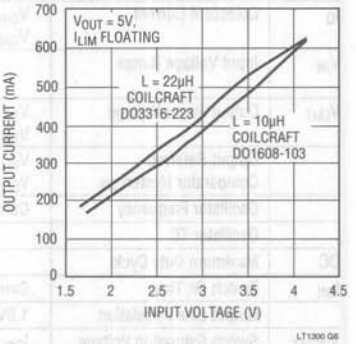
Shutdown Pin Bias Current



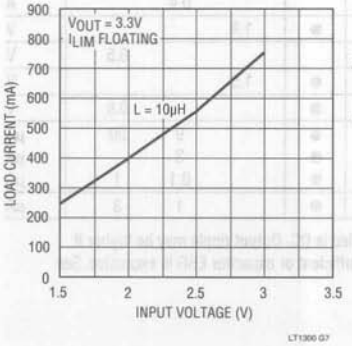
VCESAT vs ISW



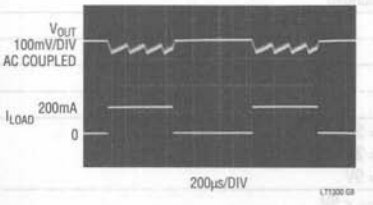
Maximum Output Current vs Input Voltage



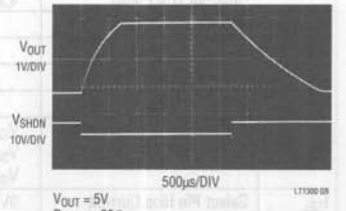
Maximum Output Current vs Input Voltage



Transient Response
VIN = 2V, VOUT = 5V



Startup Response



VOUT = 5V
RLOAD = 20Ω

PIN FUNCTIONS

GND (Pin 1): Signal Ground.

Sel (Pin 2): Output Select. When tied to V_{IN} or V_{OUT} converter regulates at 5V. When grounded converter regulates at 3.3V.

SHDN (Pin 3): Shutdown. Pull high to effect shutdown. Tie to ground for normal operation.

Sense (Pin 4): "Output" Pin.

I_{LIM} (Pin 5): Float for 1A switch current limit. Tie to ground for approximately 400mA. A resistor between I_{LIM} and ground sets peak current to some intermediate value (see Figure 5).

V_{IN} (Pin 6): Supply Pin. Must be bypassed with a large value electrolytic to ground. A 0.1µF ceramic capacitor close to the pin may be needed in some cases.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct to minimize electronic radiation.

PGND (Pin 8): Power Ground. Tie to signal ground (pin 1) under the package. Bypass capacitor from V_{IN} should be tied directly to the pin.

BLOCK DIAGRAM

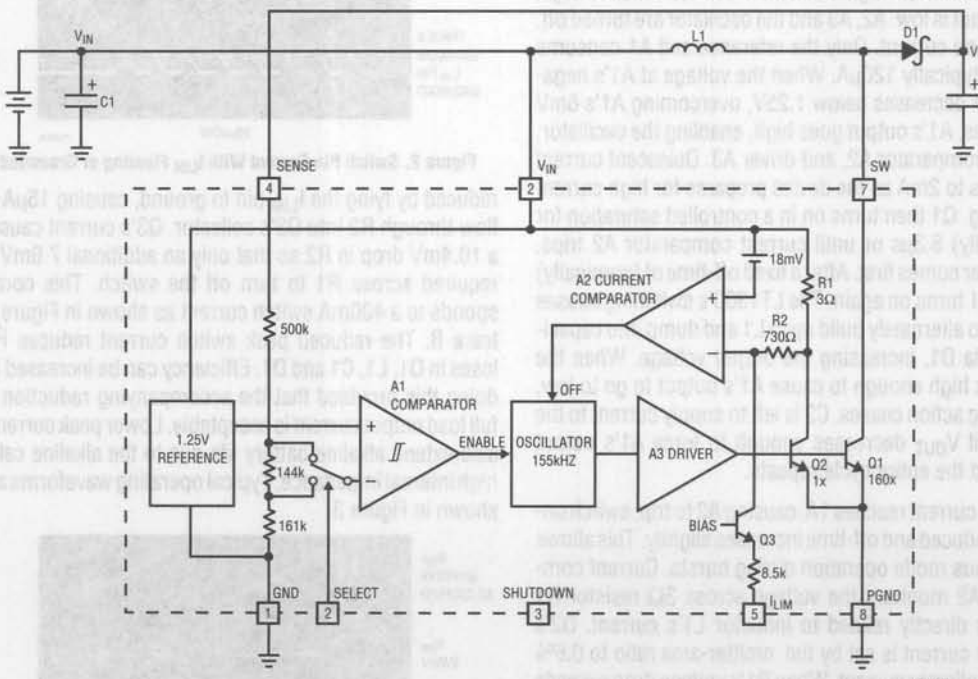
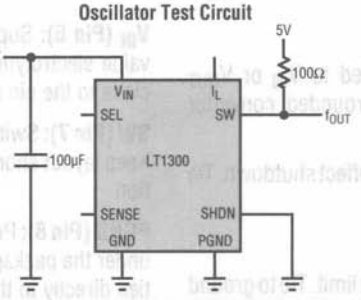


Figure 1.

TEST CIRCUIT

Oscillator Test Circuit



OPERATION

Operation of the LT1300 is best understood by referring to the Block Diagram in Figure 1. When A1's negative input, related to the Sense pin voltage by the appropriate resistor-divider ratio, is higher that the 1.25V reference voltage, A1's output is low. A2, A3 and the oscillator are turned off, drawing no current. Only the reference and A1 consume current, typically 120µA. When the voltage at A1's negative input decreases below 1.25V, overcoming A1's 6mV hysteresis, A1's output goes high, enabling the oscillator, current comparator A2, and driver A3. Quiescent current increases to 2mA as the device prepares for high current switching. Q1 then turns on in a controlled saturation for (nominally) 5.3µs or until current comparator A2 trips, whichever comes first. After a fixed off-time of (nominally) 1.2µs, Q1 turns on again. The LT1300's switching causes current to alternately build up in L1 and dump into capacitor C2 via D1, increasing the output voltage. When the output is high enough to cause A1's output to go to low, switching action ceases. C2 is left to supply current to the load until V_{OUT} decreases enough to force A1's output high, and the entire cycle repeats.

If switch current reaches 1A, causing A2 to trip, switch on-time is reduced and off-time increases slightly. This allows continuous mode operation during bursts. Current comparator A2 monitors the voltage across 3Ω resistor R1 which is directly related to inductor L1's current. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 18mV, corresponding to 1A inductor current, A2's output goes high, truncating the on-time portion of the oscillator cycle and increasing off-time to about 2µs as shown in Figure 2, trace A. This programmed peak current can be

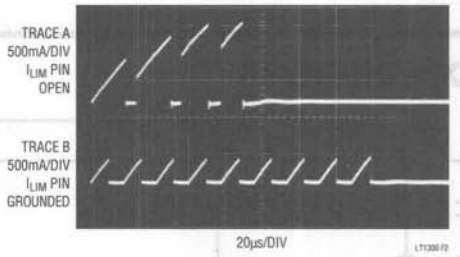


Figure 2. Switch Pin Current With I_{LIM} Floating or Grounded

reduced by tying the I_{LIM} pin to ground, causing 15µA to flow through R2 into Q3's collector. Q3's current causes a 10.4mV drop in R2 so that only an additional 7.6mV is required across R1 to turn off the switch. This corresponds to a 400mA switch current as shown in Figure 2, trace B. The reduced peak switch current reduces I^2R loses in Q1, L1, C1 and D1. Efficiency can be increased by doing this provided that the accompanying reduction in full load output current is acceptable. Lower peak currents also extend alkaline battery life due to the alkaline cell's high internal impedance. Typical operating waveforms are shown in Figure 3.

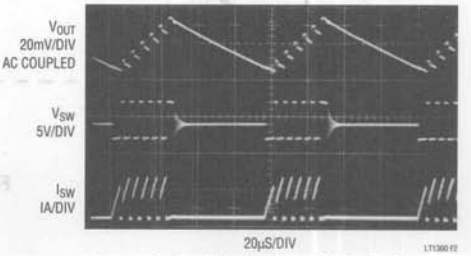


Figure 3. Burst Mode Operation in Action

APPLICATIONS INFORMATION

Output Voltage Selection

The LT1300 can be selected to 3.3V or 5V under logic control or fixed at either by tying SELECT to ground or V_{IN} respectively. It is permissible to tie SELECT to a voltage higher than V_{IN} as long as it does not exceed 10V. Efficiency in 3.3V mode will be slightly less that in 5V mode due to the fact that the diode drop is a greater percentage of 3.3V than 5V. Since the bipolar switch in the LT1300 gets its base drive from V_{IN}, no reduction in switch efficiency occurs when in 3.3V mode. When V_{IN} exceeds the programmed output voltage the output will follow the input. This is characteristic of the simple step-up or "boost" converter topology. A circuit example that provides a regulated output with an input voltage above or below the output (called a buck-boost or SEPIC) is shown in the Typical Applications section.

Shutdown

The converter can be turned off by pulling SHDN (pin 3) high. Quiescent current drops to 10µA in this condition. Bias current of 3µA to 5µA flows into the pin (at 2.5V input). It is recommended that SHDN not be left floating. Tie the pin to ground if the feature is not used.

I_{LIM} Function

The LT1300's current limit (I_{LIM}) pin can be used for soft start. Upon start-up, switching regulators require maximum current from the supply. The high currents flowing can create IR drops along supply and ground lines and are especially demanding on alkaline batteries. By installing an R1 and C3 as shown in Figure 4, the switch current in the LT1300 is limited to 400mA until the 15µA flowing out of the I_{LIM} pin charges up the 0.1µF capacitor. Input current is held to under 500mA while the output voltage ramps up to 5V as shown in Figure 5. The 1Meg resistor provides a discharge path for the capacitor without appreciably decreasing peak switch current. When the full capability of the LT1300 is not required, peak current can be reduced by changing the value of R3 as shown in Figure 6. With R3 = 0, switch current is limited to approximately 400mA.

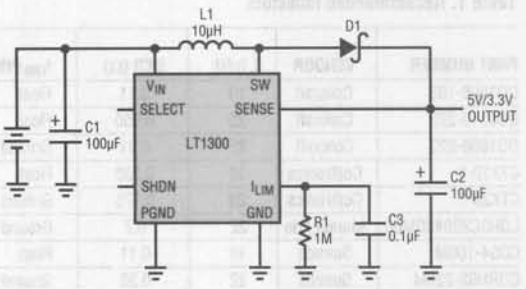


Figure 4. Addition of R1 and C3 Limit Input Current at Startup

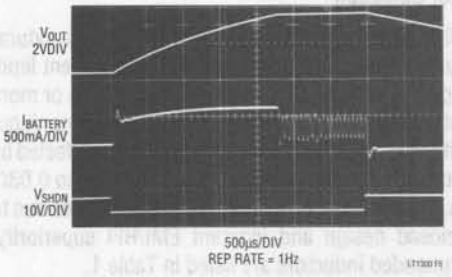


Figure 5. Startup Waveforms using Soft-Start Circuitry I_{LOAD} = 100mA, V_{OUT} = 5V

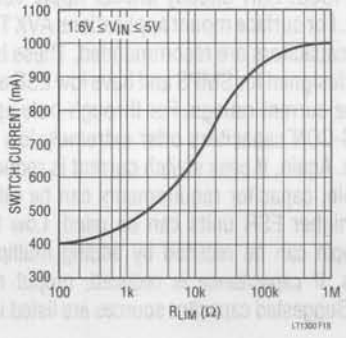


Figure 6. Peak Switch Current vs. R_{LIM}

APPLICATIONS INFORMATION

Table 1. Recommended Inductors

PART NUMBER	VENDOR	L (μH)	DCR (Ω)	I_{LIM} PIN	EFFICIENCY 2.5V_{IN}, 5V_{OUT} 50mA LOAD	EFFICIENCY 2.5V_{IN}, 5V_{OUT} 200mA LOAD	COMPONENT HEIGHT (mm)	PHONE NUMBER
DO1608-103	Coilcraft	10	0.11	Float	83	83	3.5	(708) 639-6400
DO3316-223	Coilcraft	22	0.050	Float	85	85	5.5	
DO1608-223	Coilcraft	22	0.31	Ground	85	—	3.5	
CTX10-1	Coiltronics	10	0.038	Float	85	85	4.2	(407) 241-7876
CTX20-1	Coiltronics	20	0.175	Ground	86	—	4.2	
LQH3C2204K0M00	Murata-Frie	22	0.7	Ground	81	—	2.0	(404) 436-1300
CD54-100M	Sumida	10	0.11	Float	85	85	4.5	(708) 956-0666
CDRH62-220M	Sumida	22	0.38	Ground	84	—	3.0	
CDRH62-100M	Sumida	10	0.17	Float	81	82	3.0	
GA10-102K	Gowanda	10	0.038	Float	85	86	6.6 Through-Hole	(716) 532-2234

Inductor Selection

For full output power, the inductor should have a saturation current rating of 1.25A for worst-case current limit, although it is acceptable to bias an inductor 20% or more into saturation. Smaller inductors can be used in conjunction with the I_{LIM} pin. Efficiency is significantly affected by inductor DCR. For best efficiency limit the DCR to 0.03Ω or less. Toroidal types are preferred in some cases due to their closed design and inherent EMI/RFI superiority. Recommended inductors are listed in Table 1.

Capacitor Selection

Low ESR capacitors are required for both input and output of the LT1300. ESR directly affects ripple voltage and efficiency. For surface mount applications AVX TPS series tantalum capacitors are recommended. These have been specially designed for SMPS and have low ESR along with high surge current ratings. For through-hole application Sanyo OS-CON capacitors offer extremely low ESR in a small size. Again, if peak switch current is reduced using the I_{LIM} pin, capacitor requirements can be relaxed and smaller, higher ESR units can be used. Low frequency output ripple can be reduced by adding multiple output capacitors. If capacitance is reduced, output ripple will increase. Suggested capacitor sources are listed in Table 2.

Table 2. Recommended Capacitors

VENDOR	SERIES	TYPE	PHONE#
AVX	TPS	Surface Mount	(803)448-9411
Sanyo	OS-CON	Through-Hole	(619) 661-6835
Panasonic	HFQ	Through-Hole	(201) 348-5200

Diode Selection

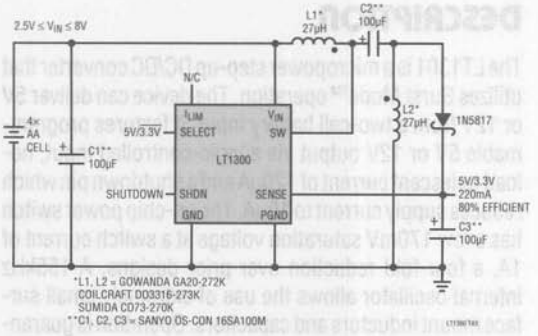
Best performance is obtained with a Schottky rectifier diode such as the 1N5817. Phillips Components makes this in surface mount as the PRLL5817. Motorola makes the MBRS130LT3 which is slightly better and also in surface mount. For lower output power a 1N4148 can be used although efficiency will suffer substantially.

Layout Considerations

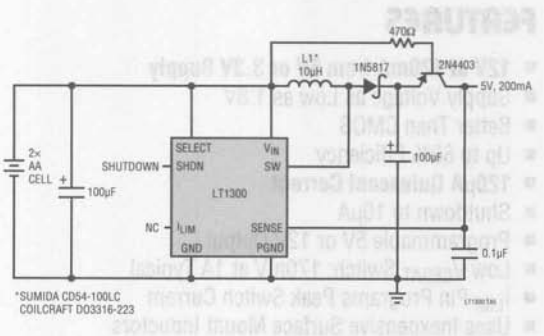
The LT1300 is a high speed, high current device. The input capacitor must be no more than 0.2" from V_{IN} (pin 6) and ground. Connect the PGND and GND (pins 8 and 1) together under the package. Place the inductor adjacent to SW (pin 7) and make the switch pin trace as short as possible. This keeps radiated noise to a minimum.

TYPICAL APPLICATIONS

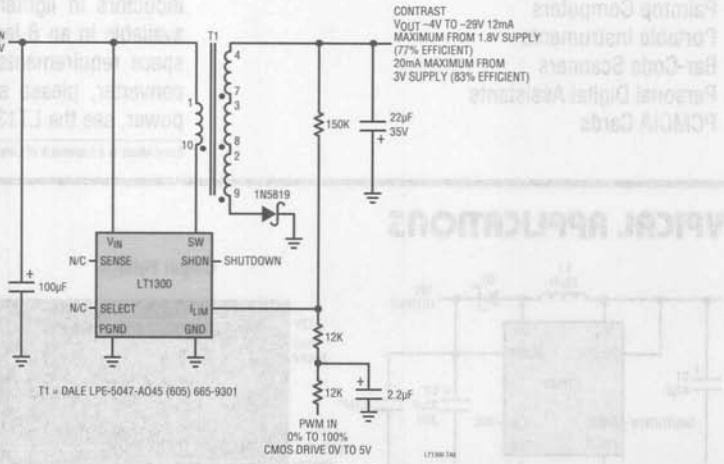
Four-Cell to 5V/3.3V Up-Down Converter



Step-Up Converter with Automatic Output Disconnect



LCD Contrast Supply



Micropower High Efficiency 5V/12V Step-Up DC/DC Converter for Flash Memory

FEATURES

- **12V at 120mA from 5V or 3.3V Supply**
- Supply Voltage as Low as 1.8V
- Better Than CMOS
- Up to 89% Efficiency
- **120μA Quiescent Current**
- Shutdown to 10μA
- Programmable 5V or 12V Output
- Low V_{CESAT} Switch: 170mV at 1A Typical
- I_{LIM} Pin Programs Peak Switch Current
- Uses Inexpensive Surface Mount Inductors
- 8-Lead DIP or SOIC Package

APPLICATIONS

- Flash Memory V_{PP} Generator
- Palmtop Computers
- Portable Instruments
- Bar-Code Scanners
- Personal Digital Assistants
- PCMCIA Cards

DESCRIPTION

The LT1301 is a micropower step-up DC/DC converter that utilizes Burst Mode™ operation. The device can deliver 5V or 12V from a two-cell battery input. It features programmable 5V or 12V output via a logic-controlled input, no-load quiescent current of 120μA and a shutdown pin which reduces supply current to 10μA. The on-chip power switch has a low 170mV saturation voltage at a switch current of 1A, a four-fold reduction over prior designs. A 155kHz internal oscillator allows the use of extremely small surface mount inductors and capacitors. Operation is guaranteed at 1.8V input. This allows more energy to be extracted from the battery, increasing operating life. The I_{LIM} pin can be used for soft start or to program peak switch current with a single resistor allowing the use of even smaller inductors in lighter load applications. The LT1301 is available in an 8-lead SOIC package, minimizing board space requirements. For a selectable 3.3V/5V step-up converter, please see the LT1300. For higher output power, see the LT1302.

Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATIONS

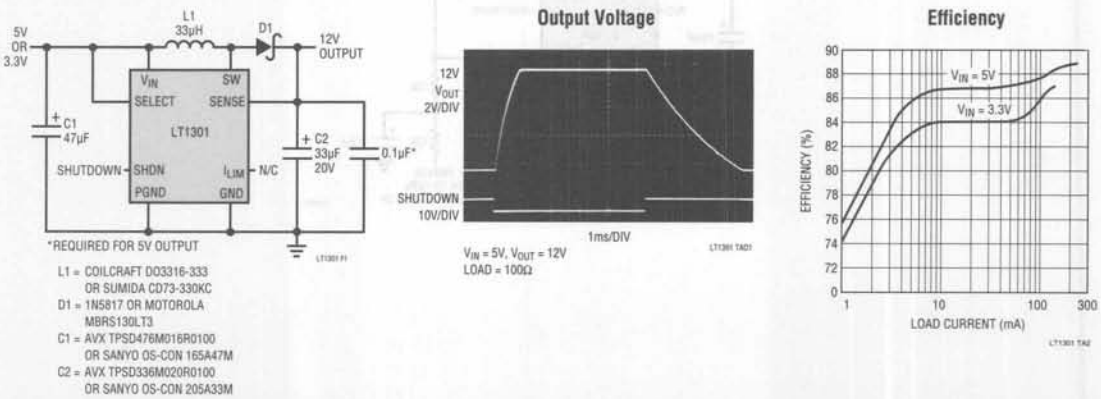
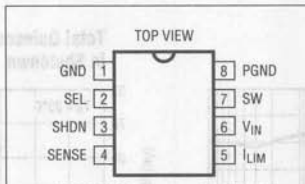


Figure 1. 3.3V/5V to 12V Step-Up Converter

ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 20V
Sense Voltage 20V
Shutdown Voltage 10V
Select Voltage 10V
I_{LIM} Voltage 0.5V
Maximum Power Dissipation 500mW
Operating Temperature Range
LT1301C ..... 0°C to 70°C
LT1301I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1301CN8 LT1301CS8 LT1301IS8
S8 PART MARKING
1301 1301I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{SEL} = 5V, V_{SENSE} = 5.5V	●		120	200	µA
		V_{SHDN} = 1.8V	●		7	15	µA
V_{IN}	Input Voltage Range			1.8			V
			●	2.0			V
V_{OUT}	Output Sense Voltage	V_{SEL} = 5V	●	11.52	12.00	12.48	V
		V_{SEL} = 0V	●	4.75	5.00	5.25	V
	Output Referred Comparator Hysteresis	V_{SEL} = 5V (Note 1)	●		50	100	mV
		V_{SEL} = 0V (Note 1)	●		22	50	mV
	Oscillator Frequency	Current Limit not Asserted.		120	155	185	kHz
	Oscillator TC				0.2		%/°C
DC	Maximum Duty Cycle			75	86	95	%
t_{ON}	Switch On-Time	Current Limit not Asserted.			5.6		µs
	Output Line Regulation	1.8V < V_{IN} < 6V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 700mA	●		130	200	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Peak Switch Current (Internal Trip Point)	I_{LIM} Floating (See Typical Application)		0.75	1.0	1.25	A
		I_{LIM} Grounded			0.4		A
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low					0.5	V
V_{SELH}	Select Pin High		●	1.5			V
V_{SELL}	Select Pin Low		●			0.8	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8	20	µA
		V_{SHDN} = 2V	●		3		µA
		V_{SHDN} = 0V	●		0.1	1	µA
I_{SEL}	Select Pin Bias Current	0V < V_{SEL} < 5V	●		1	3	µA

The ● denotes specifications which apply over the 0°C to 70°C temperature range.

Note 1: Hysteresis specified is DC. Output ripple may be higher if output capacitance is insufficient or capacitor ESR is excessive. See operation section.

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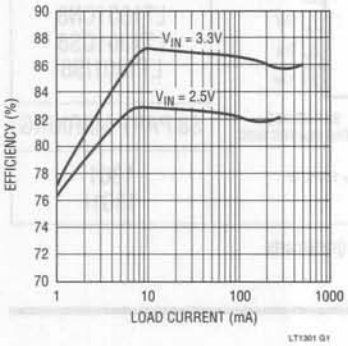
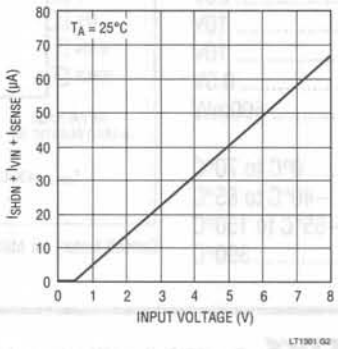
TYPICAL PERFORMANCE CHARACTERISTICS

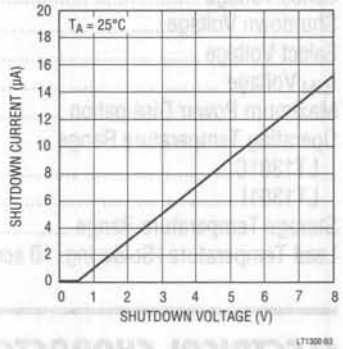
5V Output Efficiency



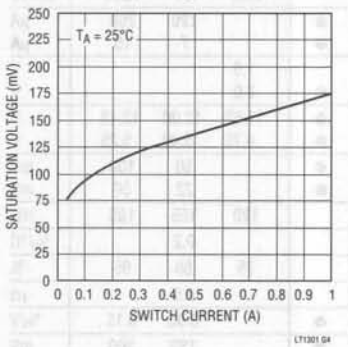
Total Quiescent Current in Shutdown



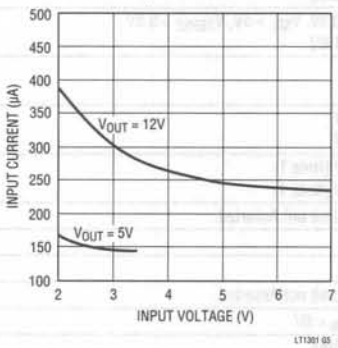
Shutdown Pin Bias Current



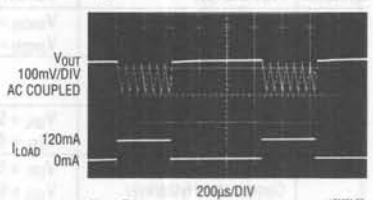
Saturation Voltage vs Switch Current



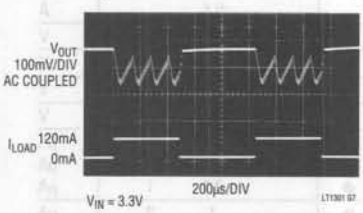
No-Load Input Current



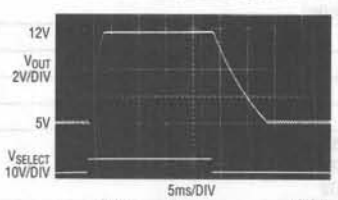
Load Transient Response of Figure 1 Circuit



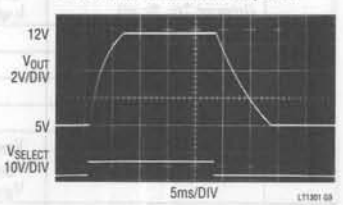
Load Transient Response of Figure 1 Circuit



Select Pin Transient Response



Select Pin Transient Response



PIN FUNCTIONS

GND (Pin 1): Signal Ground. Tie to PGND under the package.

Sel (Pin 2): Output Select. When tied to V_{IN} converter regulates at 12V. When grounded or floating converter regulates at 5V. May be driven under logic control.

SHDN (Pin 3): Shutdown. Pull high to shut down the LT1301. Ground for normal operation.

Sense (Pin 4): "Output" Pin. Goes to internal resistive divider. If operating at 5V output, a 0.1µF ceramic capacitor is required from Sense to Ground.

I_{LIM} (Pin 5): Float for 1A switch current limit. Tie to ground for approximately 400mA. A resistor between I_{LIM} and ground sets peak current to some intermediate value .

V_{IN} (Pin 6): Supply Pin. Must be bypassed with a large value electrolytic to ground. Keep bypass within 0.2" of the device.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct to minimize radio frequency interference.

PGND (Pin 8): Power Ground. Tie to signal ground (pin 1) under the package. Bypass capacitor from V_{IN} should be tied directly to PGND within 0.2" of the device.

BLOCK DIAGRAM

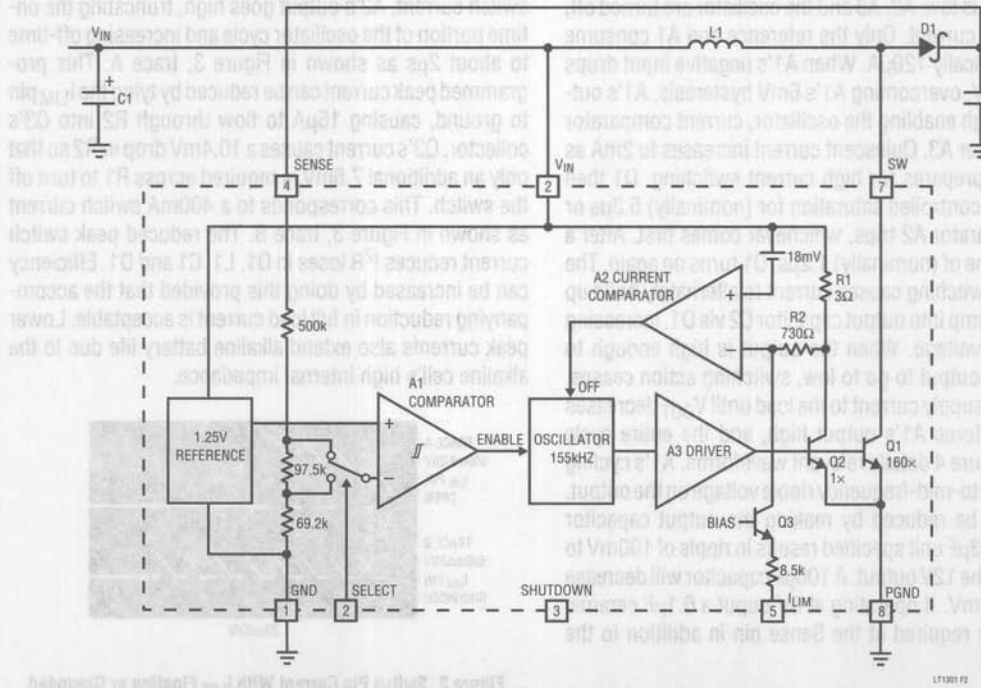
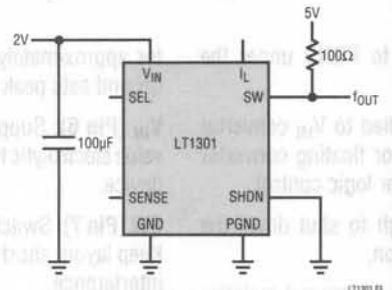


Figure 2.

TEST CIRCUIT



Oscillator Test Circuit

OPERATION

Operation of the LT1301 is best understood by referring to the Block Diagram in Figure 2. When A1's negative input, related to the Sense pin voltage by the appropriate resistor-divider ratio is higher that the 1.25V reference voltage, A1's output is low. A2, A3 and the oscillator are turned off, drawing no current. Only the reference and A1 consume current, typically 120µA. When A1's negative input drops below 1.25V, overcoming A1's 6mV hysteresis, A1's output goes high enabling the oscillator, current comparator A2, and driver A3. Quiescent current increases to 2mA as the device prepares for high current switching. Q1 then turns on in controlled saturation for (nominally) 5.3µs or until comparator A2 trips, whichever comes first. After a fixed off-time of (nominally) 1.2µs, Q1 turns on again. The LT1301's switching causes current to alternately build up in L1 and dump into output capacitor C2 via D1, increasing the output voltage. When the output is high enough to cause A1's output to go to low, switching action ceases. C2 is left to supply current to the load until V_{OUT} decreases enough to force A1's output high, and the entire cycle repeats. Figure 4 details relevant waveforms. A1's cycling causes low-to-mid-frequency ripple voltage on the output. Ripple can be reduced by making the output capacitor large. The 33µF unit specified results in ripple of 100mV to 200mV on the 12V output. A 100µF capacitor will decrease ripple to 50mV. If operating at 5V ouput a 0.1µF ceramic capacitor is required at the Sense pin in addition to the electrolytic.

If switch current reaches 1A, causing A2 to trip, switch on-time is reduced and off-time increases slightly. This allows continuous mode operation during bursts. A2 monitors the voltage across 3Ω resistor R1 which is directly related to the switch current. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 18mV, corresponding to 1A switch current, A2's output goes high, truncating the on-time portion of the oscillator cycle and increasing off-time to about 2µs as shown in Figure 3, trace A. This programmed peak current can be reduced by tying the I_{LIM} pin to ground, causing 15µA to flow through R2 into Q3's collector. Q3's current causes a 10.4mV drop in R2 so that only an additional 7.6mV is required across R1 to turn off the switch. This corresponds to a 400mA switch current as shown in Figure 3, trace B. The reduced peak switch current reduces I^2R loses in Q1, L1, C1 and D1. Efficiency can be increased by doing this provided that the accompanying reduction in full load current is acceptable. Lower peak currents also extend alkaline battery life due to the alkaline cell's high internal impedance.

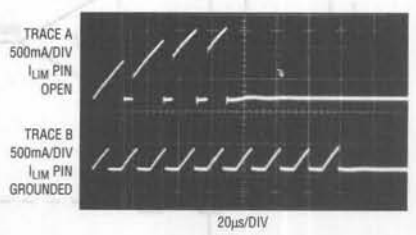
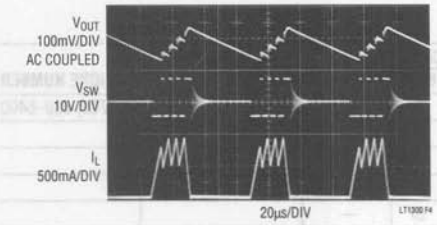


Figure 3. Switch Pin Current With I_{LIM} Floating or Grounded

APPLICATIONS INFORMATION



V_{IN} = 5V, V_{OUT} = 12V, L = 33µH
C_{OUT} = 33µF, I_{LOAD} = 90mA

Figure 4. Burst Mode Operation in Action

Output Voltage Selection

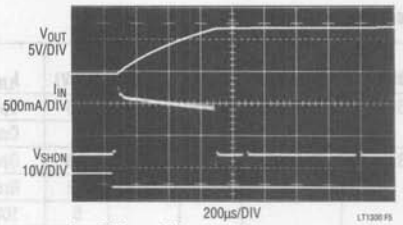
The LT1301 can be selected to 5V or 12V under logic control or fixed at either by tying Select to ground or V_{IN} respectively. It is permissible to tie Select to a voltage higher than V_{IN} as long as it does not exceed 10V. Efficiency in 5V mode will be slightly less that in 12V mode due to the fact that the diode drop is a greater percentage of 5V than 12V. Since the bipolar switch in the LT1301 gets its base drive from V_{IN}, no reduction in switch efficiency occurs when in 5V mode. When V_{IN} exceeds the programmed output voltage the output will follow the input. This is characteristic of the simple step-up or "boost" converter topology. A circuit example that provides a regulated output with an input voltage above or below the output (known as a buck-boost or SEPIC) is shown in the Typical Applications section.

Shutdown

The converter can be turned off by pulling SHDN (pin 3) high. Quiescent current drops to 10µA in this condition. Bias current of 8µA to 10µA flows into the pin (at 5V input). It is recommended that SHDN not be left floating. Tie the pin to ground if the feature is not used. SHDN can be driven high even if V_{IN} is floating.

I_{LIM} Function

The LT1301's current limit (I_{LIM}) pin can be used for soft start. Upon start-up, the LT1301 will draw maximum current from the supply (about 1A) from the supply to charge the output capacitor. Figure 5 shows V_{OUT} and I_{IN} waveforms as the device is turned on. The high current flow can create IR drops along supply and ground lines or cause the input supply to drop out momentarily. By



V_{IN} = 5V, V_{OUT} = 12V

Figure 5. Start-Up Response

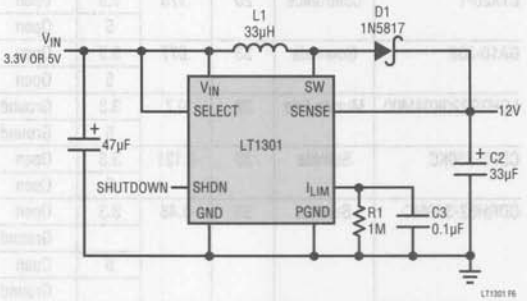
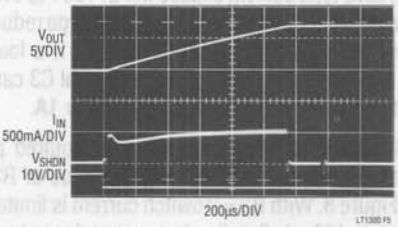


Figure 6.



V_{IN} = 5V, V_{OUT} = 12V

Figure 7. Startup Response Soft-Start Circuitry Added

adding R1 and C3 as shown in Figure 6, the switch current in the LT1301 is initially limited to 400mA until the 15µA flowing out of the I_{LIM} pin charges up C3. Input current is held to under 500mA while the output voltage ramps up to 12V as shown in Figure 7. R1 provides a discharge path for the capacitor without appreciably decreasing peak switch current. When using the I_{LIM} pin soft-start mode a minimum load of a few hundred microamperes is recommended to prevent C3 from discharging, as no current flows out of I_{LIM} when the LT1301 is not

APPLICATIONS INFORMATION

Table 1. Recommended Inductors

PART NUMBER	VENDOR	L (μH)	DCR (Ω)	V_{IN}(V)	I_{LIM} PIN	EFFICIENCY (%) 30mA	60mA	120mA	COMPONENT HEIGHT (mm)	PHONE NUMBER
DO3316-333	Coilcraft	33	0.088	3.3	Open	84	84	85	5.5	(708) 639-6400
				5	Open	89	89	90		
DO1608-223	Coilcraft	22	.31	3.3	Open	82	82	—	3.5	
				3.3	Ground	85	—	—		
				5	10k	86	87	—		
				5	Ground	88	—	—		
DO1608-103	Coilcraft	10	.11	2	Open	78	—	—	3.5	
CTX20-1	Coiltronics	20	.175	3.3	Open	84	84	—	4.2	(407) 241-7876
				5	Open	88	88	89		
GA10-332	Gowanda	33	.077	3.3	Open	86	86	87	Through-Hole	(716) 532-2234
				5	Open	89	89	90		
LQH3G220K04M00	Murata-Erie	22	0.7	3.3	Ground	81	—	—	2.0	(404) 436-1300
				5	Ground	85	—	—		
CD73-330KC	Sumida	33	0.131	3.3	Open	84	85	86	3.5	(708) 956-0666
				5	Open	88	88	89		
CDRH62-330MC	Sumida	33	0.48	3.3	Open	80	80	81	3.0	
					Ground	85	—	—		
				5	Open	84	84	85		
					Ground	83	—	—		

switching. Zero load current causes the LT1301 to switch so infrequently that C3 can completely discharge reducing subsequent peak switch current to 400mA. If a load is suddenly applied, output voltage will sag until C3 can be recharged and peak switch current returns to 1A.

If the full capacity of the LT1301 is not required peak current can be reduced by changing the value of R3 as shown in Figure 8. With R3 = 0 switch current is limited to approximately 400mA. Smaller, less expensive inductors with lower saturation ratings can then be used.

Inductor Selection

For full output power, the inductor should have a saturation current rating of 1.25A for worst-case current limit, although it is acceptable to bias an inductor 20% or more into saturation. Smaller inductors can be used in conjunction with the I_{LIM} pin. Efficiency is significantly affected by inductor DCR. For best efficiency limit the DCR to 0.03Ω or less. Toroidal types are preferred in some cases due to their inherent flux containment and EMI/RFI superiority. Recommended inductors are listed in Table 1.

Table 2. Recommended Capacitors

VENDOR	SERIES	TYPE	PHONE#
AVX	TPS	Surface Mount	(803)448-9411
Sanyo	OS-CON	Through-Hole	(619) 661-6835
Panasonic	HFQ	Through-Hole	(201) 348-5200

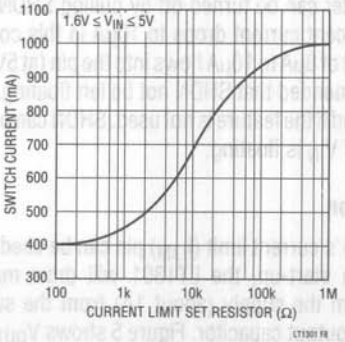


Figure 8. Peak Switch Current vs. Current Limit Set Resistor

APPLICATIONS INFORMATION

Capacitor Selection

Low ESR capacitors are required for both input and output of the LT1301. ESR directly affects ripple voltage and efficiency. For surface mount applications AVX TPS series tantalum capacitors are recommended. These have been specially designed for SMPS and have low ESR along with high surge current ratings. For through-hole applications Sanyo OS-CON capacitors offer extremely low ESR in a small size. Again, if peak switch current is reduced using the I_{LIM} pin, capacitor requirements can be relaxed and smaller, higher ESR units can be used. Suggested capacitor sources are listed in Table 2.

Diode Selection

Best performance is obtained with a Schottky rectifier diode such as the 1N5817. Phillips Components makes this in surface mount as the PRLL5817. Motorola makes the MBRS130LT3 which is slightly better and also in surface mount. For lower output power a 1N4148 can be used although efficiency will suffer substantially.

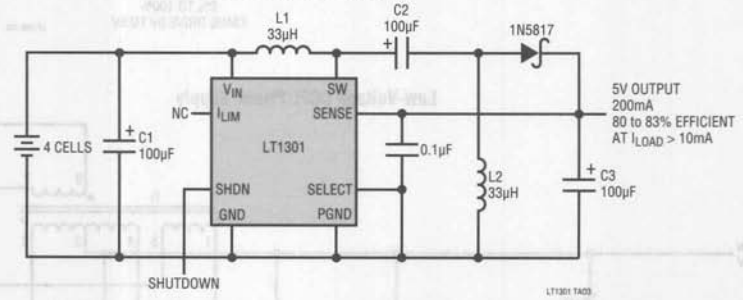
Layout Considerations

The LT1301 is a high speed, high current device. The input capacitor must be no more than 0.2″ from V_{IN} (pin 6) and ground. Connect the PGND and GND (pins 8 and 1) together under the package. Place the inductor adjacent to SW (pin 7) and make the switch pin trace as short as possible. This keeps radiated noise to a minimum.

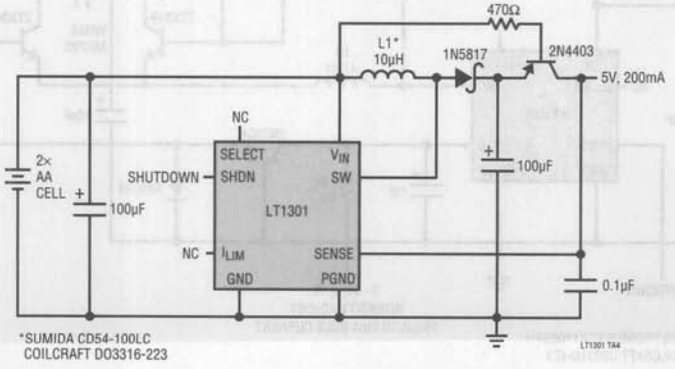
TYPICAL APPLICATIONS

4

Four-Cell to 5V Converter



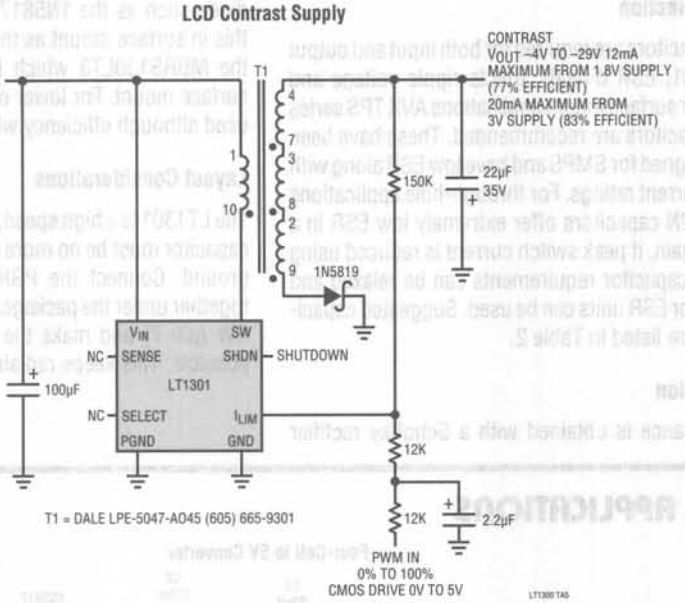
Step-Up Converter with Automatic Output Disconnect



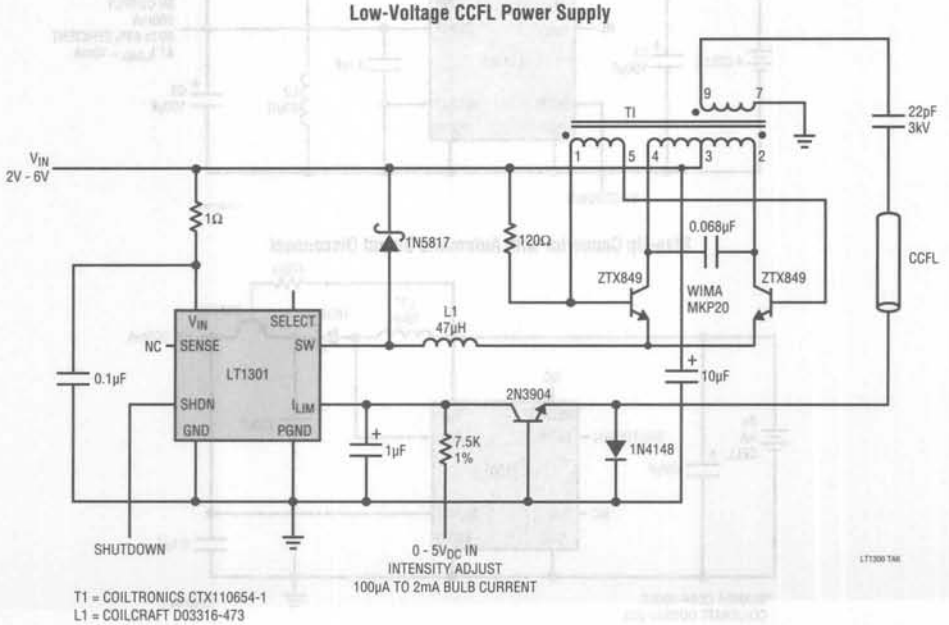
*SUMIDA CD54-100LC
COILCRAFT DO3316-223

TYPICAL APPLICATIONS

LCD Contrast Supply

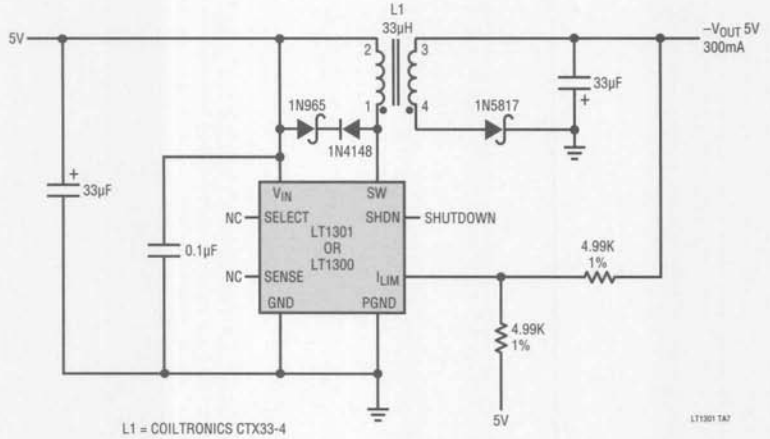


Low-Voltage CCFL Power Supply



TYPICAL APPLICATIONS

5V to –5V Converter



L1 = COILTRONICS CTX33-4

4

NOTES

SECTION 4—POWER PRODUCTS

PCMCIA HOST AND CARD POWER MANAGEMENT DEVICES

LT1106, Micropower Step-Up DC/DC Converter for PCMCIA Card Flash Memory 13-3
LTC1262, 12V, 30mA Flash Memory Programming Supply 13-35
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SECTION 5—INTERFACE

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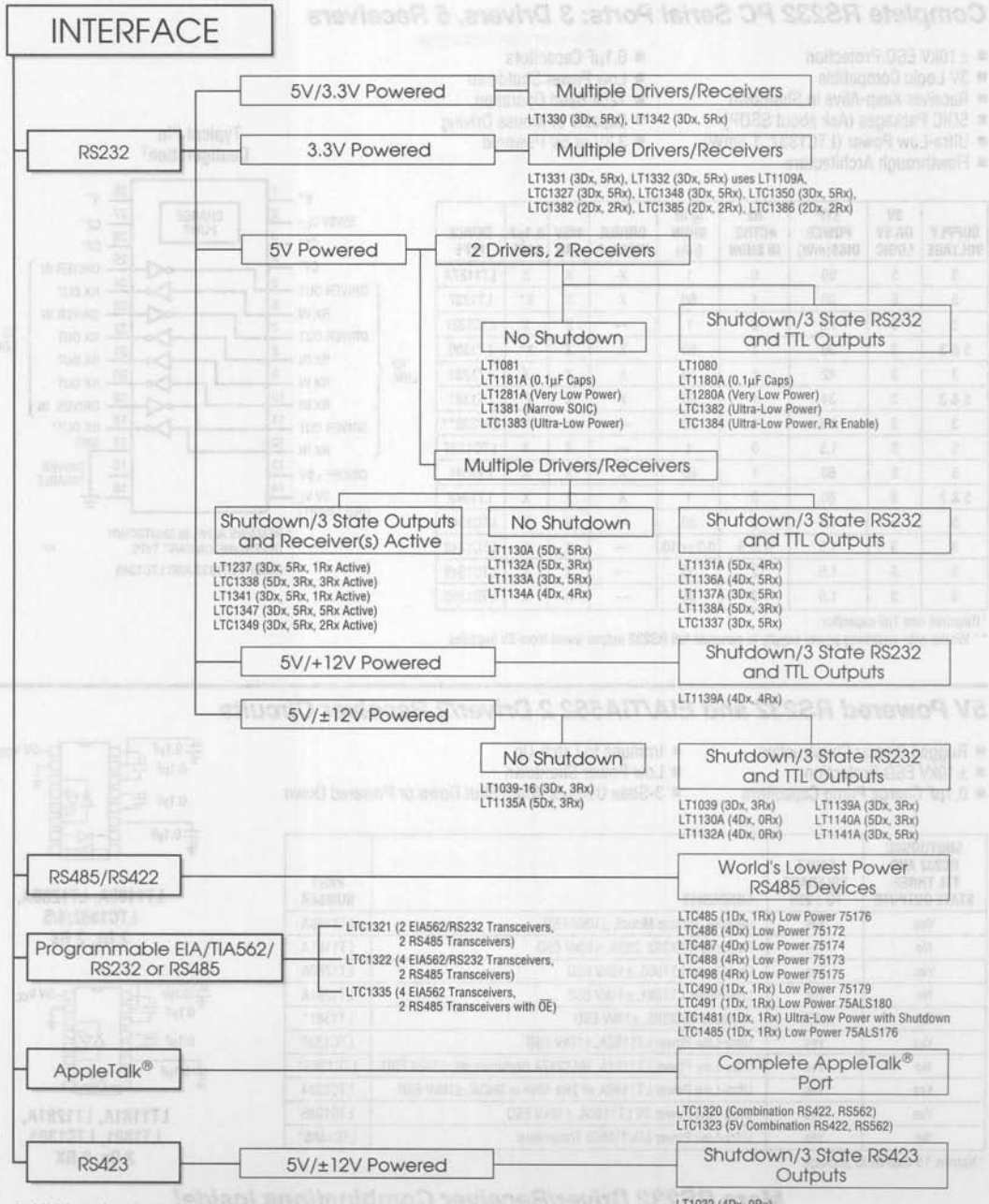
INTERFACE



AppleTalk is a registered trademark of Apple Computer, Inc.

5

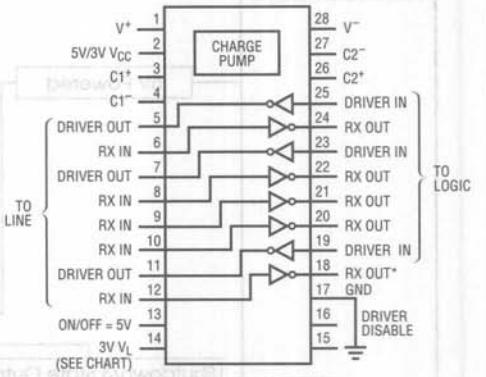
Complete RS232 PC Serial Ports: 3 Drivers, 5 Receivers

- ±10kV ESD Protection
- 3V Logic Compatible
- Receiver Keep-Alive in Shutdown
- SOIC Packages (Ask about SSOP)
- Ultra-Low Power (LTC1337: 1.5mW)
- Flowthrough Architecture
- 0.1µF Capacitors
- Low Power Shutdown
- 120k Baud Operation
- Capable of Mouse Driving
- 3.3V or 5V Powered

SUPPLY VOLTAGE	3V OR 5V LOGIC	TYP POWER DISS(mW)	Rx ACTIVE IN SHDN	I_Q IN SHDN (µA)	DRIVER DISABLE	10kV ESD	0.1µF CAPS	DEVICE TYPE
5	5	60	0	1	X	X	X	LT1137A
5	5	30	1	60	X	X	X*	LT1237
3	3	1.5	0	1	—	X	X	LTC1327
5 & 3	3	30	1	60	X	X	X*	LT1330
3	3	42	1	60	X	X	X	LT1331
5 & 3	3	34	1	60	X	X	X*	LT1331
3	3	1.5	1	70	—	X	X	LT1332**
5	5	1.5	0	1	—	X	X	LTC1337
5	5	60	1	60	X	X	X	LT1341
5 & 3	3	60	0	1	X	X	X	LT1342
5	5	1.5	5	80	—	X	X	LTC1347
3	3	1.5	0 or 5	0.2 or 10	—	X	X	LTC1348
5	5	1.5	2	35	—	X	X	LTC1349
3	3	1.5	2	35	—	X	X	LTC1350

*Requires one 1µF capacitor
** Works with switching power supply to generate full RS232 output levels from 3V supplies

Typical Pin Configuration†



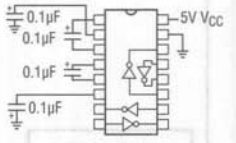
* REMAINS ALIVE IN SHUTDOWN DEPENDING ON PART TYPE
† EXCEPT LT1332 AND LTC1348

5V Powered RS232 and EIA/TIA562 2 Driver/2 Receiver Circuits

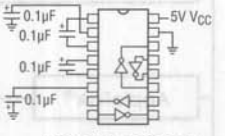
- Rugged Bipolar Construction
- ±10kV ESD Protection
- 0.1µF Charge Pump Capacitors
- Immune to Latch-Up
- Low Power Shutdown
- 3-State Outputs When Shut Down or Powered Down

SHUTDOWN/ RS232 AND TTL THREE-STATE OUTPUTS	FAULT TOLERANT TO ±25V	COMMENTS	PART NUMBER
Yes	Yes	Ideal for Surface Mount, ±10kV ESD	LT1180A
No	Yes	Replaces MAX202, 232A, ±10kV ESD	LT1181A
Yes	Yes	Low Power LT1080, ±10kV ESD	LT1280A
No	Yes	Low Power LT1081, ±10kV ESD	LT1281A
No	±15V	Replaces MAX202, ±10kV ESD	LT1381*
Yes	Yes	Ultra-Low Power LT1180A, ±10kV ESD	LTC1382
No	Yes	Ultra-Low Power LT1181A, MAX232A Replacement, ±10kV ESD	LTC1383*
Yes	Yes	Ultra-Low Power LT1180A w/ 2Rx Alive in SHDN, ±10kV ESD	LTC1384
Yes	Yes	Ultra-Low Power 3V LT1180A, ±10kV ESD	LTC1385
No	Yes	Ultra-Low Power EIA/TIA562 Transceiver	LTC1386*

*Narrow 16-lead SOIC package



LT1180A, LT1280A, LTC1382/4/5 2 Dx, 2 Rx



LT1181A, LT1281A, LT1381, LTC1383 2 Dx, 2 RX

More RS232 Driver/Receiver Combinations Inside!

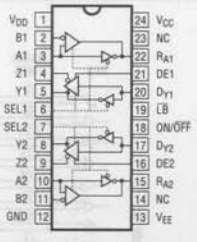
Other RS232 Driver/Receiver Combinations

DRIVERS	RECEIVERS	SUPPLIES REQUIRED	SHUTDOWN/ RS232 and TTL THREE-STATE OUTPUTS	FAULT TOLERANT to ±25V	REQ'D CHARGE PUMP CAP SIZE	COMMENTS	PART NUMBER
4	0	±12V	Yes	Yes	N/A	Low Power 1488 Upgrade	LT1030
4	0	±12V	Yes	Yes	N/A	Low Power 1488 Upgrade Also Supports RS423	LT1032
3	3	5V, ±12V	Yes	Yes	N/A	One Receiver Active in Shutdown	LT1039
3	3	5V, ±12V	No	Yes	N/A	Rugged MC145406 Replacement	LT1039-16
5	5	5V	No	Yes	0.1µF	Synchronous Communications, ±10kV ESD	LT1130A
5	4	5V	Yes	Yes	0.1µF	Synchronous Modem/DCE Interface, ±10kV ESD	LT1131A
5	3	5V	No	Yes	0.1µF	Modem/DCE Interface, ±10kV ESD	LT1132A
3	5	5V	No	Yes	0.1µF	PC/DTE Interface, ±10kV ESD	LT1133A
4	4	5V	No	Yes	0.1µF	5V Only 1488/1489 Replacement, ±10kV ESD	LT1134A
5	3	5V, ±12V	No	Yes	N/A	Modem/DCE Interface, ±10kV ESD	LT1135A
4	5	5V	Yes	Yes	0.1µF	Synchronous PC/DTE Interface, ±10kV ESD	LT1136A
5	3	5V	Yes	Yes	0.1µF	Modem/DCE Interface, ±10kV ESD	LT1138A
4	4	5V, 12V	Yes	Yes	0.1µF	1488/1489 Replacement, ±10kV ESD	LT1139A
5	3	5V, ±12V	Yes	Yes	N/A	Modem/DCE Interface, ±10kV ESD	LT1140A
3	5	5V, ±12V	Yes	Yes	N/A	PC/DTE Interface, ±10kV ESD	LT1141A
5	3	5V	Yes	Yes	0.1µF	Ultra-Low Power, 1 Receiver Keep-Alive in SHDN, ±10kV ESD	LTC1338

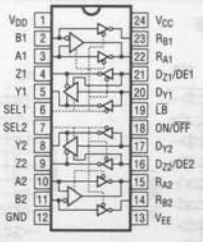
Programmable EIA/TIA562/RS232 and RS485 I/O Ports

- Low Supply Current: **1mA Typical**
- 15µA Supply Current in Shutdown
- 120k Baud in EIA/TIA562 or RS232
- 10M Baud in RS485/RS422
- Self-Testing Capability in Loopback Mode
- LTC1321/LTC1322 Have the Same Pinout as SP301/SP302
- LTC1335 Features Receiver Three-State Outputs
- Power-Up/Down Glitch-Free Outputs
- Driver Maintains High Impedance in Three-State, Shutdown, or With Power Off
- Thermal Shutdown Protection
- Protection: I/O Lines Can Withstand ±25V
- Withstands Repeated ±10kV ESD Pulses
- SOL or Dual-In-Line Packages

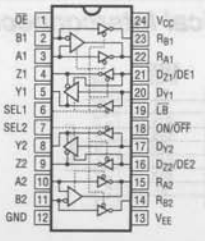
RS232 OR EIA/TIA562 TRANSCEIVERS	RS485 TRANSCEIVERS	OUTPUT LEVELS	DRIVER ENABLE	SELF TEST LOOPBACK	PART NUMBER
2	2	232/562	—	Yes	LTC1321
4	2	232/562	—	Yes	LTC1322
4	2	562	Yes	Yes	LTC1335



LTC1321
2 RS485 DRIVERS/RECEIVERS
2 EIA/TIA562 DRIVERS/RECEIVERS



LTC1322
2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA562 DRIVERS/RECEIVERS

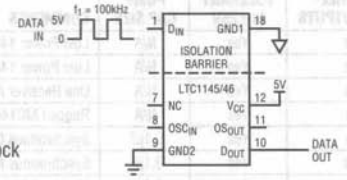


LTC1335
2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA562 DRIVERS/RECEIVERS

Low Power Digital Isolators

- UL Recognized (LTC1145A,LTC1146A) File E151738 to UL1577
- Low Input Current
  LTC1145: 700µA, LTC1146: 70µA
- Maximum Input Frequency
  LTC1145: 200kHz, LTC1146: 20kHz
- TTL Level Output
- Noise Filter Prevents Glitches at the Output
- Output Can Be Synchronized to and External Clock

Digital Isolation Interface
Data Rate Up to 200kHz



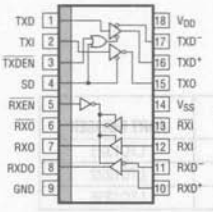
- Low Power Opto-Isolator Replacement
- Isolated Serial Data Interfaces
- Isolated Power MOSFET Drivers

ISOLATION VOLTAGE	INPUT CURRENT	MAX INPUT FREQUENCY	GLITCH-FREE OUTPUT FILTER	EXT CLOCK SYNCH	UL RECOGNIZED	PART NUMBER
2500	700µA	200kHz	Yes	Yes	✓	LTC1145A
2500	70µA	20kHz	Yes	Yes	✓	LTC1146A
500	700µA	200kHz	Yes	Yes		LTC1145
500	70µA	20kHz	Yes	Yes		LTC1146

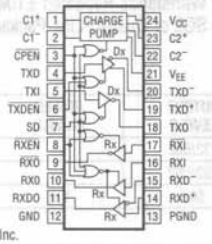
Complete AppleTalk/LocalTalk® Transceivers

- Single Chip Complete AppleTalk DCE/DTE Solutions
- Low Power
- Micropower Shutdown (LTC1320/LTC1323)
- 5V Powered (LTC1323/LTC1318)
- Surface Mount Packages
- Thermal/Short Circuit Protection

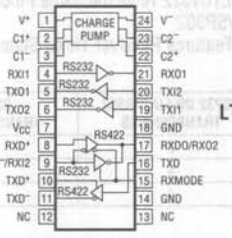
DCE/DTE	REQUIRED SUPPLIES	SUPPLY CURRENT	SHUTDOWN FUNCTION	1 RECEIVER KEEP ALIVE	SUPPLY IN SHUTDOWN	PART NUMBER
DTE	±5V	1.2mA	Yes	—	30µA	LTC1320
DTE	5V	2.4mA	Yes	Yes	65µA	LTC1323
DCE	5V	18mA	No	—	—	LTC1318



DTE LTC1320



DTE LTC1323



DCE LTC1318

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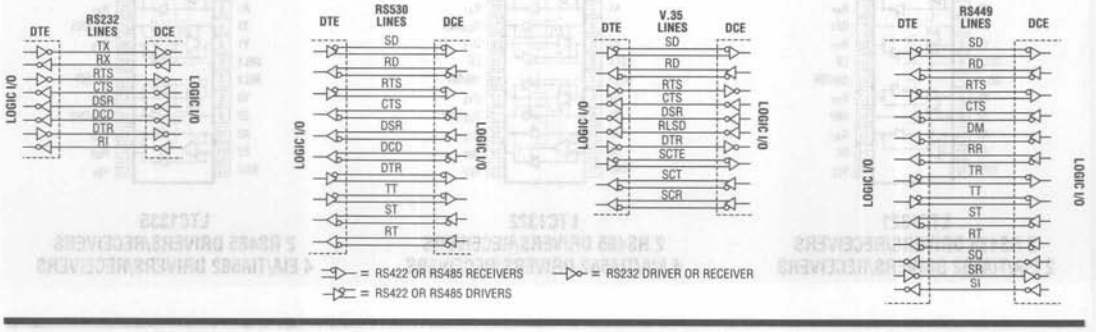
Typical Interconnection Schemes

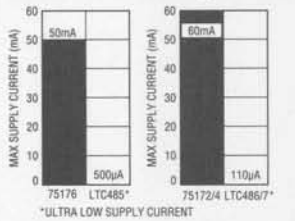


LINEAR TECHNOLOGY

RS485 Family Features

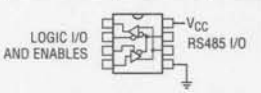
- Ultra-Low Power
- CMOS Schottky Process
- Designed for RS485 and RS422 Applications
- Three-State RS485 Outputs When Shut Down
- Power-Up/Down Glitch Free Outputs
- 10MB Operation (LTC486-489, LTC1485)
- Industry Standard Pinouts
- SOIC Available

The LTC RS485 Advantage: Low Power

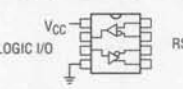


RS485/RS422 Interface

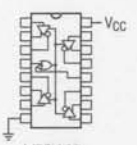
DRIVERS	RECEIVERS	SUPPLIES REQUIRED	MAX DATA RATE	MAX SUPPLY CURRENT	INDUSTRY STANDARD PINOUT	COMMENTS	PART NUMBER
1	1	5V	2.5MB	500µA	75176	Half Duplex 2-Wire RS485	LTC485
4	0	5V	10MB	150µA	75172	Good For RS449, RS530, V.35 Interface	LTC486
4	0	5V	10MB	150µA	75174	Good For RS449, RS530, V.35 Interface	LTC487
0	4	5V	10MB	10mA	75173	Good For RS449, RS530, V.35 Interface	LTC488
0	4	5V	10MB	10mA	75175	Good For RS449, RS530, V.35 Interface	LTC489
1	1	5V	2.5MB	500µA	75179	Full Duplex 4-Wire RS485	LTC490
1	1	5V	2.5MB	500µA	75ALS180	Full Duplex 4-Wire RS485	LTC491
1	1	5V	10MB	3.5mA	75ALS176B	High Speed/Half Duplex	LTC1485



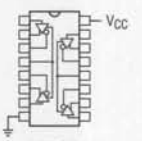
LTC485, LTC1485
1Dx, 1 Rx



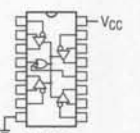
LTC490
1 Dx, 1Rx



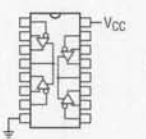
LTC486
4 Dx



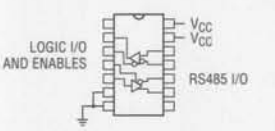
LTC487
4 Dx



LTC488
4 Rx



LTC489
4Rx



LTC491
1 Dx, 1 Rx

Interface Standards

SPECIFICATION		RS232	RS423	RS422	RS485	RS562
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential	Single-Ended
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers	1 Driver, 1 Receiver
Maximum Cable Length		50 feet*	4000 feet	4000 feet	4000 feet	50 feet*
Maximum Data Rate		20kb/s	100kb/s	10Mb/s	10Mb/s	64kb/s
Maximum Voltage Applied to Driver Output		±25V	±6V	−0.25V to 6V	−7V to 12V	±25V
Driver Output Signal	Loaded	±5V	±3.6V	±2V	±1.5V	±3.7V
	Unloaded	±15V	±6V	±5V	±5V	±13.2V
Driver Load		3kΩ to 7kΩ	450Ω (Min)	100Ω	54Ω	3kΩ to 7kΩ
Maximum Driver Output Current (High-Impedance State)	Power ON	—	—	—	—	60mA
	Power OFF	V_{MAX}/300Ω	±100µA	±100µA	±100µA	V_{MAX}/300Ω
Output Slew Rate		30V/µs (Max)	Controls Provided	—	—	30V/µs (Max)
Receiver Input Voltage Range		±15V	±12V	±7V	−7V to 12V	±25V
Receiver Input Sensitivity		±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance		3kΩ to 7kΩ	4kΩ (Min)	4kΩ (Min)	12kΩ (Min)	3kΩ to 7kΩ

*or 2500pF cable capacitance, as per EIA 232E

NOTES

SECTION 5—INTERFACE

RS232/562

LT1130A/LT1140A Series, Advanced Low Power 5V RS232 Drivers/Receivers with Small Capacitors 5-10
LT1137A, Advanced Low Power 5V RS232 Transceiver with Small Capacitors 5-20
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LTC1347, 5V Low Power RS232 3-Driver/5-Receiver Transceiver with 5 Receivers Active in SHUTDOWN 5-102
LTC1348, 3.3V Low Power RS232 3-Driver/5-Receiver Transceiver 13-116
LTC1349, 5V Low Power RS232 3-Driver/5-Receiver Transceiver with 2 Receivers Active in SHUTDOWN 5-108
LTC1350, 3.3V Low Power EIA/TIA-562 3-Driver/5-Receiver Transceiver 5-114
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LTC1383, 5V Low Power RS232 Transceiver 5-133
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LTC1385, 3.3V Low Power EIA/TIA-562 Transceiver 5-145
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Advanced Low Power 5V RS232 Drivers/Receivers with Small Capacitors

FEATURES

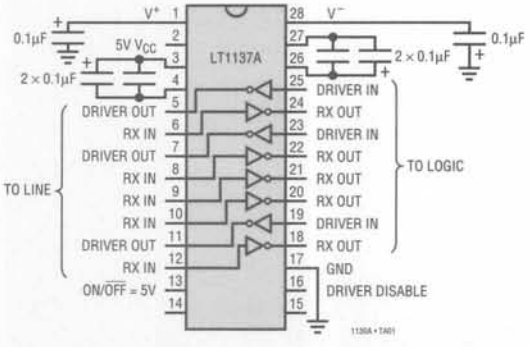
- ESD Protection over ±**10kV**
- Uses Small Capacitors: 0.1µF, 0.2µF
- 1µA Supply Current in SHUTDOWN
- Operates to 120k Baud
- CMOS Comparable Low Power
- Operates from a Single 5V Supply
- Easy PC Layout: Flowthrough Architecture
- Rugged Bipolar Design: Absolutely No Latch-Up
- Outputs Assume a High Impedance State When Off or Powered Down
- Improved Protection: RS232 I/O Lines Can be Forced to ±30V Without Damage
- Output Overvoltage Does Not Force Current Back Into Supplies
- Available in SO and SSOP Packages

DESCRIPTION

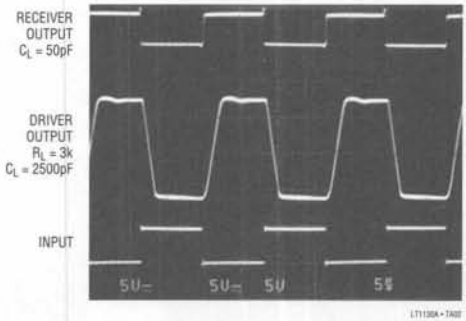
The LT1130A/LT1140A series of RS232 drivers/receivers features special bipolar construction techniques which protect the drivers and receivers beyond the fault conditions stipulated for RS232. Driver outputs and receiver inputs can be shorted to ±30V without damaging the device or the power supply generator. In addition, the RS232 I/O pins are resilient to multiple ±10kV ESD strikes. An advanced driver output stage operates up to 120kBaud while driving heavy capacitive loads. Supply current is typically 12mA, competitive with CMOS devices.

Several members of the series include flexible operating mode controls. The Driver Disable pin disables the drivers and the charge pump, the ON/$\overline{OFF}$ pin shuts down all circuitry. While shut down, the drivers and receivers assume high impedance output states.

Basic Operation



Output Waveforms



LT1130A 5-Driver/5-Receiver RS232 Transceiver
LT1131A 5-Driver/4-Receiver RS232 Transceiver w/Shutdown
LT1132A 5-Driver/3-Receiver RS232 Transceiver
LT1133A 3-Driver/5-Receiver RS232 Transceiver
LT1134A 4-Driver/4-Receiver RS232 Transceiver
LT1135A 5-Driver/3-Receiver RS232 Transceiver w/o Charge Pump
LT1136A 4-Driver/5-Receiver RS232 Transceiver w/Shutdown
LT1137A 3-Driver/5-Receiver RS232 Transceiver w/Shutdown
LT1138A 5-Driver/3-Receiver RS232 Transceiver w/Shutdown
LT1139A 4-Driver/4-Receiver RS232 Transceiver w/Shutdown
LT1140A 5-Driver/3-Receiver RS232 Transceiver w/o Charge Pump
LT1141A 3-Driver/5-Receiver RS232 Transceiver w/o Charge Pump

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- (Note 7) ..... −13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  On/Off Pin ..... −0.3V to 12V
  Driver Disable Pin ..... −0.3V to V_{CC} + 0.3V
Output Voltage
  Driver ..... −30V to 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V

Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT113XAC/LT114XAC ..... 0°C to 70°C
  LT113XAI/LT114XAI ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRODUCT SELECTION TABLE

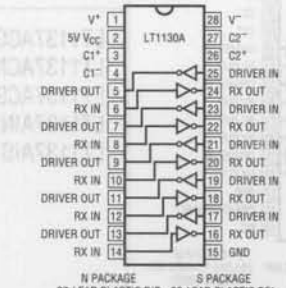
Part Number	Power Supply Voltages*	Shutdown	Driver Disable	Drivers	Receivers	External Components
LT1130A	5	No	No	5	5	4 Capacitors
LT1131A	5	Yes	Yes	5	4	4 Capacitors
LT1132A	5	No	No	5	3	4 Capacitors
LT1133A	5	No	No	3	5	4 Capacitors
LT1134A	5	No	No	4	4	4 Capacitors
LT1135A	5, 12, −12	No	No	5	3	None
LT1136A	5	Yes	Yes	4	5	4 Capacitors
LT1137A	5	Yes	Yes	3	5	4 Capacitors
LT1138A	5	Yes	Yes	5	3	4 Capacitors
LT1139A	5, 12	Yes	No	4	4	2 Capacitors
LT1140A	5, 12, −12	Yes	Yes	5	3	None
LT1141A	5, 12, −12	Yes	Yes	3	5	None

*The LT1130A, LT1131A, LT1132A, LT1134A, LT1136A, LT1137A and LT1138A can operate with 5V and 12V supplies and two external capacitors.

PACKAGE/ORDER INFORMATION

5-DRIVER/5-RECEIVER

TOP VIEW



N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)
S PACKAGE 28-LEAD PLASTIC SOL (.300" WIDE)

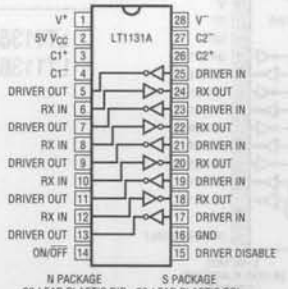
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (S)

ORDER PART NUMBER

LT1130ACN
LT1130ACS

5-DRIVER/4-RECEIVER WITH SHUTDOWN

TOP VIEW



N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)
S PACKAGE 28-LEAD PLASTIC SOL (.300" WIDE)

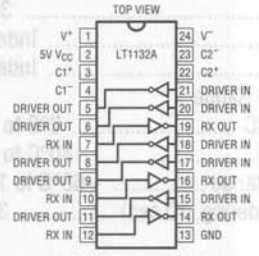
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (S)

ORDER PART NUMBER

LT1131ACN
LT1131ACS

PACKAGE/ORDER INFORMATION

5-DRIVER/3-RECEIVER



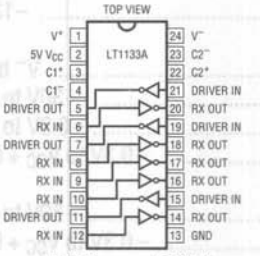
N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1132ACN
LT1132ACS

3-DRIVER/5-RECEIVER



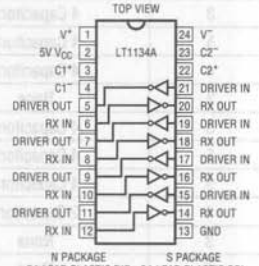
N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1133ACN
LT1133ACS

4-DRIVER/4-RECEIVER



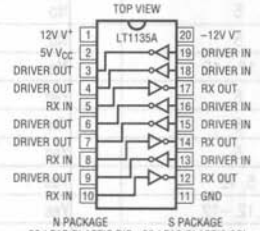
N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1134ACN
LT1134ACS
LT1134AIN
LT1134AIS

5-DRIVER/3-RECEIVER WITHOUT CHARGE PUMP



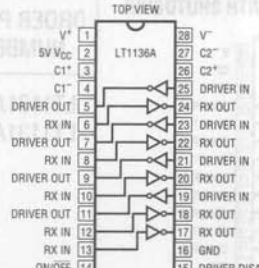
N PACKAGE 20-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 20-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 79°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER

LT1135ACN
LT1135ACS

4-DRIVER/5-RECEIVER WITH SHUTDOWN



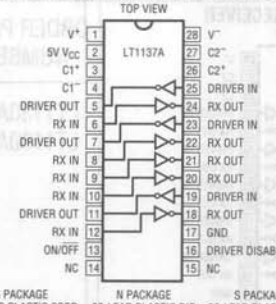
N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)
S PACKAGE 28-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (S)

ORDER PART NUMBER

LT1136ACN
LT1136ACS

3-DRIVER/5-RECEIVER WITH SHUTDOWN



G PACKAGE 28-LEAD PLASTIC SSOP (.300" WIDE)
N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)
S PACKAGE 28-LEAD PLASTIC SOL (.300" WIDE)

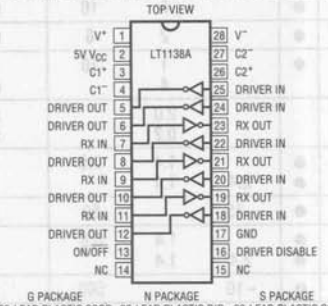
T_{JMAX} = 150°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (S)

ORDER PART NUMBER

LT1137ACG
LT1137ACN
LT1137ACS
LT1137AIN
LT1137AIS

PACKAGE/ORDER INFORMATION

5-DRIVER/3-RECEIVER WITH SHUTDOWN



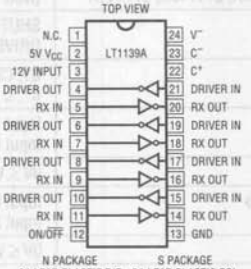
G PACKAGE 28-LEAD PLASTIC SSOP (.300" WIDE)
N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)
S PACKAGE 28-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (S)

ORDER PART NUMBER

LT1138ACG
LT1138ACN
LT1138ACS

4-DRIVER/4-RECEIVER WITH SHUTDOWN WITH 12V AND 5V SUPPLIES



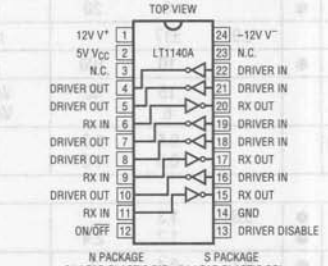
N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1139ACN
LT1139ACS

5-DRIVER/3-RECEIVER WITH SHUTDOWN WITHOUT CHARGE PUMP



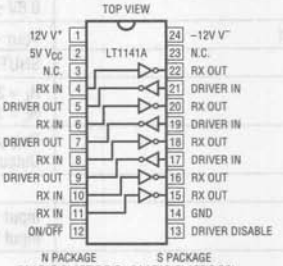
N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1140ACN
LT1140ACS

3-DRIVER/5-RECEIVER WITH SHUTDOWN WITHOUT CHARGE PUMP



N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)
S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)

T_{JMAX} = 150°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (S)

ORDER PART NUMBER

LT1141ACN
LT1141ACS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				8.6		V
V^- Output				−7.8		V
5V V_{CC} Supply Current: LT1130A, LT1131A, LT1132A, LT1133A, LT1134A, LT1136A, LT1138A	(Note 3)	●		15	25	mA
5V V_{CC} Supply Current: LT1135A, LT1140A, LT1141A	(Note 3), V^+ = 12V, V^- = −12V	●		8	15	mA
5V V_{CC} Supply Current: LT1137A	(Note 3)	●		12	17	mA
5V V_{CC} Supply Current: LT1139A	(Note 3), V^+ = 12V	●		8	15	mA
12V V^+ Supply Current: LT1135A, LT1140A, LT1141A	(Note 3), V^- = −12V	●		1	4	mA

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
12V V^+ Supply Current: LT1139A	(Note 3)	●		6	10	mA
−12V V^- Supply Current: LT1135A, LT1140A, LT1141A	(Note 3) V^+ = 12V	●		2	6	mA
Supply Current when OFF (V_{CC})	SHUTDOWN (Note 4) DRIVER DISABLE	●		1 4	10	µA mA
Supply Rise Time SHUTDOWN to Turn-On	C1, C2, C^+, C^- = 1.0µF C^+, C^- = 0.1µF, C1, C2 = 0.2µF			2.0 0.2		ms ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN) Input High Level (Device Enabled)	● ●	 2.4	1.4 1.4	0.8	V V
ON/$\overline{OFF}$ Pin Current	$0V \le V_{ON/OFF} \le 5V$	●	−15		80	µA
DRIVER DISABLE Pin Thresholds	Input Low Level (Drivers Enabled) Input High Level (Drivers Disabled)	● ●	 2.4	1.4 1.4	0.8	V V
DRIVER DISABLE Pin Current	$0V \le V_{DRIVER\ DISABLE} \le 5V$	●	−10		500	µA
Oscillator Frequency				130		kHz
Any Driver						
Output Voltage Swing	Load = 3k to GND Positive Negative	● ●	5	7.3 −6.5	 −5	V V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)	● ●	 2	1.4 1.4	0.8	V V
Logic Input Current	$0.8V \le V_{IN} \le 2V$	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		±9	±17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)	●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF R_L = 3k, C_L = 2500pF			15 6	30	V/µs V/µs
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5) Output Transition t_{LH} Low-to-High			0.6 0.5	1.3 1.3	µs µs
Any Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High) Input High Threshold (V_{OUT} = Low)	● ●	0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$	●		1	10	µA
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 10	−20 20	−10	mA mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 6) Output Transition t_{LH} Low-to-High			250 350	600 600	ns ns

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade and $-40°C \le T_A \le 85°C$ for industrial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$ = 3V.

Note 3: Supply current is measured with driver and receiver outputs unloaded and the driver inputs tied high.

Note 4: Supply current and driver leakage current measurements in SHUTDOWN are performed with $V_{ON/OFF}$ = 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ = 3V.

For LT1135A, LT1139A, LT1140A and LT1141A with 12V supplies, V_{OUT} leakage is 200µA for V_{OUT} forced to ±25V.

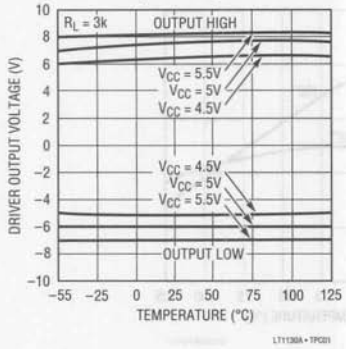
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

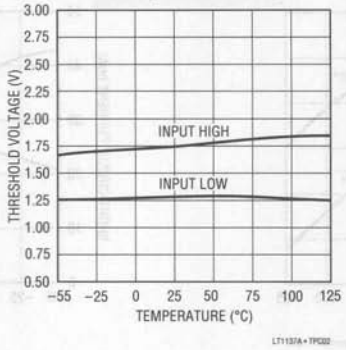
Note 7: For the LT1133A and LT1137A absolute maximum externally applied V^- = 6.5V. Internal charge pump will drive this pin to a higher negative voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

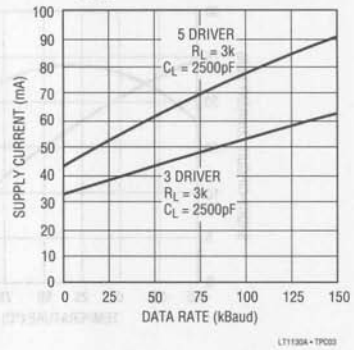
Driver Output Voltage



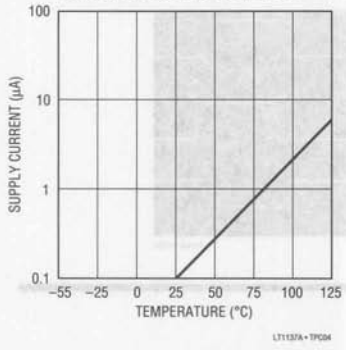
Receiver Input Thresholds



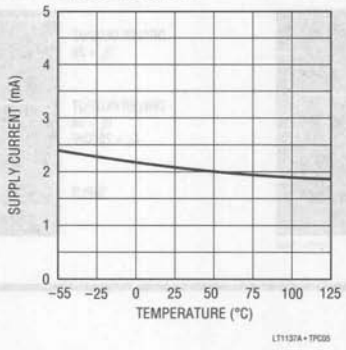
Supply Current vs Data Rate



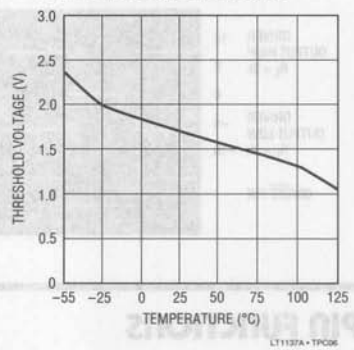
Supply Current in SHUTDOWN



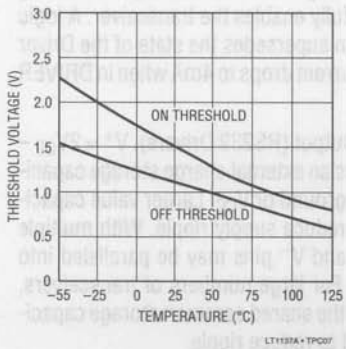
Supply Current in DRIVER DISABLE



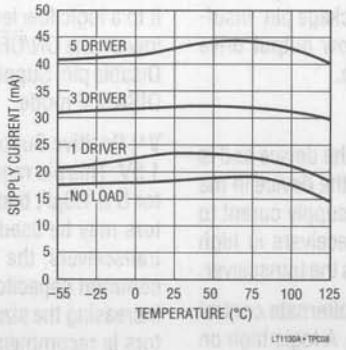
DRIVER DISABLE Threshold



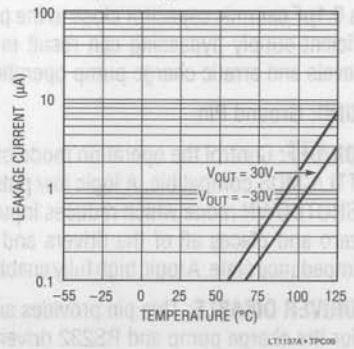
ON/$\overline{\text{OFF}}$ Thresholds



Supply Current



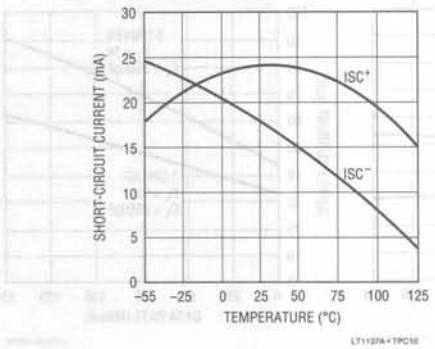
Driver Leakage in SHUTDOWN



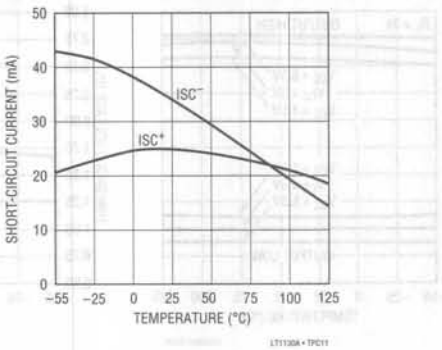
5

TYPICAL PERFORMANCE CHARACTERISTICS

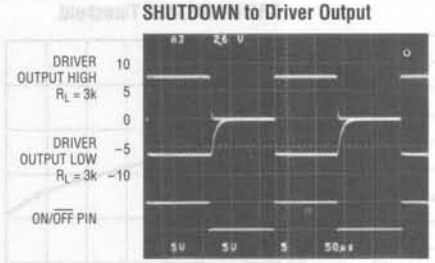
Driver Short-Circuit Current



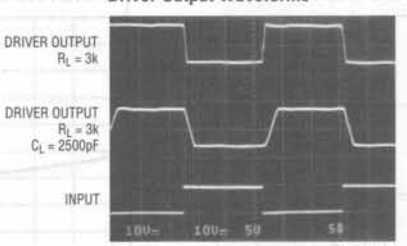
Receiver Short-Circuit Current



SHUTDOWN to Driver Output



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current drops to zero in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/$\overline{OFF}$: Control the operation mode of the device and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply curent to zero and places all of the drivers and receivers in high impedance state. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. Receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. A logic low on the ON/$\overline{OFF}$ pin supersedes the state of the Driver Disable pin. Supply current drops to 4mA when in DRIVER DISABLE mode.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 1.0\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of transceivers, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

PIN FUNCTIONS

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. V^- is short-circuit proof for 30 seconds.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance. In applications where larger positive voltages are available, such as 12V, C1 may be omitted and the positive voltage may be connected directly to the $C1^+$ pin. In this mode of operation, the V^+ pin should be decoupled with a $0.1\mu F$ ceramic capacitor.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

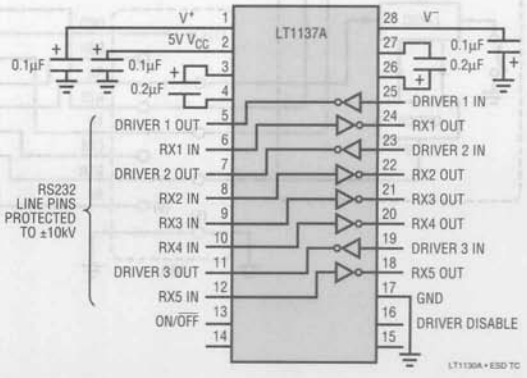
RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

5

ESD PROTECTION

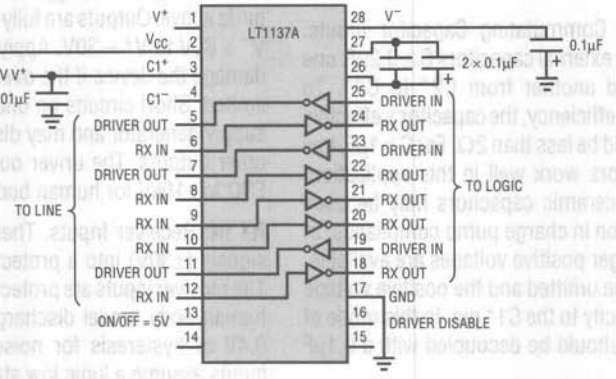
The RS232 line inputs of the LT1130A/LT1140A series of RS232 Driver/Receivers have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1130A/LT1140A must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



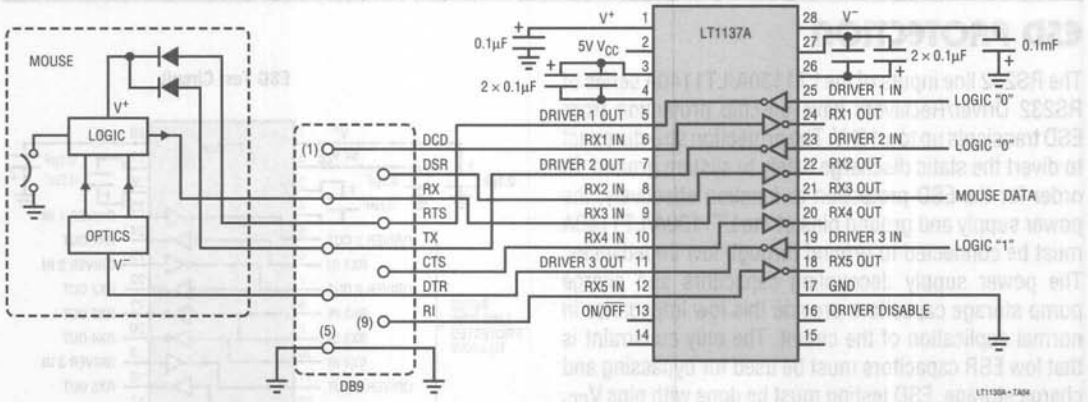
TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



LT1130A • TA03

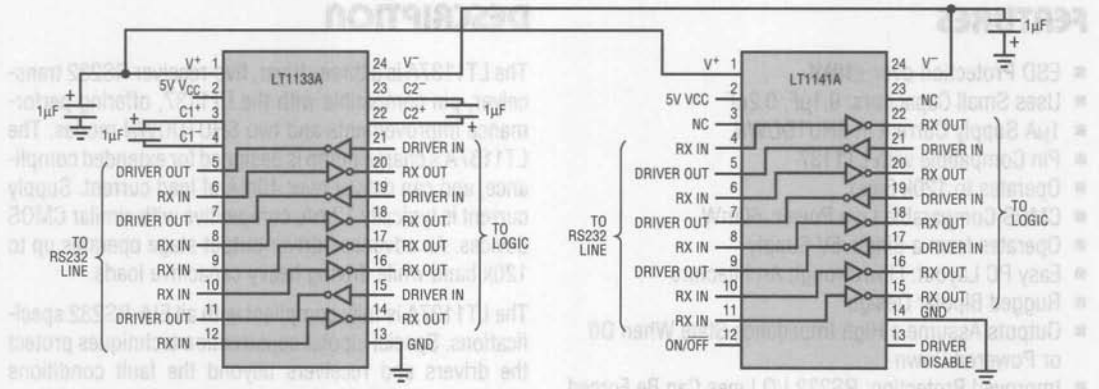
Typical Mouse Driving Application



LT1130A • TA04

TYPICAL APPLICATIONS

Sharing Power Supply Generator with a Second Transceiver



5

Advanced Low Power 5V RS232 Transceiver with Small Capacitors

FEATURES

- ESD Protection over ±**10kV**
- Uses Small Capacitors: 0.1µF, 0.2µF
- 1µA Supply Current in SHUTDOWN
- Pin Compatible with LT1137
- Operates to 120k Baud
- CMOS Comparable Low Power: 60mW
- Operates from a Single 5V Supply
- Easy PC Layout: Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Improved Protection: RS232 I/O Lines Can Be Forced to ±30V without Damage
- Output Overvoltage Does Not Force Current Back into Supplies
- Absolutely No Latch-up
- Available in SO Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

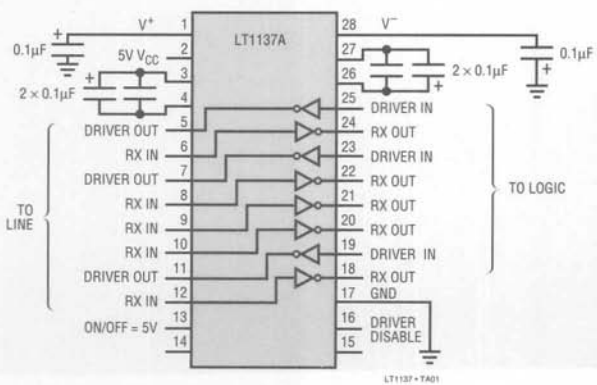
DESCRIPTION

The LT1137A is a three-driver, five-receiver RS232 transceiver, pin compatible with the LT1137, offering performance improvements and two SHUTDOWN modes. The LT1137A's charge pump is designed for extended compliance, and can deliver over 40mA of load current. Supply current is typically 12mA, competitive with similar CMOS devices. An advanced driver output stage operates up to 120k baud while driving heavy capacitive loads.

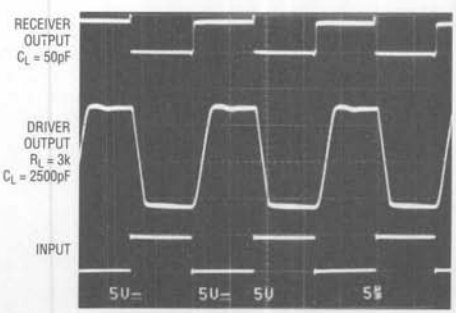
The LT1137A is fully compliant with all EIA-RS232 specifications. Special bipolar construction techniques protect the drivers and receivers beyond the fault conditions stipulated for RS232. Driver outputs and receiver inputs can be shorted to ±30V without damaging the device or the power supply generator. In addition, the RS232 I/O pins are resilient to multiple ±10kV ESD strikes.

The transceiver has two SHUTDOWN modes. One mode disables the drivers and the charge pump, the other shuts down all circuitry. While shut down, the drivers and receivers assume high impedance output states.

TYPICAL APPLICATION



Output Waveforms

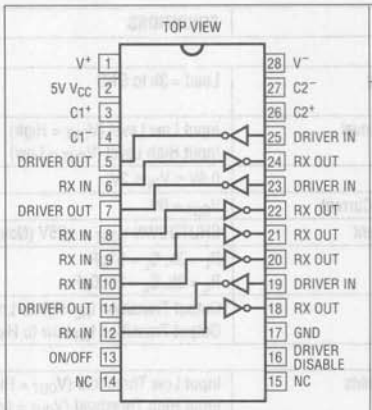


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- (Note 7) ..... −6.5V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
Output Voltage
  Driver ..... −30V to 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1137AC ..... 0°C to 70°C
  LT1137AI ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1137ACN
LT1137ACS
LT1137ACG
LT1137AIN
LT1137AIS

Consult factory for Military grade parts.

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				8.6		V
V^- Output				−7.2		V
Supply Current (V_{CC})	(Note 3)	●		12	17	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 4) DRIVER DISABLE	● ●		1 4	10	µA mA
Supply Rise Time SHUTDOWN to Turn-On	C1, C2, C^+, C^- = 1µF, C^+, C^- = 0.1µF, C1, C2 = 0.2µF			2.0 0.2		ms ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN) Input High Level (Device Enabled)	● ●	 2.4	1.4 1.4	0.8	V V
ON/OFF Pin Current	0V ≤ $V_{ON/OFF}$ ≤ 5V	●	−15		80	µA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled) Input High Level (Drivers Disabled)	● ●	 2.4	1.4 1.4	0.8	V V
Driver Disable Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	−10		500	µA
Oscillator Frequency				130		kHz

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.5		V
		Negative	●		−6.3	−5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2V$		●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V				±17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±25V (Note 4)		●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF				15	30	V/µs
	R_L = 3k, C_L = 2500pF			4	15		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)				0.6	1.3	µs
	Output Transition t_{LH} Low to High				0.5	1.3	µs
Any Receiver							
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)		●	0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V			3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)		●	3.5	4.2		V
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$		●		1	10	µA
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$				−20	−10	mA
	Sourcing Current, V_{OUT} = 0V			10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				250	600	ns
	Output Transition t_{LH} Low to High				350	600	ns

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade, and $-40°C \le T_A \le 85°C$ for industrial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$ = 3V.

Note 3: Supply current is measured with driver and receiver outputs unloaded and the driver inputs tied high.

Note 4: Supply current and leakage current measurements in SHUTDOWN are performed with $V_{ON/OFF}$ = 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ = 3V.

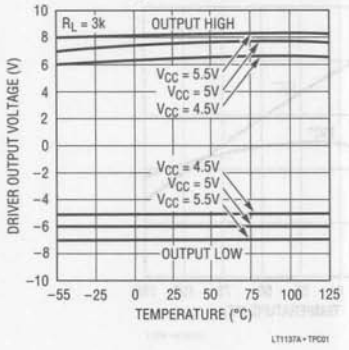
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

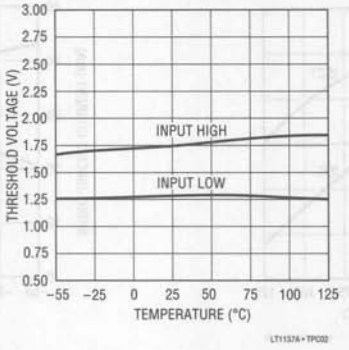
Note 7: Absolute maximum externally applied voltage. Internal charge pump may force a larger value on this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

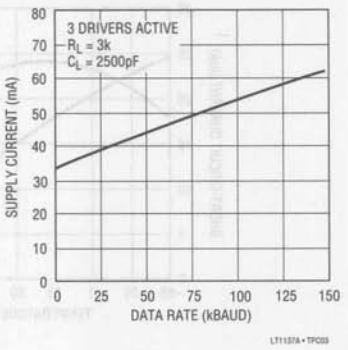
Driver Output Voltage



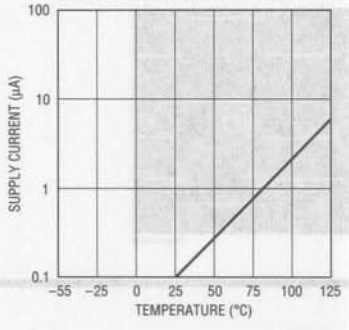
Receiver Input Thresholds



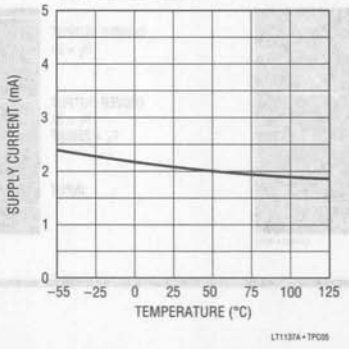
Supply Current vs Data Rate



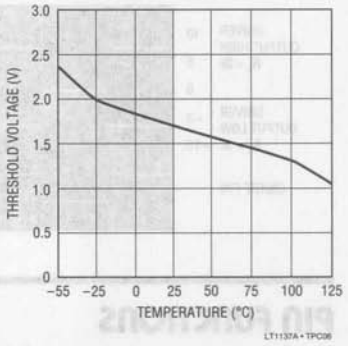
Supply Current in SHUTDOWN



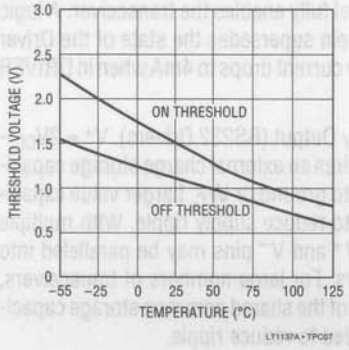
Supply Current in DRIVER DISABLE



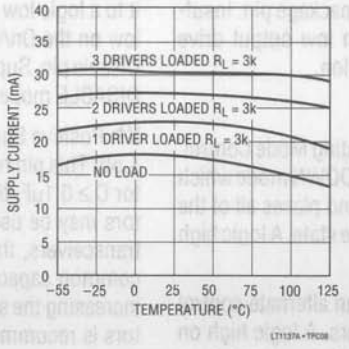
Driver Disable Threshold



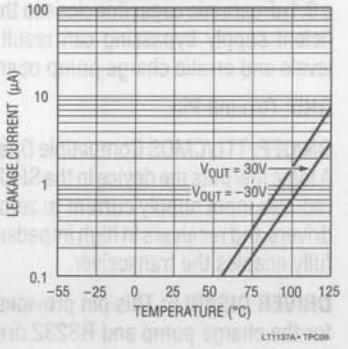
On/Off Thresholds



Supply Current



Driver Leakage in SHUTDOWN



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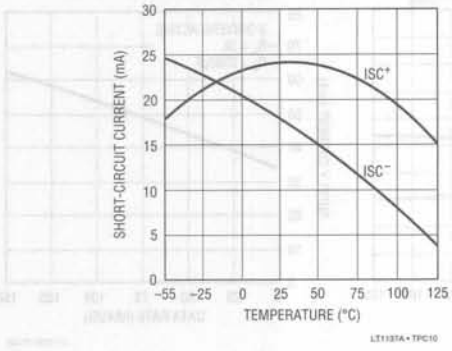
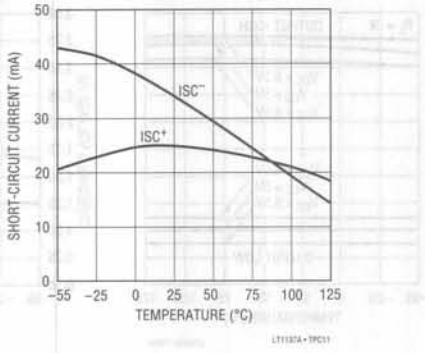
TYPICAL PERFORMANCE CHARACTERISTICS

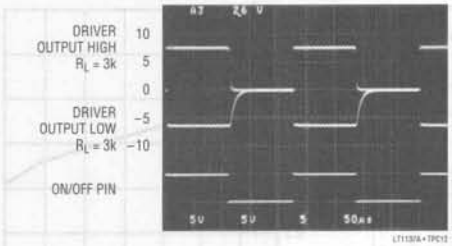
Driver Short-Circuit Current



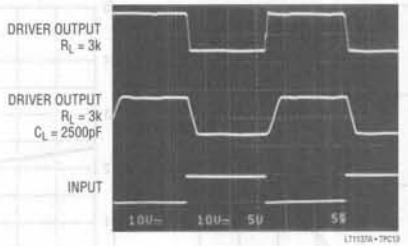
Receiver Short-Circuit Current



SHUTDOWN to Driver Output



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current drops to zero in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/OFF: TTL/CMOS Compatible Operating Mode Control. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places all of the drivers and receivers in high impedance state. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. Receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. A logic low on the On/Off pin supersedes the state of the Driver Disable pin. Supply current drops to 4mA when in DRIVER DISABLE mode.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of transceivers, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

PIN FUNCTIONS

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC}-2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. V^- is short-circuit proof for 30 seconds.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance. In applications where larger positive voltages are available, such as 12V, C1 may be omitted and the positive voltage may be connected directly to the $C1^+$ pin. In this mode of operation, the V^+ pin should be decoupled with a $0.1\mu F$ ceramic capacitor.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

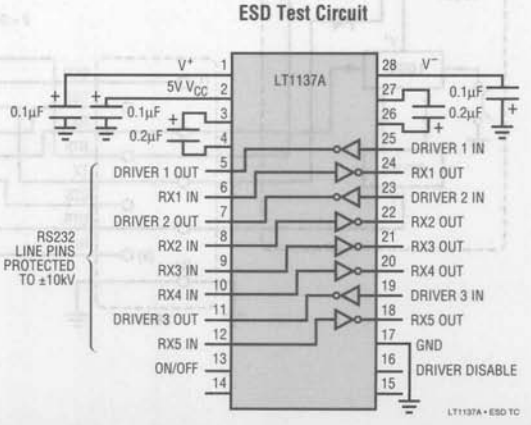
RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

5

ESD PROTECTION

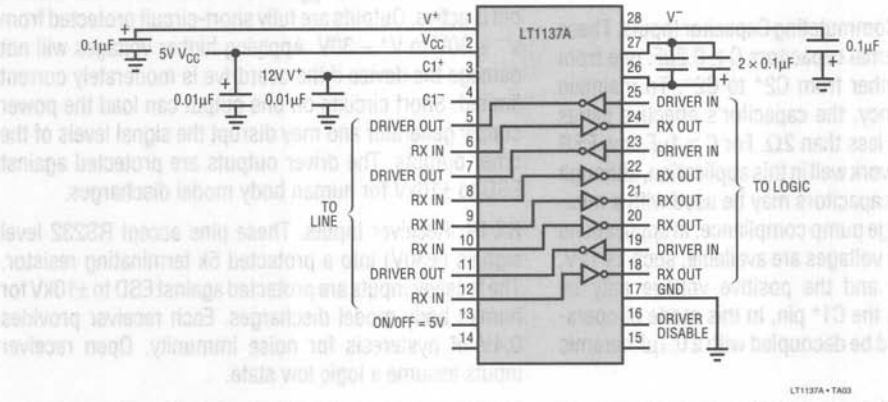
The RS232 line inputs of the LT1137A have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1137A must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit

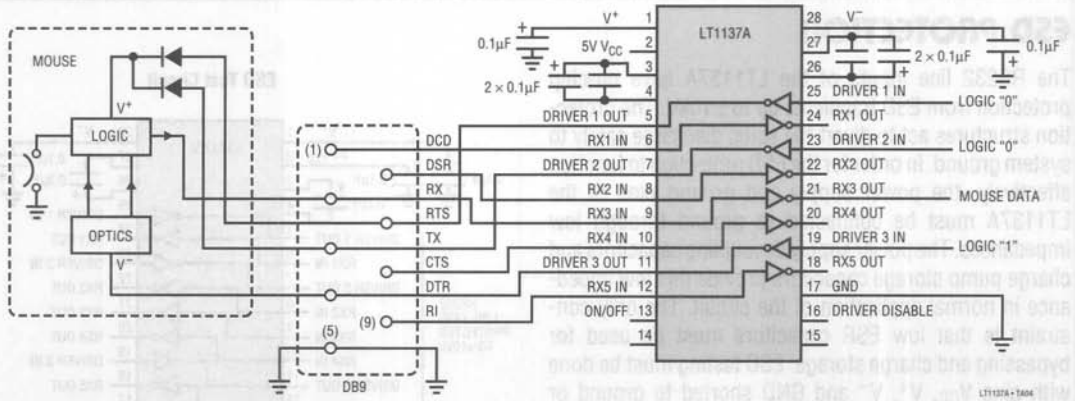


TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



Typical Mouse Driving Application



Low Power 5V RS232 Dual Driver/Receiver with 0.1µF Capacitors

FEATURES

- ESD Protection over ±**10kV**
- Uses Small Capacitors: 0.1µF
- Operates to 120k Baud
- Outputs Withstand ±30V Without Damage
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Meets All RS232 Specifications
- Available With or Without Shutdown
- Absolutely No Latch-up
- Available in SO Package

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

The LT1180A/LT1181A are dual RS232 driver/receiver pairs with integral charge pump to generate RS232 voltage levels from a single 5V supply. These circuits feature rugged bipolar design to provide operating fault tolerance and ESD protection unmatched by competing CMOS designs. Using only 0.1µF external capacitors, these circuits consume only 40mW of power, and can operate to 120k baud even while driving heavy capacitive loads. New ESD structures on the chip allow the LT1180A/LT1181A to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins. The LT1180A/LT1181A are fully compliant with EIA RS232 standards. Driver outputs are protected from overload, and can be shorted to ground or up to ±30V without damage. During SHUTDOWN or power-off conditions, driver and receiver outputs are in a high impedance state, allowing line sharing.

The LT1181A is available in 16-pin DIP and SO packages. The LT1180A is supplied in 18-pin DIP and SO packages for applications which require SHUTDOWN.

TransZorb is a registered trademark of General Instruments, GSI

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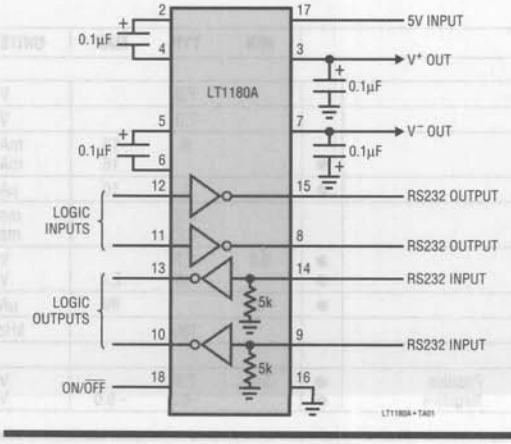
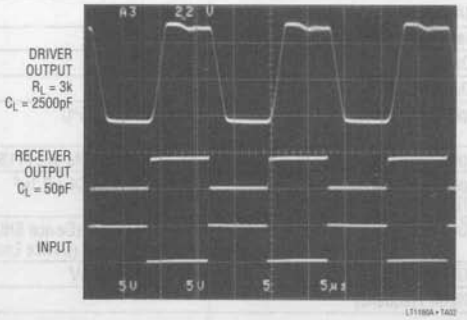
TYPICAL APPLICATION



Output Waveforms

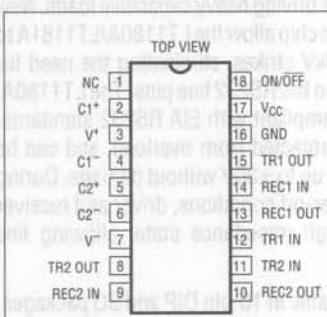


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... −13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  ON/$\overline{OFF}$ ..... −0.3V to 12V
Output Voltage
  Driver ..... V^+ − 30V to V^- + 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V

Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1180AI/LT1181AI ..... −40°C to 85°C
  LT1180AC/LT1181AC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

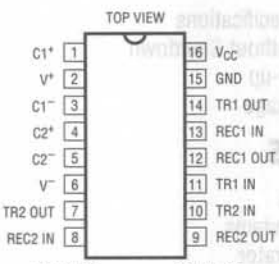


N PACKAGE 18-LEAD PLASTIC DIP
S PACKAGE 18-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 80°C/W, θ_{JC} = 36°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 26°C/W (S)

ORDER PART NUMBER

LT1180AIN
LT1180ACN
LT1180ACS



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 46°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 95°C/W, θ_{JC} = 27°C/W (S)

ORDER PART NUMBER

LT1181AIN
LT1181ACN
LT1181ACS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Generator							
V^+ Output					7.9		V
V^- Output					−7.0		V
Supply Current (V_{CC})	(Note 3), T_A = 25°C				9	13	mA
			●			16	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 4) LT1180A Only		●		1	10	µA
Supply Rise Time	C1 = C2 = C3 = C4 = 0.1µF				0.2		ms
SHUTDOWN to Turn-On	LT1180A Only				0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN)		●	0.8	1.2		V
	Input High Level (Device Enabled)		●		1.6	2.4	V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/\overline{OFF}}$ ≤ 5V		●	−15		80	µA
Oscillator Frequency					130		kHz
Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.5		V
		Negative	●		−6.3	−5.0	V

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)	● ●	 2.0	1.4 1.4	0.8	V V
Logic Input Current	$0.8V \le V_{IN} \le 2.0V$	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)	●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF R_L = 3k, C_L = 2500pF	 	 4	15 7	30	V/µs V/µs
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5) Output Transition t_{LH} Low-to-High	 		0.6 0.5	1.3 1.3	µs µs
Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High) Input High Threshold (V_{OUT} = Low)	 	0.8 	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$	●		1	10	µA
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V	 	 10	−20 20	−10	mA mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 6) Output Transition t_{LH} Low-to-High	 		250 350	600 600	ns ns

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade, and −40°C ≤ T_A ≤ 85°C for industrial grade.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/\overline{OFF}}$ = 3V, unless otherwise specified.

Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = C1 = C2 = 0.1\mu F$. All outputs are open, with all driver inputs tied high.

Note 4: Supply current measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}} \le 0.1V$.

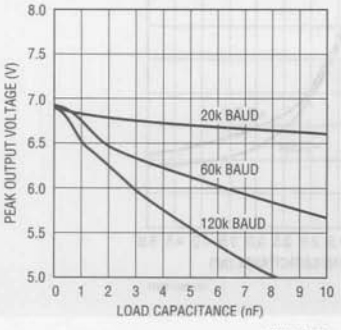
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

5

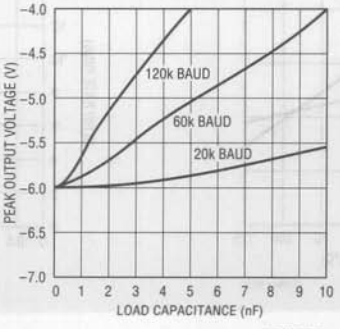
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Maximum Output Voltage vs Load Capacitance



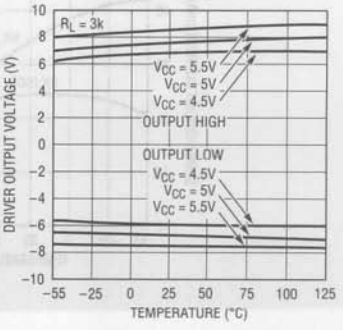
LT1180A • TPC01

Driver Minimum Output Voltage vs Load Capacitance



LT1180A • TPC02

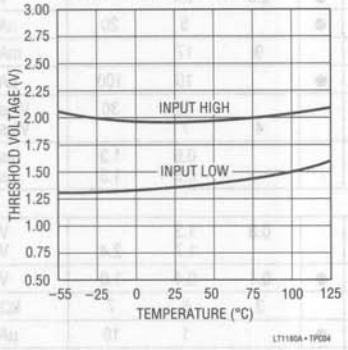
Driver Output Voltage



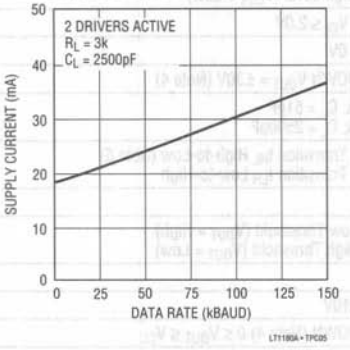
LT1180A • TPC03

TYPICAL PERFORMANCE CHARACTERISTICS

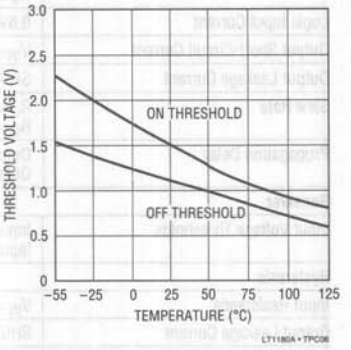
Receiver Input Thresholds



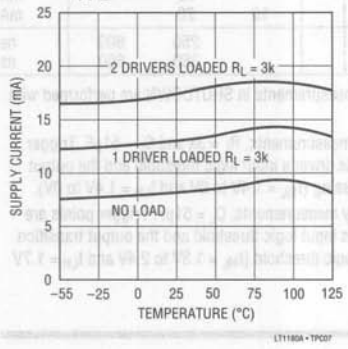
Supply Current vs Data Rate



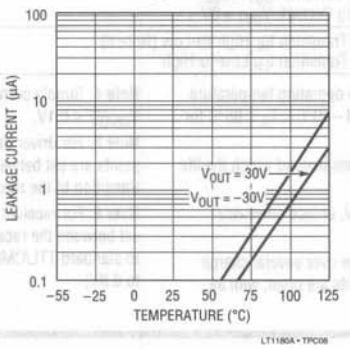
ON/$\overline{\text{OFF}}$ Thresholds



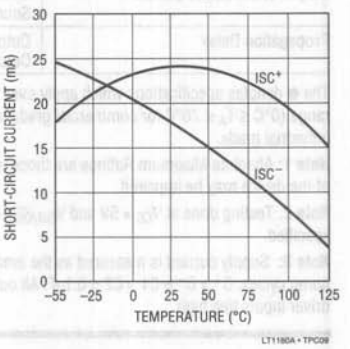
Supply Current



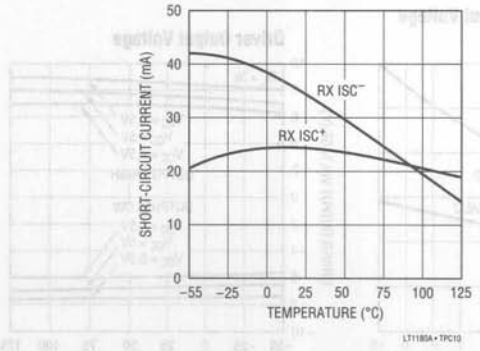
Driver Leakage in Shutdown



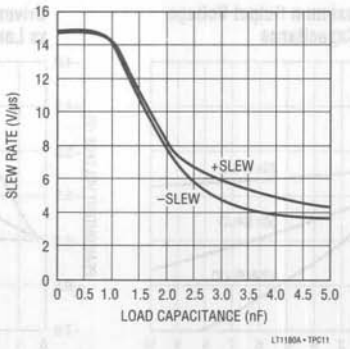
Driver Short-Circuit Current



Receiver Short-Circuit Current

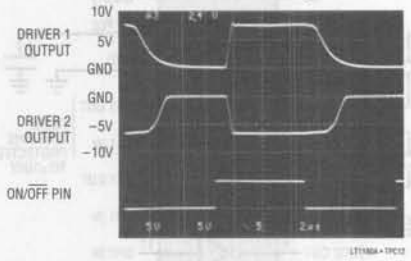


Slew Rate vs Load Capacitance

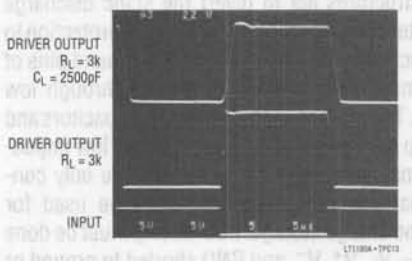


TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown to Driver Outputs



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/$\overline{OFF}$: A TTL/CMOS Compatible Operating Mode Control. A logic low puts the LT1180A in SHUTDOWN mode. Supply current drops to zero and both driver and receiver outputs assume a high impedance state. A logic high fully enables the device.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

TR1 IN, TR2 IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT, TR2 OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

REC1 IN, REC2 IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

REC1 OUT, REC2 OUT: Receiver outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power ON, OFF or in the SHUTDOWN mode.

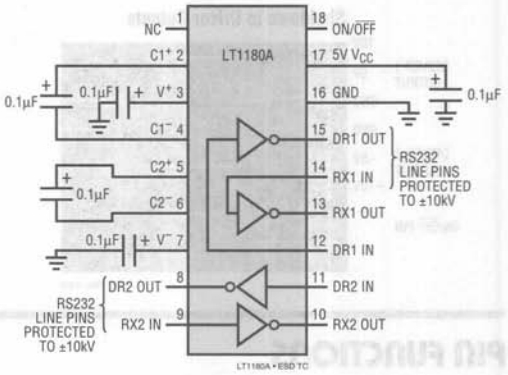
$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.1\mu F$: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. C1 should be deleted if a separate 12V supply is available and connected to pin $C1^+$. Similarly, C2 should be deleted if a separate –12V supply is connected to pin V^-.

5

ESD PROTECTION

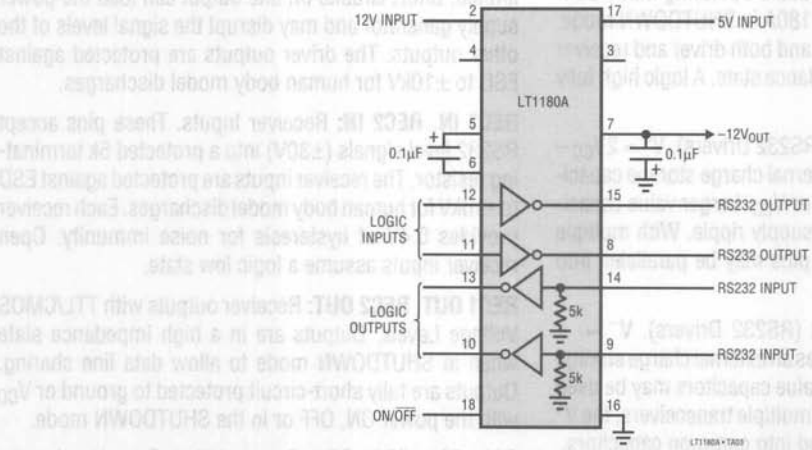
The RS232 line inputs of the LT1180A/LT1181A have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V_L, V^+, V^-, and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



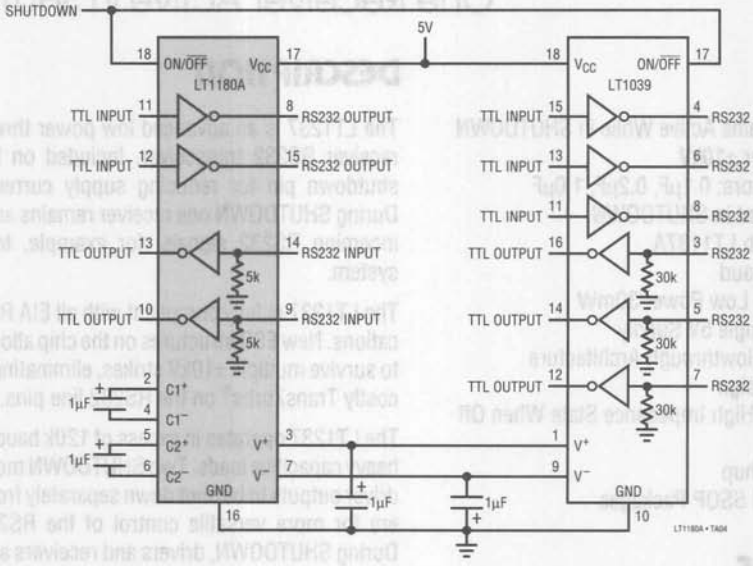
TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



TYPICAL APPLICATIONS

Supporting an LT1039 (Triple Driver/Receiver)



5

5V RS232 Transceiver with Advanced Power Management and One Receiver Active in SHUTDOWN

FEATURES

- One Receiver Remains Active While in SHUTDOWN
- ESD Protection over ±**10kV**
- Uses Small Capacitors: 0.1µF, 0.2µF, 1.0µF
- 60µA Supply Current in SHUTDOWN
- Pin-Compatible with LT1137A
- Operates to 120k Baud
- CMOS Comparable Low Power 30mW
- Operates from a Single 5V Supply
- Easy PC Layout – Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Absolutely No Latchup
- Available in SO and SSOP Packages

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

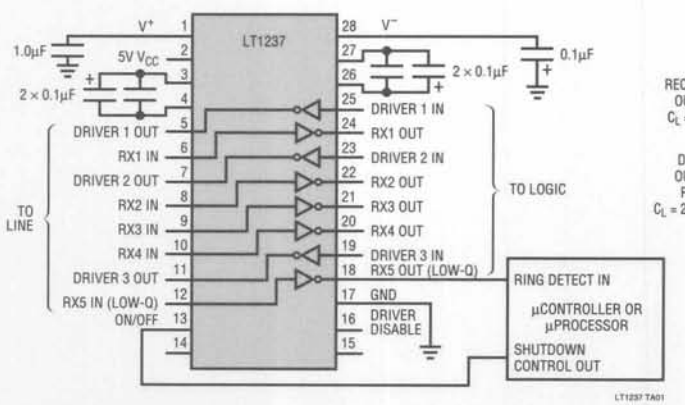
The LT1237 is an advanced low power three driver, five receiver RS232 transceiver. Included on the chip is a shutdown pin for reducing supply current near zero. During SHUTDOWN one receiver remains active to detect incoming RS232 signals, for example, to wake up a system.

The LT1237 is fully compliant with all EIA RS232 specifications. New ESD structures on the chip allow the LT1237 to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins.

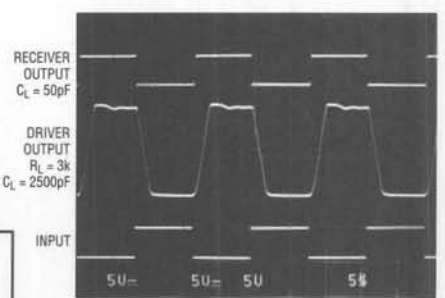
The LT1237 operates in excess of 120k baud even driving heavy capacitive loads. Two SHUTDOWN modes allow the driver outputs to be shut down separately from the receivers for more versatile control of the RS232 interface. During SHUTDOWN, drivers and receivers assume a high impedance state.

TransZorb® is a registered trademark of General Instruments, GSI

TYPICAL APPLICATION



Output Waveforms

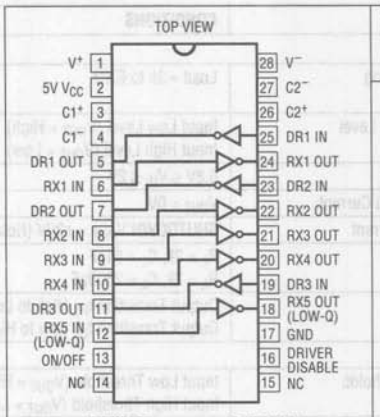


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... –30V to 30V
Output Voltage
  Driver ..... –30V to 30V
  Receiver ..... –0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1237I ..... –40°C to 85°C
  LT1237C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
28-LEAD CERAMIC DIP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD SOL

G PACKAGE
28-LEAD SSOP

T_{JMAX} = 150°C, θ_{JA} = 62°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 85°C/W (S)
T_{JMAX} = 150°C, θ_{JA} = 96°C/W (G)

ORDER PART NUMBER
LT1237IJ
LT1237IN
LT1237CJ
LT1237CN
LT1237CS
LT1237CG

Consult factory for Military grade parts.

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				7.9		V
V^- Output				–7		V
Supply Current (V_{CC})	T_A = 25°C (Note 3)			6	12	mA
		●		6	14	mA
Supply Current when OFF (V_{CC})	SHUTDOWN (Note 4)	●		0.06	0.15	mA
	DRIVER DISABLE			3.00		mA
Supply Rise Time SHUTDOWN to Turn-On	C1 = C2 = 0.2µF, C+ = 1.0µF, C– = 0.1µF			2		ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN)	●	0.8	1.2		V
	Input High Level (Device Enabled)	●		1.6	2.4	V
ON/OFF Pin Current	0V ≤ $V_{ON/OFF}$ ≤ 5V	●	–15		80	µA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●	0.8	1.4		V
	Input High Level (Drivers Disabled)	●		1.4	2.4	V
Driver Disable Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	–10		500	µA
Oscillator Frequency	Driver Outputs Loaded R_L = 3k			130		kHz

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.5		V
		Negative	●		−6.3	−5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2V$		●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)		●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF				15	30	V/µs
	R_L = 3k, C_L = 2500pF			4	7		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)				0.6	1.3	µs
	Output Transition t_{LH} Low to High				0.5	1.3	µs
Any Receiver							
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)			0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)				1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V			3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$		●		1	10	µA
Receivers 1, 2, 3, 4							
Output Voltage	Output Low, I_{OUT} = −1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)		●	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−10	−20		mA
	Sourcing Current, V_{OUT} = 0V			10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				250	600	ns
	Output Transition t_{LH} Low to High				350	600	ns
Receiver 5 (LOW I_{SUPPLY} RX)							
Output Voltage	Output Low, I_{OUT} = −500µA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)		●	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−2	−4		mA
	Sourcing Current, V_{OUT} = 0V			2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				1.0	3	µs
	Output Transition t_{LH} Low to High				0.6	3	µs

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade, and $-40°C \le T_A \le 85°C$ for industrial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$ = 3V, unless otherwise specified.

Note 3: Supply current is measured as the average over several charge pump burst cycles. C^+ = 1.0µF, C^- = 0.1µF, C1 = C2 = 0.2µF. All outputs are open, with all driver inputs tied high.

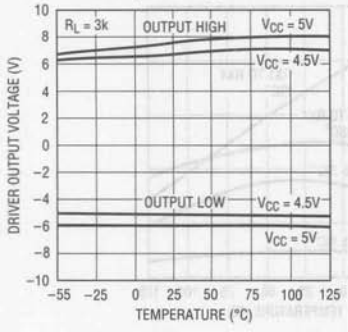
Note 4: Measurements in SHUTDOWN are performed with $V_{ON/OFF} \le 0.1V$. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE} \ge 3V$.

Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

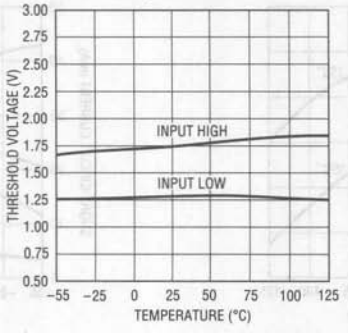
Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

TYPICAL PERFORMANCE CHARACTERISTICS

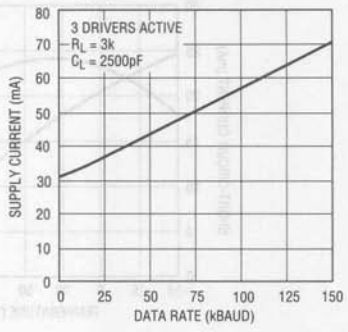
Driver Output Voltage



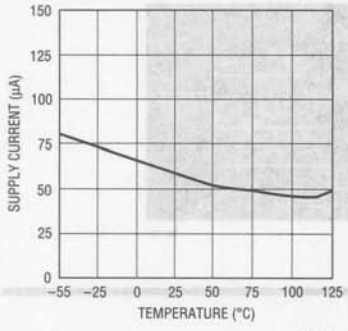
Receiver Input Thresholds



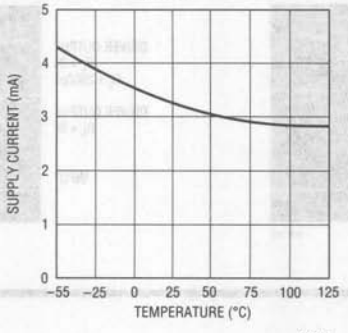
Supply Current vs Data Rate



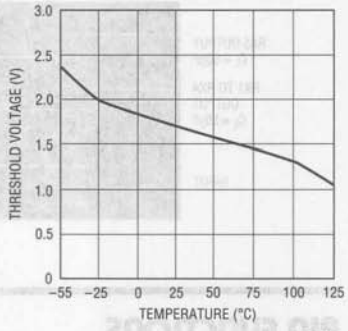
Supply Current in SHUTDOWN



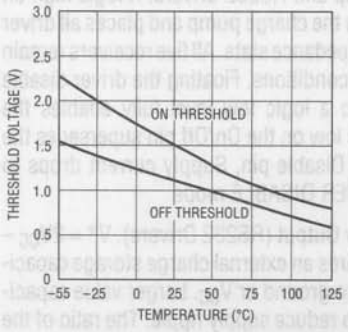
Supply Current in DRIVER DISABLE



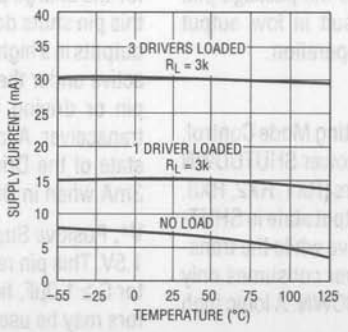
Driver Disable Threshold



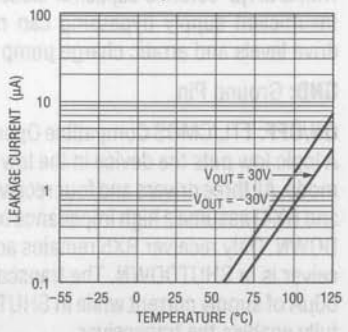
On/Off Thresholds



Supply Current



Driver Leakage in SHUTDOWN



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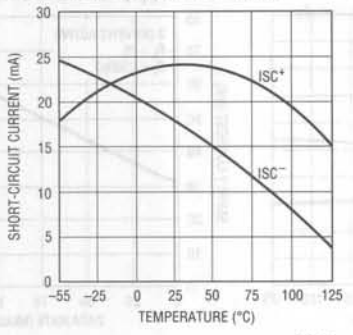
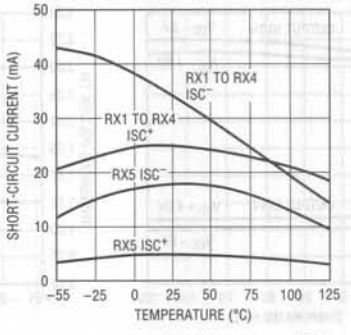
TYPICAL PERFORMANCE CHARACTERISTICS

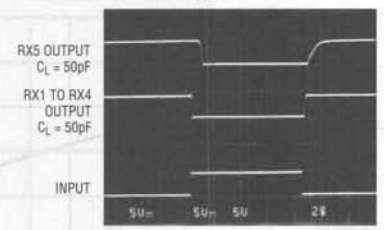
Driver Short-Circuit Current



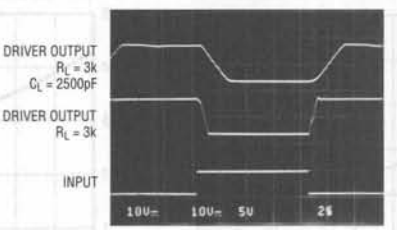
Receiver Short-Circuit Current



Receiver Output Waveforms



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/OFF: TTL/CMOS Compatible Operating Mode Control. A logic low puts the device in the low power SHUTDOWN mode. All three drivers and four receivers (RX1, RX2, RX3, and RX4) assume a high impedance output state in SHUTDOWN. Only receiver RX5 remains active while the transceiver is in SHUTDOWN. The transceiver consumes only 60µA of supply current while in SHUTDOWN. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all driver outputs in a high impedance state. All five receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. A logic low on the On/Off pin supersedes the state of the Driver Disable pin. Supply current drops to 3mA when in DRIVER DISABLE mode.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 1.0\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. The ratio of the capacitors on V^+ and V^- should be greater than 5 to 1.

PIN FUNCTIONS

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. See the Applications Information section for guidance in choosing filter capacitors for V^+ and V^-.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs, require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs RX1, RX2, RX3, and RX4 are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RX OUT, are fully short-circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

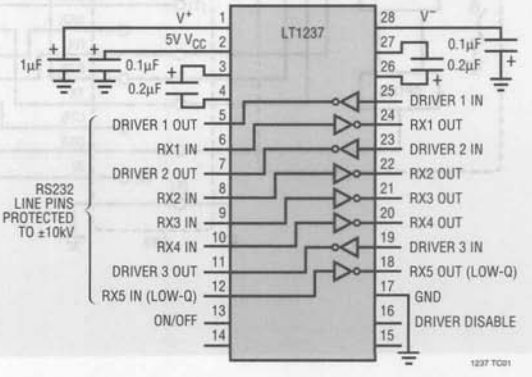
LOW Q-CURRENT RX IN: Low Power Receiver Input. This special receiver remains active when the part is in SHUTDOWN mode, consuming typically 60µA. This receiver has the same 5k input impedance and ±10kV ESD protection characteristics as the other receivers.

LOW Q-CURRENT RX OUT: Low Power Receiver Output. This pin produces the same TTL/CMOS output voltage levels as receivers RX1, RX2, RX3, and RX4 with slightly decreased speed and short-circuit current. Data rates to 120k baud are supported by this receiver.

ESD PROTECTION

The RS232 line inputs of the LT1237 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1237 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V_L, V^+, V^-, and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



APPLICATIONS INFORMATION

Storage Capacitor Selection

The V^+ and V^- storage capacitors must be chosen carefully to insure low ripple and stable operation. The LT1237 charge pump operates in a power efficient Burst Mode™. When storage capacitor voltage drops below a preset threshold, the oscillator is gated on until V^+ and V^- are boosted up to levels exceeding a second threshold. The oscillator then turns off, and current is supplied from the V^+ and V^- storage capacitors.

The V^- potential is monitored to control charge pump operation. It is therefore important to insure lower V^+ ripple than V^- ripple, or erratic operation of the charge pump will result. Proper operation is insured in most applications by choosing the V^+ filter capacitor to be at least 5 times the V^- filter capacitor value. If V^+ is more heavily loaded than V^-, a larger ratio may be needed.

The V^- filter capacitor should be selected to obtain low ripple when the drivers are loaded, forcing the charge pump into continuous mode. A minimum value 0.1µF is suggested.

Do not attempt to reduce V^- ripple when the charge pump is in discontinuous Burst Mode™ operation. The ripple in this mode is determined by internal comparator thresholds. Larger storage capacitor values increase the burst period, and do not reduce ripple amplitude.

Power Saving Operational Modes

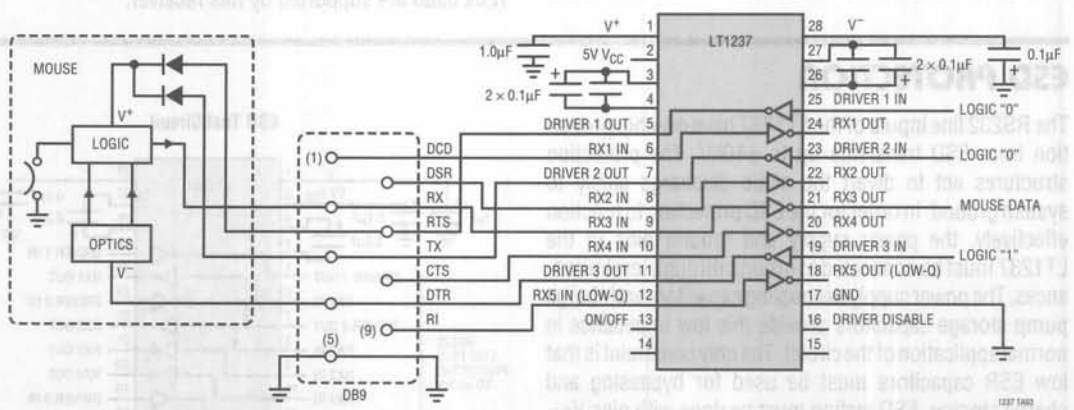
The LT1237 has both SHUTDOWN and DRIVER DISABLE operating modes. These operating modes can optimize power consumption based upon applications needs.

The On/Off shutdown control turns off all circuitry except for Low-Q RX5. When RX5 detects a signal, this information can be used to wake up the system for full operation.

If more than one line must be monitored, the DRIVER DISABLE mode provides a power efficient operating option. The DRIVER DISABLE mode turns off the charge pump and RS232 drivers, but keeps all five receivers active. Power consumption in DRIVER DISABLE mode is 3mA from V_{CC}.

Burst Mode™ is a trademark of Linear Technology Corporation

Typical Mouse Driving Application



Low Power 5V RS232 Dual Driver/Receiver with 0.1µF Capacitors

FEATURES

- 10mA Max Supply Current
- ESD Protection over ±**10kV**
- Uses Small Capacitors: 0.1µF
- Operates to 120k Baud
- Outputs Withstand ±30V Without Damage
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Meets All RS232 Specifications
- Available With or Without Shutdown
- Absolutely No Latch-up
- Available in SO Package

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

The LT1280A/LT1281A are dual RS232 driver/receiver pairs with integral charge pump to generate RS232 voltage levels from a single 5V supply. These circuits feature rugged bipolar design to provide operating fault tolerance and ESD protection unmatched by competing CMOS designs. Using only 0.1µF external capacitors, these circuits consume only 40mW of power, and can operate to 120k baud even while driving heavy capacitive loads. New ESD structures on the chip allow the LT1280A/LT1281A to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins. The LT1280A/LT1281A are fully compliant with EIA RS232 standards. Driver outputs are protected from overload, and can be shorted to ground or up to ±30V without damage. During SHUTDOWN or power-off conditions, driver and receiver outputs are in a high impedance state, allowing line sharing.

The LT1281A is available in 16-pin DIP and SO packages. The LT1280A is supplied in 18-pin DIP and SO packages for applications which require SHUTDOWN.

TransZorb is a registered trademark of General Instruments, GSI

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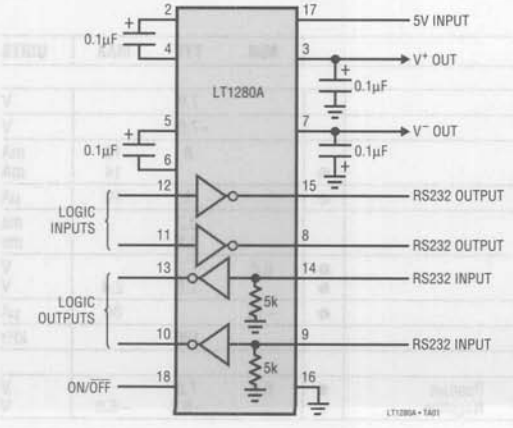
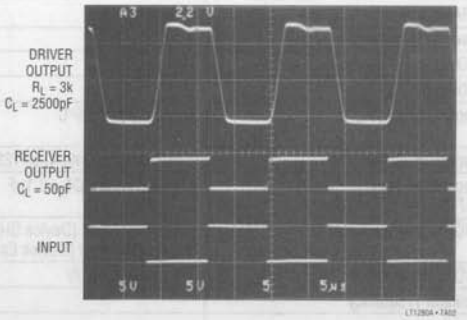
TYPICAL APPLICATION



Output Waveforms

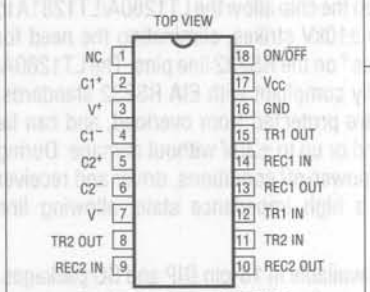


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... −13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  ON/$\overline{OFF}$ ..... −0.3V to 12V
Output Voltage
  Driver ..... V^+ − 30V to V^- + 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V

Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1280AI/LT1281AI ..... −40°C to 85°C
  LT1280AC/LT1281AC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

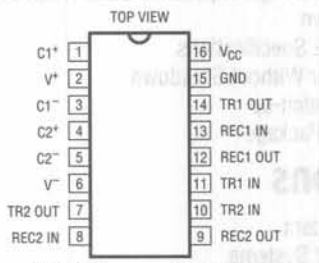


N PACKAGE 18-LEAD PLASTIC DIP
S PACKAGE 18-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 80°C/W, θ_{JC} = 36°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 26°C/W (S)

ORDER PART NUMBER

LT1280AIN
LT1280ACN
LT1280ACS



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 46°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 95°C/W, θ_{JC} = 27°C/W (S)

ORDER PART NUMBER

LT1281AIN
LT1281ACN
LT1281ACS

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Generator							
V^+ Output					7.9		V
V^- Output					−7.0		V
Supply Current (V_{CC})	(Note 3), T_A = 25°C				8	10	mA
			●			14	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 4) LT1280A Only		●		1	10	µA
Supply Rise Time	C1 = C2 = C3 = C4 = 0.1µF				0.2		ms
SHUTDOWN to Turn-On	LT1280A Only				0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN)		●	0.8	1.2		V
	Input High Level (Device Enabled)		●		1.6	2.4	V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/\overline{OFF}}$ ≤ 5V		●	−15		80	µA
Oscillator Frequency					130		kHz
Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.5		V
		Negative	●		−6.3	−5.0	V

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)	● ●	 2.0	1.4 1.4	0.8	V V
Logic Input Current	$0.8V \le V_{IN} \le 2.0V$	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)	●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF R_L = 3k, C_L = 2500pF		 4	15 7	30	V/µs V/µs
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5) Output Transition t_{LH} Low-to-High			0.6 0.5	1.3 1.3	µs µs
Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High) Input High Threshold (V_{OUT} = Low)		0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$	●		1	10	µA
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 10	−20 20	−10	mA mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 6) Output Transition t_{LH} Low-to-High			250 350	600 600	ns ns

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade, and $-40°C \le T_A \le 85°C$ for industrial grade.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/\overline{OFF}}$ = 3V, unless otherwise specified.

Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = C1 = C2 = 0.1\mu F$. All outputs are open, with all driver inputs tied high.

Note 4: Supply current measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}} \le 0.1V$.

Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

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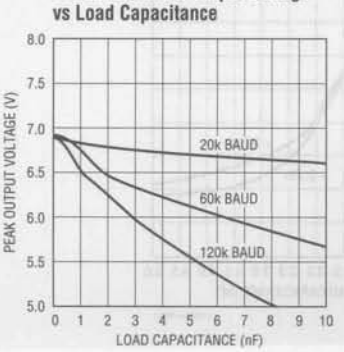
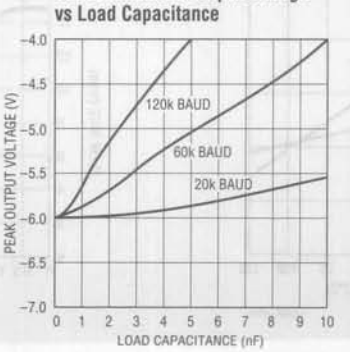
TYPICAL PERFORMANCE CHARACTERISTICS

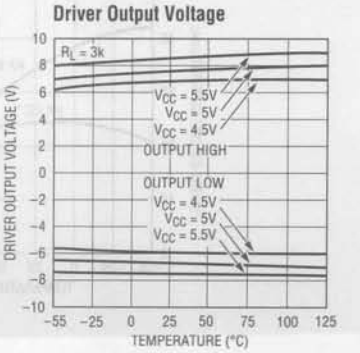
Driver Maximum Output Voltage vs Load Capacitance



Driver Minimum Output Voltage vs Load Capacitance

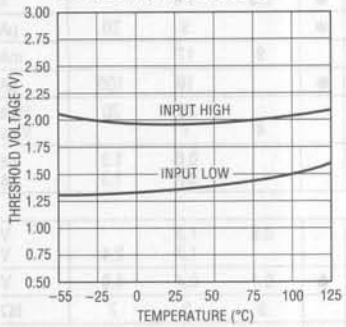


Driver Output Voltage

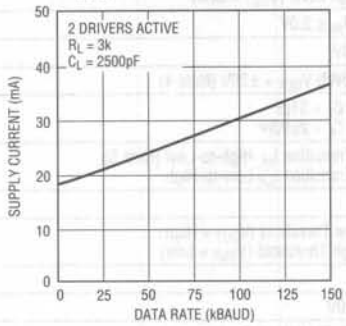


TYPICAL PERFORMANCE CHARACTERISTICS

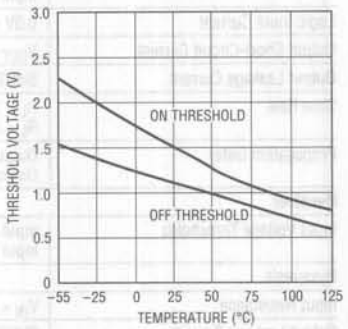
Receiver Input Thresholds



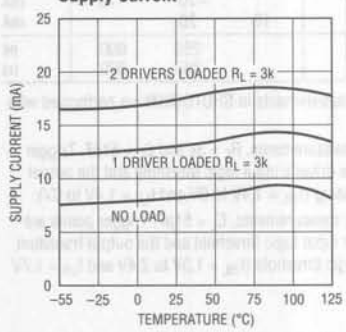
Supply Current vs Data Rate



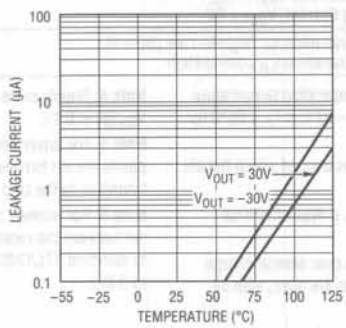
ON/$\overline{\text{OFF}}$ Thresholds



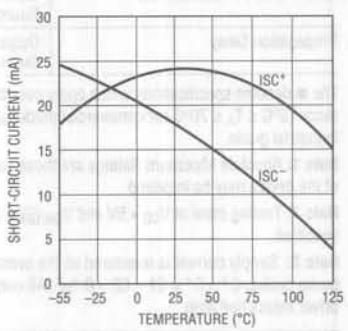
Supply Current



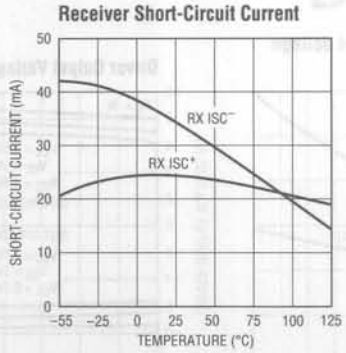
Driver Leakage in Shutdown



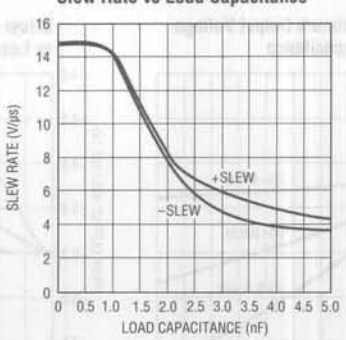
Driver Short-Circuit Current



Receiver Short-Circuit Current

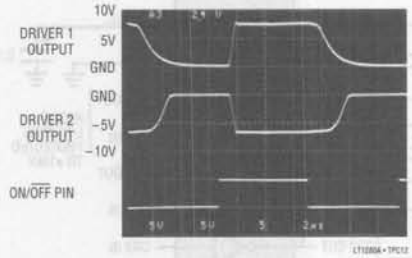


Slew Rate vs Load Capacitance

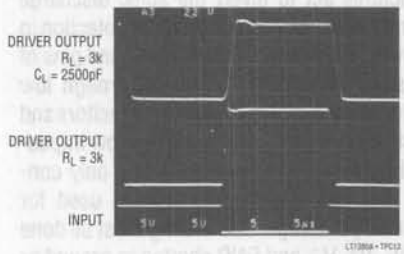


TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown to Driver Outputs



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/$\overline{OFF}$: A TTL/CMOS Compatible Operating Mode Control. A logic low puts the LT1280A in SHUTDOWN mode. Supply current drops to zero and both driver and receiver outputs assume a high impedance state. A logic high fully enables the device.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

TR1 IN, TR2 IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT, TR2 OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode or $V_{CC} = 0V$. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

REC1 IN, REC2 IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

REC1 OUT, REC2 OUT: Receiver outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power ON, OFF or in the SHUTDOWN mode.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.1\mu F$: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. C1 should be deleted if a separate 12V supply is available and connected to pin $C1^+$. Similarly, C2 should be deleted if a separate –12V supply is connected to pin V^-.

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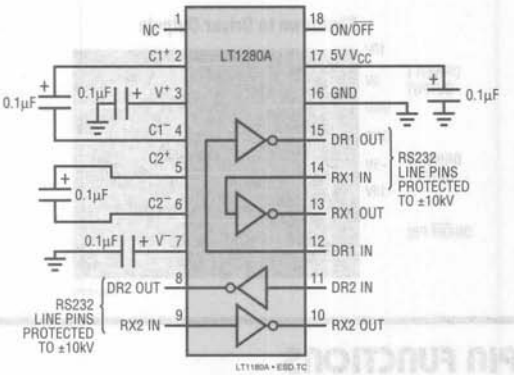
ESD PROTECTION

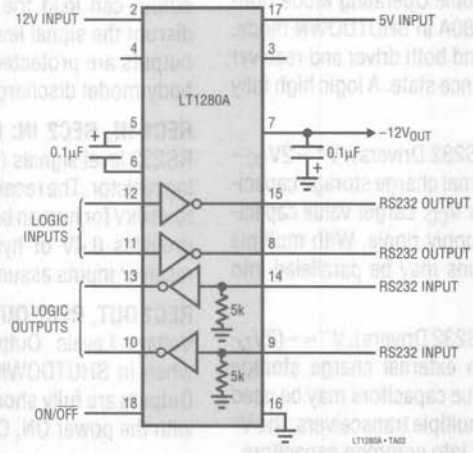
The RS232 line inputs of the LT1280A/LT1281A have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V_L, V^+, V^-, and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



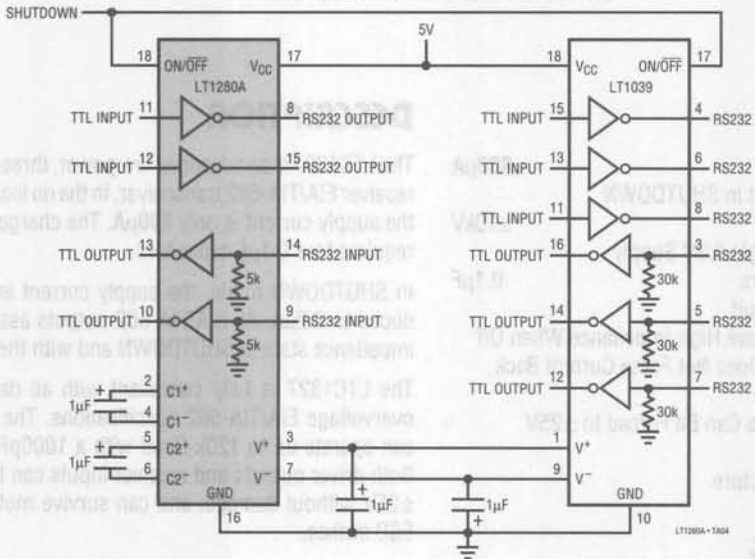
TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



TYPICAL APPLICATIONS

Supporting an LT1039 (Triple Driver/Receiver)



5

3.3V Micropower EIA/TIA-562 Transceiver

FEATURES

- Low Supply Current **300μA**
- 0.2μA Supply Current in SHUTDOWN
- ESD Protection ±10kV
- Operates From a Single 3.3V Supply
- Uses Small Capacitors 0.1μF
- Operates To 120k Baud
- Three-State Outputs are High Impedance When Off
- Output Overvoltage Does Not Force Current Back Into Supplies
- EIA/TIA-562 I/O Lines Can Be Forced to ±25V Without Damage
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

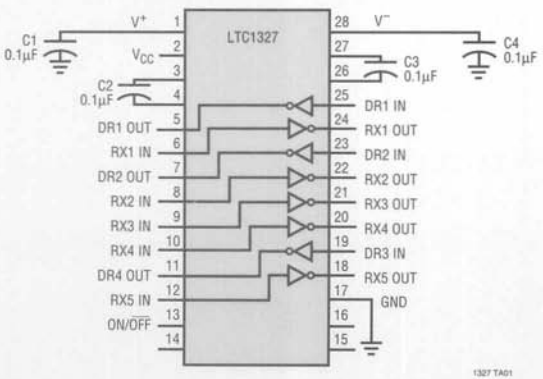
The LTC1327 is an advanced low power, three-driver/five-receiver EIA/TIA-562 transceiver. In the no load condition, the supply current is only **300μA**. The charge pump only requires four 0.1μF capacitors.

In SHUTDOWN mode, the supply current is further reduced to 0.2μA. All EIA/TIA-562 outputs assume a high impedance state in SHUTDOWN and with the power off.

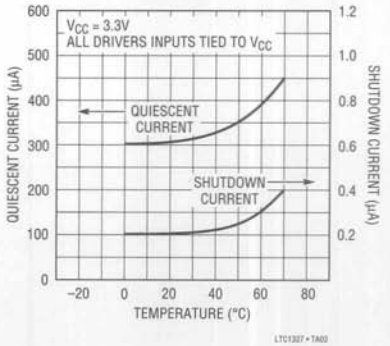
The LTC1327 is fully compliant with all data rate and overvoltage EIA/TIA-562 specifications. The transceiver can operate up to 120k Baud with a 1000pF//3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with SHUTDOWN



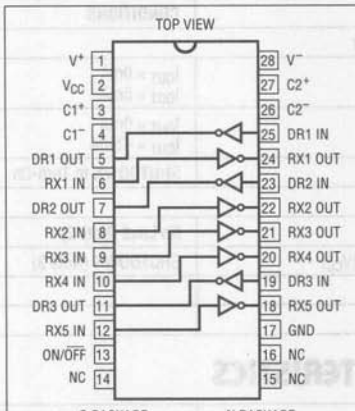
Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 5V
Input Voltage
  Driver ..... −0.3V to (V_{CC} + 0.3V)
  Receiver ..... −25V to 25V
  On/$\overline{Off}$ Pin ..... −0.3V to (V_{CC} + 0.3V)
Output Voltage
  Driver ..... −25V to 25V
  Receiver ..... −0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  Commercial LTC1327C ..... 0°C to 70°C
Storage Temperature Range ..... −65°c to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1327CG
LTC1327CN
LTC1327CS

Consult factory for Industrial and Military grade parts.

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 to C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	Positive Negative (3k to GND)	● ●	3.7 −3.7	4.5 −4.5		V V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)	● ●	 2	1.4 1.4	0.8	V V
Logic Input Current	V_{IN} = 3.3 V_{IN} = 0	● ●			5 −5	µA µA
Output Short-Circuit Current	V_{OUT} = 0V			±7		mA
Output Leakage Current	SHUTDOWN (Note 3), V_{OUT} = ±20V			±10	±500	µA
Any Receiver						
Input Voltage Thresholds	Input Low Threshold Input High Threshold	● ●	0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA (V_{CC} = 3.3V) Output High, I_{OUT} = 160µA (V_{CC} = 3.3V)	● ●	 3	0.2 3.2	0.4	V V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC}		−2	−10		mA
Output Leakage Current	SHUTDOWN (Note 3), 0 ≤ V_{OUT} ≤ V_{CC}	●		1	10	µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 to C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA I_{OUT} = 5mA			5.7 5.5		V V
V^- Output Voltage	I_{OUT} = 0mA I_{OUT} = −5mA			−5.3 −5.0		V V
Supply Rise Time	SHUTDOWN to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.3	0.5	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 3)	●		0.2	10	µA
On/$\overline{\text{Off}}$ Threshold Low		●		1.4	0.8	V
On/$\overline{\text{Off}}$ Threshold High		●	2	1.4		V

AC CHARACTERISTICS

Slew Rate	R_L = 3k, C_L = 51pF R_L = 3k, C_L = 1000pF			6 5	30	V/µs V/µs
Driver Propagation Delay (TTL to EIA/TIA-562)	t_{HLD} t_{LHD}	● ●		2 2	3.5 3.5	µs µs
Receiver Propagation Delay (EIA/TIA-562 to TTL)	t_{HLR} t_{LHR}	● ●		0.3 0.2	0.8 0.8	µs µs

The ● denotes specifications which apply over the operating temperature (0°C ≤ T_A ≤ 70°C).

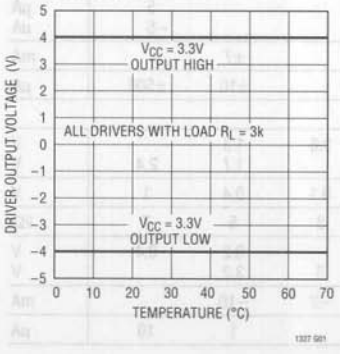
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver output unloaded and driver inputs tied high.

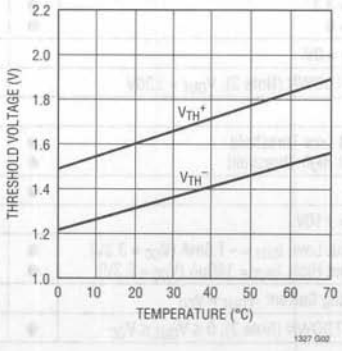
Note 3: Supply current measurement in SHUTDOWN mode is performed with $V_{ON/\overline{OFF}}$ = 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

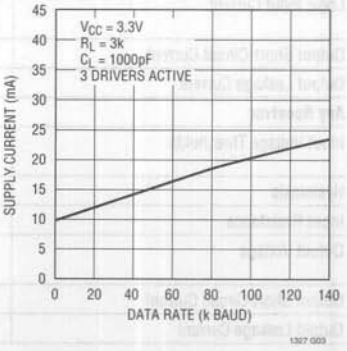
Driver Output Voltage vs Temperature



Receiver Input Thresholds vs Temperature

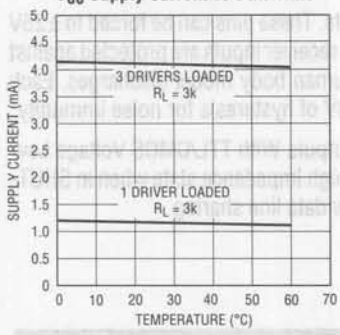


Supply Current vs Data Rate

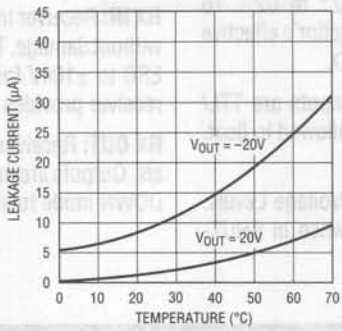


TYPICAL PERFORMANCE CHARACTERISTICS

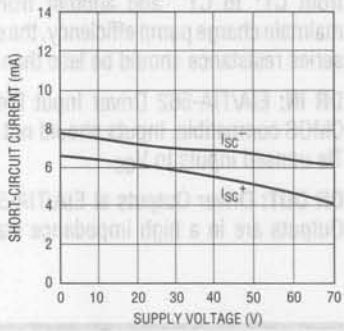
V_{CC} Supply Current vs Data Rate



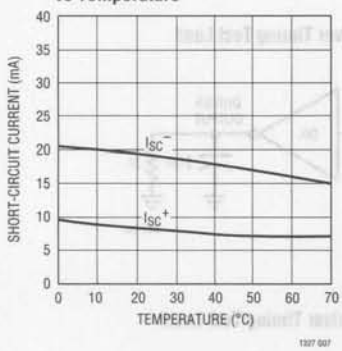
Driver Leakage in SHUTDOWN vs Temperature



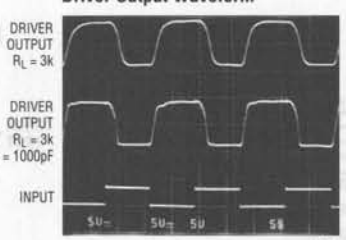
Driver Short-Circuit Current vs Supply Voltage



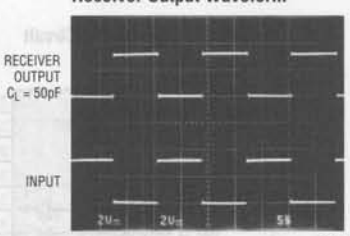
Receiver Short-Circuit Current vs Temperature



Driver Output Waveform



Receiver Output Waveform



PIN FUNCTIONS

V_{CC}: 3.3V Input Supply Pin. Supply current 0.2µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in SHUTDOWN mode which reduces the supply current to 0.2µA and places all drivers and receivers in high impedance state. This pin cannot float.

V^+: Positive Supply Output (EIA/TIA-562 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or 3.3V. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (EIA/TIA-562 Drivers). $V^- \cong -(2V_{CC} - 1.3)$. This pin requires an external capacitor C = 0.1µF for a charge storage.

PIN FUNCTIONS

C1⁺, C1⁻, C2⁺, C2⁻: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF. One from C1⁺ to C1⁻, and another from C2⁺ to C2⁻. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 20Ω.

DR IN: EIA/TIA-562 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

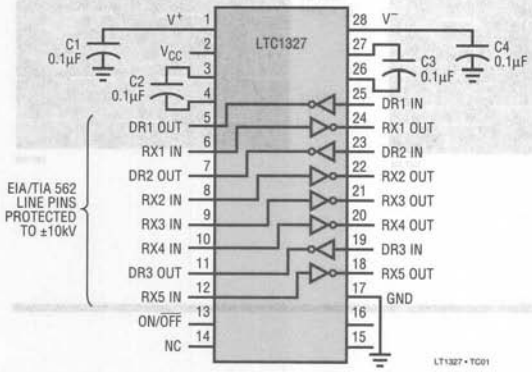
DR OUT: Driver Outputs at EIA/TIA-562 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

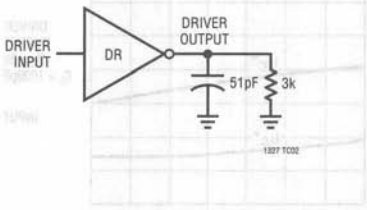
RX OUT: Receiver Outputs With TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing.

TEST CIRCUITS

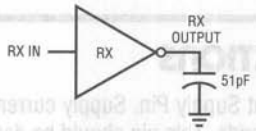
ESD Test Circuit



Driver Timing Test Load

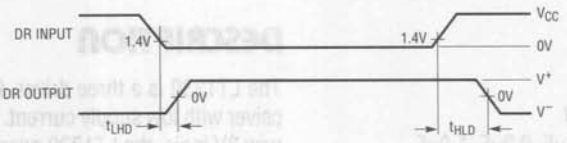


Receiver Timing Test Load

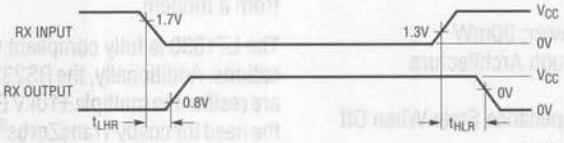


SWITCHING TIME WAVEFORMS

Driver Propagation Delay Timing



Receiver Propagation Delay Timing



APPLICATIONS INFORMATION

The LTC1327 is compatible with RS232 parts. This table shows some devices and the receiver input thresholds.

MANUFACTURER	PART NUMBER	COMPATIBLE	INPUT LOW THRESHOLD (V_{IL})			INPUT HIGH THRESHOLD (V_{IH})		
			MIN	TYP	MAX	MIN	TYP	MAX
Linear Technology	LT1080	√	0.8	1.3	–	–	1.7	2.4
	LT1137A	√	0.8	1.3	–	–	1.7	2.4
	LT1330	√	0.8	1.3	–	–	1.7	2.4
	LT1281	√	0.8	1.3	–	–	1.7	2.4
	All Others	√						
Texas Instruments	SN75189	√	0.65	1	1.25	0.9	1.3	1.6
	SN75189A	√	0.65	1	1.25	1.55	1.9	2.25
	MAX232	√	0.8	1.2	–	–	1.7	2.4
	SN75C185	√	0.65	1	1.25	1.6	2.1	2.55
Maxim	MAX232A	√	0.8	1.3	–	–	1.8	2.4
	MAX241	√	0.6	1.2	–	–	1.5	2.4
Sipex	SP232	√	0.8	1.2	–	–	1.7	2.4
	SP301	√	0.75	–	1.35	1.75	2.5	
Motorola	MC1489	√	0.75	–	1.25	1	–	1.5
	MC1489A	√	0.75	0.8	1.25	1.75	1.95	2.25
National	DS1489	√	0.75	1	1.25	1	1.25	1.5
	DS14C89A	√	0.5	–	1.9	1.3	–	2.7

5

5V RS232 Transceiver with 3V Logic Interface and One Receiver Active in SHUTDOWN

FEATURES

- **3V Logic Interface**
- ESD Protection over **±10kV**
- Uses Small Capacitors: 0.1µF, 0.2µF, 1.0µF
- One Low Power Receiver Remains Active While in SHUTDOWN
- Pin Compatible with LT1137A and LT1237
- Operates to 120k Baud
- CMOS Comparable Low Power: 30mW
- Easy PC Layout – Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Absolutely No Latchup
- 60µA Supply Current in SHUTDOWN
- Available in SO and SSOP Packages

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

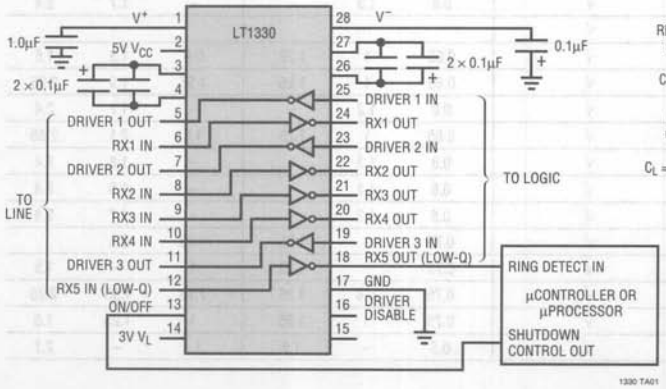
The LT1330 is a three driver, five receiver RS232 transceiver with low supply current. Designed to interface with new 3V logic, the LT1330 operates with both a 5V power supply and a 3V logic power supply. The chip may be shut down to micropower operation with one receiver remaining active to monitor RS232 inputs such as ring detect from a modem.

The LT1330 is fully compliant with all EIA RS232 specifications. Additionally, the RS232 line input and output pins are resilient to multiple ±10kV ESD strikes. This eliminates the need for costly TransZorbs® on line pins for the RS232 part.

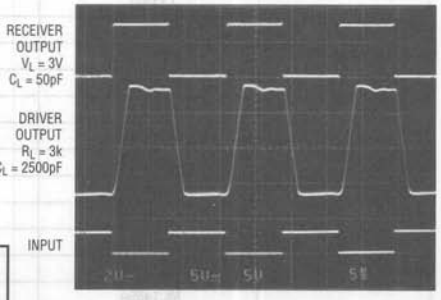
The LT1330 operates to 120k baud even driving high capacitive loads. During SHUTDOWN, driver and receiver outputs are at a high impedance state allowing devices to be paralleled.

TransZorb is a registered trademark of General Instruments, GSI

TYPICAL APPLICATION



Output Waveforms

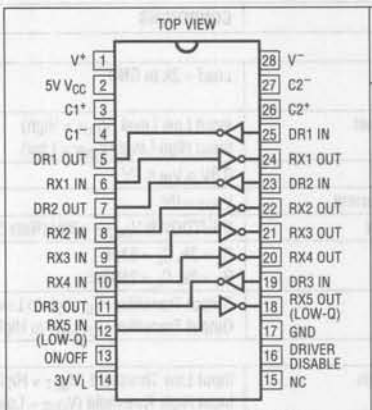


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
Supply Voltage (V_L) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... –30V to 30V
Output Voltage
  Driver ..... –30V to 30V
  Receiver ..... –0.3V to V_L + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1330I ..... –40°C to 85°C
  LT1330C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 28-LEAD CERAMIC DIP
N PACKAGE 28-LEAD PLASTIC DIP
S PACKAGE 28-LEAD SOL
G PACKAGE 28-LEAD SSOP

T_{JMAX} = 150°C, θ_{JA} = 62°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 85°C/W (S)
T_{JMAX} = 150°C, θ_{JA} = 96°C/W (G)

ORDER PART NUMBER
LT1330IJ
LT1330CJ
LT1330CN
LT1330CS
LT1330CG

Consult factory for Military grade parts.

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				7.9		V
V^- Output				–7		V
Supply Current (V_{CC})	T_A = 25°C (Note 3)			6	12	mA
		●		6	14	mA
Supply Current (V_L)	(Note 4)			0.1	1	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 5)	●		0.06	0.15	mA
	DRIVER DISABLE			3.00		mA
Supply Rise Time SHUTDOWN to Turn-On	C1 = C2 = 0.2µF, C^+ = 1.0µF, C^- = 0.1µF			0.2		ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN)	●	0.8	1.4		V
	Input High Level (Device Enabled)	●		1.4	2.4	V
ON/OFF Pin Current	0V ≤ $V_{ON/OFF}$ ≤ 5V	●	–15		80	µA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●	0.8	1.4		V
	Input High Level (Drivers Disabled)	●		1.4	2.4	V
Driver Disable Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	–10		500	µA
Oscillator Frequency	Driver Outputs Loaded R_L = 3k			130		kHz

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	Load = 3k to GND	Positive ●	5.0	7.5		V
		Negative ●		−6.3	−5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2V$	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 5)	●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF			15	30	V/µs
	R_L = 3k, C_L = 2500pF		4	15		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)			0.6	1.3	µs
	Output Transition t_{LH} Low to High			0.5	1.3	µs
Any Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)		0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)			1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 5) $0 \le V_{OUT} \le V_{CC}$	●		1	10	µA
Receivers 1, 2, 3, 4						
Output Voltage	Output Low, I_{OUT} = −1.6mA	●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_L = 3V)	●	2.7	2.9		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		−10	−20		mA
	Sourcing Current, V_{OUT} = 0V		10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7)			250	600	ns
	Output Transition t_{LH} Low to High			350	600	ns
Receiver 5 (LOW Q-Current RX)						
Output Voltage	Output Low, I_{OUT} = −500µA	●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_L = 3V)	●	2.7	2.9		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		−2	−4		mA
	Sourcing Current, V_{OUT} = 0V		2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7)			1	3	µs
	Output Transition t_{LH} Low to High			1	3	µs

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade, and $-40°C \le T_A \le 85°C$ for industrial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$ = 3V.

Note 3: Supply current is measured as the average over several charge pump burst cycles. C^+ = 1.0µF, C^- = 0.1µF, C1 = C2 = 0.2µF. All outputs are open, with all driver inputs tied high.

Note 4: V_L supply current is measured with all receiver outputs low.

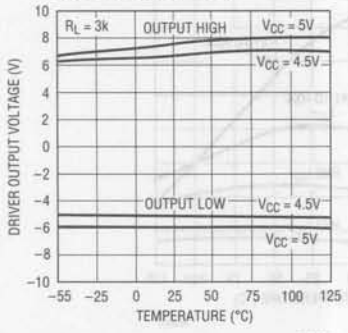
Note 5: Measurements in SHUTDOWN are performed with $V_{ON/OFF} \le 0.1V$. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE} \ge 3V$.

Note 6: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

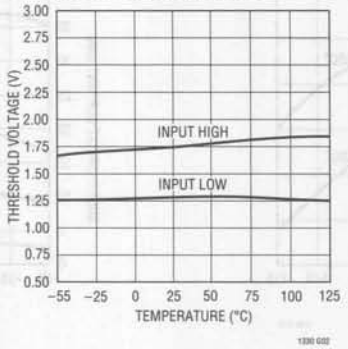
Note 7: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

TYPICAL PERFORMANCE CHARACTERISTICS

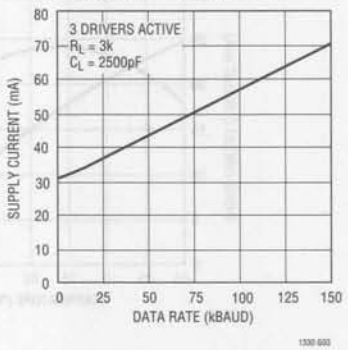
Driver Output Voltage



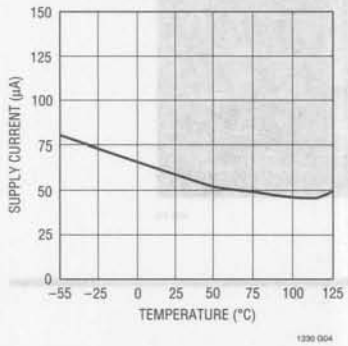
Receiver Input Thresholds



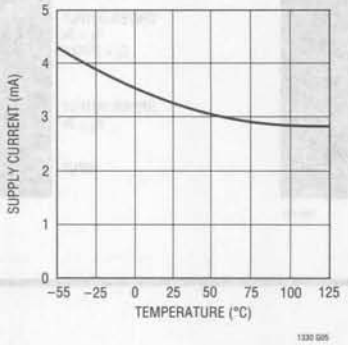
Supply Current vs Data Rate



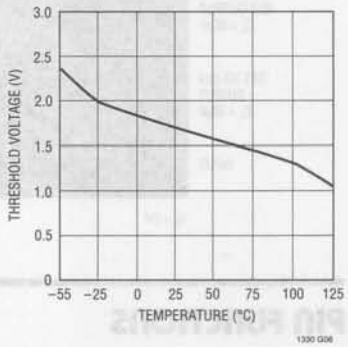
V_{CC} Supply Current in SHUTDOWN



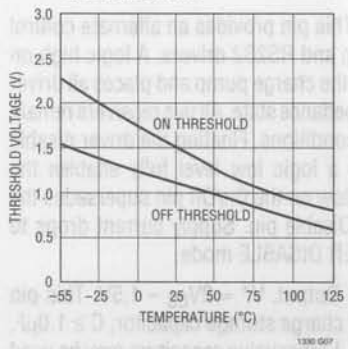
V_{CC} Supply Current in DRIVER DISABLE



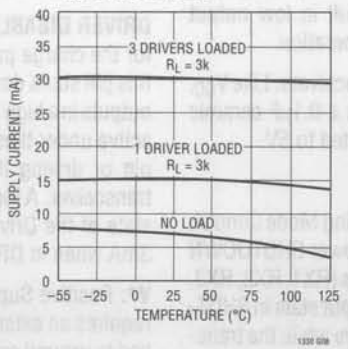
Driver Disable Threshold



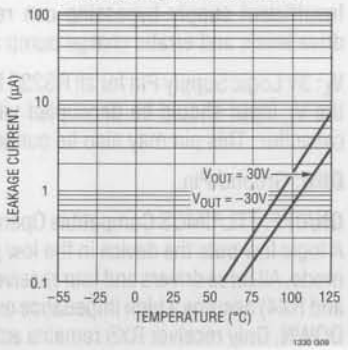
On/Off Thresholds



V_{CC} Supply Current



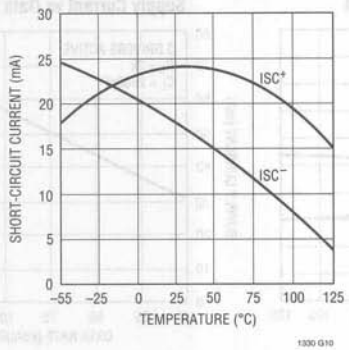
Driver Leakage in SHUTDOWN



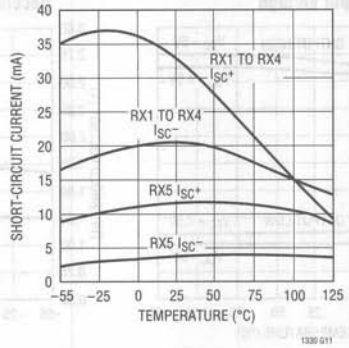
5

TYPICAL PERFORMANCE CHARACTERISTICS

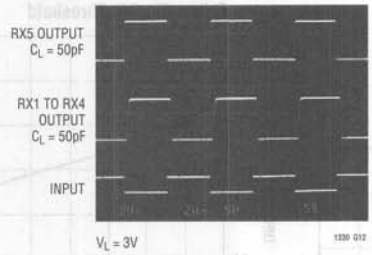
Driver Short-Circuit Current



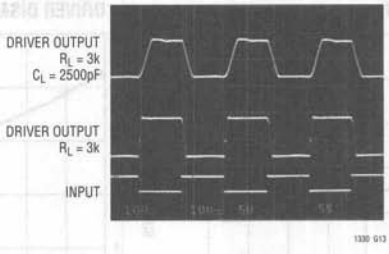
Receiver Short-Circuit Current



Receiver Output Waveforms



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

V_L: 3V Logic Supply Pin for all RS232 Receivers. Like V_{CC}, the V_L input should be decoupled with a 0.1µF ceramic capacitor. This pin may also be connected to 5V.

GND: Ground Pin.

ON/OFF: TTL/CMOS Compatible Operating Mode Control. A logic low puts the device in the low power SHUTDOWN mode. All three drivers and four receivers (RX1, RX2, RX3, and RX4) assume a high impedance output state in SHUTDOWN. Only receiver RX5 remains active while the transceiver is in SHUTDOWN. The transceiver consumes only 60µA of supply current while in SHUTDOWN. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all driver outputs in a high impedance state. All five receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. A logic low on the On/Off pin supersedes the state of the Driver Disable pin. Supply current drops to 3mA when in DRIVER DISABLE mode.

V^+: Positive Supply Output. $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor, $C \geq 1.0\mu F$, tied to ground or 5V. Larger value capacitors may be used

PIN FUNCTIONS

to reduce supply ripple. The ratio of the capacitors on V^+ and V^- should be greater than 5 to 1.

V^-: Negative Supply Output. $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor, $C \geq 0.1\mu F$. See the Applications Information section for guidance in choosing filter capacitors for V^+ and V^-.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs require two external capacitors, $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well, although ceramic capacitors may be used with a minimal reduction in charge pump compliance.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Unused inputs should be connected to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RX OUT, are fully short-circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

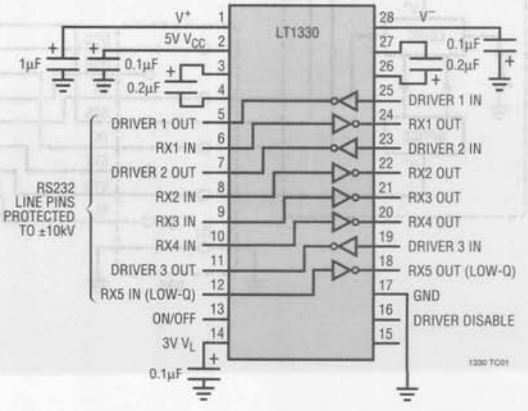
LOW Q-CURRENT RX IN: Low Power Receiver Input. This special receiver remains active when the part is in SHUTDOWN mode, consuming typically 60µA. This receiver has the same 5k input impedance and ±10kV ESD protection characteristics as the other receivers.

LOW Q-CURRENT RX OUT: Low Power Receiver Output. This pin produces the same TTL/CMOS output voltage levels as receivers RX1, RX2, RX3, and RX4 with slightly decreased speed and short-circuit current. Data rates to 120k baud are supported by this receiver.

ESD PROTECTION

The RS232 line inputs of the LT1330 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1330 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V_L, V^+, V^-, and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



APPLICATIONS INFORMATION

Storage Capacitor Selection

The V^+ and V^- storage capacitors must be chosen carefully to insure low ripple and stable operation. The LT1330 charge pump operates in a power efficient Burst Mode™. When storage capacitor voltage drops below a preset threshold, the oscillator is gated on until V^+ and V^- are boosted up to levels exceeding a second threshold. The oscillator then turns off, and current is supplied from the V^+ and V^- storage capacitors.

The V^- potential is monitored to control charge pump operation. It is therefore important to insure lower V^+ ripple than V^- ripple, or erratic operation of the charge pump will result. Proper operation is insured in most applications by choosing the V^+ filter capacitor to be at least 5 times the V^- filter capacitor value. If V^+ is more heavily loaded than V^-, a larger ratio may be needed.

The V^- filter capacitor should be selected to obtain low ripple when the drivers are loaded, forcing the charge pump into continuous mode. A minimum value 0.1µF is suggested.

Do not attempt to reduce V^- ripple when the charge pump is in discontinuous Burst Mode™ operation. The ripple in this mode is determined by internal comparator thresholds. Larger storage capacitor values increase the burst period, and do not reduce ripple amplitude.

Power Saving Operational Modes

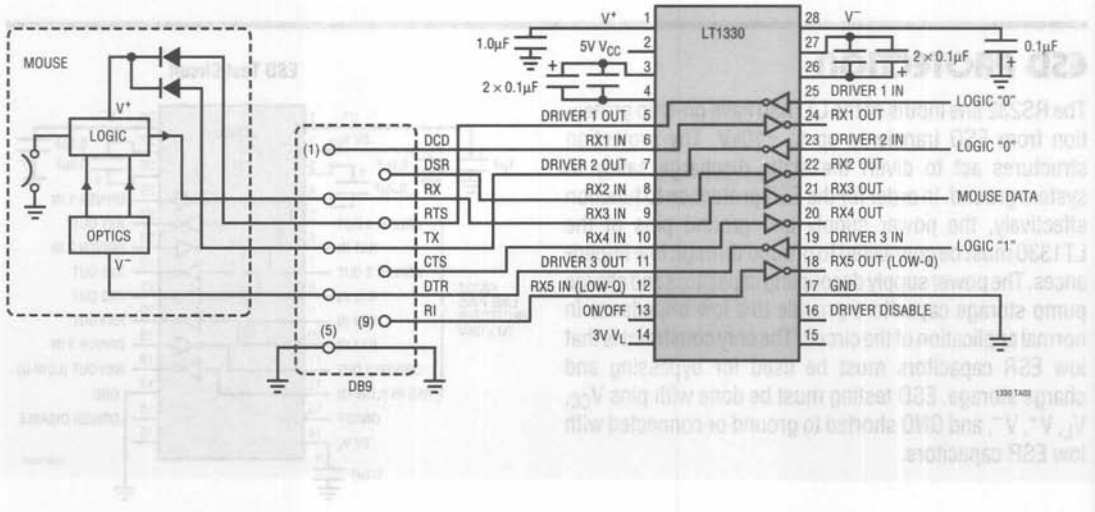
The LT1330 has both SHUTDOWN and DRIVER DISABLE operating modes. These operating modes can optimize power consumption based upon applications needs.

The On/Off shutdown control turns off all circuitry except for Low-Q RX5. When RX5 detects a signal, this information can be used to wake up the system for full operation.

If more than one line must be monitored, the DRIVER DISABLE mode provides a power efficient operating option. The DRIVER DISABLE mode turns off the charge pump and RS232 drivers, but keeps all five receivers active. Power consumption in DRIVER DISABLE mode is 3mA from V_{CC}.

Burst Mode is a trademark of Linear Technology Corporation

Typical Mouse Driving Application



3V RS562 or 5V/3V RS232 Transceiver with One Receiver Active in SHUTDOWN

FEATURES

- **RS232 Compatible 3V Operation**
- **3V Logic Interface**
- **ESD Protection Over ±10kV**
- One Low Power Receiver Remains Active While in SHUTDOWN
- 60μA Supply Current in SHUTDOWN
- Low Power DRIVER DISABLE Mode
- Uses Small Capacitors: 0.1μF, 0.2μF
- Operates to 120k Baud
- CMOS Comparable Low Power: 60mW
- Easy PC Layout: Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When OFF or Powered Down

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LT1331 is a 3-driver, 5-receiver RS232 transceiver designed for 3V and mixed 3V/5V systems. Receivers operate from 3V logic supply V_L, while the on-board charge pump and drivers operate from 5V or 3V supply V_{CC}.

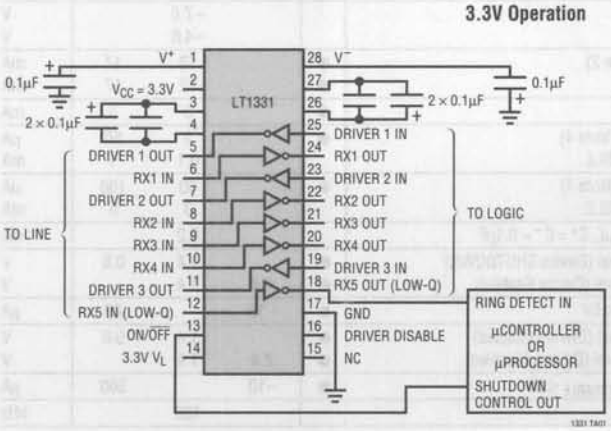
The transceiver has two SHUTDOWN modes. One mode disables the drivers and the charge pump, the other shuts down all circuitry except for one low power receiver which can be used for ring detection. The V_{CC} supply may be shut down while in ring detection mode. While shut down, the drivers and receivers assume high impedance output states.

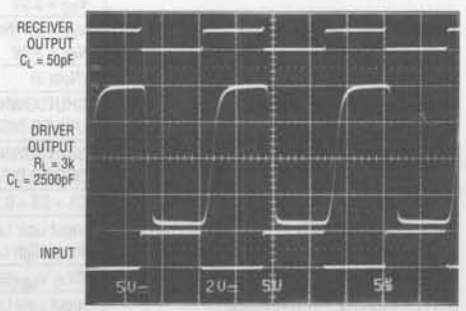
The LT1331 is fully compliant with all EIA-RS232 specifications when V_{CC} = 5V. If V_{CC} = 3V, output drive levels are compatible with all known interface circuits. Special bipolar construction techniques protect the drivers and receivers beyond the fault conditions stipulated for RS232. The RS232 I/O pins are resilient to multiple ±10kV ESD strikes. An advanced driver output stage operates up to 120k baud while driving heavy capacitive loads.

5

TYPICAL APPLICATION

3.3V Operation

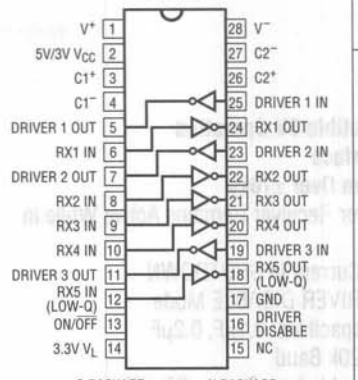




ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Supply Voltage (V_L) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^+ to V^-
  Receiver ..... 30V to –30V
  ON/$\overline{OFF}$ ..... –0.3V to V_{CC} + 0.3V
  DRIVER DISABLE ..... –0.3V to V_{CC} + 0.3V
Output Voltage
  Driver ..... –30V to 30V
  Receiver ..... –0.3V to V_L + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1331C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LT1331CG
LT1331CN
LT1331CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output	V_{CC} = 5V			8.6		V
	V_{CC} = 3.3V			5.5		V
V^- Output	V_{CC} = 5V			–7.0		V
	V_{CC} = 3.3V			–4.8		V
Supply Current (V_{CC})	V_{CC} = 5V (Note 2)	●		12	17	mA
	V_{CC} = 3.3V	●		12	17	mA
Supply Current (V_L)	(Note 3)	●		3	5	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 4)	●		2	50	µA
	DRIVER DISABLE			0.1	1	mA
Supply Current When OFF (V_L)	SHUTDOWN (Note 4)	●		60	100	µA
	DRIVER DISABLE			3	5	mA
Supply Rise Time, SHUTDOWN to Turn-On	C1 = C2 = 0.2µF, C^+ = C^- = 0.1µF			0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN)	●		1.4	0.8	V
	Input High Level (Device Enabled)	●	2.4	1.4		V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/\overline{OFF}}$ ≤ 5V	●	–15		80	µA
DRIVER DISABLE Pin Thresholds	Input Low Level (Drivers Enabled)	●		1.4	0.8	V
	Input High Level (Drivers Disabled)	●	2.4	1.4		V
DRIVER DISABLE Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	–10		500	µA
Oscillator Frequency				130		kHz

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing, Positive	V_{CC} = 5V, R_L = 3k	●	5.0	6.5		V
	V_{CC} = 3.3V, R_L = 3k		3.7	4.0		V
Output Voltage Swing, Negative	V_{CC} = 5V, R_L = 3k	●		–6.0	–5.0	V
	V_{CC} = 3.3V, R_L = 3k			–3.3	–2.7	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	0.8V ≤ V_{IN} ≤ 2V	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)	●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF			15	30	V/µs
	R_L = 3k, C_L = 2500pF			6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)			0.6	1.3	µs
	Output Transition t_{LH} Low to High			0.5	1.3	µs
Any Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)	●	0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)	●		1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Receivers 1 Through 4						
Output Voltage	Output Low, I_{OUT} = –1.6mA	●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_L = 3.3V)	●	2.0	2.4		V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC}			–20	–10	mA
	Sourcing Current, V_{OUT} = 0V		10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)			250	600	ns
	Output Transition t_{LH} Low to High			350	600	ns
Output Leakage Current	SHUTDOWN (Note 4) 0 ≤ V_{OUT} ≤ V_{CC}	●		1	10	µA
Receiver 5 (Low Q-Current RX)						
Output Voltage	Output Low, I_{OUT} = –500µA	●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_L = 3V)	●	2.0	2.4		V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC}			–4	–2	mA
	Sourcing Current, V_{OUT} = 0V		2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)			1	3	µs
	Output Transition t_{LH} Low to High			1	3	µs

The ● denotes specifications which apply over the full operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade).

Note 1: Testing done at V_{CC} = 5V, V_L = 3.3V, and $V_{ON/\overline{OFF}}$ = 3V, unless otherwise stated.

Note 2: Supply current is measured as the average over several charge pump cycles. C^+ = 1µF, C^- = 0.1µF, C1 = C2 = 0.2µF. All outputs are open with all driver inputs tied high.

Note 3: V_L supply current is measured with all receiver outputs high.

Note 4: Supply current and leakage current measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}}$ ≤ 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ ≥ 3V.

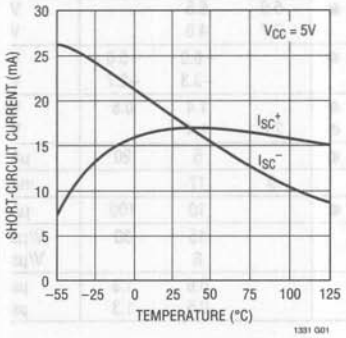
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.0V and t_{LH} = 1.7V to 0.8V).

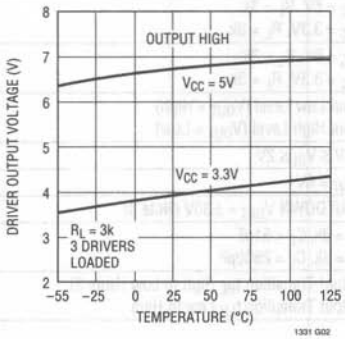
5

TYPICAL PERFORMANCE CHARACTERISTICS

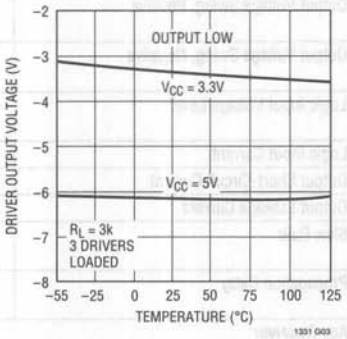
Driver Short-Circuit Current



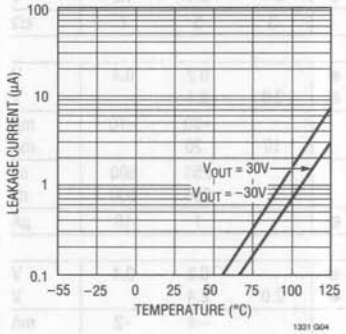
Driver Output Voltage



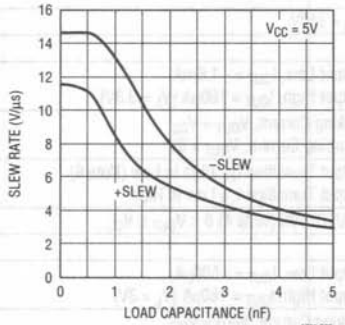
Driver Output Voltage



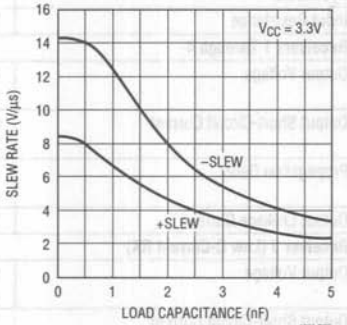
Driver Leakage in SHUTDOWN



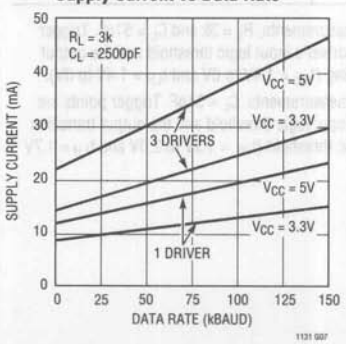
Slew Rate vs Load Capacitance



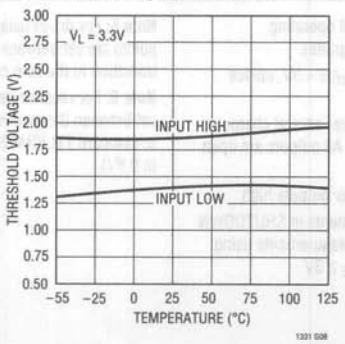
Slew Rate vs Load Capacitance



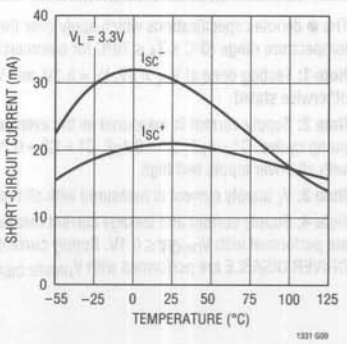
Supply Current vs Data Rate



Receiver Input Thresholds



Receiver Short-Circuit Current



PIN FUNCTIONS

V_{CC}: Power Supply for Charge Pump and Drivers. Proper circuit operation is insured for V_{CC} = 3V to 6V. V_{CC} = 5V operation gives full RS232 compliant performance, 3V operation results in lower driver output amplitude. The V_{CC} pin should be decoupled with a 0.1µF ceramic capacitor.

V_L: Power Supply for Receivers. This pin should be powered to the same voltage as the logic circuits connected to the receiver outputs, either 5V or 3V. The V_L pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground.

ON/$\overline{OFF}$: A TTL/CMOS Compatible Operating Mode Control. A logic low puts the device in the SHUTDOWN mode. All drivers and four of the receivers go to a high impedance state, and the V_{CC} supply may be turned off. A logic high fully enables the transceiver.

DRIVER DISABLE: A logic high shuts down the charge pump, placing all drivers in a high impedance state. All receivers remain active. Floating the pin, or driving it to a logic low, fully enables the transceiver. A low voltage on the ON/$\overline{OFF}$ pin supersedes the state of the DRIVER DISABLE control.

V^+: Positive Supply Output. $V^+ \cong 2V_{CC} - 1.5V$. This pin requires an external capacitor for charge storage, chosen to minimize ripple to acceptable levels. A minimum size of 0.1µF is recommended.

V^-: Negative Supply Output. $V^- \cong -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor, chosen to minimize ripple on V^-. A minimum value of 0.1µF is recommended.

$C1^+$,$C1^-$,$C2^+$,$C2^-$: These pins require two external capacitors $C \geq 0.2\mu F$. One from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω. Low ESR tantalum capacitors work well in this application, small value ceramic capacitors may also be used with minimal reduction in charge pump compliance.

DRIVER IN: RS232 Driver Inputs. Inputs are TTL/CMOS compatible. Tie unused inputs to V_{CC}.

DRIVER OUT: RS232 Driver Outputs. Outputs are in a high impedance state when in SHUTDOWN, DRIVER DISABLE, or V_{CC} = 0V. Outputs are fully short-circuit protected from V^- + 30V to V^+ – 30V. Although the outputs are protected, short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges. Output levels of –3.3V to 4V are achieved when the circuit is operated with V_{CC} = 3.3V.

RX IN: Receiver Inputs with 0.4V of Hysteresis for Noise Immunity. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges.

RX OUT: Receiver Outputs. RX1 through RX4 outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RX OUT, are fully short-circuit protected to ground, V_{CC}, or V_L. Output voltage levels are determined by the choice of power supply V_L.

LOW-Q RX IN: Low Power Receiver Input. This receiver remains active in SHUTDOWN mode, consuming only 60µA from supply V_L. This receiver has the same input and protection characteristics as receivers RX1 through RX4.

LOW-Q RX OUT: Low Power Receiver Output. This pin produces the same output levels as standard receivers, with slightly decreased speed and short-circuit current.

APPLICATIONS INFORMATION

Power Saving Operational Modes

The LT1331 has both SHUTDOWN and DRIVER DISABLE operating modes. These operating modes can optimize power consumption based upon applications needs.

The SHUTDOWN control turns off all circuitry except for Low-Q RX5. RX5 operates entirely from the V_L power supply, so the power consumption from V_{CC} drops to zero. The V_{CC} power supply may be turned off while in SHUTDOWN, which may allow greater power savings in some systems. When RX5 detects a signal, this information can be used to wake up the system for full operation.

If more than one line must be monitored, the DRIVER DISABLE mode provides a power efficient operating option. The DRIVER DISABLE mode turns off the charge pumps and RS232 drivers, but keeps all five receivers active. Power consumption in DRIVER DISABLE mode is 3mA from V_L and less than 100µA from V_{CC}.

Mixed 5V/3V Operation

When operated with V_{CC} = 5V and V_L = 3.3V supplies, the RS232 drivers meet or exceed all RS232 or V.28 communication interface standards. Data rates up to 120k baud are supported, and all standard RS232 compatible mice may be driven by the LT1331.

3V Operation

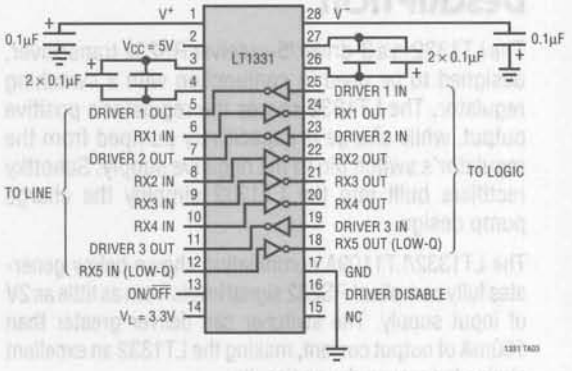
V_{CC} = 3.3V operation of the LT1331 results in lower driver output swing than with V_{CC} = 5V. The driver output swing, when operated with V_{CC} = 3.3V, is guaranteed to be at least –2.7V to 3.7V, with typical swing being –3.3V to 4V. This insures compatibility with all commonly used RS232 and RS562 interface circuits. Table 1 summarizes the receiver input threshold specifications for RS232 circuits from many manufacturers.

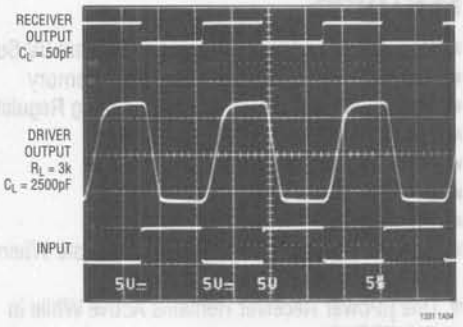
Table 1. Commonly Used RS232 Interface Circuit Receiver Thresholds

MANUFACTURER	PART NUMBER	COMPATIBLE	INPUT LOW THRESHOLD			INPUT HIGH THRESHOLD		
			MIN	TYP	MAX	MIN	TYP	MAX
Linear Technology	LT1080	✓	0.8	1.3	–	–	1.7	2.4
	LT1137A	✓	0.8	1.3	–	–	1.7	2.4
	LT1330	✓	0.8	1.3	–	–	1.7	2.4
	LT1281	✓	0.8	1.3	–	–	1.7	2.4
	All Others	✓						
Texas Instruments	SN75189	✓	0.65	1.0	1.25	0.9	1.3	1.6
	SN75189A	✓	0.65	1.0	1.25	1.55	1.9	2.25
	MAX232	✓	0.8	1.2	–	–	1.7	2.4
	SN75C185	✓	0.65	1.0	1.25	1.6	2.1	2.55
Maxim	MAX232A	✓	0.8	1.3	–	–	1.8	2.4
	MAX241	✓	0.6	1.2	–	–	1.5	2.4
Sipex	SP232	✓	0.8	1.2	–	–	1.7	2.4
	SP301	✓	0.75	–	1.35	1.75	–	2.5
Motorola	MC1489	✓	0.75	–	1.25	1.0	–	1.5
	MC1489A	✓	0.75	0.8	1.25	1.75	1.95	2.25
National	DS1489	✓	0.75	1.0	1.25	1.0	1.25	1.5
	DS14C89A	✓	0.5	–	1.9	1.3	–	2.7

TYPICAL APPLICATION

Mixed 5V/3V Supply Operation



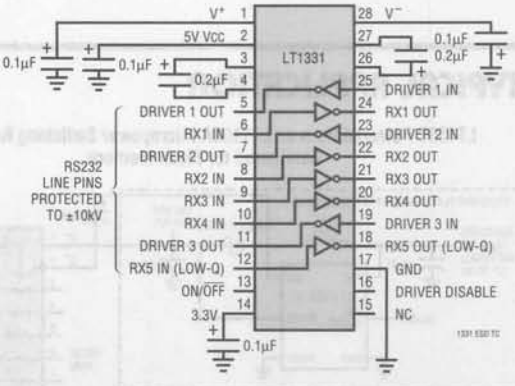


5

ESD PROTECTION

The RS232 line inputs of the LT1331 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1331 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V_L, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



Wide Supply Range Low Power RS232 Transceiver with 12V VPP Output for Flash Memory

FEATURES

- Generates Full RS232 Signal Levels from 3V Supply
- 12V VPP Output Available for Flash Memory
- Useful with a Wide Variety of Switching Regulators
- Low Supply Current: $I(V_{CC})$ = 1mA
- Wide Supply Range: $2V \leq V_{CC} \leq 6V$
- ESD Protection Over ±**10kV**
- Operates to 120k Baud
- Outputs Assume a High Impedance State When Off or Powered Down
- One µPower Receiver Remains Active While in SHUTDOWN
- Flowthrough Architecture Eases PC Board Layout
- 40µA Supply Current in SHUTDOWN
- Absolutely No Latch-Up
- Available in SO and SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers
- Mouse Driver Circuits

DESCRIPTION

The LT1332 is a 3-driver/5-receiver RS232 transceiver, designed to be used in conjunction with a switching regulator. The LT1332 shares the regulator's positive output, while charge is capacitively pumped from the regulator's switch pin to the negative supply. Schottky rectifiers built into the LT1332 simplify the charge pump design.

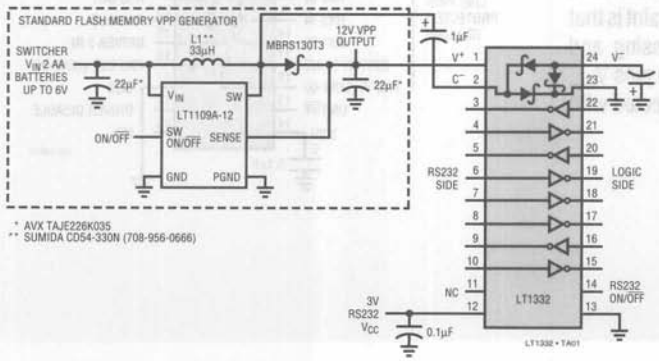
The LT1332/LT1109A combination shown below generates fully compliant RS232 signal levels from as little as 2V of input supply. The switcher can deliver greater than 100mA of output current, making the LT1332 an excellent choice for mouse driver circuits.

Advanced driver output stages operate up to 120k baud while driving heavy capacitive loads. New ESD structures on chip make the LT1332 resilient to multiple ±10kV strikes, eliminating costly transient suppressors.

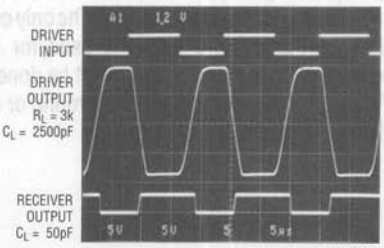
A shutdown pin disables the transceiver except for one receiver which remains active for detecting incoming RS232 signals. When shut down, the disabled drivers and receivers assume high impedance output states.

TYPICAL APPLICATION

LT1332 Powered from an LT1109A Micropower Switching Regulator Configured for Flash Memory



Output Waveforms



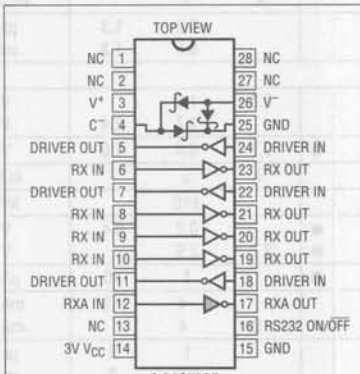
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... −13.2V
C^- ..... −15V
Input Voltage
  Driver ..... V^+ to V^-
  Receiver ..... 30V to −30V
Output Voltage
  Driver ..... 30V to −30V
  Receiver ..... −0.3V to V_{CC} + 0.3V

Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

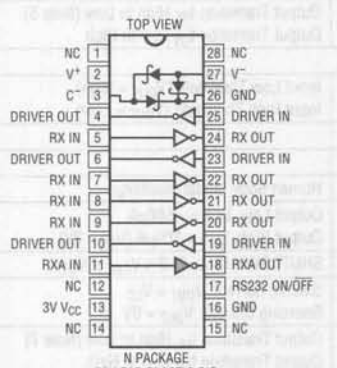


G PACKAGE
28-LEAD SSOP

T_{JMAX} = 150°C, θ_{JA} = 96°C/W

ORDER PART NUMBER

LT1332CG

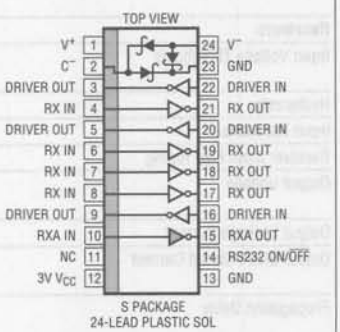


N PACKAGE
28-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 56°C/W

ORDER PART NUMBER

LT1332CN



S PACKAGE
24-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 80°C/W

ORDER PART NUMBER

LT1332CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
Supply Current I(V^+)	(Note 3)			0.3	0.8	mA
Supply Current I(V^-)	(Note 3)			−0.6	−1.0	mA
Supply Current I(V_{CC})	(Note 3)			1.0	1.5	mA
Supply Current When OFF I(V_{CC})	(Note 4)	●		0.04	0.10	mA
				0.04	0.07	mA
Supply Current When OFF I(V^+)	V_{CC} = 3V, V^+ = 8V, $V_{ON/\overline{OFF}}$ = 0.1V			0.10	0.20	mA
Supply Current When OFF I(V^-)	V_{CC} = 3V, V^- = −8V, $V_{ON/\overline{OFF}}$ = 0.1V			0.10	0.20	mA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device Shut Down)	●		0.7	0.3	V
	Input High Level (Device Enabled)	●	1.3	0.6		V
ON/$\overline{OFF}$ Pin Current	$0V \le V_{ON/\overline{OFF}} \le 5V$	●	–15		80	µA
Drivers						
Output Voltage Swing	R_L = 3k to GND Positive	●	5.0	6.6		V
	Negative	●		–7.0	–5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2.0V$	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			±17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V, $V_{ON/\overline{OFF}}$ = 0.1V	●		10	100	µA
Driver Output ESD Rating	Human Body Model Discharge			±10		kV
Slew Rate	R_L = 3k, C_L = 51pF			15	30	V/µs
	R_L = 3k, C_L = 2500pF		4	6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)			0.6	1.3	µs
	Output Transition t_{LH} Low to High			0.5	1.3	µs
Receivers						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)		0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)			1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance			3	5	7	kΩ
Receiver Input ESD Rating	Human Body Model Discharge			±10		kV
Output Voltage	Output Low, I_{OUT} = –500µA	●		0.2	0.4	V
	Output High, I_{OUT} = 100µA (V_{CC} = 3V)	●	2.7	2.9		V
Output Leakage Current	SHUTDOWN (Note 6) $0 \le V_{OUT} \le V_{CC}$	●		1	10	µA
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			–4	–2	mA
	Sourcing Current, V_{OUT} = 0V		2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7)			1	3	µs
	Output Transition t_{LH} Low to High			0.6	3	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing is done at V_{CC} = 3V, V^+ = 8V, V^- = –8V, and $V_{ON/\overline{OFF}}$ = 3V.

Note 3: Supply current is measured with all driver inputs tied high.

Note 4: Supply current measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}}$ = 0.1V, V^+ = 0V, V^- = 0V.

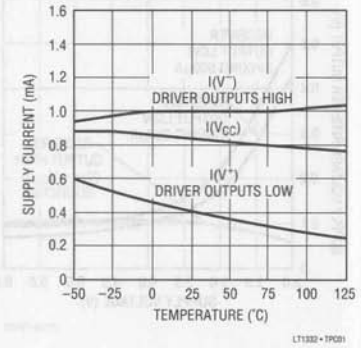
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: Receiver RXA (Pins 10 and 15, S Package) remains functioning in SHUTDOWN.

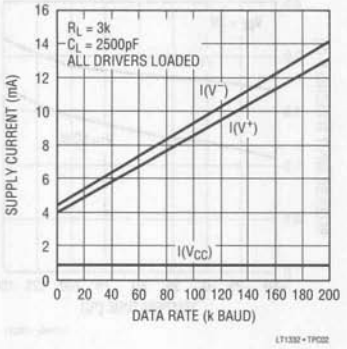
Note 7: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{LH} = 1.3V to 2.4V and t_{HL} = 1.7V to 0.8V).

TYPICAL PERFORMANCE CHARACTERISTICS

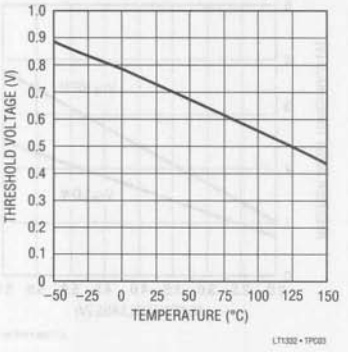
Unloaded Supply Current vs Temperature



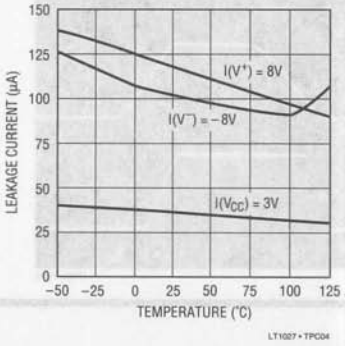
Supply Current vs Data Rate



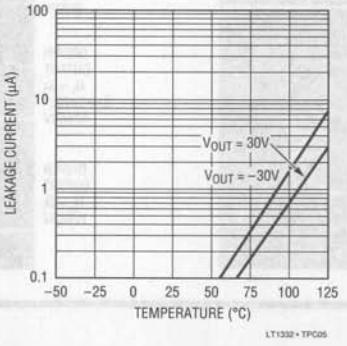
ON/OFF Threshold vs Temperature



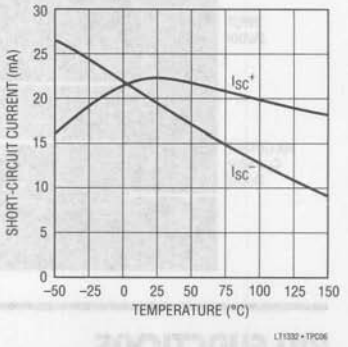
Leakage Current in Shutdown vs Temperature



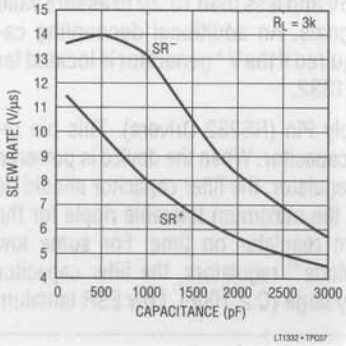
Driver Leakage in Shutdown vs Temperature



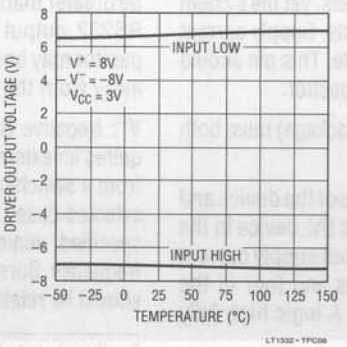
Driver Short-Circuit Current vs Temperature



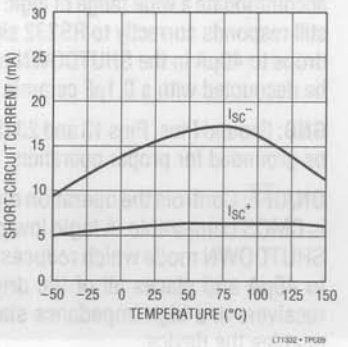
Slew Rate vs Load Capacitance



Driver Output Voltage vs Temperature



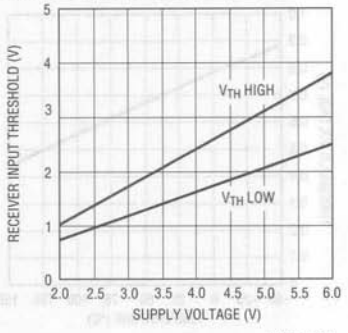
Receiver Short-Circuit Current vs Temperature



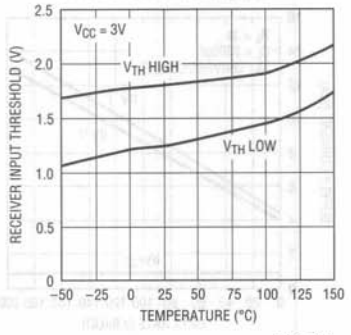
5

TYPICAL PERFORMANCE CHARACTERISTICS

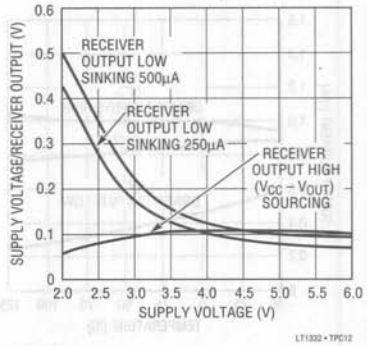
Receiver Input Thresholds vs Supply Voltage



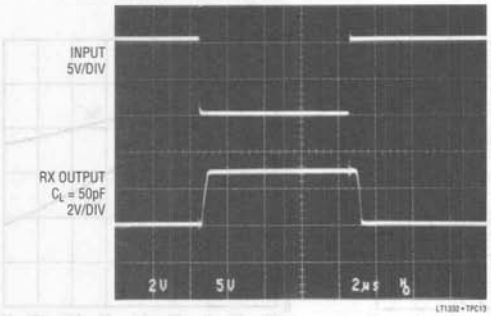
Receiver Input Thresholds vs Temperature



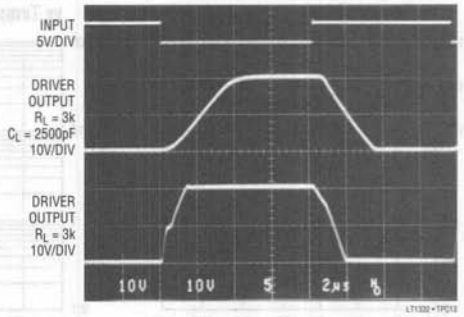
Receiver Output Voltage vs Supply Voltage



Receiver Output Waveforms



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: Input Supply Pin. V_{CC} can vary from 2V to 6V to accommodate a wide range of logic levels, yet the system still responds correctly to RS232 signals. Supply current drops to 40µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pins. Pins 13 and 23 (S Package) must both be grounded for proper operation.

ON/$\overline{OFF}$: Controls the operation mode of the device and is CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to 40µA and places all of the drivers and four of the receivers in a high impedance state. A logic high fully enables the device.

V^+: Positive Supply Input (RS232 Drivers). V^+ should be greater than 6.5V and less than 13.2V to assure valid RS232 output signals. An additional decoupling capacitor may be required if the V^+ generator is located far away from the LT1332.

V^-: Negative Supply Pin (RS232 Drivers). This pin requires an external capacitor. When the device is powered from a switching regulator, the filter capacitor should be selected based on the maximum tolerable ripple for the specified minimum regulator on time. For some low frequency Burst Mode™ regulators, the filter capacitor should be relatively large ($C \geq 10\mu F$). Low ESR tantalum

Burst Mode™ is a trademark of Linear Technology Corporation

PIN FUNCTIONS

capacitors work well in this application. When V^- is powered from an external supply, the filter capacitor can be considerably smaller ($C \geq 0.1\mu F$). Ceramic capacitors work well under these conditions. V^- should be greater than –13.2V and less than –6.5V.

C^-: Commutating Capacitor Input. When the LT1332 is used with a switching regulator, a charge pump capacitor should be connected from the regulator's switch pin to the C^- pin. Make the external capacitor 1µF or larger with low effective series resistance to maintain good charge pump efficiency. Low ESR tantalum capacitors (ESR < 2Ω) work well in this application. The C^- pin should be left open when V^- is powered from an external supply.

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible, with threshold set to 1.2V. Unused inputs should not float; tie them to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode, or V_{CC} = 0V. Outputs are fully short-circuit protected from V^- + 30V to V^+ – 30V with the power on, off or SHUTDOWN. Typical breakdowns are ±45V. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Although the outputs are protected, short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±5V to ±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. The receiver thresholds are specified at V_{CC} = 3V. When V_{CC} varies from 2V to 6V, the lower threshold increases about 3V. Regardless of these shifts, the device provides accurate data from valid RS232 input signals. A graph in the performance characteristics section shows typical changes in the thresholds. The active receiver (RXA, Pin 10, S Package) remains functional in SHUTDOWN.

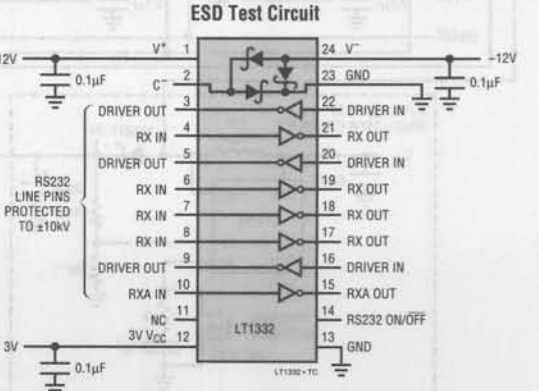
RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance stage when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power on, off or in SHUTDOWN mode. The active receiver (RXA, Pin 15, S Package) remains functional in SHUTDOWN.

5

ESD PROTECTION

The RS232 line inputs of the LT1332 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1332 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal applications of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



APPLICATIONS INFORMATION

Operation with a Switching Regulator

The LT1332 is designed to be powered from an external switching regulator which may be used elsewhere for power conditioning. In a typical application, the LT1332 shares the regulator's positive output, while charge is capacitively pumped from the regulator's switch pin to the negative supply. Schottky rectifiers built into the LT1332 simplify the charge pump design. When used with a micropower switcher like the LT1109A, the Burst Mode™ operation of the charge pump resembles the switching characteristics of the LT1237 and similar devices.

The V^- supply is not directly regulated. The circuit relies on cross regulation and the regulator's minimum duty cycle to control V^-. Select the C^- and V^- storage capacitors so that when the regulator operates at minimum duty cycle, sufficient charge will transfer to the V^- storage cap to maintain a voltage of at least –6.5V.

While only 0.1µF ceramic decoupling capacitors are needed on the positive supply inputs, low ESR tantalum capacitors should be used in the charge pump to reduce voltage losses. The C^- capacitor should be at least 1µF and the V^- capacitor should be 5 to 10 times bigger. As a rule of thumb, make the V^- capacitor at least $1/DC_{MIN}$ times bigger than the C^- capacitor where DC_{MIN} is the regulator's minimum duty cycle. Using large values for the V^- capacitor reduces ripple on the V^- supply.

Multiple Transceivers

The circuit in Figure 1 demonstrates how the LT1332 may be used with different types of switching regulators. Four LT1332s are powered from a single PWM DC/DC converter using an LT1172. Even with all twelve drivers heavily loaded (R_L = 3k, C_L = 2500pF), the circuit generates fully compliant RS232 signals at 120k baud.

Operations with External Supplies

When external RS232 supplies are available (6.5V ≤ V^+ ≤ 13.2V, –13.2V ≤ V^- ≤ –6.2V) the LT1332 can be used as a stand-alone unit. Capacitor selection is consider-

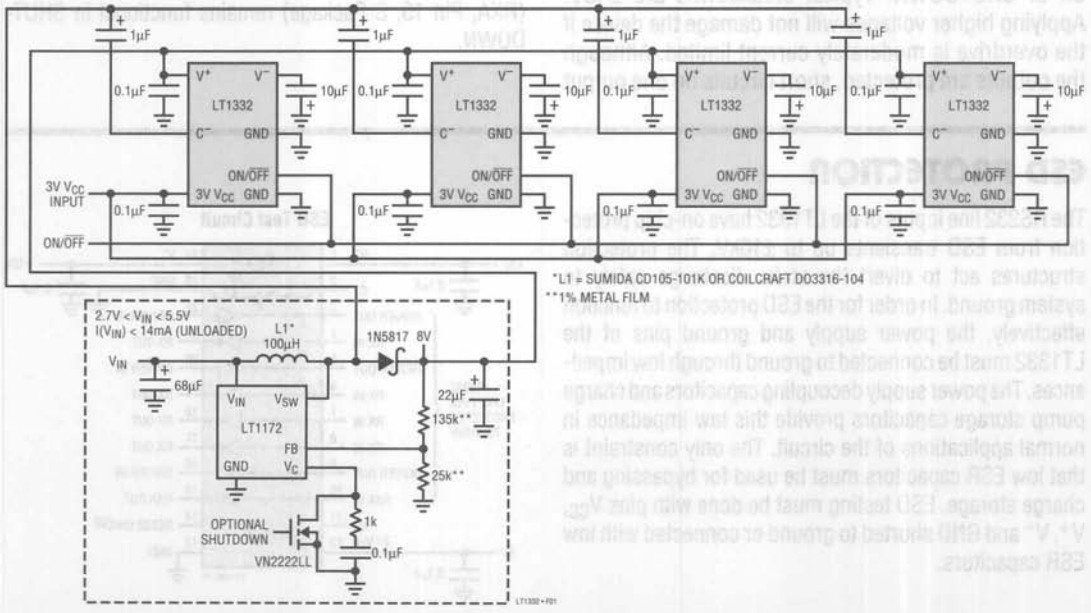


Figure 1. Multiple LT1332s Powered from a Single LT1172 DC/DC Converter

APPLICATIONS INFORMATION

ably simpler. Decouple V^+ and V^- with 0.1µF ceramic capacitors.

Shutdown Control

The LT1332 has an ON/$\overline{OFF}$ pin that controls the device's mode of operation. With the ON/$\overline{OFF}$ pin high and the device operated unloaded, the LT1332 draws 1mA of supply current. With the ON/$\overline{OFF}$ pin low, the device enters micropower shutdown mode in which the current drawn from V_{CC} drops to typically 40µA. If the power applied to V^+ and V^- remains on in shutdown, there will be approximately 100µA of leakage from each supply. If these supplies drop to zero, leakage current also drops to zero. In shutdown mode one receiver remains active which may be useful for detecting start-up signals for the transceiver.

5

5V Low Power RS232 3-Driver/5-Receiver Transceiver

FEATURES

- **Low Supply Current: 300μA**
- 1μA Supply Current in SHUTDOWN
- **ESD Protection: Over ±10kV**
- Operates from a Single 5V Supply
- Uses Small Capacitors: 0.1μF
- Operates to 120k Baud
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V without Damage
- Pin Compatible with LT1137A and LT1237
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

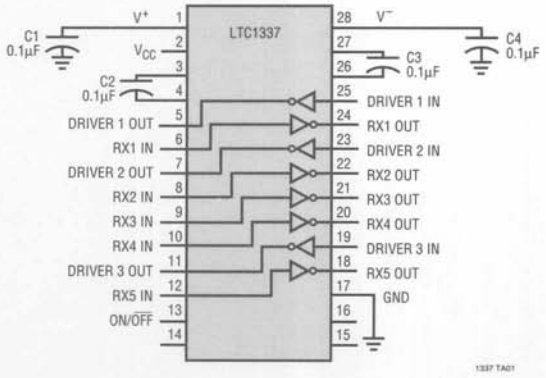
The LTC1337 is a 3-driver/5-receiver RS232 transceiver with very low supply current. In the no load condition, the supply current is only 300μA. The charge pump only requires four 0.1μF capacitors and can supply up to 12mA of extra current to power external circuitry.

In SHUTDOWN mode, the supply current is further reduced to 1μA. All RS232 outputs assume a high impedance state in SHUTDOWN and with the power off.

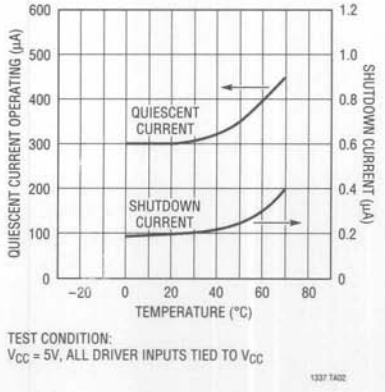
The LTC1337 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120k baud with a 1000pF//3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with SHUTDOWN



Supply Current



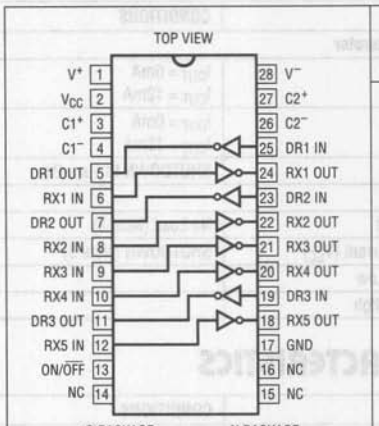
TEST CONDITION:
V_{CC} = 5V, ALL DRIVER INPUTS TIED TO V_{CC}

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  On/$\overline{\text{Off}}$ Pin ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  Commercial (LTC1337C) ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD PLASTIC SOL

$T_{JMAX} = 125°C$, $\theta_{JA} = 96°C/W$ (G)
$T_{JMAX} = 125°C$, $\theta_{JA} = 56°C/W$ (N)
$T_{JMAX} = 125°C$, $\theta_{JA} = 85°C/W$ (S)

ORDER PART NUMBER
LTC1337CG
LTC1337CN
LTC1337CS

Consult factory for Industrial and Military grade parts.

5

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	R_L = 3k to GND	Positive ●	5.0	7.0		V
	R_L = 3k to GND	Negative ●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	$V_{IN} = 5V$	●			5	µA
	$V_{IN} = 0$	●			−5	µA
Output Short-Circuit Current	$V_{OUT} = 0V$			±10		mA
Output Leakage Current	SHUTDOWN, $V_{OUT} = \pm 20V$ (Note 3)	●		10	500	µA
Any Receiver						
Input Voltage Thresholds	Input Low Threshold	●	0.8	1.3		V
	Input High Threshold	●		1.7	2.4	V
Hysteresis		●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$		3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ ($V_{CC} = 5V$)	●		0.2	0.4	V
	Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 5V$)	●	3.5	4.8		V
Output Short-Circuit Current	Sourcing Current, $V_{OUT} = 0$		15	20		mA
	Sinking Current, $V_{OUT} = V_{CC}$		−15	−40		mA
Output Leakage Current	SHUTDOWN, $0 \le V_{OUT} \le V_{CC}$ (Note 3)	●		1	10	µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V+ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 12mA			7.5		V
V⁻ Output Voltage	I_{OUT} = 0mA			−8.0		V
	I_{OUT} = 12mA			−6.5		V
Supply Rise Time	SHUTDOWN to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.3	0.8	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 3)	●		1	10	µA
On/$\overline{\text{Off}}$ Threshold Low		●		1.4	0.8	V
On/$\overline{\text{Off}}$ Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		2	4		V/µs
Driver Propagation Delay	t_{HLD} (Figure 1)	●		2	3	µs
(TTL to RS232)	t_{LHD} (Figure 1)	●		2	3	µs
Receiver Propagation Delay	t_{HLR} (Figure 2)	●		0.3	0.6	µs
(RS232 to TTL)	t_{LHR} (Figure 2)	●		0.2	0.6	µs

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C).

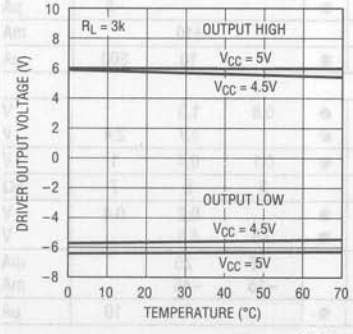
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded and driver inputs tied high.

Note 3: Supply current and leakage measurements in SHUTDOWN are performed with V_{ON} = 0V.

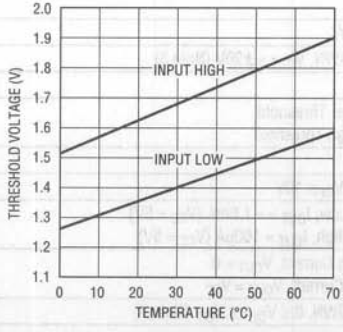
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage



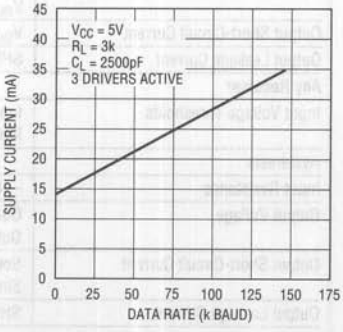
1337 G01

Receiver Input Thresholds



1337 G02

Supply Current vs Data Rate

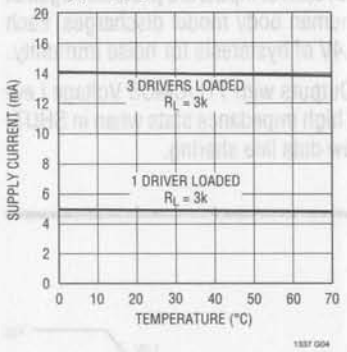


1337 G03

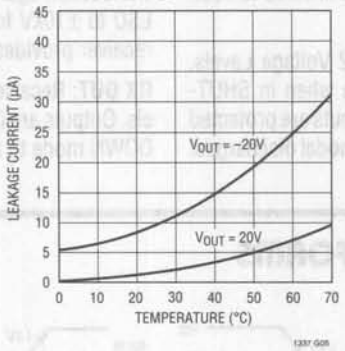
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

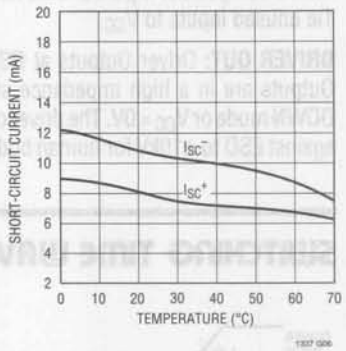
V_{CC} Supply Current



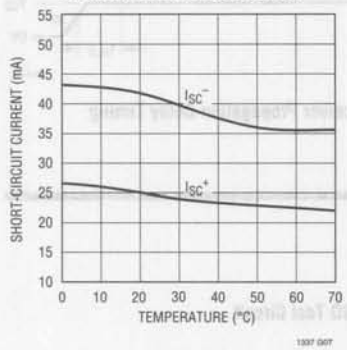
Driver Leakage in SHUTDOWN



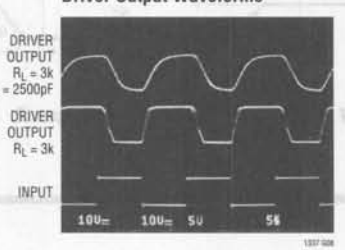
Driver Short-Circuit Current



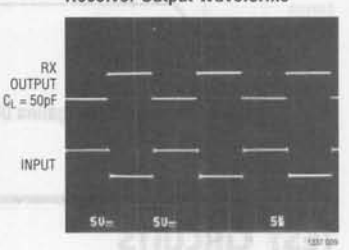
Receiver Short-Circuit Current



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current less than 1µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to less than 1µA and places all drivers and receivers in high impedance state. This pin cannot float.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or 5V. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong (2V_{CC} - 1.5V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF. One from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 50Ω.

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PIN FUNCTIONS

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing.

SWITCHING TIME WAVEFORMS

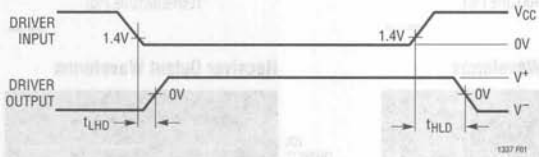


Figure 1. Driver Propagation Delay Timing

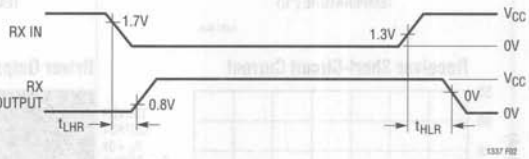


Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

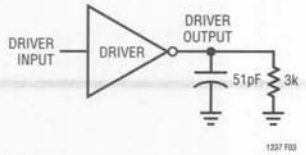


Figure 3. Driver Timing Test Load

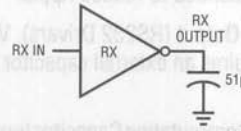
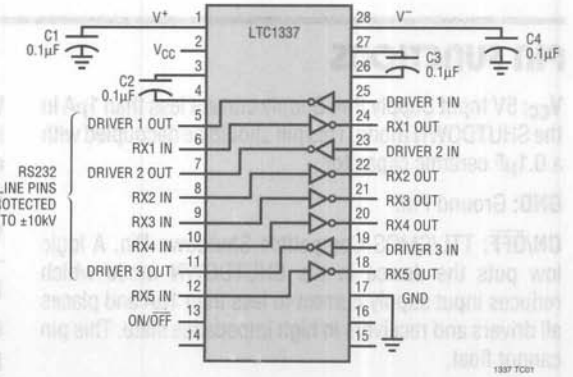


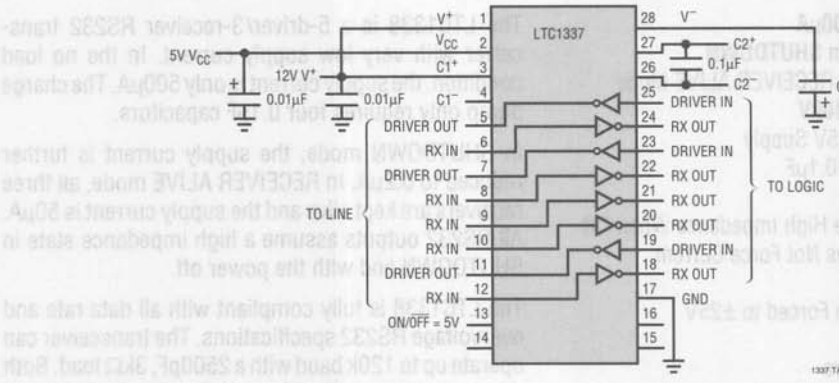
Figure 4. Receiver Timing Test Load

ESD Test Circuit

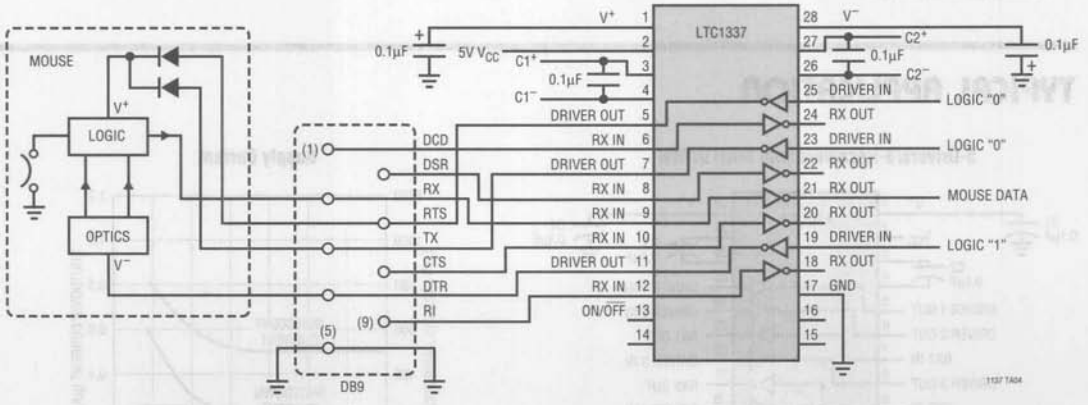


TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



Typical Mouse Driving Application



5

5V Low Power RS232 5-Driver/3-Receiver Transceiver

FEATURES

- **Low Supply Current: 500μA**
- **0.2μA Supply Current in SHUTDOWN**
- 50μA Supply Current in RECEIVER ALIVE Mode
- **ESD Protection Over ±10kV**
- Operates from a Single 5V Supply
- Uses Small Capacitors: 0.1μF
- Operates to 120k Baud
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Flowthrough Architecture

APPLICATIONS

- Battery-Powered Modems
- Battery-Powered DCE
- Notebook Computers
- Palmtop Computers

DESCRIPTION

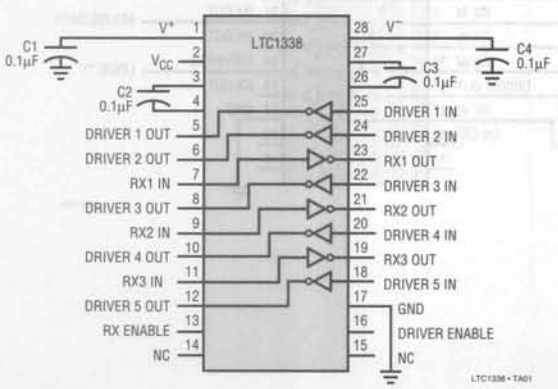
The LTC1338 is a 5-driver/3-receiver RS232 transceiver with very low supply current. In the no load condition, the supply current is only 500μA. The charge pump only requires four 0.1μF capacitors.

In SHUTDOWN mode, the supply current is further reduced to 0.2μA. In RECEIVER ALIVE mode, all three receivers are kept alive and the supply current is 50μA. All RS232 outputs assume a high impedance state in SHUTDOWN and with the power off.

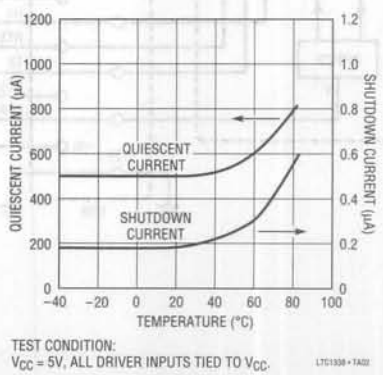
The LTC1338 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120k baud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

5-Drivers/3-Receivers with SHUTDOWN



Supply Current



TEST CONDITION:
V_{CC} = 5V, ALL DRIVER INPUTS TIED TO V_{CC}.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V

Input Voltage

- Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
- Receiver ..... $-25V$ to $25V$
- Driver/Receiver Enable Pin ..... $-0.3V$ to $V_{CC} + 0.3V$

Output Voltage

- Driver ..... $-25V$ to $25V$
- Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$

Short Circuit Duration

- V^+ ..... 30 sec
- V^- ..... 30 sec
- Driver Output ..... Indefinite
- Receiver Output ..... Indefinite

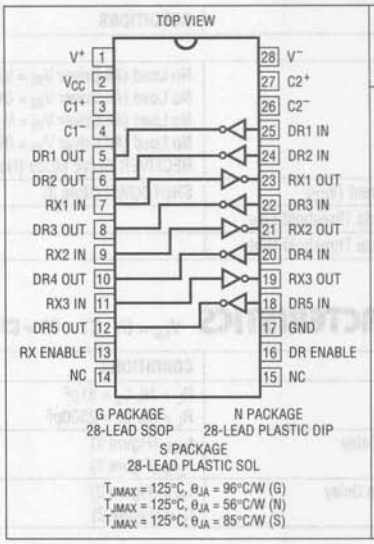
Operating Temperature Range

- Commercial (LTC1338C) ..... 0°C to 70°C
- Industrial (LTC1338I) ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1338CG
LTC1338CN
LTC1338CS
LTC1338IG
LTC1338IN
LTC1338IS

Consult factory for Military grade parts.

5

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1μF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$0 \le V_{IN} \le V_{CC}$		●			±5	μA
Output Short-Circuit Current	V_{OUT} = 0V				±12		mA
Output Leakage Current	SHUTDOWN, V_{OUT} = ±20V (Note 3)		●		±10	±500	μA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$			3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA (V_{CC} = 5V)		●		0.2	0.4	V
	Output High, I_{OUT} = 160μA (V_{CC} = 5V)		●	3.5	4.8		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−15	−40		mA
Output Leakage Current	SHUTDOWN, $0 \le V_{OUT} \le V_{CC}$ (Note 3)		●		1	10	μA
Power Supply Generator							
V^+ Output Voltage	I_{OUT} = 0mA				8.0		V
	I_{OUT} = 12mA				7.5		V
V^- Output Voltage	I_{OUT} = 0mA				−8.0		V
	I_{OUT} = −12mA				−7.0		V
Supply Rise Time	SHUTDOWN to Turn-On				0.2		ms

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
V_{CC} Supply Current	No Load (All Driver V_{IN} = V_{CC})(Note 2) 0°C ≤ T_A ≤ 70°C			0.5	1.0	mA
	No Load (All Driver V_{IN} = 0V)(Note 2) 0°C ≤ T_A ≤ 70°C			1.0	1.5	mA
	No Load (All Driver V_{IN} = V_{CC})(Note 2) –40°C ≤ T_A ≤ 85°C			0.5	1.5	mA
	No Load (All Driver V_{IN} = 0V)(Note 2) –40°C ≤ T_A ≤ 85°C			1.0	2.0	mA
	RECEIVER ALIVE Mode (Note 4)	●		50	80	µA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 3)	●		0.2	10	µA
Driver/Receiver Enable Threshold Low		●		1.4	0.8	V
Driver/Receiver Enable Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.2	0.8	µs

The ● denotes specifications which apply over the operating temperature range of 0°C to 70°C or –40°C to 85°C.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

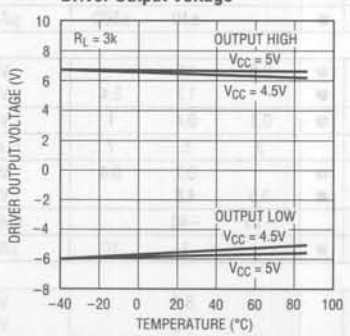
Note 2: Supply current is measured with driver and receiver outputs unloaded. The $V_{DRIVER\ ENABLE}$ and $V_{RECEIVER\ ENABLE}$ = V_{CC}.

Note 3: Supply current and leakage current measurements in SHUTDOWN are performed with $V_{DRIVER\ ENABLE}$ and $V_{RECEIVER\ ENABLE}$ = 0V.

Note 4: Supply current measurement in RECEIVER ALIVE mode is performed with $V_{DRIVER\ ENABLE}$ = 0V and $V_{RECEIVER\ ENABLE}$ = V_{CC}.

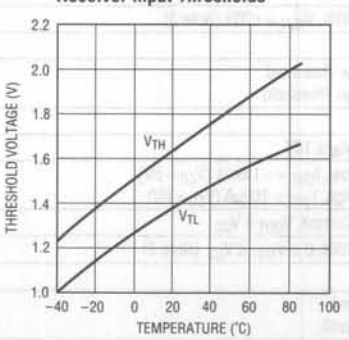
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage



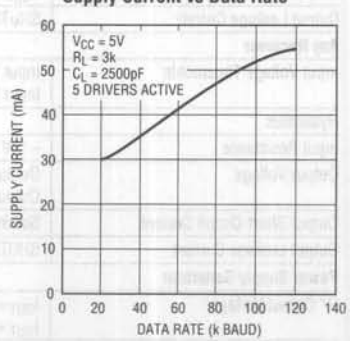
LTC1338 • TPC01

Receiver Input Thresholds



LTC1338 • TPC02

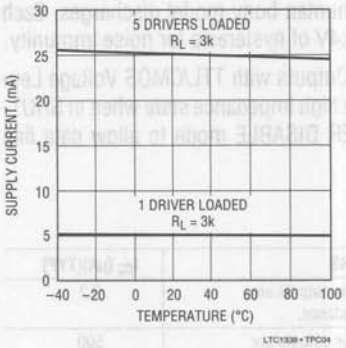
Supply Current vs Data Rate



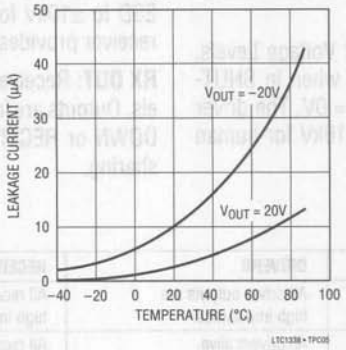
LTC1338 • TPC03

TYPICAL PERFORMANCE CHARACTERISTICS

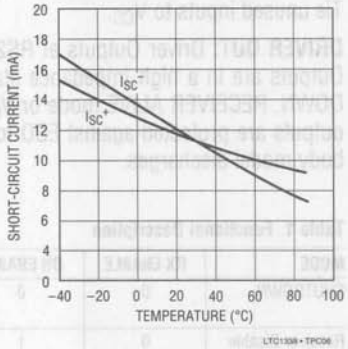
V_{CC} Supply Current



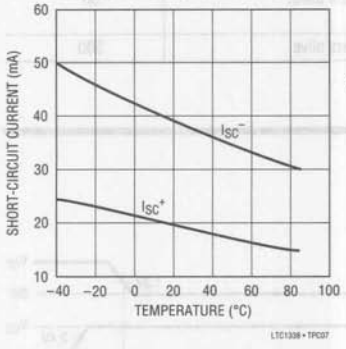
Driver Leakage in Shutdown



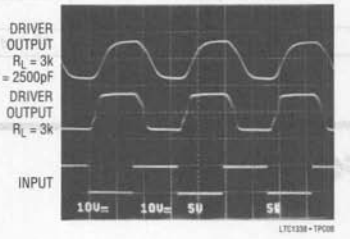
Driver Short-Circuit Current



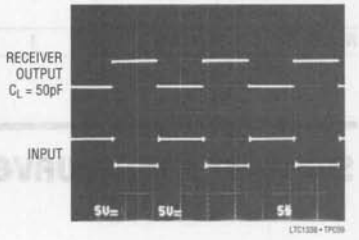
Receiver Short-Circuit Current



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current less than 0.2µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

RECEIVER ENABLE: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its functional description. This pin can not float.

DRIVER ENABLE: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its functional description. This pin can not float.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or 5V. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong 2V_{CC} - 1.5V$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 20Ω.

PIN FUNCTIONS

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN, RECEIVER ALIVE mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN or RECEIVER DISABLE mode to allow data line sharing.

Table 1. Functional Description

MODE	RX ENABLE	DR ENABLE	DRIVERS	RECEIVERS	I_{CC} (µA)(TYP)
SHUTDOWN	0	0	All driver outputs are high impedance.	All receiver outputs are high impedance.	0.2
Receiver Disable	0	1	All drivers alive.	All receiver outputs are high impedance.	500
RECEIVER ALIVE	1	0	All driver outputs are high impedance.	All receivers alive.	50
Normal	1	1	All drivers alive.	All receivers alive.	500

SWITCHING TIME WAVEFORMS

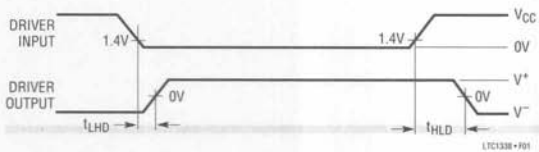


Figure 1. Driver Propagation Delay Timing

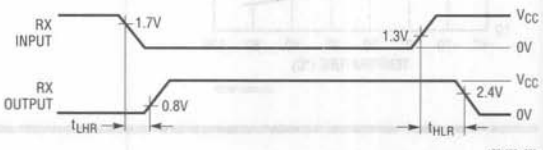
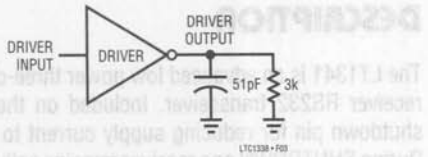


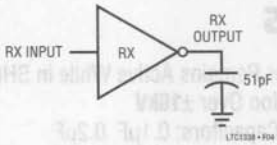
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

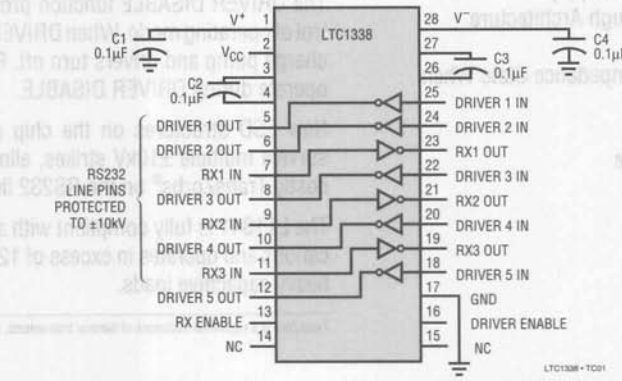
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



5

5V RS232 Transceiver with One Receiver Active in SHUTDOWN

FEATURES

- One Receiver Remains Active While in SHUTDOWN
- ESD Protection Over ±**10kV**
- Uses Small Capacitors: 0.1µF, 0.2µF
- 60µA Supply Current in SHUTDOWN
- Pin Compatible with LT1137A
- Operates to 120k Baud
- CMOS Comparable Low Power: 60mW
- Operates from a Single 5V Supply
- Easy PC Layout: Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Absolutely No Latch-Up
- Available in SSOP Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LT1341 is an advanced low power three-driver, five-receiver RS232 transceiver. Included on the chip is a shutdown pin for reducing supply current to near zero. During SHUTDOWN one receiver remains active to detect incoming RS232 signals, for example, to wake up a system. All other receivers and the drivers assume high impedance states during SHUTDOWN.

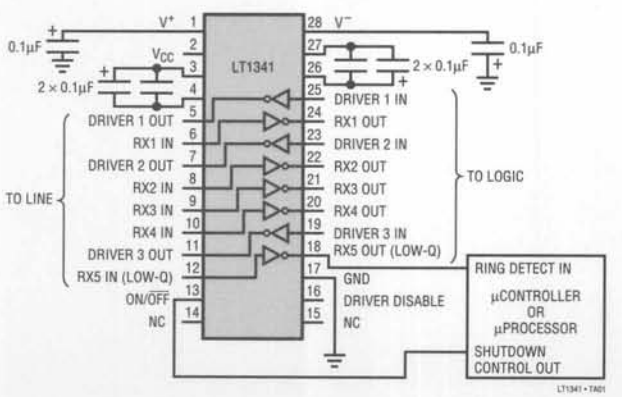
The DRIVER DISABLE function provides additional control of operating mode. When DRIVER DISABLE is high the charge pump and drivers turn off. Receivers continue to operate during DRIVER DISABLE.

New ESD structures on the chip allow the LT1341 to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins.

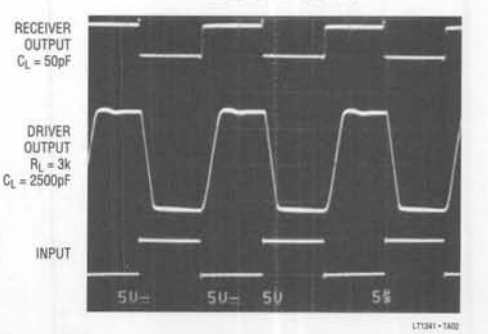
The LT1341 is fully compliant with all EIA RS232 specifications and operates in excess of 120k baud even driving heavy capacitive loads.

TransZorb is a registered trademark of General Instruments, GSI

TYPICAL APPLICATION



Output Waveforms

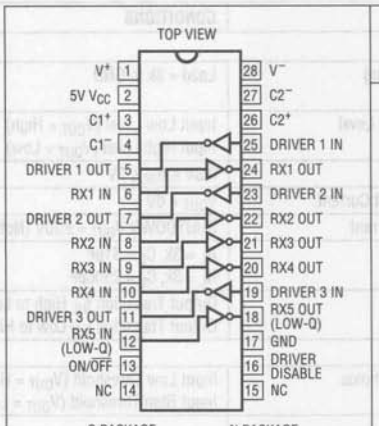


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^+ to V^-
  Receiver ..... 30V to –30V
Output Voltage
  Driver ..... –30V to 30V
  Receiver ..... –0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1341C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD SOL

T_{JMAX} = 125°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LT1341CG
LT1341CN
LT1341CS

Consult factory for Industrial and Military grade parts.

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ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				8.6		V
V^- Output				–7		V
Supply Current (V_{CC})	(Note 3)			14	17	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 4)	●		0.06	0.150	mA
	DRIVER DISABLE			3		mA
Supply Rise Time SHUTDOWN to Turn-On	C1 = C2 = 0.2µF, C+ = C– = 0.1µF			0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN)	●		1.4	0.8	V
	Input High Level (Device Enabled)	●	2.4	1.4		V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/\overline{OFF}}$ ≤ 5V	●	–15		80	µA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●		1.4	0.8	V
	Input High Level (Drivers Disabled)	●	2.4	1.4		V
Driver Disable Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	–10		500	µA
Oscillator Frequency				130		kHz

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5	7.3		V
		Negative	●		−6.5	−5	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2V$		●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			±9	±17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 4)		●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF				15	30	V/µs
	R_L = 3k, C_L = 2500pF				6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)				0.6	1.3	µs
	Output Transition t_{LH} Low to High				0.5	1.3	µs
Any Receiver							
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)			0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)				1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$		●		1	10	µA
Receivers 1 Through 4							
Output Voltage	Output Low, I_{OUT} = −1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)		●	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$				−20	−10	mA
	Sourcing Current, V_{OUT} = 0V			10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				250	600	ns
	Output Transition t_{LH} Low to High				350	600	ns
Receiver 5 (Low-I_Q RX)							
Output Voltage	Output Low, I_{OUT} = −500µA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)		●	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$				−4	−2	mA
	Sourcing Current, V_{OUT} = 0V			2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				1	3	µs
	Output Transition t_{LH} Low to High				1	3	µs

The ● denotes specifications which apply over the full operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/\overline{OFF}}$ = 3V.

Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = 0.1\mu F$, C1 = C2 = 0.2µF. All outputs are open with all driver inputs tied high.

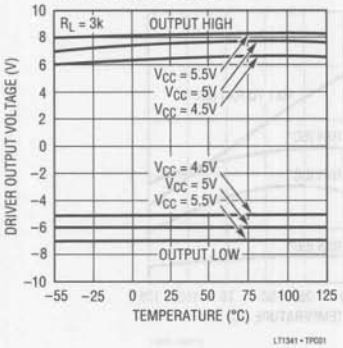
Note 4: Supply current and leakage measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}} \le 0.1V$. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE} \ge 3V$.

Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

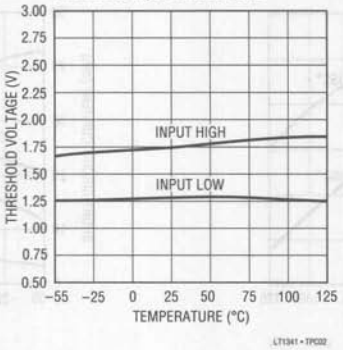
Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

TYPICAL PERFORMANCE CHARACTERISTICS

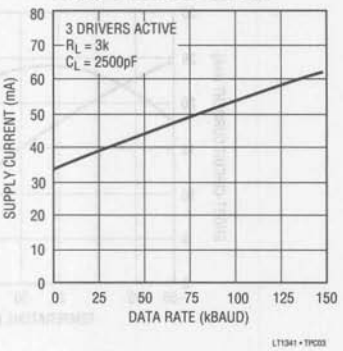
Driver Output Voltage



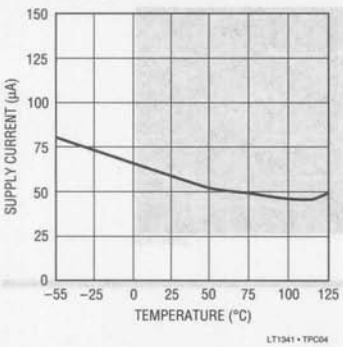
Receiver Input Thresholds



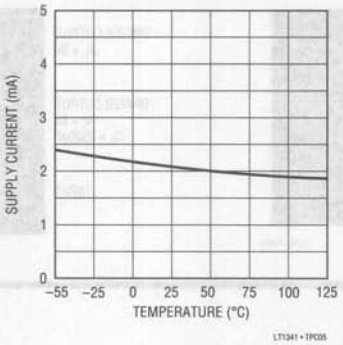
Supply Current vs Data Rate



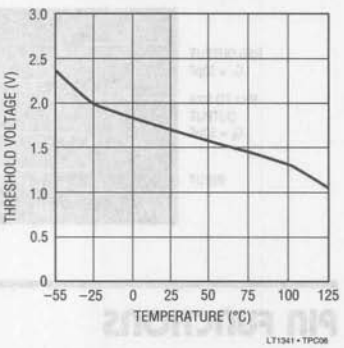
Supply Current in SHUTDOWN



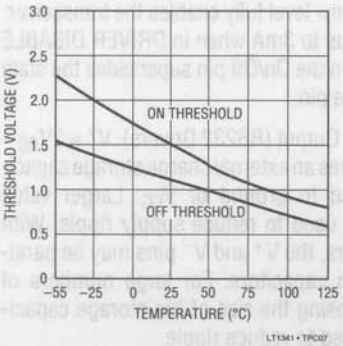
Supply Current in DRIVER DISABLE



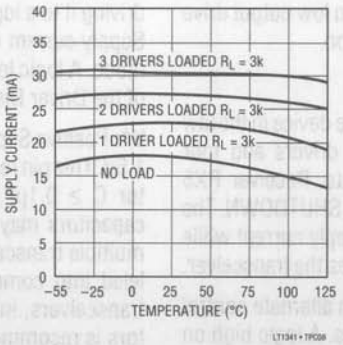
Driver Disable Threshold



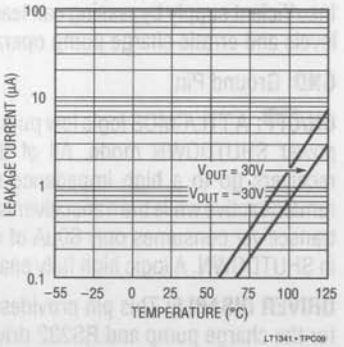
On/$\overline{\text{Off}}$ Thresholds



Supply Current



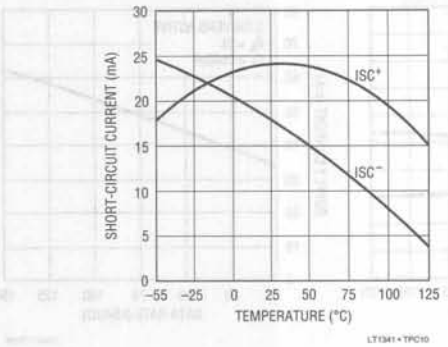
Driver Leakage in SHUTDOWN



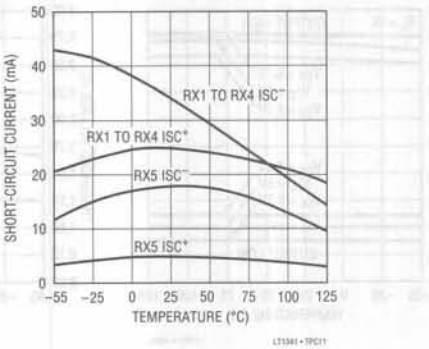
5

TYPICAL PERFORMANCE CHARACTERISTICS

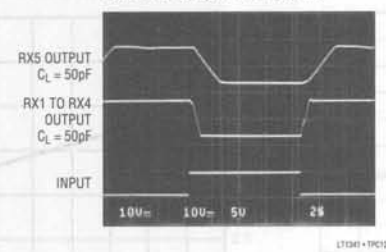
Driver Short-Circuit Current



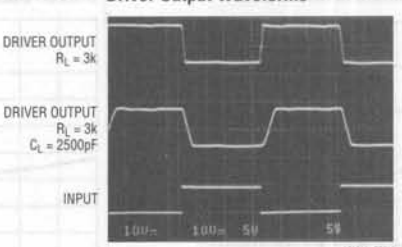
Receiver Short-Circuit Current



Receiver Output Waveforms



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can lead to low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/$\overline{OFF}$: A TTL/CMOS logic low puts the device in the low power SHUTDOWN mode. All of the drivers and four receivers go to a high impedance state. Receiver RX5 remains active while the transceiver is in SHUTDOWN. The transceiver consumes only 60µA of supply current while in SHUTDOWN. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. All receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. Supply current drops to 3mA when in DRIVER DISABLE mode. A logic low on the On/$\overline{Off}$ pin supersedes the state of the Driver Disable pin.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of transceivers, increasing the size of the storage capacitors is recommended to reduce ripple.

PIN FUNCTIONS

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. To reduce supply ripple, increase the size of the storage capacitor. With multiple transceivers, the V^+ and V^- pins may be paralleled into common filter capacitors.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance. When a 12V supply is available, C1 may be omitted. Connect the 12V supply to $C1^+$ and V^+. The 12V supply should be decoupled with a $0.1\mu F$ ceramic capacitor.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V_{OUT} = V^- + 30V$ to $V_{OUT} = V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RX OUT, are fully short-circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

LOW Q-CURRENT RX IN: Low Power Receiver Input. This special receiver remains active when the part is in SHUTDOWN mode, consuming typically 60µA. This receiver has the same input and protection characteristics as the other receivers.

LOW Q-CURRENT RX OUT: Low Power Receiver Output. This pin produces the same TTL/CMOS output voltage levels with slightly decreased speed and short-circuit current.

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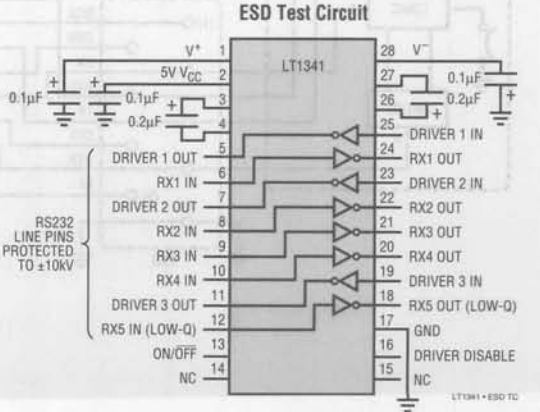
ESD PROTECTION

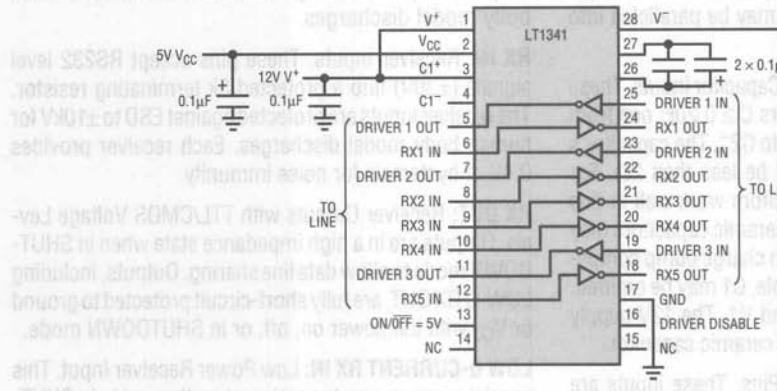
The RS232 line inputs of the LT1341 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1341 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit

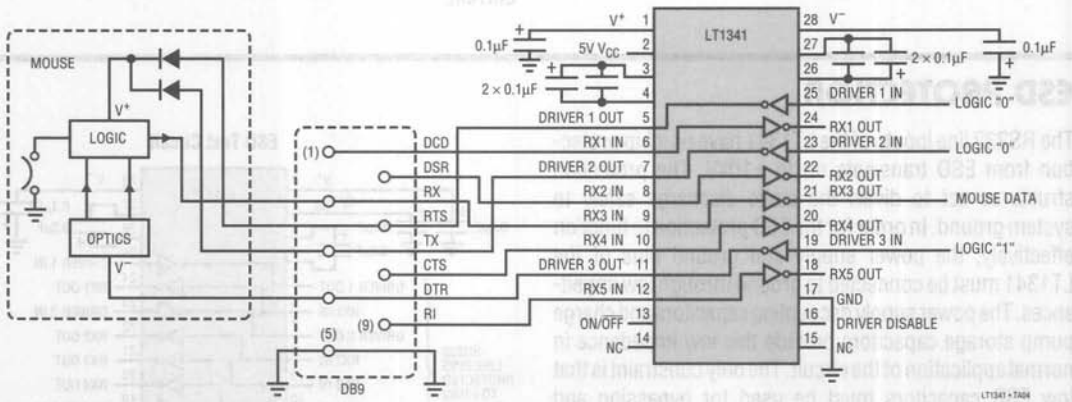


TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



Typical Mouse Driving Application



5V RS232 Transceiver with 3V Logic Interface

FEATURES

- ESD Protection Over ±**10kV**
- 3V Logic Interface
- Uses Small Capacitors: 0.1µF, 0.2µF
- 1µA Supply Current in SHUTDOWN
- Low Power Driver Disable Operating Mode
- Pin Compatible with LT1137A
- Operates to 120k Baud
- CMOS Comparable Low Power: 60mW
- Operates from a 5V Supply and 3V Logic Supply
- Easy PC Layout: Flowthrough Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Absolutely No Latch-Up

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LT1342 is an advanced low power three-driver, five-receiver RS232 transceiver. The LT1342 operates from a 5V supply and a 3V logic supply. Receiver outputs can interface directly to 3V logic circuits. Included on the chip is a shutdown pin for reducing supply current to near zero. All receivers and drivers assume high impedance states during SHUTDOWN.

The DRIVER DISABLE function provides additional control of operating mode. When DRIVER DISABLE is high the charge pump and drivers turn off. Receivers continue to operate during DRIVER DISABLE.

New ESD structures on the chip allow the LT1342 to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins.

The LT1342 is fully compliant with all EIA RS232 specifications and operates in excess of 120k baud even driving heavy capacitive loads.

TransZorb is a registered trademark of General Instruments, GSI

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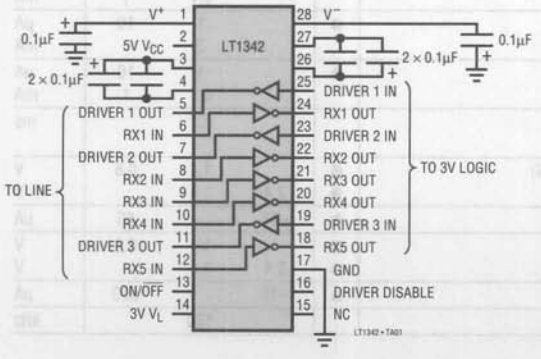
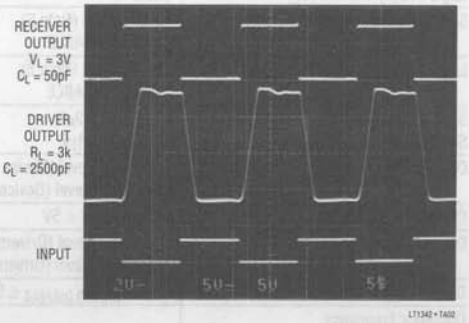
TYPICAL APPLICATION



Output Waveforms

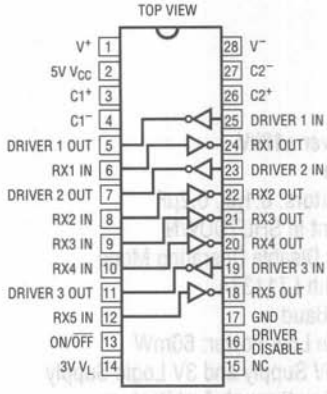


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
Supply Voltage (V_L) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... –30V to 30V
Output Voltage
  Driver ..... –30V to 30V
  Receiver ..... –0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1342C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD SOL

T_{JMAX} = 125°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LT1342CG
LT1342CN
LT1342CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				8.6		V
V^- Output				–7		V
Supply Current (V_{CC})	(Note 3)			12	17	mA
Logic Supply Current (V_L)	(Note 4)			0.1	1	mA
Supply Current When OFF (V_{CC})	SHUTDOWN (Note 5)	●		1	10	µA
	DRIVER DISABLE			3		mA
Logic Supply Current (V_L) When OFF	SHUTDOWN (Note 5)	●		1	10	µA
	DRIVER DISABLE			0.1	1	mA
Supply Rise Time SHUTDOWN to Turn-On	C1 = C2 = 0.2µF, $C^+ = C^-$ = 0.1µF			0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input Low Level (Device SHUTDOWN)	●		1.4	0.8	V
	Input High Level (Device Enabled)	●	2.4	1.4		V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/\overline{OFF}}$ ≤ 5V	●	–15		80	µA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●		1.4	0.8	V
	Input High Level (Drivers Disabled)	●	2.4	1.4		V
DRIVER DISABLE Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	–10		500	µA
Oscillator Frequency				130		kHz

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5	7.3		V
		Negative	●		−6.5	−5	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2V$		●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			9	17		mA
Output Leakage Current	SHUTDOWN V_{OUT} = ±30V (Note 5)		●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF				15	30	V/µs
	R_L = 3k, C_L = 2500pF				6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				0.6	1.3	µs
	Output Transition t_{LH} Low to High				0.5	1.3	µs
Any Receiver							
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)			0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)				1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance				3	5	7	kΩ
Output Leakage Current	SHUTDOWN (Note 4) $0 \le V_{OUT} \le V_{CC}$		●		1	10	µA
Receivers 1 Through 4							
Output Voltage	Output Low, I_{OUT} = −1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA		●	2.7	2.9		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$				−20	−10	mA
	Sourcing Current, V_{OUT} = 0V			10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7)				250	600	ns
	Output Transition t_{LH} Low to High				350	600	ns
Receiver 5							
Output Voltage	Output Low, I_{OUT} = −500µA		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA		●	2.7	2.9		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$				−4	−2	mA
	Sourcing Current, V_{OUT} = 0V			2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7)				1	3	µs
	Output Transition t_{LH} Low to High				1	3	µs

The ● denotes specifications which apply over the full operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V, V_L = 3.3V and $V_{ON/\overline{OFF}}$ = 3V.

Note 3: Supply current is measured with external capacitors $C^+ = C^-$ = 0.1µF, C1 = C2 = 0.2µF. All outputs are open with all driver inputs tied high.

Note 4: V_L supply current is measured with all receiver outputs high.

Note 5: Supply current and leakage measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}} \le 0.1V$. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE} \ge 3V$.

Note 6: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 7: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

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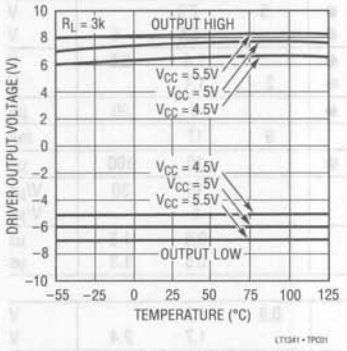
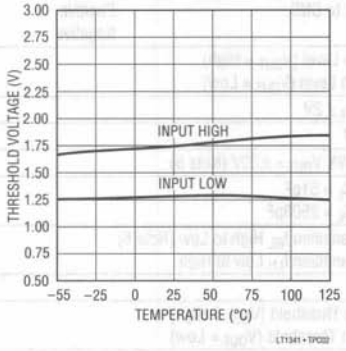
TYPICAL PERFORMANCE CHARACTERISTICS

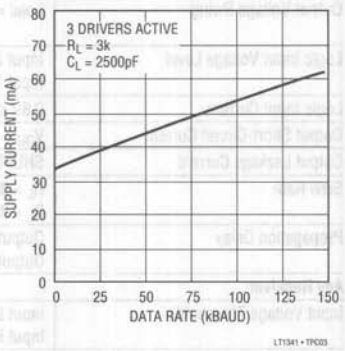
Driver Output Voltage



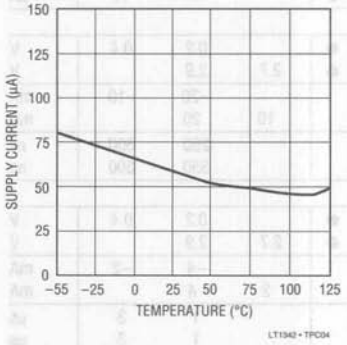
Receiver Input Thresholds



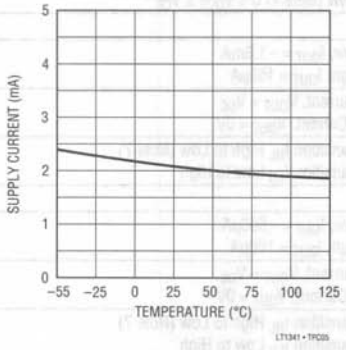
Supply Current vs Data Rate



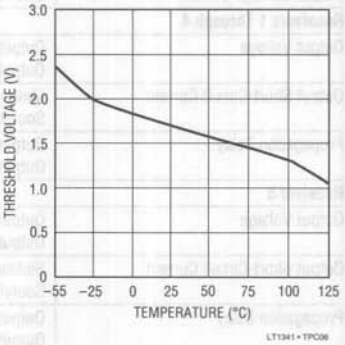
Supply Current in SHUTDOWN



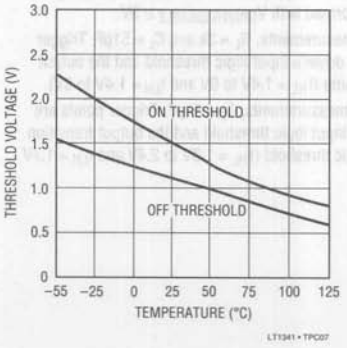
Supply Current in DRIVER DISABLE



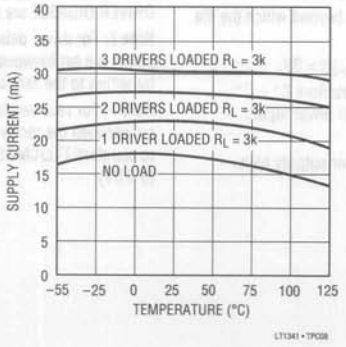
Driver Disable Threshold



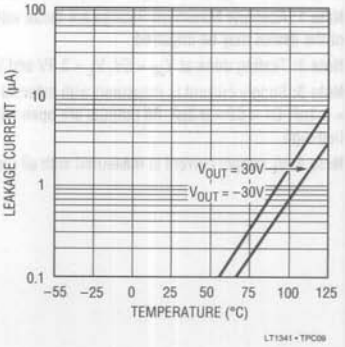
On/Off Thresholds



Supply Current

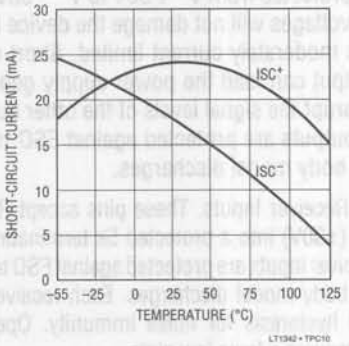


Driver Leakage in SHUTDOWN

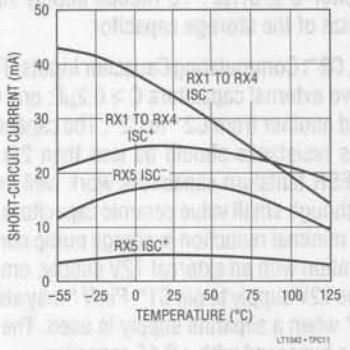


TYPICAL PERFORMANCE CHARACTERISTICS

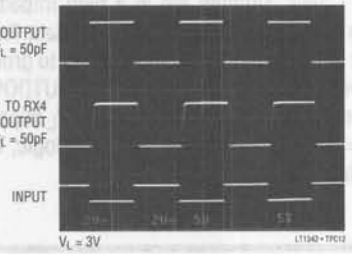
Driver Short-Circuit Current



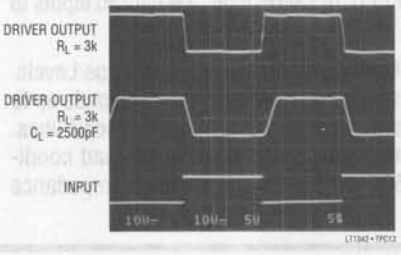
Receiver Short-Circuit Current



Receiver Output Waveforms



Driver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

V_L: 3V Logic Supply Pin. Provides power to the receiver outputs. Decouple with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: A TTL/CMOS Compatible Operating Mode Control. A logic low puts the device in the low power SHUTDOWN mode. Drivers and receivers assume a high impedance state in shutdown. The transceiver consumes almost no supply current while in shutdown. A logic high fully enables the transceiver. An On/$\overline{Off}$ logic low signal supersedes the state of the Driver Disable pin.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. All five receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver. A logic low on the On/$\overline{Off}$ pin supersedes the state of the Driver Disable pin. Supply current drops to 3mA when in Driver Disable mode.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. With multiple transceivers, the V^+ and V^- pins may be paralleled into common charge storage capacitors. Larger value capacitors may be used to reduce supply ripple.

5

PIN FUNCTIONS

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. To reduce supply ripple, increase the size of the storage capacitor.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance. For operation with an external 12V supply, omit C1 and connect the 12V supply to pin $C1^+$. Pin V^+ may also be shorted to $C1^+$ when a separate supply is used. The 12V supply must be bypassed with a 0.1F capacitor.

DRIVER IN: RS232 Driver Input Pins. These inputs are compatible with TTL or CMOS logic. Tie unused inputs to V_{CC} or V_L.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short-circuit protected from $V^- + 30V$ to $V^+ - 30V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10V for human body model discharges.

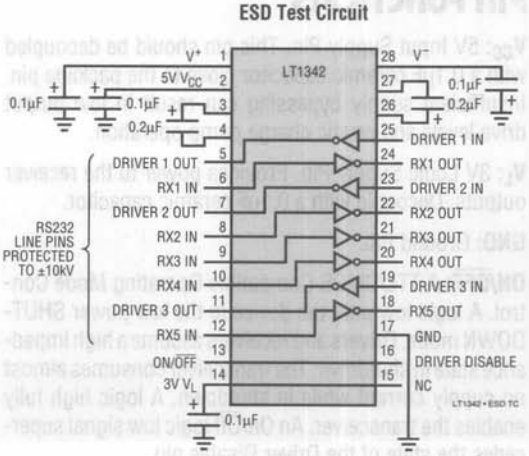
RX IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

RX OUT: Receiver Outputs with 3.3V Logic Compatible Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} or V_L with the power on, off, or in SHUTDOWN mode. Receiver output level is determined by V_L supply voltage. Use $V_L = 3.3V$ for interfacing with 3.3V logic, $V_L = 5V$ for interfacing with 5V logic.

ESD PROTECTION

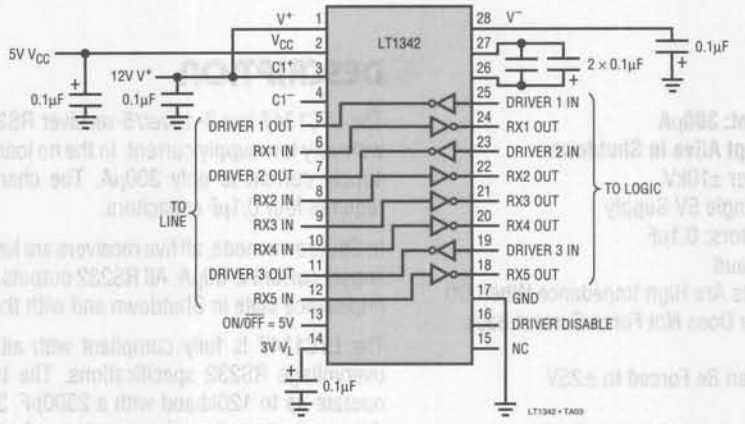
The RS232 line inputs of the LT1342 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1342 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit

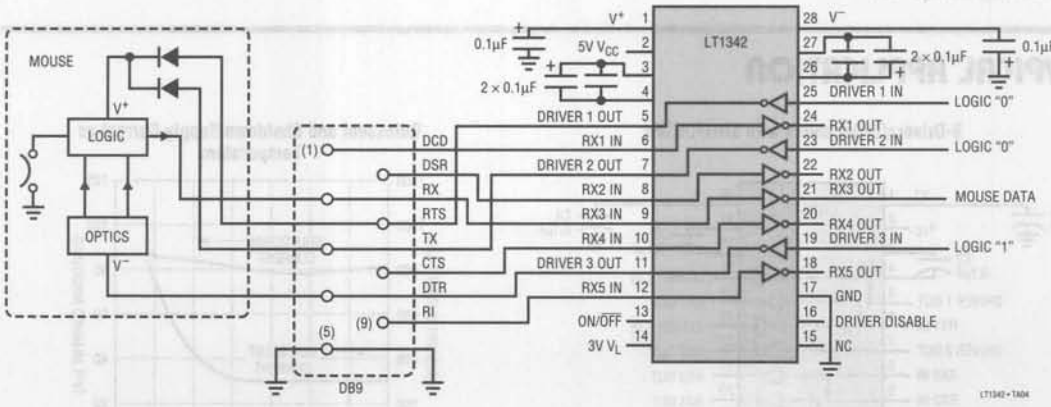


TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



Typical Mouse Driving Application



5

5V Low Power RS232 3-Driver/5-Receiver Transceiver with 5 Receivers Active in Shutdown

FEATURES

- **Low Supply Current: 300μA**
- **Five Receivers Kept Alive in Shutdown**
- ESD Protection Over ±10kV
- Operates from a Single 5V Supply
- Uses Small Capacitors: 0.1μF
- Operates to 120kBaud
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1137A and LT1237
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

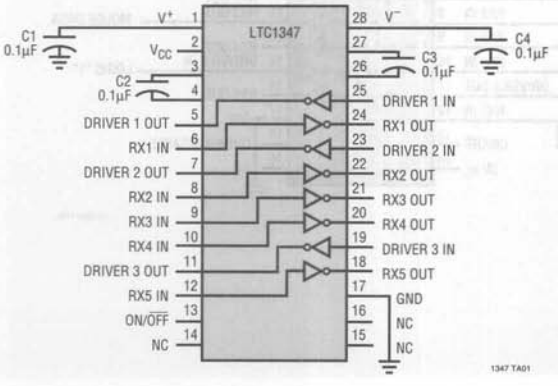
The LTC1347 is a 3-driver/5-receiver RS232 transceiver with very low supply current. In the no load condition, the supply current is only 300μA. The charge pump only requires four 0.1μF capacitors.

In Shutdown mode, all five receivers are kept alive and the supply current is 80μA. All RS232 outputs assume a high impedance state in Shutdown and with the power off.

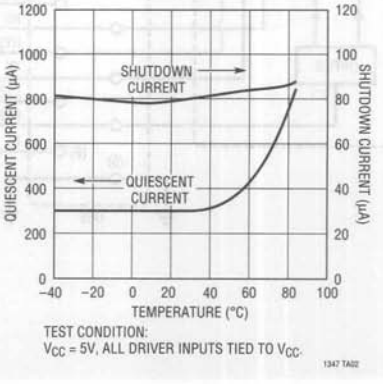
The LTC1347 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120kbaud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with SHUTDOWN



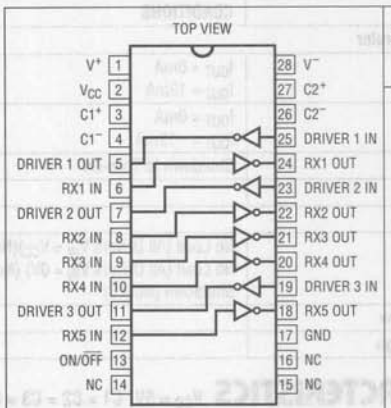
Quiescent and Shutdown Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  On/$\overline{Off}$ Pin ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD PLASTIC SOL

$T_{JMAX} = 125°C$, $\theta_{JA} = 96°C/W$ (G)
$T_{JMAX} = 125°C$, $\theta_{JA} = 56°C/W$ (N)
$T_{JMAX} = 125°C$, $\theta_{JA} = 85°C/W$ (S)

ORDER PART NUMBER
LTC1347CG
LTC1347CN
LTC1347CS

Consult factory for Industrial and Military grade parts.

5

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	–5.0	–6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = 5V$		●			5	µA
	$V_{IN} = 0V$		●			–5	µA
Output Short-Circuit Current	$V_{OUT} = 0V$				±12		mA
Output Leakage Current	Shutdown, $V_{OUT} = \pm 20V$ (Note 3)				±10	±500	µA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance	$V_{IN} = \pm 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ ($V_{CC} = 5V$)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 5V$)		●	3.5	4.8		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			–15	–40		mA
	Sourcing Current, $V_{OUT} = 0V$			10	20		mA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 12mA			7.5		V
V^- Output Voltage	I_{OUT} = 0mA			–8.0		V
	I_{OUT} = –12mA			–7.0		V
Supply Rise Time	Shutdown to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (All Drivers V_{IN} = V_{CC})(Note 2)	●		0.3	0.8	mA
	No Load (All Drivers V_{IN} = 0V) (Note 2)	●		0.5	1.0	mA
	Shutdown (Note 3)	●		80.0	120.0	µA
On/$\overline{\text{Off}}$ Threshold Low		●		1.4	0.8	V
On/$\overline{\text{Off}}$ Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.2	0.8	µs

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade.

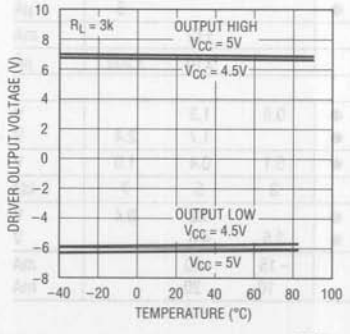
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

Note 3: Supply current and leakage current measurements in Shutdown are performed with $V_{ON/\overline{OFF}}$ = 0V.

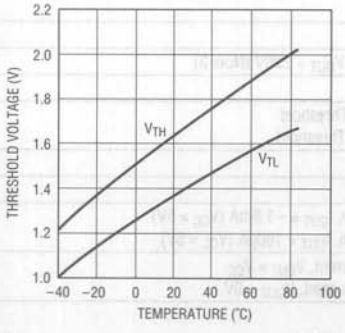
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage



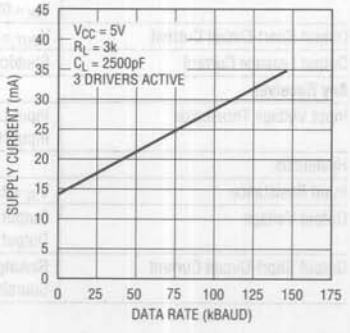
1347 G01

Receiver Input Thresholds



1347 G02

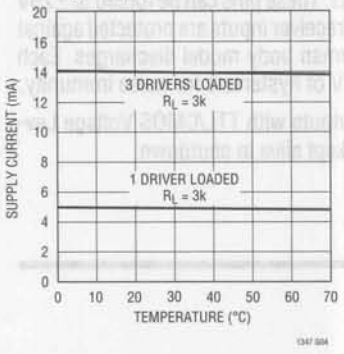
Supply Current vs Data Rate



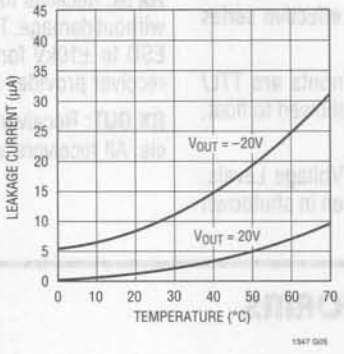
1347 G03

TYPICAL PERFORMANCE CHARACTERISTICS

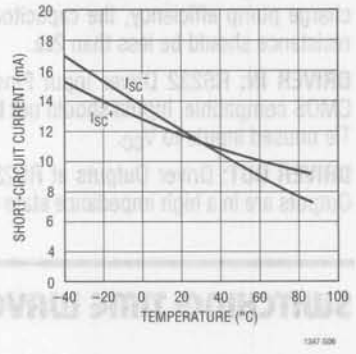
V_{CC} Supply Current



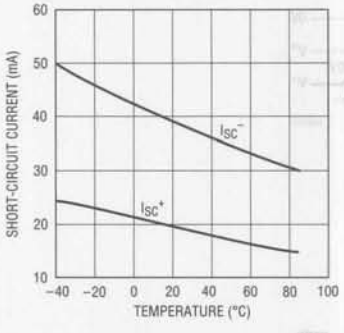
Driver Leakage in Shutdown



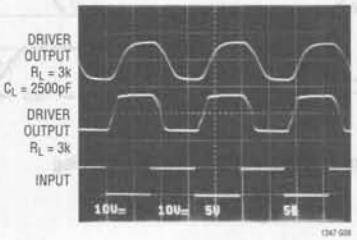
Driver Short-Circuit Current



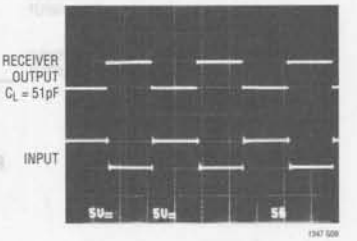
Receiver Short-Circuit Current



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current is typically 80µA in the Shutdown mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the shutdown mode with all receivers kept alive, and the supply current is 80µA. All driver outputs are in high impedance state. This pin cannot float.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 1.5V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

PIN FUNCTIONS

C1+, C1–, C2+, C2–: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from C1+ to C1–, and another from C2+ to C2–. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in shutdown mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. All receivers are kept alive in shutdown.

SWITCHING TIME WAVEFORMS

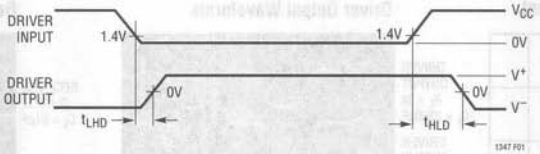


Figure 1. Driver Propagation Delay Timing

Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

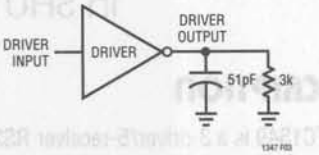


Figure 3. Driver Timing Test Load

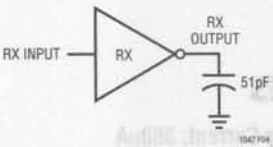


Figure 4. Receiver Timing Test Load

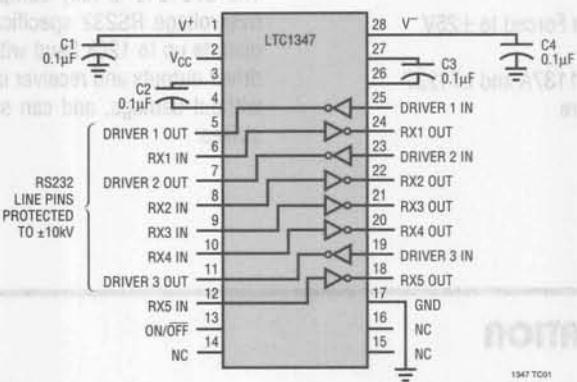


Figure 5. ESD Test Circuit

5V Low Power RS232 3-Driver/5-Receiver Transceiver with 2 Receivers Active in SHUTDOWN

FEATURES

- **Low Supply Current: 300μA**
- **Two Receivers Kept Alive in SHUTDOWN**
- **ESD Protection Over ±10kV**
- **Operates from a Single 5V Supply**
- Uses Small Capacitors: 0.1μF
- Operates to 120k Baud
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1137A and LT1237
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

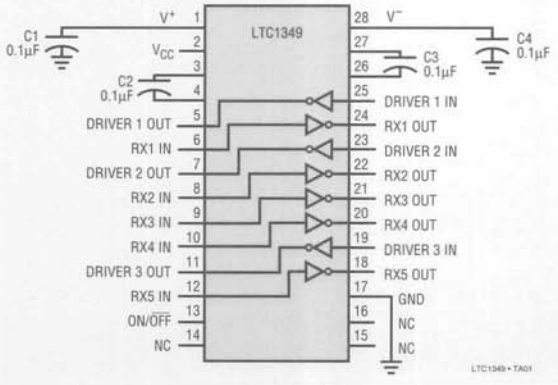
The LTC1349 is a 3-driver/5-receiver RS232 transceiver with very low supply current. In the no load condition, the supply current is only 300μA. The charge pump only requires four 0.1μF capacitors.

In SHUTDOWN mode, two receivers are kept alive and the supply current is 35μA. All RS232 outputs assume a high impedance state in SHUTDOWN and with the power off.

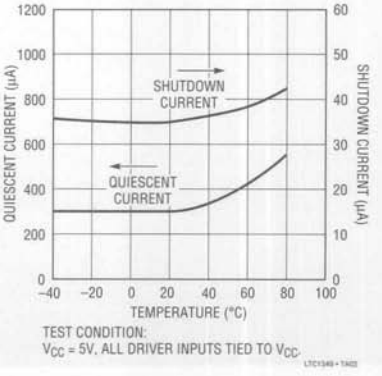
The LTC1349 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120k baud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with SHUTDOWN



Quiescent and SHUTDOWN Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Input Voltage
- Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
- Receiver ..... $-25V$ to $25V$
- On/Off Pin ..... $-0.3V$ to $V_{CC} + 0.3V$

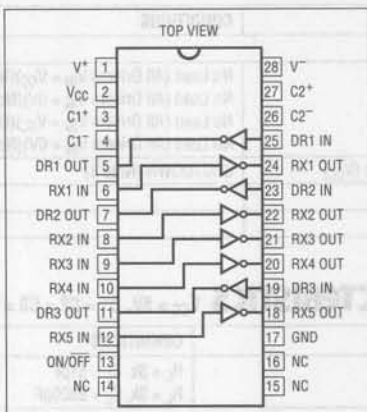
Output Voltage
- Driver ..... $-25V$ to $25V$
- Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$

Short Circuit Duration
- V^+ ..... 30 sec
- V^- ..... 30 sec
- Driver Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range
- Commercial (LTC1349C) ..... 0°C to 70°C
- Industrial (LTC1349I) ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1349CG
LTC1349CN
LTC1349CS
LTC1349IG
LTC1349IN
LTC1349IS

Consult factory for Military grade parts.

5

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	3k to GND Positive	●	5.0	7.0		V
	Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	V_{IN} = 5V	●			5	µA
	V_{IN} = 0V	●			−5	µA
Output Short-Circuit Current	V_{OUT} = 0V			±12		mA
Output Leakage Current	SHUTDOWN, V_{OUT} = ±20V (Note 3)	●		±10	±500	µA
Any Receiver						
Input Voltage Thresholds	Input Low Threshold	●	0.8	1.3		V
	Input High Threshold	●		1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	$-10V \le V_{IN} \le 10V$		3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA (V_{CC} = 5V)	●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 5V)	●	3.5	4.8		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		−15	−40		mA
Output Leakage Current	SHUTDOWN, $0 \le V_{OUT} \le V_{CC}$ (Note 3)	●		1	10	µA
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 12mA			7.5		V
V^- Output Voltage	I_{OUT} = 0mA			−8.0		V
	I_{OUT} = −12mA			−7.0		V
Supply Rise Time	SHUTDOWN to Turn-On			0.2		ms

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
V_{CC} Supply Current	No Load (All Drivers $V_{IN} = V_{CC}$)(Note 2), $0 \le T_A \le 70°C$	●		0.3	0.8	mA
	No Load (All Drivers V_{IN} = 0V)(Note 2), $0 \le T_A \le 70°C$	●		0.5	1.0	mA
	No Load (All Drivers $V_{IN} = V_{CC}$)(Note 2), $-40°C \le T_A \le 85°C$	●		0.3	1.0	mA
	No Load (All Drivers V_{IN} = 0V)(Note 2), $-40°C \le T_A \le 85°C$	●		0.5	1.5	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 3)	●		35	50	µA
On/$\overline{\text{Off}}$ Threshold Low		●		1.4	0.8	V
On/$\overline{\text{Off}}$ Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.2	0.8	µs

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$for commercial grade, $-40°C \le T_A \le 85°C$ for industrial grade).

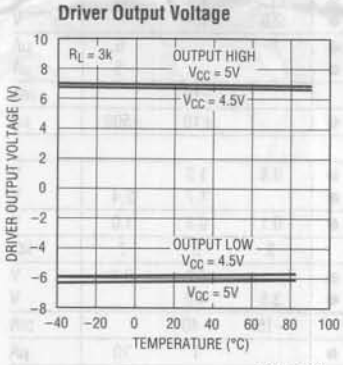
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

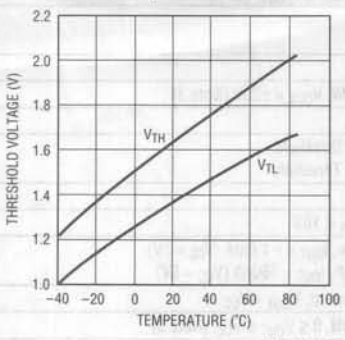
Note 3: Supply current and leakage current measurements in SHUTDOWN are performed with $V_{ON/\overline{OFF}}$ = 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

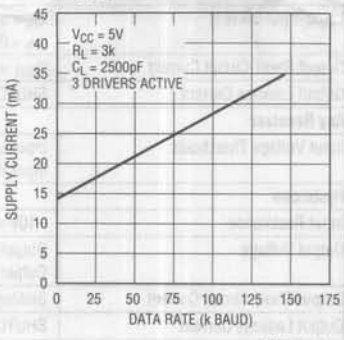
Driver Output Voltage



Receiver Input Thresholds



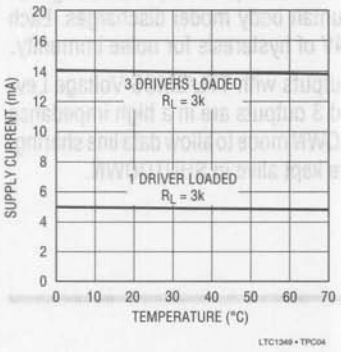
Supply Current vs Data Rate



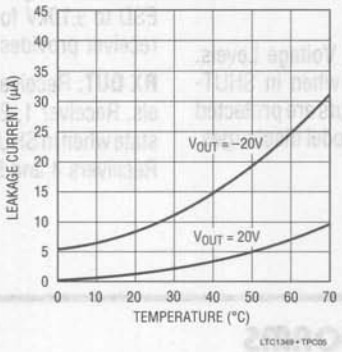
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

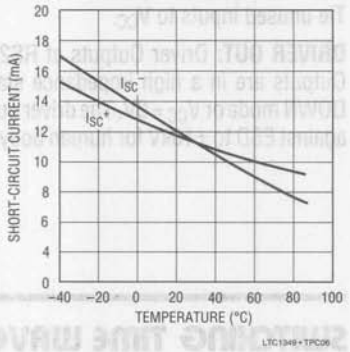
V_{CC} Supply Current



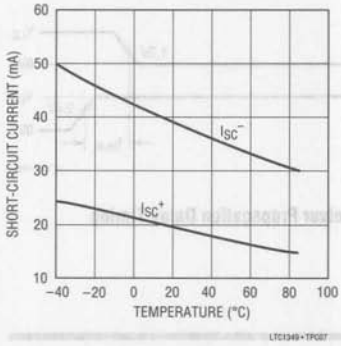
Driver Leakage in SHUTDOWN



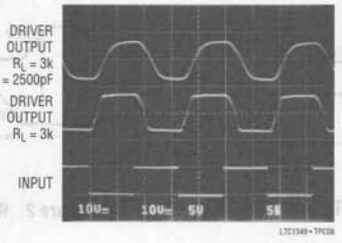
Driver Short-Circuit Current



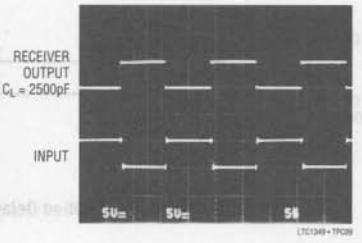
Receiver Short-Circuit Current



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current is typically 35µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible SHUTDOWN Pin. A logic low puts the device in SHUTDOWN mode, with receivers 4 and 5 kept alive and the supply current equal to 35µA. All driver outputs and other receiver outputs are in high impedance state. This pin can not float.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or 5V. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong 2V_{CC} - 1.5V$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 20Ω.

5

PIN FUNCTIONS

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Receiver 1, 2 and 3 outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Receivers 4 and 5 are kept alive in SHUTDOWN.

SWITCHING TIME WAVEFORMS

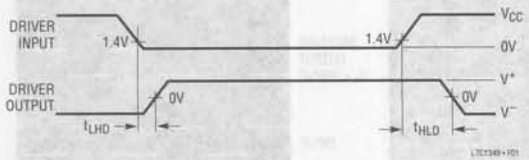


Figure 1. Driver Propagation Delay Timing

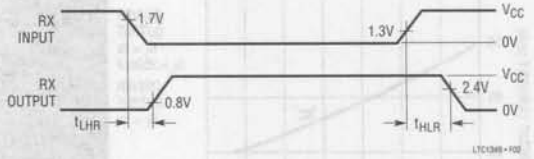
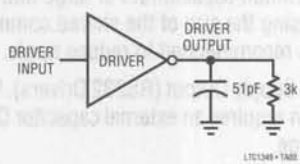


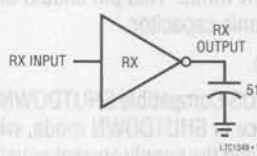
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

Driver Timing Test Load

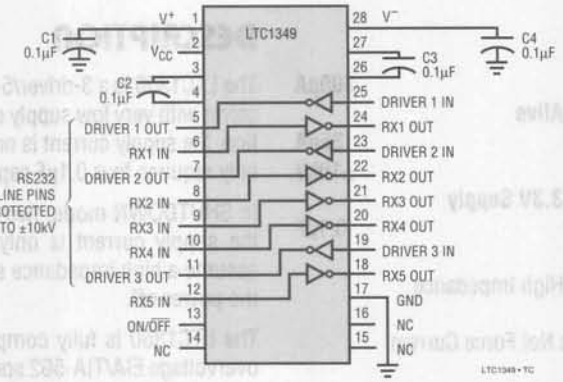


Receiver Timing Test Load



TEST CIRCUITS

ESD Test Circuit



5

3.3V Low Power EIA/TIA-562 3-Driver/ 5-Receiver Transceiver

FEATURES

- **Low Supply Current** **300µA**
- **Receivers 4 and 5 Kept Alive in SHUTDOWN** **35µA**
- **ESD Protection** **±10kV**
- **Operates from a Single 3.3V Supply**
- Uses Small Capacitors 0.1µF
- Operates to 120k Baud
- Three-State Outputs are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- EIA/TIA-562 I/O Lines Can Be Forced to ±25V Without Damage
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

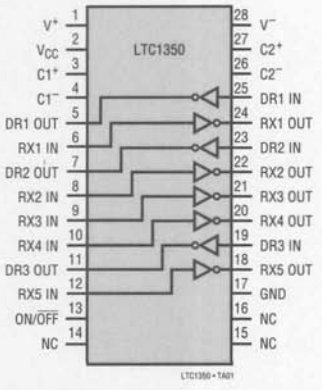
The LTC1350 is a 3-driver/5-receiver EIA/TIA-562 transceiver with very low supply current. In the no load condition, the supply current is only 300µA. The charge pump only requires four 0.1µF capacitors.

In SHUTDOWN mode, two receivers are kept alive and the supply current is only 35µA. All RS232 outputs assume a high impedance state in SHUTDOWN or with the power off.

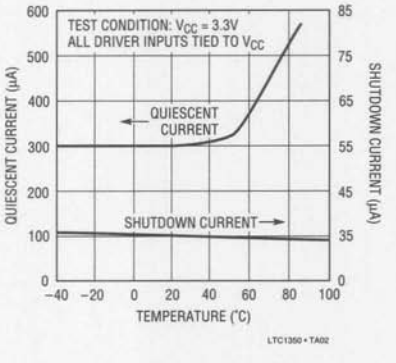
The LTC1350 is fully compliant with all data rate and overvoltage EIA/TIA-562 specifications. The transceiver can operate up to 120k baud with a 1000pF and 3k load. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with Shutdown



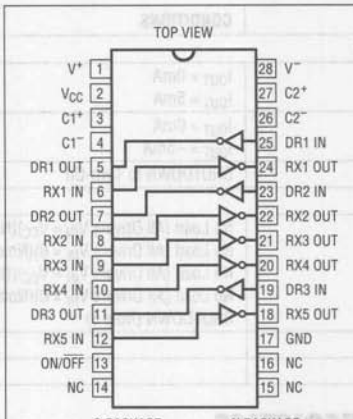
Quiescent and Shutdown Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 5V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  ON/$\overline{OFF}$ Pin ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  Commercial (LTC1350C) ..... 0°C to 70°C
  Industrial (LTC1350I) ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1350CG
LTC1350CN
LTC1350CS
LTC1350IG
LTC1350IN
LTC1350IS

Consult factory for Military grade parts

5

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	3.7	4.5		V
		Negative	●	−3.7	−4.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●			−5	µA
Output Short-Circuit Current	V_{OUT} = 0V				±10		mA
Output Leakage Current	SHUTDOWN (Note 3), V_{OUT} = ±20V				10	500	µA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	V_{IN} = ±10V			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 3.3V)		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 3.3V)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−3	−20		mA
Output Leakage Current	SHUTDOWN (Note 3), $0V \le V_{OUT} \le V_{CC}$		●		1	10	µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			5.7		V
	I_{OUT} = 5mA			5.5		V
V^- Output Voltage	I_{OUT} = 0mA			–5.3		V
	I_{OUT} = –5mA			–5.0		V
Supply Rise Time	SHUTDOWN to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (All Drivers $V_{IN} = V_{CC}$)(Note 2) 0°C ≤ T_A ≤ 70°C	●		0.3	0.6	mA
	No Load (All Drivers V_{IN} = 0)(Note 2) 0°C ≤ T_A ≤ 70°C	●		0.5	1.0	mA
	No Load (All Drivers $V_{IN} = V_{CC}$)(Note 2) –40°C ≤ T_A ≤ 85°C	●		0.3	1.0	mA
	No Load (All Drivers V_{IN} = 0)(Note 2) –40°C ≤ T_A ≤ 85°C	●		0.5	1.5	mA
	SHUTDOWN (Note 3)	●		35	50	µA
ON/$\overline{OFF}$ Threshold Low		●		1.4	0.8	V
ON/$\overline{OFF}$ Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 1000pF		3	5		V/µs
Driver Propagation Delay	t_{HLD} (Figure 1)	●		2	3.5	µs
(TTL to EIA/TIA-562)	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay	t_{HLR} (Figure 2)	●		0.3	0.8	µs
(EIA/TIA-562 to TTL)	t_{LHR} (Figure 2)	●		0.3	0.8	µs

The ● denotes specifications which apply over the operating temperature range of 0°C ≤ T_A ≤ 70°C for commercial grade, –40°C ≤ T_A ≤ 85°C for Industrial grade.

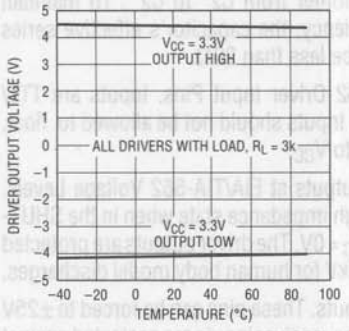
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

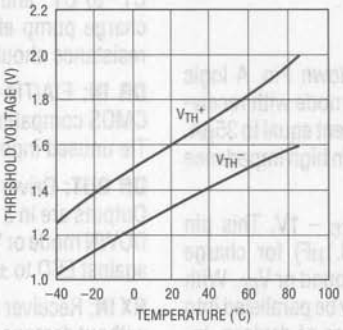
Note 3: Supply current measurement in SHUTDOWN mode is performed with $V_{ON/\overline{OFF}}$ = 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

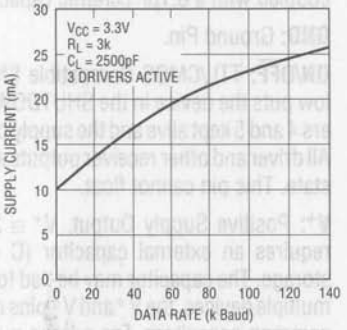
Driver Output Voltage vs Temperature



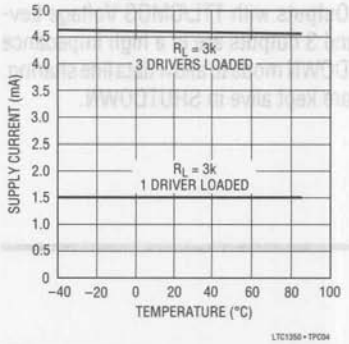
Receiver Input Thresholds vs Temperature



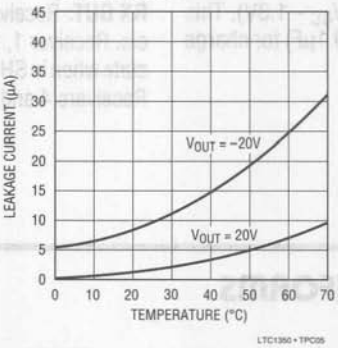
Supply Current vs Data Rate



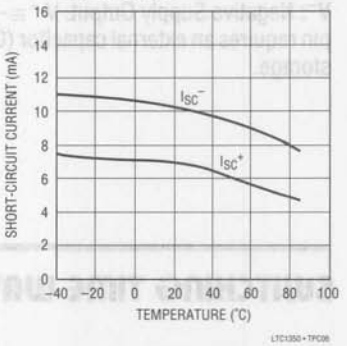
VCC Supply Current vs Temperature



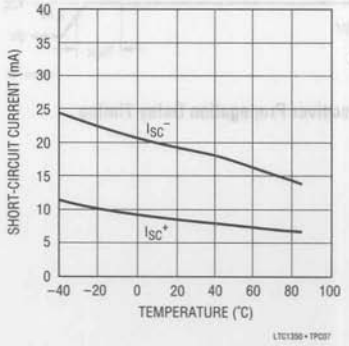
Driver Leakage in Shutdown vs Temperature



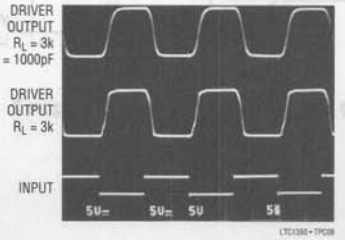
Driver Short-Circuit Current vs Temperature



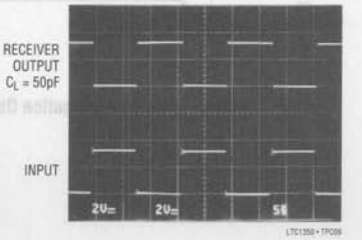
Receiver Short-Circuit Current vs Temperature



Driver Output Waveforms



Receiver Output Waveform



5

PIN FUNCTIONS

V_{CC}: 3.3V Input Supply Pin. Supply current is typically 35µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the SHUTDOWN mode with receivers 4 and 5 kept alive and the supply current equal to 35µA. All driver and other receiver outputs are in high impedance state. This pin cannot float.

V^+: Positive Supply Output. $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor (C = 0.1µF) for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For a large number of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output. $V^- \cong -(2V_{CC} - 1.3V)$. This pin requires an external capacitor (C = 0.1µF) for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors (C = 0.1µF): one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 20Ω.

DR IN: EIA/TIA-562 Driver Input Pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DR OUT: Driver Outputs at EIA/TIA-562 Voltage Levels. Outputs are in a high impedance state when in the SHUTDOWN mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Receiver 1, 2 and 3 outputs are in a high impedance state when in SHUTDOWN mode to allow data line sharing. Receivers 4 and 5 are kept alive in SHUTDOWN.

SWITCHING TIME WAVEFORMS

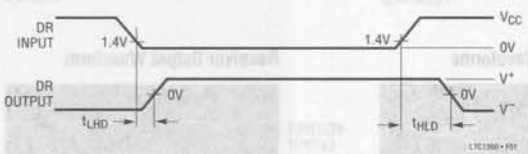


Figure 1. Driver Propagation Delay Timing

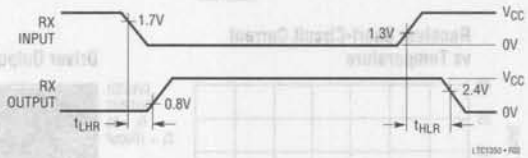
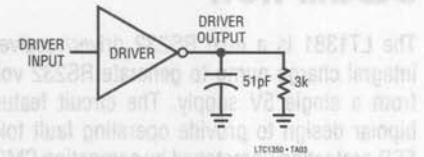


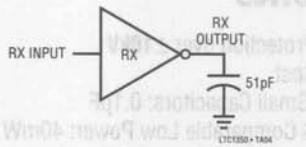
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

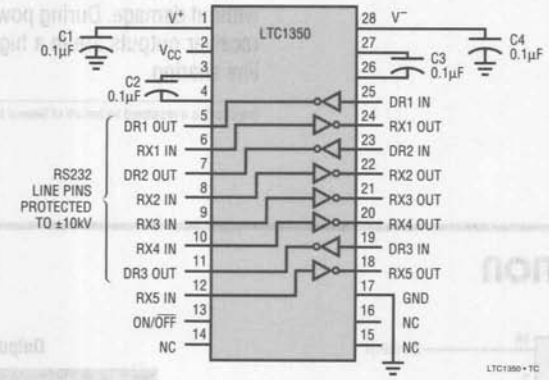
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



5

LINEAR TECHNOLOGY

LT1381

Low Power 5V RS232 Dual Driver/Receiver with 0.1µF Capacitors

FEATURES

- ESD Protection over ±**10kV**
- Low Cost
- Uses Small Capacitors: 0.1µF
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Powered Down
- Absolutely No Latch-Up
- Available in Narrow SO Package

APPLICATIONS

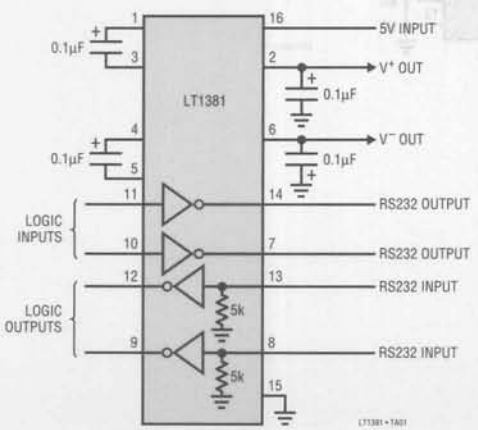
- Portable Computers
- Battery-Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

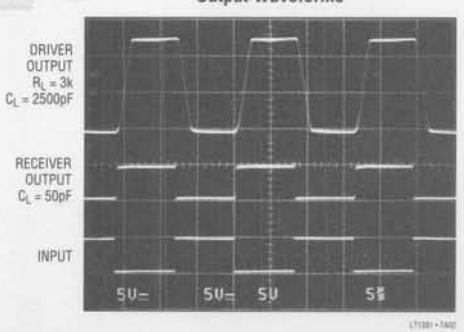
The LT1381 is a dual RS232 driver/receiver pair with integral charge pump to generate RS232 voltage levels from a single 5V supply. The circuit features rugged bipolar design to provide operating fault tolerance and ESD protection unmatched by competing CMOS designs. Using only 0.1µF external capacitors, the circuit consumes only 40mW of power and can operate to 120k baud even while driving heavy capacitive loads. New ESD structures on the chip allow the LT1381 to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins. Driver outputs are protected from overload and can be shorted to ground or up to ±25V without damage. During power-off conditions, driver and receiver outputs are in a high impedance state, allowing line sharing.

TransZorb is a registered trademark of General Instruments, GSI

TYPICAL APPLICATION



Output Waveforms



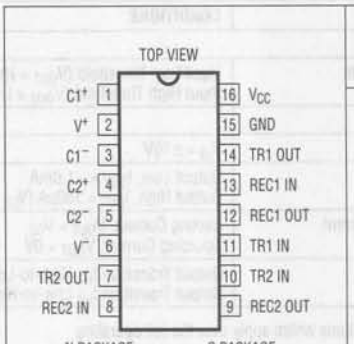
LINEAR TECHNOLOGY

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... −13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  ON/OFF ..... −0.3V to 12V
Output Voltage
  Driver ..... $V^+ - 30V$ to $V^- + 30V$
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1381C ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 46°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W, θ_{JC} = 34°C/W (S)

ORDER PART NUMBER
LT1381CN
LT1381CS

Consult factory for Industrial and Military grade parts.

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Generator							
V^+ Output					7.9		V
V^- Output					−7.0		V
Supply Current (V_{CC})	(Note 3), T_A = 25°C				8	14	mA
			●			16	mA
Supply Rise Time	C1 = C2 = C3 = C4 = 0.1µF				0.2		ms
Oscillator Frequency					130		kHz
Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.5		V
		Negative	●		−6.3	−5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	0.8V ≤ V_{IN} ≤ 2.0V		●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			9	17		mA
Output Leakage Current	Power Off V_{OUT} = ±15V		●		10	100	µA
Slew Rate	R_L = 3k, C_L = 51pF				15	30	V/µs
	R_L = 3k, C_L = 2500pF			4	6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 4)			0.6	1.3	µs	
Output Transition t_{LH} Low to High				0.5	1.3	µs	

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High) Input High Threshold (V_{OUT} = Low)		0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 10	−20 20	−10	mA mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5) Output Transition t_{LH} Low-to-High			250 350	600 600	ns ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V, unless otherwise specified.

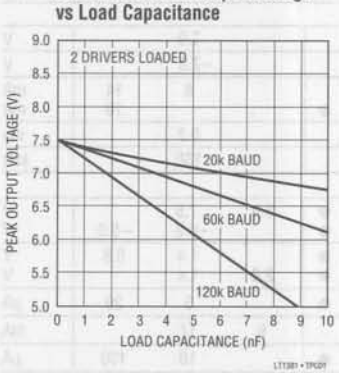
Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = C1 = C2 = 0.1\mu F$. All outputs are open, with all driver inputs tied high.

Note 4: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

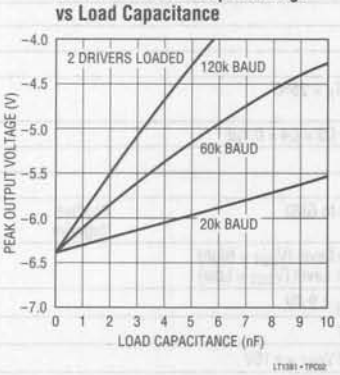
Note 5: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

TYPICAL PERFORMANCE CHARACTERISTICS

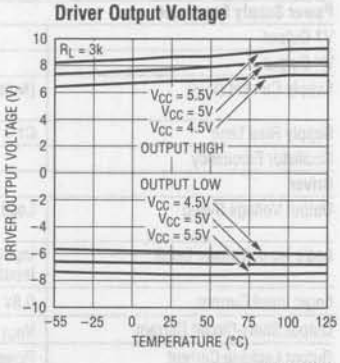
Driver Maximum Output Voltage vs Load Capacitance



Driver Minimum Output Voltage vs Load Capacitance

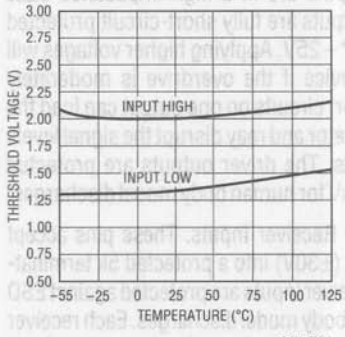


Driver Output Voltage

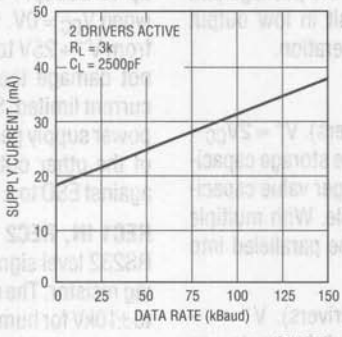


TYPICAL PERFORMANCE CHARACTERISTICS

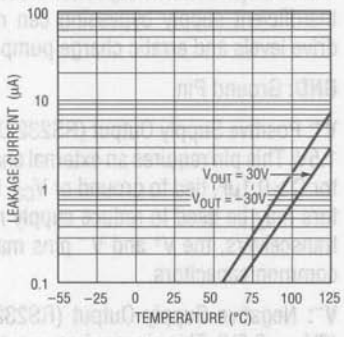
Receiver Input Threshold



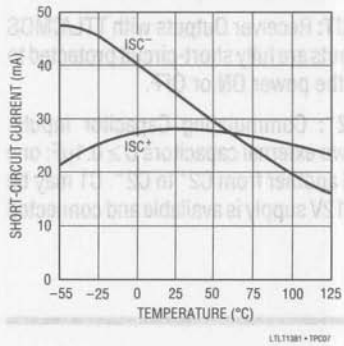
Supply Current vs Data Rate



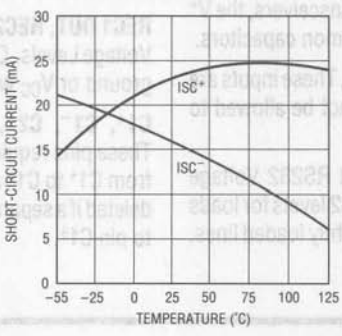
Driver Leakage in Shutdown



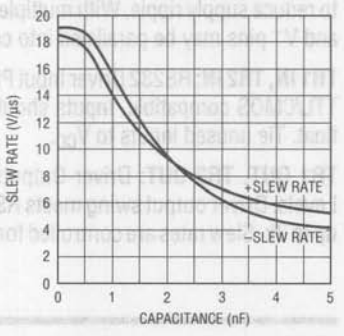
Receiver Short-Circuit Current



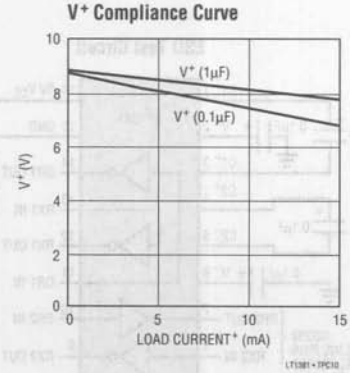
Driver Short-Circuit Current



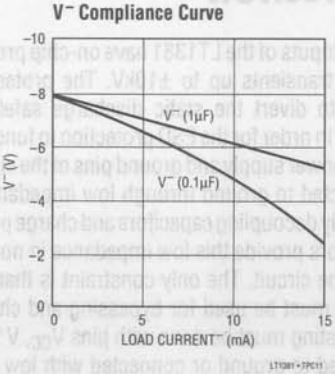
Slew Rate vs Load Capacitance



V+ Compliance Curve



V– Compliance Curve



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PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

TR1 IN, TR2 IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT, TR2 OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when $V_{CC} = 0V$. Outputs are fully short-circuit protected from $V^- + 25V$ to $V^+ - 25V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

REC1 IN, REC2 IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

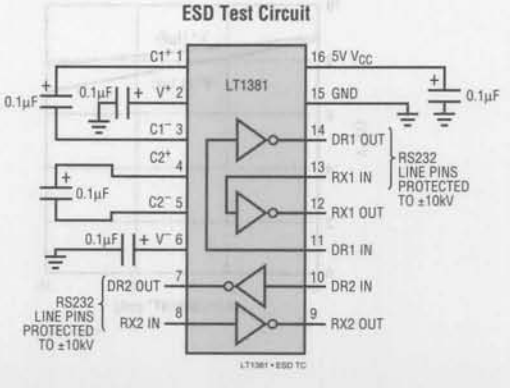
REC1 OUT, REC2 OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are fully short-circuit protected to ground or V_{CC} with the power ON or OFF.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.1\mu F$: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. C1 may be deleted if a separate 12V supply is available and connected to pin $C1^+$.

ESD PROTECTION

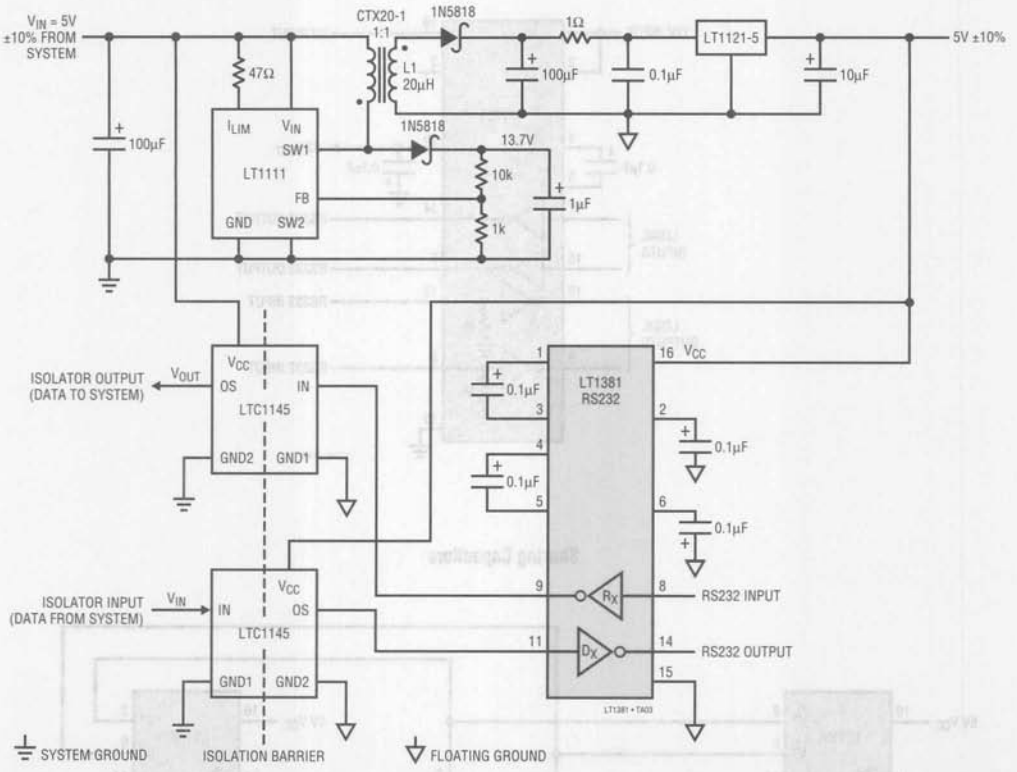
The RS232 line inputs of the LT1381 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit

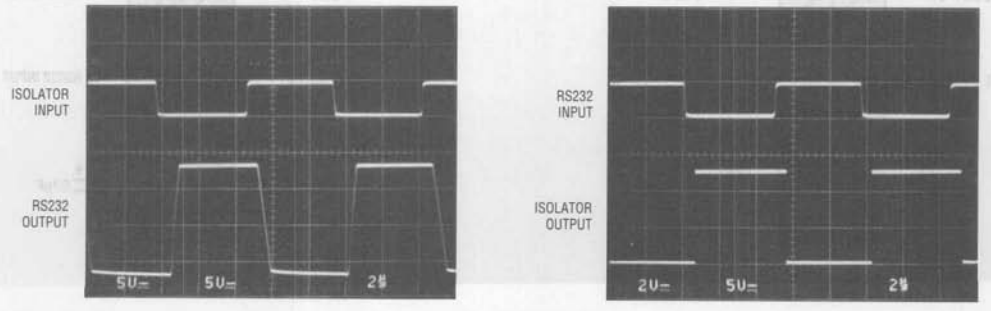


TYPICAL APPLICATIONS

Isolated RS232 Driver/Receiver



Data Transmission Across Isolation Barrier



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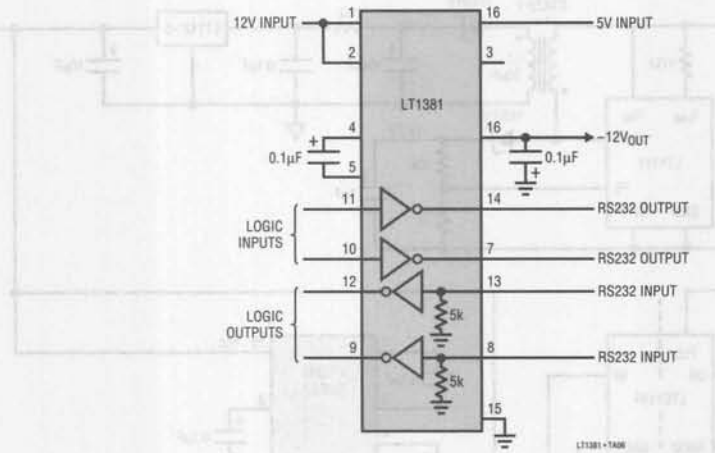
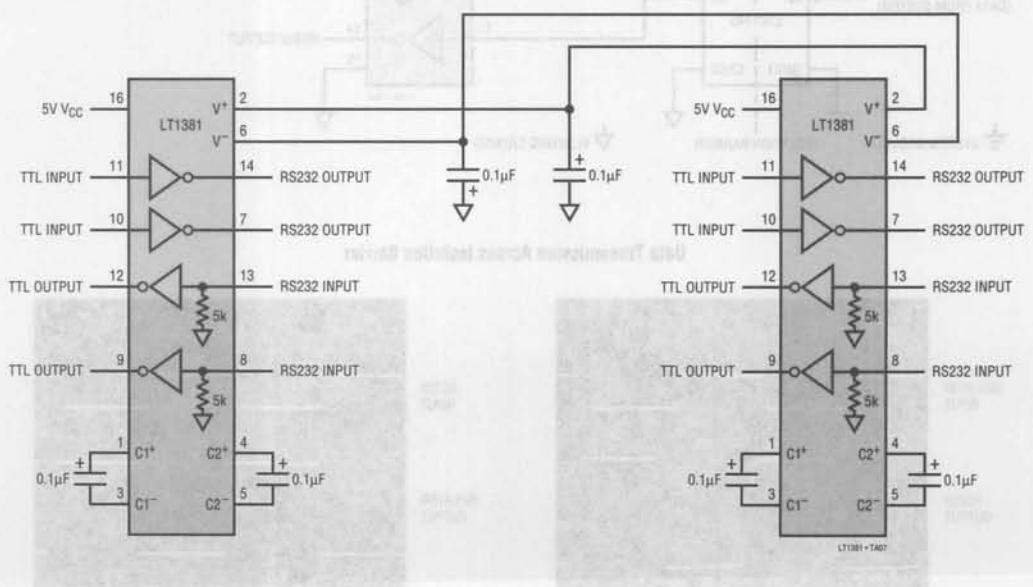
TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



Sharing Capacitors



5V Low Power RS232 Transceiver with Shutdown

FEATURES

- **Operates from a Single 5V Supply**
- **Low Supply Current: I_{CC} = 220µA**
- **I_{CC} = 0.2µA in Shutdown Mode**
- **ESD Protection Over ±10kV**
- Uses Small Capacitors: 0.1µF
- Operates to 120kBaud
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1180A

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LTC1382 is an ultra-low power 2-driver/2-receiver RS232 transceiver that operates from a single 5V supply. The charge pump requires only four space-saving 0.1µF capacitors.

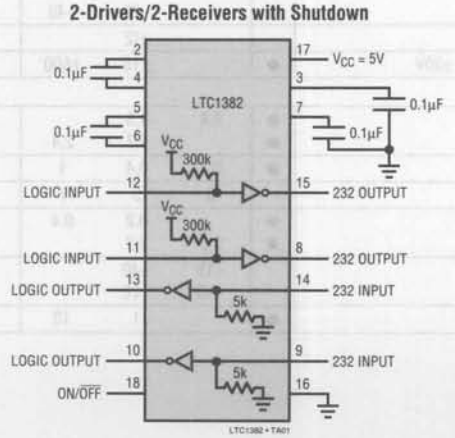
The transceiver operates in one of two modes, Normal and Shutdown. In the Normal mode, I_{CC} is only 220µA with the driver outputs unloaded. In the Shutdown mode, the charge pump is turned off, the driver outputs are forced into three-state, both receivers are off and I_{CC} drops to 0.2µA.

The LTC1382 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120kbaud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

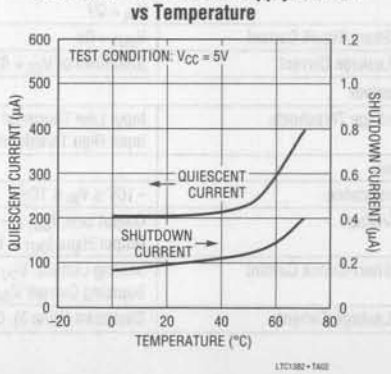
5

TYPICAL APPLICATION

2-Drivers/2-Receivers with Shutdown



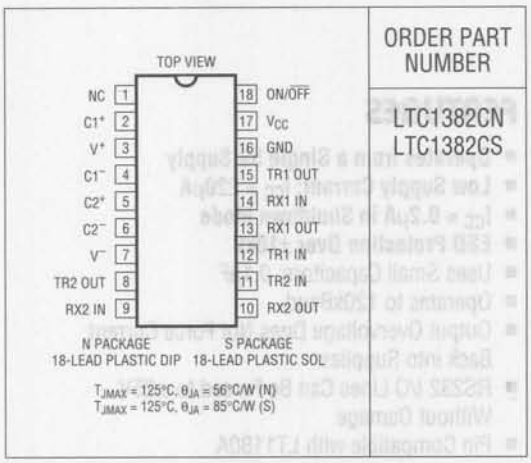
Quiescent and Shutdown Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  Digital Input ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1382CN
LTC1382CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, $V_{ON/\overline{OFF}}$ = V_{CC} unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●		−20	−40	µA
Output Short-Circuit Current	V_{OUT} = 0V				±12		mA
Output Leakage Current	Shutdown or V_{CC} = 0V (Note 3), V_{OUT} = ±20V		●		±10	±500	µA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 5V)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160µA$ (V_{CC} = 5V)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−15	−40		mA
	Sourcing Current V_{OUT} = 0V			10	20		mA
Output Leakage Current	Shutdown (Note 3), $0V \le V_{OUT} \le V_{CC}$		●		1	10	µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, $V_{ON/\overline{OFF}}$ = V_{CC}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V⁺ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 8mA			7.5		V
V⁻ Output Voltage	I_{OUT} = 0mA			−8.0		V
	I_{OUT} = −8mA			−7.0		V
Supply Rise Time	Shutdown to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.22	0.5	mA
Supply Leakage Current (V_{CC})	Shutdown (Note 3)	●		0.2	10	µA
Digital Input Threshold Low		●		1.4	0.8	V
Digital Input Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.3	0.8	µs

The ● denotes specifications which apply over the operating temperature range of 0°C ≤ T_A ≤ 70°C.

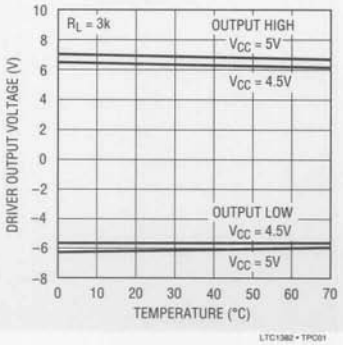
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

Note 3: Measurements made in the Shutdown mode are performed with $V_{ON/\overline{OFF}}$ = 0V.

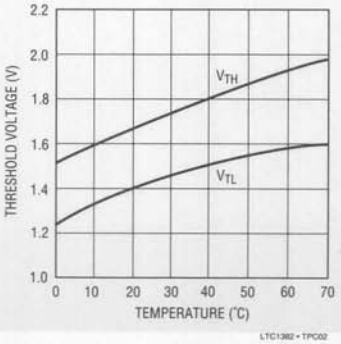
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage vs Temperature



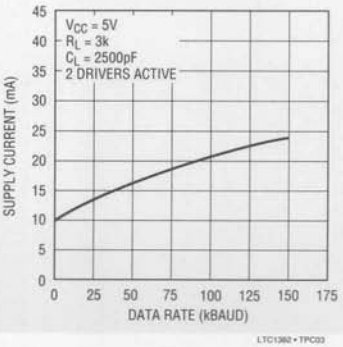
LTC1382 • TPC01

Receiver Input Thresholds vs Temperature



LTC1382 • TPC02

Supply Current vs Data Rate

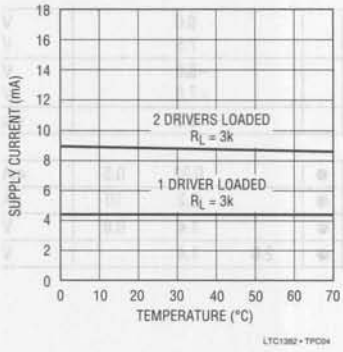


LTC1382 • TPC03

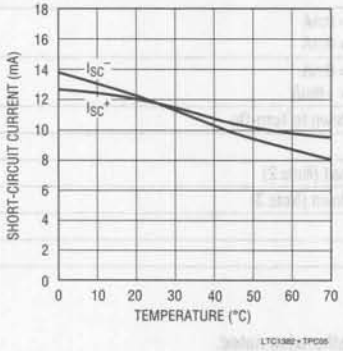
5

TYPICAL PERFORMANCE CHARACTERISTICS

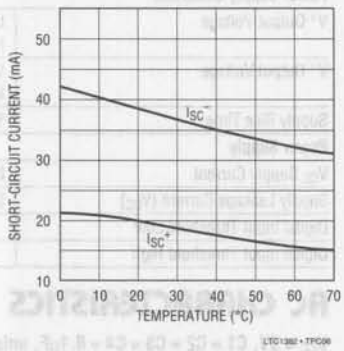
V_{CC} Supply Current vs Temperature



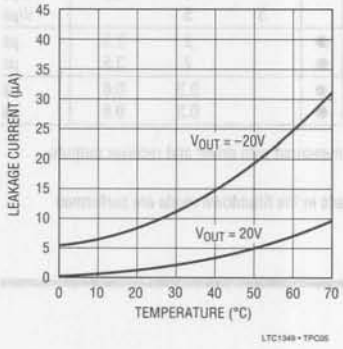
Driver Short-Circuit Current vs Temperature



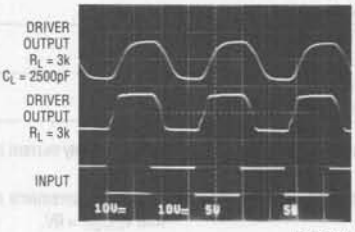
Receiver Short-Circuit Current vs Temperature



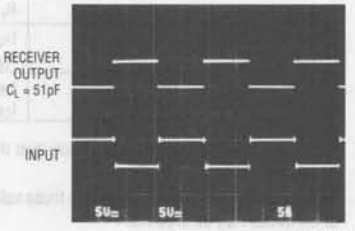
Driver Leakage in Shutdown vs Temperature



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the Shutdown mode. Both driver outputs are forced into three-state and the supply current is 0.2µA.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 2V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may share a common capacitor. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 2V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip. To minimize power consumption, the internal driver pull-up resistors are disconnected from V_{CC} in the Shutdown mode.

TR OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in the Shutdown or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in the Shutdown mode.

5

SWITCHING TIME WAVEFORMS

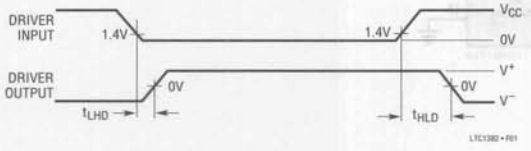


Figure 1. Driver Propagation Delay Timing

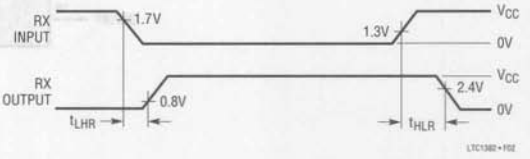
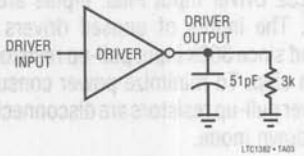


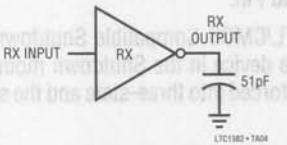
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

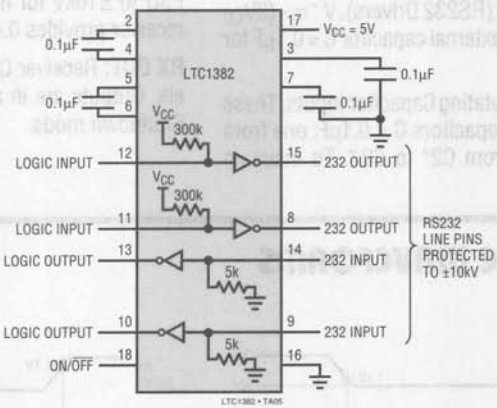
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



5V Low Power RS232 Transceiver

FEATURES

- **Operates from a Single 5V Supply**
- **Low Supply Current: I_{CC} = 220μA**
- **ESD Protection Over ±10kV**
- Available in 16-Pin SOIC Narrow Package
- Uses Small Capacitors: 0.1μF
- Operates to 120kBaud
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1181A and MAX232A

DESCRIPTION

The LTC1383 is an ultra-low power 2-driver/2-receiver RS232 transceiver that operates from a single 5V supply. The charge pump requires only four space-saving 0.1μF capacitors. The supply current (I_{CC}) of the transceiver is only 220μA with driver outputs unloaded.

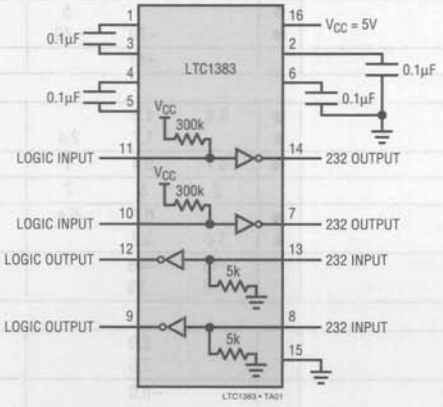
The LTC1383 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120kbaud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

APPLICATIONS

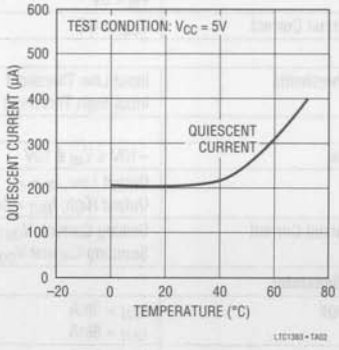
- Notebook Computers
- Palmtop Computers

5

TYPICAL APPLICATION



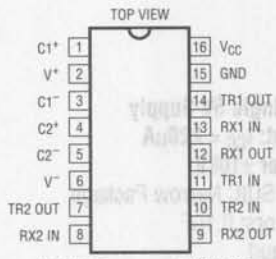
Quiescent Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  Digital Input ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD NARROW
PLASTIC SOIC

$T_{JMAX} = 125°C$, $\theta_{JA} = 65°C/W$ (N)
$T_{JMAX} = 125°C$, $\theta_{JA} = 95°C/W$ (S)

ORDER PART NUMBER
LTC1383CN LTC1383CS

Consult factory for Industrial and Military grade products.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	$V_{IN} = 0V$		●		−20	−40	µA
Output Short-Circuit Current	$V_{OUT} = 0V$				±12		mA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ ($V_{CC} = 5V$)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160µA$ ($V_{CC} = 5V$)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−15	−40		mA
	Sourcing Current $V_{OUT} = 0V$			10	20		mA
Power Supply Generator							
V^+ Output Voltage	$I_{OUT} = 0mA$				8.0		V
	$I_{OUT} = 8mA$				7.5		V
V^- Output Voltage	$I_{OUT} = 0mA$				−8.0		V
	$I_{OUT} = -8mA$				−7.0		V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.22	0.5	mA
Digital Input Threshold Low		●		1.4	0.8	V
Digital Input Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.3	0.8	µs

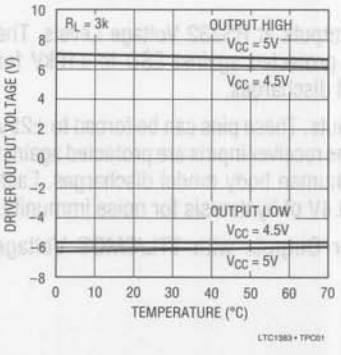
The ● denotes specifications which apply over the operating temperature range of 0°C ≤ T_A ≤ 70°C.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

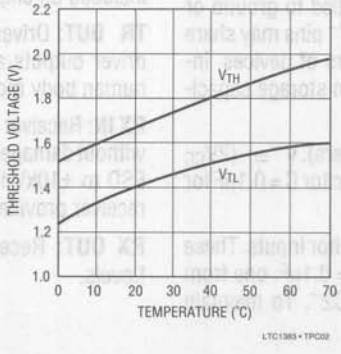
Note 2: Supply current is measured with driver and receiver outputs unloaded.

TYPICAL PERFORMANCE CHARACTERISTICS

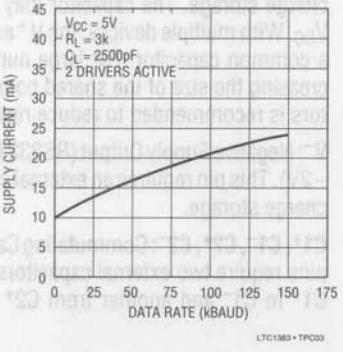
Driver Output Voltage vs Temperature



Receiver Input Thresholds vs Temperature

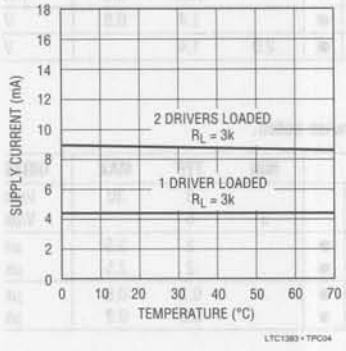


Supply Current vs Data Rate

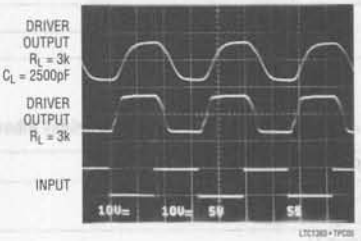


TYPICAL PERFORMANCE CHARACTERISTICS

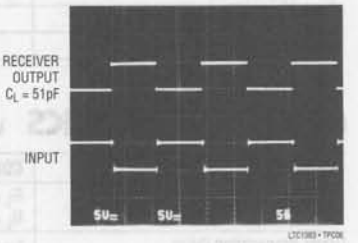
V_{CC} Supply Current vs Temperature



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 2V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may share a common capacitor. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 2V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip.

TR OUT: Driver Outputs at RS232 Voltage Levels. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels.

SWITCHING TIME WAVEFORMS

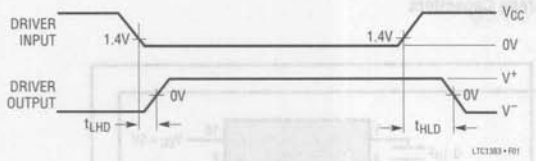


Figure 1. Driver Propagation Delay Timing

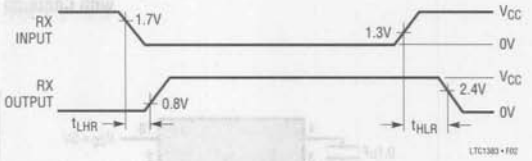
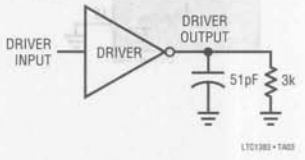


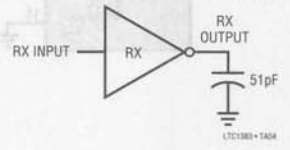
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

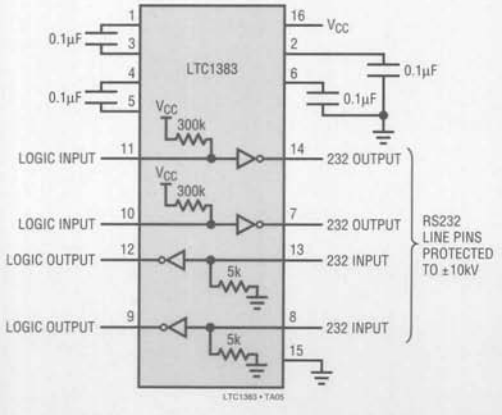
Driver Timing Test Load



Receiver Timing Test Load



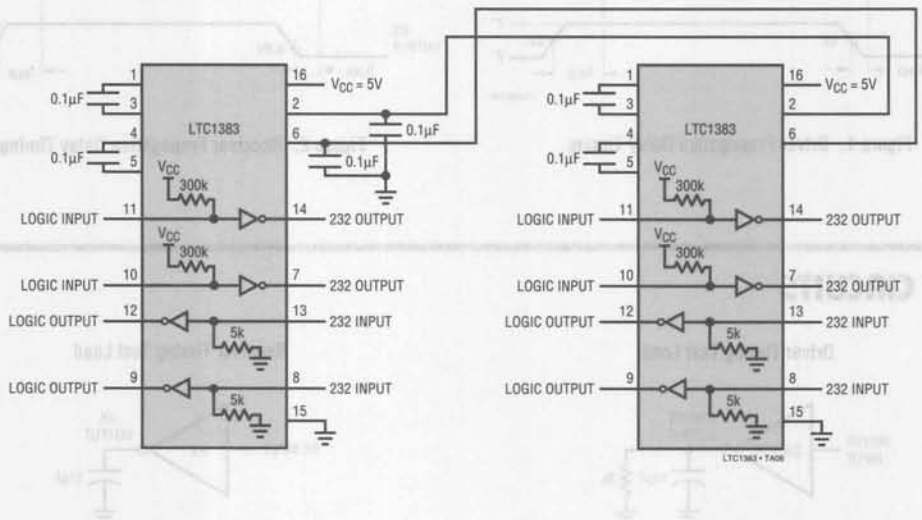
ESD Test Circuit



5

TYPICAL APPLICATIONS

Paralleling Power Supply Generator with Common Storage Capacitors



5V Low Power RS232 Transceiver with 2 Receivers Active in Shutdown

FEATURES

- **Operates from a Single 5V Supply**
- **Low Supply Current: I_{CC} = 220µA**
- **I_{CC} = 35µA in Shutdown Mode with Both Receivers Kept Alive**
- **ESD Protection Over ±10kV**
- Uses Small Capacitors: 0.1µF
- Operates to 120kBaud
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1180A

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LTC1384 is an ultra-low power 2-driver/2-receiver RS232 transceiver that operates from a single 5V supply. The charge pump requires only four space-saving 0.1µF capacitors.

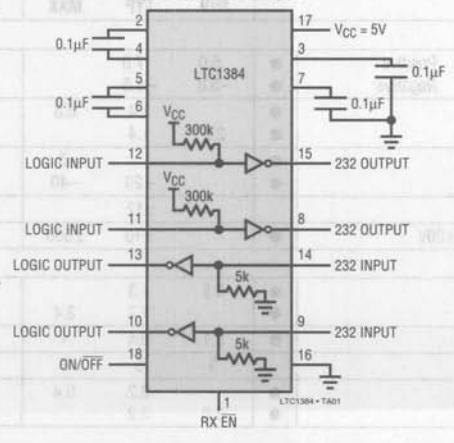
The transceiver operates in one of two modes, Normal and Shutdown. In the Normal mode, I_{CC} is only 220µA with the driver outputs unloaded. In the Shutdown mode, the charge pump is turned off, the driver outputs are forced into three-state, both receivers are kept active and I_{CC} drops to 35µA. The receiver outputs may be forced into three-state at any time using the receiver enable ($\overline{EN}$) pin.

The LTC1384 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120kbaud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

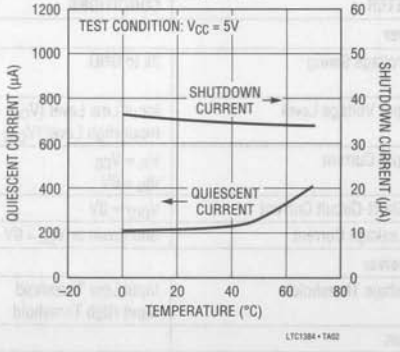
5

TYPICAL APPLICATION

2-Drivers/2-Receivers with Shutdown and Receiver Enable



Quiescent and Shutdown Supply Current vs Temperature

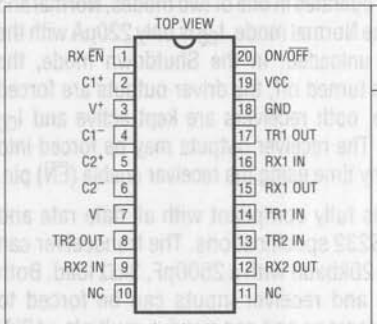


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  Digital Input ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$

Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

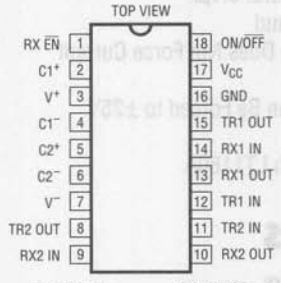


G PACKAGE
20-LEAD SSOP

T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1384CG



N PACKAGE
18-LEAD PLASTIC DIP

S PACKAGE
18-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 56°C/W

ORDER PART NUMBER

LTC1384CN
LTC1384CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, $V_{ON/\overline{OFF}} = V_{CC}$, $\overline{EN}$ = 0V, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●		−20	−40	µA
Output Short-Circuit Current	V_{OUT} = 0V				±12		mA
Output Leakage Current	Shutdown or V_{CC} = 0V (Note 3), V_{OUT} = ±20V		●		±10	±500	µA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 5V)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160µA$ (V_{CC} = 5V)		●	3.0	3.2		V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, $V_{ON/\overline{OFF}}$ = V_{CC}, $\overline{EN}$ = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC}		–15	–40		mA
	Sourcing Current, V_{OUT} = 0V		10	20		mA
Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}	●		1	10	µA
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 8mA			7.5		V
V^- Output Voltage	I_{OUT} = 0mA			–8.0		V
	I_{OUT} = –8mA			–7.0		V
Supply Rise Time	Shutdown to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.22	0.5	mA
Supply Leakage Current (V_{CC})	Shutdown (Note 3)	●		35	50	µA
Digital Input Threshold Low		●		1.4	0.8	V
Digital Input Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.3	0.8	µs

The ● denotes specifications which apply over the operating temperature range of 0°C ≤ T_A ≤ 70°C.

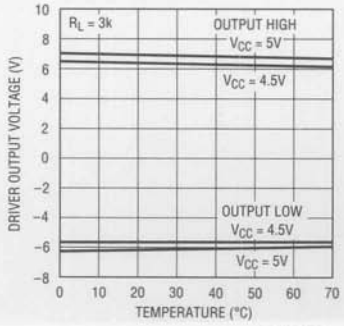
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

Note 3: Measurements made in the Shutdown mode are performed with $V_{ON/\overline{OFF}}$ = 0V.

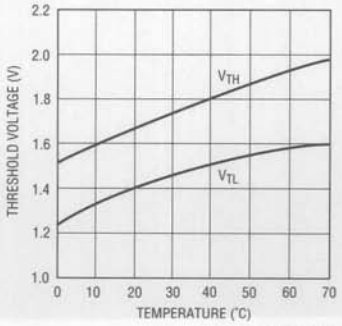
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage vs Temperature



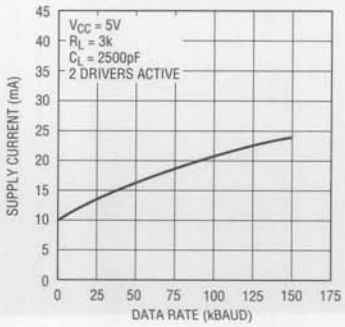
LTC1384 • TPC01

Receiver Input Thresholds vs Temperature



LTC1384 • TPC02

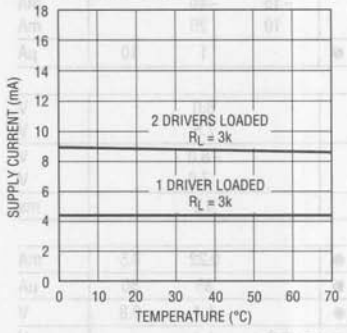
Supply Current vs Data Rate



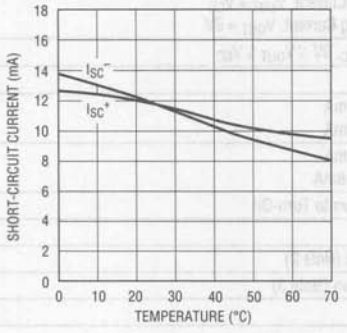
LTC1384 • TPC03

TYPICAL PERFORMANCE CHARACTERISTICS

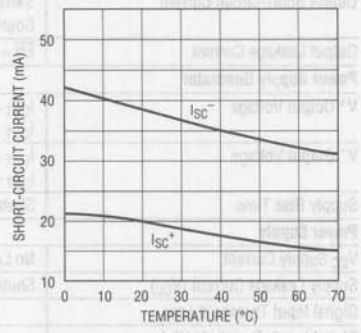
V_{CC} Supply Current vs Temperature



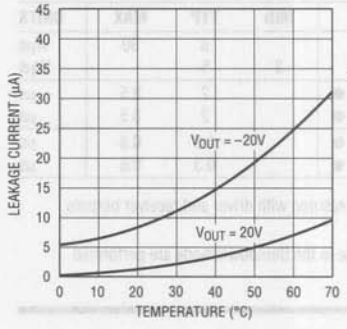
Driver Short-Circuit Current vs Temperature



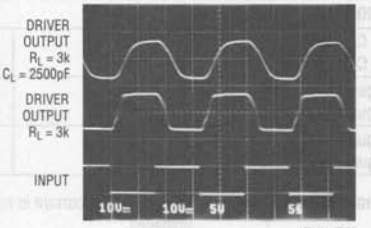
Receiver Short-Circuit Current vs Temperature



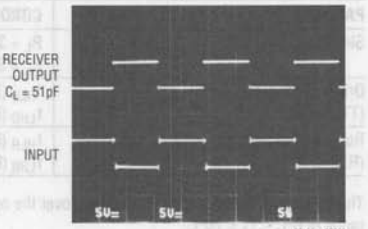
Driver Leakage in Shutdown vs Temperature



Driver Output Waveforms



Receiver Output Waveforms



PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the Shutdown mode independent of the $\overline{EN}$ pin. The supply current of the device drops to 35µA (two receivers alive) and both driver outputs are forced into three-state.

$\overline{EN}$: TTL/CMOS Compatible Receiver Enable Pin. A logic high forces the receiver outputs into three-state. A logic low enables the receiver outputs.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 2V_{CC} - 2V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may share a common capacitor. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 2V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip. To minimize power consumption, the internal driver pull-up resistors are disconnected from V_{CC} in the Shutdown mode.

TR OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in the Shutdown or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. A logic high at $\overline{EN}$ puts the outputs into three-state.

5

SWITCHING TIME WAVEFORMS

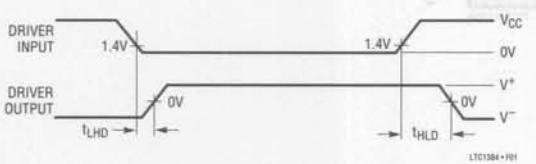


Figure 1. Driver Propagation Delay Timing

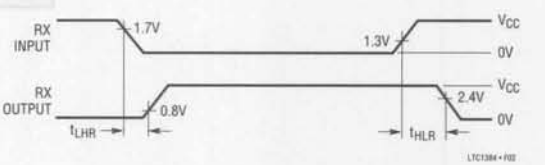
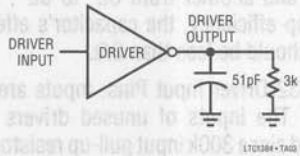


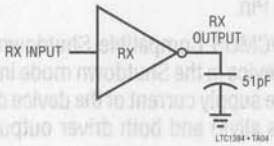
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

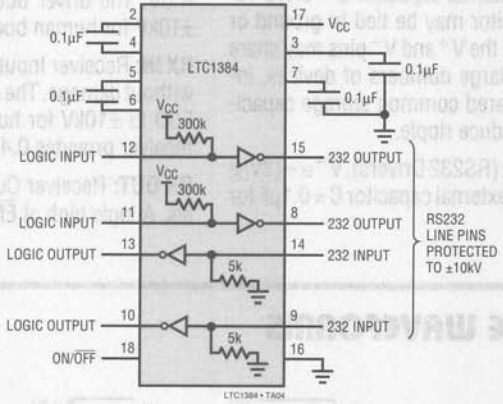
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



3.3V Low Power EIA/TIA-562 Transceiver

FEATURES

- **Operates from a Single 3.3V Supply**
- **Low Supply Current: I_{CC} = 200μA**
- **I_{CC} = 35μA in Driver Disable Mode**
- **I_{CC} = 0.2μA in Shutdown Mode**
- **ESD Protection Over ±10kV**
- Uses Small Capacitors: 0.1μF
- Operates to 120kBaud
- Output Overvoltage Does Not Force Current Back into Supplies
- EIA/TIA-562 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1180A

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

The LTC1385 is an ultra-low power, 2-driver/2-receiver EIA/TIA-562 transceiver which operates from a single 3.3V supply. The charge pump requires only four space-saving 0.1μF capacitors.

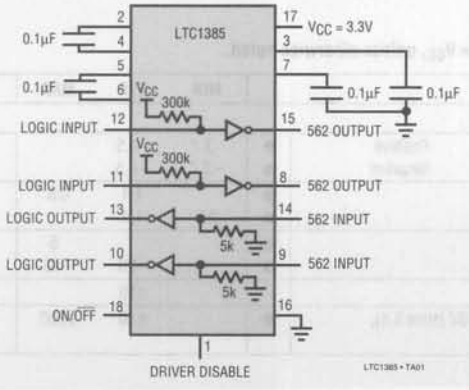
The transceiver operates in one of three modes: Normal, Driver Disable or Shutdown. In the Normal mode, I_{CC} is only 200μA in the unloaded condition. In the Driver Disable mode, the charge pump is turned off, the driver outputs are forced into three-state, both receivers are kept active, and I_{CC} drops to 35μA. In the Shutdown mode, everything is turned off and I_{CC} drops to 0.2μA.

The LTC1385 is fully compliant with all data rate and overvoltage EIA/TIA-562 specifications. The transceiver can operate up to 120kbaud with a 1000pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

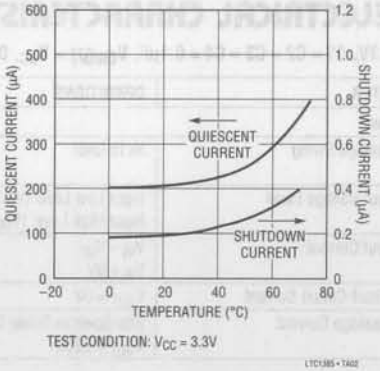
5

TYPICAL APPLICATION

2-Drivers/2-Receivers with Shutdown and Driver Disable



Quiescent and Shutdown Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 5V

Input Voltage
- Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
- Receiver ..... $-25V$ to $25V$
- Digital Input ..... $-0.3V$ to $V_{CC} + 0.3V$

Output Voltage
- Driver ..... $-25V$ to $25V$
- Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$

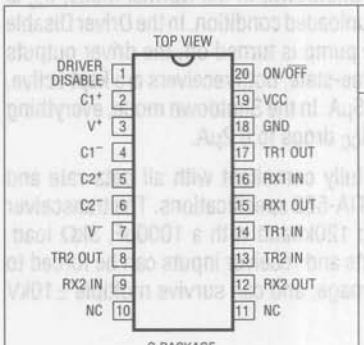
Short-Circuit Duration
- V^+ ..... 30 sec
- V^- ..... 30 sec
- Driver Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

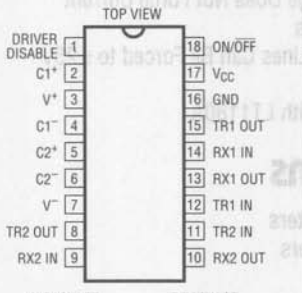


G PACKAGE
20-LEAD SSOP

T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1385CG



N PACKAGE
18-LEAD PLASTIC DIP

S PACKAGE
18-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1385CN
LTC1385CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1μF, $V_{ON/\overline{OFF}} = V_{CC}$, Driver Disable = V_{CC}, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	3.7	4.5		V
		Negative	●	−3.7	−4.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	μA
	V_{IN} = 0V		●		−20	−40	μA
Output Short-Circuit Current	V_{OUT} = 0V				±10		mA
Output Leakage Current	Shutdown or Driver Disable or V_{CC} = 0V (Note 3,4), V_{OUT} = ±20V		●		±10	±500	μA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, $V_{ON/\overline{OFF}}$ = V_{CC}, Driver Disable = V_{CC}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Receiver						
Input Voltage Thresholds	Input Low Threshold	●	0.8	1.3		V
	Input High Threshold	●		1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	$-10V \le V_{IN} \le 10V$		3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 3.3V)	●		0.2	0.4	V
	Output High, $I_{OUT} = 160µA$ (V_{CC} = 3.3V)	●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		−5	−20		mA
	Sourcing Current, V_{OUT} = 0V		2	7		mA
Output Leakage Current	Shutdown (Note 4), $0V \le V_{OUT} \le V_{CC}$	●		1	10	µA
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			5.7		V
	I_{OUT} = 5mA			5.5		V
V^- Output Voltage	I_{OUT} = 0mA			−5.3		V
	I_{OUT} = −5mA			−5.0		V
Supply Rise Time	Shutdown or Driver Disable to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2)	●		0.2	0.5	mA
Supply Leakage Current (V_{CC})	Shutdown (Note 4)	●		0.2	10	µA
	Driver Disable (Note 3)	●		35	50	µA
Digital Input Threshold Low		●		1.4	0.8	V
Digital Input Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 1000pF		3	5		V/µs
Driver Propagation Delay (TTL to EIA/TIA-562)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (EIA/TIA-562 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.2	0.8	µs

The ● denotes specifications which apply over the operating temperature range $0°C \le T_A \le 70°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

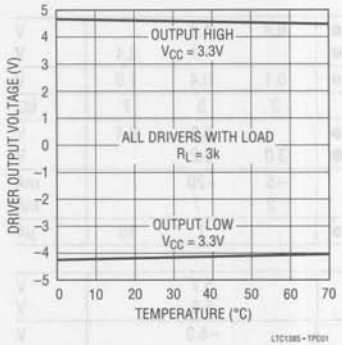
Note 3: Measurements made in the Driver Disable mode are performed with $V_{DRIVER\ DISABLE}$ = GND and $V_{ON/\overline{OFF}} = V_{CC}$.

Note 4: Measurements made in the Shutdown mode are performed with $V_{ON/\overline{OFF}}$ = 0V.

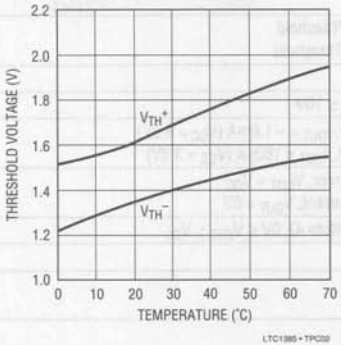
5

TYPICAL PERFORMANCE CHARACTERISTICS

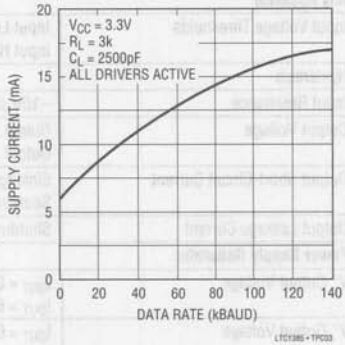
Driver Output Voltage vs Temperature



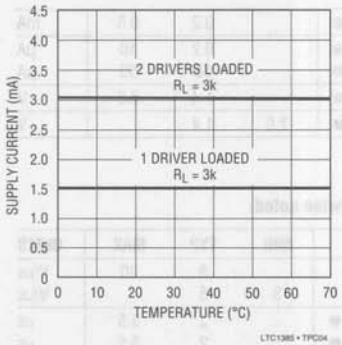
Receiver Input Thresholds vs Temperature



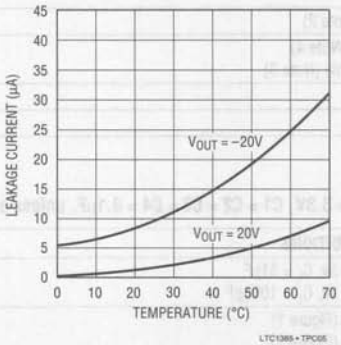
Supply Current vs Data Rate



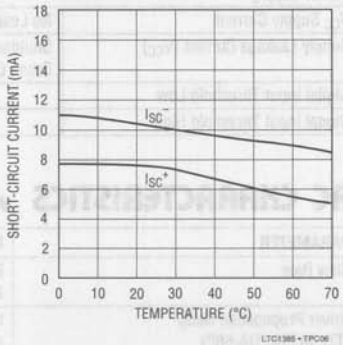
V_{CC} Supply Current vs Temperature



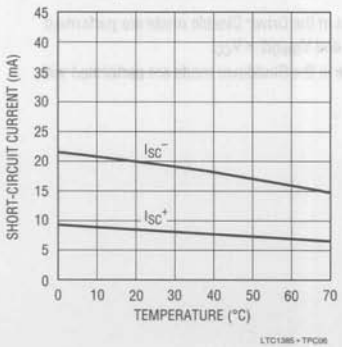
Driver Leakage in Shutdown vs Temperature



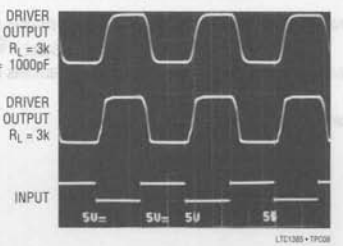
Driver Short-Circuit Current vs Temperature



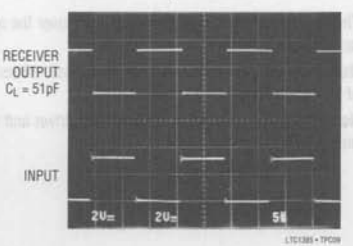
Receiver Short-Circuit Current vs Temperature



Driver Output Waveforms



Receiver Output Waveform



PIN FUNCTIONS

V_{CC}: 3.3V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Shutdown Pin. A logic low puts the device in the Shutdown mode independent of the Driver Disable pin. The supply current drops to 0.2µA and all driver and receiver outputs are forced into three-state.

DRIVER DISABLE: TTL/CMOS Compatible Input Pin. With the ON/$\overline{OFF}$ pin held high, a logic low forces the part into the Driver Disable mode with the charge pump turned off and the driver outputs forced into three-state. Both receivers remain active and the supply current drops to 35µA. A logic high forces the part into the Normal mode.

V^+: Positive Supply Output (EIA/TIA-562 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may share a common capacitor. For a large number of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (EIA/TIA-562 Drivers). $V^- \cong -(2V_{CC} - 1.3V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: EIA/TIA-562 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip. To minimize power consumption, the internal driver pull-up resistors are disconnected from V_{CC} in the Shutdown mode.

TR OUT: Driver Outputs at EIA/TIA-562 Voltage Levels. Outputs are in a high impedance state when in the Shutdown or Driver Disable mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in the Shutdown mode.

5

SWITCHING TIME WAVEFORMS

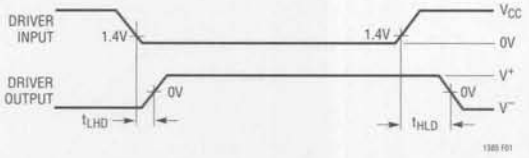


Figure 1. Driver Propagation Delay Timing

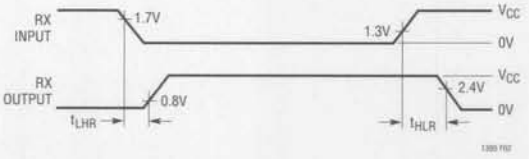
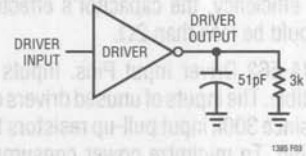


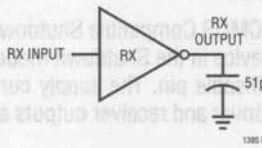
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

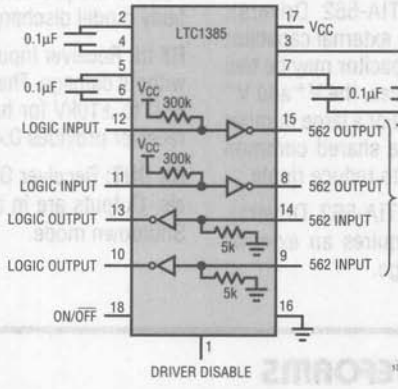
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



3.3V Low Power EIA/TIA562 Transceiver

FEATURES

- **Operates from a Single 3.3V Supply**
- **Low Supply Current: I_{CC} = 200μA**
- ESD Protection Over ±10kV
- Available in 16-Pin SOIC Narrow Package
- Uses Small Capacitors: 0.1μF
- Operates to 120kBaud
- Output Overvoltage Does Not Force Current Back into Supplies
- EIA/TIA562 I/O Lines Can Be Forced to ±25V Without Damage
- Pin Compatible with LT1181A

APPLICATIONS

- Notebook Computers
- Palmtop Computers

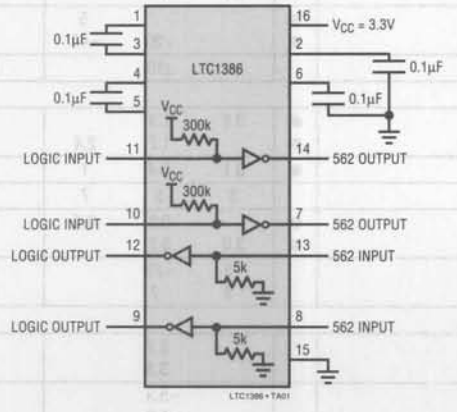
DESCRIPTION

The LTC1386 is an ultra-low power 2-driver/2-receiver EIA/TIA562 transceiver that operates from a single 3.3V supply. The charge pump requires only four space-saving 0.1μF capacitors. The supply current (I_{CC}) of the transceiver is only 200μA with driver outputs unloaded.

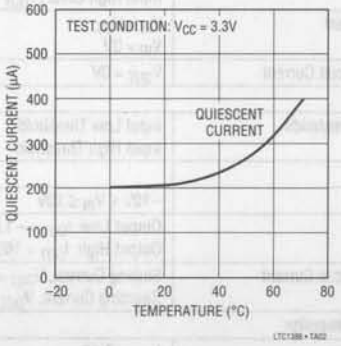
The LTC1386 is fully compliant with all data rate and overvoltage EIA/TIA562 specifications. The transceiver can operate up to 120kbaud with a 1000pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

5

TYPICAL APPLICATION



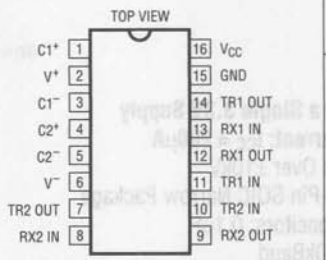
Quiescent Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 5V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  Digital Input ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD NARROW
PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 65°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 95°C/W (S)

ORDER PART NUMBER
LTC1386CN
LTC1386CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	3.7	4.5		V
		Negative	●	−3.7	−4.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●		−20	−40	µA
Output Short-Circuit Current	V_{OUT} = 0V				±10		mA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1	V
Input Resistance	$-10V \le V_{IN} \le 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 3.3V)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160µA$ (V_{CC} = 3.3V)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−5	−20		mA
	Sourcing Current, V_{OUT} = GND			2	7		mA
Power Supply Generator							
V^+ Output Voltage	I_{OUT} = 0mA				5.7		V
	I_{OUT} = 5mA				5.5		V
V^- Output Voltage	I_{OUT} = 0mA				−5.3		V
	I_{OUT} = −5mA				−5.0		V
Power Supply							
V_{CC} Supply Current	No Load (Note 2)		●		0.2	0.5	mA

AC CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 1000pF		3	5		V/µs
Driver Propagation Delay (TTL to EIA/TIA562)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (EIA/TIA562 to TTL)	t_{HLR} (Figure 2)	●		0.3	0.8	µs
	t_{LHR} (Figure 2)	●		0.3	0.8	µs

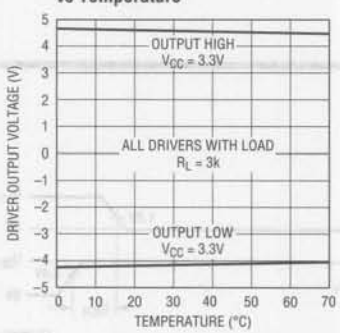
The ● denotes specifications which apply over the operating temperature range of $0°C \le T_A \le 70°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

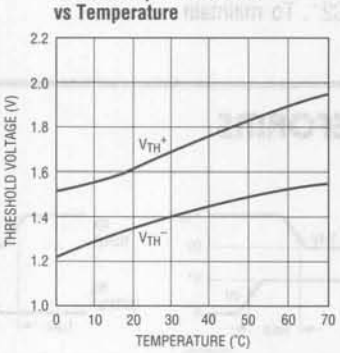
Note 2: Supply current is measured with driver and receiver outputs unloaded.

TYPICAL PERFORMANCE CHARACTERISTICS

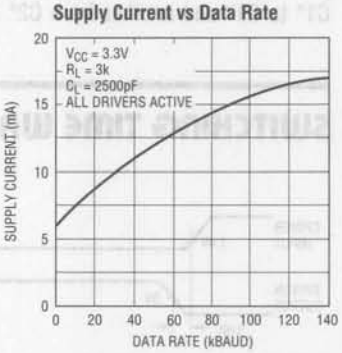
Driver Output Voltage vs Temperature



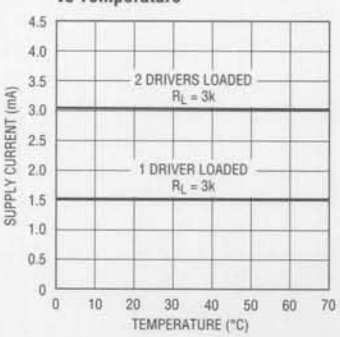
Receiver Input Thresholds vs Temperature



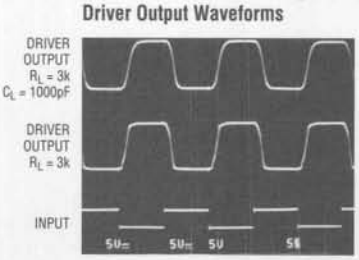
Supply Current vs Data Rate



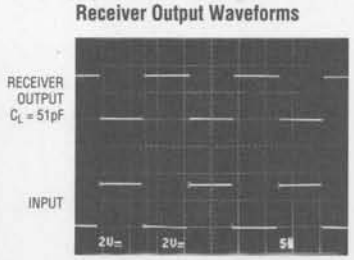
V_{CC} Supply Current vs Temperature



Driver Output Waveforms



Receiver Output Waveforms



5

PIN FUNCTIONS

V_{CC}: 3.3V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

V^+: Positive Supply Output (EIA/TIA562 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may share a common capacitor. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 1.3V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: EIA/TIA562 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip.

TR OUT: Driver Outputs at EIA/TIA562 Voltage Levels. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels.

SWITCHING TIME WAVEFORMS

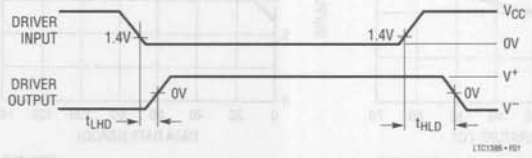


Figure 1. Driver Propagation Delay Timing

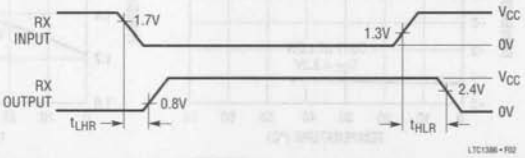
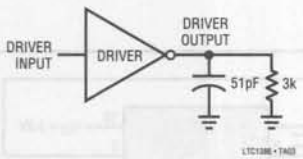


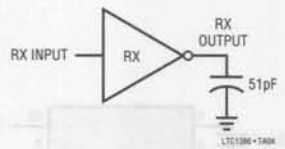
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

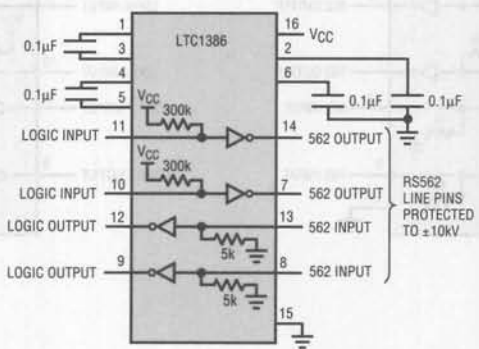
Driver Timing Test Load



Receiver Timing Test Load



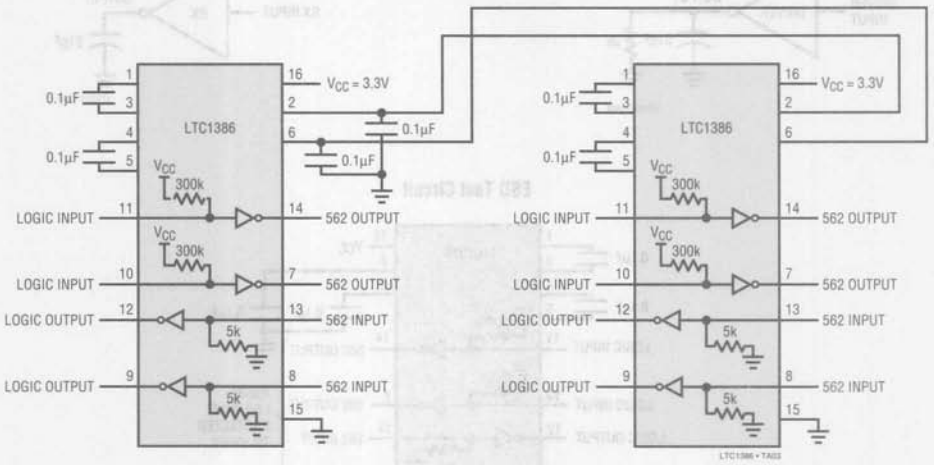
ESD Test Circuit



5

TYPICAL APPLICATIONS

Paralleling Power Supply Generator with Common Storage Capacitors



SECTION 5—INTERFACE

RS485

LTC488/LTC489, Quad RS485 Line Receiver 5-158
LTC1481, Ultra-Low Power RS485 Transceiver with Shutdown 13-122
LTC1483, Ultra-Low Power RS485 Low EMI Transceiver with Shutdown 13-129
LTC1485, Differential Bus Transceiver 5-166

5

Quad RS485 Line Receiver

FEATURES

- Low Power: I_{CC} = 7mA Typ.
- Designed for RS485 or RS422 Applications
- Single 5V Supply
- –7V to 12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- 60mV Typical Input Hysteresis
- Receiver Maintains High Impedance in Three-State or with the Power Off
- 28ns Typical Receiver Propagation Delay
- Pin Compatible with the SN75173 (LTC488)
- Pin Compatible with the SN75175 (LTC489)

APPLICATIONS

- Low Power RS485/RS422 Receivers
- Level Translator

DESCRIPTION

The LTC488 and LTC489 are low power differential bus/line receivers designed for multipoint data transmission standard RS485 applications with extended common mode range (12V to –7V). They also meet the requirements of RS422.

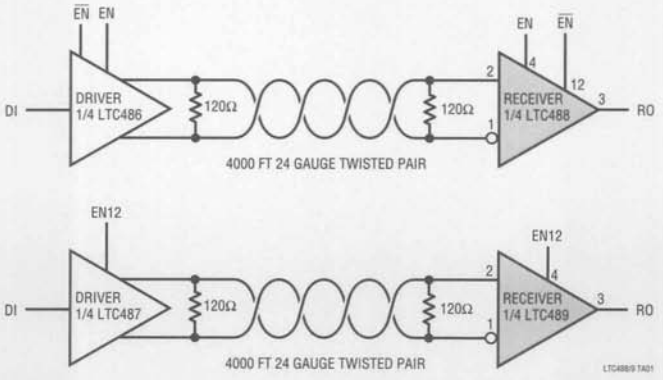
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The receiver features three-state outputs, with the receiver output maintaining high impedance over the entire common mode range.

The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION

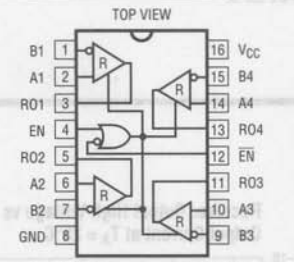


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Currents ..... – 25mA to 25mA
Control Input Voltages ..... –0.5V to V_{CC} + 0.5V
Receiver Input Voltages ..... ±14V
Receiver Output Voltages ..... –0.5V to V_{CC} + 0.5V

Operating Temperature Range
LTC488C/LTC489C ..... 0°C to 70°C
LTC488I/LTC489I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

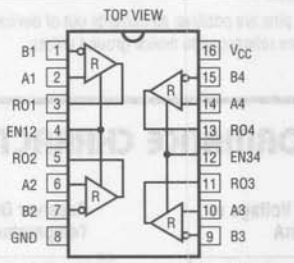


N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N PKG)
T_{JMAX} = 150°C, θ_{JA} = 90°C/W (S PKG)

ORDER PART NUMBER

LTC488CN
LTC488CS
LTC488IN
LTC488IS



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N PKG)
T_{JMAX} = 150°C, θ_{JA} = 90°C/W (S PKG)

ORDER PART NUMBER

LTC489CN
LTC489CS
LTC489IN
LTC489IS

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 5% (Notes 2 ,3 and 4), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INH}	Input High Voltage	EN, $\overline{EN}$, EN12, EN34	●	2.0			V
V_{INL}	Input Low Voltage	EN, $\overline{EN}$, EN12, EN34	●			0.8	V
I_{IN1}	Input Current	EN, $\overline{EN}$, EN12, EN34	●			±2	µA
I_{IN2}	Input Current (A, B)	V_{CC} = 0V or 5.25V, V_{IN} = 12V V_{CC} = 0V or 5.25V, V_{IN} = –7V	● ●			1.0 –0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	–7V ≤ V_{CM} ≤ 12V	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V			60		mV
V_{OH}	Receiver Output High Voltage	I_O = –4mA, V_{ID} = 0.2V	●	3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, V_{ID} = –0.2V	●			0.4	V
I_{OZR}	Three-State Output Current at Receiver	V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V	●			±1	µA
I_{CC}	Supply Current	No Load	●		7	10	mA
R_{IN}	Receiver Input Resistance	–7V ≤ V_{CM} ≤ 12V, V_{CC} = 0V	●	12			kΩ
I_{OSR}	Receiver Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7		85	mA
t_{PLH}	Receiver Input to Output	C_L = 15pF (Figures 1, 3)	●	12	28	55	ns
t_{PHL}	Receiver Input to Output	C_L = 15pF (Figures 1, 3)	●	12	28	55	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	C_L = 15pF (Figures 1, 3)			4		ns

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DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5% (Notes 2 and 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ZL}	Receiver Enable to Output Low	C_L = 15pF (Figures 2, 4) S1 Closed	●		30	60	ns
t_{ZH}	Receiver Enable to Output High	C_L = 15pF (Figures 2, 4) S2 Closed	●		30	60	ns
t_{LZ}	Receiver Disable from Low	C_L = 15pF (Figures 2, 4) S1 Closed	●		30	60	ns
t_{HZ}	Receiver Disable from High	C_L = 15pF (Figures 2, 4) S2 Closed	●		30	60	ns

The ● denotes specifications which apply over the operating temperature range.

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

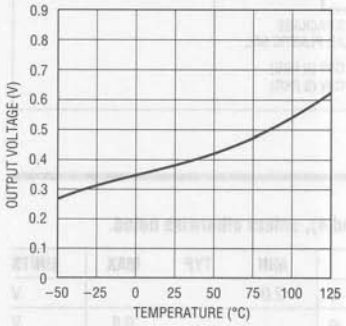
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

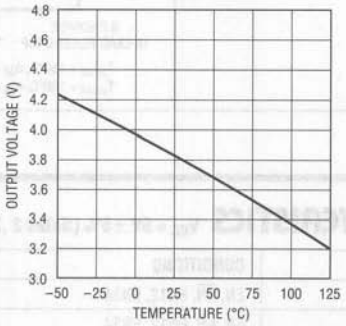
Note 4: The LTC488 is guaranteed by design to be functional over a supply voltage range of 5V ±10%. Data sheet parameters are guaranteed over the tested supply voltage range of 5V ±5%.

TYPICAL PERFORMANCE CHARACTERISTICS

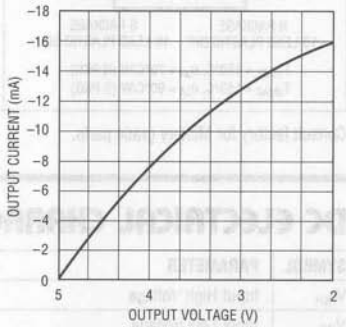
Receiver Output Low Voltage vs Temperature at I = 8mA



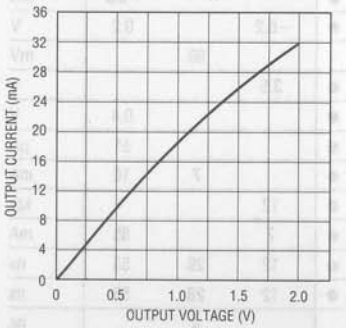
Receiver Output High Voltage vs Temperature at I = 8mA



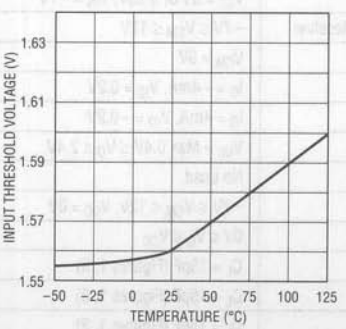
Receiver Output High Voltage vs Output Current at T_A = 25°C



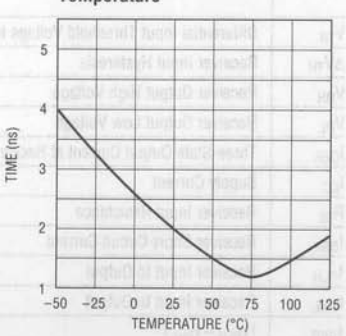
Receiver Output Low Voltage vs Output Current at T_A = 25°C



TTL Input Threshold vs Temperature

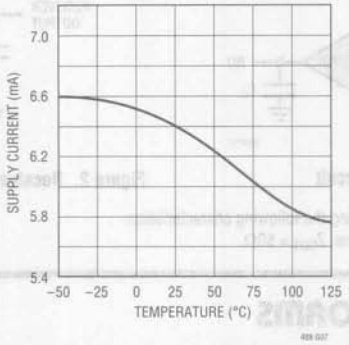


Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



PIN FUNCTIONS

PIN 1 (B1) Receiver 1 input.

PIN 2 (A1) Receiver 1 input.

PIN 3 (RO1) Receiver 1 output. If the receiver output is enabled, then if A > B by 200mV, RO1 will be high. If A < B by 200mV, then RO1 will be low.

PIN 4 (EN)(LTC488) Receiver output enabled. See Function Table for details.

PIN 4 (EN12)(LTC489) Receiver 1, Receiver 2 output enabled. See Function Table for details.

PIN 5 (RO2) Receiver 2 output. Refer to RO1.

PIN 6 (A2) Receiver 2 input.

PIN 7 (B2) Receiver 2 input.

PIN 8 (GND) Ground connection.

PIN 9 (B3) Receiver 3 input.

PIN 10 (A3) Receiver 3 input.

PIN 11 (RO3) Receiver 3 output. Refer to RO1.

PIN 12 ($\overline{EN}$)(LTC488) Receiver output disabled. See Function Table for details.

PIN 12 (EN34)(LTC489) Receiver 3, Receiver 4 output enabled. See Function Table for details.

PIN 13 (RO4) Receiver 4 output. Refer to RO1.

PIN 14 (A4) Receiver 4 input.

PIN 15 (B4) Receiver 4 input.

PIN 16 (V_{CC}) Positive Supply; 4.75V ≤ V_{CC} ≤ 5.25V

FUNCTION TABLES

LTC488

DIFFERENTIAL	ENABLES		OUTPUT
A – B	EN	$\overline{EN}$	RO
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$-0.2V < V_{ID} < 0.2V$	H	X	?
	X	L	?
$V_{ID} \leq 0.2V$	H	X	L
	X	L	L
X	L	H	Z

LTC489

DIFFERENTIAL	ENABLES	OUTPUT
A – B	EN12 or EN34	RO
$V_{ID} \geq 0.2V$	H	H
$-0.2V < V_{ID} < 0.2V$	H	?
$V_{ID} \leq 0.2V$	H	L
X	L	Z

H: High Level
L: Low Level
X: Irrelevant

?: Indeterminate
Z: High Impedance (Off)

5

TEST CIRCUITS

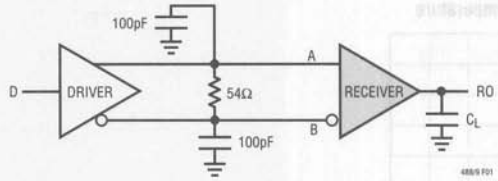


Figure 1. Receiver Timing Test Circuit

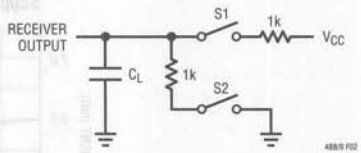


Figure 2. Receiver Enable and Disable Timing Test Circuit

Note: The input pulse is supplied by a generator having the following characteristics: f = 1MHz, Duty Cycle = 50%, t_r < 10ns, $t_f \leq$ 10ns, Z_{OUT} = 50Ω

SWITCHING TIME WAVEFORMS

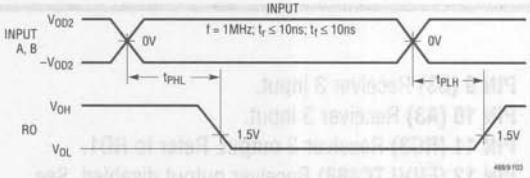


Figure 3. Receiver Propagation Delays

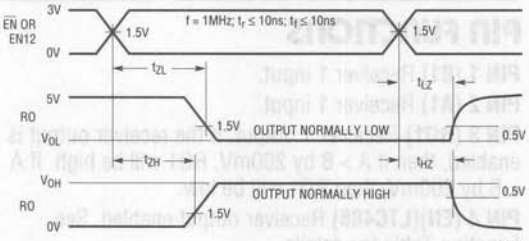


Figure 4. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

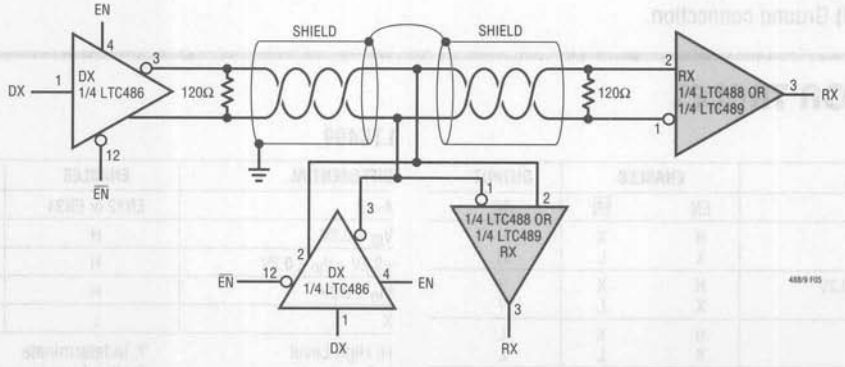


Figure 5. Typical Connection

APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC488/LTC489 is shown in Figure 5. Two twisted-pair wires connect up to 32 driver/receiver pairs for half-duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. The input impedance of a receiver is typically 20k to GND, or 0.5 unit RS485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted-pair help reduce unwanted noise, and are connected to GND at one end.

Cables and Data Rate

The transmission line of choice for RS485 applications is a twisted-pair. There are coaxial cables (twinaxial) made for this purpose that contain straight-pairs, but these are less flexible, more bulky, and more costly than twisted-pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cable such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low overall loss (Figure 6).

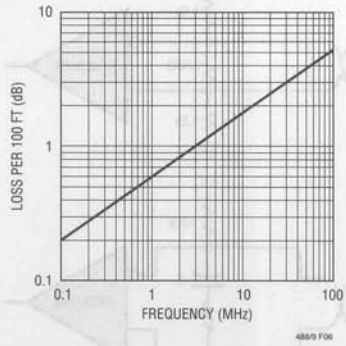


Figure 6. Attenuation vs Frequency for Belden 9841

When using low loss cables, Figure 7 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted-pairs have terrible losses at high data rates (> 100kbps), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

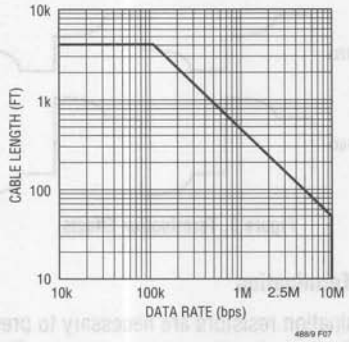


Figure 7. Cable Length vs Data Rate

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with its characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 8).

If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot). If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the drive output. An input frequency of 30kHz is adequate for tests out to 4000 ft. of cable.

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APPLICATIONS INFORMATION

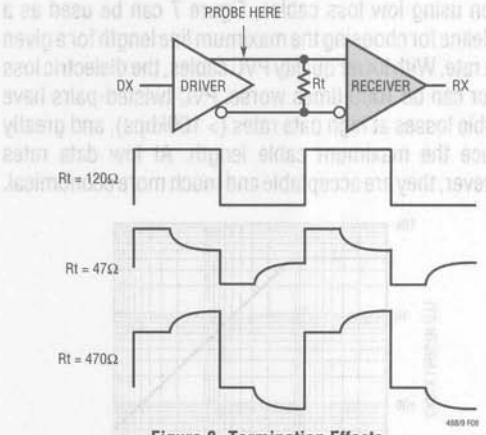


Figure 8. Termination Effects

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 60 times greater than the supply current of the LTC488/LTC489. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 9.

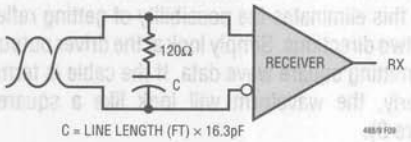


Figure 9. AC Coupled Termination

The coupling capacitor must allow high frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 4000 ft. in length. Be aware that the power savings start to decrease once the data rate surpasses $1/(120\Omega \times C)$.

Receiver Open-Circuit Fail-Safe

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced in three-state. The receiver of the LTC488/LTC489 has a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 60mV of hysteresis, the receiver output will maintain the last data bit received. If the receiver output must be forced to a known state, the circuits of Figure 10 can be used.

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this

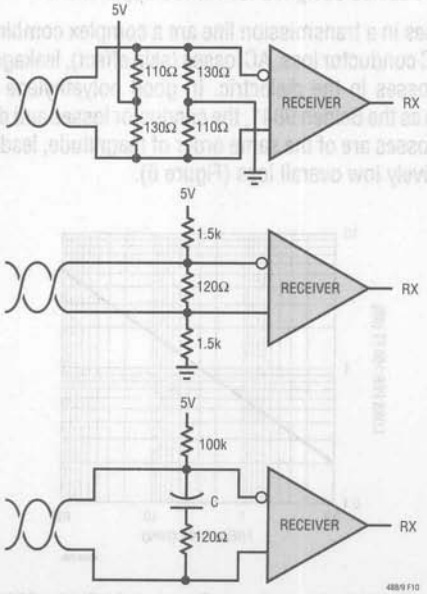


Figure 10. Forcing "0" When All Drivers Are Off

APPLICATIONS INFORMATION

case a logic 0. The first method consumes about 208mW and the second about 8mW. The lowest power solution is to use an AC termination with a pullup resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

Fault Protection

All of LTC's RS485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5k). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 11).

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General instruments, GSI, and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

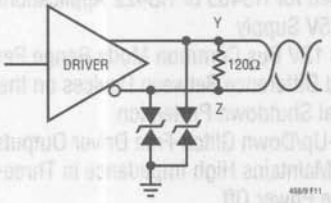
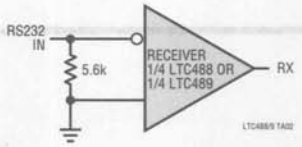


Figure 11. ESD Protection with TransZorbs®

TransZorb is a registered trademark of General Instruments, GSI

TYPICAL APPLICATIONS

RS232 Receiver



Differential Bus Transceiver

FEATURES

- Low Power: I_{CC} = 1.8mA Typ.
- 28ns Typical Driver Propagation Delays with 4ns Skew
- Designed for RS485 or RS422 Applications
- Single 5V Supply
- –7V to 12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs
- Driver Maintains High Impedance in Three-State or with the Power Off
- Combined Impedance of a Driver Output and Receiver Allows up to 32 Transceivers on the Bus
- 60mV Typical Input Hysteresis
- Pin-Compatible with the SN75176A, DS75176A, and SN75LBC176

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

The LTC1485 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common mode range (12V to –7V). It also meets the requirements of RS422.

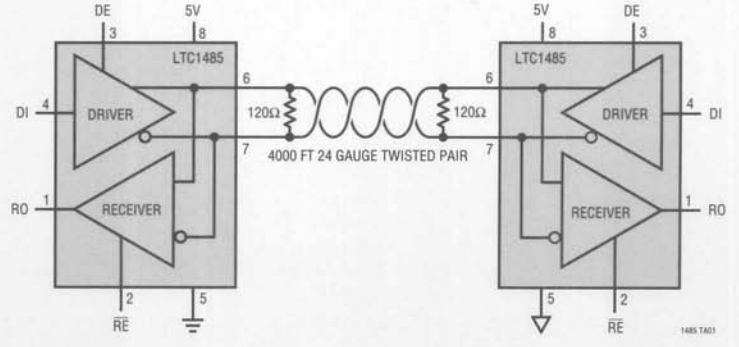
The CMOS with Schottky design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from –40°C to 85°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION

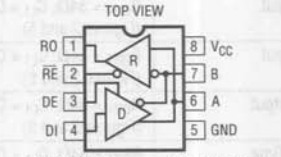


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltages ..... $-0.5V$ to $V_{CC} + 0.5V$
Control Input Currents ..... $-50mA$ to $50mA$
Driver Input Voltages ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Currents ..... $-25mA$ to $25mA$
Driver Output Voltages ..... $\pm14V$
Receiver Input Voltages ..... $\pm14V$
Receiver Output Voltages ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1485C ..... 0°C to 70°C
LTC1485I ..... $-40°C$ to 85°C
Storage Temperature Range ..... $-65°C$ to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = XXX°C, θ_{JA} = XXX°C/W (N8)
T_{JMAX} = XXX°C, θ_{JA} = XXX°C/W (S8)

ORDER PART NUMBER
LTC1485CN8 LTC1485IN8 LTC1485CS8 LTC1485IS8
S8 PART MARKING
1485 1485I

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 5% (Notes 2 and 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●		5	V	
V_{OD2}	Differential Driver Output Voltage (With Load)	R = 50Ω; (RS422)	●	2			V
		R = 27Ω; (RS485) (Figure 1)	●	1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Driver Common Mode Output Voltage	R = 27Ω or R = 50Ω (Figure 1)	●			3	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
V_{INH}	Input High Voltage	DI, DE, $\overline{RE}$	●	2.0			V
V_{INL}	Input Low Voltage	DI, DE, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DI, DE, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	V_{CC} = 0V or 5.25V, V_{IN} = 12V	●			1.0	mA
		V_{CC} = 0V or 5.25V, V_{IN} = −7V	●			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		60		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 0.2V$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -0.2V$	●			0.4	V
I_{OZR}	Three-State Output Current at Receiver	V_{CC} = Max $0.4V \le V_O \le 2.4V$	●			±1	µA
I_{CC}	Supply Current	No Load; DI = GND or V_{CC}					
		Outputs Enabled	●		1.8	2.3	mA
		Outputs Disabled	●		1.7	2.3	mA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = High	$V_O = -7V$	●			250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = Low	$V_O = 10V$	●			250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

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SWITCHING CHARACTERISTICS

V_{CC} = 5V ± 5% (Notes 2 and 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 5)	●	10	30	50	ns
t_{PHL}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 5)	●	10	30	50	ns
t_{SKEW}	Driver Output to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 5)	●		4	10	ns
t_r, t_f	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 5)	●	5	15	25	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 7)	●	15	25	50	ns
t_{PHL}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 7)	●	20	30	55	ns
t_{SKEW}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2 and 7)	●		5	15	ns
t_{ZL}	Receiver Enable to Output Low	C_L = 15pF (Figures 3 and 8) S1 Closed	●		30	45	ns
t_{ZH}	Receiver Enable to Output High	C_L = 15pF (Figures 3 and 8) S2 Closed	●		30	45	ns
t_{LZ}	Receiver Disable from Low	C_L = 15pF (Figures 3 and 8) S1 Closed	●		30	45	ns
t_{HZ}	Receiver Disable from High	C_L = 15pF (Figures 3 and 8) S2 Closed	●		30	45	ns

The ● denotes specifications which apply over the operating temperature range.

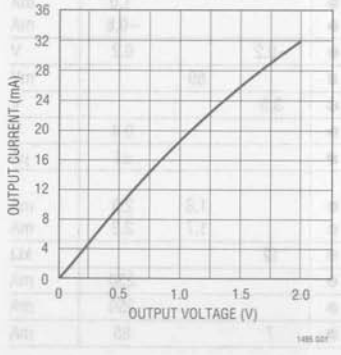
Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

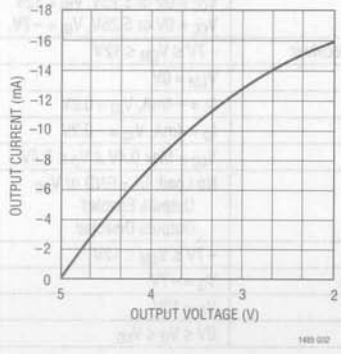
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

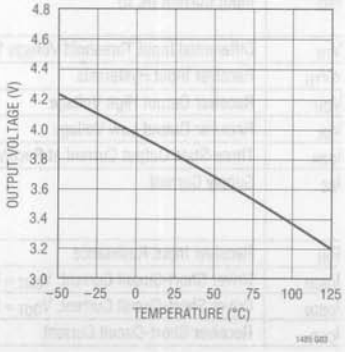
Receiver Output Low Voltage vs Output Current at T_A = 25°C



Receiver Output High Voltage vs Output Current at T_A = 25°C

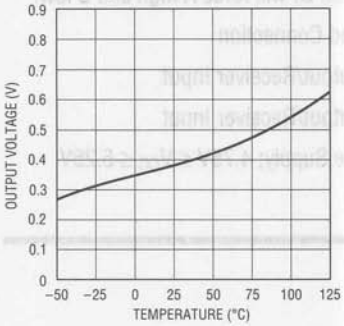


Receiver Output High Voltage vs Temperature at I = 8mA

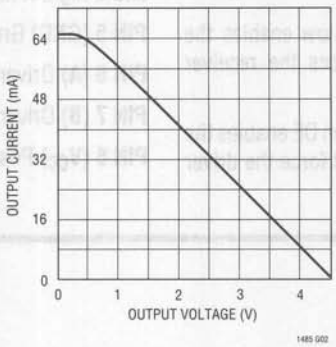


TYPICAL PERFORMANCE CHARACTERISTICS

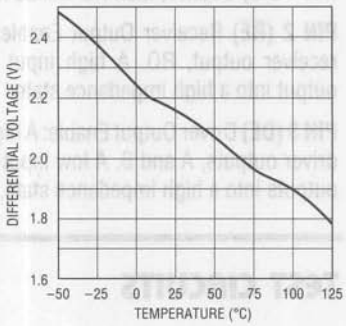
Receiver Output Low Voltage vs Temperature at I = 8mA



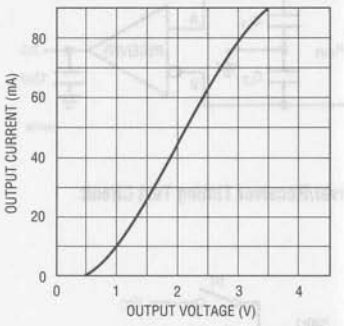
Driver Differential Output Voltage vs Output Current at T_A = 25°C



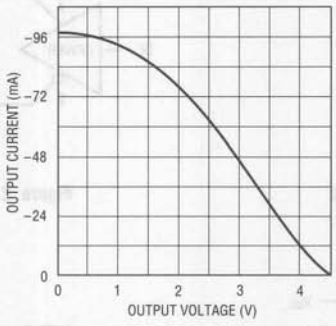
Driver Differential Output Voltage vs Temperature at R_L = 54Ω



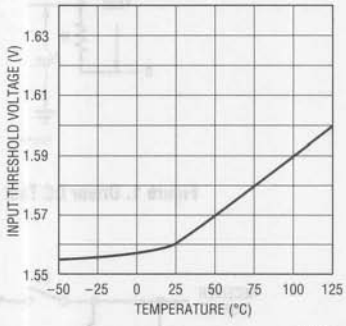
Driver Output Low Voltage vs Output Current at T_A = 25°C



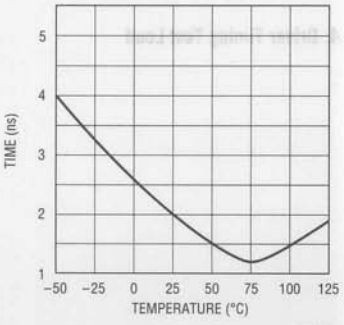
Driver Output High Voltage vs Output Current at T_A = 25°C



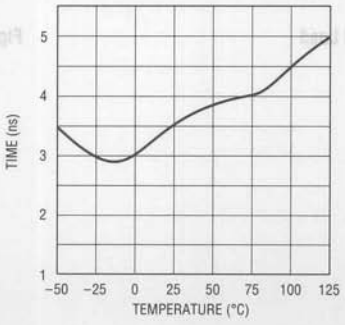
TTL Input Threshold vs Temperature



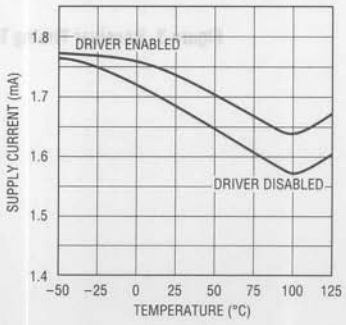
Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



Driver Skew vs Temperature



Supply Current vs Temperature



5

PIN FUNCTIONS

PIN 1 (RO) Receiver Output: If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

PIN 2 ($\overline{RE}$) Receiver Output Enable: A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

PIN 3 (DE) Driver Output Enable: A high on DE enables the driver outputs, A and B. A low input will force the driver outputs into a high impedance state.

PIN 4 (DI) Driver Input: If the driver outputs are enabled (DE high), then a low on DI forces the driver outputs A low and B high. A high on DI will force A high and B low.

PIN 5 (GND) Ground Connection

PIN 6 (A) Driver Output/Receiver Input

PIN 7 (B) Driver Output/Receiver Input

PIN 8 (V_{CC}) Positive Supply; 4.75V ≤ V_{CC} ≤ 5.25V

TEST CIRCUITS

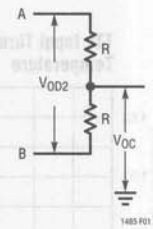


Figure 1. Driver DC Test Load

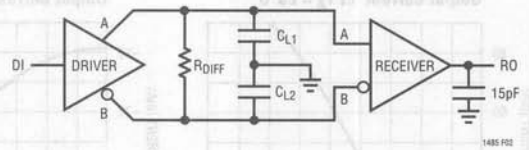


Figure 2. Driver/Receiver Timing Test Circuit

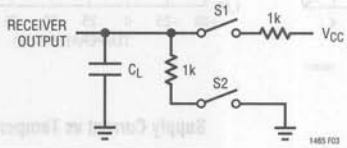


Figure 3. Receiver Timing Test Load

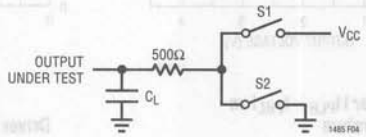


Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

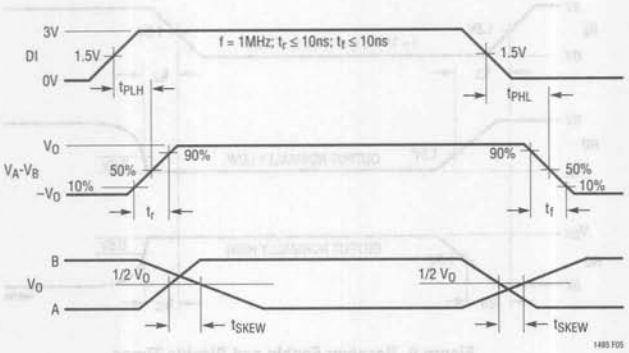


Figure 5. Driver Propagation Delays

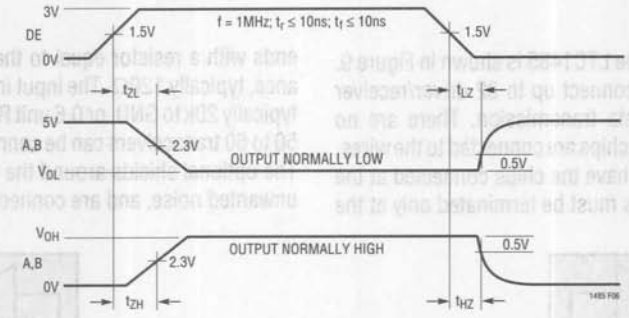


Figure 6. Driver Enable and Disable Times

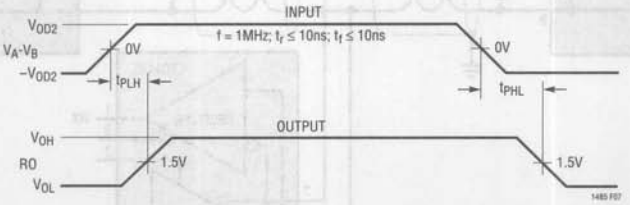


Figure 7. Receiver Propagation Delays

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SWITCHING TIME WAVEFORMS

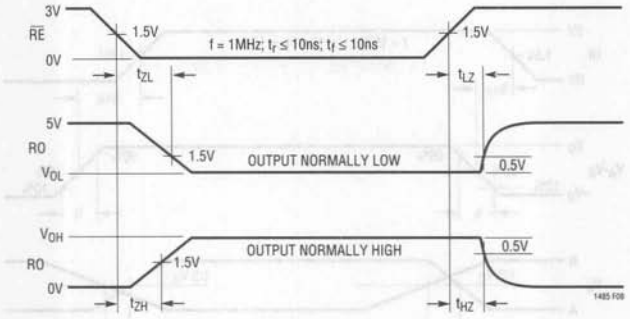


Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC1485 is shown in Figure 9. Two twisted pair wires connect up to 32 driver/receiver pairs for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. The input impedance of a receiver is typically 20k to GND, or 0.6 unit RS485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

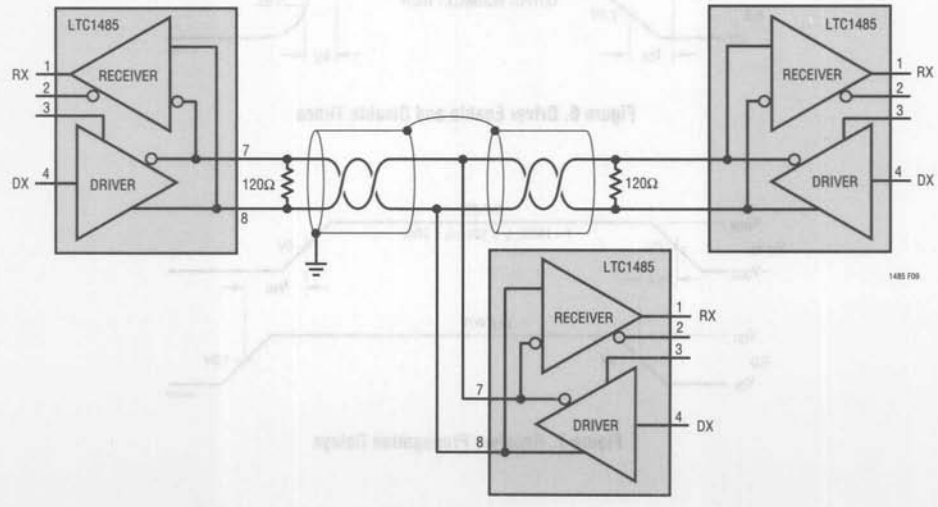


Figure 9. Typical Connection

APPLICATIONS INFORMATION

Thermal Shutdown

The LTC1485 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidentally shorted to a power supply or low impedance source, up to 250mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. If the outputs of two or more LTC1485 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown. Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

Cables and Data Rate

The transmission line of choice for RS485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low overall loss (Figure 10).

When using low loss cables, Figure 11 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (>100kbs), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with its characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable,

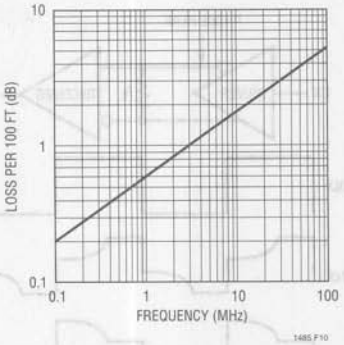


Figure 10. Attenuation vs Frequency for Belden 9481

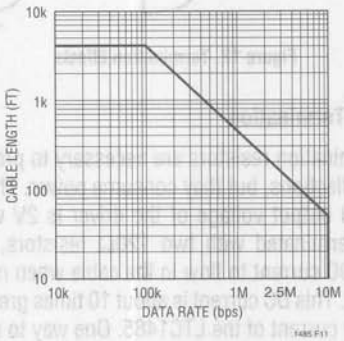


Figure 11. Cable Length vs Data Rate

since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 12).

If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot). If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30kHz is adequate for tests out to 4000 feet of cable.

5

APPLICATIONS INFORMATION

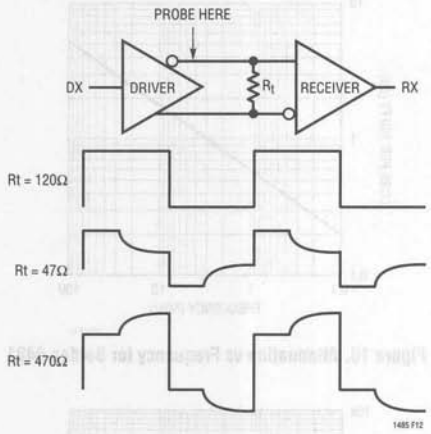


Figure 12. Termination Effects

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 10 times greater than the supply current of the LTC1485. One way to eliminate the unwanted current is by AC-coupling the termination resistors as shown in Figure 13.

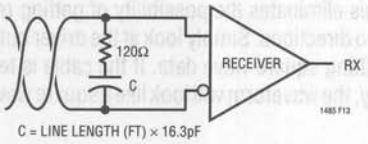


Figure 13. AC-Coupled Termination

The coupling capacitor must allow high frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 400 feet in length. Be aware that the power savings start to decrease once the data rate surpasses $1/(120\Omega \times C)$.

Receiver Open-Circuit Fail-Safe

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into three-state. The receiver of the LTC1485 has a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70mV of hysteresis, the receiver output will maintain the last data bit received.

If the receiver output must be forced to a known state, the circuits of Figure 14 can be used.

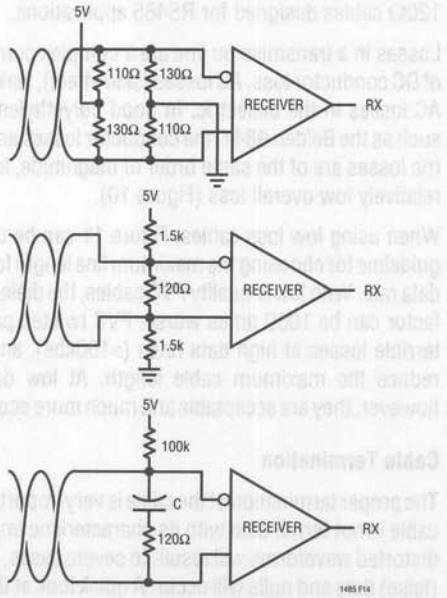


Figure 14. Forcing "0" When All Drivers Are Off

APPLICATIONS INFORMATION

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0. The first method consumes about 208mW and the second about 8mW. The lowest power solution is to use an AC termination with a pullup resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

Fault Protection

All of LTC's RS485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 15).

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

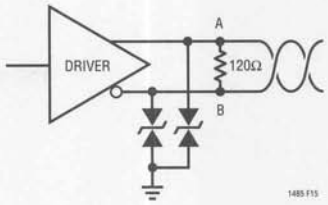
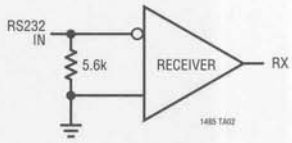


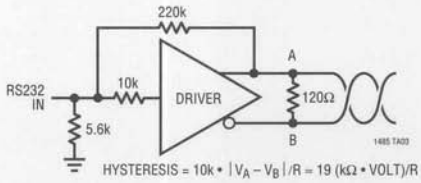
Figure 15. ESD Protection with TransZorbs

TYPICAL APPLICATIONS

RS232 Receiver



RS232 to RS485 Level Translator with Hysteresis



SECTION 5—INTERFACE

AppleTalk®

LTC1318, Single 5V RS232/RS422/AppleTalk® Transceiver 13-79
LTC1320, AppleTalk® Transceiver 5-178
LTC1323, Single 5V AppleTalk® Transceiver 13-85

FEATURES

- Single Chip Provides Complete LocalTalk®/AppleTalk® Port
- Low Power: I_{CC} = 1.2mA Typ
- Shutdown Pin Reduces I_{CC} to 30µA Typ
- Drivers Maintain High Impedance in Three-State or with Power Off
- 30ns Driver Propagation Delay Typ
- 5ns Driver Skew Typ
- Thermal Shutdown Protection
- Drivers are Short-Circuit Protected

APPLICATIONS

- LocalTalk Peripherals
- Notebook/Palmtop Computers
- Battery-Powered Systems

AppleTalk and LocalTalk are registered trademarks of Apple Computer, Inc.

DESCRIPTION

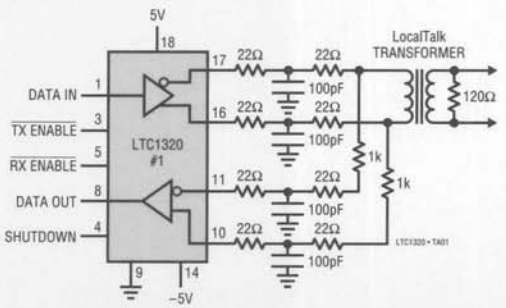
The LTC1320 is an RS422/RS562 line transceiver designed to operate on LocalTalk networks. It provides one differential RS422 driver, one single-ended RS562 driver, two single-ended RS562 receivers, and one differential RS422 receiver. The LTC1320 draws only 1.2mA quiescent current when active and 30µA in shutdown, making it ideal for use in battery-powered devices and other systems where power consumption is a primary concern.

The LTC1320 drivers are specified to drive ±2V into 100Ω. Additionally, the driver outputs three-state when disabled, during shutdown, or when the power is off; they maintain high impedance even with output common-mode voltages beyond the power supply rails. Both the driver outputs and receiver inputs are protected against ESD damage to beyond 5kV.

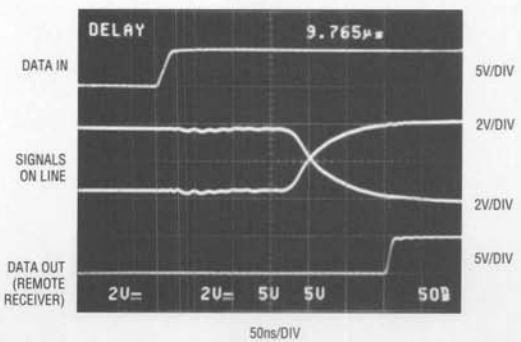
The LTC1320 is available in the 18-pin SOL package.

TYPICAL APPLICATION

Typical LocalTalk Connection



Output Waveforms

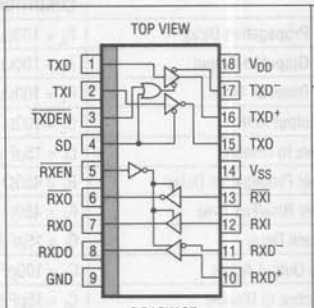


50ns/DIV

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}) 7V
Supply Voltage (V_{SS}) ..... −7V
Input Voltage (Logic Inputs) ..... −0.3V to V_{DD} + 0.3V
Input Voltage (Receiver Inputs) ..... ±15V
Driver Output Voltage (Forced) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C ot 70°C
Storage Temperature Range ..... −65°c to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1320CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_S = ±5V ±5%, T_A = 0°C to 70°C (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD}	Differential Driver Output Voltage	No Load R_L = 100Ω (Figure 1)	● ●	8.0 2.0			V V
	Change in Magnitude of Driver Differential Output Voltage	R_L = 100Ω (Figure 1)			0.2		V
V_{OC}	Driver Common-Mode Output Voltage	R_L = 100Ω (Figure 1)			3		V
	Output Common-Mode Range	SD = 5V or Power Off	●			±10	V
	Single-Ended Driver Output Voltage	No Load R_L = 400Ω	● ●	±4.0 ±3.4			V V
	Input High Voltage	All Logic Input Pins	●	2.0			V
	Input Low Voltage	All Logic Input Pins	●			0.8	V
	Input Current	All Logic Input Pins	●		±1	±20	µA
	Three-State Output Current	SD = 5V or Power Off, −10V < V_O < 10V	●		±2	±100	µA
	Driver Short-Circuit Current	−5V < V_O < 5V	●	35	350	500	mA
	Receiver Input Resistance	−7V < V_{IN} < 7V	●	12			kΩ
V_{OH}	Receiver Output High Voltage	I_O = −4mA	●	3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA	●			0.4	V
	Receiver Output Short-Circuit Current	0V < V_O < 5V	●	7		85	mA
	Receiver Output Three-State Current	0V < V_O < 5V	●		±2	±100	µA
	Differential Receiver Threshold Voltage	−7V < V_{CM} < 7V	●	−200		200	mV
	Differential Receiver Input Hysteresis	−7V < V_{CM} < 7V			70		mV
	Single-Ended Receiver Input Low Voltage		●			0.8	V
	Single-Ended Receiver Input High Voltage		●	2			V
I_{DD}	Supply Current	No Load, SD = 0V No Load, SD = 5V	● ●		1.2 30	3.0 350	mA µA
I_{SS}	Supply Current	No Load, SD = 5V	●		2	350	µA

5

SWITCHING CHARACTERISTICS

$V_S = \pm5V \pm5\%$, $T_A = 0°C$ to $70°C$ (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PLH, HL}$	Differential Driver Propagation Delay	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 8)	●		40	120	ns
t_{SKEW}	Differential Driver Output to Output	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 8)	●		10	50	ns
$t_{r, f}$	Differential Driver Rise/Fall Time	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 8)	●		15	80	ns
$t_{ENH, L}$	Driver Enable to Output Active	$C_L = 100pF$ (Figures 3, 4, 10)	●		50	150	ns
$t_{H, Ldis}$	Driver Output Active to Disable	$C_L = 15pF$ (Figures 3, 4, 10)	●		50	150	ns
$t_{PLH, HL}$	Single-Ended Driver Propagation Delay	$R_L = 450\Omega$, $C_L = 100pF$ (Figures 5, 11)	●		40	120	ns
$t_{r, f}$	Single-Ended Driver Rise/Fall Time	$R_L = 450\Omega$, $C_L = 100pF$ (Figures 5, 12)	●		15	80	ns
$t_{PLH, HL}$	Receiver Propagation Delay	$C_L = 15pF$ (Figures 13, 14)	●		60	160	ns
$t_{ENH, L}$	Receiver Enable to Output Active	$C_L = 100pF$ (Figures 6, 7, 15)	●		30	100	ns
$t_{H, Ldis}$	Receiver Output Active to Disable	$C_L = 15pF$ (Figures 6, 7, 15)	●		30	100	ns

The ● denotes specifications which apply over the full operating temperature range.

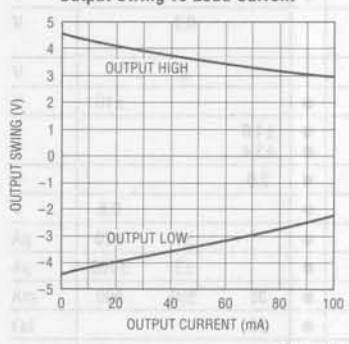
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

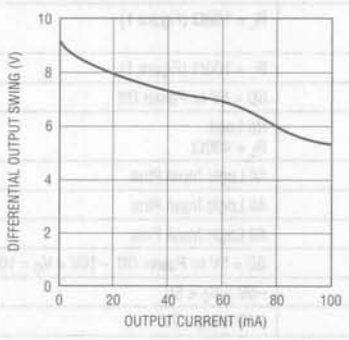
Note 3: All typicals are given at $V_S = \pm5V$, $T_A = 25°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

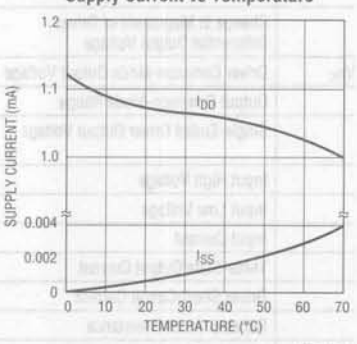
Output Swing vs Load Current



Differential Output Swing vs Load Current



Supply Current vs Temperature



PIN FUNCTIONS

TXD (Pin 1): RS422 Differential Driver Input (TTL Compatible).

TXI (Pin 2): RS562 Single-Ended Driver Input (TTL compatible.

$\overline{\text{TXDEN}}$ (Pin 3): RS422 Differential Driver Output Enable (TTL Compatible). A high level on this pin forces the RS422 driver into three-state; a low level enables the driver. This input does not affect the RS562 single-ended driver.

SD (Pin 4): Shutdown Input (TTL Compatible). When this pin is high, the chip is shut down: all driver outputs three-state and the supply current drops to 30μA. A low on this pin allows normal operation.

PIN FUNCTIONS

$\overline{\text{RXEN}}$ (Pin 5): Receiver Enable (TTL Compatible). A high level on this pin disables the receivers and three-states the logic outputs; a low level allows normal operation. To prevent erratic behavior at the receiver outputs during shutdown, $\overline{\text{RXEN}}$ should be pulled high along with SD.

$\overline{\text{RXO}}$ (Pin 6): Inverting RS562 Single-Ended Receiver Output.

RXO (Pin 7): Noninverting RS562 Single-Ended Receiver Output.

RXDO (Pin 8): RS422 Differential Receiver Output.

GND (Pin 9): Ground Pin.

RXD$^+$ (Pin 10): RS422 Differential Receiver Noninverting Input. When this pin is ≥200mV above RXD$^-$, RXDO will be high; when this pin is ≥200mV below RXD$^-$, RXDO will be low.

RXD$^-$ (Pin 11): RS422 Differential Receiver Inverting Input.

RXI (Pin 12): Noninverting RS562 Receiver Input. This input controls the RXO output; it has no effect on the $\overline{\text{RXO}}$ output.

$\overline{\text{RXI}}$ (Pin 13): Inverting RS562 Receiver Input. This input controls the $\overline{\text{RXO}}$ output; it has no effect on the RXO output.

V_{SS} (Pin 14): Negative Supply. $-4.75 \geq V_{SS} \geq -5.25V$. The voltage on this pin must never exceed ground on power up or power-down.

TXO (Pin 15): RS562 Single-Ended Driver Output.

TXD$^+$ (Pin 16): RS422 Differential Driver Noninverting Output.

TXD$^-$ (Pin 17): RS422 Differential Driver Inverting Output.

V_{DD} (Pin 18): Positive Supply. $4.75V \leq V_{DD} \leq 5.25V$.

5

TEST CIRCUITS

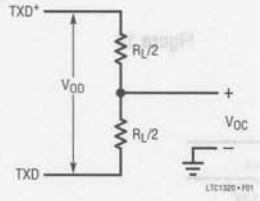


Figure 1

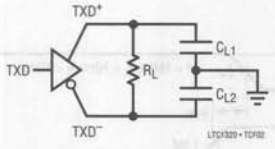


Figure 2

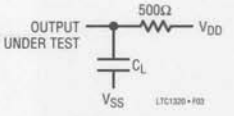


Figure 3

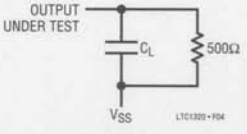


Figure 4

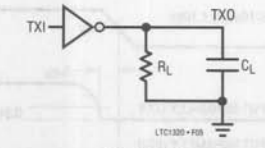


Figure 5

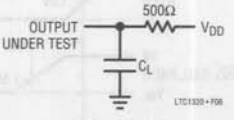


Figure 6

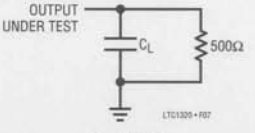


Figure 7

SWITCHING WAVEFORMS

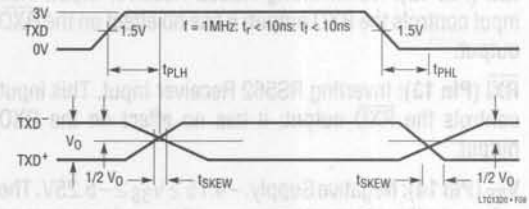


Figure 8

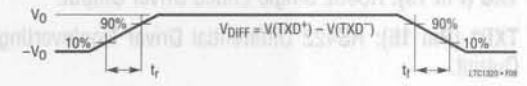


Figure 9

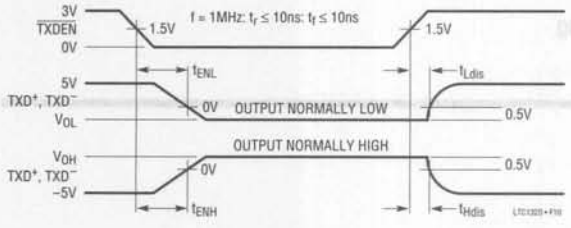


Figure 10

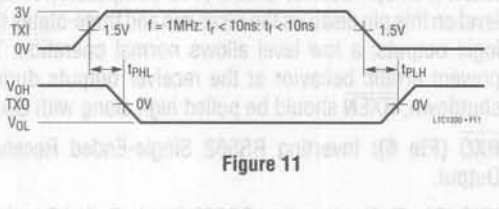


Figure 11

Figure 12

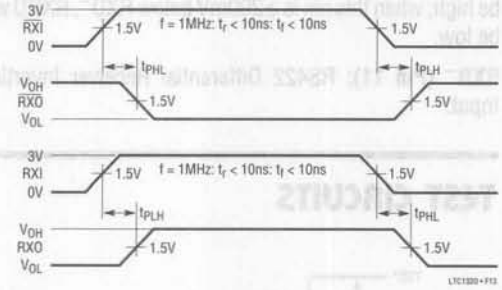


Figure 13

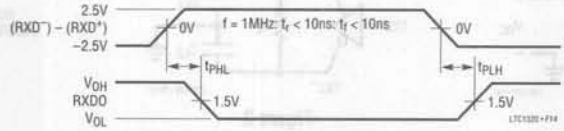


Figure 14

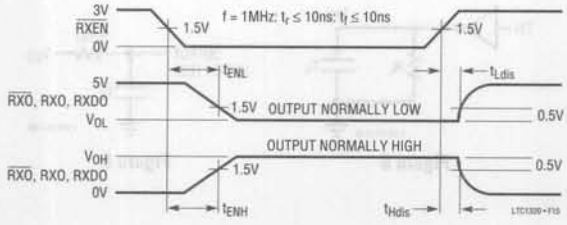


Figure 15

APPLICATIONS INFORMATION

Thermal Shutdown Protection

The LTC1320 includes a thermal shutdown circuit which protects the part against prolonged shorts at the driver outputs. If any driver output is shorted to another output or to the power supply, the current will be initially limited to 450mA max. The die temperature will rise to about 150°C, at which point the thermal shutdown circuit turns off the driver outputs. When the die cools to about 130°C, the outputs re-enable. If the shorted condition still exists, the part will heat again and the cycle will repeat. When the short is removed, the part will return to normal operation. This oscillation occurs at about 10Hz and prevents the part from being damaged by excessive power dissipation.

Power Shutdown

The power shutdown feature of the LTC1320 is designed primarily for battery-powered systems. When SD (pin 4) is forced high, the part enters shutdown mode. In shutdown, the supply current drops from 1.2mA to 30µA typ. The driver outputs are three-stated and the power to the receivers is removed. The receiver outputs are not automatically three-stated in shutdown, and can toggle erroneously due to feedthrough from the inputs. This can be prevented by pulling $\overline{RXEN}$ high along with SD; this will three-state the receiver outputs and prevent the generation of spurious data.

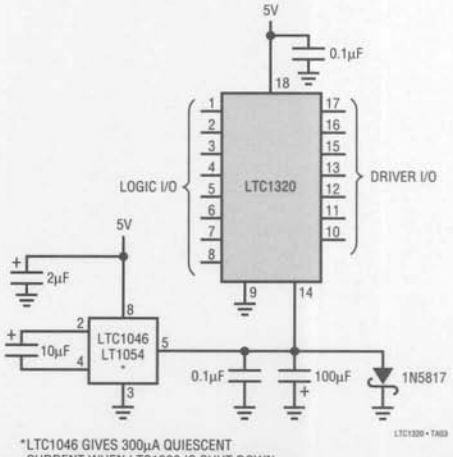
Supply Bypassing

The LTC1320 requires that both V_{DD} and V_{SS} are well bypassed; data errors can result from inadequate bypassing. Bypass capacitor values of 0.1µF to 1µF from V_{DD} to ground and from V_{SS} to ground are adequate. Lead lengths and trace lengths between the capacitors and the chip should be short to minimize lead inductance.

5

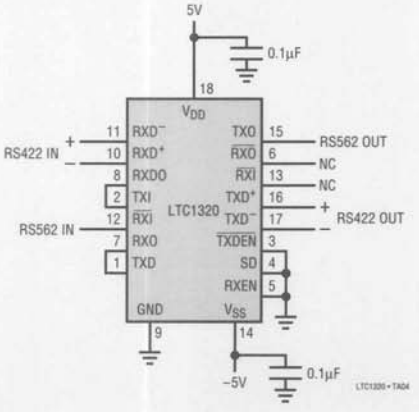
TYPICAL APPLICATIONS

Single 5V Supply



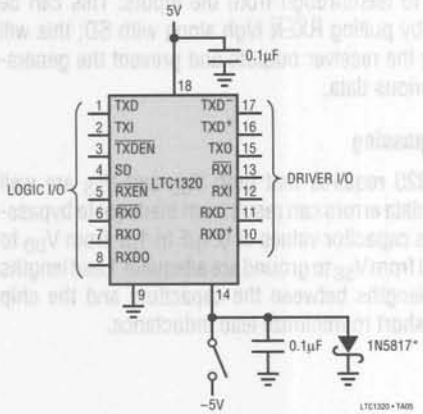
*LTC1046 GIVES 300µA QUIESCENT CURRENT WHEN LTC1320 IS SHUT DOWN
LT1054 PROVIDES HIGHER OUTPUT DRIVE

RS422 to RS562/RS562 to RS422 Converter



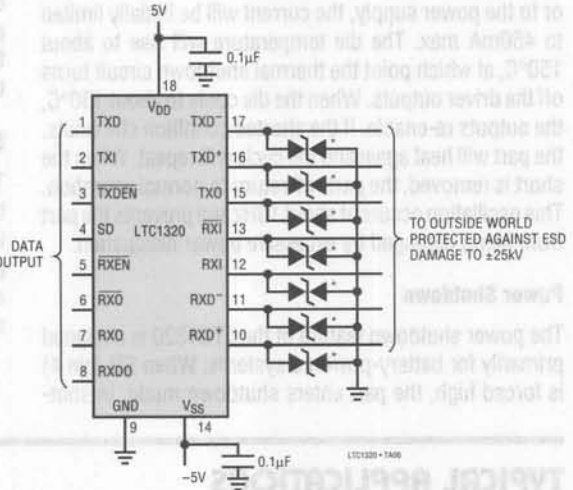
TYPICAL APPLICATIONS

Switched Negative Supply



*SCHOTTKY DIODE PREVENTS V_{SS} FROM EXCEEDING GND ON POWER-UP OR POWER-DOWN

≥25k ESD Protection



*GENERAL SEMICONDUCTOR ICTE-22C OR EQUIVALENT

SECTION 5—INTERFACE

DIGITAL ISOLATORS

LTC1145/LTC1146, Low Power Digital Isolator 5-186

Low Power Digital Isolator

FEATURES

- UL Recognized (LTC1145A, LTC1146A) File E151738 to UL1577
- **Low Input Current**
  LTC1145: 700μA
  LTC1146: 70μA
- Maximum Input Frequency
  LTC1145: 200kHz
  LTC1146: 20kHz
- TTL Level Output
- Noise Filter Prevents Glitches at the Output
- Output Can Be Synchronized to an External Clock

APPLICATIONS

- Low Power Opto-Isolator Replacement
- Isolated Serial Data Interfaces
- Isolated Power MOSFET Drivers

DESCRIPTION

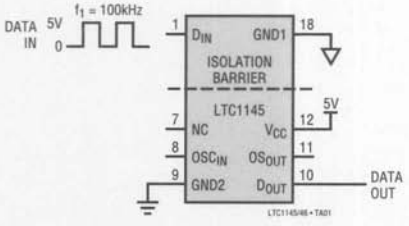
The LTC1145A/LTC1146A provide $2500V_{RMS}$ (1minute) or $3000V_{RMS}$ (1 second) of input to output isolation for TTL digital/CMOS signals. The LTC1145/LTC1146 are intended for less stringent applications and are rated for $500V_{RMS}$. Unlike opto-isolators, the input current is a mere 70μA for the LTC1146 which can handle frequencies up to 20kHz. The faster LTC1145 will handle frequencies up to 200kHz while only drawing 700μA.

The output signal is in phase with the input and swings between GND2 and V_{CC} providing a TTL/CMOS compatible signal without any pull-up resistors. An on-chip noise filter helps prevent glitches and data errors at the output, and a pin is provided for synchronizing the output signal to an external system clock.

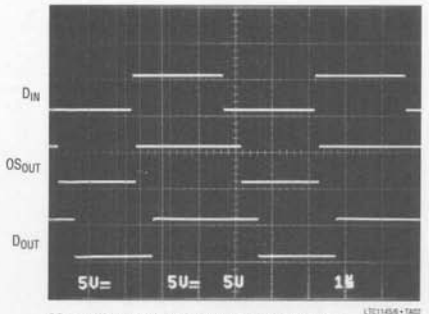
EDN IC Innovation of the Year Winner

TYPICAL APPLICATION

Digital Isolation Interface
Data Rate Up to 200kHz



LTC1145 Typical Waveforms



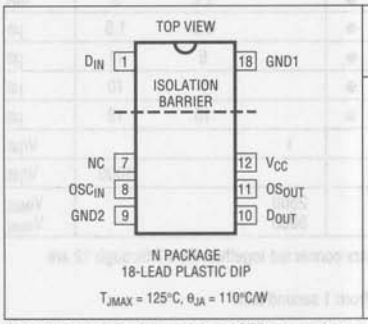
OS_{OUT} AND D_{OUT} LOADED WITH 15pF SCOPE PROBE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 12V
Input Voltage
D_{IN} ..... 11V to (GND1 – 0.3V)
OSC_{IN} ..... (V_{CC} + 0.3V) to (GND2 – 0.3V)
Output Voltage
OS_{OUT}, D_{OUT} ..... (V_{CC} + 0.3V) to (GND2 – 0.3V)

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

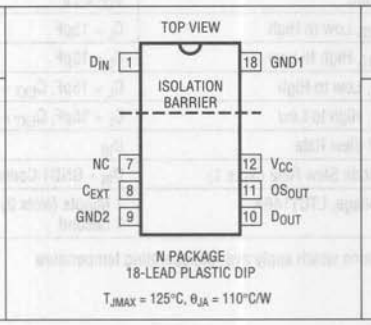


N PACKAGE
18-LEAD PLASTIC DIP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1145CN
LTC1145ACN



N PACKAGE
18-LEAD PLASTIC DIP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1146CN
LTC1146ACN

Consult factory for Industrial and Military grade parts.

5

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LTC1145							
V_{OL}	Output Low Voltage	OS_{OUT}, D_{OUT} at 4mA	●			0.4	V
V_{OH}	Output High Voltage	OS_{OUT}, D_{OUT} at 4mA	●	3.5			V
V_{IL}	External Frequency Input Low Voltage	OSC_{IN}	●			0.8	V
V_{IH}	External Frequency Input High Voltage	OSC_{IN}	●	2.4			V
I_{IN}	Input Current	OSC_{IN} at 5V D_{IN} at 3V D_{IN} at 5V D_{IN} at 10V	● ● ● ●		 0.45 0.70 1.85	10.0 0.65 1.30 3.20	µA mA mA mA
I_{CC}	Supply Current	OSC_{IN} = 0V	●		2	3.5	mA
t_{PLH1}	D_{IN} to OS_{OUT}, Low to High	C_L = 15pF	●		0.2	0.7	µs
t_{PHL1}	D_{IN} to OS_{OUT}, High to Low	C_L = 15pF	●		0.4	1.1	µs
t_{PLH2}	D_{IN} to D_{OUT}, Low to High	C_L = 15pF	●		0.7	1.5	µs
t_{PHL2}	D_{IN} to D_{OUT}, High to Low	C_L = 15pF	●		1.1	2	µs
SR	Input Signal Slew Rate	D_{IN}		1			V/µs
CMSR	Common-Mode Slew Rate (Note 1)	D_{IN} = GND1 Connected to V_{CM}				1000	V/µs
V_{INH}	Input High Voltage	D_{IN}	●	3			V
V_{INL}	Input Low Voltage	D_{IN}	●			0.8	V
V_{ISO}	Isolation Voltage, LTC1145A	1 Minute (Note 2) 1 Second		2500 3000			V_{RMS} V_{RMS}

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LTC1146							
V_{OL}	Output Low Voltage	OS_{OUT}, D_{OUT} at 4mA	●			0.4	V
V_{OH}	Output High Voltage	OS_{OUT}, D_{OUT} at 4mA	●	3.5			V
V_{IL}	Input Low Voltage	D_{IN}	●			0.8	V
V_{IH}	Input High Voltage	D_{IN}	●	3			V
I_{IN}	Input Current	D_{IN} at 3V D_{IN} at 5V D_{IN} at 10V	● ● ●		40 70 225	80 120 350	µA µA µA
I_{CC}	Supply Current	V_{CC} = 5V	●		1.8	3	mA
t_{PLH1}	D_{IN} to OS_{OUT}, Low to High	C_L = 15pF	●		0.5	1.5	µs
t_{PHL1}	D_{IN} to OS_{OUT}, High to Low	C_L = 15pF	●		6	11	µs
t_{PLH2}	D_{IN} to D_{OUT}, Low to High	C_L = 15pF, C_{EXT} = 50pF	●		5	10	µs
t_{PHL2}	D_{IN} to D_{OUT}, High to Low	C_L = 15pF, C_{EXT} = 50pF	●		10	18	µs
SR	Input Signal Slew Rate	D_{IN}		1			V/µs
CMSR	Common-Mode Slew Rate (Note 1)	D_{IN} = GND1 Connected to V_{CM}				1000	V/µs
V_{ISO}	Isolation Voltage, LTC1146A	1 Minute (Note 2) 1 Second		2500 3000			V_{RMS} V_{RMS}

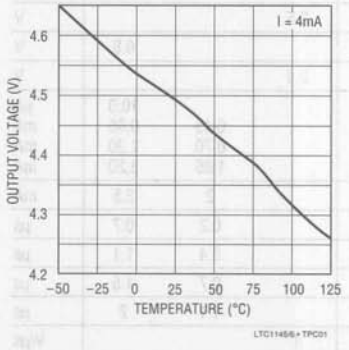
The ● denotes specifications which apply over the operating temperature range.

Note 1: Pins 1 and 18 are connected together. Pins 7 through 12 are connected together.

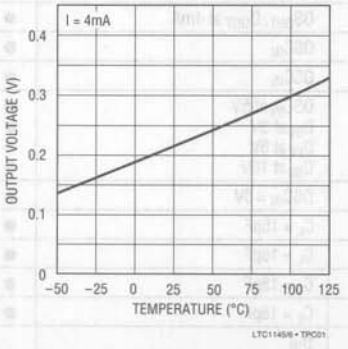
Note 2: Value derived from 1 second test.

TYPICAL PERFORMANCE CHARACTERISTICS

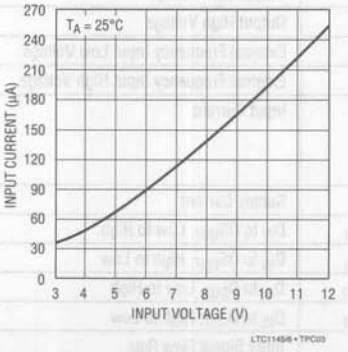
Output High Voltage (D_{OUT} and OS_{OUT}) vs Temperature



Output Low Voltage (D_{OUT} and OS_{OUT}) vs Temperature

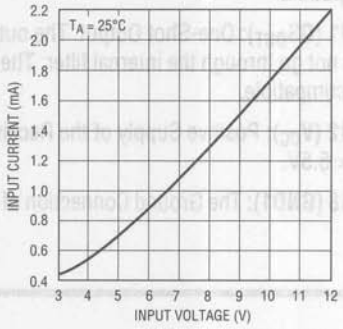


LTC1146 Input Current vs Input Voltage

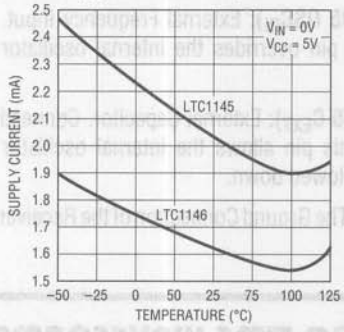


TYPICAL PERFORMANCE CHARACTERISTICS

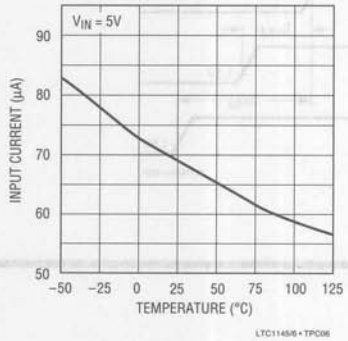
LTC1145
Input Current vs Input Voltage



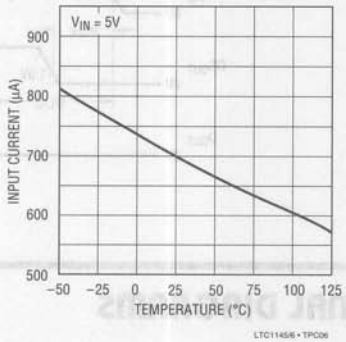
LTC1145/LTC1146
Supply Current vs Temperature



LTC1146
Input Current vs Temperature



LTC1145
Input Current vs Temperature



5

PIN FUNCTIONS

Pin 1 (D_{IN}): Data Input

Pin 7 (NC): Not Connected

Pin 8 (LTC1145 OSC_{IN}): External Frequency Input. The signal on this pin overrides the internal oscillator frequency.

Pin 8 (LTC1146 C_{EXT}): External Capacitor. Connecting a capacitor at this pin allows the internal oscillator frequency to be slowed down.

Pin 9 (GND2): The Ground Connection of the Receiver Die.

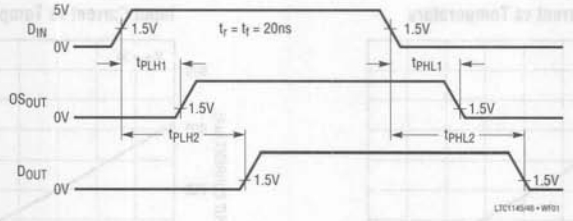
Pin 10 (D_{OUT}): Data Output. The output signal has gone through the internal filter. The output level is TTL compatible.

Pin 11 (OS_{OUT}): One-Shot Output. The output signal that does not go through the internal filter. The output level is TTL compatible.

Pin 12 (V_{CC}): Positive Supply of the Receiver Die, 4.5V < V_{CC} < 5.5V.

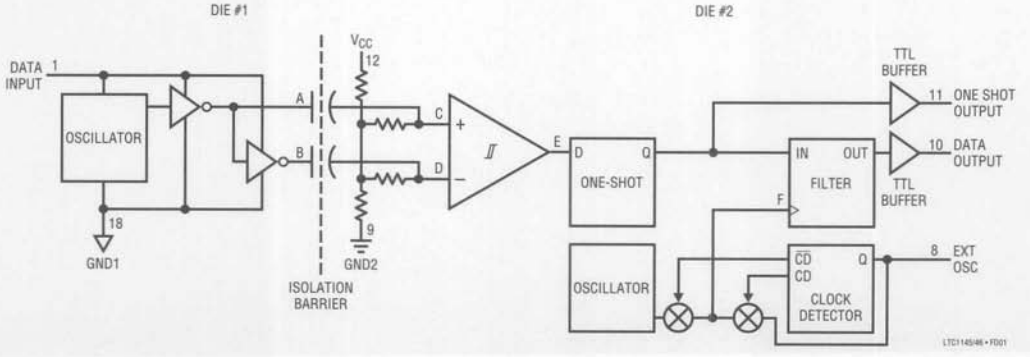
Pin 18 (GND1): The Ground Connection of the Driver Die.

SWITCHING TIME WAVEFORMS

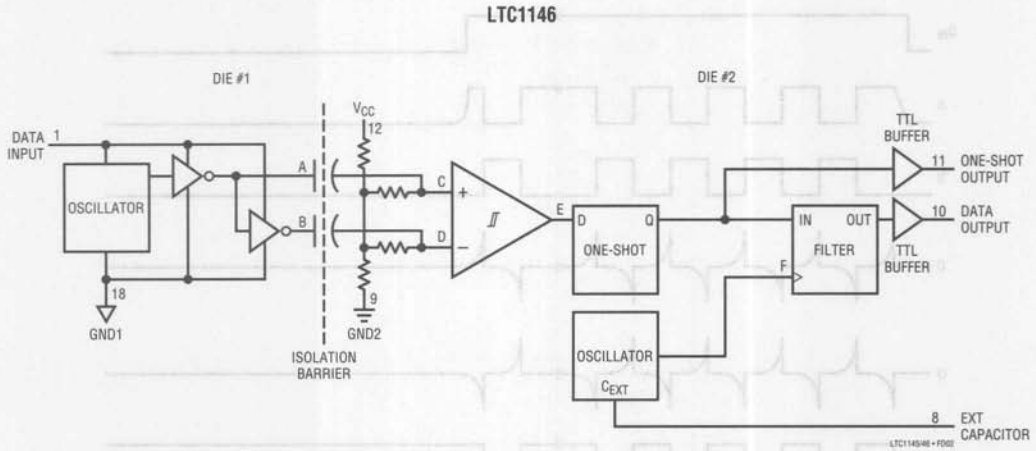


FUNCTIONAL DIAGRAMS

LTC1145



FUNCTIONAL DIAGRAMS



OPERATION

Basic Functionality

The LTC1145/LTC1146 consist of two separate die (see Functional Diagram) and two internal 1pF capacitors which provide isolation. Die #1 contains a low power oscillator and two low power drivers. The supply current for the oscillator and drivers comes from the digital input.

When the digital input exceeds 3V, the oscillator turns on and provides a 4MHz square wave to the drivers (400kHz for the LTC1146). The drivers pass the signal through the isolation capacitors and form a differential signal at the input to the comparator (points C and D) on die #2. As soon as the comparator output changes state in either direction, the one-shot output (OS) goes high. The time constant of the one-shot is set to 2 times the oscillation period, so the one-shot output will stay high as long as the oscillation continues. When the digital input goes low, the oscillator on die #1 turns off and the one-shot output resets low.

To increase the noise immunity of the system, a filter is added to die #2. The filter is basically a binary counter clocked by either an internal free running oscillator or external oscillator. A clock detector circuit disconnects the internal oscillator from the filter and connects the external oscillator after detecting three pulses on the OSC_{IN} pin. The frequency of the internal free running oscillator on die #2 is designed to match the frequency of the gated oscillator on die #1, but the two oscillators are not synchronized. For the digital output (D_{OUT}) to go high, the filter must count four consecutive clock cycles with the one-shot output remaining high. For the digital output to go low, the filter must count four consecutive clock cycles with the one-shot output remaining low.

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OPERATION

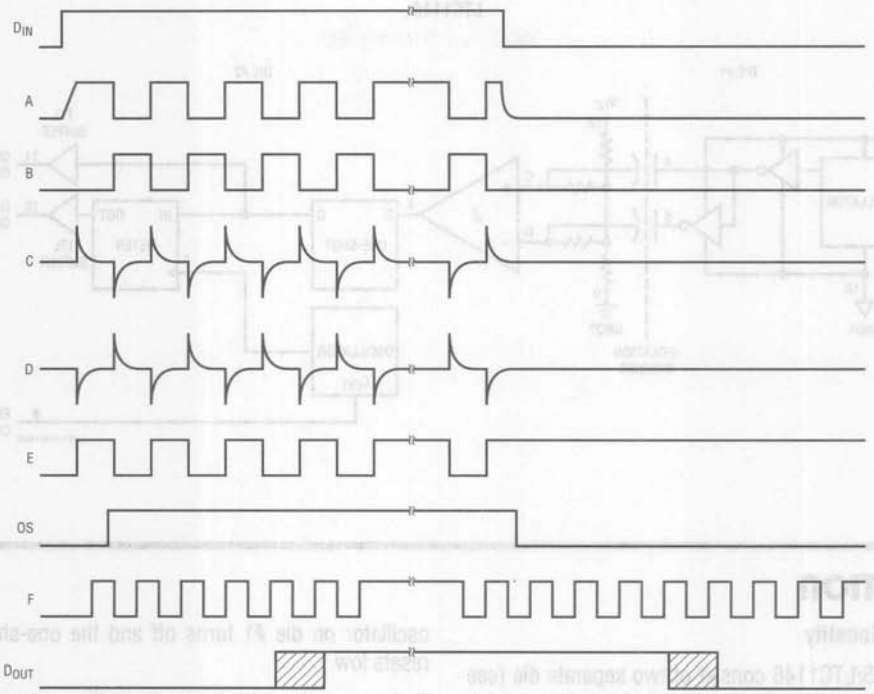


Figure 1. Block Diagram Waveforms

Noise and Glitch Immunity

As an example, assume that the digital input is low and the oscillator on die #1 is off. There is a very large fast rising common-mode signal at the ground and input pins to die #1 with respect to the ground of die #2.

Any mismatch in the internal capacitors will convert the common-mode signal into a differential glitch at the inputs to the comparator. The output of the comparator will toggle and the output of the one-shot will go high. However, the filter will only count one clock cycle before the output of the one-shot resets, so the digital output will remain low. The filter works as long as the period of the common-mode signal is greater than the one-shot period.

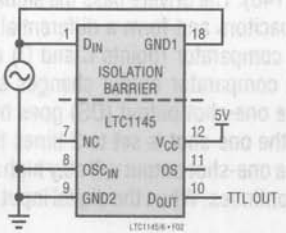


Figure 2. Common-Mode Rejection Test Circuit

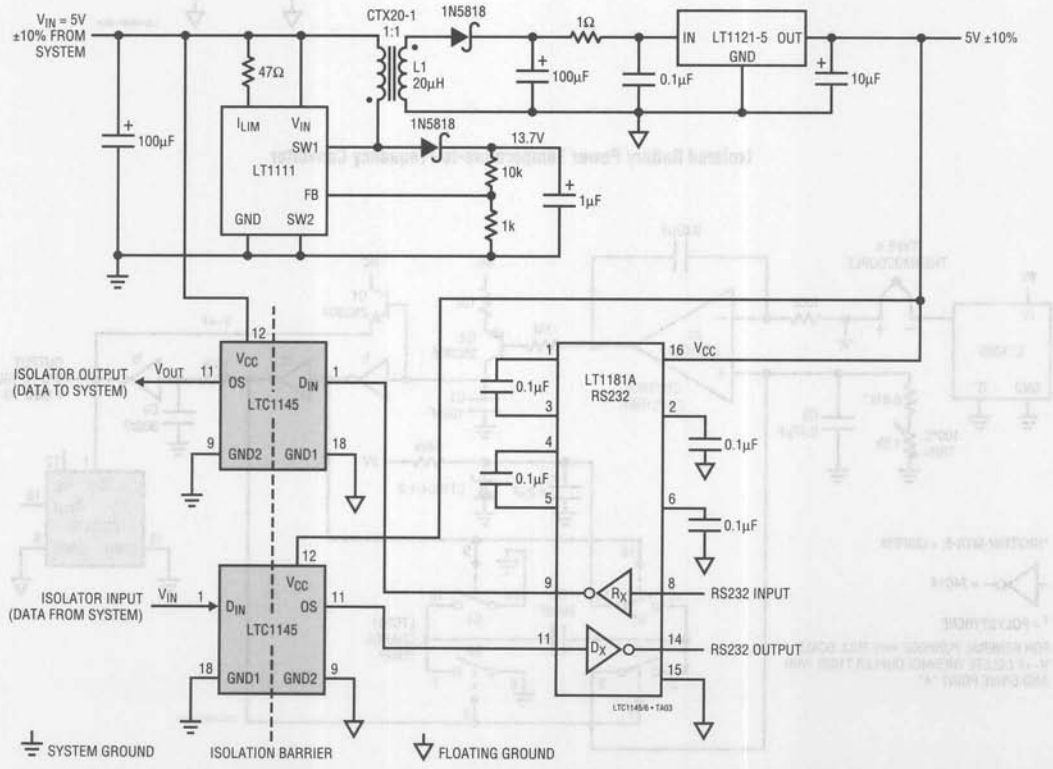
OPERATION

Internal Capacitors

A special lead frame has been designed for the LTC1145/LTC1146 which includes two die paddles and the isolation capacitors. Each capacitor is formed by three parallel metal fingers spaced about 20 mils apart. The capacitors' metal fingers and bonding posts replace the 5 center pins on each side of the 18-pin package. The dielectric for the capacitors is the plastic package moulding compound. The material has a high dielectric constant and a high breakdown voltage. Typically the capacitance between the input and output is in the order of 1pF. This provides sufficient isolation in even the most critical of applications and is suitable for handling high voltage with high $\Delta V/\Delta t$.

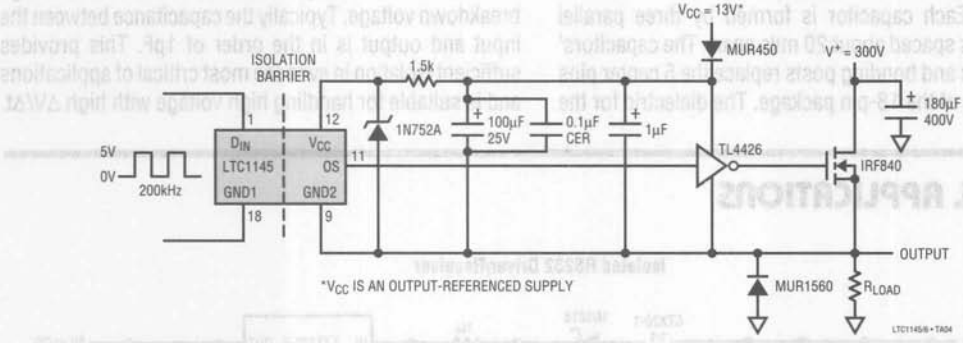
TYPICAL APPLICATIONS

Isolated RS232 Driver/Receiver

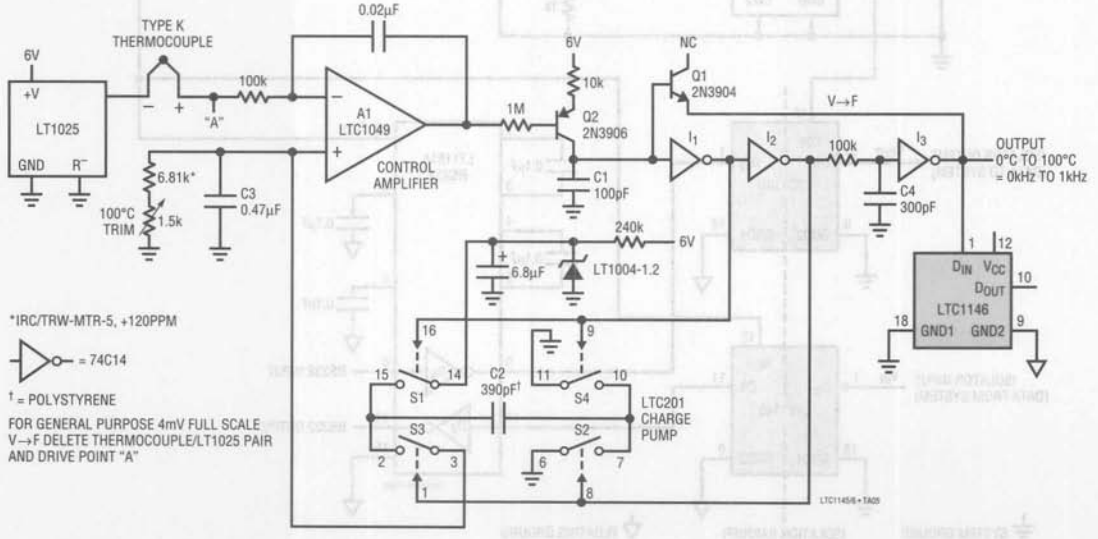


TYPICAL APPLICATIONS

300V Isolated High-Side Driver

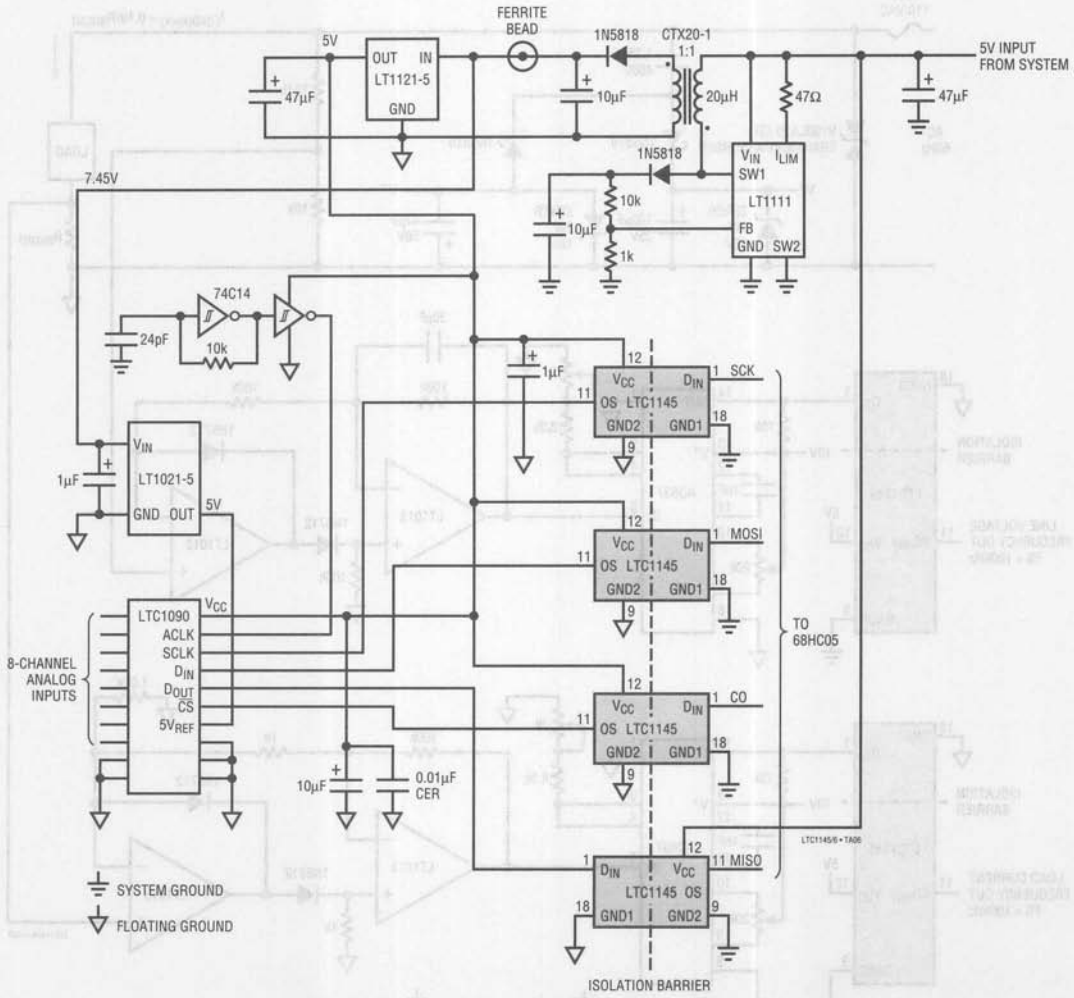


Isolated Battery Power Temperature-to-Frequency Converter



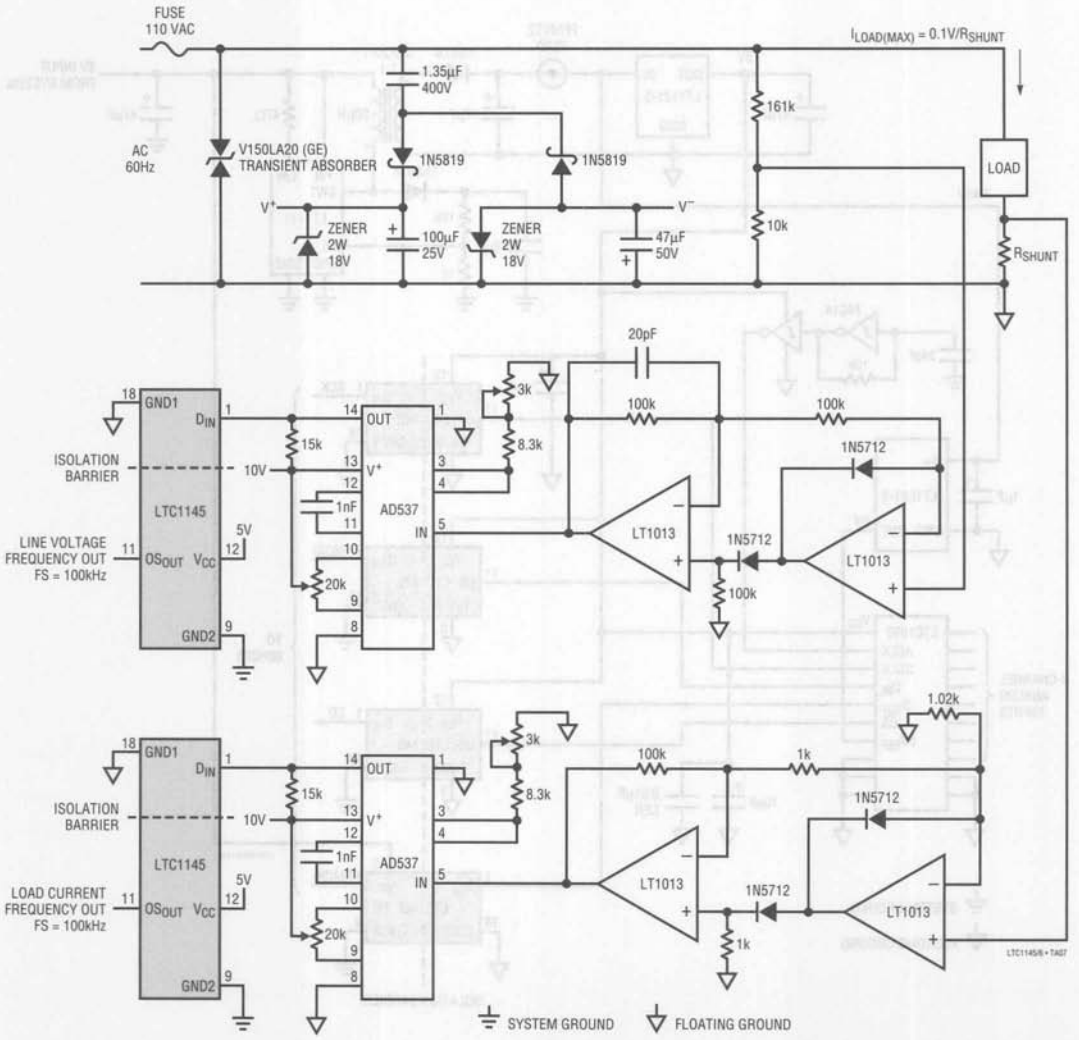
TYPICAL APPLICATIONS

Isolated 10-Bit Data Acquisition Systems



TYPICAL APPLICATIONS

AC Line Monitor



SECTION 5—INTERFACE

MIXED PROTOCOL

LTC1321/LTC1322/LTC1335, RS232/EIA562/RS485 Transceivers 5-198

RS232/EIA562/RS485 Transceivers

FEATURES

- **LTC1321: 2-EIA562/RS232 Transceivers/2-RS485 Transceivers**
- **LTC1322: 4-EIA562/RS232 Transceivers/2-RS485 Transceivers**
- **LTC1335: 4-EIA562 Transceivers/2-RS485 Transceivers with $\overline{OE}$**
- LTC1321/LTC1322 Have the Same Pinout as SP301/SP302
- LTC1335 Features Receiver Three-State Outputs
- Low Supply Current: **1mA Typical**
- 15µA Supply Current in Shutdown
- 120kBaud in EIA/TIA-562 or RS232 Mode
- 10MBaud in RS485/RS422 Mode
- Self-Testing Capability in Loopback Mode
- Power-Up/Down Glitch-Free Outputs
- Driver Maintains High Impedance in Three-State, Shutdown or With Power Off
- Thermal Shutdown Protection
- I/O Lines Can Withstand ±25V
- Withstands Repeated 10kV ESD Pulses

APPLICATIONS

- Low Power RS485/RS422/EIA562/RS232 Interface
- Cable Repeater
- Level Translator

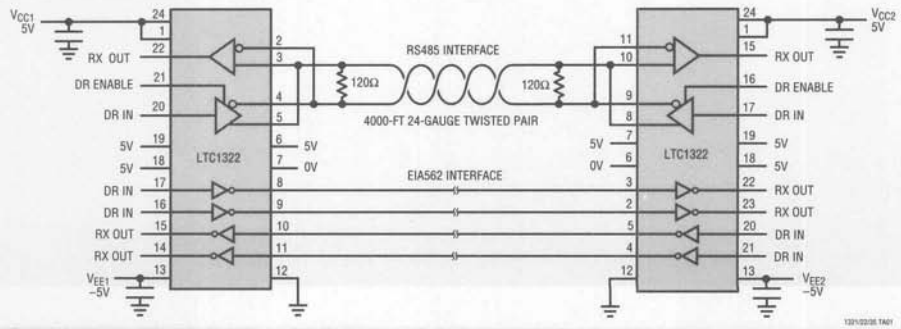
DESCRIPTION

The LTC1321/LTC1322/LTC1335 are low power CMOS bidirectional transceivers, each featuring two reconfigurable interface ports. Each can be configured as two RS485 differential ports, as two single-ended ports, or as one RS485 differential port and one single-ended port. The LTC1321/LTC1322 can provide RS232 or EIA562 compatible single-ended outputs; the LTC1335 provides EIA562 compatible outputs and additionally includes an output enable pin, allowing the receiver logic level outputs to be three-stated.

The RS232/EIA562 transceivers operate to 120kbaud and are in full compliance with EIA/TIA-562 specification. The RS485 transceivers operate to 10Mbaud and are in full compliance with RS485 and RS422 specifications. All interface drivers feature short-circuit and thermal shutdown protection. An enable pin allows RS485 driver outputs to be forced into high impedance which is maintained even when the outputs are forced beyond supply rails or power is off. Both driver outputs and receiver inputs feature **±10kV** ESD protection. A loopback mode connects the driver outputs back to the receiver inputs for diagnostic self-test.

The LTC1321/LTC1322 can support RS232 voltage levels when $6.5V \leq V_{DD} \leq 10V$ and $-6.5V \geq V_{EE} \geq -10V$. The LTC1335 supports receiver output enable but not RS232 levels. A shutdown mode reduces the I_{CC} supply current to 15µA.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{CC} 6.5V
- V_{DD} (LTC1321/LTC1322 Only) 10V
- V_{EE} ..... −10V

Input Voltage
- Drivers ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −25V to 25V
- ON/OFF, $\overline{LB}$, SEL1, SEL2, $\overline{OE}$ ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage
- Drivers ..... −25V to 25V
- Receivers ..... −0.3V to (V_{CC} + 0.3V)

Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range
- LTC1321C/LTC1322C/LTC1335C ..... 0°C to 70°C
- LTC1321I/LTC1322I/LTC1335I ..... −40°C to 85°C

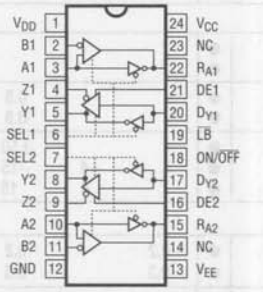
Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

2 RS485 DRIVERS/RECEIVERS
2 EIA/TIA-562 DRIVERS/RECEIVERS

TOP VIEW



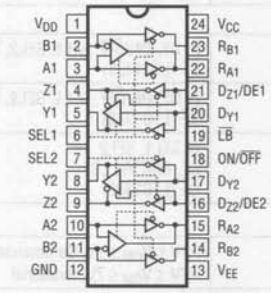
N PACKAGE 24-LEAD PLASTIC DIP
S PACKAGE 24-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1321CN
LTC1321CS
LTC1321IN
LTC1321IS

2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA-562 DRIVERS/RECEIVERS

TOP VIEW



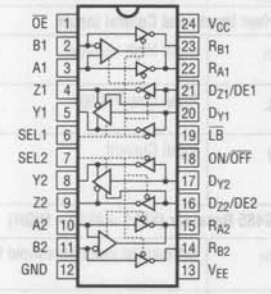
N PACKAGE 24-LEAD PLASTIC DIP
S PACKAGE 24-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1322CN
LTC1322CS
LTC1322IN
LTC1322IS

2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA-562 DRIVERS/RECEIVERS

TOP VIEW



N PACKAGE 24-LEAD PLASTIC DIP
S PACKAGE 24-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1335CN
LTC1335CS
LTC1335IN
LTC1335IS

Consult factory for Military grade parts.

5

DC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{DD} (LTC1321/LTC1322) = 5V ±5%, V_{EE} = −5V ±5% (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS485 Driver (SEL1 = SEL2 = HIGH)							
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0	●			5	V
V_{OD2}	Differential Driver Output Voltage (With Load)	Figure 1, R = 50Ω (RS422) Figure 1, R = 27Ω (RS485)	● ●	2.0 1.5		5 5	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	Figure 1, R = 27Ω or R = 50Ω	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	Figure 1, R = 27Ω or R = 50Ω	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	Figure 1, R = 27Ω or R = 50Ω	●			0.2	V
I_{OSD}	Driver Short-Circuit Current	−7V ≤ V_O ≤ 12V, V_O = HIGH −7V ≤ V_O ≤ 12V, V_O = LOW (Note 4)	● ●	35 10		250 250	mA mA
I_{OZD}	Three-State Output Current (Y, Z)	−7V ≤ V_O ≤ 12V	●		±5	±500	µA
EIA/TIA-562 Driver (SEL1 = SEL2 = LOW)							
V_O	Output Voltage Swing	Figure 4, R_L = 3k, Positve Figure 4, R_L = 3k, Negative	● ●	3.7 −3.7	4.2 −4.3		V V
I_{OSD}	Output Short-Circuit Current	V_O = 0V	●		±11	±60	mA
Driver Inputs and Control Inputs							
V_{IH}	Input High Voltage	D, DE, ON/$\overline{OFF}$, SEL1, SEL2, $\overline{LB}$ $\overline{OE}$ (LTC1335)	● ●	2 2			V V
V_{IL}	Input Low Voltage	D, DE, ON/$\overline{OFF}$, SEL1, SEL2, $\overline{LB}$ $\overline{OE}$ (LTC1335)	● ●			0.8 0.8	V V
I_{IN}	Input Current	D, SEL1, SEL2 DE, ON/$\overline{OFF}$, $\overline{LB}$ $\overline{OE}$ (LTC1335)	● ● ●		 −4 4	±10 −15 15	µA µA µA
RS485 Receiver (SEL1 = SEL2 = HIGH)							
V_{TH}	Differential Input Threshold Voltage	−7V ≤ V_{CM} ≤ 7V, Commercial −7V ≤ V_{CM} ≤ 7V, Industrial	● ●	−0.2 −0.3		0.2 0.3	V V
ΔV_{TH}	Input Hysteresis	V_{CM} = 0V	●		70		mV
I_{IN}	Input Current (A, B)	−7V ≤ V_{IN} ≤ 12V	●			±1	mA
R_{IN}	Input Resistance	−7V ≤ V_{IN} ≤ 12V	●	12	24		kΩ
EIA/TIA-562 Receiver (SEL1 = SEL2 = LOW)							
V_{TH}	Receiver Input Voltage Threshold	Input Low Threshold Input High Threshold	● ●	0.8	1.1 1.7	 2.4	V V
ΔV_{TH}	Receiver Input Hysteresis		●	0.1	0.6	1.0	V
R_{IN}	Receiver Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Receiver Output							
V_{OH}	Receiver Output High Voltage	I_O = −3mA, V_{IN} = 0V, SEL1 = SEL2 = LOW	●	3.5	4.6		V
V_{OL}	Receiver Output Low Voltage	I_O = 3mA, V_{IN} = 3V, SEL1 = SEL2 = LOW	●		0.2	0.4	V
I_{OSR}	Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7		85	mA
I_{OZR}	Three-State Output Current	ON/$\overline{OFF}$ = 0V $\overline{OE}$ = V_{CC} (LTC1335)	● ●			±10 ±10	µA µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{DD} (LTC1321/LTC1322) = 5V ±5%, V_{EE} = −5V ±5% (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Currents							
I_{CC}	V_{CC} Supply Current	No Load (SEL1 = SEL2 = HIGH)	●		1000	2000	µA
		Shutdown, ON/$\overline{OFF}$ = 0V	●		15	50	µA
I_{DD}	V_{DD} Supply Current (LTC1321/LTC1322)	No Load (SEL1 = SEL2 = LOW)	●		300	1000	µA
		Shutdown, ON/$\overline{OFF}$ = 0V	●		0.1	50	µA
I_{EE}	V_{EE} Supply Current	No Load (SEL1 = SEL2 = HIGH)	●		−1000	−2000	µA
		Shutdown, ON/$\overline{OFF}$ = 0V	●		−0.1	−50	µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{DD} (LTC1321/LTC1322) = 5V ±5%, V_{EE} = −5V ±5% (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-562 Mode (SEL1 = SEL2 = LOW)							
SR	Slew Rate	Figure 4, R_L = 3k, C_L = 15pF	●		14	30	V/µs
		Figure 4, R_L = 3k, C_L = 1000pF	●	4	7		V/µs
t_T	Transition Time	Figure 4, R_L = 3k, C_L = 2500pF	●	0.22	1.9	3.1	µs
t_{PLH}	Driver Input to Output	Figures 4,10, R_L = 3k, C_L = 15pF	●		0.6	4	µs
t_{PHL}	Driver Input to Output	Figures 4,10, R_L = 3k, C_L = 15pF	●		0.6	4	µs
t_{PLH}	Receiver Input to Output	Figures 5,11	●		0.3	6	µs
t_{PHL}	Receiver Input to Output	Figures 5,11	●		0.4	6	µs
RS485 Mode (SEL1 = SEL2 = HIGH)							
t_{PLH}	Driver Input to Output	Figures 2,7, R_L = 54Ω, C_L = 100pF	●	20	40	70	ns
t_{PHL}	Driver Input to Output	Figures 2,7, R_L = 54Ω, C_L = 100pF	●	20	40	70	ns
t_{SKEW}	Driver Output to Output	Figures 2,7, R_L = 54Ω, C_L = 100pF	●		5	15	ns
t_r, t_f	Driver Rise or Fall Time	Figures 2,7, R_L = 54Ω, C_L = 100pF	●	3	15	40	ns
t_{ZL}	Driver Enable to Output Low	Figures 3,8, C_L = 100pF, S1 Closed	●		50	90	ns
t_{ZH}	Driver Enable to Output High	Figures 3,8, C_L = 100pF, S2 Closed	●		50	90	ns
t_{LZ}	Driver Disable from Low	Figures 3,8, C_L = 15pF, S1 Closed	●		50	90	ns
t_{HZ}	Driver Disable from High	Figures 3,8, C_L = 15pF, S2 Closed	●		60	90	ns
t_{PLH}	Receiver Input to Output	Figures 2,9, R_L = 54Ω, C_L = 100pF	●	20	60	140	ns
t_{PHL}	Receiver Input to Output	Figures 2,9, R_L = 54Ω, C_L = 100pF	●	20	70	140	ns
t_{SKEW}	Differential Receiver Skew, $\lvert t_{PLH}-t_{PHL} \rvert$	Figures 2,9, R_L = 54Ω, C_L = 100pF	●		10		ns
Receiver Output Enable/Disable (LTC1335)							
t_{ZL}	Receiver Enable to Output Low	Figures 6,12, C_L = 15pF, S1 Closed	●		40	90	ns
t_{ZH}	Receiver Enable to Output High	Figures 6,12, C_L = 15pF, S2 Closed	●		40	90	ns
t_{LZ}	Receiver Disable from Low	Figures 6,12, C_L = 15pF, S1 Closed	●		40	90	ns
t_{HZ}	Receiver Disable from High	Figures 6,12, C_L = 15pF, S2 Closed	●		50	90	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

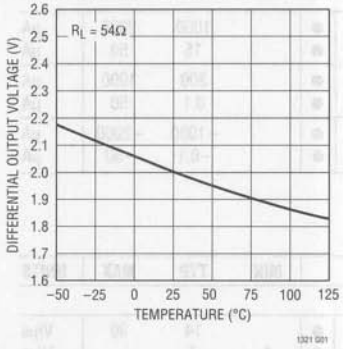
Note 3: All typicals are given at V_{CC} = V_{DD} (LTC1321/LTC1322) = 5V, V_{EE} = −5V, and T_A = 25°C.

Note 4: Short-circuit current for RS485 driver output low state folds back above V_{CC}. Peak current occurs around V_O = 3V.

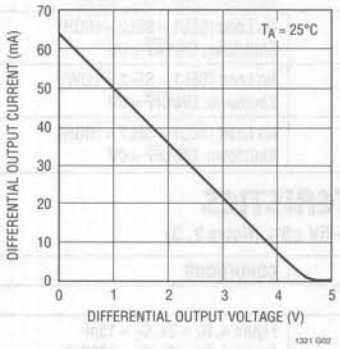
5

TYPICAL PERFORMANCE CHARACTERISTICS

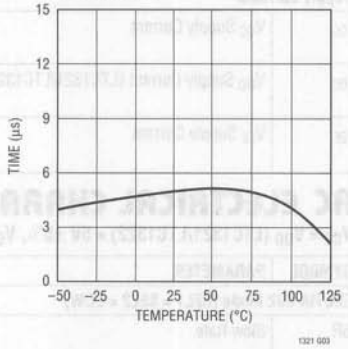
RS485 Driver Differential Output Voltage vs Temperature



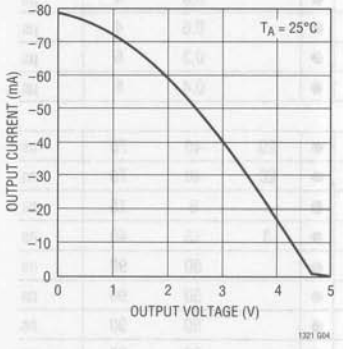
RS485 Driver Differential Output Current vs Output Voltage



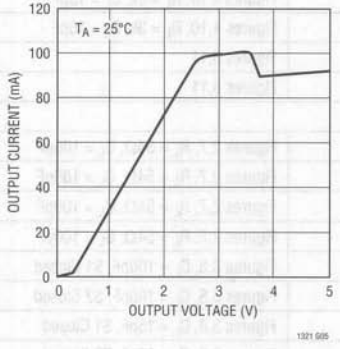
RS485 Driver Skew vs Temperature



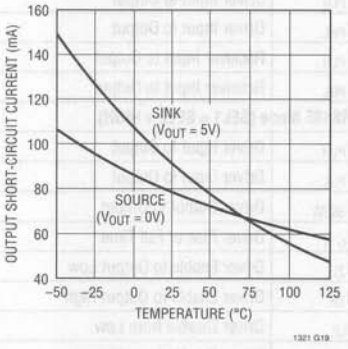
RS485 Driver Output High Voltage vs Output Current



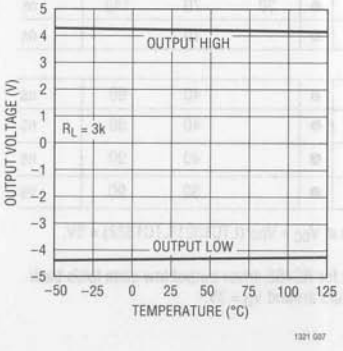
RS485 Driver Output Low Voltage vs Output Current



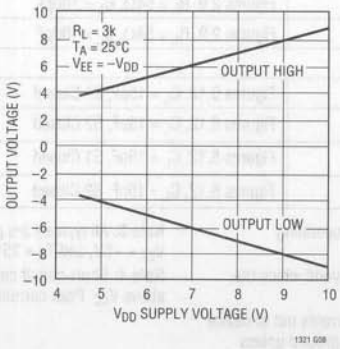
RS485 Driver Output Short-Circuit Current vs Temperature



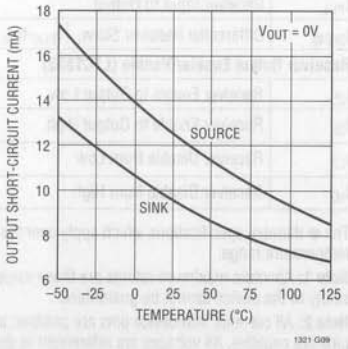
EIA562 Driver Output Voltage vs Temperature



EIA562 Driver Output Voltage vs Supply Voltage

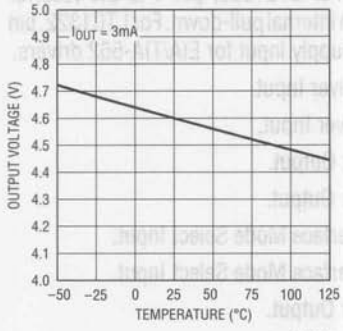


EIA562 Driver Output Short-Circuit Current vs Temperature

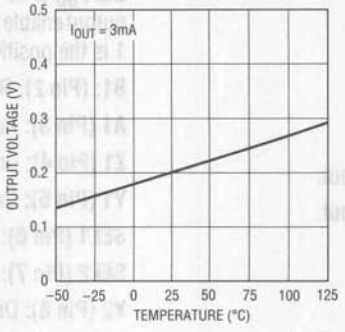


TYPICAL PERFORMANCE CHARACTERISTICS

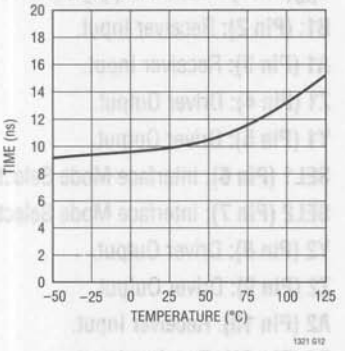
Receiver Output High Voltage vs Temperature



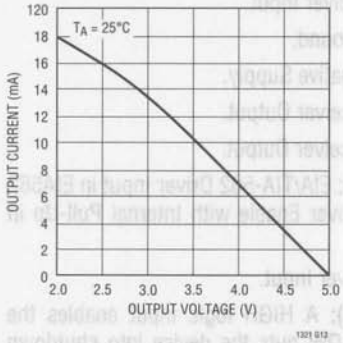
Receiver Output Low Voltage vs Temperature



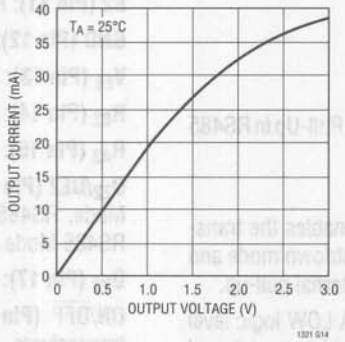
RS485 Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



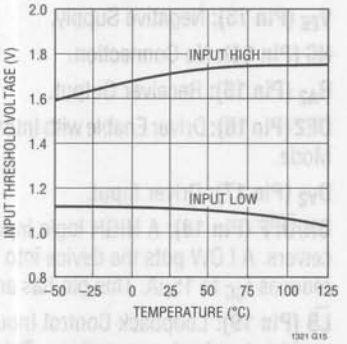
Receiver Output Current vs Output High Voltage



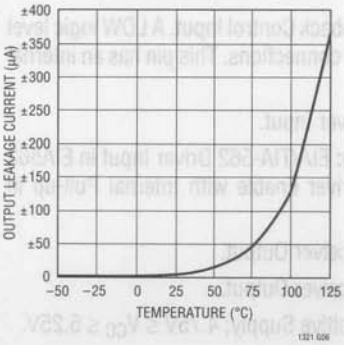
Receiver Output Current vs Output Low Voltage



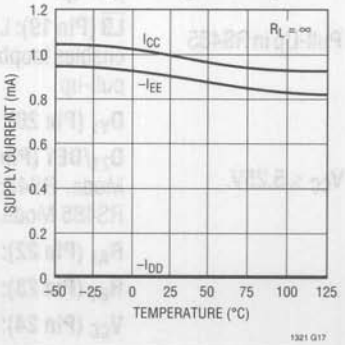
EIA562 Receiver Input Threshold Voltage vs Temperature



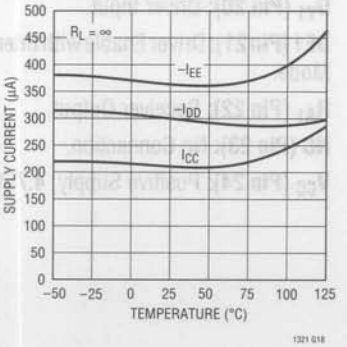
Driver Output Leakage Current (Disable/Shutdown) vs Temperature



Supply Current in RS485 Mode vs Temperature (Both Ports)



Supply Current in EIA562 Mode vs Temperature (Both Ports)



5

PIN FUNCTIONS

LTC1321

V_{DD} (Pin 1): Positive Supply Input for EIA/TIA-562 Drivers.

B1: (Pin 2): Receiver Input.

A1 (Pin 3): Receiver Input.

Z1 (Pin 4): Driver Output.

Y1 (Pin 5): Driver Output.

SEL1 (Pin 6): Interface Mode Select Input.

SEL2 (Pin 7): Interface Mode Select Input.

Y2 (Pin 8): Driver Output.

Z2 (Pin 9): Driver Output.

A2 (Pin 10): Receiver Input.

B2 (Pin 11): Receiver Input.

GND (Pin 12): Ground.

V_{EE} (Pin 13): Negative Supply.

NC (Pin 14): No Connection.

R_{A2} (Pin 15): Receiver Output.

DE2 (Pin 16): Driver Enable with Internal Pull-Up in RS485 Mode.

D_{Y2} (Pin 17): Driver Input.

ON/$\overline{OFF}$ (Pin 18): A HIGH logic input enables the transceivers. A LOW puts the device into shutdown mode and reduces I_{CC} to 15µA. This pin has an internal pull-up.

$\overline{LB}$ (Pin 19): Loopback Control Input. A LOW logic level enables loopback connections. This pin has an internal pull-up.

D_{Y1} (Pin 20): Driver Input.

DE1 (Pin 21): Driver Enable with Internal Pull-Up in RS485 Mode.

R_{A1} (Pin 22): Receiver Output.

NC (Pin 23): No Connection.

V_{CC} (Pin 24): Positive Supply; $4.75V \leq V_{CC} \leq 5.25V$.

LTC1322/LTC1335

$\overline{OE}/V_{DD}$ (Pin 1): For LTC1335, pin 1 is the receiver output enable with internal pull-down. For LTC1322, pin 1 is the positive supply input for EIA/TIA-562 drivers.

B1: (Pin 2): Receiver Input.

A1 (Pin 3): Receiver Input.

Z1 (Pin 4): Driver Output.

Y1 (Pin 5): Driver Output.

SEL1 (Pin 6): Interface Mode Select Input.

SEL2 (Pin 7): Interface Mode Select Input.

Y2 (Pin 8): Driver Output.

Z2 (Pin 9): Driver Output.

A2 (Pin 10): Receiver Input.

B2 (Pin 11): Receiver Input.

GND (Pin 12): Ground.

V_{EE} (Pin 13): Negative Supply.

R_{B2} (Pin 14): Receiver Output.

R_{A2} (Pin 15): Receiver Output.

D_{Z2}/DE2 (Pin 16): EIA/TIA-562 Driver Input in EIA562 Mode. RS485 Driver Enable with Internal Pull-Up in RS485 Mode.

D_{Y2} (Pin 17): Driver Input.

ON/$\overline{OFF}$ (Pin 18): A HIGH logic input enables the transceivers. A LOW puts the device into shutdown mode and reduces I_{CC} to 15µA. This pin has an internal pull-up.

$\overline{LB}$ (Pin 19): Loopback Control Input. A LOW logic level enables loopback connections. This pin has an internal pull-up.

D_{Y1} (Pin 20): Driver Input.

D_{Z1}/DE1 (Pin 21): EIA/TIA-562 Driver Input in EIA562 Mode. RS485 Driver Enable with Internal Pull-up in RS485 Mode.

R_{A1} (Pin 22): Receiver Output.

R_{B1} (Pin 23): Receiver Output.

V_{CC} (Pin 24): Positive Supply; $4.75V \leq V_{CC} \leq 5.25V$.

FUNCTION TABLES

LTC1321

RS485 Driver Mode

INPUTS				LINE	OUTPUTS	
ON/$\overline{OFF}$	SEL	DE	D	CONDITION	Y	Z
1	1	1	0	No Fault	0	1
1	1	1	1	No Fault	1	0
1	1	1	X	Fault	Z	Z
1	1	0	X	X	Z	Z
0	1	X	X	X	Z	Z

RS485 Receiver Mode

INPUTS			OUTPUT
ON/$\overline{OFF}$	SEL	A – B	R
1	1	< –0.2V	0
1	1	> 0.2V	1
1	1	Inputs Open	1
0	1	X	Z

RS232/EIA562 Driver Mode

INPUTS			LINE	OUTPUT
ON/$\overline{OFF}$	SEL	D	CONDITION	Y
1	0	0	No Fault	1
1	0	1	No Fault	0
1	0	X	Fault	Z
0	0	X	X	Z

RS232/EIA562 Receiver Mode

INPUTS			OUTPUT
ON/$\overline{OFF}$	SEL	A	R
1	0	0	1
1	0	1	0
1	0	Inputs Open	1
0	0	X	Z

LTC1322

RS485 Driver Mode

INPUTS				LINE	OUTPUTS	
ON/$\overline{OFF}$	SEL	DE	D	CONDITION	Y	Z
1	1	1	0	No Fault	0	1
1	1	1	1	No Fault	1	0
1	1	1	X	Fault	Z	Z
1	1	0	X	X	Z	Z
0	1	X	X	X	Z	Z

RS485 Receiver Mode

INPUTS			OUTPUT
ON/$\overline{OFF}$	SEL	A – B	R
1	1	< –0.2V	0
1	1	> 0.2V	1
1	1	Inputs Open	1
0	1	X	Z

RS232/EIA562 Driver Mode

INPUTS			LINE	OUTPUT
ON/$\overline{OFF}$	SEL	D	CONDITION	Y, Z
1	0	0	No Fault	1
1	0	1	No Fault	0
1	0	X	Fault	Z
0	0	X	X	Z

RS232/EIA562 Receiver Mode

INPUTS			OUTPUT
ON/$\overline{OFF}$	SEL	A OR B	R
1	0	0	1
1	0	1	0
1	0	Input Open	1
0	0	X	Z

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FUNCTION TABLES

LTC1335

RS485 Driver Mode

INPUTS				LINE	OUTPUTS	
ON/$\overline{OFF}$	SEL	DE	D	CONDITION	Y	Z
1	1	1	0	No Fault	0	1
1	1	1	1	No Fault	1	0
1	1	1	X	Fault	Z	Z
1	1	0	X	X	Z	Z
0	1	X	X	X	Z	Z

EIA562 Driver Mode

INPUTS			LINE	OUTPUT
ON/$\overline{OFF}$	SEL	D	CONDITION	Y, Z
1	0	0	No Fault	1
1	0	1	No Fault	0
1	0	X	Fault	Z
0	0	X	X	Z

RS485 Receiver Mode

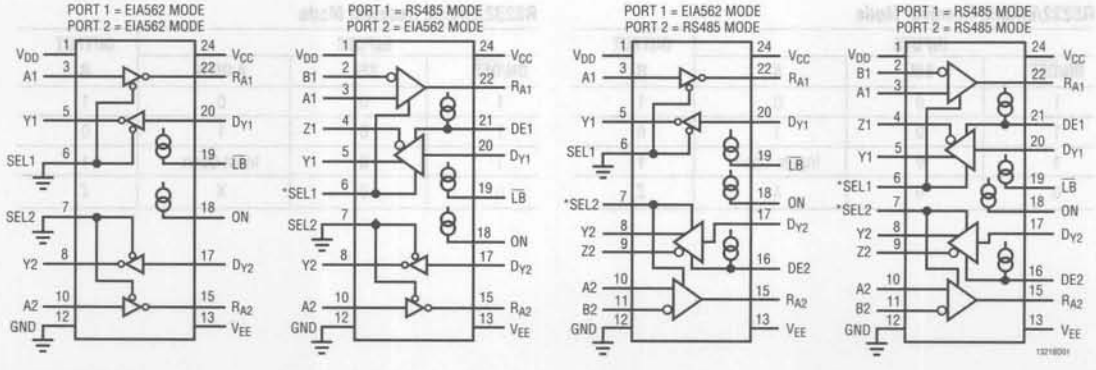
INPUTS				OUTPUT
ON/$\overline{OFF}$	SEL	$\overline{OE}$	A – B	R
1	1	0	< –0.2V	0
1	1	0	> 0.2V	1
1	1	0	Inputs Open	1
1	1	1	X	Z
0	1	X	X	Z

EIA562 Receiver Mode

INPUTS				OUTPUT
ON/$\overline{OFF}$	SEL	$\overline{OE}$	A OR B	R
1	0	0	0	1
1	0	0	1	0
1	0	0	Input Open	1
1	0	1	X	Z
0	0	X	X	Z

BLOCK DIAGRAMS

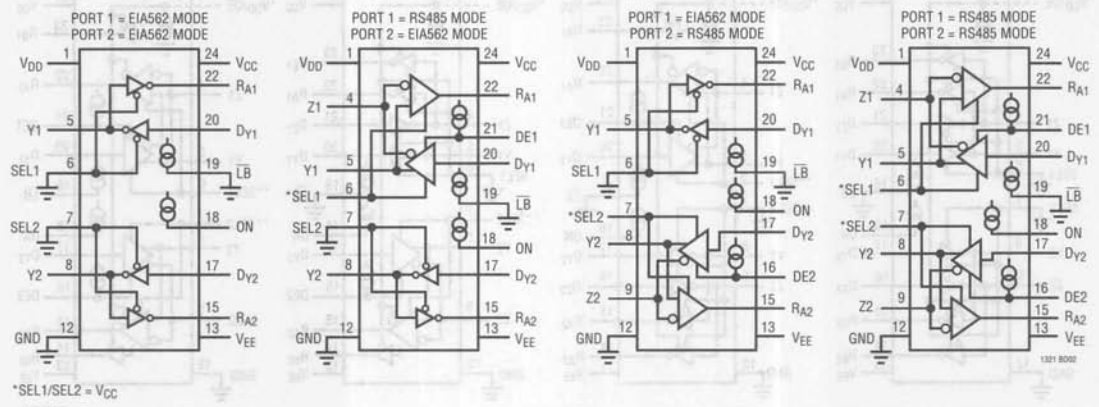
LTC1321 Interface Configuration Without Loopback



* SEL1/SEL2 = V_{CC}

BLOCK DIAGRAMS

LTC1321 Interface Configuration With Loopback



*SEL1/SEL2 = V_{CC}

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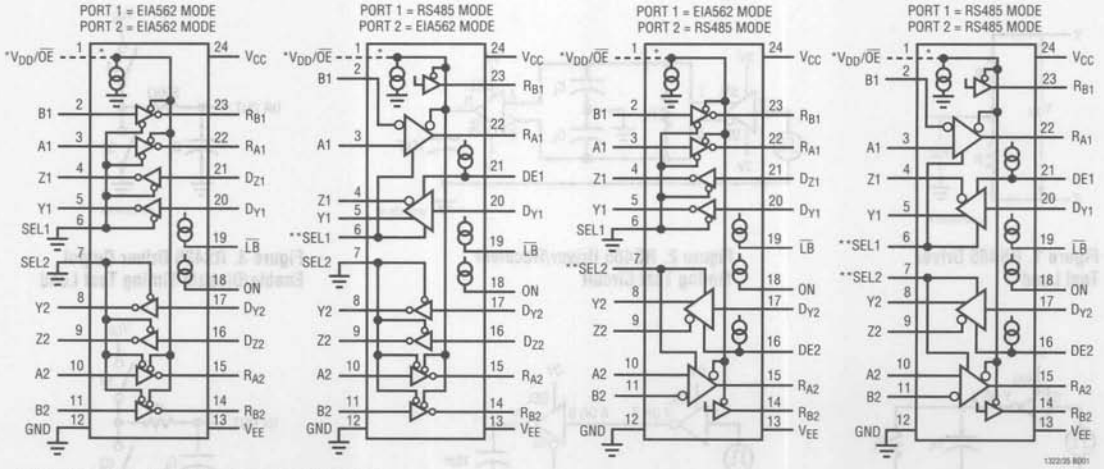
LTC1322/LTC1335 Interface Configuration Without Loopback

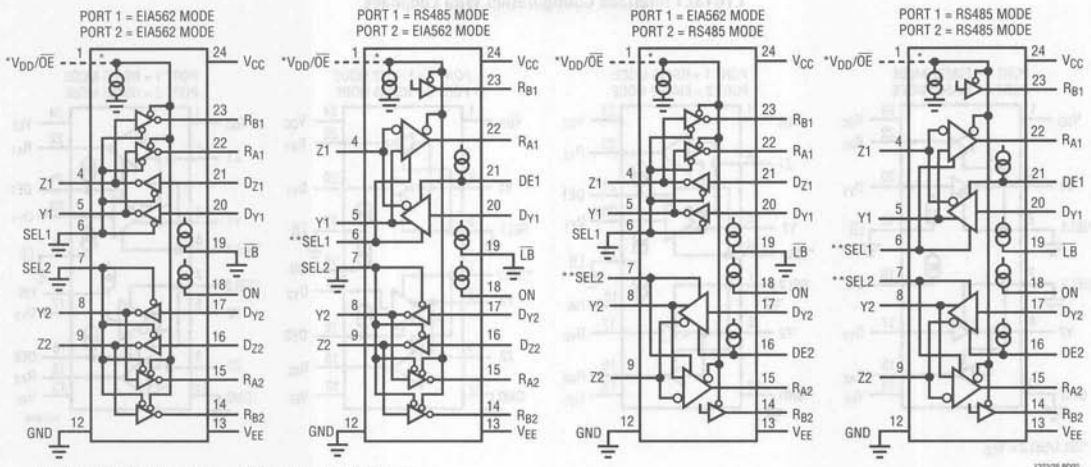


*FOR LTC1322 ONLY, PIN 1 IS V_{DD}, AND $\overline{OE}$ IS ALWAYS ENABLED.
FOR LTC1335, PIN 1 IS $\overline{OE}$, AND V_{DD} IS CONNECTED TO V_{CC}.

**SEL1/SEL2 = V_{CC}.

BLOCK DIAGRAMS

LTC1322/LTC1335 Interface Configuration With Loopback



*FOR LTC1322 ONLY, PIN 1 IS V_{DD}, AND $\overline{OE}$ IS ALWAYS ENABLED.
FOR LTC1335, PIN 1 IS $\overline{OE}$, AND V_{DD} IS CONNECTED TO V_{CC}.

**SEL1/SEL2 = V_{CC}.

TEST CIRCUITS

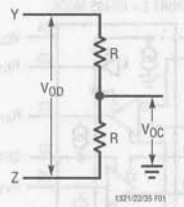


Figure 1. RS485 Driver Test Load

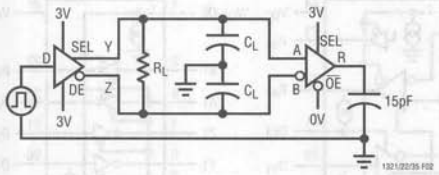


Figure 2. RS485 Driver/Receiver Timing Test Circuit

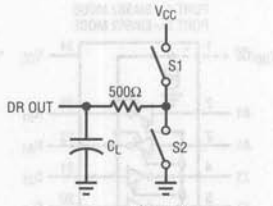


Figure 3. RS485 Driver Output Enable/Disable Timing Test Load

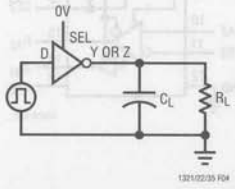


Figure 4. EIA/TIA-562 Driver Timing Test Circuit

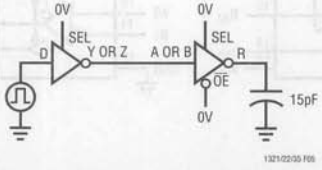


Figure 5. EIA/TIA-562 Receiver Timing Test Circuit

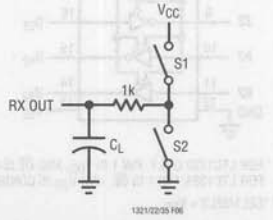


Figure 6. Receiver Output Enable/Disable Timing Test Load

SWITCHING WAVEFORMS

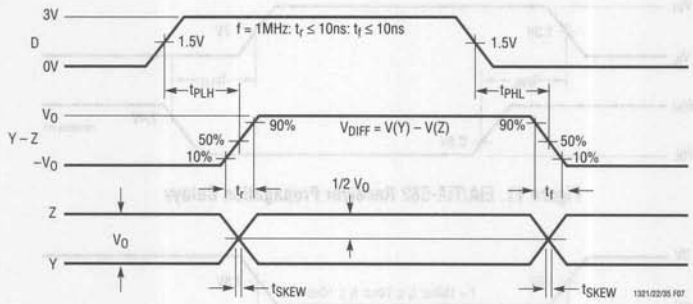


Figure 7. RS485 Driver Propagation Delays

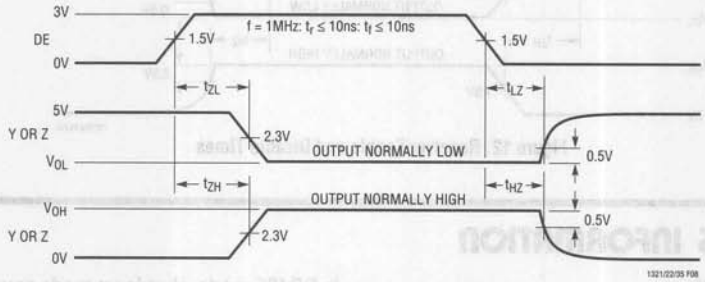


Figure 8. RS485 Driver Enable and Disable Times

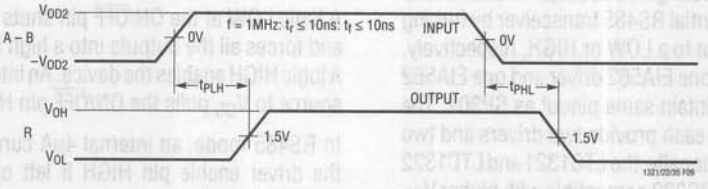


Figure 9. RS485 Receiver Propagation Delays

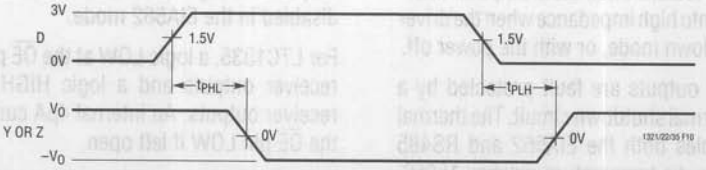


Figure 10. EIA/TIA-562 Driver Propagation Delays

SWITCHING WAVEFORMS

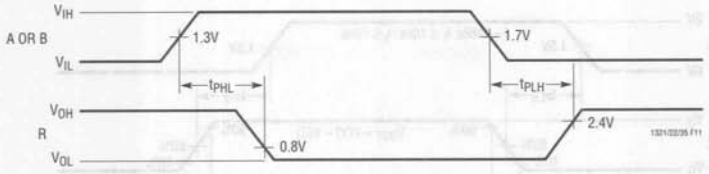


Figure 11. EIA/TIA-562 Receiver Propagation Delays

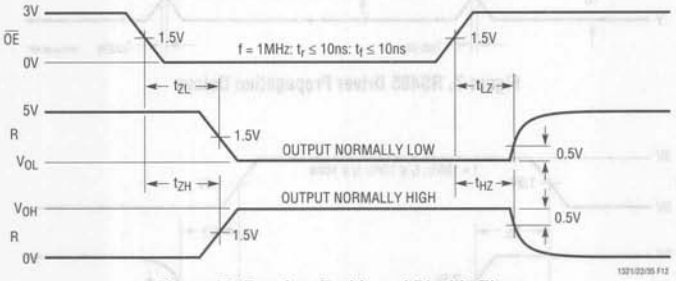


Figure 12. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Basic Theory of Operation

The LTC1321/LTC1322/LTC1335 each have two interface ports. Each port may be configured as single-ended EIA562 transceiver(s) or differential RS485 transceiver by forcing the port's selection input to a LOW or HIGH, respectively. The LTC1321 provides one EIA562 driver and one EIA562 receiver per port to maintain same pinout as SP301. The LTC1322 and LTC1335 each provide two drivers and two receivers per port. Additionally, the LTC1321 and LTC1322 single-ended ports are RS232 compatible with higher V_{DD} and V_{EE} supply levels.

All the interface drivers feature three-state outputs. Interface outputs are forced into high impedance when the driver is disabled, in the shutdown mode, or with the power off.

All the interface driver outputs are fault protected by a current limiting and thermal shutdown circuit. The thermal shutdown circuit disables both the EIA562 and RS485 driver outputs when the die temperature reaches 150°C. The thermal shutdown circuit enables the drivers when the die temperature cools to 135°C.

In RS485 mode, shutdown mode or with the power off, the input resistance of the receiver is 24k. The input resistance drops to 6.3k in EIA562 mode.

A logic LOW at the ON/$\overline{OFF}$ pin shuts down the device and forces all the outputs into a high impedance state. A logic HIGH enables the device. An internal 4µA current source to V_{CC} pulls the ON/$\overline{OFF}$ pin HIGH if left open.

In RS485 mode, an internal 4µA current source pulls the driver enable pin HIGH if left open. The RS485 receiver has a 4µA current source at the noninverting input. If both the RS485 receiver inputs are open, the output is a high state. Both the current sources are disabled in the EIA562 mode.

For LTC1335, a logic LOW at the $\overline{OE}$ pin enables all the receiver outputs and a logic HIGH disables all the receiver outputs. An internal 4µA current source pulls the $\overline{OE}$ pin LOW if left open.

A loopback mode enables internal connections from driver outputs to receiver inputs for self-test when the

APPLICATIONS INFORMATION

$\overline{LB}$ pin has a LOW logic state. The driver outputs are not isolated from the external loads. This allows transmitter verification under the loaded condition. An internal 4μA current source pulls the $\overline{LB}$ pin HIGH if left open and disables the loopback configuration.

EIA562/RS485 Applications

EIA562 and RS485 output levels are supported when LTC1321/LTC1322/LTC1335 are powered from ±5V supplies. The LTC1321/LTC1322 require the V_{DD} and V_{CC} pins to be tied together and connected to 5V supply (Figure 13). The V_{DD} and V_{CC} are connected internally and brought out at V_{CC} pin in the LTC1335. The unloaded outputs will swing from –5V to 5V in EIA562 mode, and from 0V to 5V in RS485 mode.

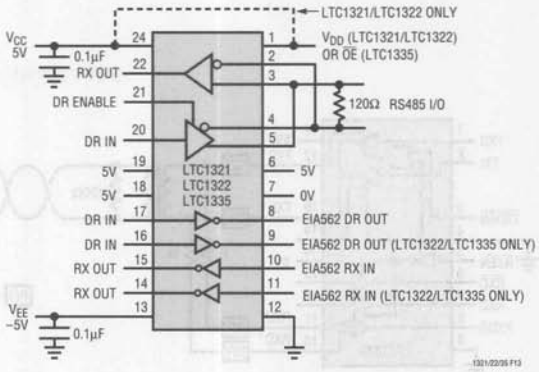


Figure 13. EIA562/RS485 Interfaces with ±5V Supplies

RS232/RS485 Applications

If true RS232-compatible outputs are required, the LTC1321/LTC1322 may be used with the V_{DD} and V_{EE} supply voltages increased to provide the additional signal swing. To meet RS232, V_{DD} must be between 6.5V and 10V, and V_{EE} must be between –6.5V and –10V. V_{CC} remains connected to 5V. If only ±12V supplies are available, inexpensive Zener diodes (Z1 and Z2) may be connected in series with V_{DD} and V_{EE} supply pins as shown in Figure 14. An optional 16V Zener diode between V_{CC} and V_{EE} is recommended to keep the maximum voltage between V_{CC} and V_{EE} within safe limits.

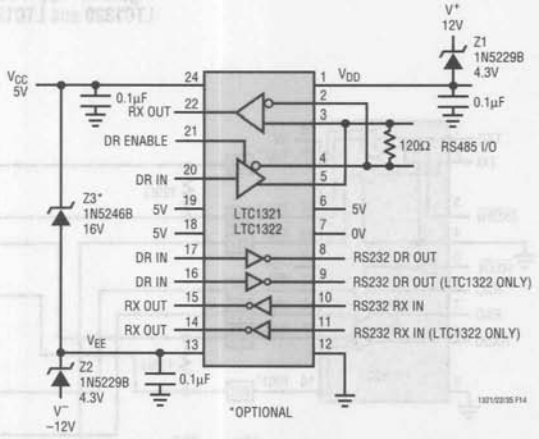


Figure 14. RS232/RS485 Interfaces with 5V, ±12V Supplies

LocalTalk®/AppleTalk® Applications

The LTC1321/LTC1322/LTC1335 can be used to provide AppleTalk/LocalTalk-compatible signals in RS485 mode. Figure 15 shows one half of an LTC1335 connected to an LTC1320 AppleTalk transceiver in a typical LocalTalk configuration. Figure 16 shows a typical direct-wire connection with the LTC1335 as the DCE transceiver and the LTC1320 as the DTE transceiver. The LTC1321/LTC1322/LTC1335 RS485 mode is capable of meeting all AppleTalk protocol specifications.

LocalTalk and AppleTalk are registered trademarks of Apple Computer, Inc.

APPLICATIONS INFORMATION

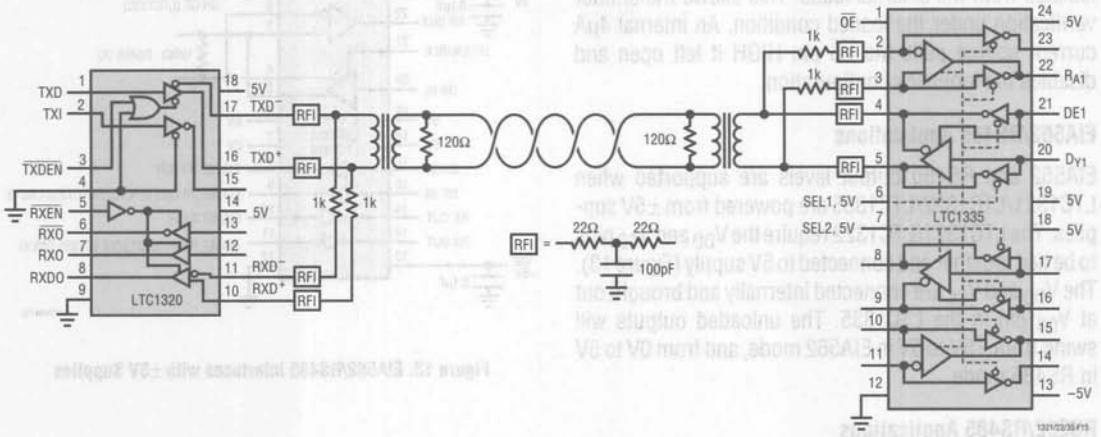


Figure 15. Apple LocalTalk Implemented Using LTC1320 and LTC1335 Transceivers

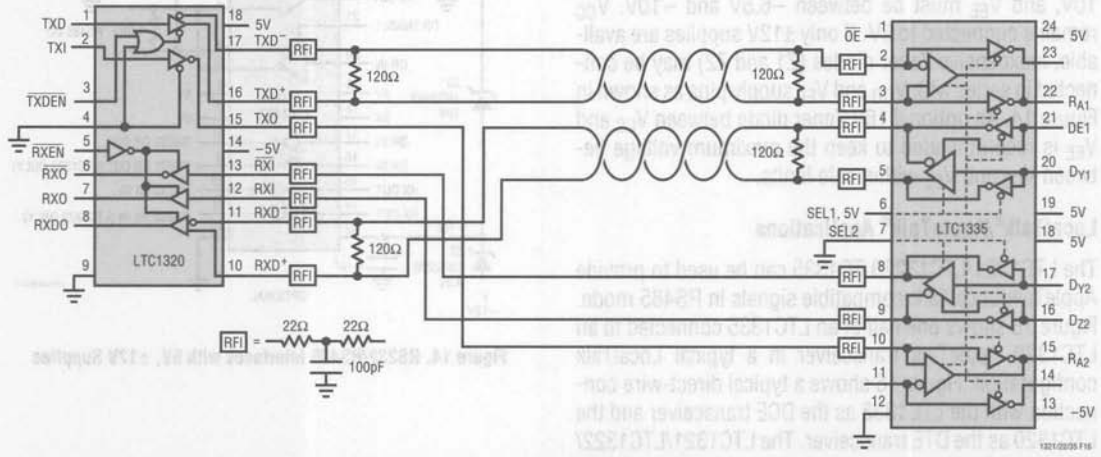


Figure 16. AppleTalk Direct Connect Using LTC1320 for DTE and LTC1335 for DCE Transceivers

TYPICAL APPLICATIONS

A typical EIA562/RS232 interface application is shown in Figure 17 with LTC1322. A typical EIA562 interface application with LTC1335 is shown in Figure 18.

A typical connection for RS485 transceiver is shown in Figure 19. A twisted pair of wires connects up to 32 drivers and receivers for half duplex multi-point data transmission. The wires must be terminated at both ends with resistors equal to the wire's characteristic impedance, generally 120Ω. An optional shield around the twisted pair helps to reduce unwanted noise and should be connected to ground at one end.

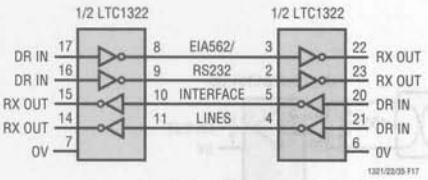


Figure 17. Typical Connection for EIA562/RS232 Interface

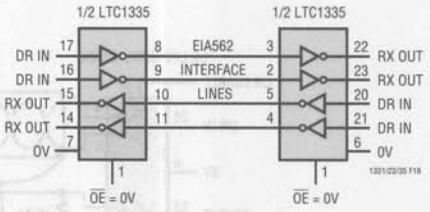


Figure 18. Typical Connection for EIA562 Interface

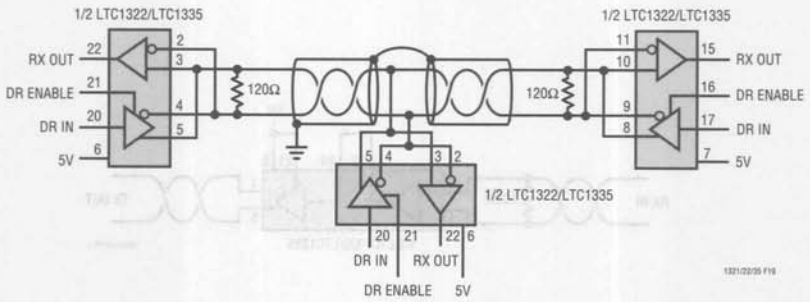


Figure 19. Typical Connection for RS485 Interface

TYPICAL APPLICATIONS

A typical RS422 connection shown in Figure 20 allows one driver and ten receivers on a twisted pair of wires terminated with a 100Ω resistor at one end. The ground shield is optional.

A typical twisted pair line repeater is shown in Figure 21. As data transmission rate drops with increased cable length, repeater can be inserted to improve transmission rate or to transmit beyond 4000 feet limit.

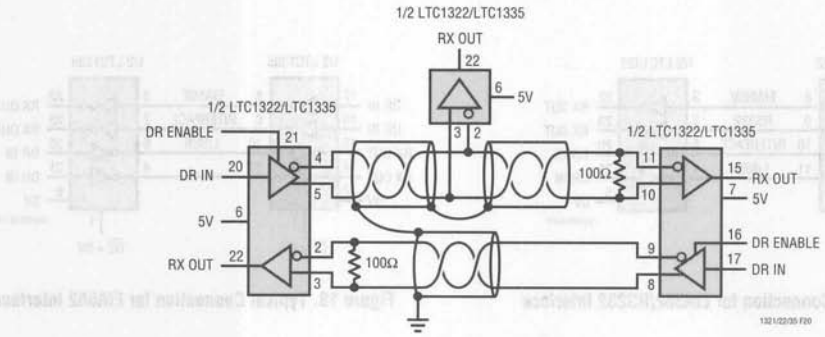


Figure 20. Typical Connection for RS422 Interface

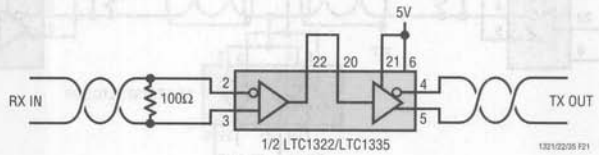


Figure 21. Typical Cable Repeater for RS422 Interface

TYPICAL APPLICATIONS

The LTC1322/LTC1335 can be used to translate EIA562 to RS422 interface level or vice versa as shown in Figure 22. One port is configured as EIA562 transceiver and the other as RS485 transceiver. The LTC1322 can also support RS232 to RS422 level translation if V_{DD} is between 6.5V and 10V, and V_{EE} is between –6.5V and –10V.

Using two LTC1321/LTC1335 as level translators, the EIA562/RS232 interface distance can be extended to 4000 feet with twisted wires (Figure 23).

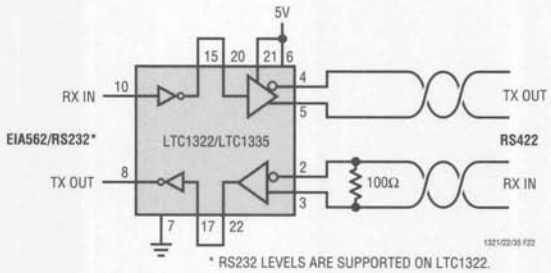


Figure 22. Typical EIA562/RS232 to RS422 Level Translator

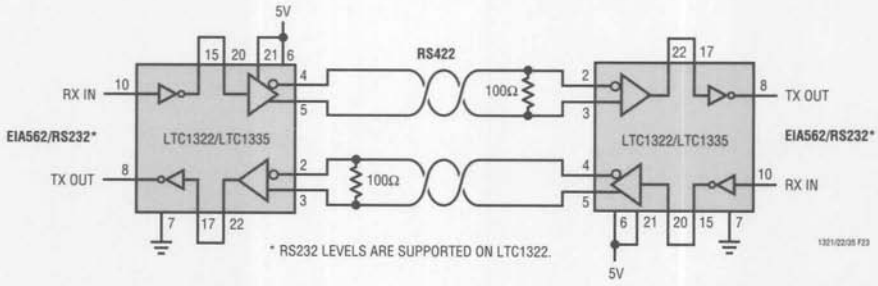


Figure 23. Typical Cable Extension for EIA562/RS232 Interface

SECTION 6—DATA CONVERSION

SECTION 6—DATA CONVERSION

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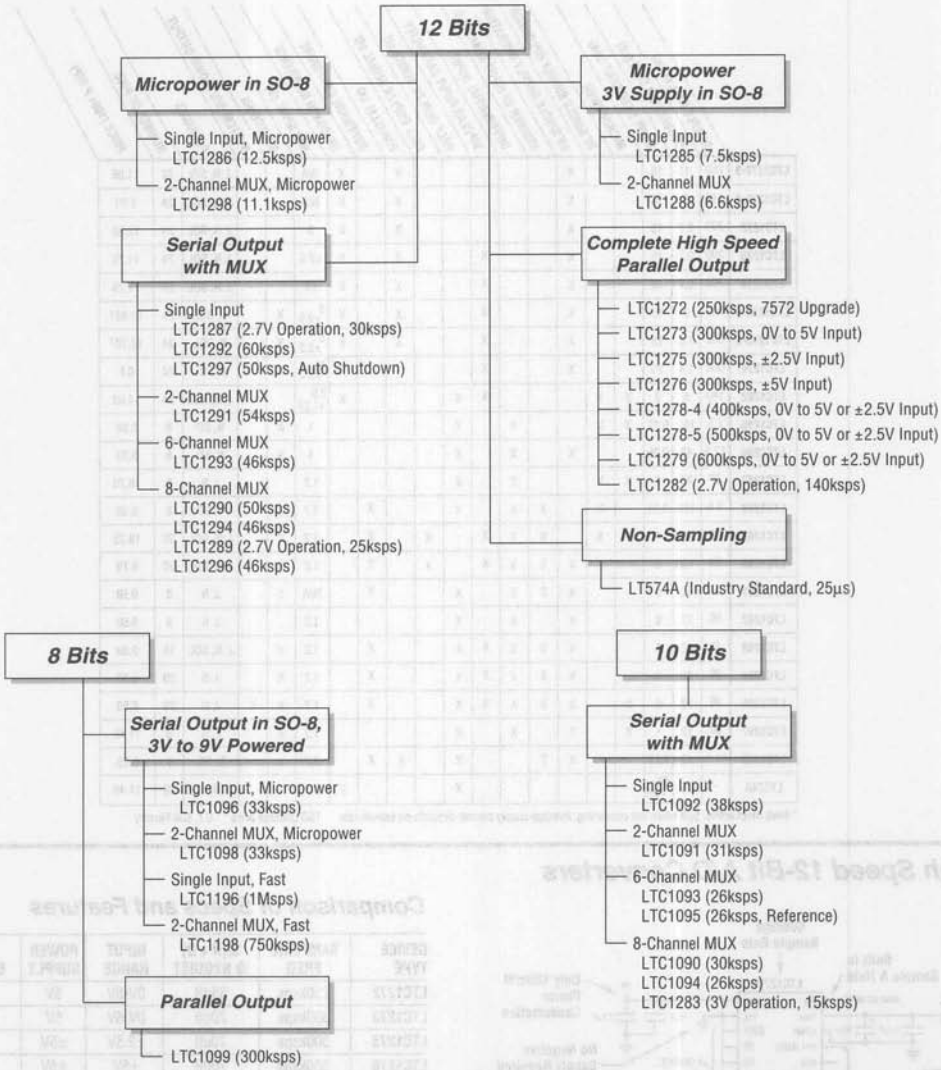
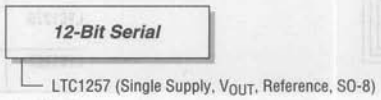
Analog-to-Digital Converters



Digital-to-Analog Converters

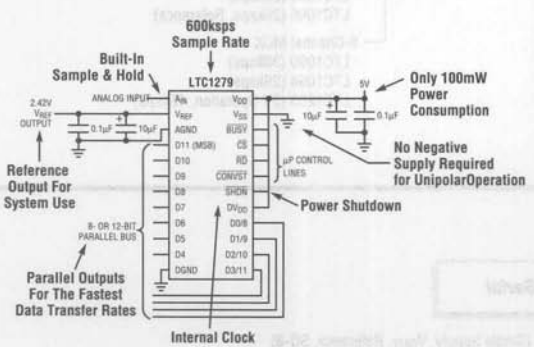


Complete Linear Technology 12-Bit A/D Feature Matrix

	SAMPLE RATE (ksps)	CONVERSION TIME (µs)	SUPPLY CURRENT (mA)	MICROPOWER	3V SINGLE SUPPLY OPERATION	5V SINGLE SUPPLY OPERATION	NUMBER OF INPUT CHANNELS	DIFFERENTIAL INPUT	BIPOLAR INPUT CAPABILITY	HALF DUPLEX SERIAL I/O	FULL DUPLEX SERIAL I/O	PARALLEL I/O	SOFTWARE CONFIGURE	ON-BOARD REFERENCE	MIN SPAN (V)	SHUTDOWN	SYSTEM SHUTDOWN OUTPUT	PACKAGES	NUMBER OF PINS	PRICE (100s, P DIP)
LTC1272-3	250	13	15			X					X		X	N/A				J, N, SOL	24	11.05
LTC1272-8	110	8	15			X					X		X	N/A				J, N, SOL	24	8.00
LTC1273	300	2.7	15			X					X		X	5				J, N, SOL	24	12.50
LTC1275	300	2.7	15			X			X		X		X	±2.5				J, N, SOL	24	11.75
LTC1276	300	2.7	15			X			X		X		X	±5				J, N, SOL	24	11.75
LTC1278-4	400	2	15			X			X		X		X	5 ±2.5	X			N, SOL	24	12.85†
LTC1278-5	500	1.6	15			X			X		X		X	5 ±2.5	X			N, SOL	24	13.70†
LTC1279	600	1.4	20			X			X				X	5 ±2.5	X			N, SOL	24	C.F.
LTC1282	140	5	8	X	X				X	X			X	2.5 ±1.25				J, N, SOL	24	14.00
LTC1285	7.5	160	0.12	X	X			X		X				1	X			N, SO	8	6.50
LTC1286	12.5	48	0.25			X		X		X				1	X			N, SO	8	5.25
LTC1287	30	24	1	X	X			X		X				1.2				J, N	8	16.70
LTC1288	6.6	180	0.16		X		2	X		X			X	2.7	X			N, SO	8	6.50
LTC1289	25	26	1		X		8	X	X		X		X	1.2	X			J, N, SOL	20	18.35
LTC1290	50	13	6			X	8	X	X		X		X	1.2	X			J, N, SOL	20	6.70
LTC1291	54	12	6			X	2	X		X			X	N/A	X			J, N	8	9.50
LTC1292	60	12	6			X		X		X				1.2				J, N	8	9.50
LTC1293	46	12	6			X	6	X	X	X			X	1.2	X			J, N, SOL	16	9.50
LTC1294	46	12	6			X	8	X	X	X			X	1.2	X			J, N	20	9.50
LTC1296	46	12	6	X		X	8	X	X	X			X	1.2	X	X		J, N	20	9.50
LTC1297	50	12	*	X		X		X		X				1.2	X			J, N	8	11.40
LTC1298	11.1	48	0.25			X	2			X		X	X	2.7	X			N, SO	8	5.25
LT574A	-	25	40 –25							X				X	10			N	28	11.40

* 6mA when active, 5µA when not converting: Average supply current depends on sample rate. †SO package price C.F. Call Factory

High Speed 12-Bit A/D Converters



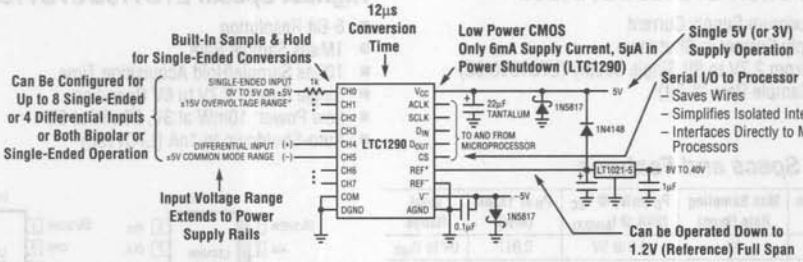
Comparison of Specs and Features

DEVICE TYPE	SAMPLING FREQ	S/(N + D) @ NYQUIST	INPUT RANGE	POWER SUPPLY	POWER DISSIPATION
LTC1272	250ksps	65dB	0V-5V	5V	75mW
LTC1273	300ksps	70dB	0V-5V	5V	75mW
LTC1275	300ksps	70dB	±2.5V	±5V	75mW
LTC1276	300ksps	70dB	±5V	±5V	75mW
LTC1278-4	400ksps	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 5mW*
LTC1278-5	500ksps	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 5mW*
LTC1279	600ksps	70dB	0V-5V or ±2.5V	5V or ±5V	100mW
LTC1282	140ksps	68dB	0V-2.5V or ±1.25V	3V or ±3V	12mW

*5mW power shutdown with instant wake up

Serial I/O 12-Bit A/D Converters

12-Bit Serial Interface A/D Converter Systems



Comparison of Specs and Features

Device Type	Analog Input Channels	Supply Voltage (V)	Sample Rate (ksps)	Number of Pins	Full/Half Duplex I/O	Auto Shutdown	Shutdown Status Pin
LTC1290	8	5/±5	50	20	Full		
LTC1291	2	5	54	8	Half		
LTC1292	1	5	60	8	Half		
LTC1293	6	5/±5	46	16	Half		
LTC1294	8	5/±5	46	20	Half		
LTC1296	8	5/±5	46	20	Half		X
LTC1297	1	5	50	8	Half	X	
LTC1287	1	3	30	8	Half		
LTC1289	8	3/±3	25	20	Full		

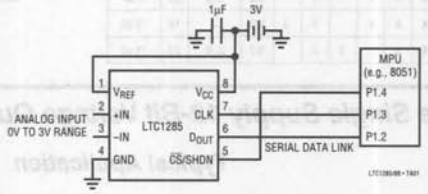
Micropower 12-Bit A/D Converters in SO-8 Packages

6

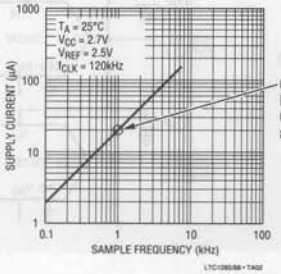
World's Lowest Power 12-Bit ADCs

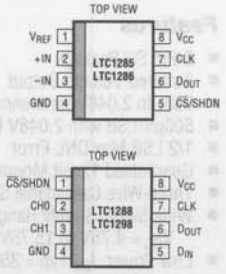
- 12-Bit Resolution
- 8-Pin SOIC Plastic Package
- Low Cost
- Low Supply Current: 160µA Typ (LT1285)
- Guaranteed ±3/4LSB Max DNL
- Auto-Shutdown to 1nA Typ
- Single Supply 3V to 6V Operation (LT1285/88) or 5V to 9V (LTC1286/98)
- On-Chip Sample-and-Hold
- 100µs Conversion Time
- Sampling Rates: 12.5ksps (LTC1286)
  11.1ksps (LTC1298)
- I/O Compatible with SPI, Microwire, etc.
- Differential Inputs (LTC1285, LTC1286)
- 2-Channel MUX (LTC1288, LTC1298)

12µW, SO-8 Package, 12-Bit ADC
Samples at 200Hz and Runs Off a 3V Battery



Supply Current vs Sample Rate (LTC1285)





SO-8 Package:
8-Lead Plastic SOIC

8-Bit A/D Converters in 8-Pin SO Packages

Lowest Power: LTC1096/LTC1098

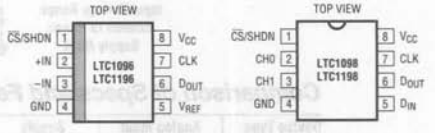
- 80µA Maximum Supply Current
- 1nA Supply Current in Shutdown
- Operate from 2.7V to 9V Single Supply (LTC1096/98)
- 33ksps Sample Rate (8-Bit)

Highest Speed: LTC1196/LTC1198

- 8-Bit Resolution
- 1Msps Sample Rate
- 100ns Sample/Hold Acquisition Time
- Single Supply 2.7V to 6V Operation
- Low Power: 10mW at 3V, 50mW at 5V
- Auto-Shutdown to 1nA (LTC1198)

Comparison of Specs and Features

Device Type	Supply Voltage Range (V_{CC})	Max Sampling Rate (ksps)	P_D (mW) @ V_{CC} MSR @ $f_{S(MAX)}$	P_D @ 1ksps (mW)	Input Range
LTC1096	2.7 to 9	33	0.6 @ 5V	0.017	0V to V_{REF}
LTC1098	2.7 to 6	33	0.6 @ 5V	0.017	0V to V_{CC}
LTC1196	2.7 to 6	1000	55 @ 5V	40	0V to V_{REF}
LTC1198	2.7 to 6	750	55 @ 5V	0.05	0V to V_{CC}

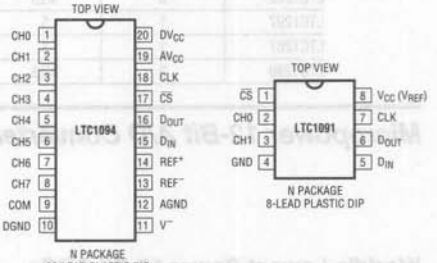


N8 Package: 8-Lead Plastic DIP
S8 Package: 8-Lead Plastic SOIC

10-Bit A/D Converter "Systems on a Chip"

	SAMPLE RATE (kHz)	CONVERSION TIME (µs)	SUPPLY CURRENT (mA)	3V SINGLE SUPPLY OPERATION	5V SINGLE SUPPLY OPERATION	NUMBER OF INPUT CHANNELS	DIFFERENTIAL INPUT	BIPOLAR INPUT CAPABILITY	HALF DUPLEX SERIAL I/O	FULL DUPLEX SERIAL I/O	SOFTWARE CONFIGURE	ON-BOARD REFERENCE	MIN SPAN (V)	PACKAGES	NUMBER OF PINS	PRICE (100+ # DIP)
LTC1090	30	22	1		X	8	X	X		X	X		0.2	J, N, SOL	20	9.90
LTC1091	31	20	1.5		X	2	X		X		X		N/A	J, N	8	9.90
LTC1092	38	20	1		X		X		X				0.2	J, N	8	9.90
LTC1093	26	20	1		X	6	X	X	X		X		0.2	J, N, SOL	16	9.90
LTC1094	26	20	1		X	8	X	X	X		X		0.2	J, N	20	9.90
LTC1095	26	20	2.3		X	6	X	X	X		X	X	N/A	J	18	12.00
LTC1283	15	44	0.15	X		8	X	X		X	X		0.2	J, N	20	11.40

Representative Pin Configurations



LTC1257: Complete Single Supply 12-Bit Voltage Output DAC in SO-8 Package

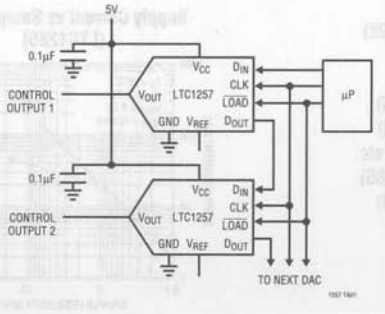
Features

- 8-Pin SO Package
- Buffered Voltage Output
- Built-In 2.048V Reference
- 500µV/LSB with 2.048V Full Scale
- 1/2 LSB Max DNL Error
- Guaranteed 12-Bit Monotonic
- Three-Wire Cascadable Serial Interface
- Wide Single Supply Range: V_{CC} = 4.75V to 15.75V
- Low Power: I_{CC} Typ = 350µA with 5V Supply

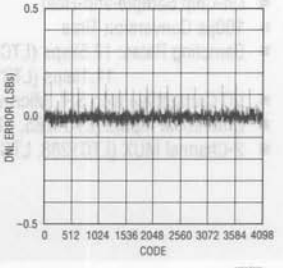
Applications

- Digital Offset/Gain Adjustment
- Industrial Process Control
- Automatic Test Equipment

Typical Application



Differential Nonlinearity vs Input Code



LINEAR TECHNOLOGY

SECTION 6—DATA CONVERSION

ANALOG TO DIGITAL CONVERTERS

LTC1096/LTC1098, Micropower Sampling 8-Bit Serial I/O A/D Converters 6-8
LTC1196/LTC1198, 8-Bit, SO-8, 1MSPS ADCs with Auto-Shutdown Options 6-32
LTC1273/LTC1275/LTC1276, 12-Bit, 300ksps Sampling A/D Converters with Reference 6-58
LTC1278, 12-Bit, 500ksps Sampling A/D Converter with Shutdown 6-80
LTC1282, 3V 140ksps 12-Bit Sampling A/D Converter with Reference 6-95
LTC1283, 3V Single Chip 10-Bit Data Acquisition System 6-117
LTC1285/LTC1288, 3V Micropower 12-Bit A/D Converters in SO-8 Packages 13-39
LTC1286/LTC1298, Micropower Sampling 12-Bit A/D Converters in SO-8 Packages 6-140
LTC1291, Single Chip 12-Bit Data Acquisition System 6-163
LTC1292/LTC1297, Single Chip 12-Bit Data Acquisition Systems 6-182

ANALOG TO DIGITAL CONVERTERS, *ENHANCED* SECOND SOURCE

LT574A, Complete 12-Bit A/D Converter 6-205

Micropower Sampling 8-Bit Serial I/O A/D Converters

FEATURES

- **80μA Maximum Supply Current**
- **1nA Typical Supply Current in Shutdown**
- **8-Pin SOIC Plastic Package**
- **Single Supply 3V to 9V Operation**
- **2.7V and 5V Specified**
- Sample-and-Hold
- 16μs Conversion Time
- 33kHz Sample Rate
- ±1/2LSB Total Unadjusted Error Over Temp
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports

APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Battery Gas Gauges
- Temperature Measurement
- Isolated Data Acquisition

DESCRIPTION

The LTC1096/LTC1098 are micropower, 8-bit A/D converters which draw only 80μA of supply current when converting. They automatically power down to 1nA typical supply current whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 3V to 9V supplies. These 8-bit, switched-capacitor, successive approximation ADCs include sample-and-hold. The LTC1096 has a single differential analog input. The LTC1098 offers a software selectable 2-channel MUX.

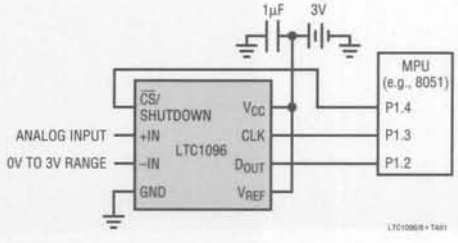
On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

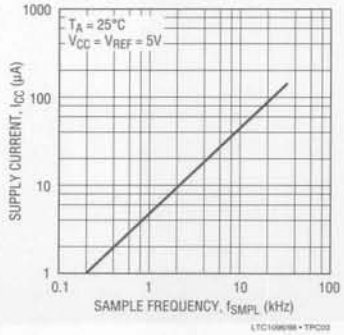
All grades are specified with offset and linearity errors of ±0.5LSB maximum over temperature. The A grade devices are specified with total unadjusted error of ±0.5LSB maximum over temperature.

TYPICAL APPLICATION

10μW, S-8 Package, 8-Bit A/D Samples at 200Hz and Runs Off a 3V Battery



Supply Current vs Sample Rate



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW

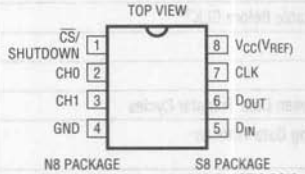
Operating Temperature
  LTC1096/LTC1098AC,
  LTC1096/LTC1098C ..... 0°C to 70°C
Storage Temperature Range ..... −65°c to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION (Notes 3)

N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

ORDER PART NUMBER
LTC1096ACN8
LTC1096CN8
LTC1096ACS8
LTC1096CS8
S8 PART MARKING
1096A
1096



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

ORDER PART NUMBER
LTC1098ACN8
LTC1098CN8
LTC1098ACS8
LTC1098CS8
S8 PART MARKING
1098A
1098

Consult factory for Industrial and Military grade parts.

6

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	LTC1096 LTC1098	2.7 2.7		9 6	V V
V_{CC} = 5V Operation						
f_{CLK}	Clock Frequency	V_{CC} = 5V	25		500	kHz
t_{CYC}	Total Cycle Time	LTC1096, f_{CLK} = 500kHz LTC1098, f_{CLK} = 500kHz	29 29			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 5V	150			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 5V, LTC1096 V_{CC} = 5V, LTC1098	500 500			ns ns
t_{WAKEUP}	Wakeup Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Figure 1 LTC1096 Operating Sequence)	V_{CC} = 5V, LTC1096	10			µs
	Wakeup Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Figure 2 LTC1098 Operating Sequence)	V_{CC} = 5V, LTC1098	10			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	400			ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	0.8			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	0.8			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	1			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096, f_{CLK} = 500kHz LTC1098, f_{CLK} = 500kHz	28 28			µs µs

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 2.7V Operation						
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	25		250	kHz
t_{CYC}	Total Cycle Time	LTC1096, f_{CLK} = 250kHz LTC1098, f_{CLK} = 250kHz	58 58			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 2.7V, LTC1096 V_{CC} = 2.7V, LTC1098	1 1			µs µs
t_{WAKEUP}	Wakeup Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Figure 1 LTC1096 Operating Sequence)	V_{CC} = 2.7V, LTC1096	10			µs
	Wakeup Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Figure 2 LTC1098 Operating Sequence)	V_{CC} = 2.7V, LTC1098	10			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	1			µs
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	1.6			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	1.6			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 2.7V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096, f_{CLK} = 250kHz LTC1098, f_{CLK} = 250kHz	56 56			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 500kHz, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1096A/LTC1098A MIN	LTC1096A/LTC1098A TYP	LTC1096A/LTC1098A MAX	LTC1096/LTC1098 MIN	LTC1096/LTC1098 TYP	LTC1096/LTC1098 MAX	UNITS
Resolution (No Missing Code)		●	8			8			Bits
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Note 4)	●			±0.5			±0.5	LSB
Full Scale Error		●			±0.5			±1.0	LSB
Total Unadjusted Error (Note 5)	V_{REF} = 5.000V	●			±0.5			±1.0	LSB
Analog Input Range	(Notes 6 and 7)				−0.05V to V_{CC} + 0.05V				V
REF Input Range (Notes 6 and 7)	4.5 ≤ V_{CC} ≤ 6V 6V < V_{CC} ≤ 9V, LTC1096				−0.05V to V_{CC} + 0.05V −0.05V to 6V				V V
Analog Input Leakage Current	(Note 8)	●			±1.0			±1.0	µA

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1096A/LTC1098A MIN	LTC1096A/LTC1098A TYP	LTC1096A/LTC1098A MAX	LTC1096/LTC1098 MIN	LTC1096/LTC1098 TYP	LTC1096/LTC1098 MAX	UNITS
Resolution (No Missing Code)		●	8			8			Bits
Offset Error		●			±0.5			±1.0	LSB
Linearity Error	(Notes 4 and 9)	●			±0.5			±1.0	LSB
Full Scale Error		●			±0.5			±1.0	LSB
Total Unadjusted Error (Notes 5 and 9)	V_{REF} = 2.500V	●			±1.0			±1.5	LSB
Analog Input Range	(Notes 6 and 7)				−0.05V to V_{CC} + 0.05V				V
REF Input Range (Notes 6, 7, and 9)	2.7 ≤ V_{CC} ≤ 6V				−0.05V to V_{CC} + 0.05V				V
Analog Input Leakage Current	(Notes 8 and 9)	●			±1.0			±1.0	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA	●	4.5	4.74		V
		I_O = 360µA	●	2.4	4.72		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS} \geq V_{IH}$	●			±3.0	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		mA
I_{REF}	Reference Current	$\overline{CS} = V_{CC}$	●		0.001	2.5	µA
		$t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		3.500	7.5	µA
		t_{CYC} = 29µs, f_{CLK} = 500kHz	●		35.00	50.0	µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$	●		0.001	3.0	µA
		LTC1096, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		40	80	µA
		LTC1096, t_{CYC} = 29µs, f_{CLK} = 500kHz	●		120	180	µA
		LTC1098, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		44	88	µA
		LTC1098, t_{CYC} = 29µs, f_{CLK} = 500kHz	●		155	230	µA

V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current (Note 9)	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current (Note 9)	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA	●	2.3	2.69		V
		I_O = 360µA	●	2.1	2.64		V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage (Note 9)	$\overline{CS} \geq V_{IH}$	●			±3.0	µA
I_{SOURCE}	Output Source Current (Note 9)	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current (Note 9)	$V_{OUT} = V_{CC}$			15		mA
I_{REF}	Reference Current (Note 9)	$\overline{CS} = V_{CC}$	●		0.001	2.5	µA
		$t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		3.500	7.5	µA
		t_{CYC} = 58µs, f_{CLK} = 250kHz	●		35.00	50.0	µA
I_{CC}	Supply Current (Note 9)	$\overline{CS} = V_{CC}$	●		0.001	3.0	µA
		LTC1096, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		40	80	µA
		LTC1096, t_{CYC} = 58µs, f_{CLK} = 250kHz	●		120	180	µA
		LTC1098, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$	●		44	88	µA
		LTC1098, t_{CYC} = 58µs, f_{CLK} = 250kHz	●		155	230	µA

6

AC CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 500kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	33			kHz
t_{CONV}	Conversion Time	See Operating Sequence			8		CLK Cycles
t_{dDO}	Delay Time, $\overline{CLK}\downarrow$ to D_{OUT} Data Valid	See Test Circuits	●		200	450	ns
t_{dis}	Delay Time, CS↑ to D_{OUT} Hi-Z	See Test Circuits	●		170	450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		60	250	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			180		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	100	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel			25		pF
		Off Channel			5		pF
		Digital Input			5		pF

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	16.5			kHz
t_{CONV}	Conversion Time	See Operating Sequence			8		CLK Cycles
t_{dDO}	Delay Time, $\overline{CLK}\downarrow$ to D_{OUT} Data Valid	See Test Circuits (Note 9)	●		500	1000	ns
t_{dis}	Delay Time, CS↑ to D_{OUT} Hi-Z	See Test Circuits (Note 9)	●		220	800	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits (Note 9)	●		160	480	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			400		ns
t_f	D_{OUT} Fall Time	See Test Circuits (Note 9)	●		70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits (Note 9)	●		50	150	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel			25		pF
		Off Channel			5		pF
		Digital Input			5		pF

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For the 8-lead plastic DIP, consult the factory.

Note 4: Linearity error is specified between the actual and points of the A/D transfer curve.

Note 5: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for $2.7V \le V_{CC} \le 5.5V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading. For $5.5V < V_{CC} \le 9V$, reference and analog input range cannot exceed 5.55V. If reference and analog input range are greater than 5.55V, the output code will not be guaranteed to be correct.

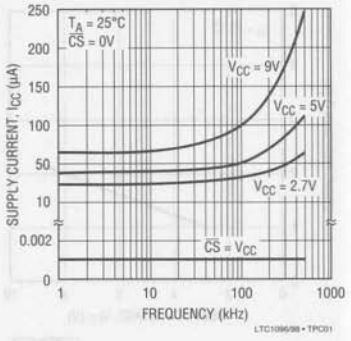
Note 7: The supply voltage range for the LTC1096 is from 2.7V to 9V, but the supply voltage range for the LTC1098 is only from 2.7V to 6V.

Note 8: Channel leakage current is measured after the channel selection.

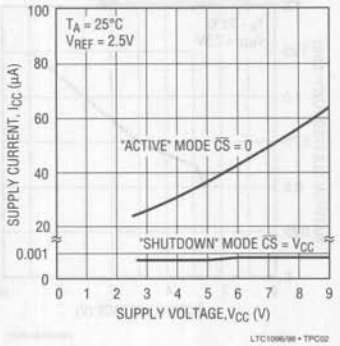
Note 9: These specifications are either correlated from 5V specifications or guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

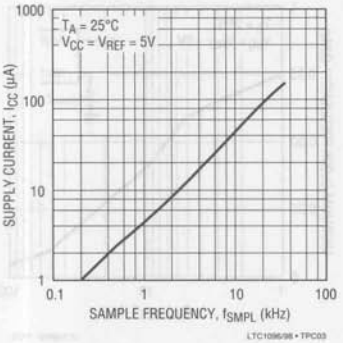
Supply Current vs Clock Rate for Active and Shutdown Modes



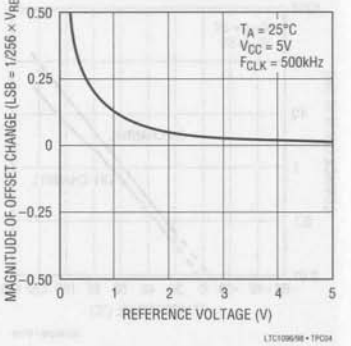
Supply Current vs Supply Voltage Active and Shutdown Modes



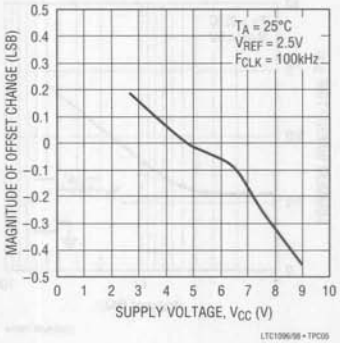
Supply Current vs Sample Frequency LTC1096



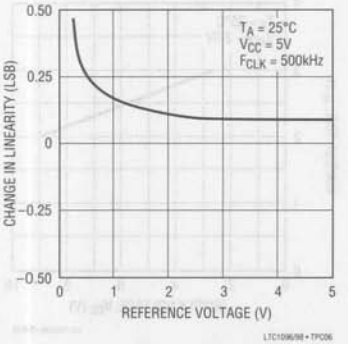
Change in Offset vs Reference Voltage LTC1096



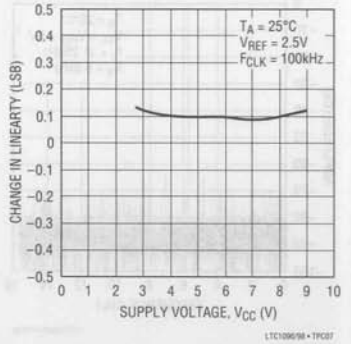
Change in Offset vs Supply Voltage



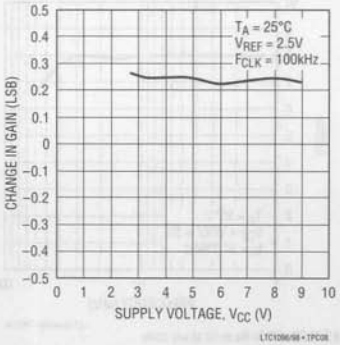
Change in Linearity vs Reference Voltage LTC1096



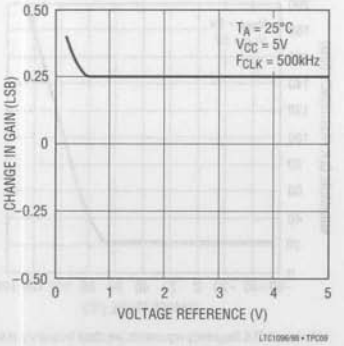
Change in Linearity vs Supply Voltage



Change in Gain vs Supply Voltage



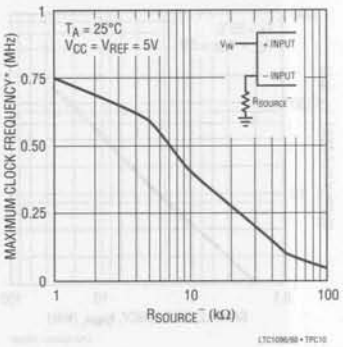
Change in Gain vs Reference Voltage LTC1096



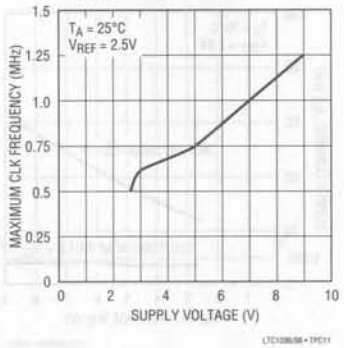
6

TYPICAL PERFORMANCE CHARACTERISTICS

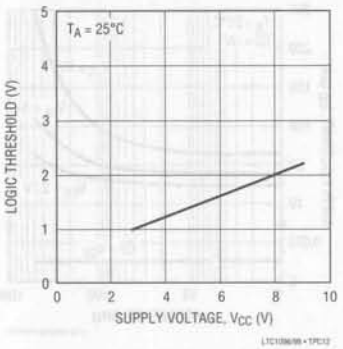
Maximum Clock Frequency vs Source Resistance



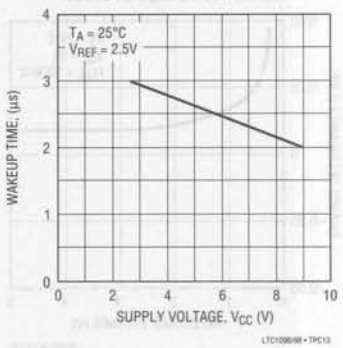
Maximum Clock Frequency vs Supply Voltage



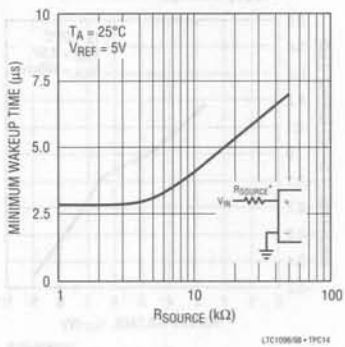
Digital Input Logic Threshold vs Supply Voltage



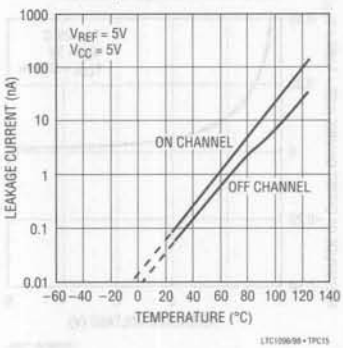
Wakeup Time vs Supply Voltage



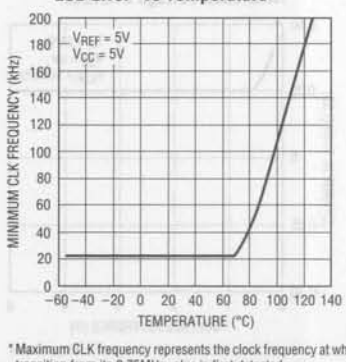
Minimum Wakeup Time vs Source Resistance



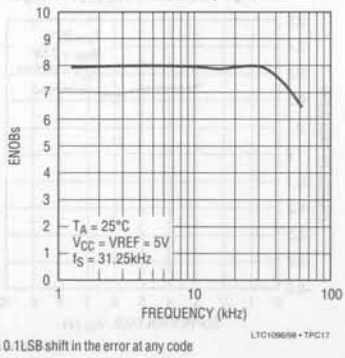
Input Channel Leakage Current vs Temperature



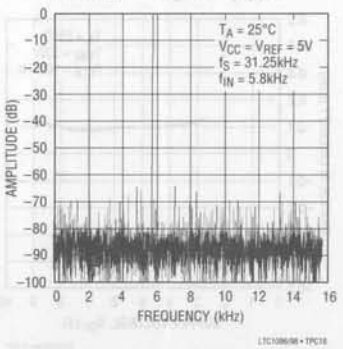
Minimum Clock Frequency for 0.1 LSB Error† vs Temperature



ENOBs vs Frequency



FFT Plot



* Maximum CLK frequency represents the clock frequency at which a 0.1LSB shift in the error at any code transition from its 0.75MHz value is first detected.

† As the CLK frequency is decreased from 500kHz, minimum CLK frequency (Δerror ≤ 0.1LSB) represents the frequency at which a 0.1LSB shift in any code transition from its 500kHz value is first detected.

PIN FUNCTIONS

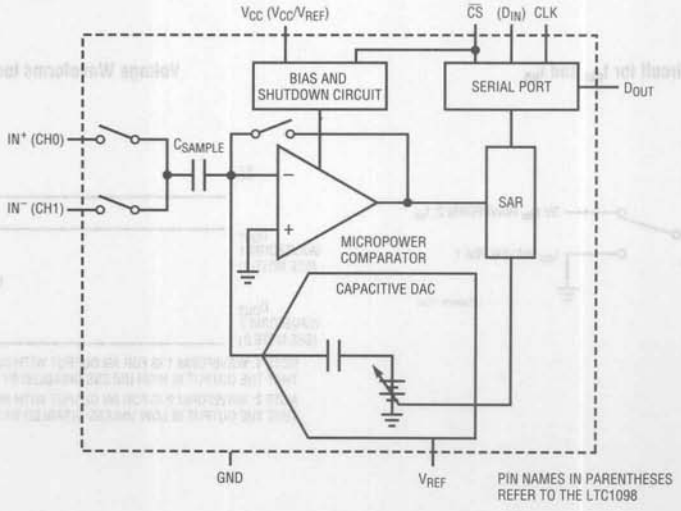
LTC1096

#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$/SHUTDOWN	Chip Select Input	A logic low on this input enables the LTC1096. A logic high on this input disables the LTC1096 and disconnects the power to LTC1096.
2	IN^+	Analog Input	This input must be free of noise with respect to GND.
3	IN^-	Analog Input	This input must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	V_{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC}	Power Supply Voltage	This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1098

#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$/SHUTDOWN	Chip Select Input	A logic low on this input enables the LTC1098. A logic high on this input disables the LTC1098 and disconnects the power to LTC1098.
2	CH0	Analog Input	This input must be free of noise with respect to GND.
3	CH1	Analog Input	This input must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	D_{IN}	Digital Data Input	The multiplexer address is shifted into this input.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	$V_{CC}(V_{REF})$	Power Supply and Reference Voltage	This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

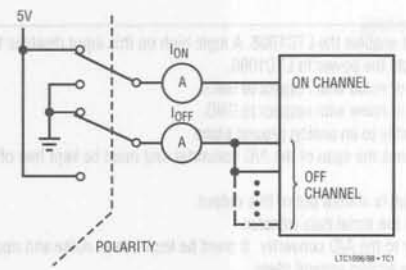
BLOCK DIAGRAM



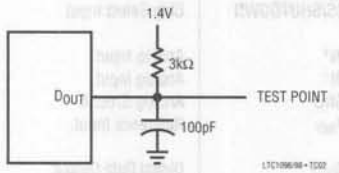
6

TEST CIRCUITS

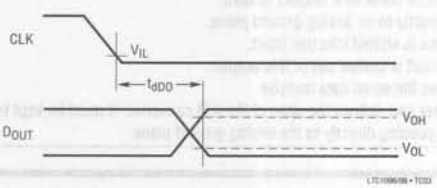
On and Off Channel Leakage Current



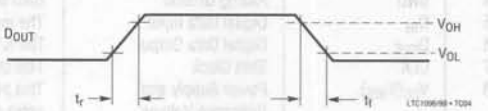
Load Circuit for t_{dDO}, t_r and t_f



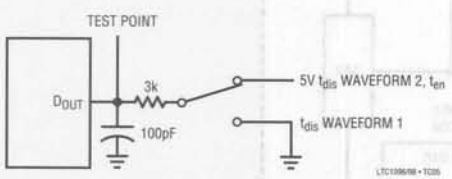
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



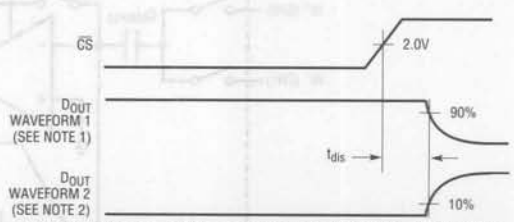
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Load Circuit for t_{dis} and t_{en}



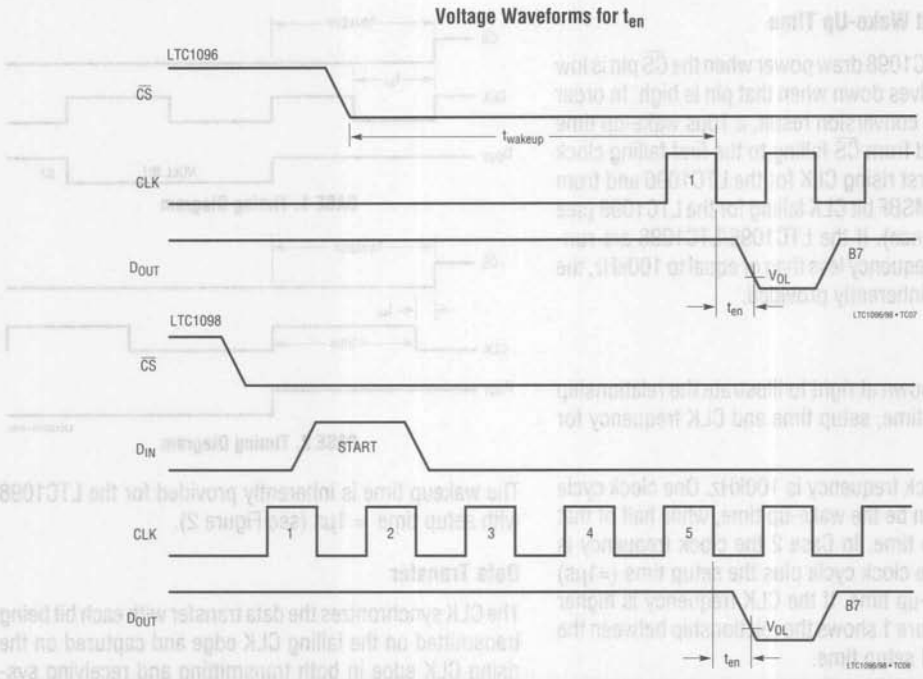
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS



APPLICATIONS INFORMATION

OVERVIEW

The LTC1096 and LTC1098 are 8-bit micropower, switched-capacitor A/D converters. These sampling ADCs typically draw 100μA of supply current when sampling at 33kHz. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate on page 1). The ADCs automatically power down when not performing conversion, drawing only leakage current. They are packaged in 8-pin SO packages. The LTC1096 operates on a single supply ranging from 2.7V to 9V while the LTC1098 operates from 2.7V to 6V supplies.

Both the LTC1096 and the LTC1098 comprise an 8-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1096 and LTC1098 differ in some respects. The LTC1096 has a differential input and has an external reference input pin. It can measure signals floating on a DC common mode voltage and can operate with reduced spans down to 250mV. Reducing the span allows it to achieve 1mV resolution. The LTC1098 has a 2-channel input multiplexer and can convert either channel with respect to ground or the difference between the two.

SERIAL INTERFACE

The LTC1098 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface while the LTC1096 uses a 3-wire interface (see Operating Sequence in Figure 1 and 2).

APPLICATIONS INFORMATION

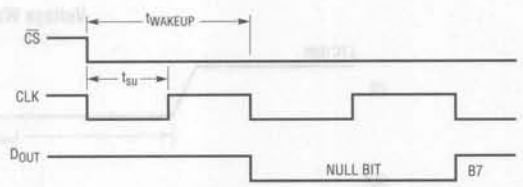
Power Down and Wake-Up Time

The LTC1096/LTC1098 draw power when the $\overline{CS}$ pin is low and shut themselves down when that pin is high. In order to have a correct conversion result, a 10µs wake-up time must be provided from $\overline{CS}$ falling to the first falling clock (CLK) after the first rising CLK for the LTC1096 and from $\overline{CS}$ falling to the MSBF bit CLK falling for the LTC1098 (see Operating Sequence). If the LTC1096/LTC1098 are running with clock frequency less than or equal to 100kHz, the wake-up time is inherently provided.

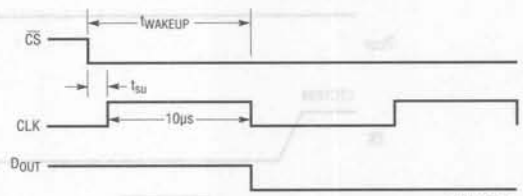
Example

Two cases are shown at right to illustrate the relationship among wake-up time, setup time and CLK frequency for the LT1096.

In Case 1 the clock frequency is 100kHz. One clock cycle is 10µs which can be the wake-up time, while half of that can be the setup time. In Case 2 the clock frequency is 50kHz, half of the clock cycle plus the setup time (=1µs) can be the wake-up time. If the CLK frequency is higher than 100kHz, Figure 1 shows the relationship between the wakeup time and setup time.



CASE 1. Timing Diagram

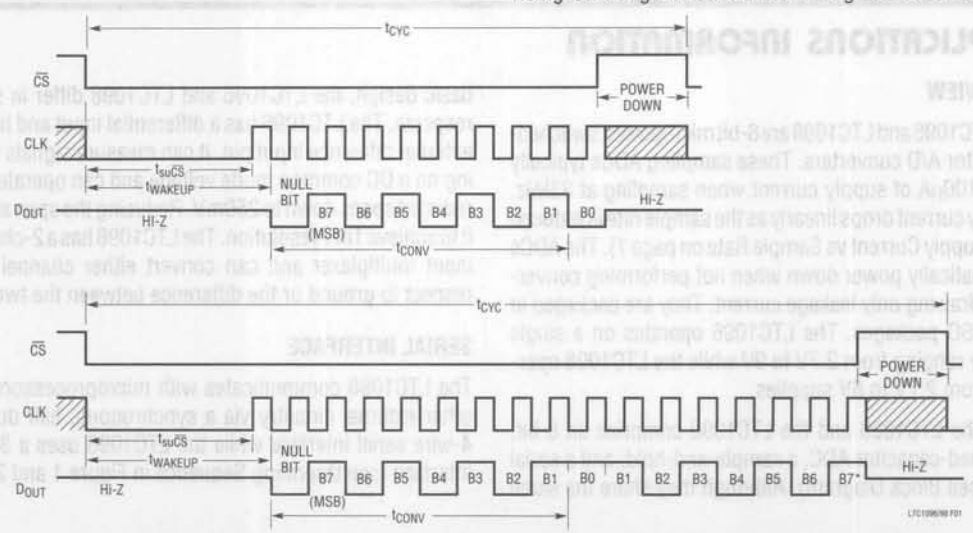


CASE 2. Timing Diagram

The wakeup time is inherently provided for the LTC1098 with setup time = 1µs (see Figure 2).

Data Transfer

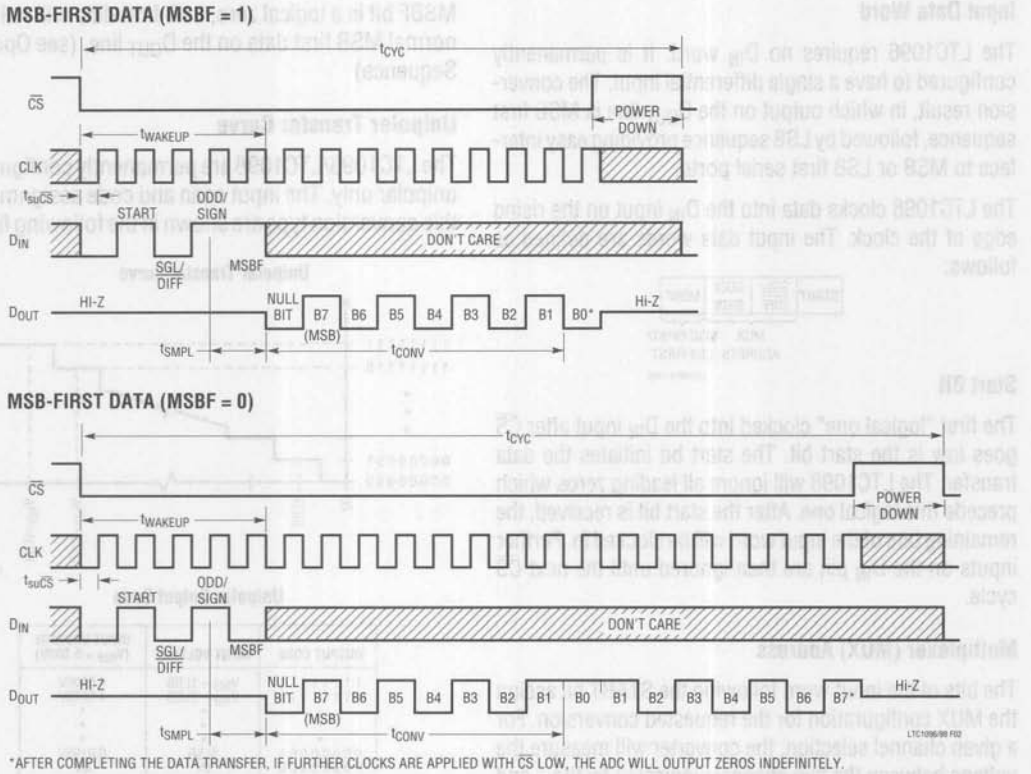
The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving sys-



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

Figure 1. LTC1096 Operating Sequence

APPLICATIONS INFORMATION

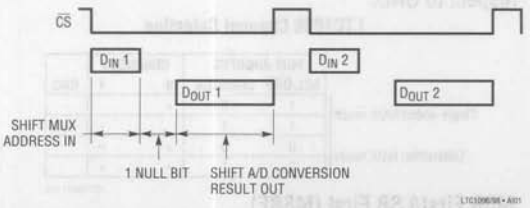


*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

Figure 2. LTC1098 Operating Sequence Example: Differential Inputs (CH⁺, CH⁻)

tems. The LTC1098 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1098 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1098 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1098 in preparation for the next data exchange.



The LTC1096 does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1096 operating sequence. After $\overline{CS}$ falls, the first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1096 for the next data exchange.

APPLICATIONS INFORMATION

Input Data Word

The LTC1096 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result, in which output on the D_{OUT} line is MSB first sequence, followed by LSB sequence providing easy interface to MSB or LSB first serial ports.

The LTC1098 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1098 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the followintg tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1098 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/$\overline{DIFF}$	ODD/SIGN	0	1	GND
Single-ended MUX mode	1	0	+		–
	1	1		+	–
Differential MUX mode	0	0	+	–	
	0	1	–	+	

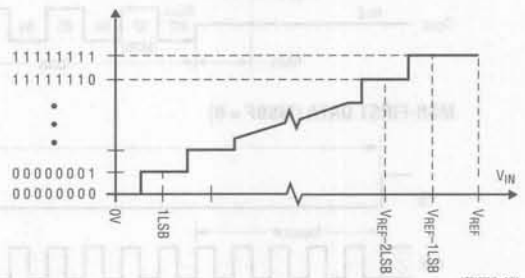
MSB First/LSB First (MSBF)

The output data of the LTC1098 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (see Operating Sequence)

Unipolar Transfer Curve

The LTC1096/LTC1098 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Unipolar Transfer Curve



Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111	V_{REF} – 1LSB	4.9805V
11111110	V_{REF} – 2LSB	4.9609V
•	•	•
•	•	•
•	•	•
00000001	1LSB	0.0195V
00000000	0V	0V

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1098 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1098 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1098 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

APPLICATIONS INFORMATION

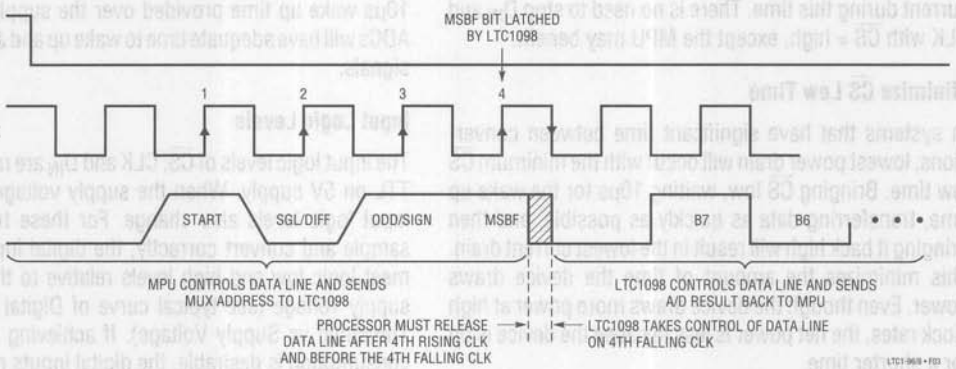


Figure 3. LTC1098 Operation with D_{IN} and D_{OUT} Tied Together

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 40μA and automatic shutdown between conversions, the LTC1096/LTC1098 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). In systems that convert continuously, the LTC1096/LTC1098 will draw its normal operating power continuously. Figure 5 shows that the typical current varies from 40μA at clock rates below 50kHz to 100μA at 500kHz. Several things must be taken into account to achieve such a low power consumption.

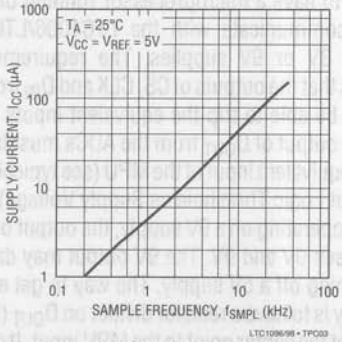


Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate.

Shutdown

Figures 1 and 2 show the operating sequence of the LTC1096/LTC1098. The converter draws power when the

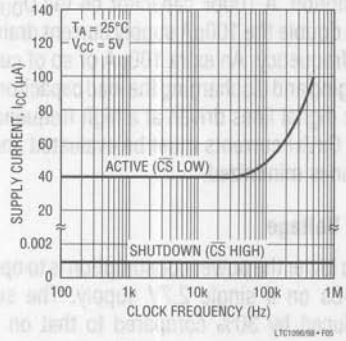


Figure 5. After a conversion, when the microprocessor drives $\overline{CS}$ high, the ADC automatically shuts down until the next conversion. The supply current, which is very low during conversions, drops to zero in shutdown.

$\overline{CS}$ pin is low and powers itself down when that pin is high. If the $\overline{CS}$ pin is not taken to ground when it is low and not taken to supply voltage when it is high, the input buffers of the converter will draw current. This current may be larger than the typical supply current. It is worthwhile to bring the $\overline{CS}$ pin all the way to ground when it is low and all the way to supply voltage when it is high to obtain the lowest supply current.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input have no effect on supply

APPLICATIONS INFORMATION

current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high, except the MPU may benefit.

Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, waiting 10µs for the wake up time, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. Even though the device draws more power at high clock rates, the net power is less because the device is on for a shorter time.

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can more than double the 100µA supply current drain at a 500kHz clock frequency. An extra 100µA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The CxVxf currents must be evaluated and the troublesome ones minimized.

Lower Supply Voltage

Another way to lower the power consumption is to operate these two ADCs on a single 2.7V supply. The supply current is reduced by 30% compared to that on a 5V supply and the power consumption is 60% lower than that on a 5V supply (see typical curve of Supply Current vs Supply Voltage).

OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1096 operates from 2.7V to 9V supplies and the LTC1098 operates from 2.7V to 6V supplies. To operate the LTC1096/LTC1098 on other than 5V supplies, a few things must be kept in mind.

Wake Up Time

A 10µs wake up time must be provided for the ADCs to convert correctly on a 5V supply. The wake up time is typically less than 3µs over the supply voltage range (see typical curve of Wake Up Time vs Supply Voltage). With 10µs wake up time provided over the supply range, the ADCs will have adequate time to wake up and acquire input signals.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on 5V supply. When the supply voltage varies, the input logic levels also change. For these two ADCs to sample and convert correctly, the digital inputs have to meet logic low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

Clock Frequency

The maximum recommended clock frequency is 500kHz for the LTC1096/LTC1098 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1096/LTC1098 operating on 3V or 9V supplies. The requirement to achieve this is that the outputs of $\overline{CS}$, CLK and D_{IN} from the MPU have to be able to trip the equivalent inputs of the ADCs and the output of D_{OUT} from the ADCs must be able to toggle the equivalent input of the MPU (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1096 operating on a 9V supply, the output of D_{OUT} may go between 0V and 9V. The 9V output may damage the MPU running off a 5V supply. The way to get around this possibility is to have a resistor divider on D_{OUT} (Figure 6) and connect the center point to the MPU input. It should be noted that to get full shutdown, the $\overline{CS}$ input of the LTC1096/LTC1098 must be driven to the V_{CC} voltage. This would require adding a level shift circuit to the $\overline{CS}$ signal in Figure 6.

APPLICATIONS INFORMATION

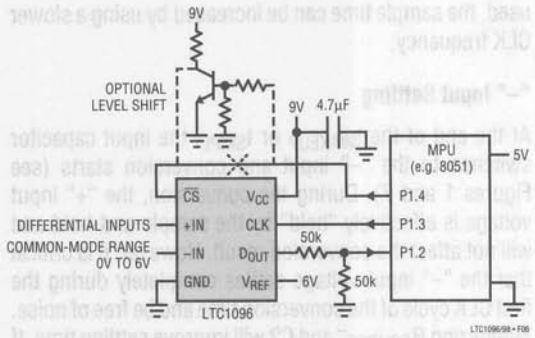


Figure 6. Interfacing a 9V Powered LTC1096 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1096/LTC1098 should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 1µF tantalum with leads as short as possible. If power supply is clean, the LTC1096/LTC1098 can also operate with smaller 0.1µF surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1096 and the LTC1098 provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1096 acquires input signals from "+" input relative to "–" input during the t_{WAKEUP} time (see Figure 1). However, the S&H of the LTC1098 can sample input signals in the single-ended mode or in the differential inputs during the t_{SMPL} time (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1098 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

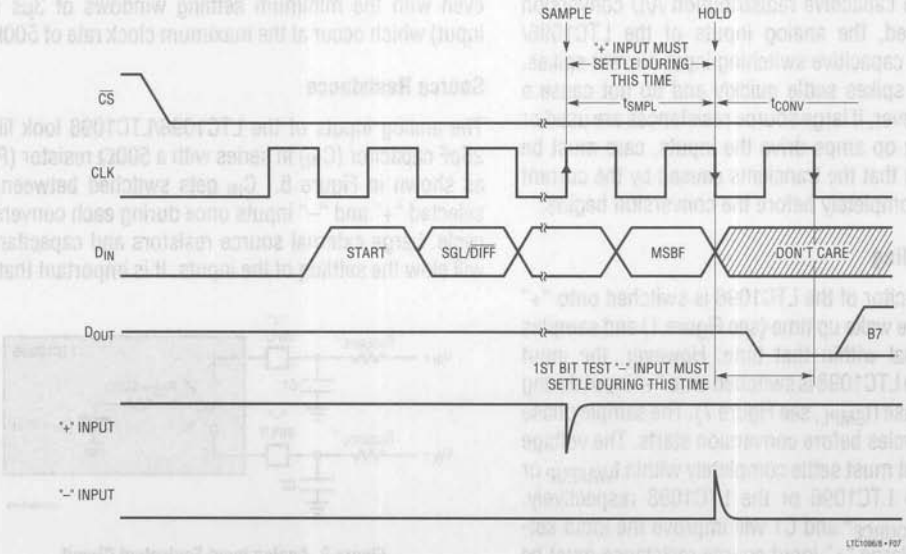


Figure 7. LTC1098 "+" and "–" Input Settling Windows

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Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 8 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 8/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (5mV) with the converter running at CLK = 500kHz, its peak value would have to be 750mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1096/LTC1098 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1096 is switched onto "+" input during the wake up time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1098 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 1 1/2 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{WAKEUP} or t_{SMPLE} for the LTC1096 or the LTC1098 respectively. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"–" Input Settling

At the end of the t_{WAKEUP} or t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 3µs ("+" input) which occur at the maximum clock rate of 500kHz.

Source Resistance

The analog inputs of the LTC1096/LTC1098 look like a 25pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the

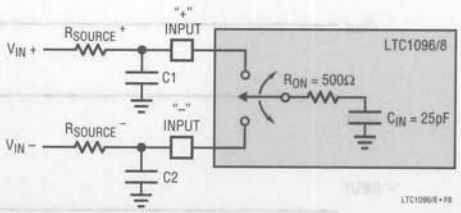

Figure 8. Analog Input Equivalent Circuit

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overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 25pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 29µs, the input current equals 4.3µA at V_{IN} = 5V. In this case, a filter resistor of 390Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

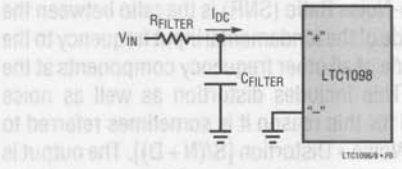

Figure 9. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 3.9k will cause a voltage drop of 3.9mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The voltage on the reference input of the LTC1096 defines the voltage span of the A/D converter. The reference input transient capacitive switching currents due to the switched-capacitor conversion technique (see Figure 10). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These current spikes settle quickly and do not cause a problem.

Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2µs bit time.

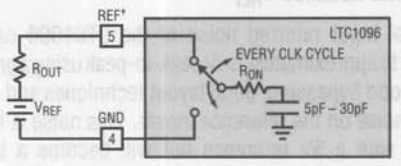

Figure 10. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1098 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1096 can operate with reference voltages below 1V.

The effective resolution of the LTC1096 can be increased by reducing the input span of the converter. The LTC1096 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1096 has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 2mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a

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0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1096.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1096 can be reduced to approximately 1mV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 1mV noise is only 0.05LSB peak-to-peak. In this case, the LTC1096 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 1mV noise is 0.25LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 200mV, the 1mV noise becomes equal to 1.25LSBs and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1096 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

Input Divider

It is OK to use an input divider on the reference input of the LTC1096 as long as the reference input can be made to settle within the bit time at which the clock is running. When using a larger value resistor divider on the reference input the "–" input should be matched with an equivalent resistance.

Bypassing Reference Input with Divider

Bypassing the reference input with a divider is also possible. However care must be taken to make sure that the DC voltage on the reference input will not drop too much below the intended reference voltage.

AC PERFORMANCE

Two commonly used figures of merit for specifying the dynamic performance of the ADCs in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits (ENOB).

Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. This includes distortion as well as noise products and for this reason it is sometimes referred to as Signal-to-Noise + Distortion [S/(N + D)]. The output is band limited to frequencies from DC to one half the sampling frequency. Figure 11 shows spectral content from DC to 15.625kHz which is 1/2 the 31.25kHz sampling rate.

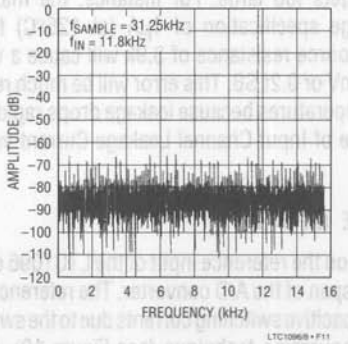

Figure 11. This clean FFT of an 11.8kHz input shows remarkable performance for an ADC that draws only 100μA when sampling at the 31.25kHz rate.

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Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an A/D and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 33kHz the LTC1096 maintains 7.5 ENOBs or better to 40kHz. Above 40kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains approximately 70dB.

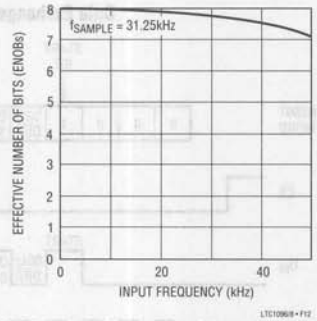


Figure 12. Dynamic Accuracy is Maintained Up to an Input Frequency of 40kHz

TYPICAL APPLICATIONS

MICROPROCESSOR INTERFACES

The LTC1096/LTC1098 can interface directly (without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1096/LTC1098. Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC05C4,CM68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfer data MSB first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the D_{IN} word to the LTC1098 and clocks into the processor. The second 8-bit transfer clocks the A/D conversion result, B7 through B0, into the MPU.

ANDing the first MUP received byte with 00Hex clears the first byte. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1096/LTC1098

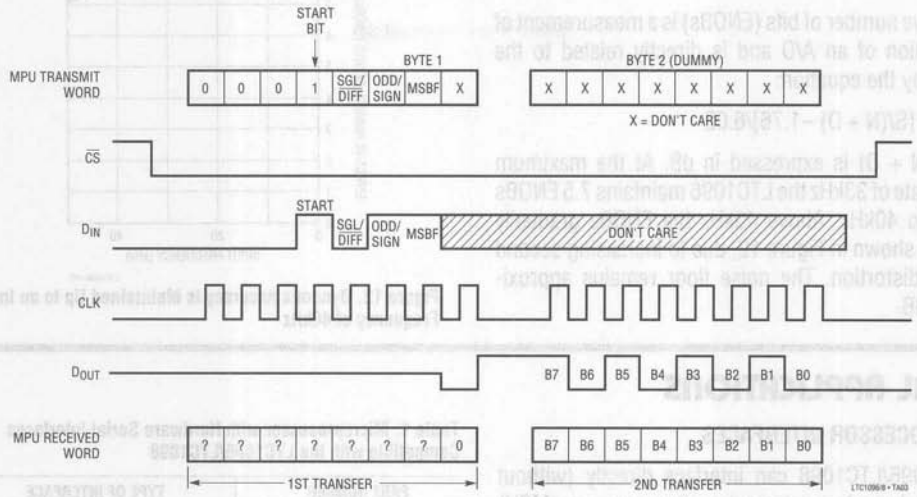
PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2,S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIR/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port

* Requires external hardware

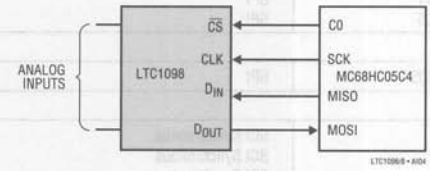
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

TYPICAL APPLICATIONS

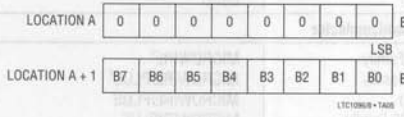
Data Exchange Between LTC1098 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4



D_{OUT} from LTC1098 Stored in MC68HC05C4



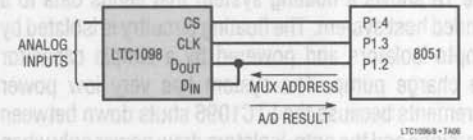
LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load LTC1098 D_{IN} word into Acc.
	STA	Load LTC1098 D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear the first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

Interfacing to the Parallel Port of the INTEL 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1098 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1098 tied together as described in the SERIAL INTERFACE section. This saves one wire.

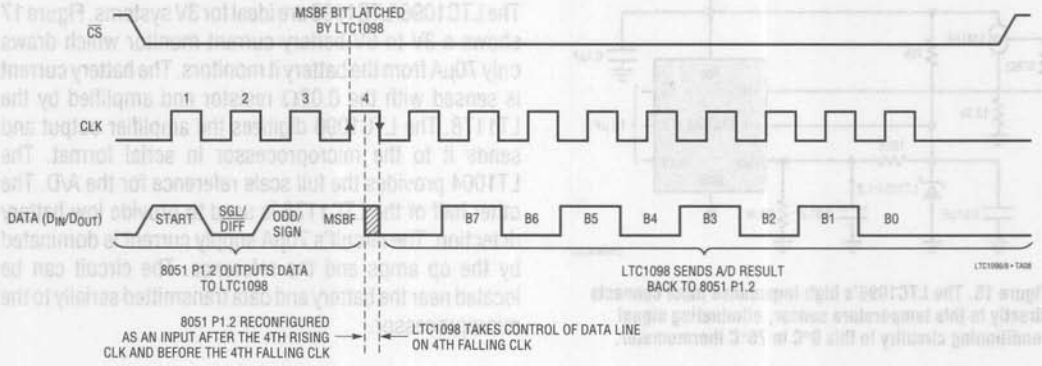
The 8051 first sends the start bit and MUX address to the LTC1098 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 8-bit A/D result over the same data line.

TYPICAL APPLICATIONS



DOUT FROM LTC1098 STORED IN 8051 RAM

LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1098
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	CLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1098
	SETB	P1.3	CLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	CLK goes low
	MOV	R4, #09	Load counter
LOOP	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	SETB	P1.4	$\overline{CS}$ goes high



A "Quick Look" Circuit for the LTC1096

Users can get a quick look at the function and timing of the LT1096 by using the following simple circuit (Figure 13). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74C161 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 14). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

Figure 15 shows a temperature measurement system. The LTC1096 is connected directly to the low cost silicon temperature sensor. The voltage applied to the V_{REF} pin adjusts the full scale of the A/D to the output range of the sensor. The zero point of the converter is matched to the zero output voltage of the sensor by the voltage on the LTC1096's negative input.

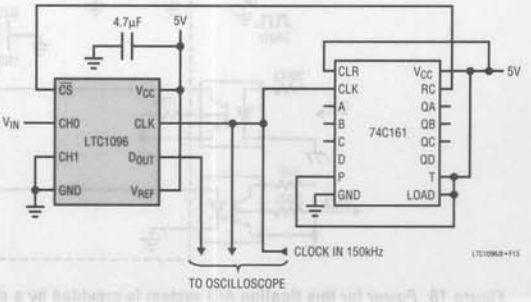


Figure 13. "Quick Look" Circuit for the LTC1096

TYPICAL APPLICATIONS

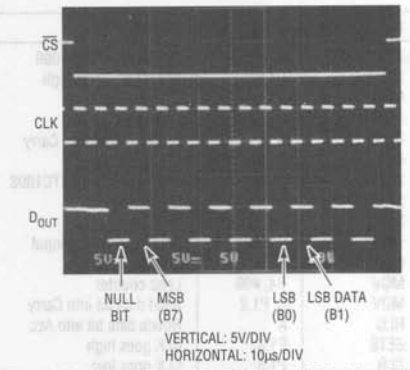


Figure 14. Scope Trace the LTC1096 "Quick Look" Circuit Showing A/D Output 10101010 (AA_{HEX})

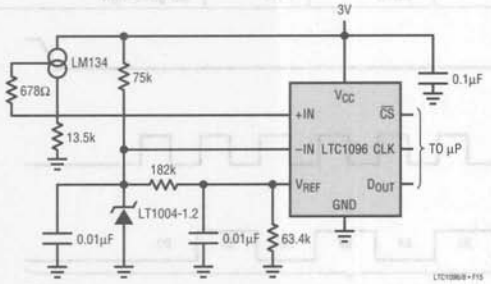


Figure 15. The LTC1096's high impedance input connects directly to this temperature sensor, eliminating signal conditioning circuitry in this 0°C to 70°C thermometer.

Remote or Isolated Systems

Figure 16 shows a floating system that sends data to a grounded host system. The floating circuitry is isolated by two opto-isolators and powered by a simple capacitor diode charge pump. The system has very low power requirements because the LTC1096 shuts down between conversions and the opto-isolators draw power only when data is being transferred. The system consumes only 50µA at a sample rate of 10Hz (1ms on-time and 99ms off-time). This is easily within the current supplied by the charge pump running at 5MHz. If a truly isolated system is required, the system's low power simplifies generating an isolated supply or powering the system from a battery.

A/D Conversion for 3V Systems

The LTC1096/LTC1098 are ideal for 3V systems. Figure 17 shows a 3V to 6V battery current monitor which draws only 70µA from the battery it monitors. The battery current is sensed with the 0.02Ω resistor and amplified by the LT1178. The LTC1096 digitizes the amplifier output and sends it to the microprocessor in serial format. The LT1004 provides the full scale reference for the A/D. The other half of the LTC1178 is used to provide low battery detection. The circuit's 70µA supply current is dominated by the op amps and the reference. The circuit can be located near the battery and data transmitted serially to the microprocessor.

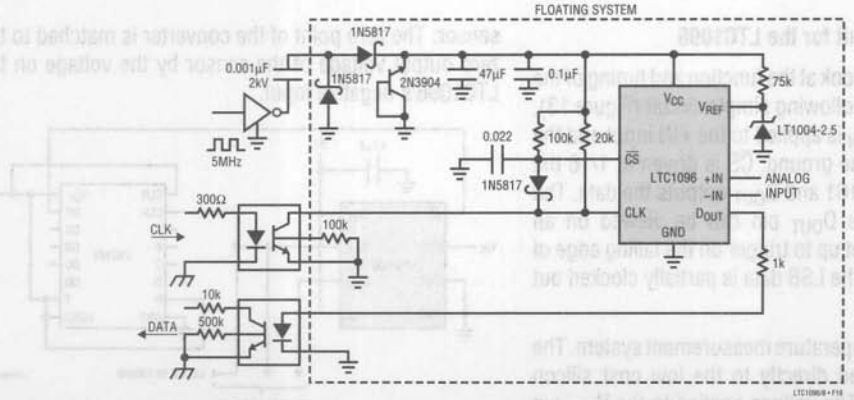


Figure 16. Power for this floating A/D system is provided by a simple capacitor diode charge pump. The two opto-isolators draw no current between samples, turning on only to send the clock and receive data.

TYPICAL APPLICATIONS

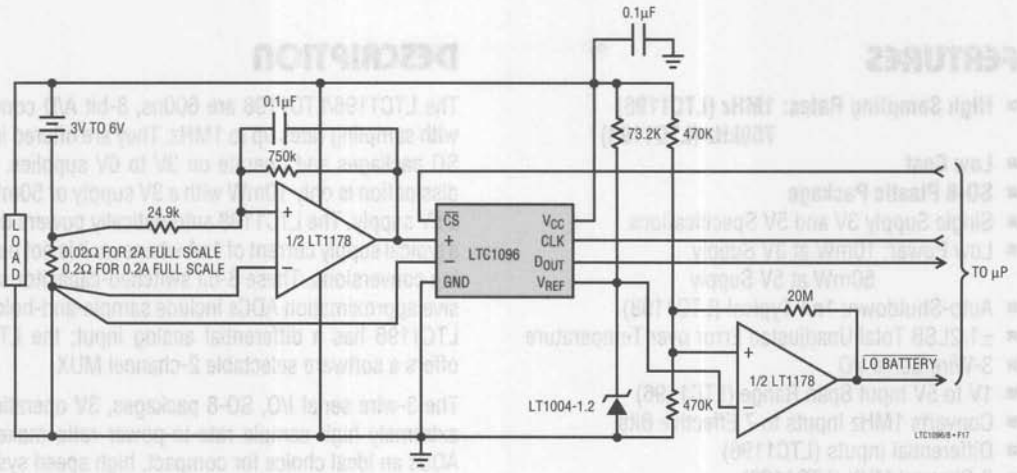


Figure 17. This 0A to 2A Battery Current Monitor Draws Only 70µA from a 3V Battery

6

8-Bit, SO-8, 1MSPS ADCs with Auto-Shutdown Options

FEATURES

- **High Sampling Rates: 1MHz (LTC1196)**
  750kHz (LTC1198)
- **Low Cost**
- **SO-8 Plastic Package**
- Single Supply 3V and 5V Specifications
- Low Power: 10mW at 3V Supply
  50mW at 5V Supply
- Auto-Shutdown: 1nA Typical (LTC1198)
- ±1/2LSB Total Unadjusted Error over Temperature
- 3-Wire Serial I/O
- 1V to 5V Input Span Range (LTC1196)
- Converts 1MHz Inputs to 7 Effective Bits
- Differential Inputs (LTC1196)
- 2-Channel MUX (LTC1198)

APPLICATIONS

- High Speed Data Acquisition
- Disk Drives
- Portable or Compact Instrumentation
- Low Power or Battery-Operated Systems

DESCRIPTION

The LTC1196/LTC1198 are 600ns, 8-bit A/D converters with sampling rates up to 1MHz. They are offered in 8-pin SO packages and operate on 3V to 6V supplies. Power dissipation is only 10mW with a 3V supply or 50mW with a 5V supply. The LTC1198 automatically powers down to a typical supply current of 1nA whenever it is not performing conversions. These 8-bit switched-capacitor successive approximation ADCs include sample-and-holds. The LTC1196 has a differential analog input; the LTC1198 offers a software selectable 2-channel MUX.

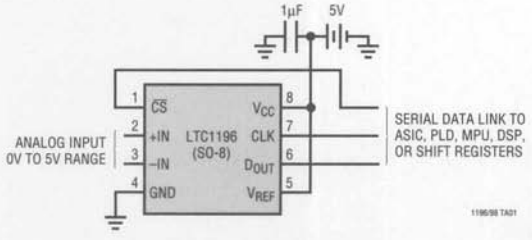
The 3-wire serial I/O, SO-8 packages, 3V operation and extremely high sample rate-to-power ratio make these ADCs an ideal choice for compact, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans below 1V full scale (LTC1196) allow direct connection to signal sources in many applications, eliminating the need for gain stages.

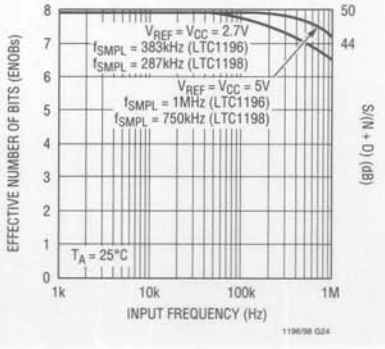
The A grade devices are specified with total unadjusted error of ±1/2LSB maximum over temperature.

TYPICAL APPLICATION

Single 5V Supply, 1MSPS, 8-Bit Sampling ADC



Effective Bits and S/(N + D) vs Input Frequency



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

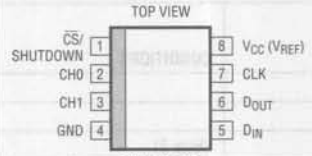
Supply Voltage (V_{CC}) to GND 7V
Voltage
  Analog Reference ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 7V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1196-1AC, LTC1198-1AC, LTC1196-1BC, LTC1198-1BC, LTC1196-2AC, LTC1198-2AC, LTC1196-2BC, LTC1198-2BC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER*
LTC1196-1ACS8 LTC1196-1BCS8 LTC1196-2ACS8 LTC1196-2BCS8
S8 PART MARKING
1961A 1961B 1962A 1962B



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER*
LTC1198-1ACS8 LTC1198-1BCS8 LTC1198-2ACS8 LTC1198-2BCS8
S8 PART MARKING
1981A 1981B 1982A 1982B

*Parts available in N8 package. Consult factory for N8 samples.
Consult factory for Industrial and Military grade parts.

6

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		6	2.7		6	V
V_{CC} = 5V Operation										
f_{CLK}	Clock Frequency			0.01		14.4	0.01		12.0	MHz
			●	0.01		12.0	0.01		9.6	MHz
t_{CYC}	Total Cycle Time	LTC1196		12			12			CLK
		LTC1198		16			16			CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ Low After Last CLK↑			10			13			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			20			26			ns
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		20			26			ns

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198	20			26			ns
t_{WHCLK}	CLK High Time	$f_{CLK} = f_{CLK(MAX)}$	40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK Low Time	$f_{CLK} = f_{CLK(MAX)}$	40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles		25			32			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1196 LTC1198	11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-XA LTC1198-XA MIN	TYP	MAX	LTC1196-XB LTC1198-XB MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 5.000V LTC1198, V_{CC} = 5.000V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196		−0.05V to V_{CC} + 0.05V						V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.5 2.4	4.74 4.71		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−25		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			45		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS}$ = V_{CC} f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.001 0.5	3 1	µA mA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}, LTC1198 (Shutdown) $\overline{CS}$ = V_{CC}, LTC1196 f_{SMPL} = $f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 7 11	3 15 20	µA mA mA

DYNAMIC ACCURACY

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	500kHz/1MHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	500kHz/1MHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	500kHz/1MHz Input Signal			55/48			55/48		dB
IMD	Intermodulation Distortion	f_{IN1} = 499.37kHz, f_{IN2} = 502.446kHz			51			51		dB
	Full Power Bandwidth				8			8		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB]				1			1		MHz

AC CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)					600			710	ns
			●			710			900	ns
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196		1.20			1.00			MHz
		LTC1196	●	1.00			0.80			MHz
		LTC1198		0.90			0.75			MHz
		LTC1198	●	0.75			0.60			MHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF			55	64		68	78	ns
			●			73			94	ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		70	120		88	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		30	50		43	63	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	30	45		30	55		ns
t_r	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		5	15		10	20	ns
t_f	D_{OUT} Rise Time	C_{LOAD} = 20pF	●		5	15		10	20	ns
C_{IN}	Input Capacitance	Analog Input On Channel			30			30		pF
		Analog Input Off Channel			5			5		pF
		Digital Input			5			5		pF

RECOMMENDED OPERATING CONDITIONS

V_{CC} = 2.7V Operation

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
f_{CLK}	Clock Frequency			0.01		5.4	0.01		4	MHz
			●	0.01		4.6	0.01		3	MHz
t_{CYC}	Total Cycle Time	LTC1196		12			12			CLK
		LTC1198		16			16			CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ Low After Last CLK↑			20			40			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			40			78			ns

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RECOMMENDED OPERATING CONDITIONS

V_{CC} = 2.7V Operation

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		40			78			ns
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198		40			78			ns
t_{WHCLK}	CLK High Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK Low Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles			50			96			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1196 LTC1198		11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-XA LTC1198-XA MIN	TYP	MAX	LTC1196-XB LTC1198-XB MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 2.500V LTC1198, V_{CC} = 2.700V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196			−0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.3 2.1	2.60 2.45		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			15		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS} = V_{CC}$ $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.25	3.0 0.5	µA mA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$ = 3.3V, LTC1198 (Shutdown) $\overline{CS} = V_{CC}$ = 3.3V, LTC1196 $f_{SMPL} = f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 1.5 2.0	3.0 4.5 6.0	µA mA mA

DYNAMIC ACCURACY

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	190kHz/380kHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	190kHz/380kHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	190kHz/380kHz Input Signal			53/46			53/46		dB
IMD	Intermodulation Distortion	f_{IN1} = 189.37kHz, f_{IN2} = 192.446kHz			51			51		dB
	Full Power Bandwidth				5			5		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB]				0.5			0.5		MHz

AC CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)					1.58			2.13	µs
			●			1.85			2.84	µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196		450			333			kHz
		LTC1196	●	383			250			kHz
		LTC1198		337			250			kHz
		LTC1198	●	287			187			kHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF			100	150		130	200	ns
			●			180			250	ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		110	220		120	250	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		80	130		100	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	45	90		45	120		ns
t_r	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		10	30		15	40	ns
t_f	D_{OUT} Rise Time	C_{LOAD} = 20pF	●		10	30		15	40	ns
C_{IN}	Input Capacitance	Analog Input On Channel			30			30		pF
		Analog Input Off Channel			5			5		pF
		Digital Input			5			5		pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

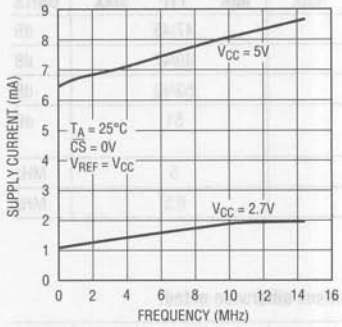
Note 4: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 5: Channel leakage current is measured after the channel selection.

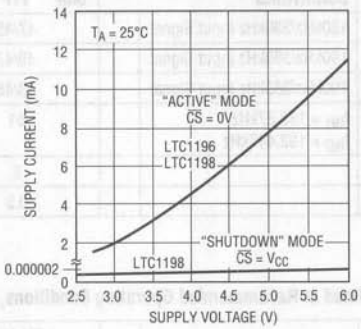
6

TYPICAL PERFORMANCE CHARACTERISTICS

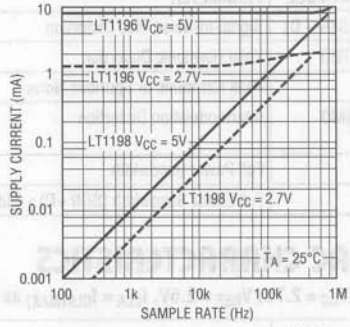
Supply Current vs Clock Rate



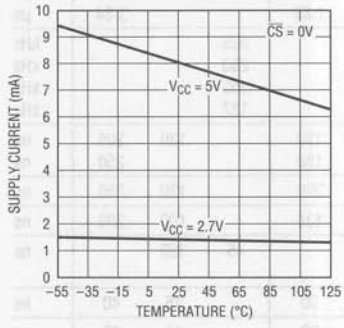
Supply Current vs Supply Voltage



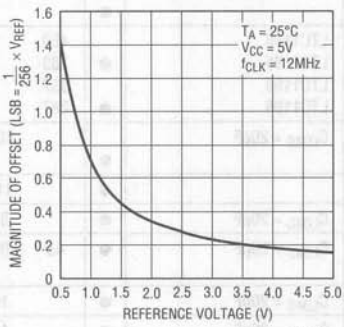
Supply Current vs Sample Rate



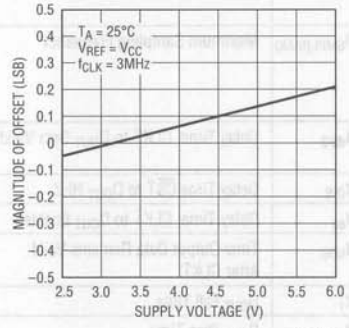
Supply Current vs Temperature



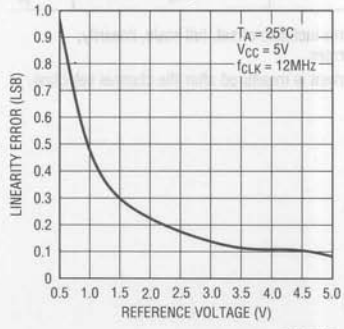
Offset vs Reference Voltage



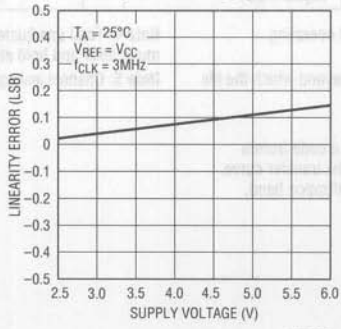
Offset vs Supply Voltage



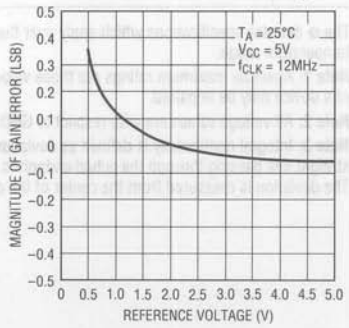
Linearity Error vs Reference Voltage



Linearity Error vs Supply Voltage

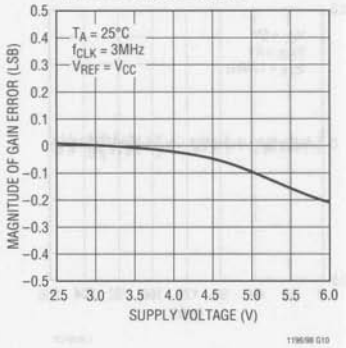


Gain Error vs Reference Voltage

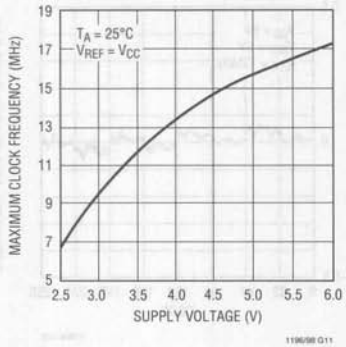


TYPICAL PERFORMANCE CHARACTERISTICS

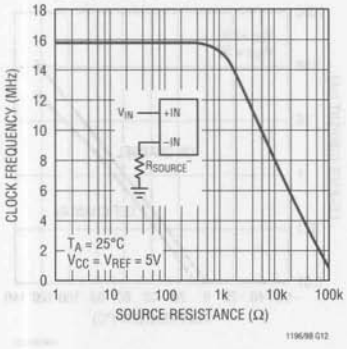
Gain vs Supply Voltage



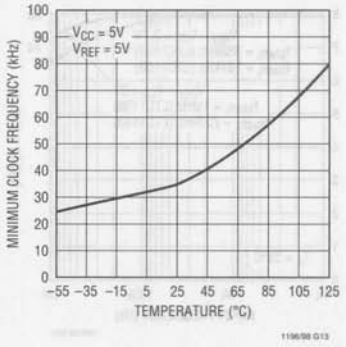
Maximum Clock Frequency vs Supply Voltage



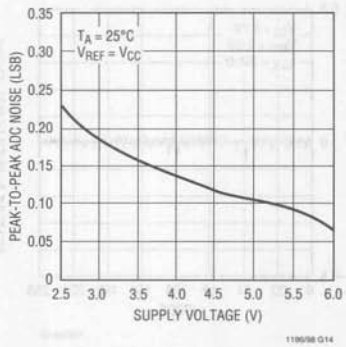
Maximum Clock Frequency vs Source Resistance



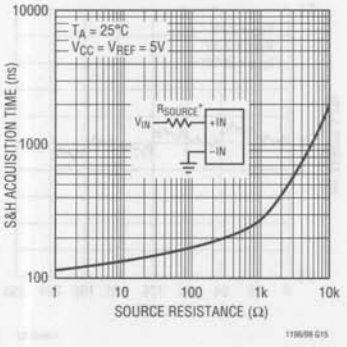
Minimum Clock Rate for 0.1LSB* Error



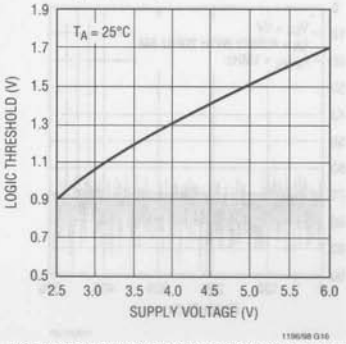
ADC Noise vs Reference and Supply Voltage



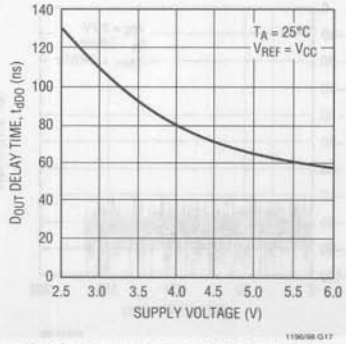
Sample-and-Hold Acquisition Time vs Source Resistance



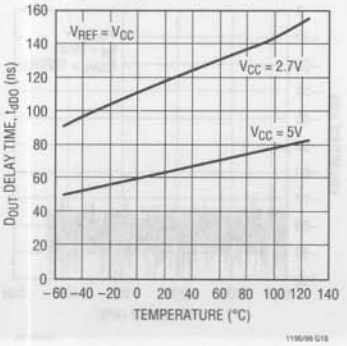
Digital Input Logic Threshold vs Supply Voltage



D_{OUT} Delay Time vs Supply Voltage



D_{OUT} Delay Time vs Temperature

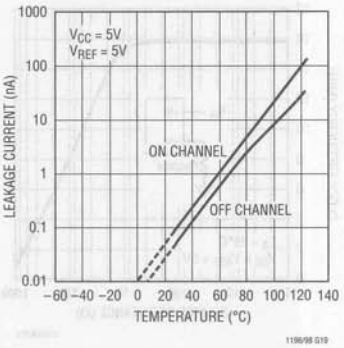


*AS THE FREQUENCY IS DECREASED FROM 12MHz, MINIMUM CLOCK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 12MHz VALUE IS FIRST DETECTED.

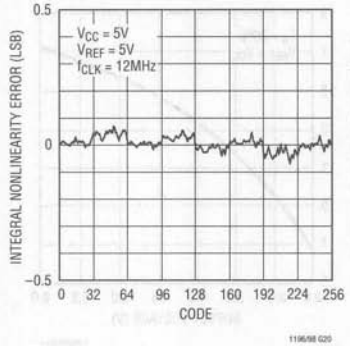
6

TYPICAL PERFORMANCE CHARACTERISTICS

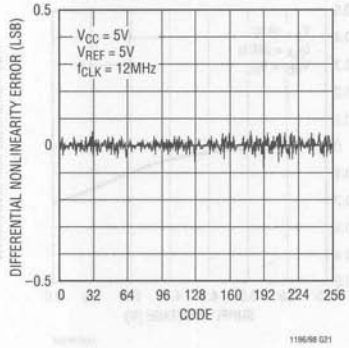
Input Channel Leakage Current vs Temperature



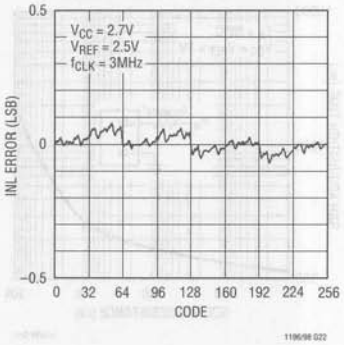
Integral Nonlinearity vs Code at 5V



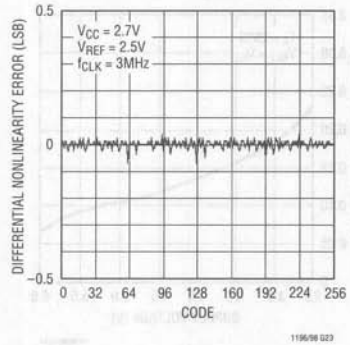
Differential Nonlinearity vs Code at 5V



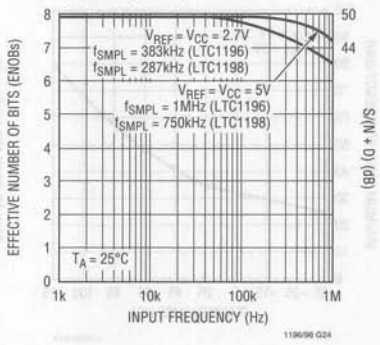
Integral Nonlinearity vs Code at 2.7V



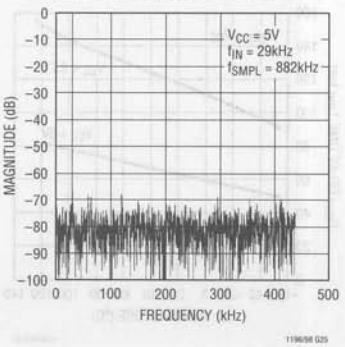
Differential Nonlinearity vs Code at 2.7V



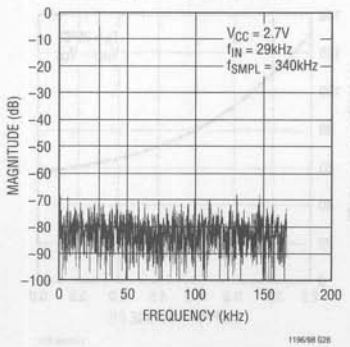
Effective Bits and S/(N + D) vs Input Frequency



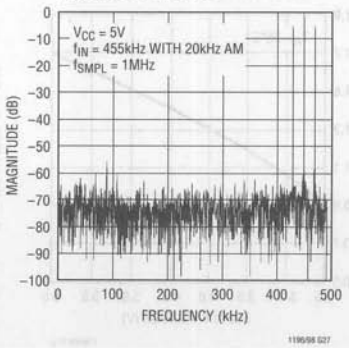
4096 Point FFT Plot at 5V



4096 Point FFT at 2.7V

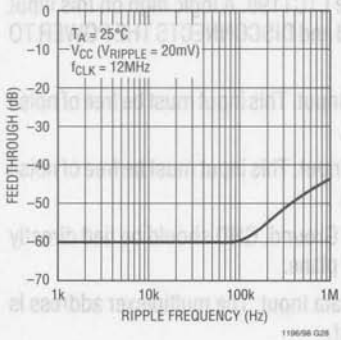


FFT Output of 455kHz AM Signal Digitized at 1MSPS

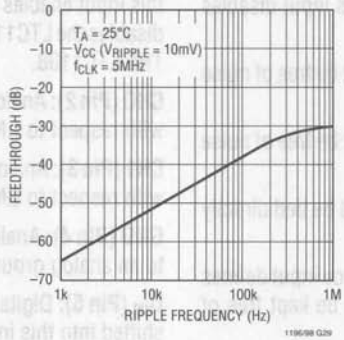


TYPICAL PERFORMANCE CHARACTERISTICS

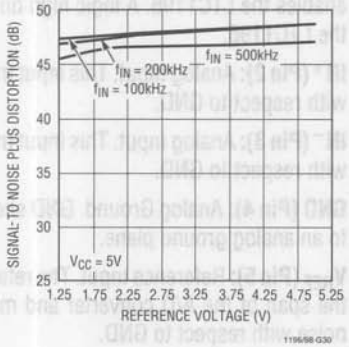
Power Supply Feedthrough vs Ripple Frequency



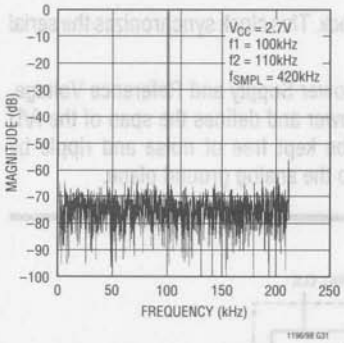
Power Supply Feedthrough vs Ripple Frequency



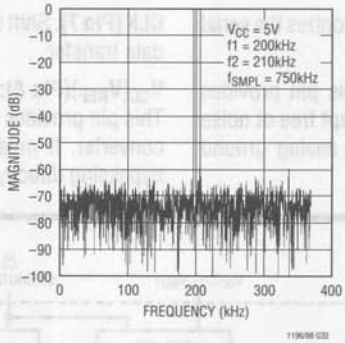
S/(N + D) vs Reference Voltage and Input Frequency



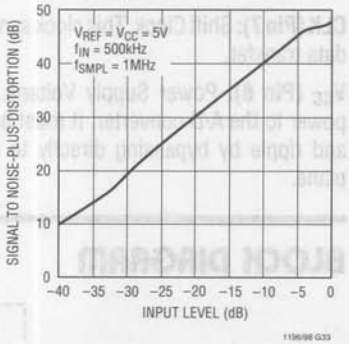
Intermodulation Distortion at 2.7V



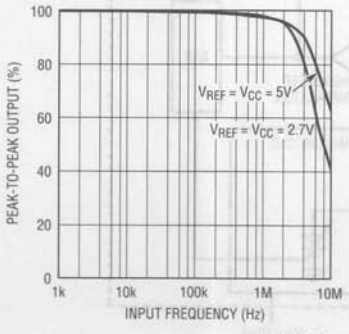
Intermodulation Distortion at 5V



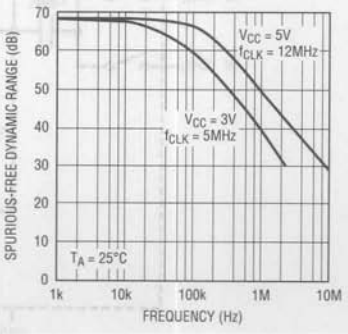
S/(N + D) vs Input Level



Output Amplitude vs Input Frequency



Spurious-Free Dynamic Range vs Frequency



6

PIN FUNCTIONS

LTC1196

$\overline{CS}$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1196. A logic high on this input disables the LTC1196.

IN⁺ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN⁻ (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1198

$\overline{CS}$/SHUTDOWN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1198. A logic high on this input disables the LTC1198 and DISCONNECTS THE POWER TO THE LTC1198.

CH0 (Pin 2): Analog Input. This input must be free of noise with respect to GND.

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

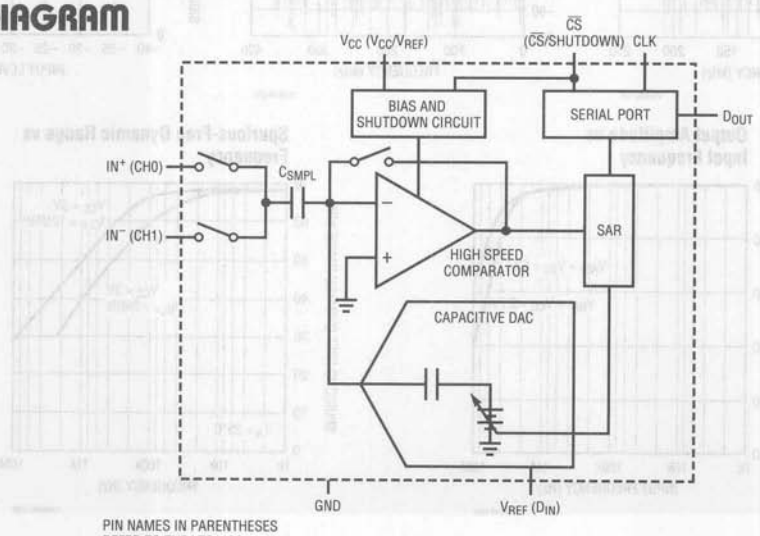
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

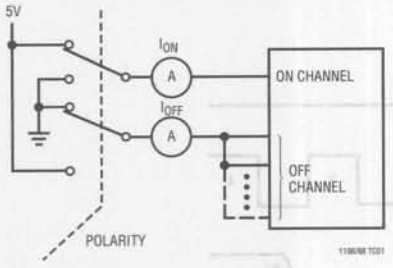
V_{CC}(V_{REF})(Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

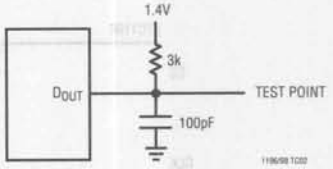


TEST CIRCUITS

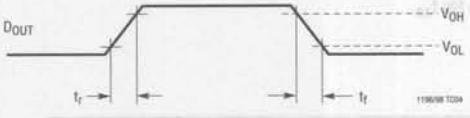
On and Off Channel Leakage Current



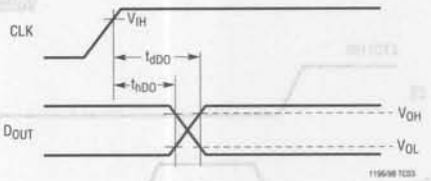
Load Circuit for t_{dDO}, t_r and t_f



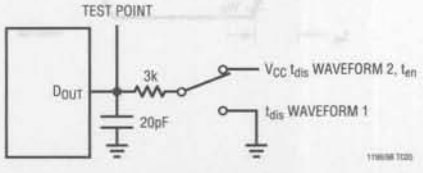
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



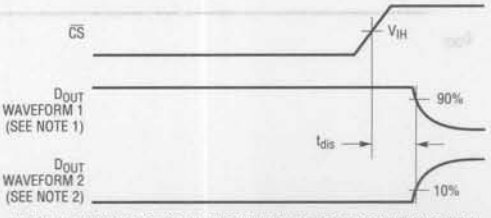
Voltage Waveform for D_{OUT} Delay Time, t_{dDO} and t_{hDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



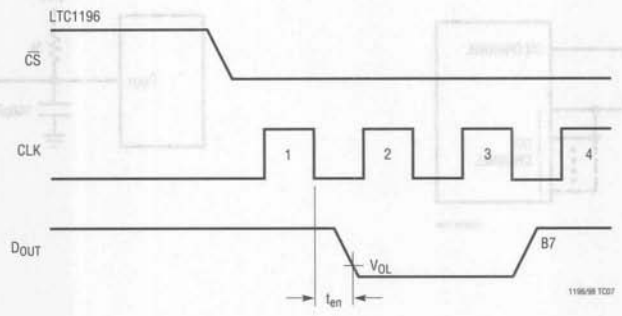
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

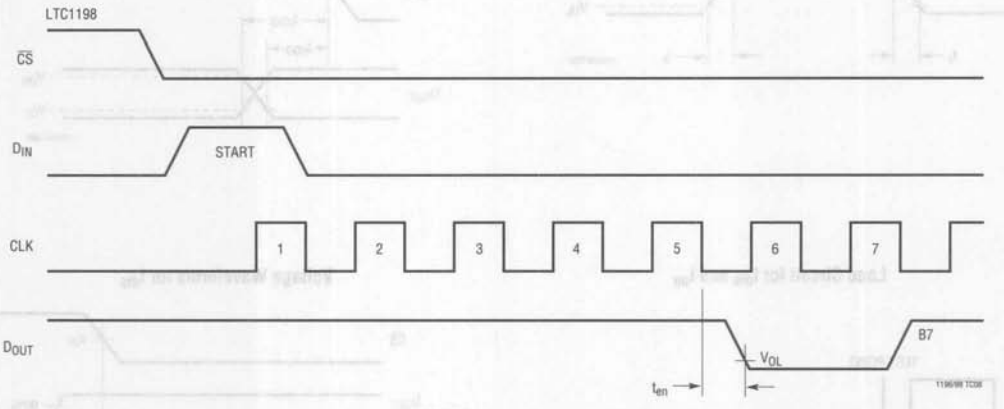
6

TEST CIRCUITS

Voltage Waveforms for t_{en}



Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

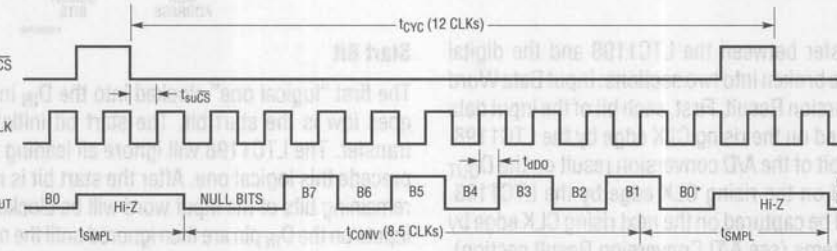
OVERVIEW

The LTC1196/LTC1198 are 600ns sampling 8-bit A/D converters packaged in tiny 8-pin SO packages and operating on 3V to 6V supplies. The ADCs draw only 10mW from a 3V supply or 50mW from a 5V supply.

Both the LTC1196 and the LTC1198 contain an 8-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). The on-chip sample-and-holds have full-accuracy input bandwidths of 1MHz. Although they share the same basic design, the LTC1196 and LTC1198 differ in some respects. The LTC1196 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans below 1V. The LTC1198 has a 2-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. It also automatically powers down when not performing conversion, drawing only leakage current.

SERIAL INTERFACE

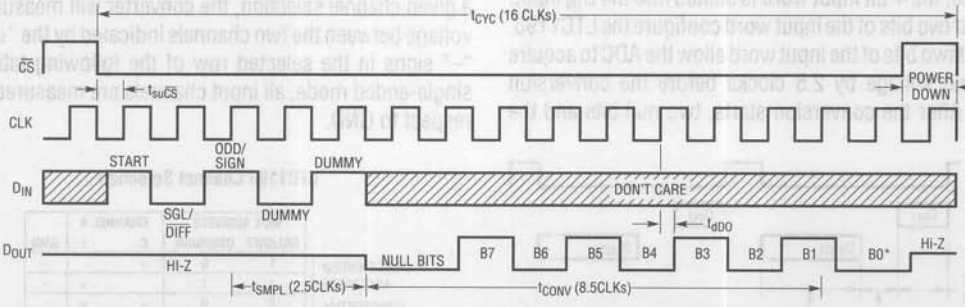
The LTC1196/LTC1198 will interface via three or four wires to ASICs, PLDs, microprocessors, DSPs, or shift registers (see Operating Sequence in Figures 1 and 2). To run at their fastest conversion rates (600ns), they must be clocked at 14.4MHz. HC logic families and any high speed ASIC or PLD will easily interface to the ADCs at that speed (see Data Transfer and Typical Application sections). Full speed operation from a 3V supply can still be achieved with 3V ASICs, PLDs or HC logic circuits.



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

1196/98 F01

Figure 1. LTC1196 Operating Sequence



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

1196/98 F02

Figure 2. LTC1198 Operating Sequence Example: Differential Inputs (CH1, CH0)

APPLICATIONS INFORMATION

Connection to a microprocessor or a DSP serial port is quite simple (see Data Transfer section). It requires no additional hardware, but the speed will be limited by the clock rate of the microprocessor or the DSP which limits the conversion time of the LTC1196/LTC1198.

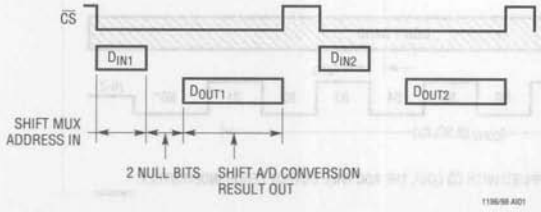
Data Transfer

Data transfer differs slightly between the LTC1196 and the LTC1198. The LTC1196 interfaces over 3 lines: $\overline{CS}$, CLK and D_{OUT}. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1196 Operating Sequence. After $\overline{CS}$ falls, the first CLK pulse enables D_{OUT}. After two null bits, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1196 for the next data exchange.

The LTC1198 can transfer data with 3 or 4 wires. The additional input, D_{IN}, is used to select the 2-channel MUX configuration.

The data transfer between the LTC1198 and the digital systems can be broken into two sections: Input Data Word and A/D Conversion Result. First, each bit of the input data word is captured on the rising CLK edge by the LTC1198. Second, each bit of the A/D conversion result on the D_{OUT} line is updated on the rising CLK edge by the LTC1198. This bit should be captured on the next rising CLK edge by the digital systems (see A/D Conversion Result section).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal as shown in the LTC1198 Operating Sequence. After $\overline{CS}$ falls the LTC1198 looks for a start bit. After the start bit is received, the 4-bit input word is shifted into the D_{IN} input. The first two bits of the input word configure the LTC1198. The last two bits of the input word allow the ADC to acquire the input voltage by 2.5 clocks before the conversion starts. After the conversion starts, two null bits and the conversion result are output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1198 in preparation for the next data exchange.



Input Data Word

The LTC1196 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result is output on the D_{OUT} line in an MSB-first sequence, followed by zeros indefinitely if clocks are continuously applied with $\overline{CS}$ low.

The LTC1198 clocks data into the D_{IN} input on the rising edge of the clock. The input data word is defined as follows:

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1198 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The 2 bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND.

LTC1198 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

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Dummy Bits

The last 2 bits of the input word following the MUX Address are dummy bits. Either bit can be a "logical one" or a "logical zero." These 2 bits allow the ADC 2.5 clocks to acquire the input signal after the channel selection.

A/D Conversion Result

Both the LTC1196 and the LTC1198 have the A/D conversion result appear on the D_{OUT} line after two null bits (see Operating Sequence in Figures 1 and 2). Data on the D_{OUT} line is updated on the rising edge of the CLK line. The D_{OUT} data should also be captured on the rising CLK edge by the digital systems. Data on the D_{OUT} line remains valid for a minimum time of t_{hDO} (30ns at 5V) to allow the capture to occur (see Figure 3).

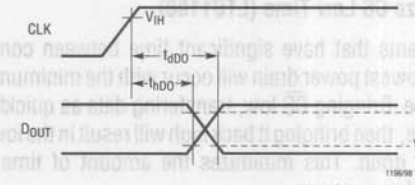
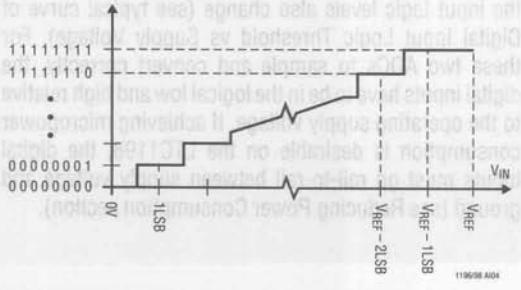


Figure 3. Voltage Waveform for D_{OUT} Delay Time, t_{dDO} and t_{hDO}

Unipolar Transfer Curve

The LTC1196/LTC1198 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Unipolar Transfer Curve



Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111	V_{REF} – 1LSB	4.9805V
11111110	V_{REF} – 2LSB	4.9609V
•	•	•
•	•	•
•	•	•
00000001	1LSB	0.0195V
00000000	0V	0V

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Operation with D_{IN} and D_{OUT} Tied Together

The LTC1198 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the digital systems. Data is transmitted in both directions on a single wire. The pin of the digital systems connected to this data line should be configurable as either an input or an output. The LTC1198 will take control of the data line and drive it low on the 5th falling CLK edge after the start bit is received (see Figure 4). Therefore the port line of the digital systems must be switched to an input before this happens to avoid a conflict.

REDUCING POWER CONSUMPTION

The LTC1196/LTC1198 can sample at up to a 1MHz rate, drawing only 50mW from a 5V supply. Power consumption can be reduced in two ways. Using a 3V supply lowers the power consumption on both devices by a factor of five, to 10mW. The LTC1198 can reduce power even further because it shuts down whenever it is not converting. Figure 5 shows the supply current versus sample rate for the LTC1196 and LTC1198 on 3V and 5V. To achieve such a low power consumption, especially for the LTC1198, several things must be taken into consideration.

Shutdown (LTC1198)

Figure 2 shows the operating sequence of the LTC1198. The converter draws power when the $\overline{CS}$ pin is low and powers itself down when that pin is high. For lowest power consumption in shutdown, the $\overline{CS}$ pin should be driven with CMOS levels (0V to V_{CC}) so that the $\overline{CS}$ input buffer of the converter will not draw current.

6

APPLICATIONS INFORMATION

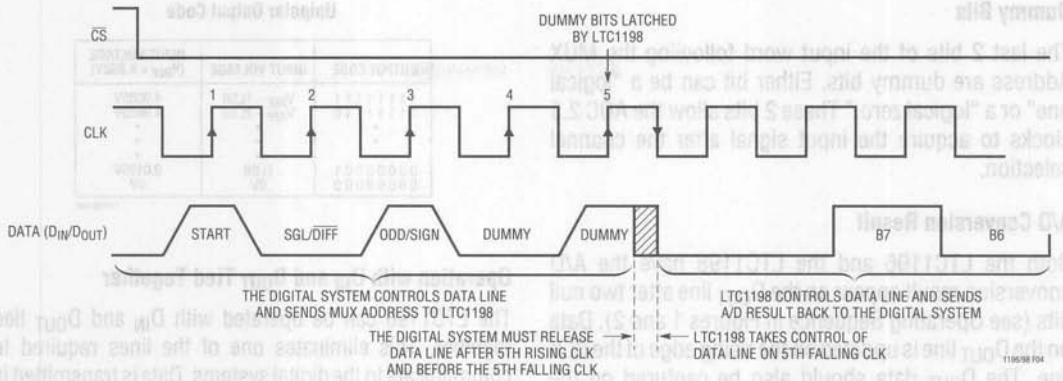

Figure 4. LTC1198 Operation with D_{IN} and D_{OUT} Tied Together

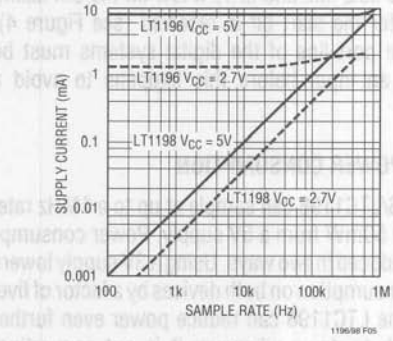

Figure 5. Supply Current vs Sample Rate for LTC1196/ LTC1198 Operating on 5V and 2.7V Supplies

When the $\overline{CS}$ pin is high (= supply voltage), the LTC1198 is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input has no effect on the supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

Minimize $\overline{CS}$ Low Time (LTC1198)

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transfering data as quickly as possible, then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power.

OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1196/LTC1198 operate from single 2.7V to 6V supplies. To operate the LTC1196/LTC1198 on other than 5V supplies, a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on 5V supply. When the supply voltage varies, the input logic levels also change (see typical curve of Digital Input Logic Threshold vs Supply Voltage). For these two ADCs to sample and convert correctly, the digital inputs have to be in the logical low and high relative to the operating supply voltage. If achieving micropower consumption is desirable on the LTC1198, the digital inputs must go rail-to-rail between supply voltage and ground (see Reducing Power Consumption section).

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Clock Frequency

The maximum recommended clock frequency is 14.4MHz at 25°C for the LTC1196/LTC1198 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the supply is reduced, the clock rate must be reduced also. At 3V the devices are specified with a 5.4MHz clock at 25°C.

Mixed Supplies

It is possible to have a digital system running off a 5V supply and communicate with the LTC1196/LTC1198 operating on a 3V supply. Achieving this reduces the outputs of D_{OUT} from the ADCs to toggle the equivalent input of the digital system. The $\overline{CS}$, CLK and D_{IN} inputs of the ADCs will take 5V signals from the digital system without causing any problem (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1196 operating on a 3V supply, the output of D_{OUT} only goes between 0V and 3V. This signal easily meets TTL levels (see Figure 6).

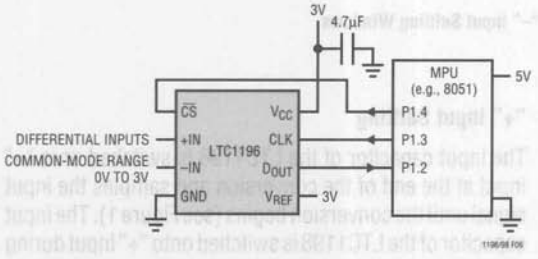

Figure 6. Interfacing a 3V Powered LTC1196 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1196/LTC1198 are easy to use if some care is taken. They should be used with an analog ground plane and single-point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 1µF tantalum with leads as short as possible. If the power supply is clean, the LTC1196/LTC1198 can also operate with smaller 0.1µF surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single-point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1196 and the LTC1198 provide a built-in sample-and-hold (S&H) function to acquire the input signal. The S&H acquires the input signal from "+" input during t_{SMPL} as shown in Figures 1 and 2. The S&H of the LTC1198 can sample input signals in either single-ended or differential mode (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1198 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the first DUMMY bit is shifted in and continues until the falling CLK edge after the second DUMMY bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 8.5 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input, this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 8.5/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the

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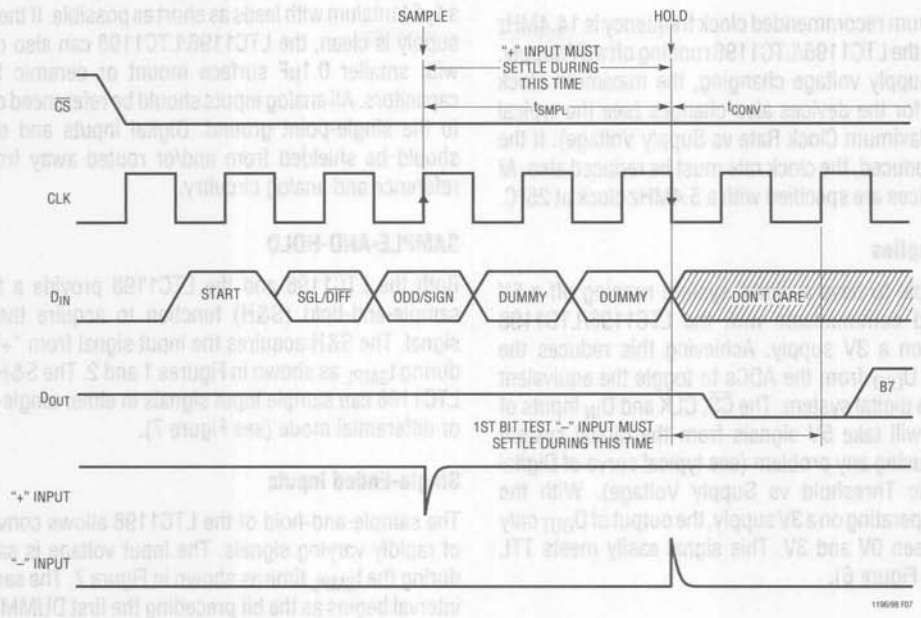

Figure 7. LTC1198 "+" and "–" Input Settling Windows

CLK. V_{ERROR} is proportional to f("–") and inversely proportional to f_{CLK}. For a 60Hz signal on the "–" input to generate a 1/4LSB error (5mV) with the converter running at CLK = 12MHz, its peak value would have to be 18.7V.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1196/LTC1198 have one capacitive switching input current spike per conversion. These current spikes settle quickly and do not cause a problem. However, if source resistances larger than 100Ω are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1196 is switched onto "+" input at the end of the conversion and samples the input signal until the conversion begins (see Figure 1). The input capacitor of the LTC1198 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 2.5 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPL} for the LTC1196/LTC1198. Minimizing R_{SOURCE}^+ will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by allowing more time between conversions for the LTC1196 or by using a slower CLK frequency for the LTC1198.

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"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figures 1 and 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps.

To achieve the full sampling rate, the analog input should be driven with a low impedance source (<100Ω) or a high speed op amp (e.g., the LT1223, LT1191, or LT1226). Higher impedance sources or slower op amps can easily be accommodated by allowing more time for the analog input to settle as described above.

Source Resistance

The analog inputs of the LTC1196/LTC1198 look like a 25pF capacitor (C_{IN}) in series with a 120Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within t_{SMPL}.

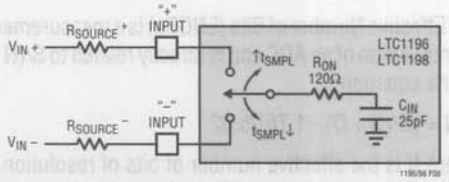

Figure 8. Analog Input Equivalent Circuit

REFERENCE INPUT

The voltage on the reference input of the LTC1196 defines the voltage span of the A/D converter. The reference input has transient capacitive switching currents which are due to the switched-capacitor conversion technique (see Figure 9). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These high frequency current spikes will settle quickly and do not cause a problem if the reference input is bypassed with at least a 0.1µF capacitor.

The reference input can be driven with standard voltage references. Bypassing the reference with a 0.1µF capacitor is recommended to keep the high frequency impedance low as described above. Some references require a small resistor in series with the bypass capacitor for frequency stability. See the individual reference data sheet for details.

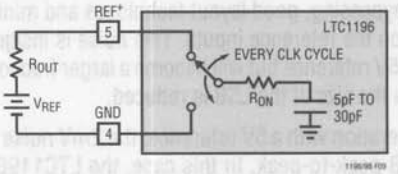

Figure 9. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1198 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1196 can operate with reference voltages below 1V.

The effective resolution of the LTC1196 can be increased by reducing the input span of the converter. The LTC1196 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full-Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise

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Offset with Reduced V_{REF}

The offset of the LTC1196 has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 2mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSB with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1196.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1196 can be reduced to approximately $2mV_{P-P}$ using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 2mV noise is only 0.1LSB peak-to-peak. In this case, the LTC1196 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 2mV noise is 0.5LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 200mV, the 2mV noise becomes equal to 2.5LSB and a stable code is difficult to achieve. In this case averaging readings is necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

DYNAMIC PERFORMANCE

The LTC1196/LTC1198 have exceptionally high speed sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using a FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 10 shows a typical LTC1196 FFT plot.

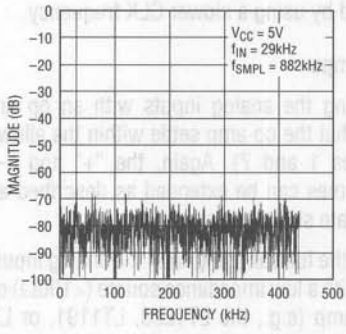

Figure 10. LTC1196 Non-Averaged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 10 shows a typical spectral content with a 882kHz sampling rate.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling

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rate of 1.2MHz with a 5V supply the LTC1196 maintains above 7.5 ENOBs at 400kHz input frequency. Above 500kHz the ENOBs gradually decline, as shown in Figure 11, due to increasing second harmonic distortion. The noise floor remains low.

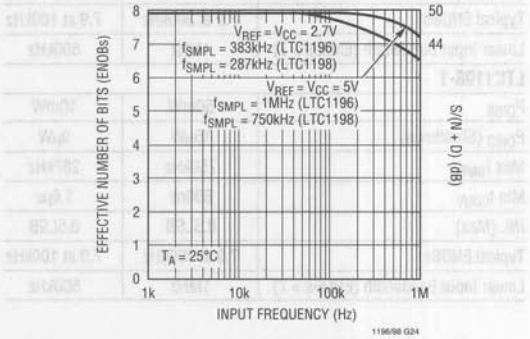

Figure 11. Effective Bits and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the Nth harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 100kHz input signal, the LTC1196/LTC1198 have typical THD of 50dB and 49dB with V_{CC} = 5V and V_{CC} = 3V, respectively.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20\log\left[\frac{\text{amplitude}\,(f_a \pm f_b)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 499kHz and 502kHz, the IMD of the LTC1196/LTC1198 is 51dB with a 5V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 7 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1196/LTC1198 have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency.

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3V VERSUS 5V PERFORMANCE COMPARISON

Table 1 shows the performance comparison between 3V and 5V supplies. The power dissipation drops by a factor of five when the supply is reduced to 3V. The converter slows down somewhat but still gives excellent performance on a 3V rail. With a 3V supply, the LTC1196 converts in 1.6µs, samples at 450kHz, and provides a 500kHz linear-input bandwidth.

Dynamic accuracy is excellent on both 5V and 3V. The ADCs typically provide 49.3dB of 7.9 ENOBs of dynamic accuracy at both 3V and 5V. The noise floor is extremely low, corresponding to a transition noise of less than 0.1LSB. DC accuracy includes ±0.5LSB total unadjusted error at 5V. At 3V, linearity error is ±0.5LSB while total unadjusted error increases to ±1LSB.

Table 1. 5V/3V Performance Comparison

LTC1196-1	5V	3V
P_{DISS}	50mW	10mW
Max f_{SMPL}	1MHz	383kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz
LTC1198-1		
P_{DISS}	50mW	10mW
P_{DISS} (Shutdown)	15µW	9µW
Max f_{SMPL}	750kHz	287kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz

TYPICAL APPLICATIONS

PLD Interface Using the Altera EPM5064

The Altera EPM5064 has been chosen to demonstrate the interface between the LTC1196 and a PLD. The EPM5064 is programmed to be a 12-bit counter and an equivalent 74HC595 8-bit shift register as shown in Figure 12. The circuit works as follows: bringing ENA high makes the $\overline{CS}$ output high and the EN input low to reset the LTC1196 and disable the shift register. Bringing ENA low, the $\overline{CS}$ output goes high for one CLK cycle with every 12 CLK cycles. The inverted signal, EN, of the $\overline{CS}$ output makes the 8-bit data available on the B0-B7] lines. Figures 13 and 14 show the interconnection between the LTC1196 and EPM5064 and the timing diagram of the signals between these two devices. The CLK frequency in this circuit can run up to $f_{CLK(MAX)}$ of the LTC1196.

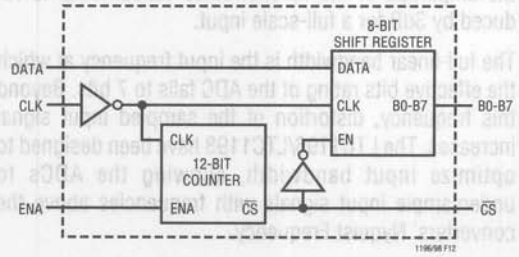


Figure 12. An Equivalent Circuit of the EPM5064

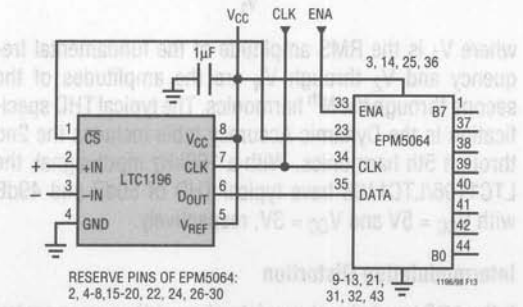


Figure 13. Intefacing the LTC1196 to the Altera EPM5064 PLD

TYPICAL APPLICATIONS

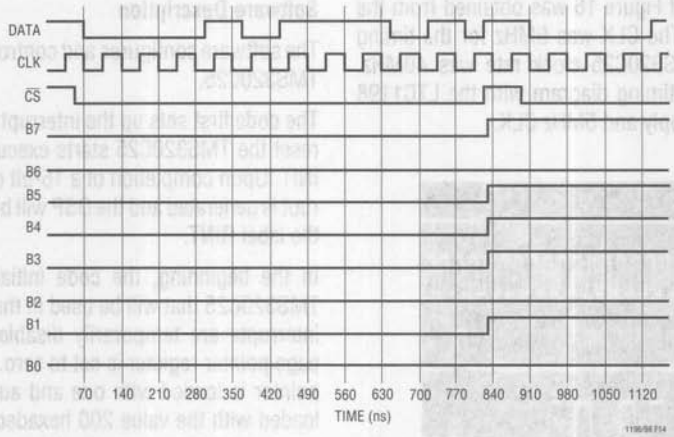


Figure 14. The Timing Diagram

Interfacing the LTC1198 to the TMS320C25 DSP

Figure 15 illustrates the interface between the LTC1198 8-bit data acquisition system and the TMS320C25 digital signal processor (DSP). The interface, which is optimized for speed of transfer and minimum processor supervision, can complete a conversion and shift the data in 4µs with f_{CLK} = 5MHz. The cycle time, 4µs, of each conversion is limited by maximum clock frequency of the serial port of the TMS320C25 which is 5MHz. The supply voltage for the LTC1198 in Figure 15 can be 2.7V to 6V with f_{CLK} = 5MHz. At 2.7V, f_{CLK} = 5MHz will work at 25°C. See Recommended Operating Conditions for limits over temperature.

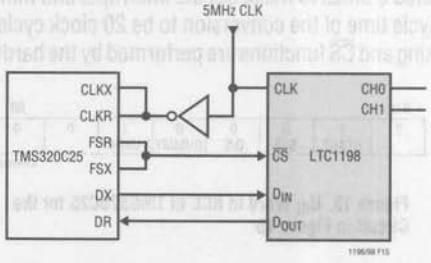


Figure 15. Interfacing the LTC1198 to the TMS320C25 DSP

Hardware Description

The circuit works as follows: the LTC1198 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous format over D_{IN} and D_{OUT}. The serial port of the TMS320C25 is compatible with that of the LTC1198. The data shift clock lines (CLKR, CLKX) are inputs only. The data shift clock comes from an external source. Inverting the shift clock is necessary because the LTC1198 and the TMS320C25 clock the input data on opposite edges.

The schematic of Figure 15 is fed by an external clock source. The signal is fed into the CLK pin of the LTC1198 directly. The signal is inverted with a 74HC04 and then applied to the data shift clock lines (CLKR, CLKX). The framing pulse of the TMS320C25 is fed directly to the $\overline{CS}$ of the LTC1198. DX and DR are tied directly to D_{IN} and D_{OUT} respectively.

TYPICAL APPLICATIONS

The timing diagram of Figure 16 was obtained from the circuit of Figure 15. The CLK was 5MHz for the timing diagram and the TMS320C25 clock rate was 40MHz. Figure 17 shows the timing diagram with the LTC1198 running off a 2.7V supply and 5MHz CLK.

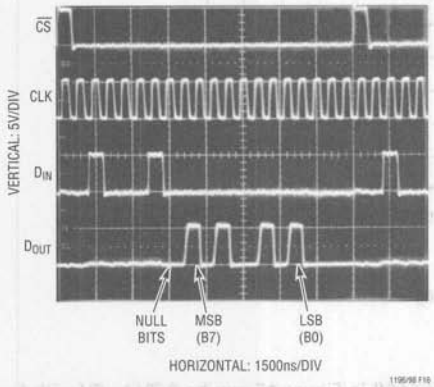


Figure 16. Scope Trace the LTC1198 Running Off 5V Supply in the Circuit of Figure 15

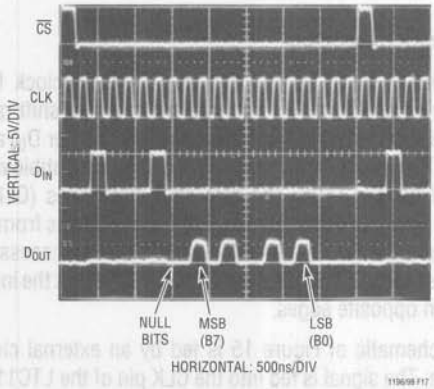


Figure 17. Scope Trace the LTC1198 Running Off 2.7V Supply in the Circuit of Figure 15

Software Description

The software configures and controls the serial port of the TMS320C25.

The code first sets up the interrupt and reset vectors. On reset the TMS320C25 starts executing code at the label INIT. Upon completion of a 16-bit data transfer, an interrupt is generated and the DSP will begin executing code at the label RINT.

In the beginning, the code initializes registers in the TMS320C25 that will be used in the transfer routine. The interrupts are temporarily disabled. The data memory page pointer register is set to zero. The auxiliary register pointer is loaded with one and auxiliary register one is loaded with the value 200 hexadecimal. This is the data memory location where the data from the LTC1198 will be stored. The interrupt mask register (IMR) is configured to recognize the RINT interrupt, which is generated after receiving the last of 16 bits on the serial port. This interrupt is still disabled at this time. The transmit framing synchronization pin (FSX) is configured to be an output. The F0 bit of the status register ST1, is initialized to zero which sets up the serial port to operate in the 16-bit mode.

Next, the code in TXRX routine starts to transmit and receive data. The D_{IN} word is loaded into the ACC and shifted left eight times so that it appears as in Figure 18. This D_{IN} word configures the LTC1198 for CH0 with respect to CH1. The D_{IN} word is then put in the transmit register and the RINT interrupt is enabled. The NOP is repeated 3 times to mask out the interrupts and minimize the cycle time of the conversion to be 20 clock cycles. All clocking and $\overline{CS}$ functions are performed by the hardware.

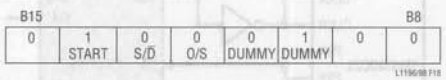


Figure 18. D_{IN} Word in ACC of TMS320C25 for the Circuit in Figure 15

TYPICAL APPLICATIONS

Once RINT is generated the code begins execution at the label RINT. This code stores the D_{OUT} word from the LTC1198 in the ACC and then stores it in location 200 hex. The data appears in location 200 hex right-justified as shown in Figure 19. The code is set up to continually loop, so at this point the code jumps to label TXRX and repeats from here.

Figure 19. Memory Map for the Circuit in Figure 15

LABEL	MNEMONIC		COMMENTS
	AORG	0	ON RESET CODE EXECUTION STARTS AT 0
	B	INIT	BRANCH TO INITIALIZATION ROUTINE
	AORG	>26	ADDRESS OF RINT INTERRUPT VECTOR
	B	RINT	BRANCH TO RINT SERVICE ROUTINE
	AORG	>32	MAIN PROGRAM STARTS HERE
INIT	DINT		DISABLE INTERRUPTS
	LDPK	>0	SET DATA MEMORY PAGE POINTER TO 0
	LARP	>1	SET AUXILIARY REGISTER POINTER TO 1
	LRLK	AR1,>200	SET AUXILIARY REGISTER 1 TO >200
	LACK	>10	LOAD IMR CONFIG WORD INTO ACC
	SACL	>4	STORE IMR CONFIG WORD INTO IMR
	STXM		CONFIGURE FSX AS AN OUTPUT
	FORT	0	SET SERIAL PORT TO 16-BIT MODE
TXRX	LACK	>44	LOAD LTC1198 D_{IN} WORD INTO ACC
	SFSM		FSX PULSES GENERATED ON XSR LOAD
	RPTK	7	REPEAT NEXT INSTRUCTION 8 TIMES
	SFL		SHIFTS D_{IN} WORD TO RIGHT POSITION
	SACL	>1	PUT D_{IN} WORD IN TRANSMIT REGISTER
	EINT		ENABLE INTERRUPT (DISABLED ON RINT)
	RPTK	2	MINIMIZE THE CONVERSION CYCLE TIME
	NOP		TO BE 20 CLOCK CYCLES
RINT	ZALS	>0	STORE LTC1198 DOUT WORD IN ACC
	SACL	*, 0	STORE ACC IN LOCATION >200
	B	TXRX	BRANCH TO TRANSMIT RECEIVE ROUTINE
	END		

Figure 20. TMS320C25 Code for the Circuit in Figure 15

12-Bit, 300ksps Sampling A/D Converters with Reference

FEATURES

- Single Supply 5V or ±5V Operation
- 300ksps Sample Rate
- 75mW (Typ) Power Dissipation
- On-Chip 25ppm/°C Reference
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- 70dB S/(N + D) and 77dB THD at Nyquist
- ±1/2LSB INL and ±3/4LSB DNL Max (A Grade)
- ESD Protected On All Pins
- 24-Pin Narrow DIP and SOL Packages
- Variety of Input Ranges:
  0V to 5V (LTC1273)
  ±2.5V (LTC1275)
  ±5V (LTC1276)

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC1273/LTC1275/LTC1276 are 300ksps, sampling 12-bit A/D converters that draw only 75mW from single 5V or ±5V supplies. These easy-to-use devices come complete with 600ns sample-and-holds, precision references and internally trimmed clocks. Unipolar and bipolar conversion modes provide flexibility for various applications. They are built with LTBiCMOS™ switched capacitor technology.

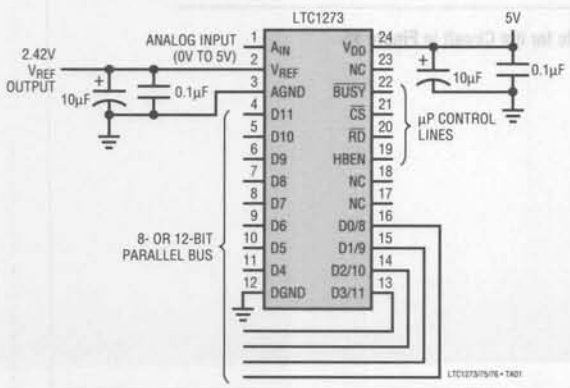
These devices have 25ppm/°C (max) internal references. The LTC1273 converts 0V to 5V unipolar inputs from a single 5V supply. The LTC1275/LTC1276 convert ±2.5V and ±5V respectively from ±5V supplies. Maximum DC specifications include ±1/2LSB INL, ±3/4LSB DNL and 25ppm/°C full scale drift over temperature. Outstanding AC performance includes 70dB S/(N + D) and 77dB THD at the Nyquist input frequency of 150kHz.

The internal clock is trimmed for 2.7µs maximum conversion time. The clock automatically synchronizes to each sample command eliminating problems with asynchronous clock noise found in competitive devices. A high speed parallel interface eases connections to FIFOs, DSPs and microprocessors.

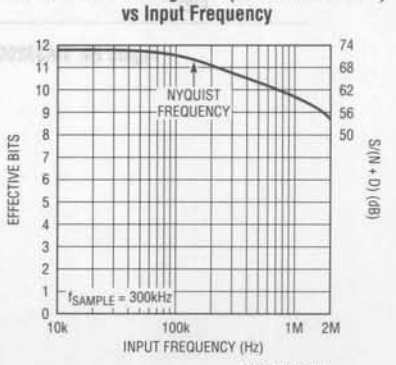
LTBiCMOS™ is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Single 5V Supply, 300ksps, 12-Bit Sampling A/D Converter



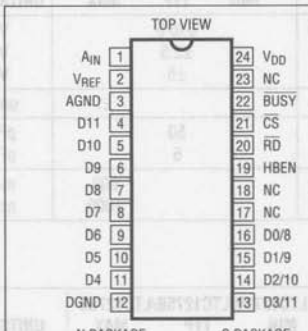
Effective Bits and Signal to (Noise + Distortion) vs Input Frequency



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{DD}) 12V
Negative Supply Voltage (V_{SS})
LTC1275/LTC1276 ..... −6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
LTC1275/LTC1276 ..... 12V
Analog Input Voltage (Note 3)
LTC1273 ..... −0.3V to V_{DD} + 0.3V
LTC1275/LTC1276 ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
LTC1273 ..... −0.3V to 12V
LTC1275/LTC1276 ..... V_{SS} − 0.3V to 12V
Digital Output Voltage (Note 3)
LTC1273 ..... −0.3V to V_{DD} + 0.3V
LTC1275/LTC1276 ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1273AC, LTC1273BC, LTC1275AC
LTC1275BC, LTC1276AC, LTC1276BC .... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

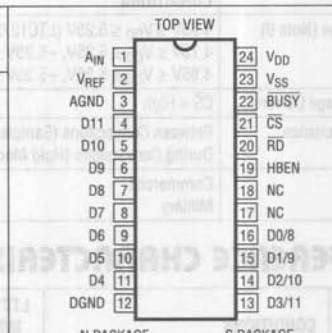
PACKAGE/ORDER INFORMATION



N PACKAGE 24-LEAD PLASTIC DIP
S PACKAGE 24-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (S)

ORDER PART NUMBER
LTC1273ACN
LTC1273BCN
LTC1273ACS
LTC1273BCS



N PACKAGE 24-LEAD PLASTIC DIP
S PACKAGE 24-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (S)

ORDER PART NUMBER
LTC1275ACN
LTC1275BCN
LTC1275ACS
LTC1275BCS
LTC1276ACN
LTC1276BCN
LTC1276ACS
LTC1276BCS

Consult factory for Industrial and Military grade parts.

CONVERTER CHARACTERISTICS With Internal Reference (Notes 5 and 6)

PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A MIN	TYP	MAX	LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7)				±1/2			±1	LSB
	Commercial	●			±1/2			±1	LSB
	Military	●			±3/4			±1	LSB
Differential Linearity Error	Commercial	●			±3/4			±1	LSB
	Military	●			±1			±1	LSB
Offset Error	(Note 8)				±3			±4	LSB
		●			±4			±6	LSB
Gain Error					±10			±15	LSB
Gain Error Tempco	$I_{OUT(REFERENCE)}$ = 0	●		±5	±25		±10	±45	ppm/°C

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz/150kHz Input Signal		72/70		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz/150kHz Input Signal		–83/–74		dB
	Peak Harmonic or Spurious Noise	50kHz/150kHz Input Signal		–85/–76		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz		–80		dB
	Full Power Bandwidth			4.5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)			200		kHz

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.95V ≤ V_{DD} ≤ 5.25V (LTC1273)	●		0 to 5		V
		4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (LTC1275)	●		±2.5		V
		4.95V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.95V (LTC1276)	●		±5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			50		pF
		During Conversions (Hold Mode)			5		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Commercial	●			600	ns
		Military	●			1000	ns

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A MIN	TYP	MAX	LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±5	±25		±10	±45	ppm/°C
V_{REF} Line Regulation	4.95V ≤ V_{DD} ≤ 5.25V			0.01			0.01		LSB/V
	–5.25V ≤ V_{SS} ≤ –4.95V			0.01			0.01		LSB/V
V_{REF} Load Regulation	0V ≤ $\|I_{OUT}\|$ ≤ 1mA			2			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.95V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.95V					
		I_O = –10µA			4.7		V
		I_O = –200µA	●	4.0			V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	V_{DD} = 4.95V					
		I_O = 160µA			0.05		V
		I_O = 1.6mA	●		0.10	0.4	V
I_{OZ}	High Z Output Leakage D11-D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High Z Output Capacitance D11-D0/8	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	LTC1273/LTC1276 (Notes 10, 11)		4.95		5.25	V
		LTC1275 (Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	LTC1275 (Note 10)		−2.45		−5.25	V
		LTC1276 (Notes 10, 11)		−4.95		−5.25	V
I_{DD}	Positive Supply Current		●		15	25	mA
I_{SS}	Negative Supply Current	LTC1275/LTC1276	●		0.065	0.200	mA
P_D	Power Dissipation				75		mW

TIMING CHARACTERISTICS See Timing Characteristics Figures (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 10)					
		Commercial	●	300			kHz
		Military	●	250			kHz
t_{CONV}	Conversion Time	Commercial	●			2.7	µs
		Military	●			3.0	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time		●	0			ns
t_2	$\overline{RD}$ to $\overline{BUSY}$ Delay	C_L = 50pF			80	190	ns
		Commercial	●			230	ns
		Military	●			270	ns
t_3	Data Access Time After $\overline{RD}$↓	C_L = 20pF			40	90	ns
		Commercial	●			110	ns
		Military	●			120	ns
		C_L = 100pF			50	125	ns
		Commercial	●			150	ns
		Military	●			170	ns
t_4	$\overline{RD}$ Pulse Width		●	t_3			ns
t_5	$\overline{CS}$ to $\overline{RD}$ Hold Time		●	0			ns
t_6	Data Setup Time After $\overline{BUSY}$↑				40	70	ns
		Commercial	●			90	ns
		Military	●			100	ns

6

TIMING CHARACTERISTICS See Timing Characteristics Figures (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
t_7	Bus Relinquish Time			20	30	75	ns
		Commercial	●	20		85	ns
		Military	●	20		90	ns
t_8	HBEN to $\overline{RD}$ Setup Time		●	0			ns
t_9	HBEN to $\overline{RD}$ Hold Time		●	0			ns
t_{10}	Delay Between $\overline{RD}$ Operations		●	40			ns
t_{11}	Delay Between Conversions	(Note 10)		500			ns
		Commercial	●	600			ns
		Military	●	1000			ns
t_{12}	Aperture Delay of Sample-and-Hold				25		ns

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for LTC1273) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for LTC1273) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for LTC1273) they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for LTC1273) without latch-up. These pins are not clamped to V_{DD}.

Note 5: $V_{DD} = 5V$ ($V_{SS} = -5V$ for LTC1275/LTC1276), 300kHz at 70°C and 250kHz at 125°C, $t_r = t_f = 5ns$ unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset (LTC1275/LTC1276) is the different voltage measured from –0.5LSB when the LTC1275/LTC1276 output code flickers between 0000 0000 0000 and 1111 1111 1111.

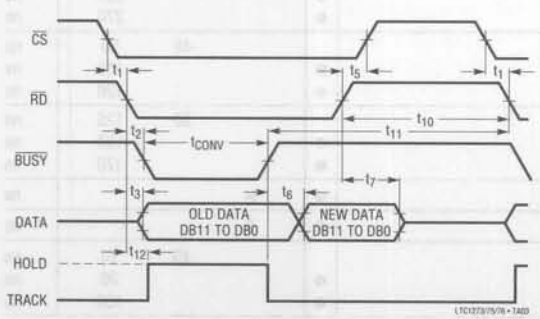
Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

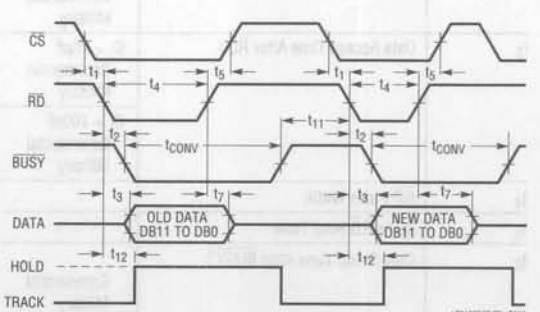
Note11: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy. Therefore the minimum supply voltage for the LTC1273 is +4.95V. The minimum supplies for the LTC1275 are +4.75V and –2.45V and the minimum supplies for the LTC1276 are ±4.95V.

TIMING CHARACTERISTICS (Note 5)

Slow Memory Mode, Parallel Read Timing Diagram

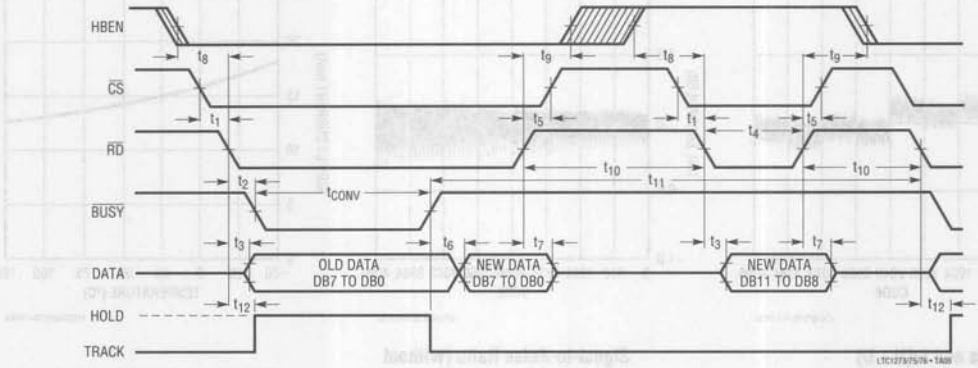


ROM Mode, Parallel Read Timing Diagram

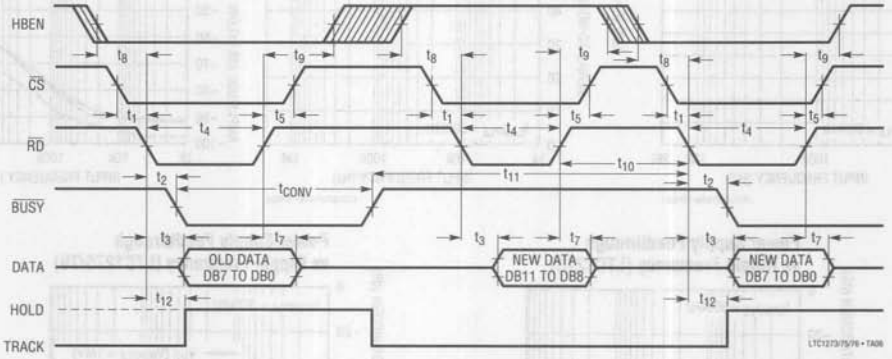


TIMING CHARACTERISTICS (Note 5)

Slow Memory Mode, Two Byte Read Timing Diagram



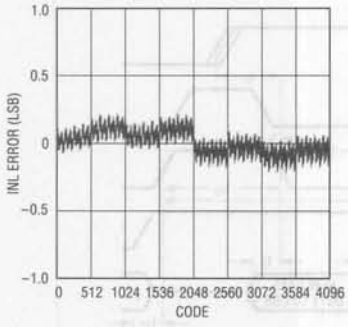
ROM Mode, Two Byte Read Timing Diagram



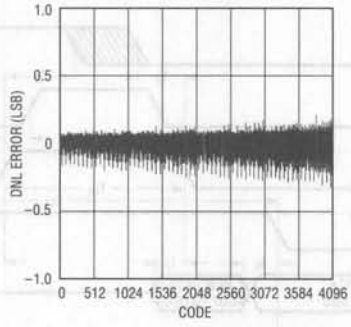
6

TYPICAL PERFORMANCE CHARACTERISTICS

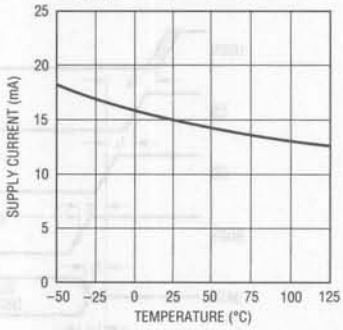
Integral Nonlinearity



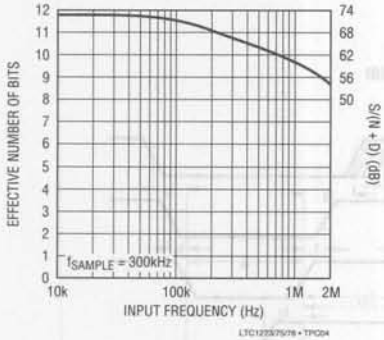
Differential Nonlinearity



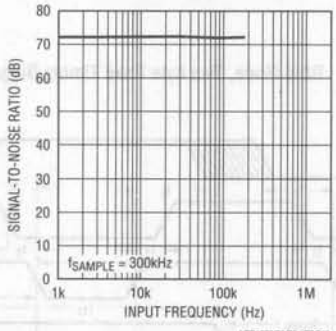
Supply Current vs Temperature



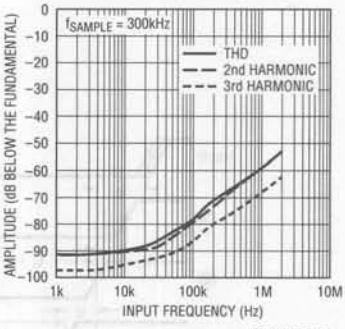
ENOBs and S/(N + D) vs Input Frequency



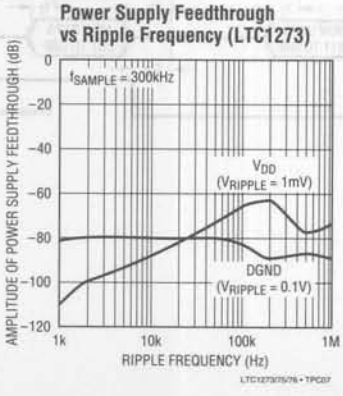
Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



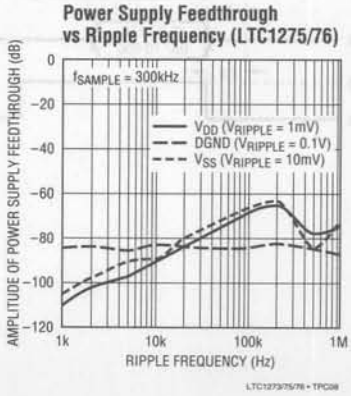
Distortion vs Input Frequency



Power Supply Feedthrough vs Ripple Frequency (LTC1273)

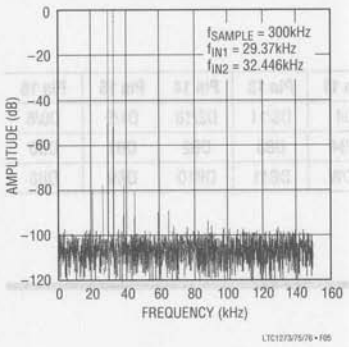


Power Supply Feedthrough vs Ripple Frequency (LTC1275/76)

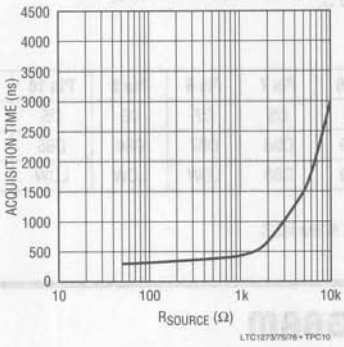


TYPICAL PERFORMANCE CHARACTERISTICS

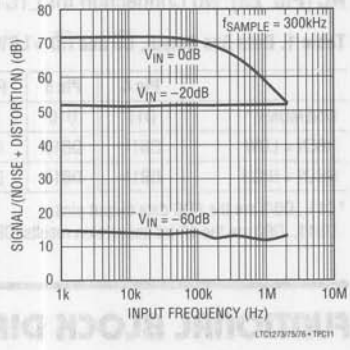
Intermodulation Distortion Plot



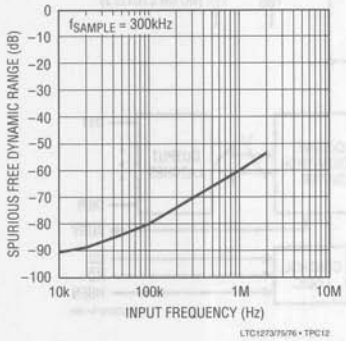
Acquisition Time vs Source Impedance



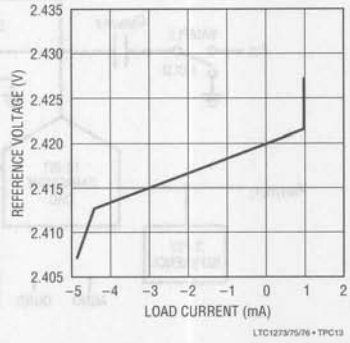
S/(N + D) vs Input Frequency and Amplitude



Spurious Free Dynamic Range vs Input Frequency



Reference Voltage vs Load Current



PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 5V (LTC1273), ±2.5V (LTC1275) or ±5V (LTC1276).

V_{REF} (Pin 2): +2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11-D4 (Pins 4 to 11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11-D0/8 (Pins 13 to 16): Three-State Data Outputs.

NC (Pins 17 and 18): No Connection.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). See Table 1. HBEN also disables conversion start when HIGH.

$\overline{RD}$ (Pin 20): READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output shows the converter status. It is low when a conversion is in progress.

PIN FUNCTIONS

V_{SS} (Pin 23): Negative Supply. –5V for LTC1275/LTC1276. Bypass to AGND with 0.1µF ceramic.

V_{DD} (Pin 24): Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

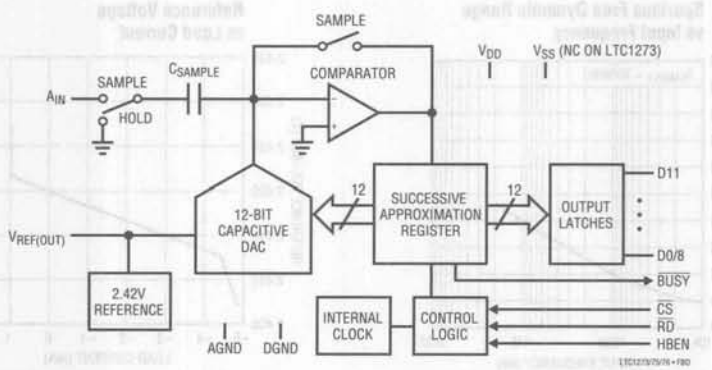
NC (Pin 23): No Connection for LTC1273.

Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

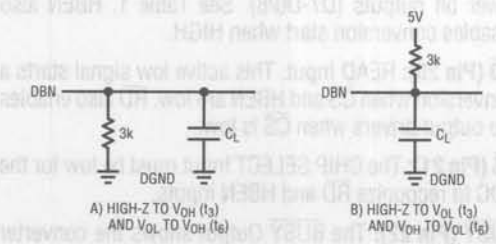
*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

FUNTIONAL BLOCK DIAGRAM

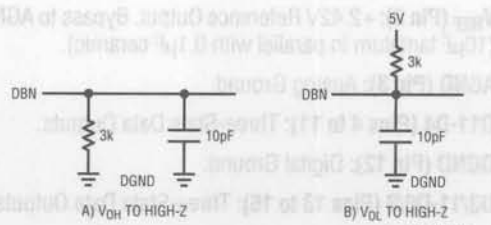


TEST CIRCUITS

Load Circuits for Access Time



Load Circuits for Output Float Delay



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1273/LTC1275/LTC1276 use a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel or 2-byte output. The ADCs are complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 600ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit output latches.

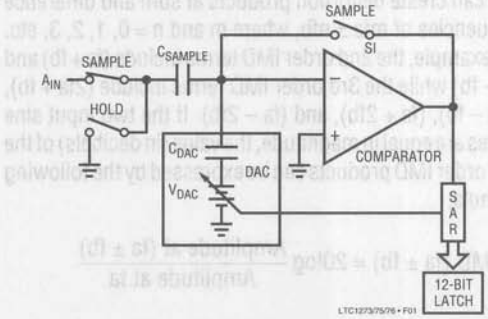


Figure 1. A_{IN} Input

DYNAMIC PERFORMANCE

The LTC1273/LTC1275/LTC1276 have an exceptionally high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1275 FFT plot.

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 300kHz sampling rate and a 29kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 150kHz.

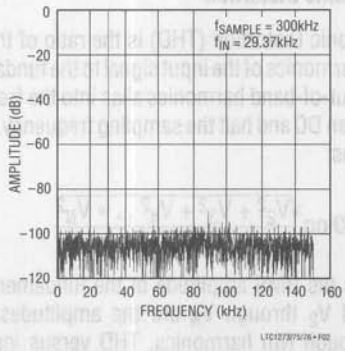


Figure 2. LTC1275 Nonaveraged, 1024 Point FFT Plot

APPLICATIONS INFORMATION

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 300kHz the LTC1273/LTC1275/LTC1276 maintain very good ENOBs up to the Nyquist input frequency of 150kHz. Refer to Figure 3.

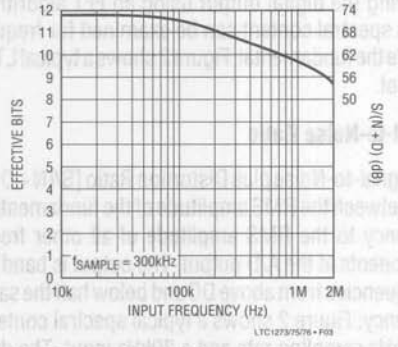


Figure 3. Effective Bits and Signal to (Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input frequency is shown in Figure 4. The LTC1273/LTC1275/LTC1276 have good distortion performance up to Nyquist and beyond.

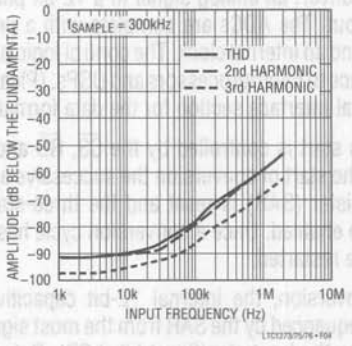


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log \frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

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Figure 5 shows the IMD performance at a 30kHz input.

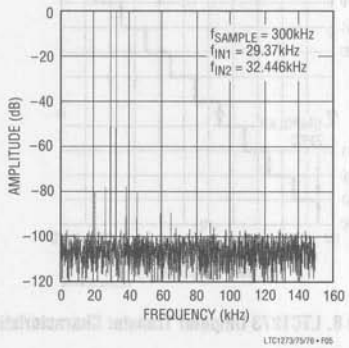

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1273/LTC1275/LTC1276 have been designed to optimize input bandwidth, allowing ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The analog inputs of the LTC1273/LTC1275/LTC1276 are easy to drive. They draw only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 600ns to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADCs' A_{IN} input include the LT1190/LT1191, LT1007, LT1220, LT1223 and LT1224 op amps.

The analog input tolerates source resistance very well. Here again, the only requirement is that the analog input must settle before the next conversion starts. For larger source resistance, full DC accuracy can be obtained if more time is allowed between conversions. For more information, see the Acquisition Time vs Source Resistance curve in the Typical Performance Characteristics section. For optimum frequency domain performance [e.g., S/(N + D)], keep the source resistance below 100Ω.

Internal Reference

The LTC1273/LTC1275/LTC1276 have an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

In the LTC1275, the V_{REF} pin can be driven above its normal value with a DAC or other means to provide input span adjustment or to improve the reference temperature drift. Figure 6 shows an LT1006 op amp driving the

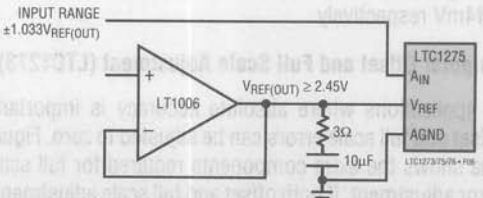

Figure 6. Driving the V_{REF} with the LT1006 Op Amp

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reference pin. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies. In the LTC1273/LT1276, the input spans are 0V to 5V and ±5V respectively with the internal reference. Driving the reference is not recommended on the LTC1273/LTC1276 since the input spans will exceed the supplies and codes will be lost at full scale.

Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1275. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.582V full scale.

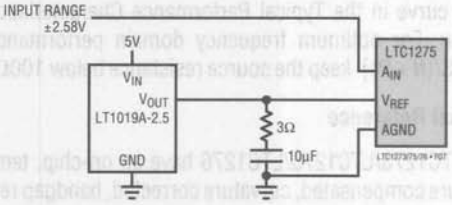

Figure 7. Supplying a 2.5V Reference Voltage to the LTC1275 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1273. The code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 1 1/2LSBs, 2 1/2LSBs, ... FS – 1 1/2LSBs). The output code is natural binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 9 shows the input/output transfer characteristics for the LTC1275/LTC1276 in 2's complement format. As stated in the figure, 1LSB for LTC1275/LTC1276 are 1.22mV and 2.44mV respectively.

Unipolar Offset and Full Scale Adjustment (LTC1273)

In applications where absolute accuracy is important, offset and full scale errors can be adjusted to zero. Figure 10a shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 10b can be used. Offset

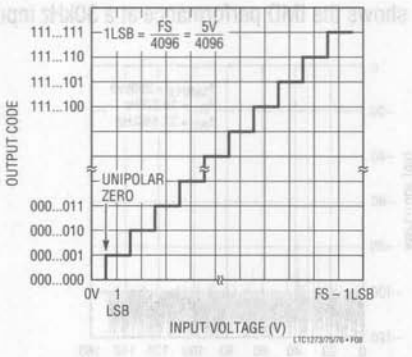

Figure 8. LTC1273 Unipolar Transfer Characteristic

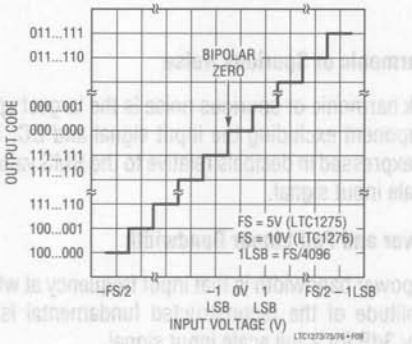

Figure 9. LTC1275/LTC1276 Bipolar Transfer Characteristic

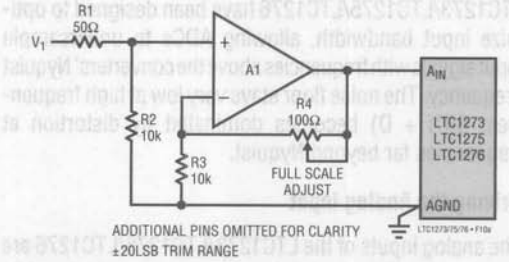

Figure 10a. Full Scale Adjust Circuit

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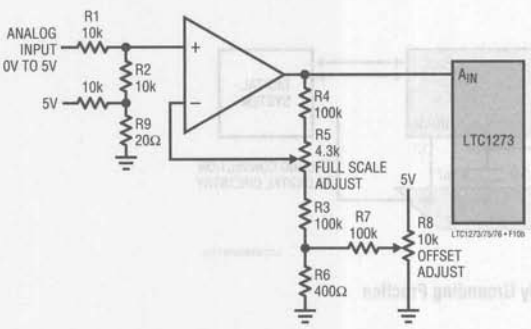

Figure 10b. LTC1273 Offset and Full Scale Adjust Circuit

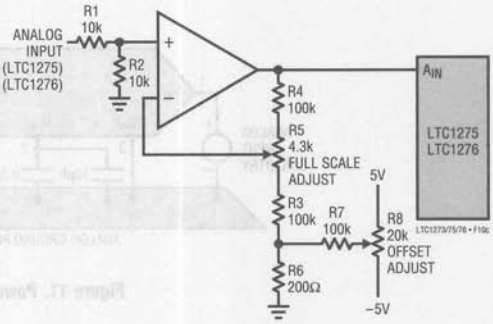

Figure 10c. LTC1275/LTC1276 Offset and Full Scale Adjust Circuit

should be adjusted before full scale. To adjust offset, apply 0.61mV (i.e., 1/2LSB) at the input and adjust the offset trim until the LTC1273 output code flickers between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply an analog input of 4.99817V (i.e., FS – 1 1/2LSBs or last code transition) at the input and adjust the full scale trim until the LTC1273 output code flickers between 1111 1111 1110 and 1111 1111 1111. It should be noted that if negative ADC offsets need to be adjusted or if an output swing to ground is required, the op amp in Figure 10b requires a negative power supply.

Bipolar Offset and Full Scale Adjustment (LTC1275/LTC1276)

Bipolar offset and full scale errors are adjusted in a similar fashion to the unipolar case. Figure 10a shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 10c can be used. Again, bipolar offset must be adjusted before full scale error. Bipolar offset adjustment is achieved by trimming the offset adjustment of Figure 10c while the input voltage is 1/2LSB below ground. This is done by applying an input voltage of –0.61mV or –1.22mV (–0.5LSB for LTC1275 or LTC1276) to the input in Figure 10c and adjusting R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 2.49817V or 4.99636V (FS – 1 1/2LSBs for LTC1275 or LTC1276) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

The LTC1273/LTC1275/LTC1276 are easy to use. To obtain the best performance from the devices a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 11. For the LTC1275/LTC1276 a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Noise: Input signal leads to A_{IN} and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an

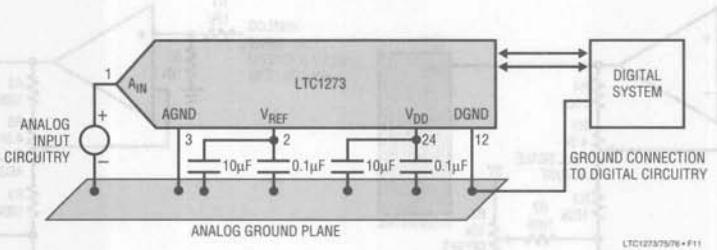

Figure 11. Power Supply Grounding Practice

error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground plane separate from the logic system ground should be established at Pin 3 (AGND) or as close as possible to the ADC, as shown in Figure 11. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the width for these traces should be as wide as possible.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the ADC. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADCs are designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally either connected to the microprocessor address bus or grounded.

Internal Clock

These ADCs have an internal clock that eliminates the need for synchronization between an external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 2.45µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required and, with the guaranteed maximum acquisition time of 600ns, throughput performance of 300ksps is assured.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 12 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required

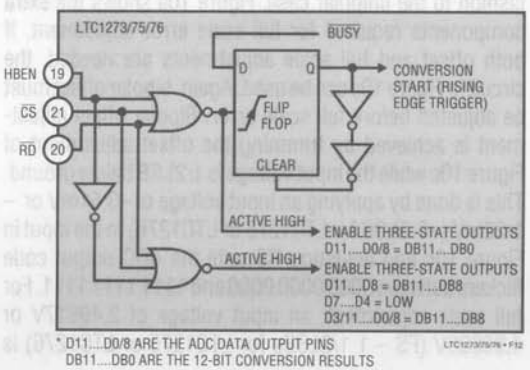

Figure 12. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

APPLICATIONS INFORMATION

on all three inputs to initiate a conversion. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

There are two modes of operation as outlined by the timing diagrams of Figures 13 to 16. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

Data Format

The output format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7...D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7...D0/8 outputs (4MSBs or 8MSBs) where it can be read in two read cycles. The 4MSBs always appear on D11...D8 whenever the three-state output drivers are turned on.

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 13 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low trigger a conversion and the ADC acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11...D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only 8 data outputs D7...D0/8 are used. Conversion start procedure and data output status for the first read operation are identical to Slow Memory Mode, Parallel Read. See Figure 14 timing diagram and Table 3 data bus status. At the end of the conversion, the low data byte (D7...D0/8) is read from the ADC. A second READ operation, with the HBEN high, places the high byte on data outputs D3/11...D0/8 and disables conversion start. Note

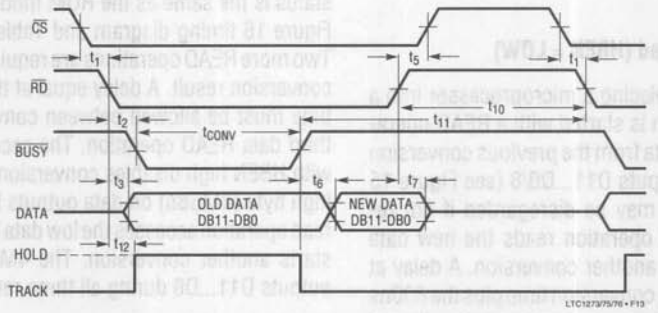

Figure 13. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

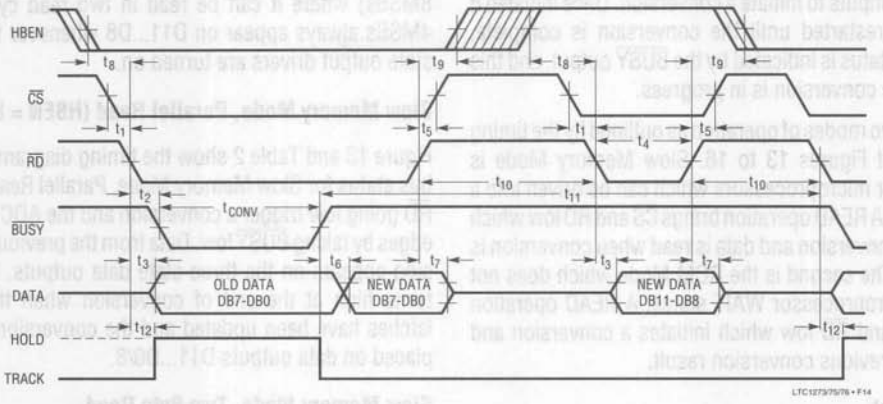

Figure 14. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

that the 4MSBs appear on data output D11...D8 during both READ operations.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a WAIT state. A conversion is started with a READ operation, and the 12 bits of data from the previous conversion are available on data outputs D11...D0/8 (see Figure 15 and Table 4). This data may be disregarded if not required. A second READ operation reads the new data (DB11...DB0) and starts another conversion. A delay at least as long as the ADC's conversion time plus the 600ns minimum delay between conversions must be allowed between READ operations.

ROM Mode, Two Byte Read

As previously mentioned for a two byte read, only data outputs D7...D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM mode, Parallel Read (see Figure 16 timing diagram and Table 5 data bus status). Two more READ operations are required to access the new conversion result. A delay equal at the ADCs' conversion time must be allowed between conversion start and the third data READ operation. The second READ operation with HBEN high disables conversion start and places the high byte (4MSBs) on data outputs D3/11...D0/8. A third read operation accesses the low data byte (DB7...DB0) and starts another conversion. The 4MSBs appear on data outputs D11...D8 during all three read operations.

MICROPROCESSOR INTERFACING

The LTC1273/LTC1275/LTC1276 allow easy interfacing to digital signal processors as well as modern high speed, 8-bit or 16-bit microprocessors. Here are several examples.

APPLICATIONS INFORMATION

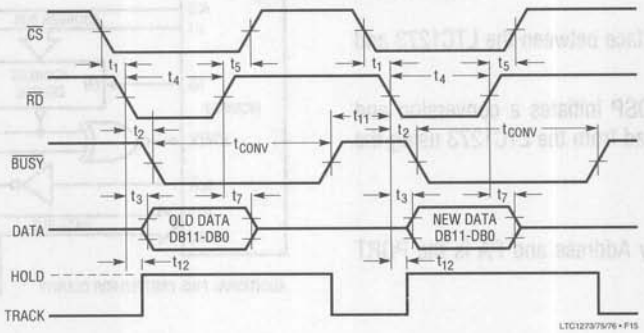

Figure 15. ROM Mode, Parallel Read Timing Diagram (HBEN = LOW)

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

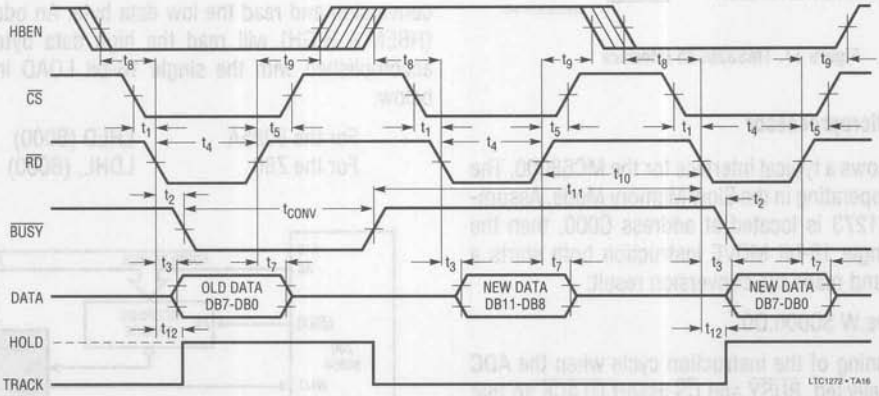

Figure 16. ROM Mode Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read (New Data)	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read (New Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

TMS320C25

Figure 17 shows an interface between the LTC1273 and the TMS320C25.

The W/R signal of the DSP initiates a conversion and conversion results are read from the LTC1273 using the following instruction:

IN D, PA

where D is Data Memory Address and PA is the PORT ADDRESS.

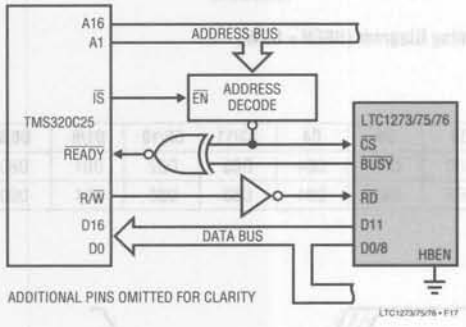

Figure 17. TMS320C25 Interface

MC68000 Microprocessor

Figure 18 shows a typical interface for the MC68000. The LTC1273 is operating in the Slow Memory Mode. Assuming the LTC1273 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result:

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, BUSY and CS assert DTACK so that the MC68000 is forced into a WAIT state. At the end of conversion, BUSY returns high and the conversion result is placed in the D0 register of the microprocessor.

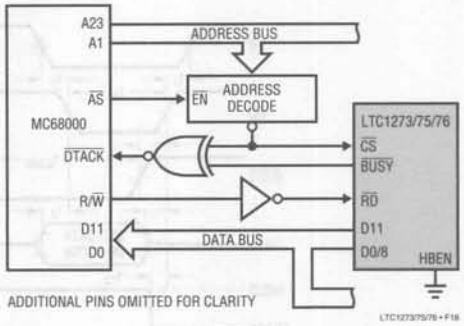

Figure 18. MC68000 Interface

8085A/Z80 Microprocessor

Figure 19 shows an LTC1273 interface for the Z80/8085A. The LTC1273 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN so that an even address (HBEN = LOW) to the LTC1273 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A	LHLD (B000)
For the Z80	LDHL, (B000)

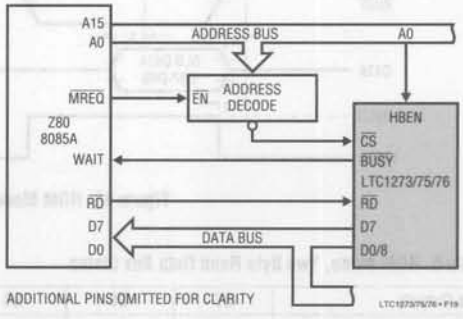

Figure 19. 8085A and Z80 Interface

APPLICATIONS INFORMATION

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the LTC1273 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 20 shows an LTC1273/TMS32010 interface. The LTC1273 is operating in the ROM Mode.

The LTC1273 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

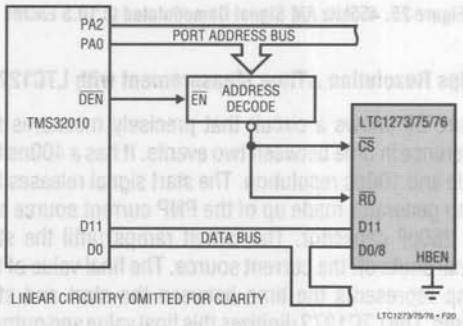

Figure 20. TMS32010 Interface

MUXing with CD4051

The high input impedance of the LTC1273/LTC1275/LTC1276 provides an easy, cheap, fast, and accurate way to multiplex many channels of data through one converter. Figure 21 shows a low cost CD4051 connected to the LTC1275. The LTC1275's input draws no DC input current so it can be accurately driven by the unbuffered MUX. The CD4520 counter increments the MUX channel after each sample is taken. Figure 22 shows the acquisition time of LTC1275 vs the source resistance. For a 500Ω maximum "on" resistance of the CD4051, the acquisition time of the ADC is not greatly affected. For larger source resistances, modest increases in acquisition time must be allowed.

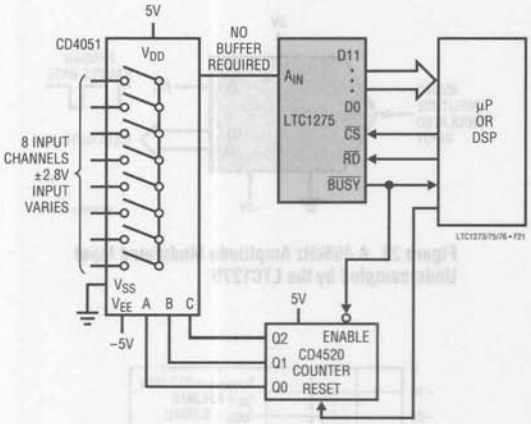

Figure 21. MUXing the LTC1275 with CD4051

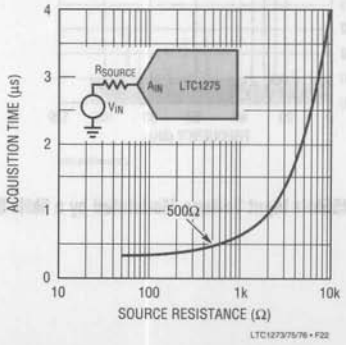

Figure 22. Acqusition Time of LTC1275 vs Source Resistance

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APPLICATIONS INFORMATION

Demodulating a Signal by Undersampling with LTC1275

Figure 23 shows a 455kHz amplitude modulated input undersampled by the LTC1275. With a 227.5kHz sample rate, the converter provides a 100dB noise floor and 68dB distortion when digitizing the 455kHz AM input.

Figure 24 shows an FFT of the AM signal digitized at 212.5kHz.

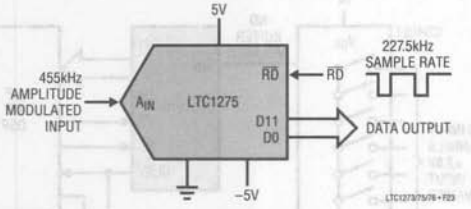


Figure 23. A 455kHz Amplitude Modulated Input Undersampled by the LTC1275

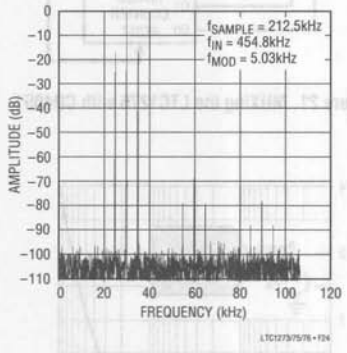


Figure 24. 455kHz Input Voltage Modulated by a 5kHz Signal

A time domain view of the demodulation is shown in Figure 25. The top trace shows the 455kHz waveform modulated by a –6dB, 5kHz signal. The bottom trace shows the demodulated signal produced by the LTC1275 reconstructed through a 12-bit DAC. The resultant frequency is 5kHz with a sample rate of 227.5kHz. There are roughly 45 points per cycle.

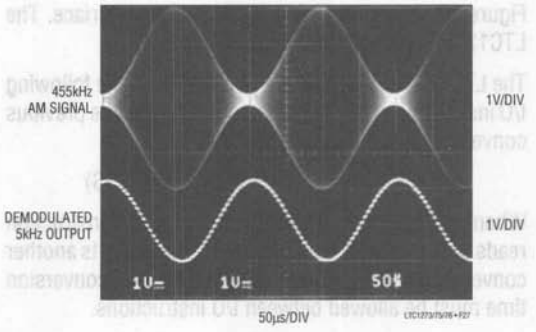


Figure 25. 455kHz AM Signal Demodulated to 10.5 ENOBs

100ps Resolution ΔTime Measurement with LTC1273

Figure 26 shows a circuit that precisely measures the difference in time between two events. It has a 400ns full scale and 100ps resolution. The start signal releases the ramp generator made up of the PNP current source and the 250pF capacitor. The circuit ramps until the stop signal shuts off the current source. The final value of the ramp represents the time between the start and stop events. The LTC1273 digitizes this final value and outputs the digital data.

APPLICATIONS INFORMATION

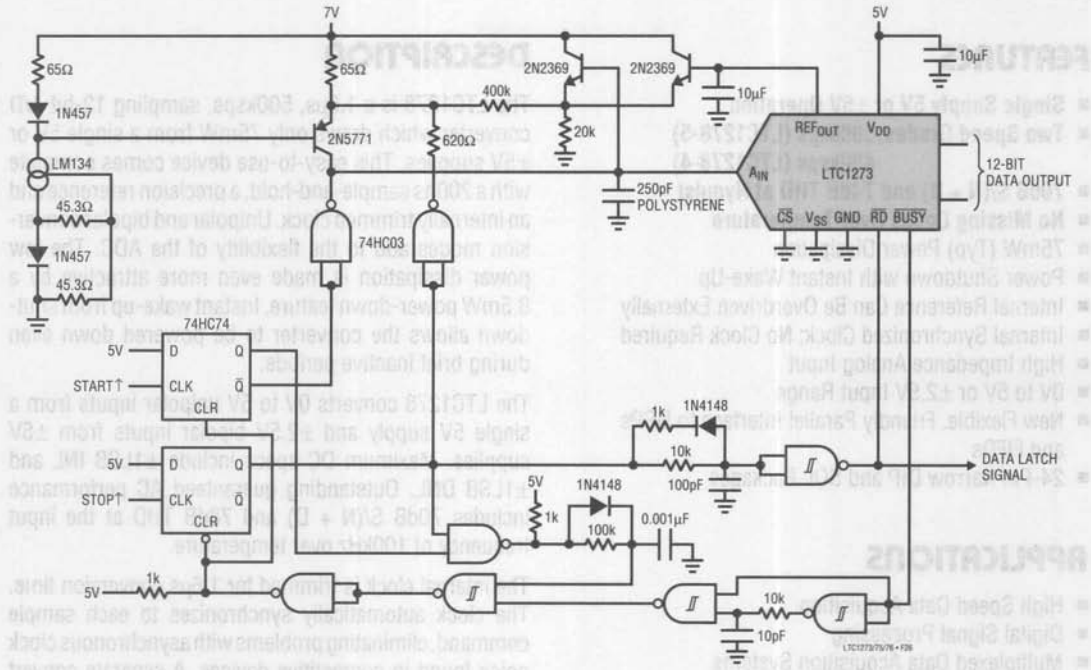


Figure 26. ΔTime Measurement with the LTC1273

12-Bit, 500ksps Sampling A/D Converter with Shutdown

FEATURES

- **Single Supply 5V or ±5V Operation**
- **Two Speed Grades, 500ksps (LTC1278-5)**
  400ksps (LTC1278-4)
- **70dB S/(N + D) and 74dB THD at Nyquist**
- **No Missing Codes Over Temperature**
- 75mW (Typ) Power Dissipation
- Power Shutdown with Instant Wake-Up
- Internal Reference Can Be Overdriven Externally
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- 0V to 5V or ±2.5V Input Range
- New Flexible, Friendly Parallel Interface to DSPs and FIFOs
- 24-Pin Narrow DIP and SOL Packages

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

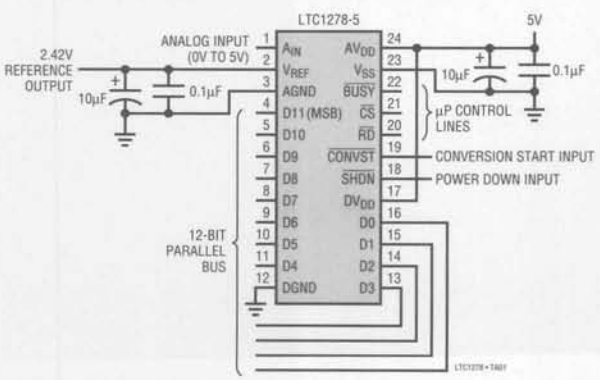
The LTC1278 is a 1.6µs, 500ksps, sampling 12-bit A/D converter which draws only 75mW from a single 5V or ±5V supplies. This easy-to-use device comes complete with a 200ns sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The low power dissipation is made even more attractive by a 8.5mW power-down feature. Instant wake-up from shutdown allows the converter to be powered down even during brief inactive periods.

The LTC1278 converts 0V to 5V unipolar inputs from a single 5V supply and ±2.5V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL and ±1LSB DNL. Outstanding guaranteed AC performance includes 70dB S/(N + D) and 78dB THD at the input frequency of 100kHz over temperature.

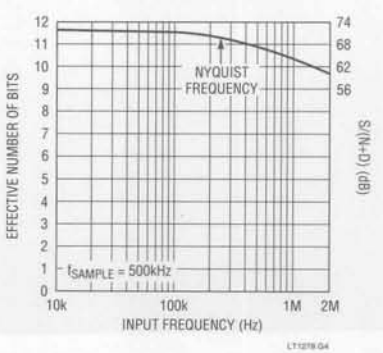
The internal clock is trimmed for 1.6µs conversion time. The clock automatically synchronizes to each sample command, eliminating problems with asynchronous clock noise found in competitive devices. A separate convert start input and a data ready signal (BUSY) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Single 5V Supply, 500kHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

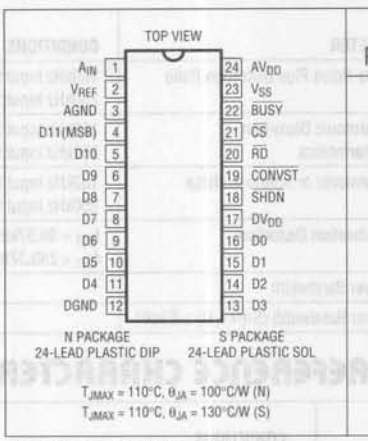


ABSOLUTE MAXIMUM RATINGS

$AV_{DD} = DV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 12V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... – 0.3V to V_{DD} + 0.3V
  Bipolar Operation..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  Unipolar Operation .....–0.3V to 12V
  Bipolar Operation..... V_{SS} – 0.3V to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to V_{DD} + 0.3V
  Bipolar Operation..... V_{SS} – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1278-4C, LTC1278-5C ..... 0°C to 70°C
  LTC1278-4I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1278-4CN
LTC1278-5CN
LTC1278-4IN
LTC1278-4CS
LTC1278-5CS
LTC1278-4IS

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bit
Integral Linearity Error	(Note 7)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error	(Note 8)				±4	LSB
		●			±6	LSB
Gain Error					±15	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.95V ≤ V_{DD} ≤ 5.25V (Unipolar)	●		0 to 5		V
		4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (Bipolar)	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			45		pF
		During Conversions (Hold Mode)			5		pF

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DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 250kHz Input Signal	● 	70	72 70		dB dB
THD	Total Harmonic Distortion First 5 Harmonics	100kHz Input Signal 250kHz Input Signal	● 		−80 −74	−78 	dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 250kHz Input Signal	● 		−84 −74	−82 	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 99.37kHz, f_{IN2} = 102.4kHz f_{IN1} = 249.37kHz, f_{IN2} = 252.4kHz			−82 −70		dB dB
	Full Power Bandwidth				4		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				350		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.95V ≤ V_{DD} ≤ 5.25V −5.25V ≤ V_{SS} ≤ −4.95V			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	0V ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.95V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.95V I_O = −10µA I_O = −200µA	 ●	 4	4.7		 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.95V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 10, 11)	Unipolar		4.95		5.25	V
		Bipolar		4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 10)	Bipolar Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 500ksps	●		15.0	29.5	mA
		$\overline{SHDN}$ = 0V	●		1.7	3.0	mA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 500ksps, V_{SS} = –5V	●		0.12	0.30	mA
P_D	Power Dissipation	f_{SAMPLE} = 500ksps	●		75.0	150	mW
		$\overline{SHDN}$ = 0V	●		8.5	15	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1278-4/LTC1278-5 MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	LTC1278-4	●	400			kHz
		LTC1278-5	●	500			
$t_{SAMPLE(MIN)}$	Minimum Throughput Time	LTC1278-4	●			2.5	µs
	(Acquisition Time Plus Conversion Time)	LTC1278-5	●			2.0	µs
t_{CONV}	Conversion Time	LTC1278-4			2.0	2.3	µs
		LTC1278-5			1.6	1.85	µs
t_{ACQ}	Acquisition Time				200		ns
t_1	$\overline{CS}\downarrow$ to $\overline{RD}\downarrow$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	20			ns
t_3	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 10)			350		ns
t_4	$\overline{CONVST}$ Low Time	(Notes 10, 12)	●	40			ns
t_5	$\overline{CONVST}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 100pF			40	110	ns
		Commercial	●			130	ns
		Industrial	●			140	ns
t_6	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 100pF	●	20	40		ns
t_7	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	Mode 2, (see Figure 14) (Note 9)	●	–20			ns
t_8	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 9)			50	90	ns
		Commercial	●			110	ns
		Industrial	●			120	ns
		C_L = 100pF			70	125	ns
		Commercial	●			150	ns
		Industrial	●			170	ns
t_9	Bus Relinquish Time			20	30	75	ns
		Commercial	●	20		85	ns
		Industrial	●	20		90	ns
t_{10}	$\overline{RD}$ Low Time	(Note 9)	●	t_8			ns
t_{11}	$\overline{CONVST}$ High Time	(Notes 9, 12)	●	40			ns
t_{12}	Aperture Delay of Sample-and-Hold	Jitter <50ps			15		ns

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TIMING CHARACTERISTICS (Note 5)

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: $AV_{DD} = DV_{DD} = V_{DD} = 5V$, ($V_{SS} = -5V$ for bipolar mode), f_{SAMPLE} = 400kHz (LTC1278-4), 500kHz (LTC1278-5), $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

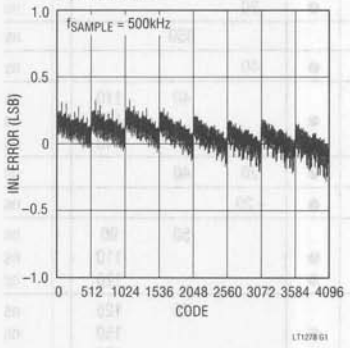
Note 10: Recommended operating conditions.

Note 11: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy. Therefore the minimum supply voltage for the unipolar mode is 4.95V. The minimum for the bipolar mode is 4.75V, –2.45V.

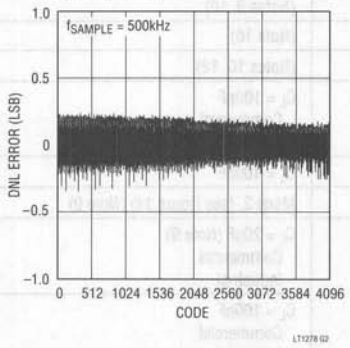
Note 12: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high either within 120ns after conversion start (i.e., before the first bit decision) or after $\overline{\text{BUSY}}$ rises (i.e., after the last bit test). See mode 1a and 1b (Figures 12 and 13) timing diagrams.

TYPICAL PERFORMANCE CHARACTERISTICS

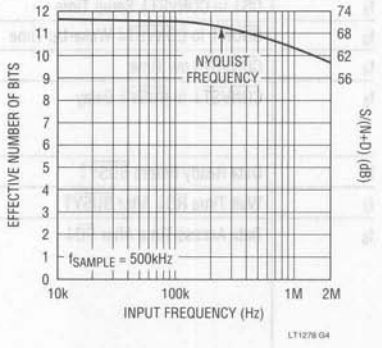
Integral Nonlinearity vs Output Code



Differential Nonlinearity vs Output Code

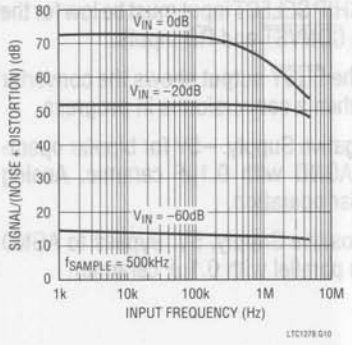


ENOBs and S/(N + D) vs Input Frequency

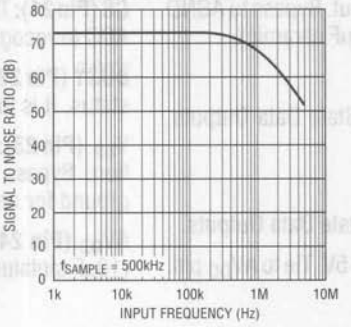


TYPICAL PERFORMANCE CHARACTERISTICS

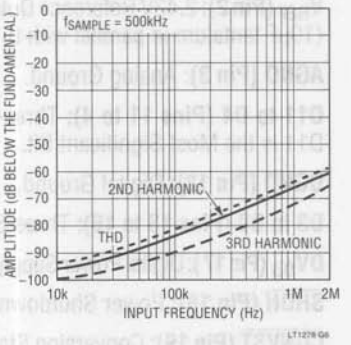
S/(N + D) vs Input Frequency and Amplitude



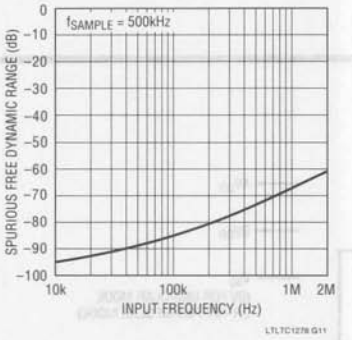
Signal-to-Noise Ratio (without Harmonics) vs Input Frequency



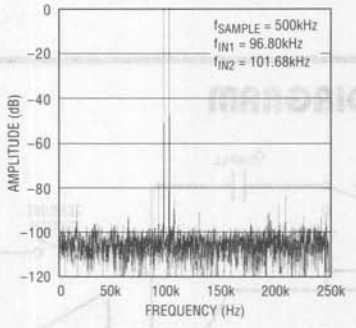
Distortion vs Input Frequency



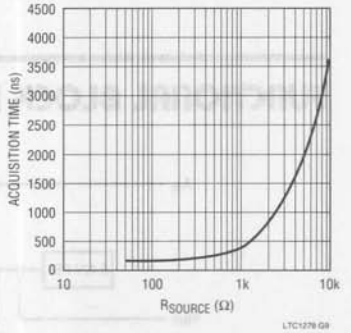
Spurious Free Dynamic Range vs Input Frequency



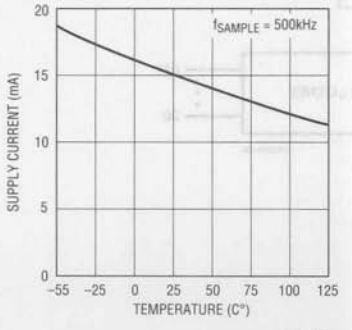
Intermodulation Distortion Plot



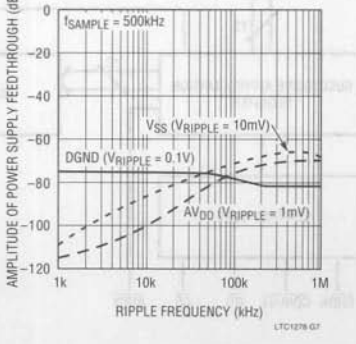
Acquisition Time vs Source Impedance



Supply Current vs Temperature



Power Supply Feedthrough vs Ripple Frequency



Reference Voltage vs Load Current

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PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 5V (Unipolar), ±2.5V (Bipolar).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 11 to 4): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

DV_{DD} (Pin 17): Digital Power Supply, 5V. Tie to AV_{DD} pin.

$\overline{SHDN}$ (Pin 18): Power Shutdown.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be low).

$\overline{RD}$ (Pin 20): READ Input. This enables the output drivers when $\overline{CS}$ is low.

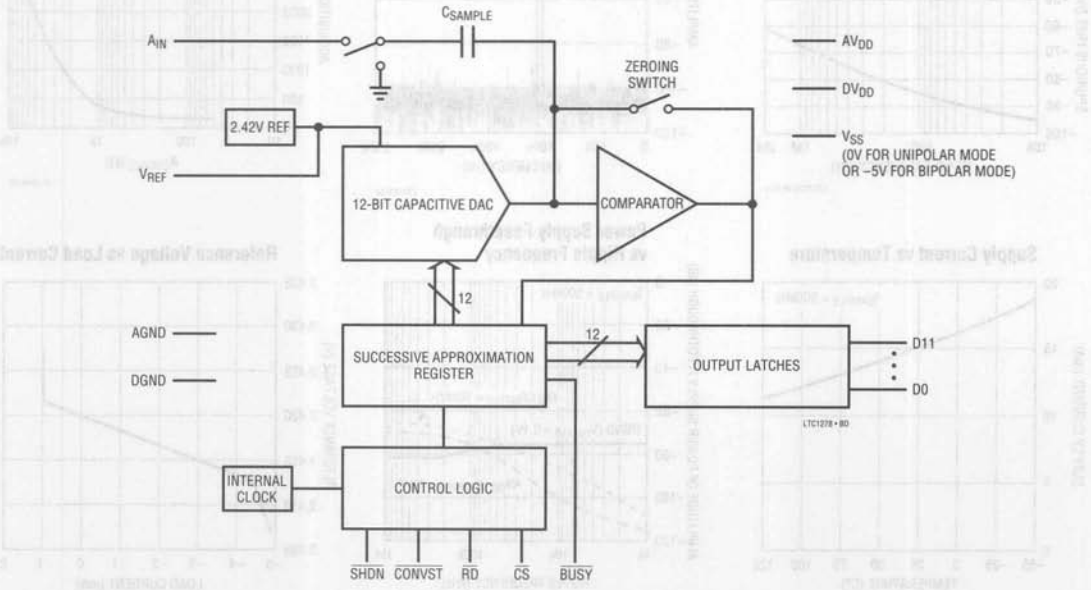
$\overline{CS}$ (Pin 21): The CHIP SELECT input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress.

V_{SS} (Pin 23): Negative Supply. –5V for bipolar operation. Bypass to AGND with 0.1µF ceramic. Analog ground for unipolar operation.

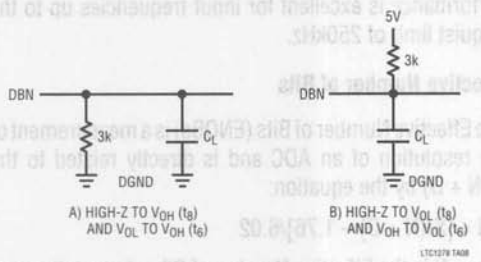
AV_{DD} (Pin 24): Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

FUNCTIONAL BLOCK DIAGRAM

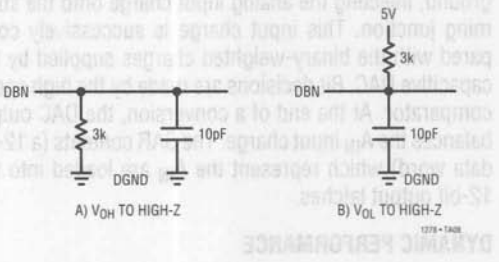


TEST CIRCUITS

Load Circuits for Access Timing

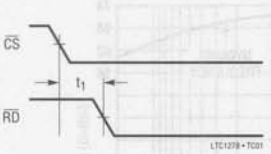


Load Circuits for Output Float Delay

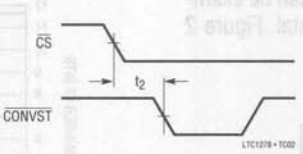


TIMING DIAGRAMS

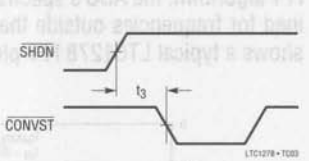
$\overline{CS}$ to $\overline{RD}$ Setup Timing



$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



$\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing



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APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1278 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the

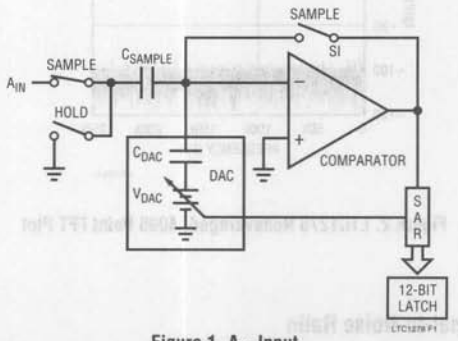

Figure 1. A_{IN} Input

APPLICATIONS INFORMATION

compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit output latches.

DYNAMIC PERFORMANCE

The LTC1278 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1278 FFT plot.

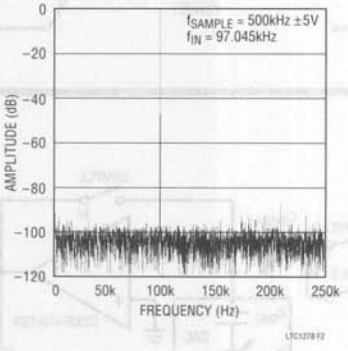

Figure 2. LTC1278 Nonaveraged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 500kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 250kHz.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 500kHz the LTC1278 maintains very good ENOBs up to the Nyquist input frequency of 250kHz. Refer to Figure 3.

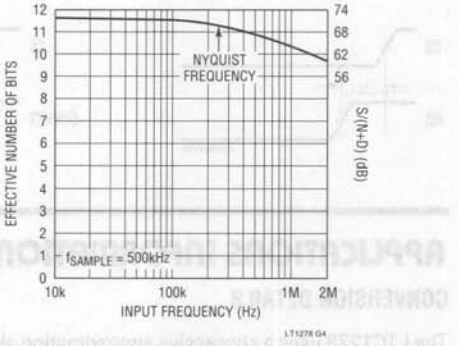

Figure 3. Effective Bits and Signal-to-Noise + Distortion vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input

APPLICATIONS INFORMATION

frequency is shown in Figure 4. The LTC1278 has good distortion performance up to the Nyquist frequency and beyond.

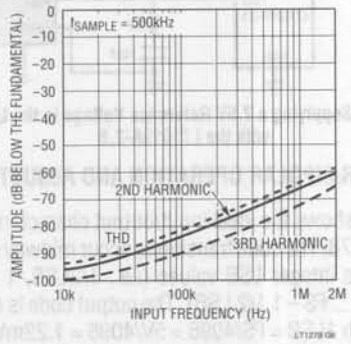

Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log \frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 100kHz input.

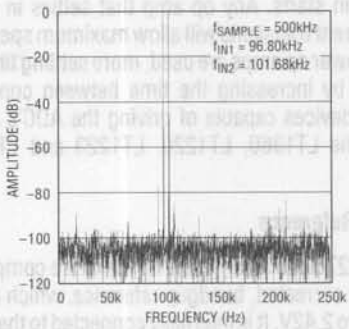

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1278 has been designed to optimize input bandwidth, allowing ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The analog input of the LTC1278 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next

APPLICATIONS INFORMATION

conversion starts. Any op amp that settles in 200ns to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT1360, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1278 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies.

Figure 6 shows an LT1006 op amp driving the reference pin. (In the unipolar mode, the input span is already 0V to 5V with the internal reference so driving the reference is not recommended, since the input span will exceed the supply and codes will be lost at the full scale.) Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1278. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.582V full scale.

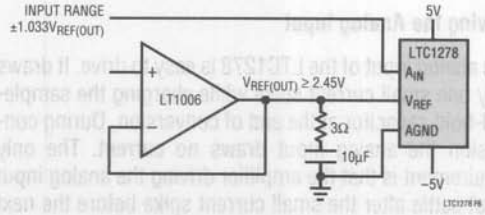

Figure 6. Driving the V_{REF} with the LT1006 Op Amp

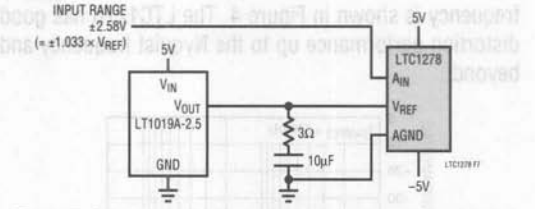

Figure 7. Supplying a 2.5V Reference Voltage to the LTC1278 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8a shows the ideal input/output characteristics for the LTC1278. The code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 1 1/2LSB, 2 1/2LSB, ... FS – 1 1/2 LSB). The output code is naturally binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 8b shows the input/output transfer characteristics for the bipolar mode in two's complement format.

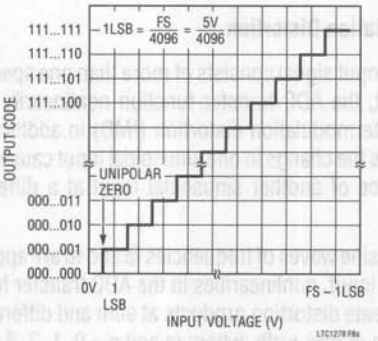

Figure 8a. LTC1278 Unipolar Transfer Characteristics

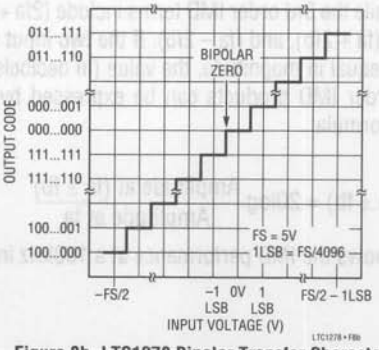

Figure 8b. LTC1278 Bipolar Transfer Characteristics

APPLICATIONS INFORMATION

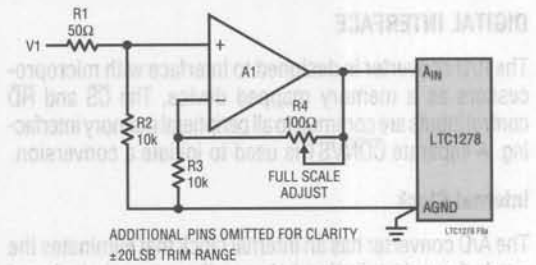

Figure 9a. Full Scale Adjust Circuit

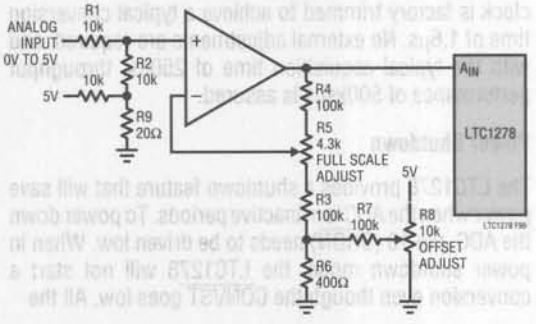

Figure 9b. LTC1278 Unipolar Offset and Full Scale Adjust Circuit

Unipolar Offset and Full Scale Error Adjustments

In applications where absolute accuracy is important, then offset and full scale errors can be adjusted to zero. Offset error must be adjusted before full scale error. Figure 9a shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 9b can be used. For zero offset error apply 0.61mV (i.e., 1/2LSB) at the input and adjust the offset trim until the LTC1278 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full scale error apply an analog input of 4.99817V (i.e., FS – 1 1/2LSB or last code transition) at the input and adjust R5 until the LTC1278 output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Offset and Full Scale Error Adjustments

Bipolar offset and full scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp

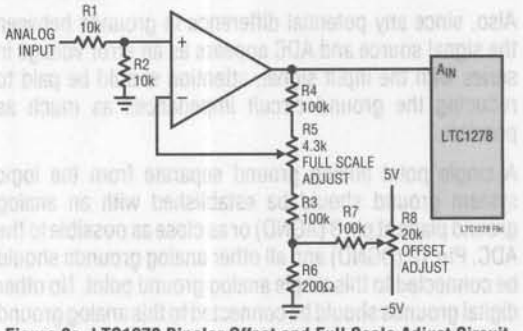

Figure 9c. LTC1278 Bipolar Offset and Full Scale Adjust Circuit

driving the analog input of the LTC1278 while the input voltage is 1/2LSB below ground. This is done by applying an input voltage of –0.61mV (–1/2LSB) to the input in Figure 9c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 2.49817V (FS – 3/2LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1278, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the AV_{DD} and V_{REF} pins as shown in Figure 10. For the bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from AGND (pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended.

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Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 1.6µs. No external adjustments are required, and with the typical acquisition time of 250ns, throughput performance of 500ksps is assured.

Power Shutdown

The LTC1278 provides a shutdown feature that will save power when the ADC is in inactive periods. To power down the ADC, pin 18 ($\overline{SHDN}$) needs to be driven low. When in power shutdown mode, the LTC1278 will not start a conversion even though the $\overline{CONVST}$ goes low. All the

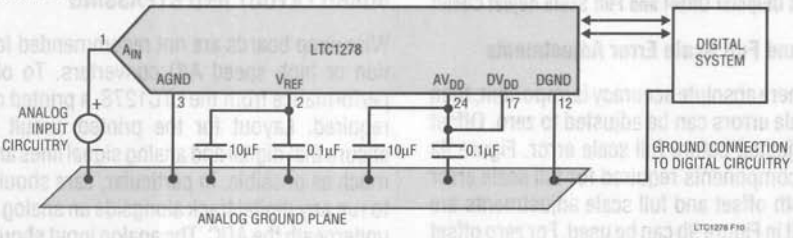

Figure 10. Power Supply Grounding Practice

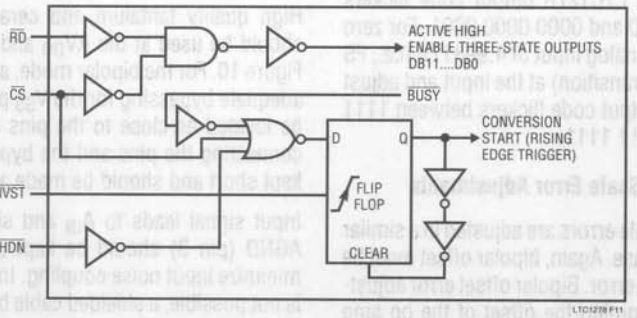

Figure 11. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ and $\overline{SHDN}$

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power is off except the Internal Reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 8.5mW instead of 75mW (for minimum power, the logic inputs must be within 600mV of the supply rails). The wake-up time from the power shutdown to active state is 350ns.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. Figure 11 shows the logic structure associated with these inputs. A logic "0" for $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

Figures 12 through 16 show several different modes of operation. In modes 1a and 1b (Figures 12 and 13) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow low going $\overline{CONVST}$ pulse. Mode 1b shows high going $\overline{CONVST}$ pulse.

In mode 2 (Figure 14) $\overline{CS}$ is tied low. The falling $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In Slow memory and ROM modes (Figures 15 and 16) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts conversion and read the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In Slow memory mode the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low and starts the conversion. $\overline{BUSY}$ goes low forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor, and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low which starts a conversion and reads the previous conversion result. After the conversion is complete, the processor can read the new result (which will initiate another conversion).

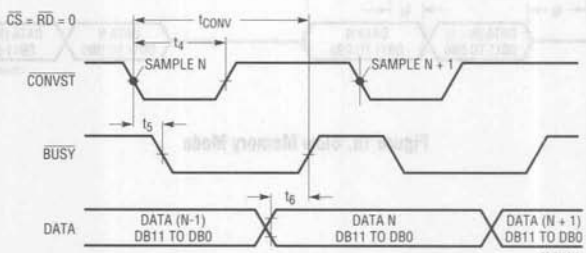

Figure 12. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Ouputs Always Enabled.($\overline{CONVST}$ =)

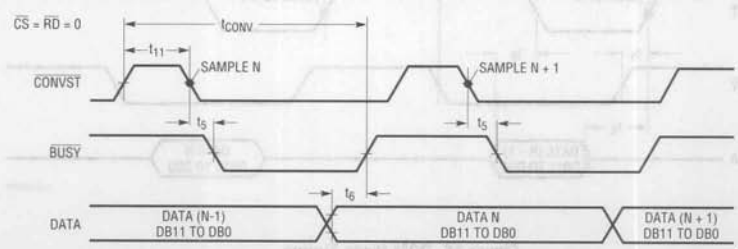

Figure 13. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled.($\overline{CONVST}$ =)

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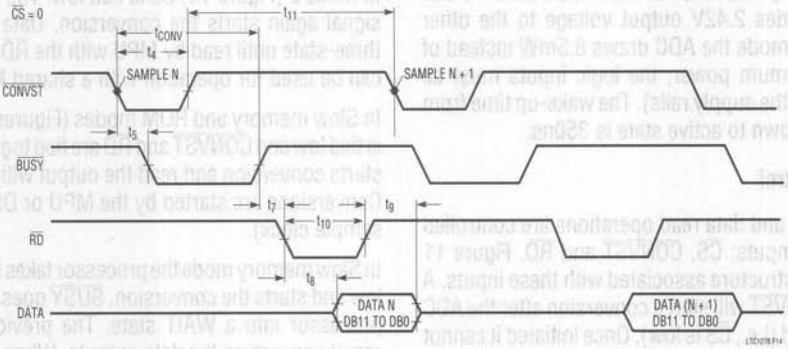

Figure 14. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

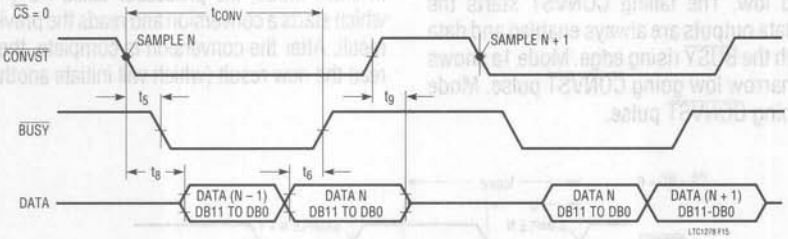

Figure 15. Slow Memory Mode

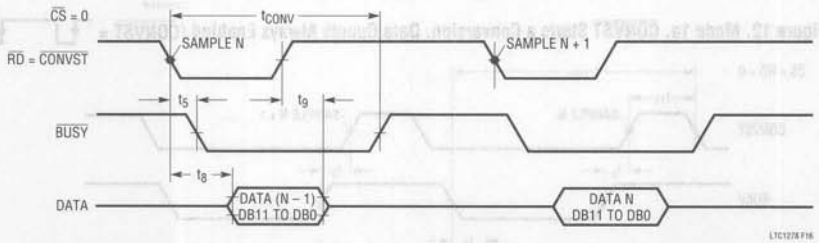

Figure 16. ROM Mode Timing

3V 140ksps 12-Bit Sampling A/D Converter with Reference

FEATURES

- **Single Supply 3V or ±3V Operation**
- **140ksps Throughput Rate**
- **12mW (Typ) Power Dissipation**
- On-Chip 25ppm/°C Reference
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- 69dB S/(N + D) and 77dB THD at Nyquist
- ±1/2LSB INL and ±3/4LSB DNL Max (A Grade)
- 2.7V Guaranteed Minimum Supply Voltage
- ESD Protected On All Pins
- 24-Pin Narrow DIP and SOL Packages
- 0V to 2.5V or ±1.25V Input Ranges

APPLICATIONS

- 3V Powered Systems
- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC1282 is a 6µs, 140ksps, sampling 12-bit A/D converter which draws only 12mW from a single 3V or dual ±3V supply. This easy-to-use device comes complete with 1.0µs sample-and-hold, precision reference and internally trimmed clock. Unipolar and bipolar conversion modes provide flexibility for various applications. They are built with LTBiCMOS™ switched capacitor technology.

The LTC1282 has a 25ppm/°C (max) internal reference and converts 0V to 2.5V unipolar inputs from a single 3V supply. With ±3V supplies its input range is ±1.25V with two's complement output format. Maximum DC specifications include ±1/2LSB INL, ±3/4LSB DNL and 25ppm/°C full scale drift over temperature. Outstanding AC performance includes 69dB S/(N + D) and 77dB THD at the Nyquist input frequency of 70kHz.

The internal clock is trimmed for 6µs maximum conversion time. The clock automatically synchronizes to each sample command eliminating problems with asynchronous clock noise found in competitive devices. A high speed parallel interface eases connections to FIFOs, DSPs and microprocessors.

LTBiCMOS™ is a trademark of Linear Technology Corporation

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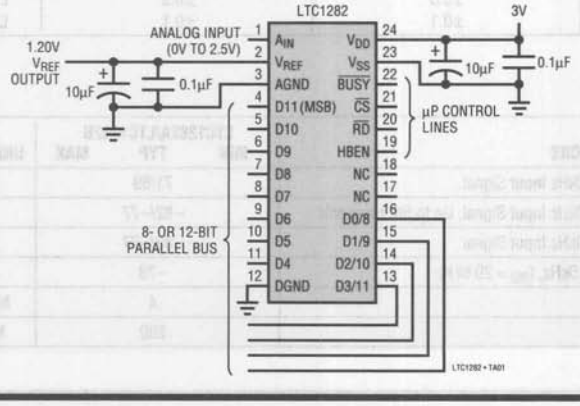
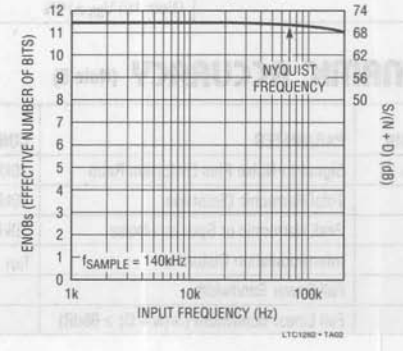
TYPICAL APPLICATION

Single 3V Supply, 140ksps, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

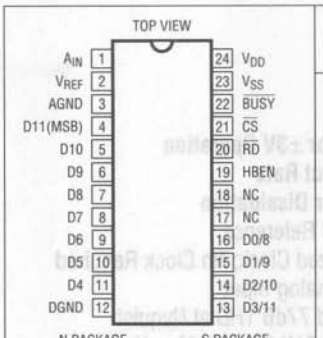


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{DD}) 12V
Negative Supply Voltage (V_{SS}) ..... −6V to GND
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} − 0.3V to 12V
Digital Output Voltage
(Note 3) ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Specified Temperature Range (Note 14) ..... 0°C to 70°C
Operating Temperature Range
LTC1282AC, LTC1282BC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1282ACN
LTC1282BCN
LTC1282ACS
LTC1282BCS

Consult factory for Industrial and Military grade parts (Note 14).

CONVERTER CHARACTERISTICS With Internal Reference (Notes 5 and 6)

PARAMETER	CONDITIONS		LTC1282A MIN	LTC1282A TYP	LTC1282A MAX	LTC1282B MIN	LTC1282B TYP	LTC1282B MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7)				±1/2			±1	LSB
	Commercial	●			±1/2			±1	LSB
	Military	●			±3/4			±1	LSB
Differential Linearity Error	Commercial	●			±3/4			±1	LSB
	Military	●			±1			±1	LSB
Offset Error	(Note 8)				±3			±4	LSB
		●			±4			±6	LSB
Gain Error					±10			±15	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±5	±25		±10	±45	ppm/°C
Power Supply Rejection	(Note 9) V_{DD} ±10%			±0.3			±0.3		LSB
	(Note 10) V_{SS} ±10%			±0.1			±0.1		LSB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1282A/LTC1282B MIN	LTC1282A/LTC1282B TYP	LTC1282A/LTC1282B MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	10kHz/70kHz Input Signal		71/69		dB
THD	Total Harmonic Distortion	10kHz/70kHz Input Signal, Up to 5th Harmonic		−82/−77		dB
	Peak Harmonic or Spurious Noise	10kHz/70kHz Input Signal		−82/−77		dB
IMD	Intermodulation Distortion	f_{IN1} = 19.0kHz, f_{IN2} = 20.6kHz		−78		dB
	Full Power Bandwidth			4		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)			200		kHz

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1282A/LTC1282B MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 11)	$2.7V \le V_{DD} \le 3.6V$ (Unipolar Mode) $2.7V \le V_{DD} \le 3.6V$, $-3.3V \le V_{SS} \le -2.5V$ (Bipolar Mode)	● ●		0 to 2.5 ±1.25		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			63 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Commercial Military	● ●		0.45	1.00 1.50	µs µs

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1282A MIN	TYP	MAX	LTC1282B MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	$I_{OUT} = 0$		1.1900	1.200	1.210	1.190	1.200	1.210	V
V_{REF} Output Tempco	$I_{OUT} = 0$	●		±5	±25		±10	±45	ppm/°C
V_{REF} Line Regulation	$2.7V \le V_{DD} \le 3.6V$ $-3.6V \le V_{SS} \le -2.7V$			0.55 0.02			0.55 0.02		LSB/V LSB/V
V_{REF} Load Regulation	$0V \le \lvert I_{OUT} \rvert \le 1mA$			3			3		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1282A/LTC1282B MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.7V	●			0.45	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 2.7V $I_O = -10\mu A$ $I_O = -200\mu A$	 ●	 2.3	2.6		 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.7V $I_O = 160\mu A$ $I_O = 1.6mA$	 ●		0.05 0.10	 0.4	 V V
I_{OZ}	High Z Output Leakage D11-D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High Z Output Capacitance D11-D0/8	$\overline{CS}$ High (Note 12)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−4.5		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{DD}$			4.5		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1282A/LTC1282B MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 13)		2.70		3.60	V
V_{SS}	Negative Supply Voltage	Bipolar Operation (Note 13)		−2.50		−3.60	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 140ksps	●		4	7.8	mA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 140ksps	●		0.03	0.15	mA
P_D	Power Dissipation	f_{SAMPLE} = 140ksps	●		12	24	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1282A/LTC1282B MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	Commercial (Note 13)	●	140			kHz
		Military (Note 13)	●	120			kHz
t_{CONV}	Conversion Time	Commercial	●			6.0	µs
		Military	●			6.5	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time		●	0			ns
t_2	$\overline{RD}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 50pF			140	200	ns
		Commercial	●			230	ns
		Military	●			260	ns
t_3	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 13)			100	180	ns
		Commercial	●			200	ns
		Military	●			220	ns
		C_L = 100pF (Note 13)			110	200	ns
		Commercial	●			240	ns
		Military	●			260	ns
t_4	$\overline{RD}$ Pulse Width	(Note 13)	●	t_3			ns
t_5	$\overline{CS}$ to $\overline{RD}$ Hold Time	(Note 13)	●	0			ns
t_6	Data Setup Time After $\overline{BUSY}\uparrow$	(Note 13)			60	85	ns
		Commercial	●			110	ns
		Military	●			120	ns
t_7	Bus Relinquish Time	(Note 13)		40	60	120	ns
		Commercial	●	40		130	ns
		Military	●	40		150	ns
t_8	HBEN to $\overline{RD}$ Setup Time	(Note 13)	●	0			ns
t_9	HBEN to $\overline{RD}$ Hold Time	(Note 13)	●	0			ns
t_{10}	Delay Between $\overline{RD}$ Operations		●	40			ns
t_{11}	Delay Between Conversions	Commercial (Note 13)	●	1000	450		ns
		Military (Note 13)	●	1500			ns
t_{12}	Aperture Delay of Sample-and-Hold				30		ns

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 3V, V_{SS} = 0V for unipolar mode and V_{SS} = −3V for bipolar mode, f_{SAMPLE} = 140kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the different voltage measured from −1/2LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Full scale change when V_{SS} = 0V (Unipolar Mode) or −3V (Bipolar Mode).

Note 10: Full scale change when V_{DD} = 3V.

Note 11: The LTC1282 can perform unipolar and bipolar conversions. When V_{SS} is grounded (i.e. $-0.1V \le V_{SS}$), the ADC will convert in unipolar mode with input voltage of 0V to 2.5V. When V_{SS} is taken negative (i.e. $V_{SS} \le -2.5V$), the ADC will convert in bipolar mode with an input voltage of ±1.25V. A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy.

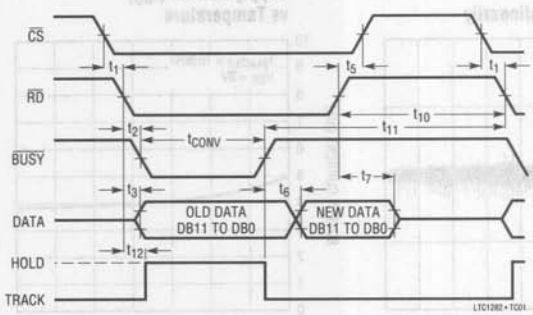
Note 12: Guaranteed by design, not subject to test.

Note 13: Recommended operating conditions.

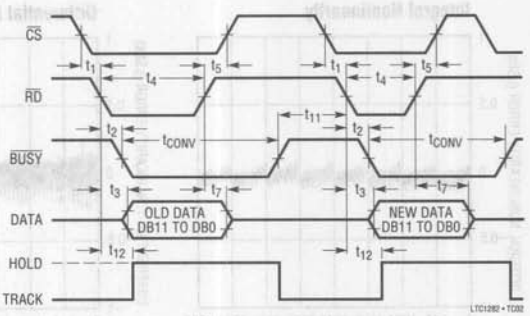
Note 14: Commercial grade parts are designed to operate over the temperature range of −40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over −40°C to 85°C are available on special request. Consult factory.

TIMING CHARACTERISTICS (Note 5)

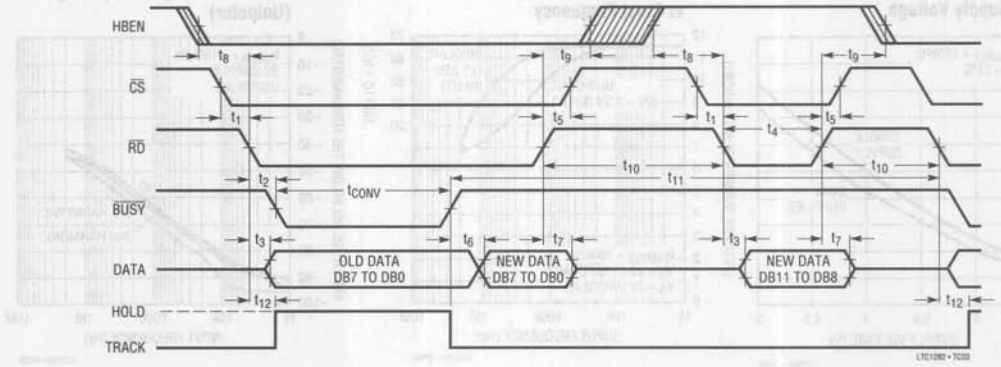
Slow Memory Mode, Parallel Read Timing Diagram



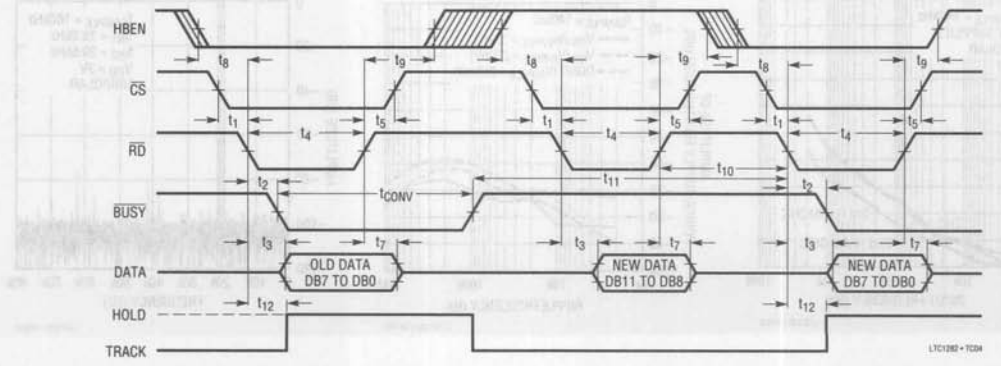
ROM Mode, Parallel Read Timing Diagram



Slow Memory Mode, Two Byte Read Timing Diagram

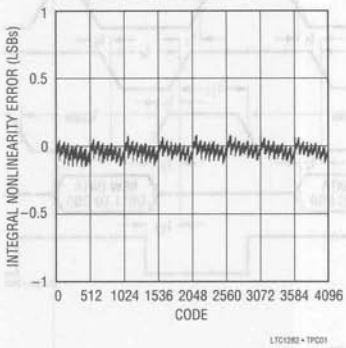


ROM Mode, Two Byte Read Timing Diagram

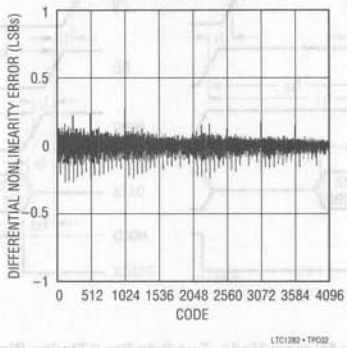


TYPICAL PERFORMANCE CHARACTERISTICS

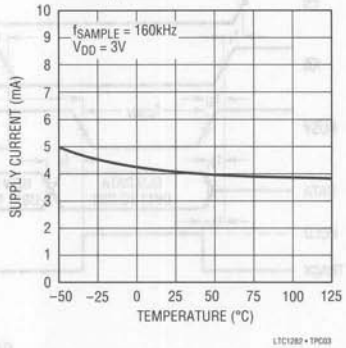
Integral Nonlinearity



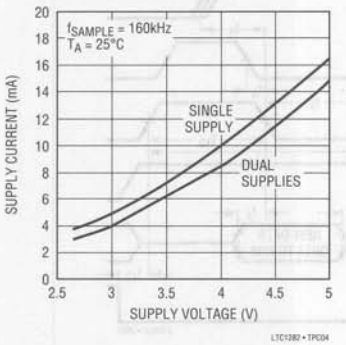
Differential Nonlinearity



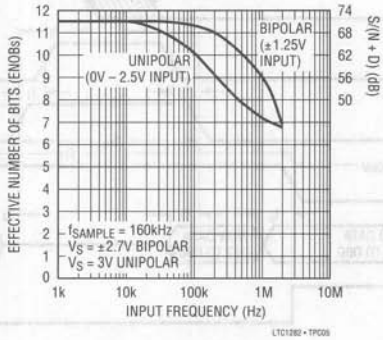
Supply Current (I_{DD}) vs Temperature



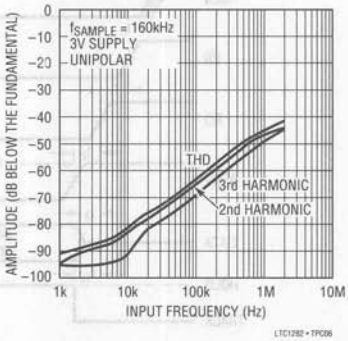
Supply Current (I_{DD}) vs Supply Voltage



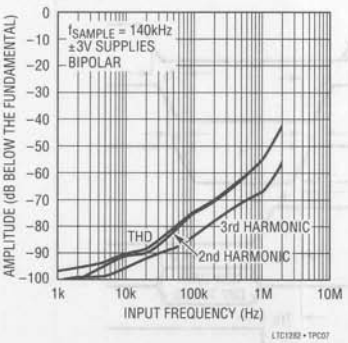
ENOBs and S/(N + D) vs Input Frequency



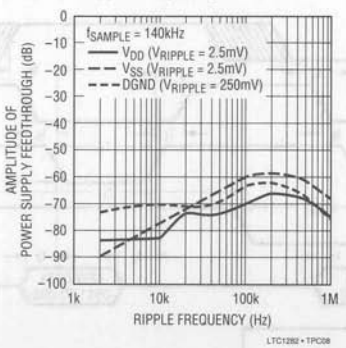
Distortion vs Input Frequency (Unipolar)



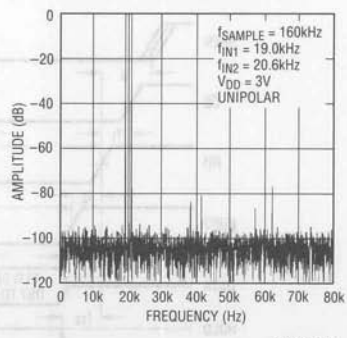
Distortion vs Input Frequency (Bipolar)



Power Supply Feedthrough vs Ripple Frequency

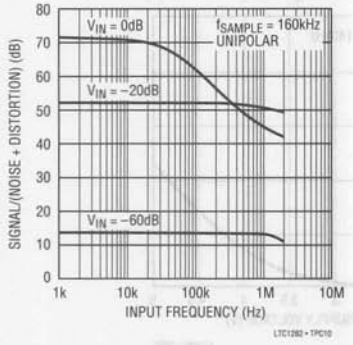


Intermodulation Distortion Plot

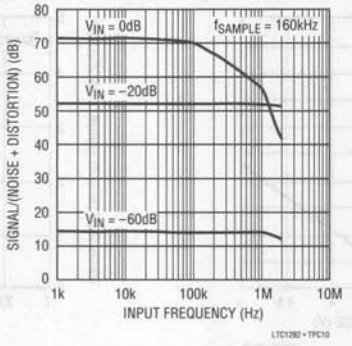


TYPICAL PERFORMANCE CHARACTERISTICS

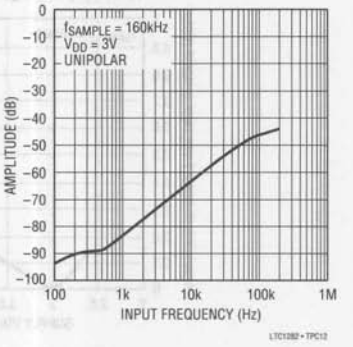
S/(N + D) vs Input Frequency and Amplitude (Unipolar, V_{DD} = 3V)



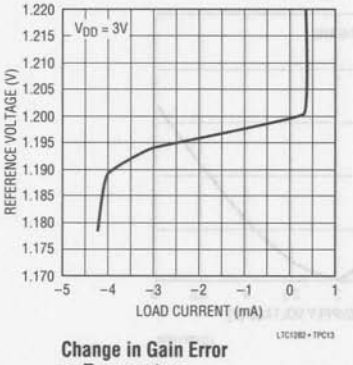
S/(N + D) vs Input Frequency and Amplitude (Bipolar, ±3V Supplies)



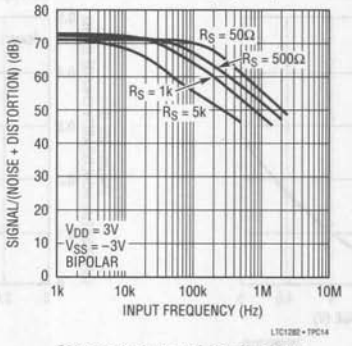
Spurious Free Dynamic Range vs Input Frequency



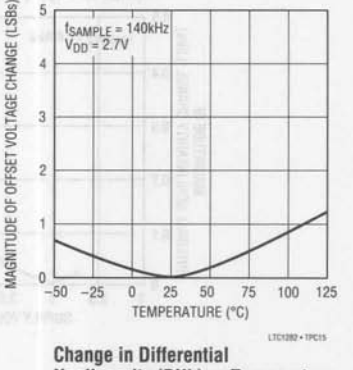
Reference Voltage vs Load Current



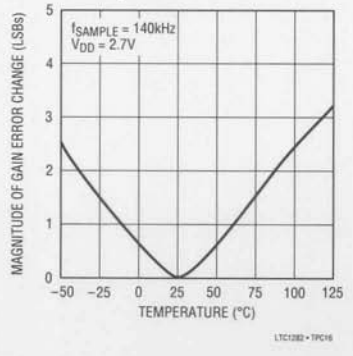
S/(N +D) vs Input Frequency vs Source Resistance (Bipolar)



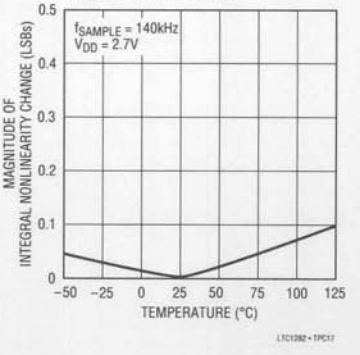
Change in Offset Voltage vs Temperature



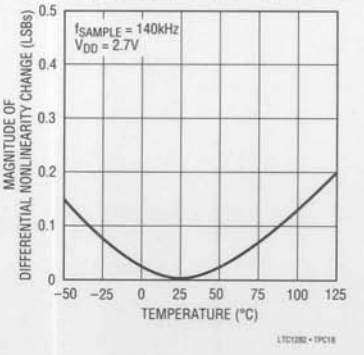
Change in Gain Error vs Temperature



Change in Integral Nonlinearity (INL) vs Temperature



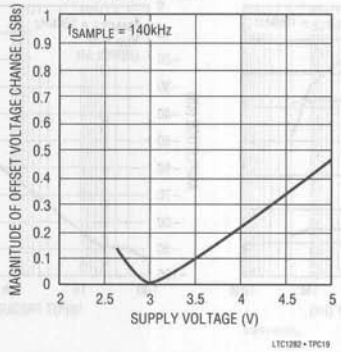
Change in Differential Nonlinearity (DNL) vs Temperature



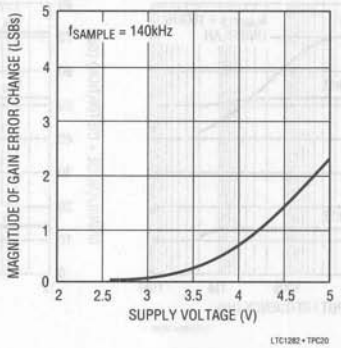
6

TYPICAL PERFORMANCE CHARACTERISTICS

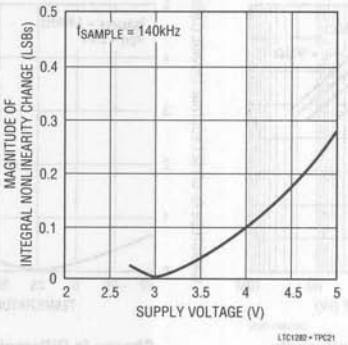
Change in Offset Voltage vs Supply Voltage



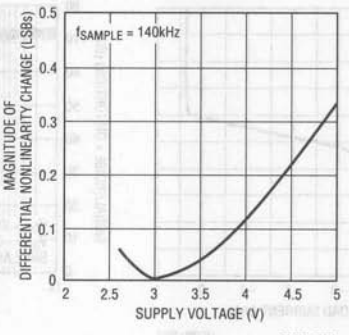
Change in Gain Error vs Supply Voltage



Change in Integral Nonlinearity (INL) vs Supply Current



Change in Differential Nonlinearity (DNL) vs Supply Current



PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 2.5V (Unipolar), ±1.25V (Bipolar).

V_{REF} (Pin 2): +1.20V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11-D4 (Pins 4 to 11): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3/11-D0/8 (Pins 13 to 16): Three-State Data Outputs.

NC (Pins 17 and 18): No Connection.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7 and D0/8). See Table 1. HBEN also disables conversion start when HIGH.

$\overline{RD}$ (Pin 20): READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output shows the converter status. It is low when a conversion is in progress.

V_{SS} (Pin 23): Bipolar Mode — Negative Supply, –3V. Bypass to AGND with 0.1µF ceramic.

Unipolar Mode — Tie to DGND.

V_{DD} (Pin 24): Positive Supply, 3V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

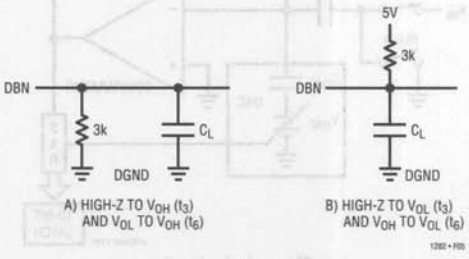
	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

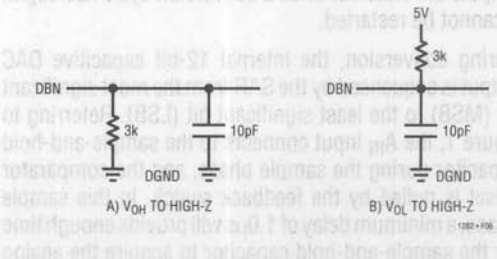
6

TEST CIRCUITS

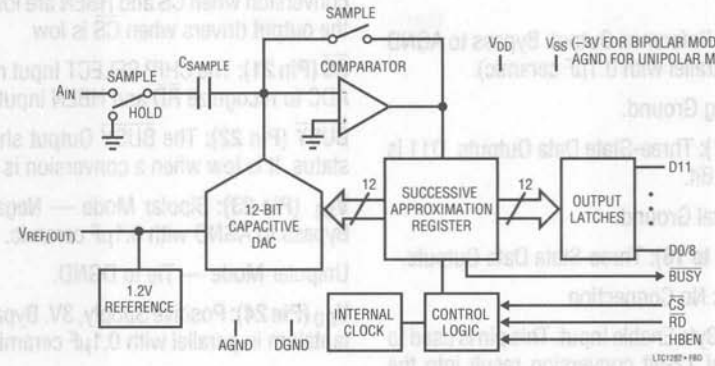
Load Circuits for Access Time



Load Circuits for Output Float Delay



FUNTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1282 uses a successive approximation and an internal sample-and-hold circuitry to convert an analog signal to a 12-bit parallel or 2-byte output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. Please refer to the Digital Interface section for the data format.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the sample phase, and the comparator offset is nulled by the feedback switch. In this sample phase, a minimum delay of 1.0µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge to the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit latch.

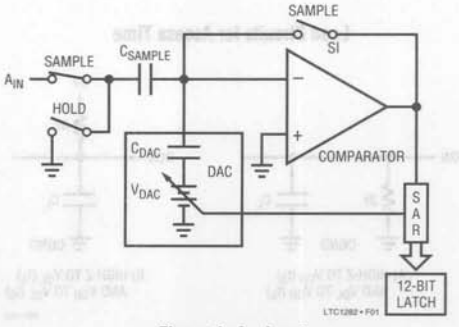


Figure 1. A_{IN} Input

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

The LTC1282 has exceptionally high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1282 FFT plot.

Signal-to-(Noise + Distortion) Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical LTC1282 FFT plot.

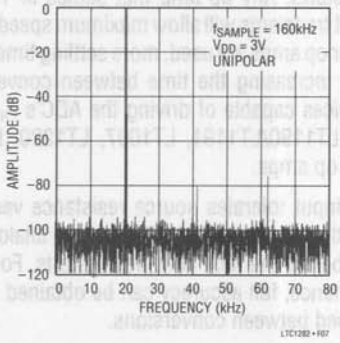


Figure 2. LTC1282 Nonaveraged, 1024 Point FFT Plot

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 140kHz the LTC1282 maintains 11.3 ENOBs at 70kHz input frequency. Refer to Figure 3.

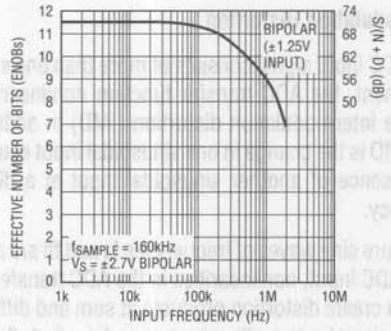


Figure 3. ENOBs and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 70kHz input signal, the LTC1282 has a typical –82dB THD as shown in Figure 4.

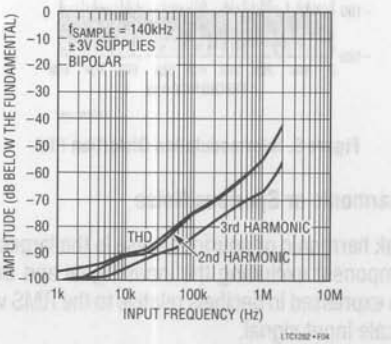


Figure 4. Distortion vs Input Frequency (Bipolar)

APPLICATIONS INFORMATION

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb) if the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order. IMD products can be expressed by the following formula:

$$\text{IMD (fa} \pm \text{fb)} = 20\log\frac{\text{Amplitude at (fa} \pm \text{fb)}}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 20kHz input.

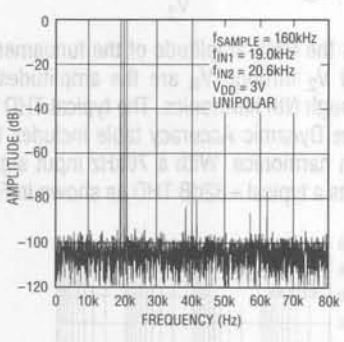


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1282 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency.

Driving the Analog Input

The analog input of the LTC1282 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 1.0µs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT1190/LT1191, LT1007, LT1220, LT1223 and LT1224 op amps.

The analog input tolerates source resistance very well. Here again, the only requirement is that the analog input must settle before the next conversion starts. For larger source resistance, full accuracy can be obtained if more time is allowed between conversions.

Internal Reference

The LTC1282 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 1.20V. It is internally connected to the DAC and is available at pin 2 to provide up to 0.3mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

APPLICATIONS INFORMATION

Overdriving the Internal Reference

The V_{REF} pin can be driven above its normal value with a DAC or other means to provide input span adjustment. Figure 6 shows an LT1006 op amp driving the reference pin. The V_{REF} pin must be driven to at least 1.25V to prevent conflict with the internal reference. The reference should be driven to no more than 1.44V in unipolar mode or 2.88V for bipolar mode to keep the input span within the single 3V or ±3V supplies.

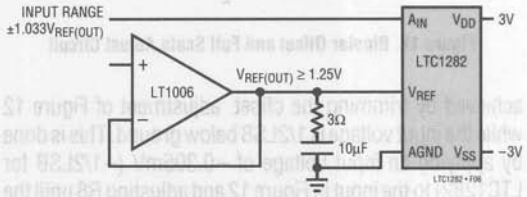


Figure 6. Driving the V_{REF} with the LT1006 Op Amp

Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1282 operating in bipolar mode. This will provide an improved drift (due to the 5ppm/°C of the LT1019A-2.5) and a ±2.604V full scale.

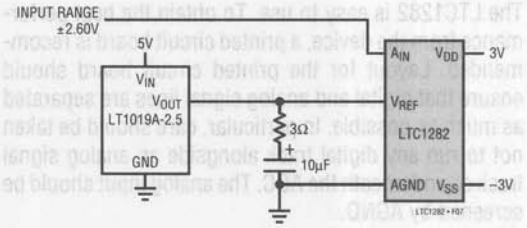


Figure 7. Supplying a 2.5V Reference Voltage to the LTC1282 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1282. The code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 1 1/2LSBs, 2 1/2LSBs, FS – 1 1/2LSBs). The output code is natural binary with 1LSB = FS/4096 = 2.5V/4096 = 0.61mV. Figure 9 shows the input/output transfer characteristics for the LTC1282 in bipolar operation. The full scale for LTC1282 in bipolar mode is still 2.5V and 1LSB = 0.61mV.

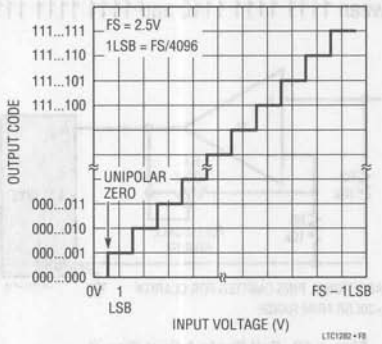


Figure 8. LTC1282 Unipolar Transfer Characteristic

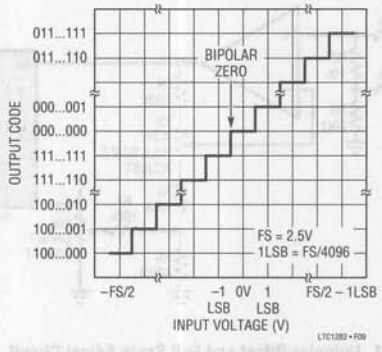


Figure 9. LTC1282 Bipolar Transfer Characteristic

Unipolar Offset and Full Scale Adjustment

In applications where absolute accuracy is important, offset and full scale errors can be adjusted to zero. Figure 10 shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 11 can be used. Offset should be adjusted before full scale. To adjust offset,

APPLICATIONS INFORMATION

apply 0.305mV (i.e., 1/2LSB) at V1 and adjust the op amp offset voltage until the LTC1282 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full scale error, apply an analog input of 2.49909V (i.e., FS – 1 1/2LSBs or last code transition) at the input and adjust the full scale trim until the LTC1282 output code flickers between 1111 1111 1110 and 1111 1111 1111.

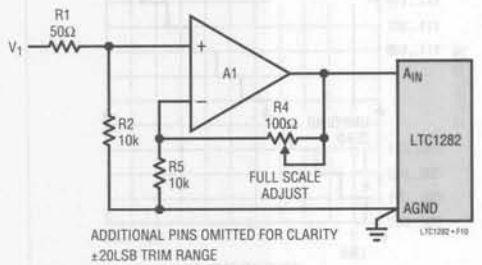


Figure 10. Full Scale Adjust Circuit

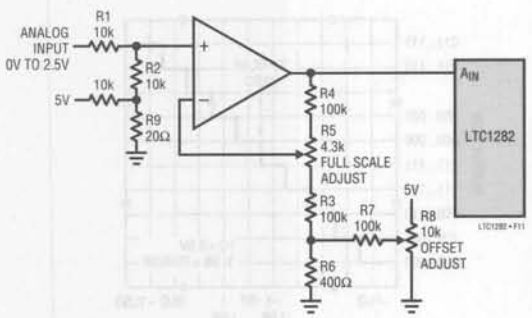


Figure 11. Unipolar Offset and Full Scale Adjust Circuit

Bipolar Offset and Full Scale Adjustment

Bipolar offset and full scale errors are adjusted in a similar fashion to the unipolar case. Figure 10 shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 12 can be used. Again, bipolar offset must be adjusted before full scale error. Bipolar offset error adjustment is

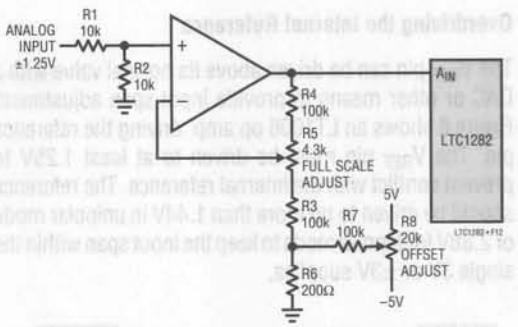


Figure 12. Bipolar Offset and Full Scale Adjust Circuit

achieved by trimming the offset adjustment of Figure 12 while the input voltage is 1/2LSB below ground. This is done by applying an input voltage of –0.305mV (–1/2LSB for LTC1282) to the input in Figure 12 and adjusting R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 1.24909V (FS – 3/2LSBs for LTC1282) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

The LTC1282 is easy to use. To obtain the best performance from the device, a printed circuit board is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 13. In bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

APPLICATIONS INFORMATION

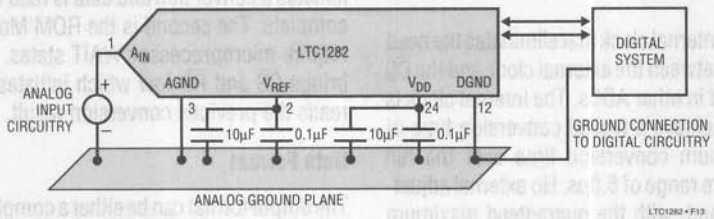


Figure 13. Power Supply Grounding Practice

Noise: Input signal leads to A_{IN} and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the ADC, as shown in Figure 13. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADC is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally either connected to the microprocessor address bus or grounded.

Connecting to 5V Logic Systems

The LTC1282 interfaces well to 5V logic because the ESD clamps on the inputs do not clamp to the positive supply (see Figure 14). Inputs of 0V to 5V do not bother the ADC at all. In addition, the 0V to 3V outputs of the 3V ADC are more than adequate to meet TTL input levels in the 5V logic. (5V logic with CMOS input levels requires a level shift.)

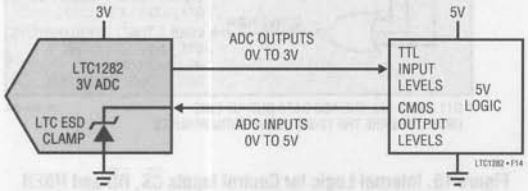


Figure 14. 3V ADC ESD Protection Handles 0V to 5V Swings Easily

APPLICATIONS INFORMATION

Internal Clock

The LTC1282 has an internal clock that eliminates the need for synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 5.5µs, and a maximum conversion time over the full operating temperature range of 6.0µs. No external adjustments are required and, with the guaranteed maximum acquisition time of 1.0µs, throughput performance of 140ksps is assured.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 15 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

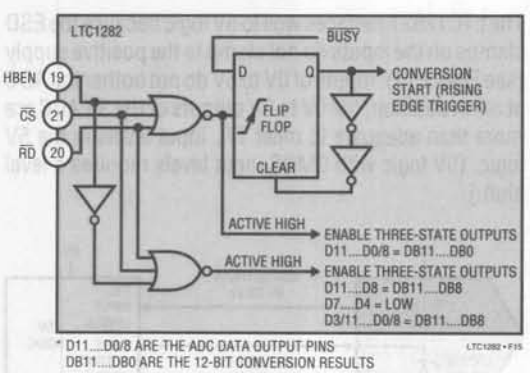


Figure 15. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

There are two modes of operation as outlined by the timing diagrams of Figures 16 to 19. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

Data Format

The output format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7...D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7...D0/8 outputs (4MSBs or 8MSBs) where it can be read in two read cycles. The 4MSBs always appear on D11...D8 whenever the three-state output drivers are turned on.

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 16 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low trigger a conversion and the ADC acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11...D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only 8 data outputs D7...D0/8 are used. Conversion start procedure and data output status for the first read operation are identical to Slow Memory Mode, Parallel Read. See Figure 17 timing diagram and Table 3 data bus status. At the end of the conversion, the low data byte (D7...D0/8) is read from the ADC. A second READ operation with the HBEN high, places the high byte on data outputs D3/11...D0/8 and disables conversion start. Note the 4MSBs appear on data output D11...D8 during the two READ operations.

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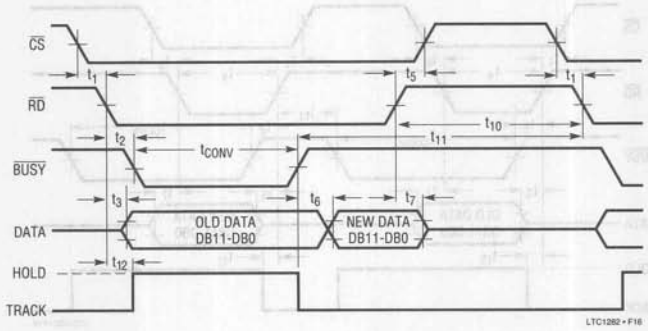

Figure 16. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

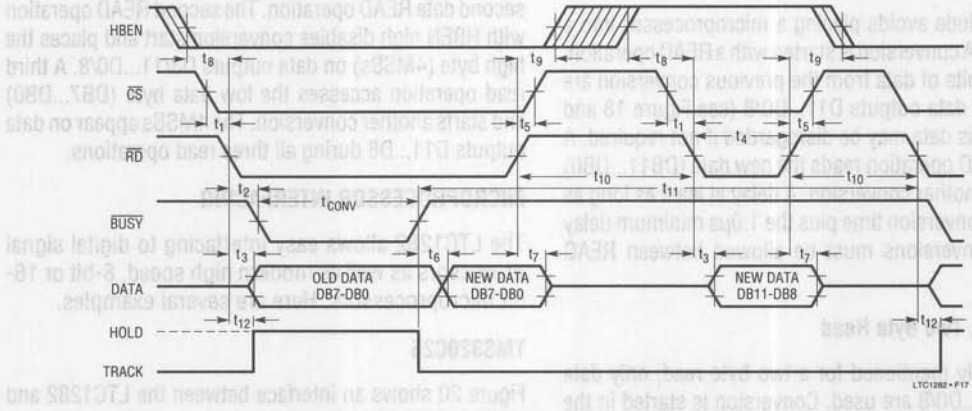

Figure 17. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

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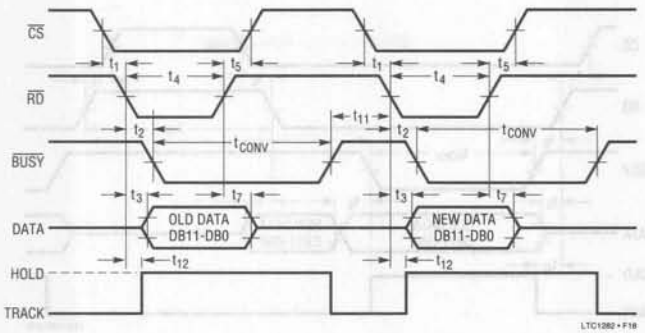


Figure 18. ROM Mode, Parallel Read Timing Diagram (HBEN = LOW)

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

ROM Mode, Parallel Read (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a WAIT state. A conversion is started with a READ operation, and the 12 bits of data from the previous conversion are available on data outputs D11...D0/8 (see Figure 18 and Table 4). This data may be disregarded if not required. A second READ operation reads the new data (DB11...DB0) and starts another conversion. A delay at least as long as the ADC's conversion time plus the 1.0µs minimum delay between conversions must be allowed between READ operations.

ROM Mode, Two Byte Read

As previously mentioned for a two byte read, only data outputs D7...D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM mode, Parallel Read (see Figure 19 timing diagram and Table 5 data bus status). Two more READ operations are required to access the new conversion result. A delay equal to the ADC's conversion time must be allowed between conversion start and the second data READ operation. The second READ operation with HBEN high disables conversion start and places the high byte (4MSBs) on data outputs D3/11...D0/8. A third read operation accesses the low data byte (DB7...DB0) and starts another conversion. The 4MSBs appear on data outputs D11...D8 during all three read operations.

MICROPROCESSOR INTERFACING

The LTC1282 allows easy interfacing to digital signal processors as well as modern high speed, 8-bit or 16-bit microprocessors. Here are several examples.

TMS320C25

Figure 20 shows an interface between the LTC1282 and the TMS320C25.

The R/$\overline{W}$ signal of the DSP initiates a conversion and conversion results are read from the LTC1282 using the following instruction:

```
IN      D, PA
```

APPLICATIONS INFORMATION

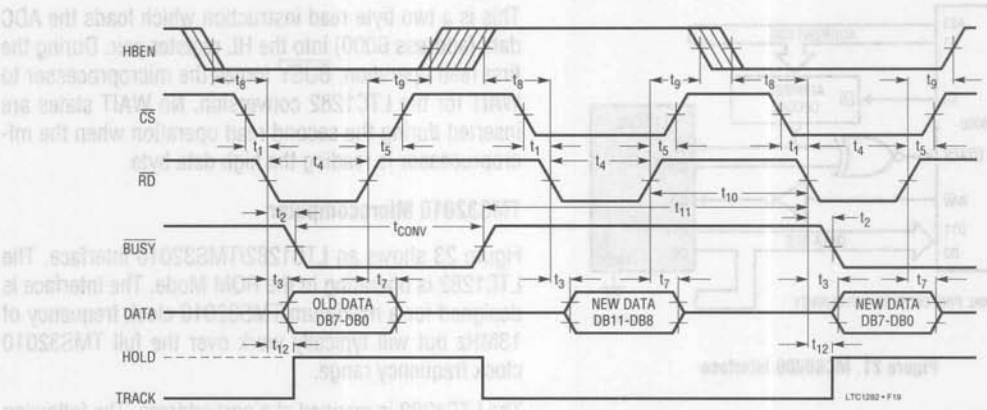


Figure 19. ROM Mode Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read (New Data)	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read (New Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

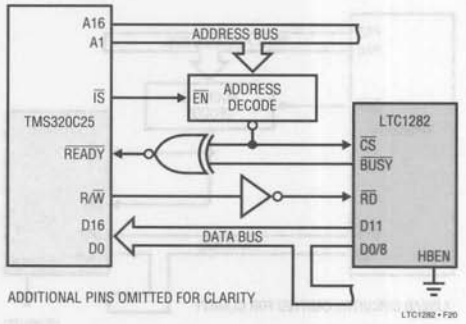


Figure 20. TMS320C25 Interface

where D is Data Memory Address and PA is the PORT ADDRESS.

MC68000 Microprocessor

Figure 21 shows a typical interface for the MC68000. The LTC1282 is operating in the Slow Memory Mode. Assuming the LTC1282 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result:

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$ so that the MC68000 is forced into a WAIT state. At the end of conversion, $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the microprocessor.

APPLICATIONS INFORMATION

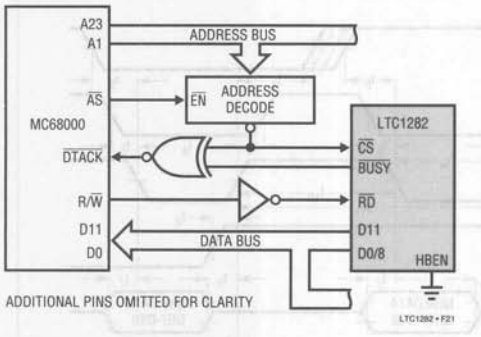


Figure 21. MC68000 Interface

8085A/Z80 Microprocessor

Figure 22 shows an LTC1282 interface for the Z80 and 8085A. The LTC1282 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN so that an even address (HBEN = LOW) to the LTC1282 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A LHLD (B000)
For the Z80 LDHL, (B000)

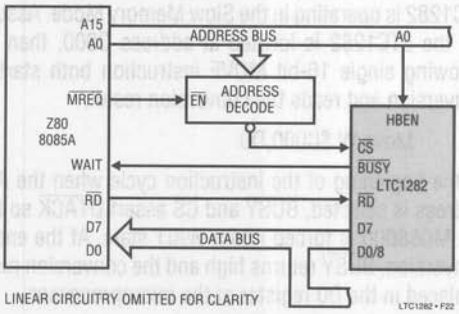


Figure 22. 8085A and Z80 Interface

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the LTC1282 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 23 shows an LTC1282/TMS32010 interface. The LTC1282 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The LTC1282 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

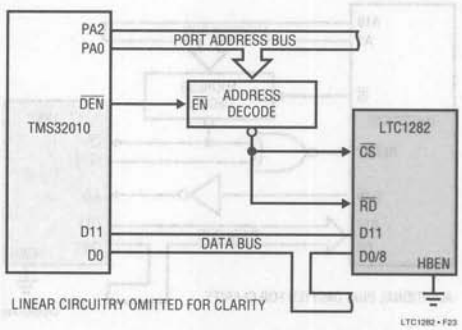


Figure 23. TMS32010 Interface

APPLICATIONS INFORMATION

MUXing with CD4051

The high input impedance of the LTC1282 provides an easy, cheap, fast, and accurate way to multiplex many channels of data through one converter. Figure 24 shows a low cost CD4051, one of the most common multiplexers connected to the LTC1282. The LTC1282's input draws no DC input current so it can be accurately driven by the unbuffered MUX. The CD4520 counter increments the MUX channel after each sample is taken.

100ps Resolution ΔTime Measurement with LTC1282

Figure 25 shows a circuit that precisely measures the difference in time between two events. It has a 400ns full scale and 100ps resolution. The start signal releases the ramp generator made up of the PNP current source and the 500pF capacitor. The circuit ramps until the stop signal shuts off the current source. The final value of the ramp represents the time between the start and stop events. The LTC1282 digitizes this final value and outputs the digital data.

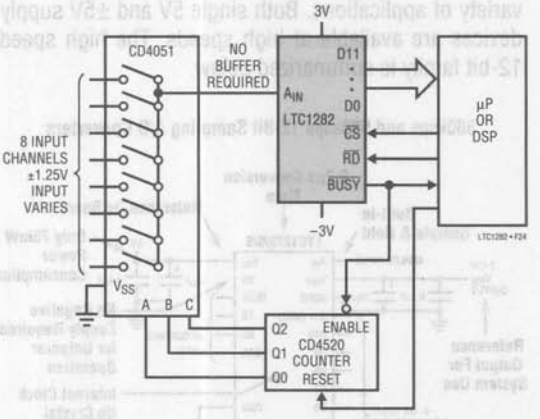


Figure 24. MUXing the LTC1282 with CD4051

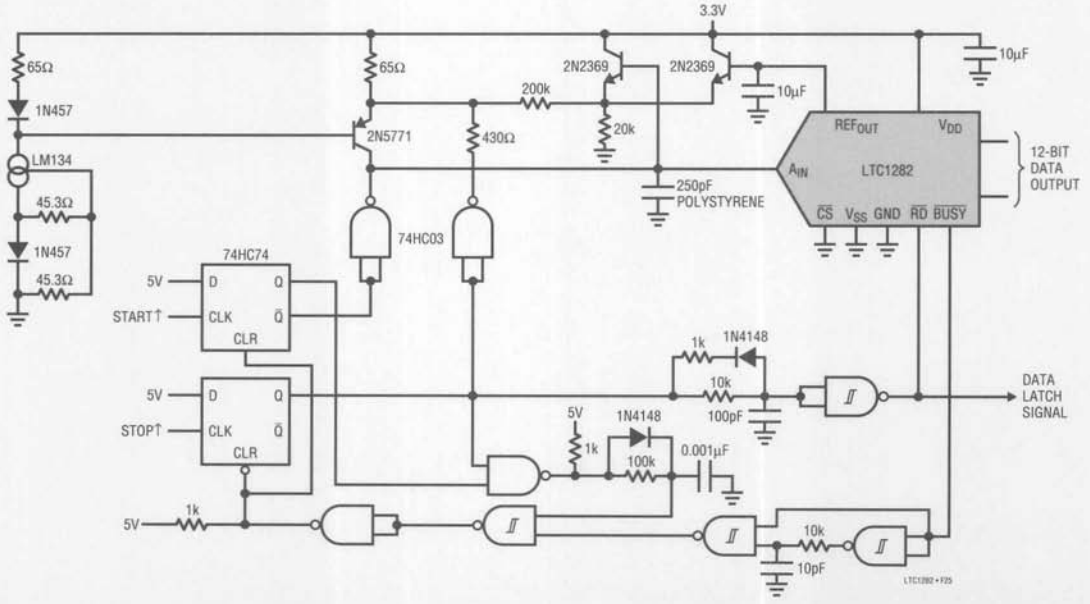


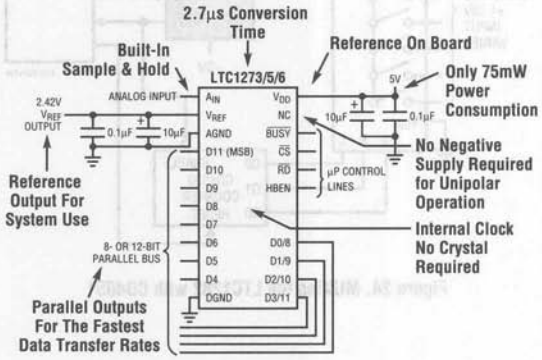
Figure 25. Δ Time Measurement with the LTC1282

APPLICATIONS INFORMATION

Other High Speed A/D Converters

LTC makes a family of high speed sampling ADCs for a variety of applications. Both single 5V and ±5V supply devices are available at high speeds. The high speed 12-bit family is summarized below.

300ksps and 500ksps 12-Bit Sampling A/D Converters



Comparison of Specifications and Features

DEVICE TYPE	SAMPLING FREQ	S/(N + D) @ NYQUIST	INPUT RANGE	POWER SUPPLY	POWER DISSIPATION
LTC1272	250kHz	65dB	0V-5V	5V	75mW
LTC1273	300kHz	70dB	0V-5V	5V	75mW
LTC1275	300kHz	70dB	±2.5V	±5V	75mW
LTC1276	300kHz	70dB	±5V	±5V	75mW
LTC1278	500kHz	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 6mW*
LTC1282	**140kHz**	**68dB**	**0V-2.5V or ±1.25V**	**3V or ±3V**	**12mW**

*6mW power shutdown with instant wake up

3V Single Chip 10-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V or ±3.3V Operation
- Software Programmable Features:
  - Unipolar/Bipolar Conversions
  - 4 Differential/8 Single-Ended Inputs
  - MSB- or LSB-First Data Sequence
  - Variable Data Word Length
- Built-In Sample-and-Hold
- Direct 4-Wire Interface to Most MPU Serial Ports and all MPU Parallel Ports
- 15kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Minimum Guaranteed Supply Voltage: 3V
- Resolution: 10 Bits
- Offset Error: ±0.5LSB Max
- Linearity Error: ±0.5LSB Max
- Gain Error (LTC1283A): ±1LSB Max
- Conversion Time: 44µs
- Supply Current: 350µA Max, 150µA Typ

DESCRIPTION

The LTC1283 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 10-bit unipolar, or 9-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single-ended or differential inputs (or combinations thereof). An on-chip sample-and-hold is included for all single-ended input channels.

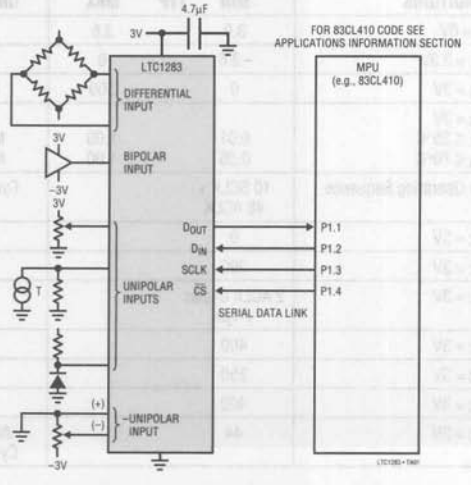
The serial I/O is designed to be compatible with industry-standard full-duplex serial interfaces. It allows either MSB- or LSB-first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8-, 10-, 12-, or 16-bit. This allows easy interface to shift registers and a variety of processors.

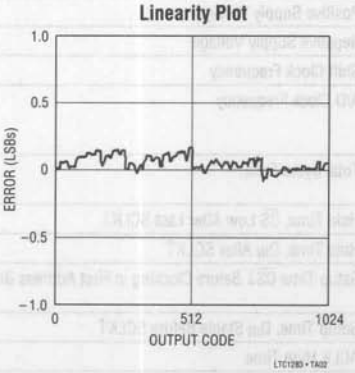
Both the LTC1283A and LTC1283 are specified with offset and linearity errors less than ±0.5LSB. The LTC1283A has a gain error limit of ±1LSB. The 1283 is specified with a gain error limit of ±2LSB for applications where gain is adjustable or less critcial.

LTCMOS is a trademark of Linear Technology Corp.

6

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Voltage
  Analog and Reference
  Inputs ..... (V^-) –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 12V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V
Negative Supply Voltage (V–) ..... –6V to GND
Power Dissipation 500mW
Operating Temperature
  LTC1283AC, LTC1283C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

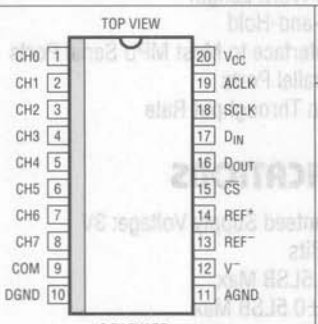
PACKAGE/ORDER INFORMATION

N PACKAGE
20-LEAD PLASTIC DIP

$T_{J\,MAX}$ = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LTC1283ACN
LTC1283CN



S PACKAGE
20-LEAD PLASTIC SOL

$T_{J\,MAX}$ = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1283ACS
LTC1283CS

Consult factory for Industrial and Military grade parts

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1283/LTC1283A MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	V^- = 0V	3.0		3.6	V
V^-	Negative Supply Voltage	V_{CC} = 3.3V	–3.6		0	V
f_{SCLK}	Shift Clock Frequency	V_{CC} = 3V	0		500	kHz
f_{ACLK}	A/D Clock Frequency	V_{CC} = 3V $T_A \le 25°C$ $T_A \le 70°C$	 0.01 0.05		 1.00 1.00	 MHz MHz
t_{CYC}	Total Cycle Time	See Operating Sequence	10 SCLK + 48 ACLK			Cycles
$t_{h\overline{CS}}$	Hold Time, $\overline{CS}$ Low After Last SCLK↓	V_{CC} = 3V	0			ns
t_{hDI}	Hold Time, D_{IN} After SCLK↑	V_{CC} = 3V	200			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before Clocking in First Address Bit (Note 8)	V_{CC} = 3V	2 ACLK Cycles + 1µs			
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK↑	V_{CC} = 3V	400			ns
t_{WHACLK}	ACLK High Time	V_{CC} = 3V	250			ns
t_{WLACLK}	ACLK Low Time	V_{CC} = 3V	400			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 3V	44			ACLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1283A MIN	LTC1283A TYP	LTC1283A MAX	LTC1283 MIN	LTC1283 TYP	LTC1283 MAX	UNITS
Offset Error	(Note 4)	●			±0.5			±0.5	LSB
Linearity Error	(Notes 4 and 5)	●			±0.5			±0.5	LSB
Gain Error	(Note 4)	●			±1.0			±2.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			10			10	Bits
Reference Input Resistance				10			10		kΩ
Analog and REF Input Range	(Note 6)			$(V^-) - 0.05V$ to $V_{CC} + 0.05V$					V
On Channel Leakage Current (Note 7)	On Channel = 3V Off Channel = 0V	●			1			1	µA
	On Channel = 0V Off Channel = 3V	●			–1			–1	µA
Off Channel Leakage Current (Note 7)	On Channel = 3V Off Channel = 0V	●			–1			–1	µA
	On Channel = 0V Off Channel = 3V	●			1			1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	LTC1283/LTC1283A TYP	LTC1283/LTC1283A MAX	UNITS
t_{ACC}	Delay Time From $\overline{CS}\downarrow$ to D_{OUT} Data Valid	(Note 8)			2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			5		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			44		ACLK Cycles
t_{dDO}	Delay Time, SCLK↓ to D_{OUT} Data Valid	See Test Circuits	●		400	900	ns
t_{dis}	Delay Time, $\overline{CS}\uparrow$ to D_{OUT} Hi-Z	See Test Circuits	●		240	500	ns
t_{en}	Delay Time, 2nd CLK↓ to D_{OUT} Enabled	See Test Circuits	●		300	800	ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				75		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel Digital Inputs			65 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	LTC1283/LTC1283A TYP	LTC1283/LTC1283A MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{CC} = 3.6V$	●	1.7			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 3V$	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●			–2.5	µA
V_{OH}	High Level Output Voltage	$V_{CC} = 3V$, $I_O = -20\mu A$ $I_O = -200\mu A$	 ●	2.6 2.0	2.8		V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 3V$, $I_O = 20\mu A$ $I_O = 400\mu A$	 ●		0.05 0.10	 0.30	V V

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DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	TYP	MAX	UNITS
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High $V_{OUT} = 0V$, $\overline{CS}$ High	● ●			3 −3	µA µA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			−4.5		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			4.5		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, REF^+ Open	●		150	350	µA
I_{REF}	Reference Current	$V_{REF} = 2.5V$	●		250	500	µA
I^-	Negative Supply Current	$\overline{CS}$ High, $V^- = -3V$	●		−1	−50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND and REF^- wired together (unless otherwise noted).

Note 3: $V_{CC} = 3V$, $V_{REF^+} = 2.5V$, $V_{REF^-} = 0V$, $V^- = 0V$ for unipolar mode and −3V for bipolar mode, ACLK = 1MHz, SCLK = 0.25MHz unless otherwise specified.

Note 4: These specifications apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when $V_{REF} = 2.5V$, 1LSB (bipolar) = 2(2.5V)/1024 = 4.88mV.

Note 5: Linearity error is the deviation from ideal of the slope between the two end points of the transfer curve.

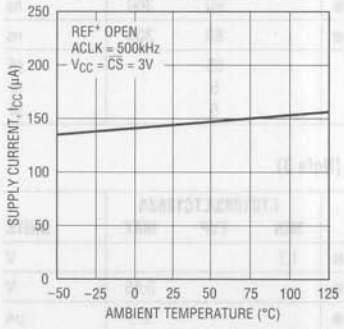
Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level reference or analog inputs can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 7: Channel leakage current is measured after the channel selection.

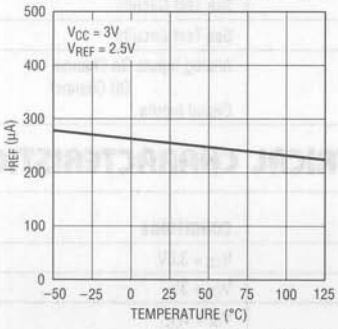
Note 8: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

TYPICAL PERFORMANCE CHARACTERISTICS

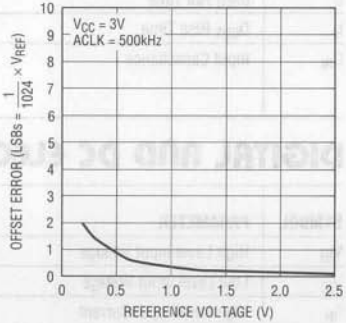
Supply Current vs Temperature



Reference Current vs Temperature

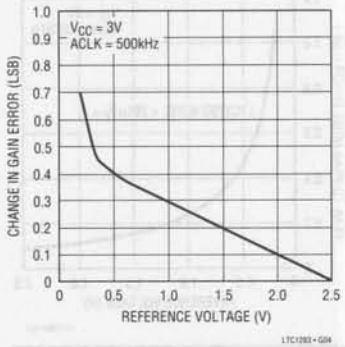


Unadjusted Offset Error vs Reference Voltage

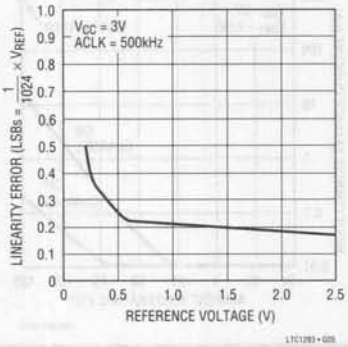


TYPICAL PERFORMANCE CHARACTERISTICS

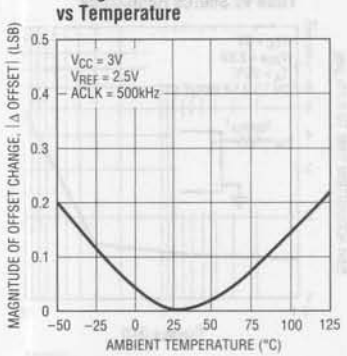
Change in Full-Scale Error vs Reference Voltage



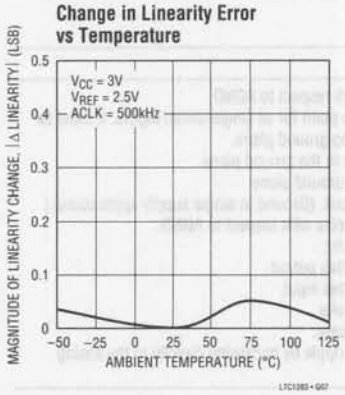
Linearity Error vs Reference Voltage



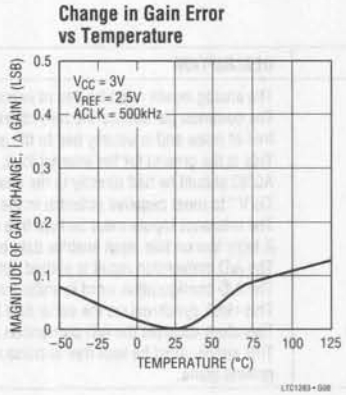
Change in Offset Error vs Temperature



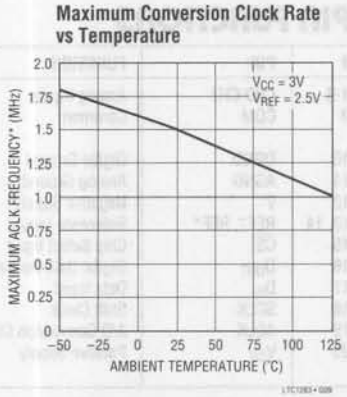
Change in Linearity Error vs Temperature



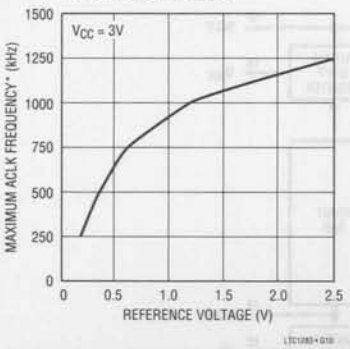
Change in Gain Error vs Temperature



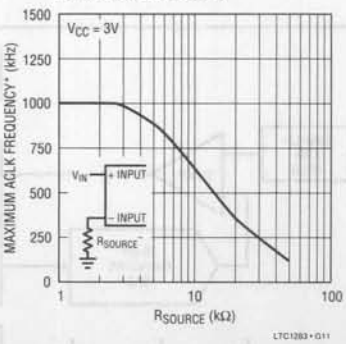
Maximum Conversion Clock Rate vs Temperature



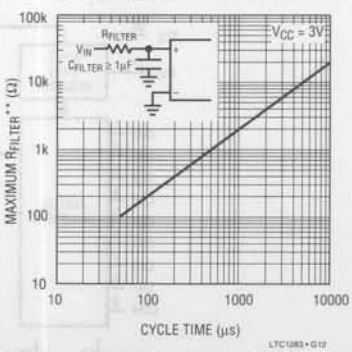
Maximum Conversion Clock Rate vs Reference Voltage



Maximum Conversion Clock Rate vs Source Resistance



Maximum Filter Resistor vs Cycle Time



*Maximum ACLK frequency represents the ACLK frequency at which a 0.1LSB shift in the error at any code transition from its 100kHz value is first detected.

**Maximum R_{FILTER} represents the filter resistor value at which a 0.1LSB change in full-scale error from its value at R_{FILTER} = 0 is first detected.

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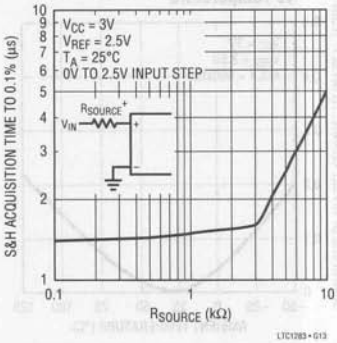
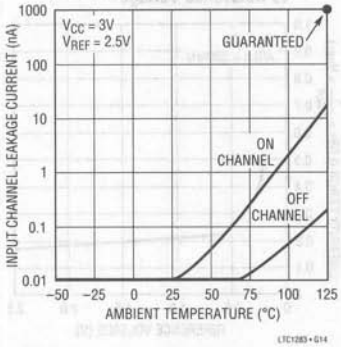
TYPICAL PERFORMANCE CHARACTERISTICS

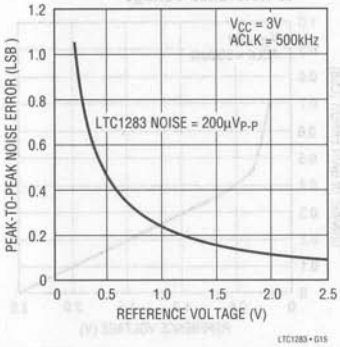
Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



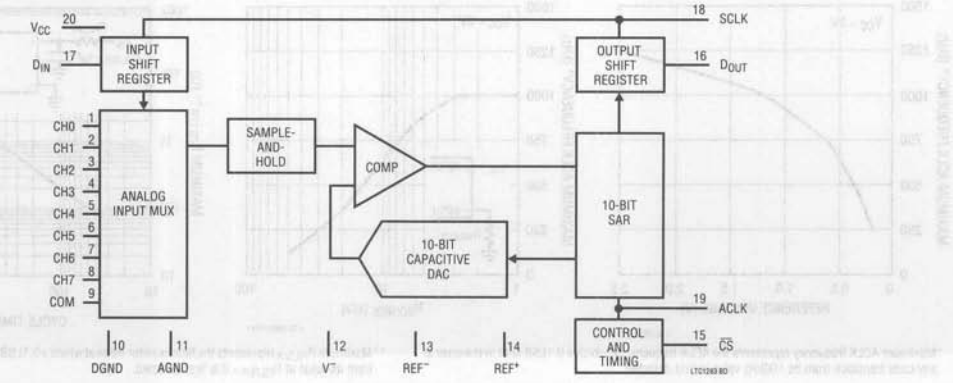
Noise Error vs Reference Voltage



PIN FUNCTIONS

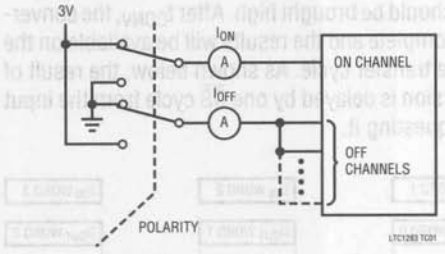
#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	$\overline{REF}^-$, REF^+	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND.
15	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

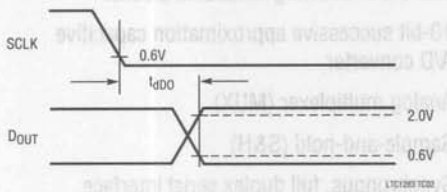


TEST CIRCUITS

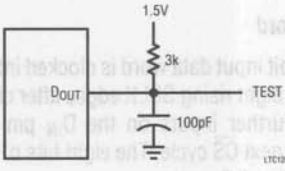
On and Off Channel Leakage Current



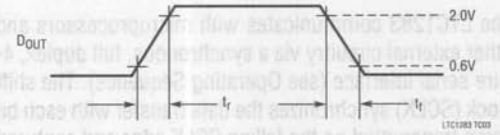
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



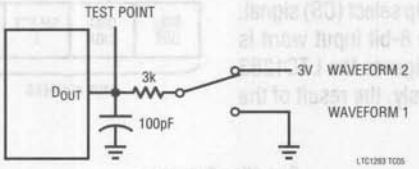
Load Circuit for t_{dDO}, t_r, t_f and t_{en}



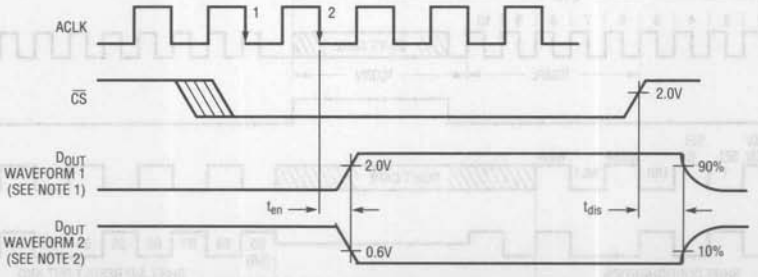
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r and t_f



Load Circuit for t_{dis}



Voltage Waveforms for t_{en} and t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1283 TC04

6

APPLICATIONS INFORMATION

The LTC1283 is a 3V data acquisition component which contains the following functional blocks:

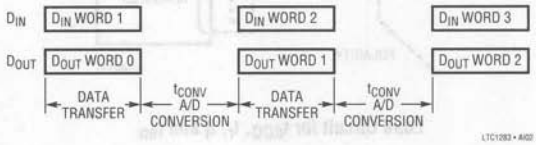
1. 10-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S&H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

1. Serial Interface

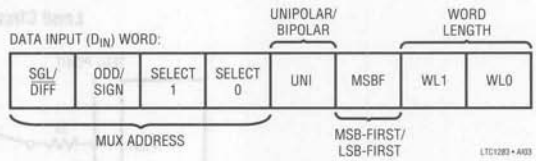
The LTC1283 communicates with microprocessors and other external circuitry via a synchronous, full duplex, 4-wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1283 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.

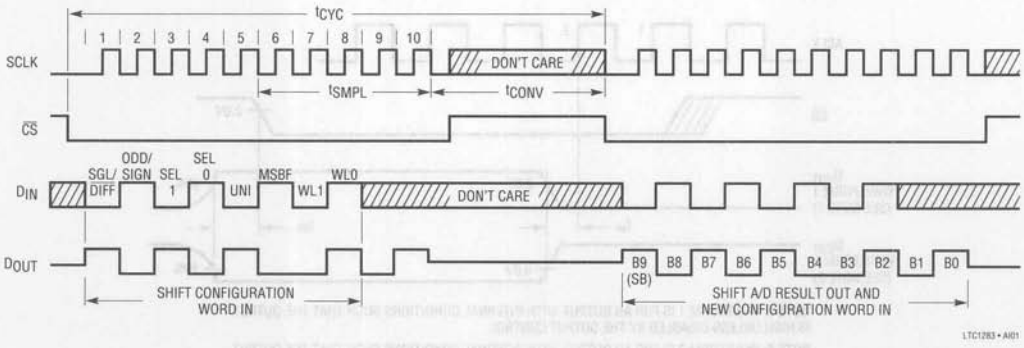


2. Input Data Word

The LTC1283 8-bit input data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:



Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB-First and 10-Bit Word Length)



APPLICATIONS INFORMATION

Multiplexer (MUX) Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicted by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{\text{DIFF}}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM. Figure 1 shows some examples of multiplexer assignments.

Table 1. Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
SGL/ DIFF	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	SGL/ DIFF	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	COM
0	0	0	0	+	–							1	0	0	0	+								–
0	0	0	1			+	–					1	0	0	1			+						–
0	0	1	0					+	–			1	0	1	0					+				–
0	0	1	1							+	–	1	0	1	1							+		–
0	1	0	0	–	+							1	1	0	0		+							–
0	1	0	1			–	+					1	1	0	1				+					–
0	1	1	0					–	+			1	1	1	0						+			–
0	1	1	1							–	+	1	1	1	1								+	–

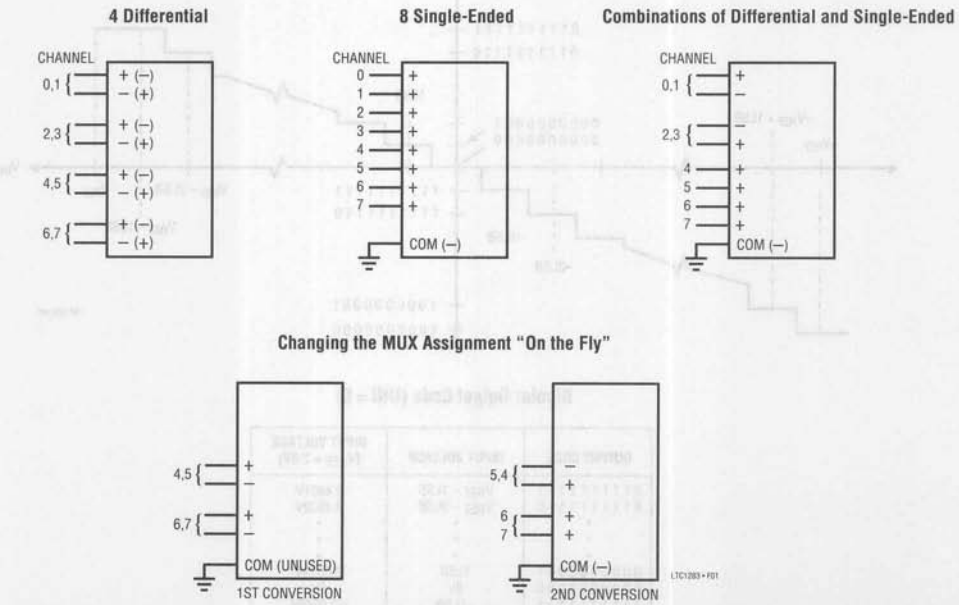


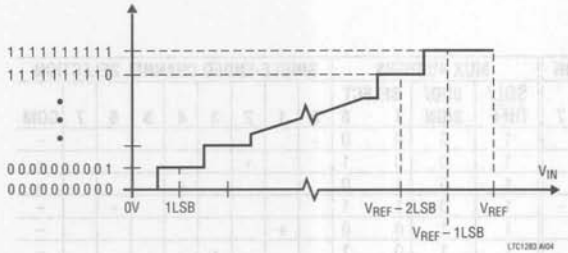
Figure 1. Examples of Multiplexer Options on the LTC1283

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Transfer Curve (UNI = 1)

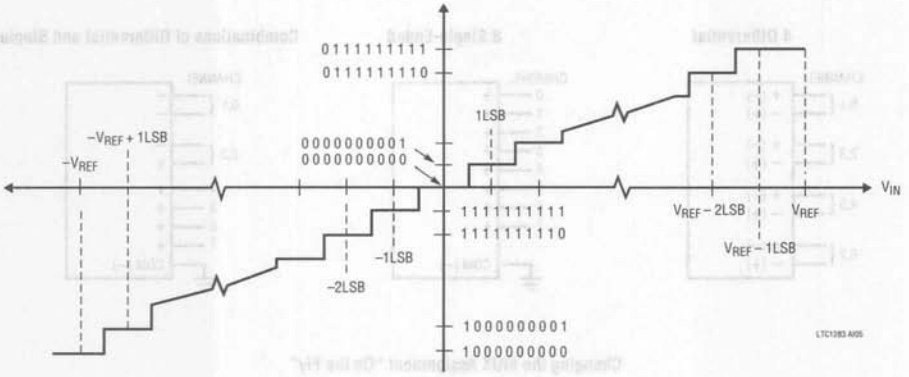


Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (VREF = 2.5V)
1111111111	VREF – 1LSB	2.4976V
1111111110	VREF – 2LSB	2.4951V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0024V
0000000000	0V	0V

LTC1283 A06

Bipolar Transfer Curve (UNI = 0)



Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (VREF = 2.5V)
0111111111	VREF – 1LSB	2.4951V
0111111110	VREF – 2LSB	2.4902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V
1111111111	–1LSB	–0.0049V
1111111110	–2LSB	–0.0098V
•	•	•
•	•	•
•	•	•
1000000001	–(VREF) + 1LSB	–2.4951V
1000000000	–(VREF)	–2.5000V

LTC1283 A07

APPLICATIONS INFORMATION

MSB-First/LSB-First Format (MSBF)

The output data of the LTC1283 is programmed for MSB-first or LSB-first sequence using the MSBF bit. For MSB-first output data the input word clocked to the LTC1283 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB-first output data, the input word clocked to the LTC1283 should always contain a zero in the MSBF bit location. The MSBF bit in a given D_{IN} word will control the order of the next D_{OUT} word. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB-First
1	MSB-First

LTC1283 A08

Word Length (WL1, WL0)

The last two bits of the input word (WL1 and WL0) program the output data word length of the LTC1283. Word lengths of 8-, 10-, 12- or 16-bit can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. **WL1 and WL2 are never "don't cares"** and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU.

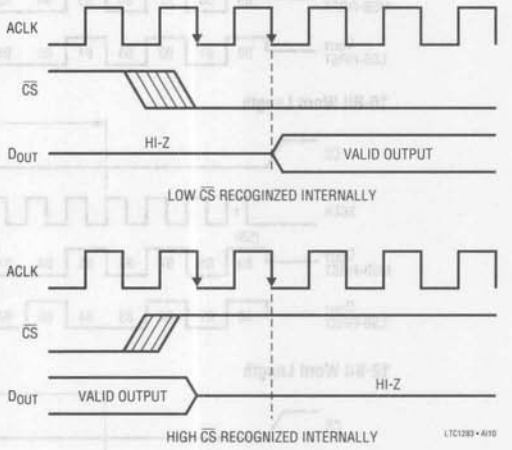
WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	10 Bits
1	0	12 Bits
1	1	16 Bits

LTC1283 • A09

Figure 2 shows how the data output (D_{OUT}) timing can be controlled with word length selection and MSB/LSB-first format selection.

3. Deglitcher

A deglitching circuit has been added to the chip select input of the LTC1283 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than 1 ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1283 waits for two falling edges of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ low recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.



4. $\overline{CS}$ Low During Conversion

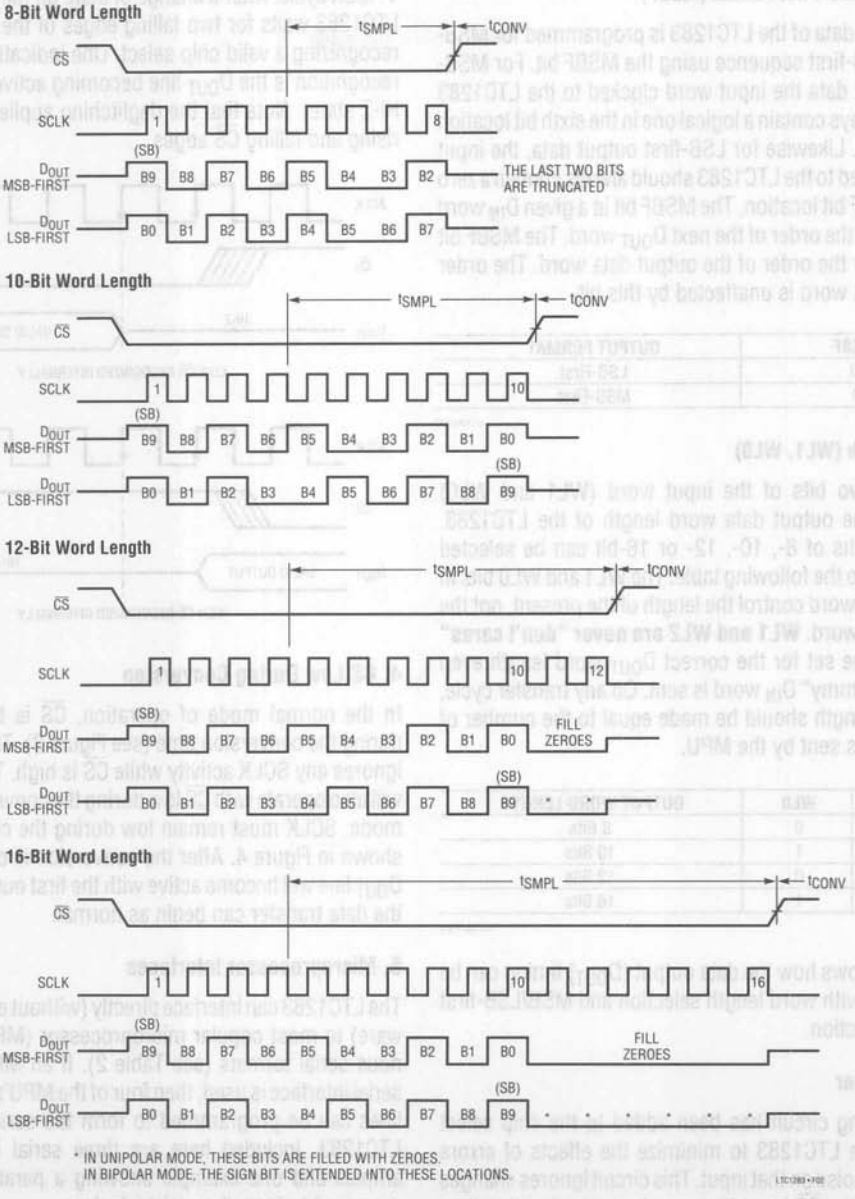
In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time (see Figure 3). The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1283 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in Figure 4. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

5. Microprocessor Interfaces

The LTC1283 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 2). If an MPU without a serial interface is used, then four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1283. Included here are three serial interface examples and one example showing a parallel port programmed to form the serial interface.

6

APPLICATIONS INFORMATION



* IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROES.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

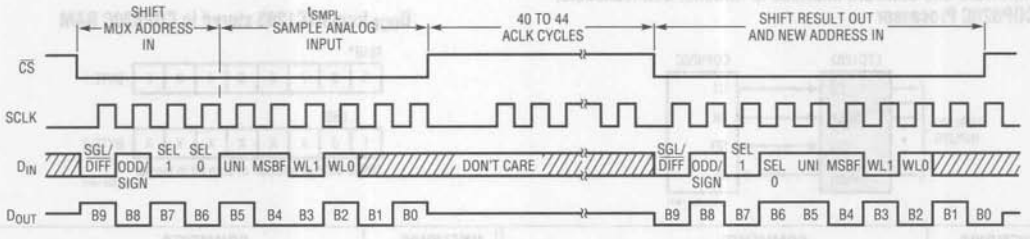


Figure 3. $\overline{CS}$ High During Conversion

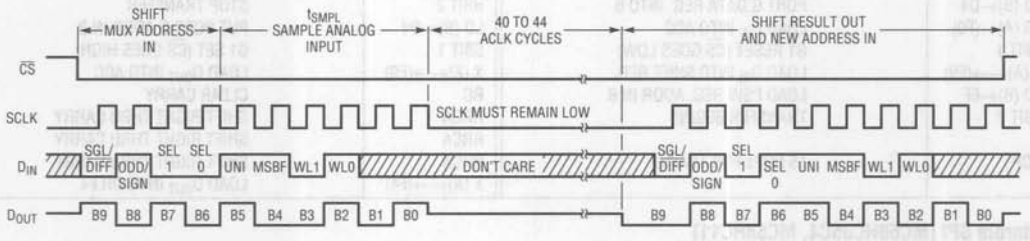


Figure 4. $\overline{CS}$ Low During Conversion

Table 2. 3V Microprocessor with Hardware Serial Interfaces Compatible with the LTC1283*

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
National Semiconductor	
COP800 Family	MICROWIRE/PLUS†
HPC16000 Family	MICROWIRE/PLUS†
Texas Instruments	
TMS70C02	Serial Port
TMS70C42	Serial Port

*Contact factory for interface information for processors not on this list
†MICROWIRE/PLUS is a trademark of National Semiconductor Corp.

Serial Port Microprocessors

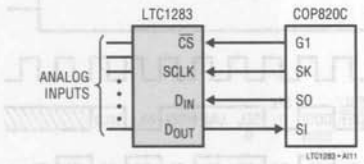
Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufacturers as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB- or MSB-first). The following examples show how the LTC1283 accommodates these differences.

National MICROWIRE (COP820C)

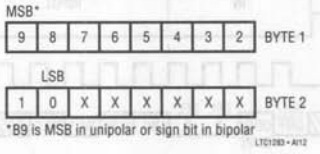
The COP820C transfers data MSB-first and in 8-bit increments. This is easily accommodated by setting the LTC1283 to MSB-first format and 10-bit word length. The data output word is then received by the COP820C in one 8-bit block and one 2-bit block.

APPLICATIONS INFORMATION

Hardware and Software Interface to National Semiconductor COP820C Processor



D_{OUT} from LTC1283 stored in COP820C RAM



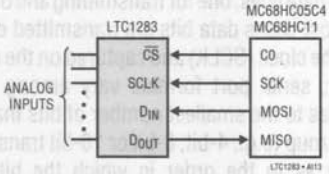
MNEMONIC	COMMENTS
LD (F0)←0D	LOAD 0D INTO F0 (D_{IN})
LD (D5)←32	CONFIGURE PORT G
LD (EE)←8	CONFIGURE CONTROL REG.
LD (B)←D4	PORT G DATA REG. INTO B
LD (A)←(F0)	LOAD D_{IN} INTO ACC
RBIT 1	G1 RESET ($\overline{CS}$ GOES LOW)
X (A)←→(E9)	LOAD D_{IN} INTO SHIFT REG.
LD (B)←EF	LOAD PSW REG. ADDR IN B
SBIT 2	TRANSFER BEGINS
↑	
NOP	15 NOPs FOR TIMING
↓	

MNEMONIC	COMMENTS
X(A)←→(E9)	LOAD D_{OUT} INTO ACC
SBIT 2	TRANSFER CONTINUES
X (A)←→(F3)	LOAD D_{OUT} IN ADDR F3
RBIT 2	STOP TRANSFER
LD (B)←D4	PUT PORT G ADDR IN B
SBIT 1	G1 SET ($\overline{CS}$ GOES HIGH)
X (A)←→(E9)	LOAD D_{OUT} INTO ACC
RC	CLEAR CARRY
RRCA	SHIFT RIGHT THRU CARRY
RRCA	SHIFT RIGHT THRU CARRY
RRCA	SHIFT RIGHT THRU CARRY
X (A)←→(F4)	LOAD D_{OUT} IN ADDR F4

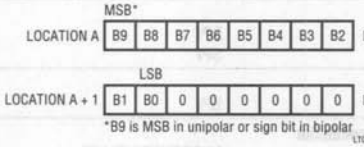
Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 and MC68HC11 transfer data MSB-first and in 8-bit increments. Programming the LTC1283 for MSB-first format and 16-bit word length allows the 10-bit data output to be received by the MPU as two 8-bit bytes with the final 6 unused bits filled with zeroes by the LTC1283.

Hardware and Software Interface to Motorola MC68HC05C4 and MC68HC11 Processors



D_{OUT} from LTC1283 stored in MC68HC05C4 or MC68HC11 RAM



MNEMONIC	COMMENTS
BCLR n	C0 IS CLEARED ($\overline{CS}$ GOES LOW)
LDA	LOAD D_{IN} FOR LTC1283 INTO ACC
STA	LOAD D_{IN} FROM ACC TO SPI DATA REG. START SCK
↑	
NOP	8 NOPs FOR TIMING
↓	
LDA	LOAD CONTENTS OF SPI STATUS REG. INTO ACC
LDA	LOAD LTC1283 D_{OUT} FROM SPI DATA REG. INTO ACC (BYTE 1)
STA	LOAD LTC1283 D_{OUT} INTO RAM (LOCATION A)

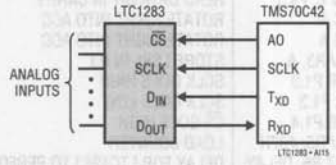
MNEMONIC	COMMENTS
STA	START NEXT SPI CYCLE
↑	
NOP	6 NOPs FOR TIMING
↓	
BSET n	C0 IS SET ($\overline{CS}$ GOES HIGH)
LDA	LOAD CONTENTS OF SPI STATUS REG. INTO ACC
LDA	LOAD LTC1283 D_{OUT} FROM SPI DATA REG. INT ACC (BYTE 2)
STA	LOAD LTC1283 INTO RAM (LOCATION A +1)

APPLICATIONS INFORMATION

Texas Instruments TMS70C42

The TMS70C42 transfers serial data in 8-bit increments, LSB-first. To accommodate this, the LTC1283 is programmed for 16-bit word length and LSB-first format. The 10-bit output data is received by the processor as two 8-bit bytes, LSB-first. The LTC1283 fills the final 6 unused bits (after the MSB) with zeroes.

Hardware and Software Interface to TI TMS70C42 Processor



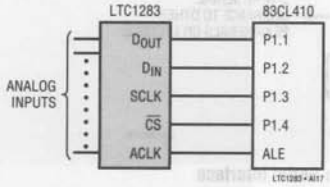
D_{OUT} from LTC1283 stored in TMS70C42 RAM

LABEL	MNEMONIC		DESCRIPTION
START	DINT		DISABLES ALL INTERRUPTS
	MOVP	% > 2A, P0	DISABLE INTERRUPT FLAGS
	MOVP	% > 02, P16	DISABLE INTERRUPT FLAGS
	MOV	% > 60, B	ADDRESS OF STACK
	LDSP		PUT ADDRESS INTO POINTER
	MOVP	% > DF, P5	CONFIGURE PORT A
	MOVP	% > 08, P6	ENABLE Tx BY SETTING B3 = 1
	MOVP	% > 40, P21	RESET THE SERIAL PORT
	MOVP	% > 0C, P20	CONFIGURE THE SERIAL PORT
	MOVP	% > 00, P24	TURN START BIT OFF
	MOVP	% > 00, P21	ENABLE THE SERIAL PORT
	MOVP	% > 00, P23	SET SCLK RATE (TIMER 3)
	MOVP	% > C0, P24	START TIMER
LOOP	MOV	% > DF, A	LOAD D_{IN} WORD IN A
	CALL	SXTNBIT	ROUTINE THAT SHIFTS DATA
	MOV	B, R5	PUT FIRST 8 LSBs IN R5
	MOV	A, R6	PUT MSBs IN R6
SXTNBIT	ANDP	% > FE, P4	A0 CLEARED ($\overline{CS}$ GOES LOW)
	MOVP	A, P26	PUT D_{IN} INTO TXBUF
	MOVP	% > 40, P24	SCLK OFF (TIMER 3 DISABLED)
	MOVP	% > 17, P21	ENABLE SERIAL PORT
	MOVP	% > C0, P24	SCLK ON (TRANSFER BEGINS)
	MOVP	% > 16, P21	TXEN GOES LOW
	MOV	% > 02, A	LOAD COUNTER
WAIT1	DJNZ	A, WAIT1	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P25, B	PUT D_{OUT} IN B
	MOVP	A, P26	LOAD TXBUF
	MOVP	% > 40, P24	SCLK OFF (TIMER 3 DISABLE)
	MOVP	% > 17, P21	ENABLE SERIAL PORT
	MOVP	% > C0, P24	SCLK ON (TRANSFER BEGINS)
	MOVP	% > 16, P21	TXEN GOES LOW
	MOV	% > 02, A	LOAD COUNTER
WAIT2	DJNZ	A, WAIT2	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P25, A	PUT D_{OUT} IN A
	ORP	% > 01, P4	A0 SET ($\overline{CS}$ GOES HIGH)
	RETS		RETURN TO MAIN PROGRAM

Parallel Port Microprocessors

When interfacing the LTC1283 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the $\overline{CS}$, SCLK and D_{IN} signals for the LTC1283. A fourth port line reads the D_{OUT} line. An example is made of the Signetics 83CL410.

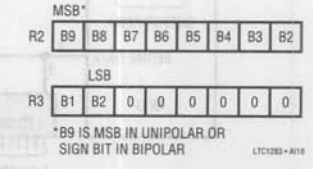
Hardware and Software Interface to Signetics 83CL410 Processor



Signetics 83CL410

To interface to the 83CL410, (a 3V version of the 80C51) the LTC1283 is programmed for MSB-first format and 10-bit word length. The 83CL410 generates $\overline{CS}$, SCLK and D_{IN} on three port lines and reads D_{OUT} on the fourth.

D_{OUT} from LTC1283 stored in 83CL410 RAM



APPLICATIONS INFORMATION

83CL410 Code

MNEMONIC		DESCRIPTION	MNEMONIC		DESCRIPTION
	MOV P1, #02H	INITIALIZE PORT 1 (BIT 1 IS MADE AN INPUT)		MOV C, P1.1	READ DATA BIT INTO CARRY
				CLR A	CLEAR ACC
	CLR P1.3	SCLK GOES LOW		RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.4	$\overline{CS}$ GOES LOW		SETB P1.3	SCLK GOES HIGH
CONTINUE:	MOV A, #0DH	D_{IN} WORD FOR THE LTC1283 IS PLACED IN ACC		CLR P1.3	SCLK GOES LOW
				MOV C, P1.1	READ DATA BIT IN CARRY
	CLR P1.4	$\overline{CS}$ GOES LOW		RRC A	ROTATE RIGHT INTO ACC
	MOV R4, #08	LOAD COUNTER		RRC A	ROTATE RIGHT INTO ACC
	NOP	DELAY FOR DEGLITCHER		MOV R3, A	STORE LSBs IN R3
LOOP:	MOV C, P1.1	READ DATA BIT INTO CARRY		SETB P1.3	SCLK GOES HIGH
	RLC A	ROTATE DATA BIT INTO ACC		CLR P1.3	SCLK GOES LOW
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1283		SETB P1.4	$\overline{CS}$ GOES HIGH
	SETB P1.3	SCLK GOES HIGH		MOV R5, #07H	LOAD COUNTER
	CLR P1.3	SCLK GOES LOW	DELAY:	DJNZ R5, DELAY	DELAY FOR LTC1283 TO PERFORM CONVERSION
	DJNZ R4, LOOP	NEXT BIT			
	MOV R2, A	STORE MSBs IN R2		AJMP CONTINUE	REPEAT PROGRAM

6. Sharing the Serial Interface

The LTC1283 can share the same 3-wire serial interface with other peripheral components or other LTC1283s (see Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1283 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1283 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 4.7µF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 6 shows an example of an ideal ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors

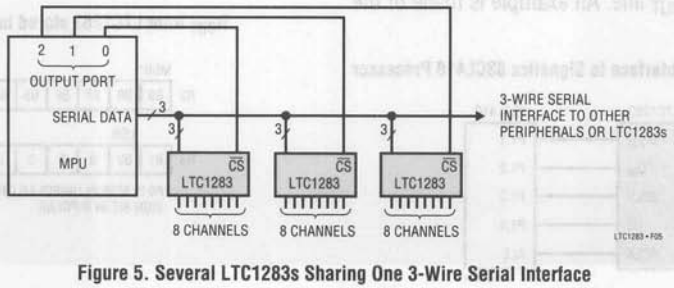


Figure 5. Several LTC1283s Sharing One 3-Wire Serial Interface

APPLICATIONS INFORMATION

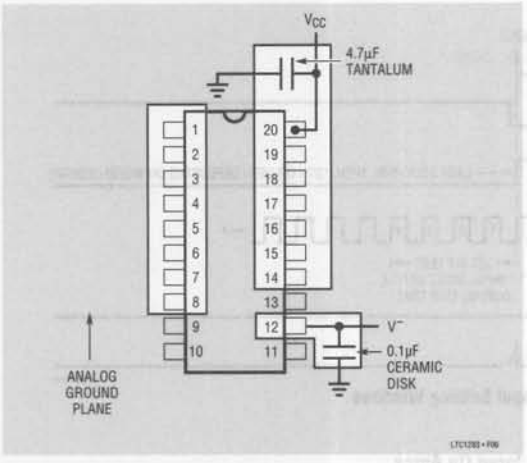


Figure 6. Example Ground Plane for the LTC1283

or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7µF tantalum with leads as short as possible. Figures 7 and 8 show the effects of good and poor V_{CC} bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1283 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem.

However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1283 look like 65pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 9. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

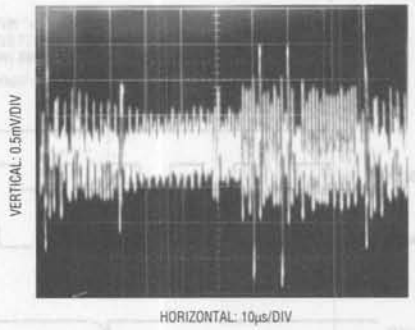


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple can Cause A/D Errors

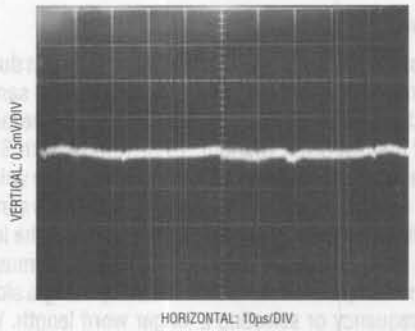


Figure 8. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

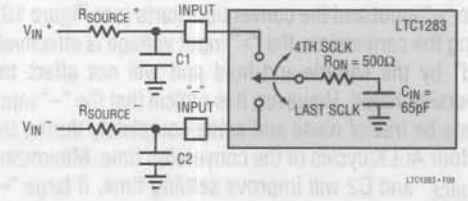


Figure 9. Analog Input Equivalent Circuit

6

APPLICATIONS INFORMATION

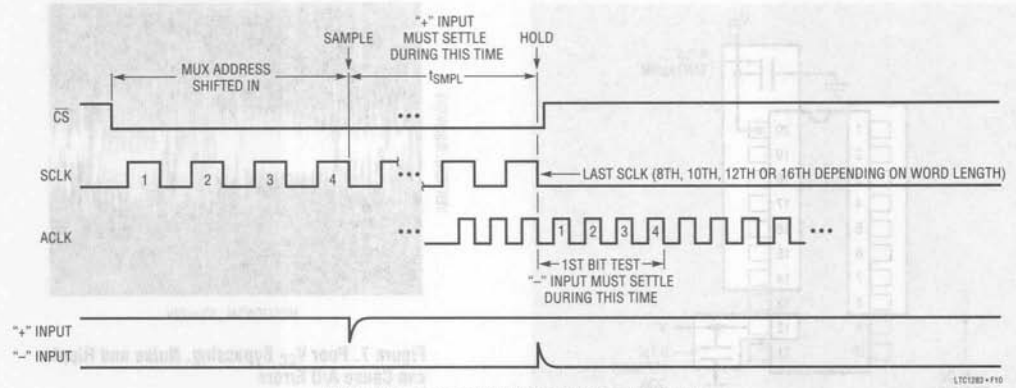


Figure 10. "+" and "–" Input Settling Windows

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 10th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 8µs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 10). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 1MHz, **R_{SOURCE}^- < 1k and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 8µs ("+" input) and 4µs ("–" input) which occur at the maximum clock rates (ACLK = 1MHz and SCLK = 0.5MHz). Figures 11 and 12 show examples of adequate and poor op amp settling.

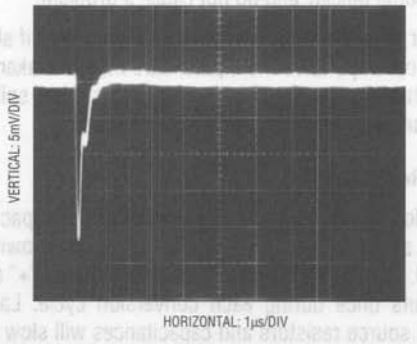


Figure 11. Adequate Settling of Op Amp Driving Analog Input

APPLICATIONS INFORMATION

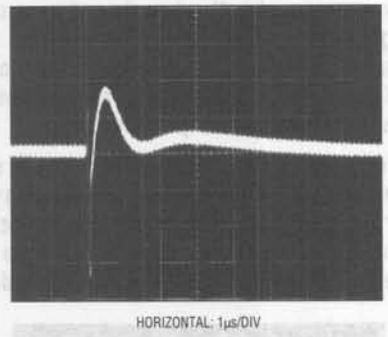


Figure 12. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 65pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 68μs, the input current equals 2.5μA at V_{IN} = 2.5V. In this case, a filter resistor of 100Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve Maximum Filter Resistor vs Cycle Time.

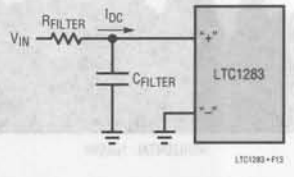


Figure 13. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.4LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the pins of the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample-and-Hold

Single-Ended Inputs

The LTC1283 provides a built-in sample-and-hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). This sample-and-hold allows the LTC1283 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 10th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs, or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the

APPLICATIONS INFORMATION

differencing operation may not be performed accurately. The conversion time is 44 ACLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 44/f_{ACLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (0.61mV) with the converter running at ACLK = 1MHz, its peak value would have to be 38mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1283 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10k resistor but will have transient capacitive switching currents due to the switched-capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

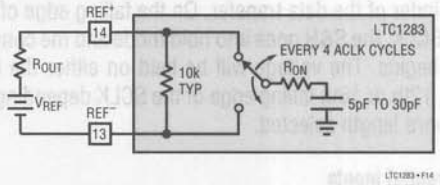


Figure 14. Reference Input Equivalent Circuit

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 300μA maximum reference current (I_{REF}).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 1MHz most references and op amps can be made to settle within the 4μs bit time.
3. It is recommended that the REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

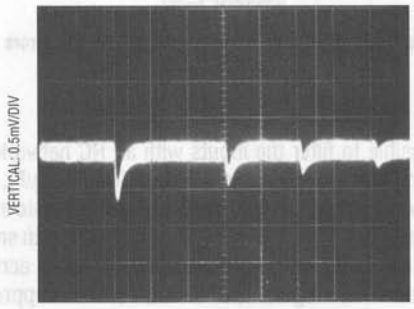


Figure 15. Adequate Reference Settling

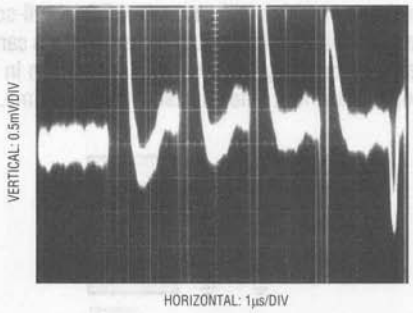


Figure 16. Poor Reference Settling Can Cause A/D Errors

6. Reduced Reference Operation

The effective resolution to the LTC1283 can be increased by reducing the input span of the converter. The LTC1283 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken

APPLICATIONS INFORMATION

when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Conversion speed (ACLK frequency)
2. Offset
3. Noise

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1283 internal comparator overdrive is reduced. With less overdrive, more time is required to perform a conversion. Therefore, the maximum ACLK frequency should be reduced when low values of V_{REF} are used. This is shown in the typical curve of Maximum Conversion Clock Rate vs Reference Voltage.

Offset with Reduced V_{REF}

The offset of the LTC1283 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.5mV which is 0.2LSB with a 2.5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1283.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1283 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

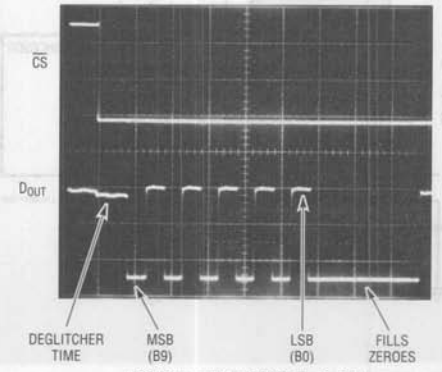
For operation with a 2.5V reference, the 200µV noise is only 0.08LSB peak-to-peak. In this case, the LTC1283 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200µV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200µV noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

A "Quick Look" Circuit for the LTC1283

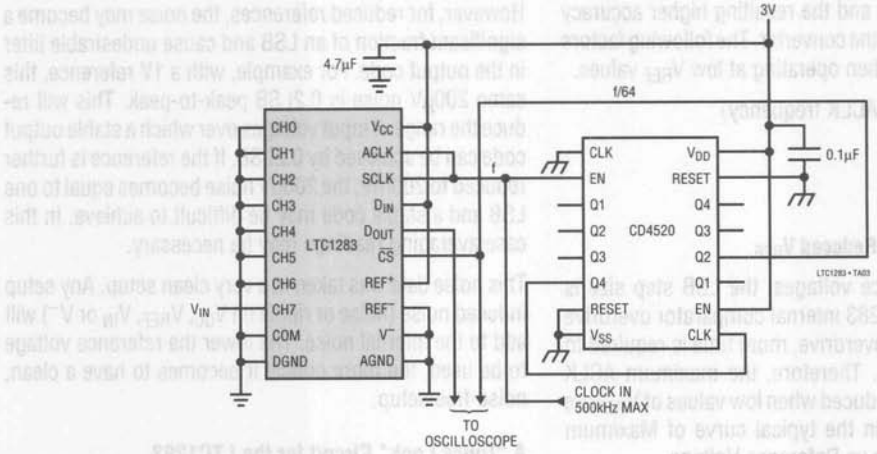
Users can get a quick look at the function and timing of the LTC1283 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 3V input span, CH7 as a single-ended input, unipolar mode, MSB-first format and 16-bit word length. ACLK and SCLK are tied together and driven by an external clock. $\overline{CS}$ is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

Scope Trace of LTC1283 "Quick Look" Circuit Showing A/D Output of 0101010101 (155_{HEX})



TYPICAL APPLICATIONS

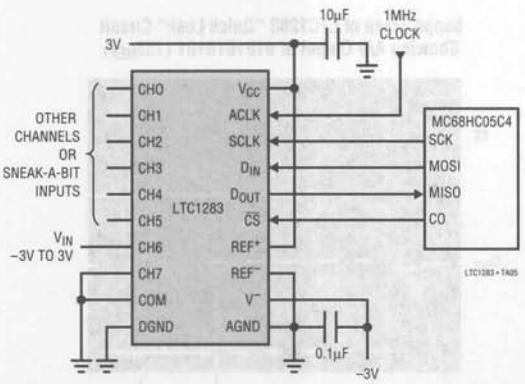
A "Quick Look" Circuit for the LTC1283



SNEAK-A-BIT™

The LTC1283's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 10-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example; however, any processor could be used.

SNEAK-A-BIT Circuit

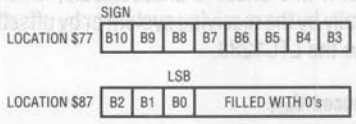


SNEAK-A-BIT is a trademark of Linear Technology Corp.

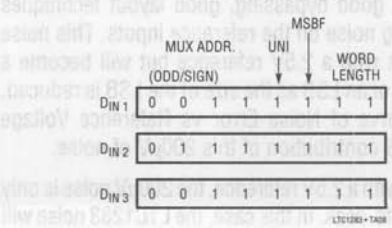
Two 10-bit unipolar conversions are performed: the first over a 0V to 3V span and the second over a 0V to –3V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contain it. Then the resulting number (ranging from –1023 to 1023 decimal) is converted to 2's complement notation and stored in RAM.

SNEAK-A-BIT Code

D_{OUT} from LTC1283 in MC68HC05C4



D_{IN} Words for LTC1283



TYPICAL APPLICATIONS

Sneak-A-Bit Code for the LTC1283 Using the MC68HC05C4

MNEMONIC			DESCRIPTION
	LDA	#$50	CONFIGURATION DATA FOR SPCR
	STA	$0A	LOAD CONFIGURATION DATA INTO $0A
	LDA	#$FF	CONFIGURATION DATA FOR PORT C DDR
	STA	$06	LOAD CONFIGURATION DATA INTO PORT C DDR
	BSET	0, $02	MAKE SURE $\overline{CS}$ IS HIGH
	JSR	READ –/+	DUMMY READ CONFIGURES LTC1283 FOR NEXT READ
	JSR	READ +/–	READ CH6 WITH RESPECT TO CH7
	JSR	READ –/+	READ CH7 WITH RESPECT TO CH6
	JSR	CHK SIGN	DETERMINES WHICH READING HAS VALID DATA, CONVERTS TO 2's COMPLEMENT AND STORES IN RAM
READ –/+:	LDA	#$3F	LOAD D_{IN} WORD FOR LTC1283 INTO ACC
	JSR	TRANSFER	READ LTC1283 ROUTINE
	LDA	$60	LOAD MSBs FROM LTC1283 INTO ACC
	STA	$71	STORE MSBs IN $71
	LDA	$61	LOAD LSBs FROM LTC1283 INTO ACC
	STA	$72	STORE LSBs IN $72
	RTS		RETURN
Read +/–:	LDA	#$7F	LOAD D_{IN} WORD FOR LTC1283 INTO ACC
	JSR	TRANSFER	READ LTC1283 ROUTINE
	LDA	$60	LOAD MSBs FROM LTC1283 INTO ACC
	STA	$73	STORE MSBs IN $73
	LDA	$61	LOAD LSBs FROM LTC1283 INTO ACC
	STA	$74	STORE LSBs IN $74
	RTS		RETURN
TRANSFER:	BCLR	0, $02	$\overline{CS}$ GOES LOW
	STA	$0C	LOAD D_{IN} INTO SPI. START TRANSFER
LOOP 1:	TST	$0B	TEST STATUS OF SPIF
	BPL	LOOP 1	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	LDA	$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	$0C	START NEXT CYCLE
	STA	$60	STORE MSBs IN $60

MNEMONIC			DESCRIPTION
LOOP 2:	TST	$0B	TEST STATUS OF SPIF
	BPL	LOOP 2	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	BSET	0, $02	$\overline{CS}$ GOES HIGH
	LDA	$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	$61	STORE LSBs IN $61
	RTS		RETURN
CHK SIGN:	LDA	$73	LOAD MSBs OF +/– READ INTO ACC
	ORA	$74	OR ACC (MSBs) WITH LSBs OF +/– read
	BEQ	MINUS	IF RESULT IS 0 GOTO MINUS
	CLC		CLEAR CARRY
	ROR	$73	ROTATE RIGHT $73 THROUGH CARRY
	ROR	$74	ROTATE RIGHT $74 THROUGH CARRY
	LDA	$73	LOAD MSBs OF +/– READ INTO ACC
	STA	$77	STORE MSBs IN RAM LOCATION $77
	LDA	$74	LOAD LSBs OF +/– READ INTO ACC
	STA	$87	STORE LSBs IN RAM LOCATION $87
	BRA	END	GOTO END OF ROUTINE
MINUS:	CLC		CLEAR CARRY
	ROR	$71	SHIFT MSBs OF –/+ READ RIGHT
	ROR	$72	SHIFT LSBs –/+ READ RIGHT
	COM	$71	1's COMPLEMENT OF MSBs
	COM	$72	1's COMPLEMENT OF LSBs
	LDA	$72	LOAD LSBs INTO ACC
	ADD	#$01	ADD 1 TO LSBs
	STA	$72	STORE ACC IN $72
	CLRA		CLEAR ACC
	ADC	$71	ADD WITH CARRY TO MSBs. RESULT IN ACC
	STA	$71	STORE ACC IN $71
	STA	$77	STORE MSBs IN RAM LOCATION $77
	LDA	$72	LOAD LSBs IN ACC
	STA	$87	STORE LSBs IN RAM LOCATION $87
END:	RTS		RETURN

Micropower Sampling 12-Bit A/D Converters In SO-8 Packages

FEATURES

- **12-Bit Resolution**
- **8-Pin SOIC Plastic Package**
- **Low Cost**
- **Low Supply Current: 250μA Typ.**
- Auto Shutdown to 1nA Typ.
- Guaranteed ±3/4LSB Max DNL
- Single Supply 5V to 9V Operation
- On-Chip Sample-and-Hold
- 60μs Conversion Time
- Sampling Rates:
  12.5 ksps (LTC1286)
  11.1 ksps (LTC1298)
- I/O Compatible with SPI, Microwire, etc.
- Differential Inputs (LTC1286)
- 2-Channel MUX (LTC1298)
- 3V Versions Available: LTC1285/LTC1288

APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Handheld Terminal Interface
- Temperature Measurement
- Isolated Data Acquisition

DESCRIPTION

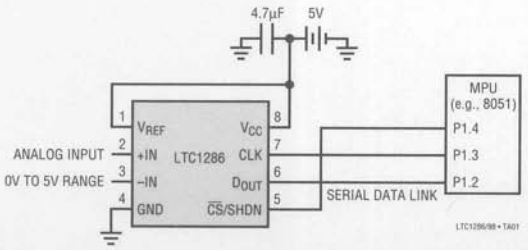
The LTC1286/LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. They typically draw only 250μA of supply current when converting and automatically power down to a typical supply current of 1nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 5V to 9V supplies. These 12-bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1286 has a single differential analog input. The LTC1298 offers a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

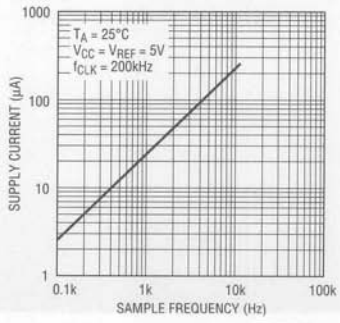
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATIONS

25μW, SO-8 Package, 12-Bit ADC Samples at 200Hz and Runs Off a 5V Supply



Supply Current vs Sample Rate



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
Analog and Reference ..... −0.3V to V_{CC} + 0.3V
Digital Inputs ..... −0.3V to 12V
Digital Output ..... −0.3V to V_{CC} + 0.3V

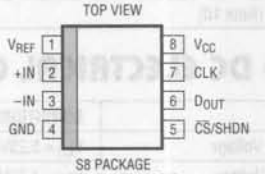
Power Dissipation 500mW
Operating Temperature Range
LTC1286C/LTC1298C ..... 0°C to 70°C
LTC1286I/LTC1298I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1286CN8
LTC1286IN8



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER

LTC1286CS8
LTC1286IS8

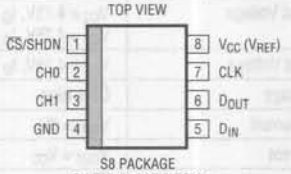
PART MARKING

1286C
1286I

N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1298CN8
LTC1298IN8



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER

LTC1298CS8
LTC1298IS8

PART MARKING

1298C
1298I

Consult factory for military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)	LTC1286 LTC1298	4.5 4.5		9.0 5.5	V V
f_{CLK}	Clock Frequency	V_{CC} = 5V	(Note 4)		200	kHz
t_{CYC}	Total Cycle Time	LTC1286, f_{CLK} = 200kHz LTC1298, f_{CLK} = 200kHz	80 90			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 5V	150			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	LTC1286, V_{CC} = 5V LTC1298, V_{CC} = 5V	2 2			µs µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	400			ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	2			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	2			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1286, f_{CLK} = 200kHz LTC1298, f_{CLK} = 200kHz	75 85			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1286 MIN	LTC1286 TYP	LTC1286 MAX	LTC1298 MIN	LTC1298 TYP	LTC1298 MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●		±3/4	±2		±3/4	±2	LSB
Differential Linearity Error		●		±1/4	±3/4		±1/4	±3/4	LSB
Offset Error		●		3/4	±3		3/4	±3	LSB
Gain Error		●		±2	±8		±2	±8	LSB
Analog Input Range	(Note 7 and 8)	●		−0.05V to V_{CC} + 0.05V					V
REF Input Range (LTC1286) (Notes 7, 8, and 9)	$4.5 \le V_{CC} \le 5.5V$ $5.5V < V_{CC} \le 9V$			1.5V to V_{CC} + 0.05V 1.5V to 5.55V					V V
Analog Input Leakage Current (Note 10)		●		±1			±1		µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.0 2.4	4.64 4.62		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		mA
R_{REF}	Reference Input Resistance (LTC1286)	$\overline{CS} = V_{CC}$ $\overline{CS}$ = GND			5000 55		MΩ kΩ
I_{REF}	Reference Current (LTC1286)	$\overline{CS} = V_{CC}$ $t_{CYC} \ge 640µs$, $f_{CLK} \le 25kHz$ $t_{CYC} = 80µs$, $f_{CLK} = 200kHz$	● ● ●		0.001 90 90	2.5 140 140	µA µA µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$	●		0.001	±3.0	µA
		LTC1286, $t_{CYC} \ge 640µs$, $f_{CLK} \le 25kHz$ LTC1286, $t_{CYC} = 80µs$, $f_{CLK} = 200kHz$	● ●		200 250	400 500	µA µA
		LTC1298, $t_{CYC} \ge 720µs$, $f_{CLK} \le 25kHz$ LTC1298, $t_{CYC} = 90µs$, $f_{CLK} = 200kHz$	● ●		290 340	490 640	µA µA

DYNAMIC ACCURACY f_{SMPL} = 12.5kHz (LTC1286), f_{SMPL} = 11.1kHz (LTC1298) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N +D)	Signal-to-Noise Plus Distortion Ratio	1kHz/7kHz Input Signal		71/68		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz/7kHz Input Signal		−84/−80		dB
SFDR	Spurious-Free Dynamic Range	1kHz/7kHz Input Signal		90/86		dB
	Peak Harmonic or Spurious Noise	1kHz/7kHz Input Signal		−90/−86		dB

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1286 LTC1298	● ●	12.5 11.1			kHz kHz
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		250	600	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		135	300	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		75	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			230		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		20	75	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		20	75	ns
C_{IN}	Input Capacitance	Analog Inputs, On Channel Analog Inputs, Off Channel Digital Input			20 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: These devices are specified at 5V. For 3V specified devices, see LTC1285 and LTC1288.

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 120kHz$ at 85°C, $f_{CLK} \geq 75kHz$ at 70° and $f_{CLK} \geq 1kHz$ at 25°C.

Note 5: V_{CC} = 5V, V_{REF} = 5V and CLK = 200kHz unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for $4.5V \leq V_{CC} \leq 5.5V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading. For $5.5V < V_{CC} \leq 9V$, reference and analog input range cannot exceed 5.55V. If reference and analog input range are greater than 5.55V, the output code will not be guaranteed to be correct.

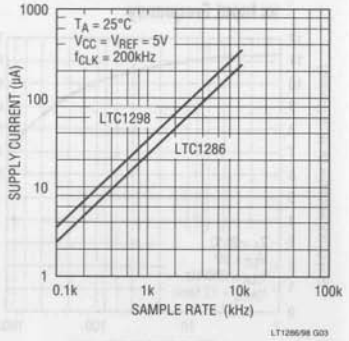
Note 8: The supply voltage range for the LTC1286 is from 4.5V to 9V, but the supply voltage range for the LTC1298 is only from 4.5V to 5.5V.

Note 9: Recommended operating conditions

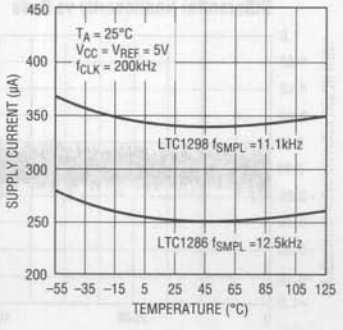
Note 10: Channel leakage current is measured after the channel selection.

TYPICAL PERFORMANCE CHARACTERISTICS

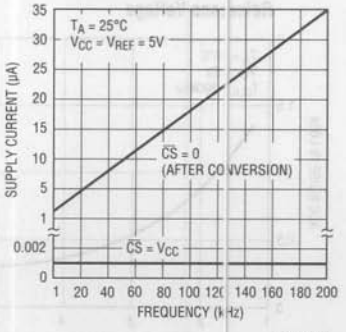
Supply Current vs Sample Rate



Supply Current vs Temperature

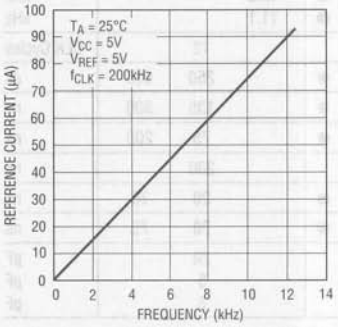


Shutdown Supply Current vs Clock Rate with $\overline{CS}$ High and $\overline{CS}$ Low

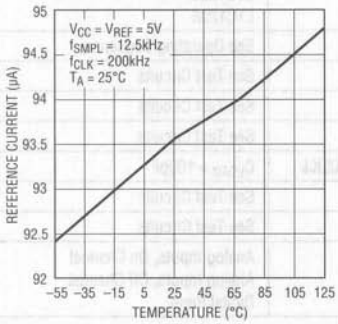


TYPICAL PERFORMANCE CHARACTERISTICS

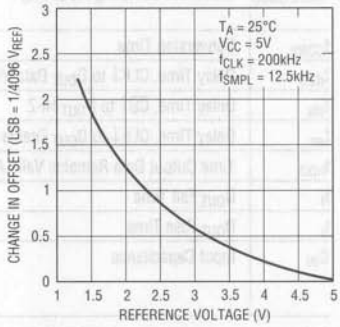
Reference Current vs Sample Rate (LTC1286)



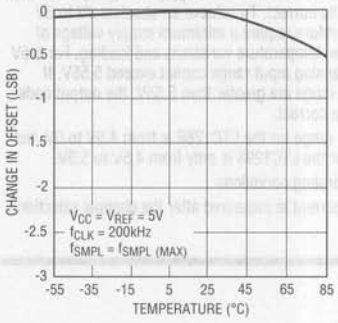
Reference Current vs Temperature



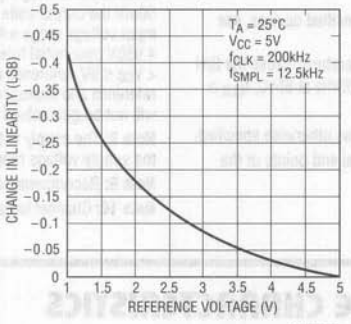
Change in Offset vs Reference Voltage



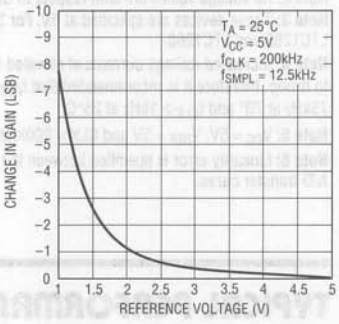
Change in Offset vs Temperature



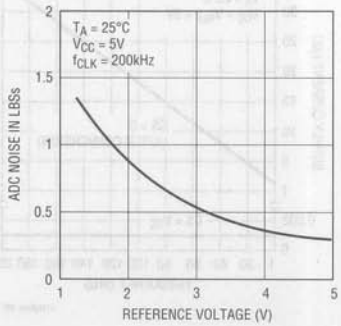
Change In Linearity vs Reference Voltage



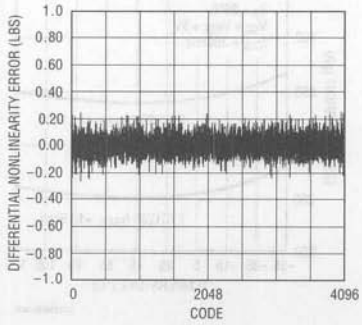
Change In Gain vs Reference Voltage



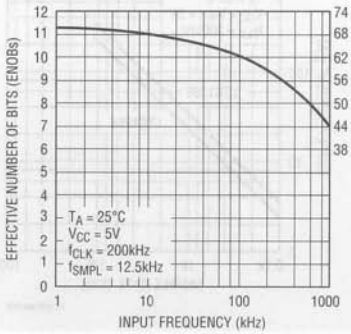
Peak-to-Peak ADC Noise vs Reference Voltage



Differential Nonlinearity vs Code

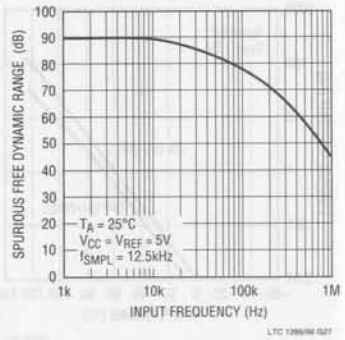


Effective Bits and S/(N + D) vs Input Frequency

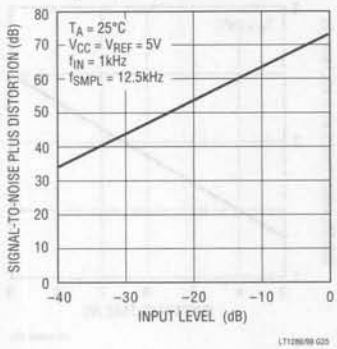


TYPICAL PERFORMANCE CHARACTERISTICS

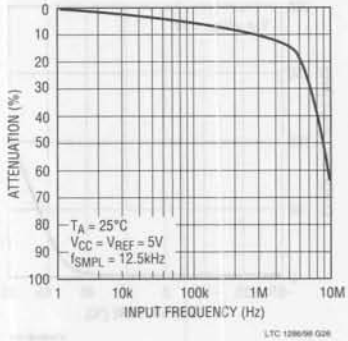
Spurious Free Dynamic Range vs Frequency



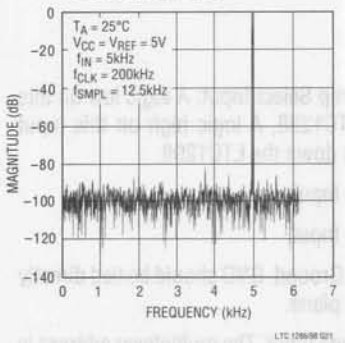
S/(N+D) vs Input Level



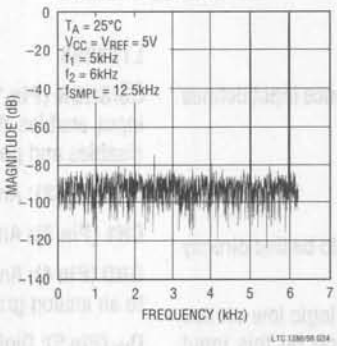
Attenuation vs Input Frequency



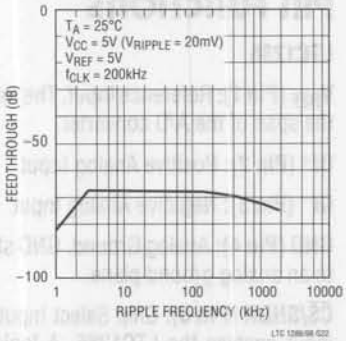
4096 Point FFT Plot



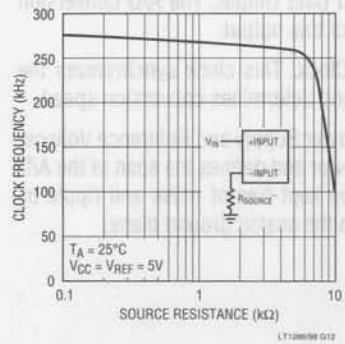
Intermodulation Distortion



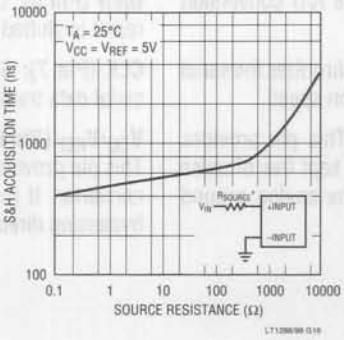
Power Supply Feedthrough vs Ripple Frequency



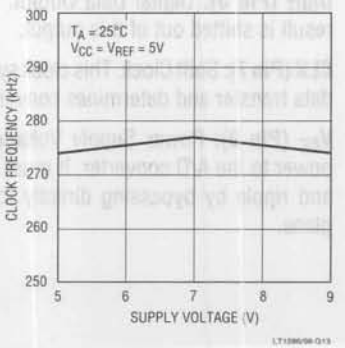
Maximum Clock Frequency vs Source Resistance



Sample and Hold Aquisition Time vs Source Resistance



Maximum Clock Frequency vs Supply Voltage



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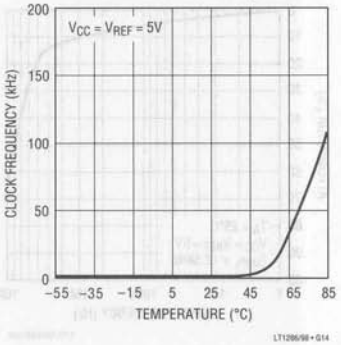
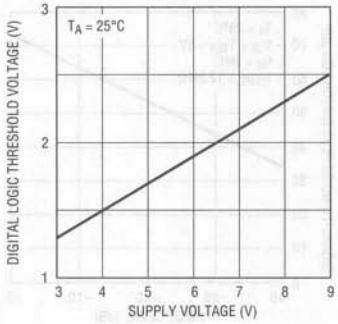
TYPICAL PERFORMANCE CHARACTERISTICS

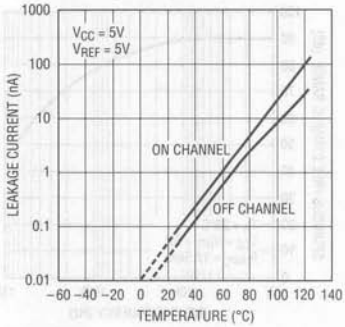
Minimum Clock Frequency for 0.1 LSB Error vs Temperature



Digital Input Logic Threshold vs Supply Voltage



Input Channel Leakage Current vs Temperature



PIN FUNCTIONS

LTC1286

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter.

IN^+ (Pin 2): Positive Analog Input.

IN^- (Pin 3): Negative Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$/SHDN (Pin 5): Chip Select Input. A logic low on this input enables the LTC1286. A logic high on this input disables and powers down the LTC1286.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1298

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1298. A logic high on this input disables and powers down the LTC1298.

CH0 (Pin 2): Analog Input.

CH1 (Pin 3): Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

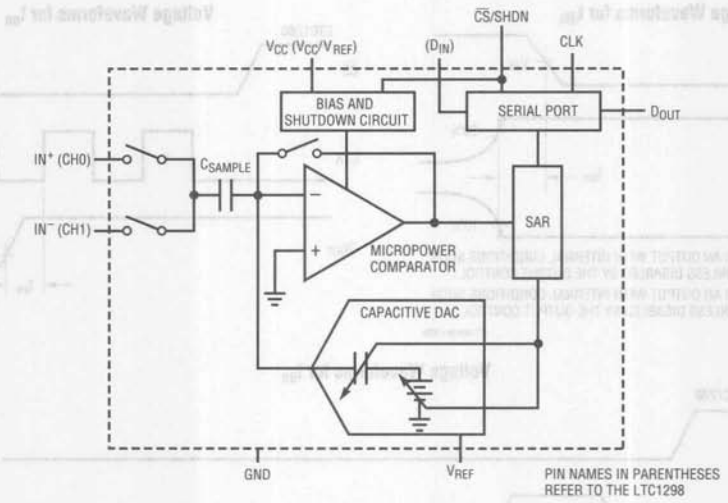
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

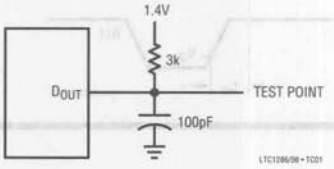
V_{CC}/V_{REF} (Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM



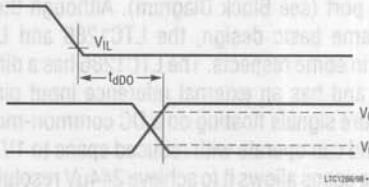
TEST CIRCUITS

Load Circuit for t_{dDO}, t_r and t_f

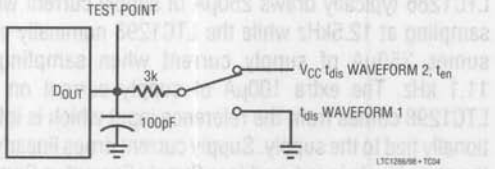


Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



Load Circuit for t_{dis} and t_{en}



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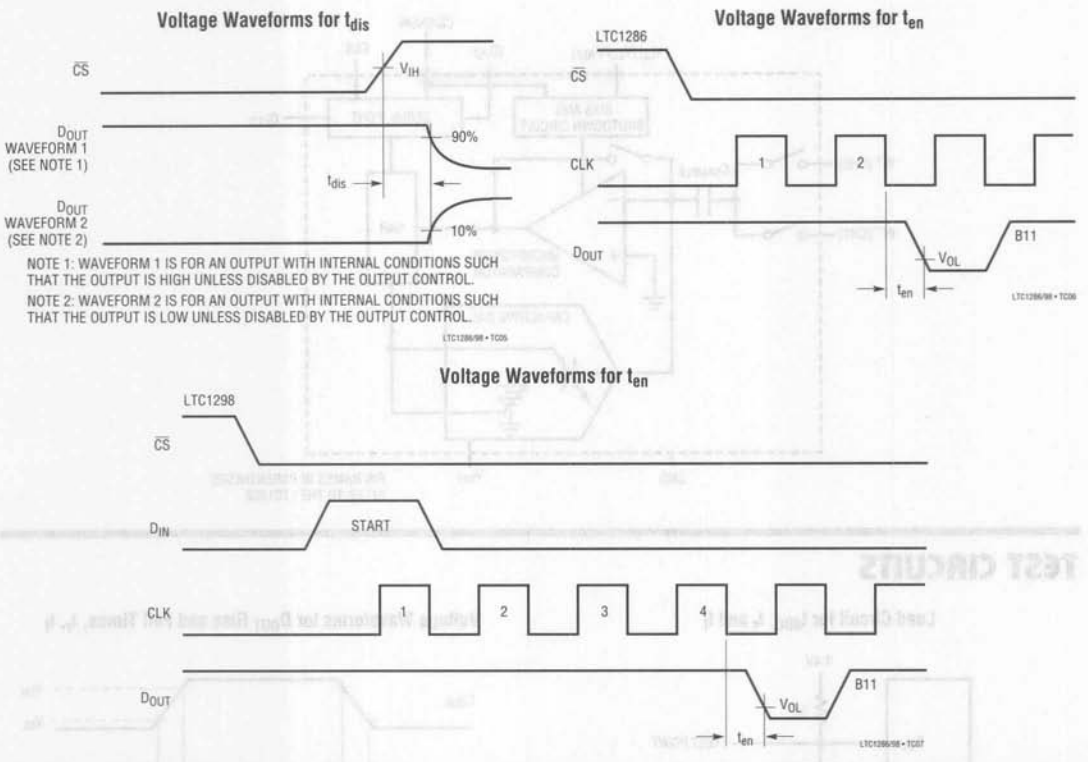
TEST CIRCUITS



APPLICATION INFORMATION

OVERVIEW

The LTC1286 and LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. The LTC1286 typically draws 250μA of supply current when sampling at 12.5kHz while the LTC1298 nominally consumes 350μA of supply current when sampling at 11.1 kHz. The extra 100μA of supply current on the LTC1298 comes from the reference input which is intentionally tied to the supply. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. They are packaged in 8-pin SO and DIP packages. The LTC1286 operates on a single supply from 4.5V to 9V, while the LTC1298 operates from a 4.5V to 5.5V supply.

Both the LTC1286 and the LTC1298 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1286 and LTC1298 differ in some respects. The LTC1286 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans to 1V. Reducing the spans allows it to achieve 244μV resolution. The LTC1298 has a two-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. The reference input is tied to the supply pin.

APPLICATION INFORMATION

SERIAL INTERFACE

The 2-channel LTC1298 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The single channel LTC1286 uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1286 does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1286 operating sequence. After $\overline{CS}$ falls the second CLK pulse enables D_{OUT}. After one null bit the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1286 for the next data exchange.

The LTC1298 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1298 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1298 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1298 in preparation for the next data exchange.

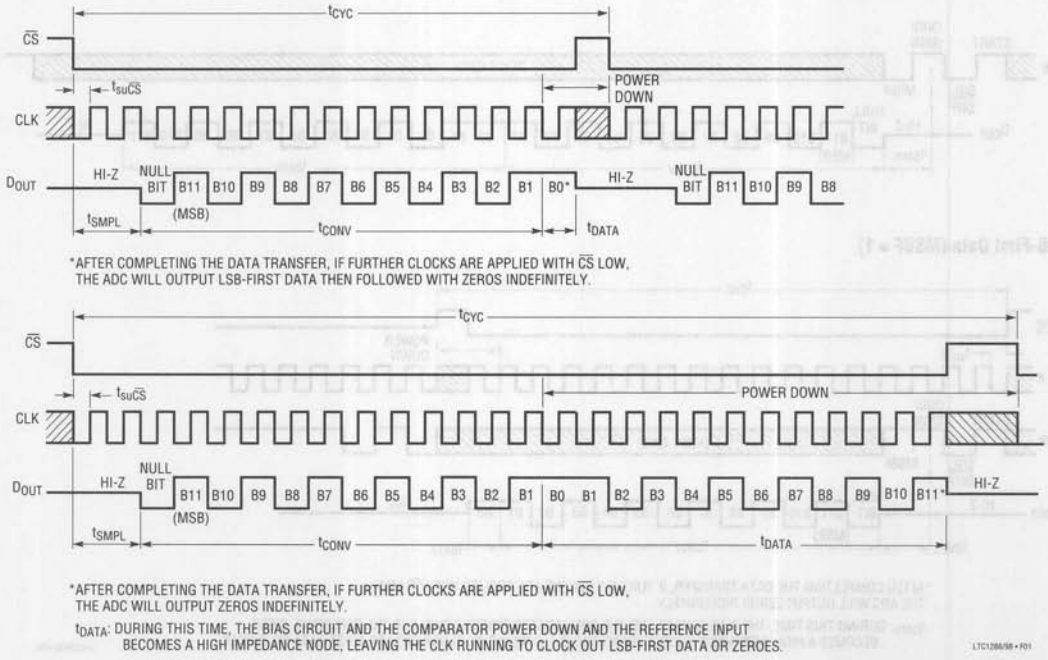
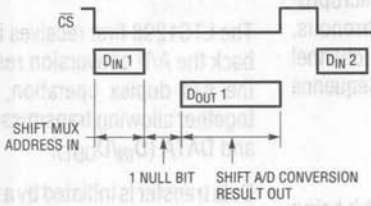
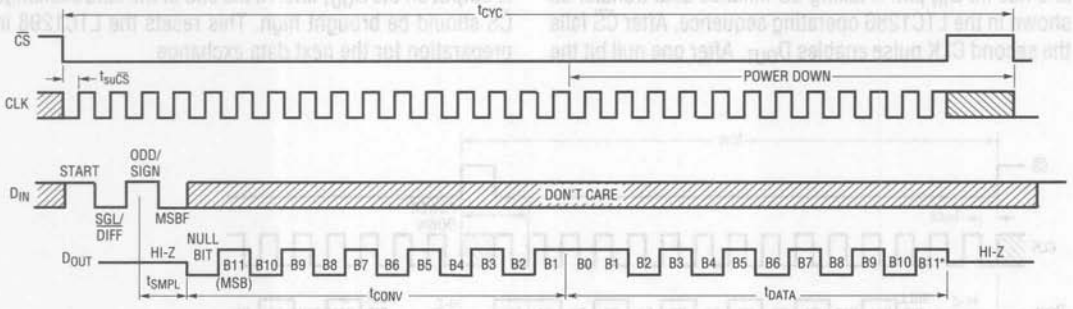


Figure 1. LTC1286 Operating Sequence

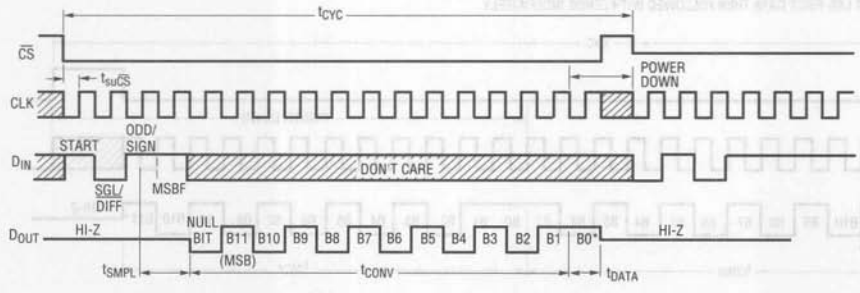
APPLICATION INFORMATION



MSB-First Data (MSBF = 0)



MSB-First Data (MSBF = 1)



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

t_{DATA}: DURING THIS TIME, THE BIAS CIRCUIT AND THE COMPARATOR POWER DOWN AND THE REFERENCE INPUT BECOMES A HIGH IMPEDANCE NODE, LEAVING THE CLK RUNNING TO CLOCK OUT LSB-FIRST DATA OR ZEROES.

Figure 2. LTC1298 Operating Sequence Example: Differential Inputs (CH+, CH−)

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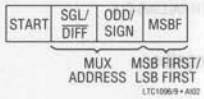
Input Data Word

The LTC1286 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result appears on the D_{OUT} line. The data format is MSB first followed by the LSB sequence. This provides easy interface to MSB or LSB first serial ports. For MSB first data the $\overline{CS}$ signal can be taken high after B0 (see Figure 1). The LTC1298 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1298 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1298 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

LTC1096/8 • AI03

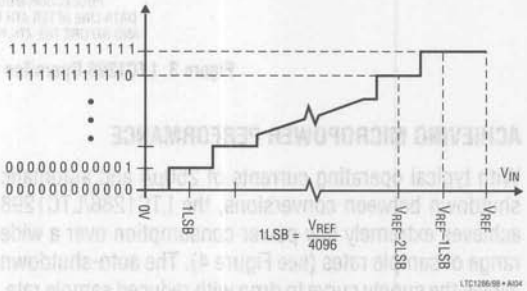
MSB First/LSB First (MSBF)

The output data of the LTC1298 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (see Operating Sequence)

Transfer Curve

The LTC1286/LTC1298 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Transfer Curve



Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111111111	V_{REF} – 1LSB	4.99878V
11111111111110	V_{REF} – 2LSB	4.99756V
•	•	•
•	•	•
•	•	•
00000000000001	1LSB	0.00122V
00000000000000	0V	0V

LTC1286/98 • AI05

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1298 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1298 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1298 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

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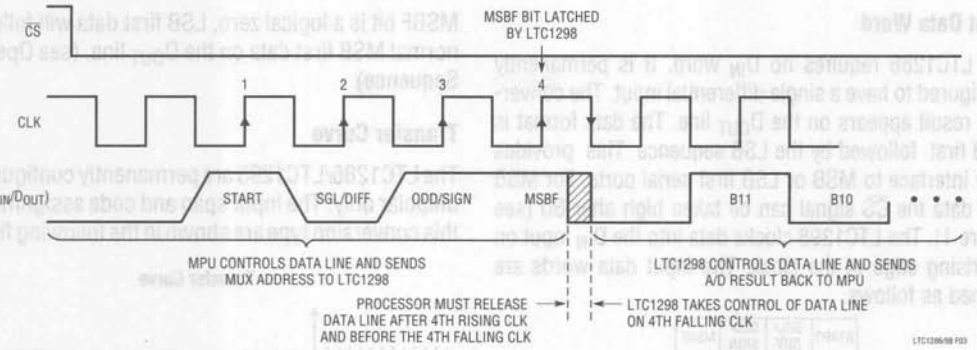

Figure 3. LTC1298 Operation with D_{IN} and D_{OUT} Tied Together

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 250µA and automatic shutdown between conversions, the LTC1286/LTC1298 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). The auto-shutdown allows the supply curve to drop with reduced sample rate. Several things must be taken into account to achieve such a low power consumption.

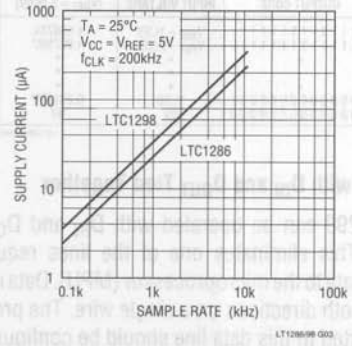

Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate.

Shutdown

The LTC1286/LTC1298 are equipped with automatic shutdown features. They draw power when the $\overline{CS}$ pin is low and shut down completely when that pin is high. The bias circuit and comparator powers down and the reference input becomes high impedance at the end of each conversion leaving the CLK running to clock out the LSB first data or zeroes (see Figures 1 and 2). If the $\overline{CS}$ is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the $\overline{CS}$ pin to ground when it is low and to supply voltage when it is high.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input have no effect on supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. After a conversion the ADC automatically shuts down even if $\overline{CS}$ is held low (see Figures 1 and 2). If the clock is left running to clock out LSB-data or zero, the logic will draw a small current. Figure 5 shows that the typical supply current with $\overline{CS}$ = ground varies from 1µA at 1kHz to 35µA at 200kHz. When $\overline{CS}$ = V_{CC}, the logic is gated off and no supply current is drawn regardless of the clock frequency.

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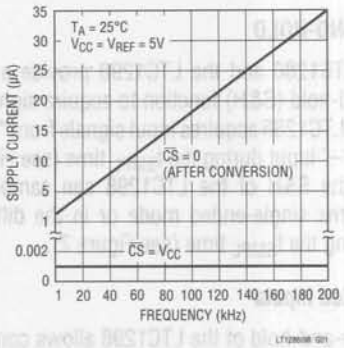

Figure 5. Shutdown current with $\overline{CS}$ high is 1nA typically, regardless of the clock. Shutdown current with $\overline{CS}$ = ground varies from 1µA at 1kHz to 35µA at 200kHz.

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can add more than 50µA to the supply current at a 200kHz clock frequency. An extra 50µA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The C × V × f currents must be evaluated and the troublesome ones minimized.

OPERATING ON OTHER THAN 5V SUPPLIES (LTC1286)

The LTC1286 operates from 4.5V to 9V supplies and the LTC1298 operates from a 5V supply. To operate the LTC1286 on other than 5V supplies a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on a 5V supply. When the supply voltage varies, the input logic levels also change. For the LTC1286 to sample and convert correctly, the digital inputs have to be in the proper logical low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

Clock Frequency

The maximum recommended clock frequency is 200kHz for the LTC1286/LTC1298 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1286 operating on a 9V supply. The requirement to achieve this is that the outputs of $\overline{CS}$ and CLK from the MPU have to be able to trip the equivalent inputs of the LTC1286 and the output of D_{OUT} from the LTC1286 must be able to toggle the equivalent input of the MPU (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1286 operating on a 9V supply, the output of D_{OUT} may go between 0V and 9V. The 9V output may damage the MPU running off a 5V supply. The way to get around this possibility is to have a resistor divider on D_{OUT} (Figure 6) and connect the center point to the MPU input. It should be noted that to get full shutdown, the $\overline{CS}$ input of the LTC1286 must be driven to the V_{CC} voltage to keep the $\overline{CS}$ input buffer from drawing current. An alternative is to leave $\overline{CS}$ low after a conversion, clock data until D_{OUT} outputs zeros, and then stop the clock low.

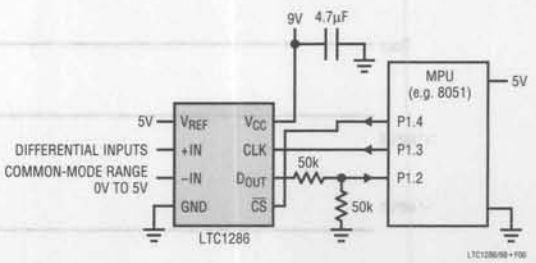

Figure 6. Interfacing a 9V Powered LTC1286 to a 5V System

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BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1286/LTC1298 are easy to use if some care is taken. They should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 10µF tantalum capacitor with leads as short as possible. If the power supply is clean, the LTC1286/LTC1298 can also operate with smaller 1µF or less surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1286 and the LTC1298 provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1286 acquires input signals from "+" input relative to "–" input during the t_{SMPL} time (see Figure 1). However, the S&H of the LTC1298 can sample input signals in the single-ended mode or in the differential inputs during the t_{SMPL} time (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1298 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

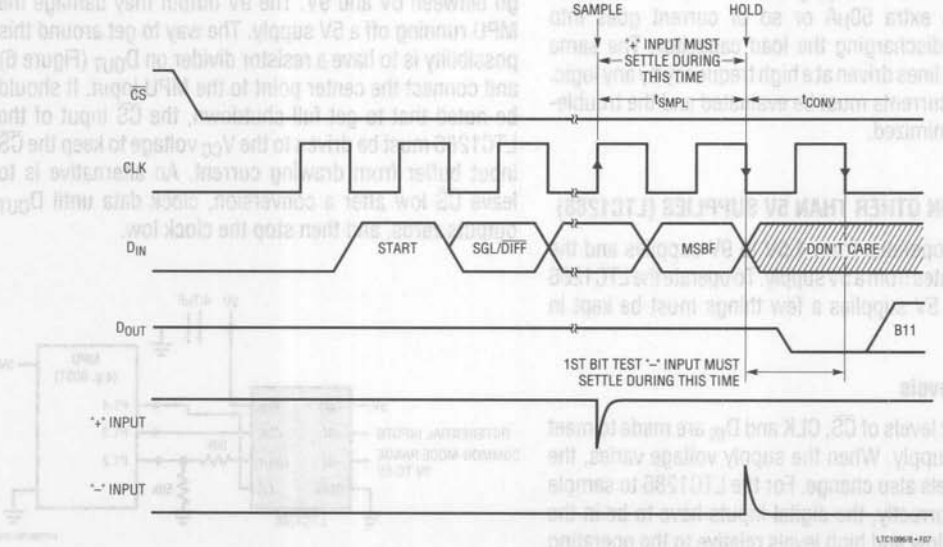

Figure 7. LTC1298 "+" and "–" Input Settling Windows

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Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 12 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 12/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (305μV) with the converter running at CLK = 200kHz, its peak value would have to be 13.48mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1286/LTC1298 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1286 is switched onto "+" input during the t_{SMPL} time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1298 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 1 1/2 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPLE} for the LTC1286 and the LTC1298 respectively. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 6μs ("+" input) which occur at the maximum clock rate of 200kHz.

Source Resistance

The analog inputs of the LTC1286/LTC1298 look like a 20pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances

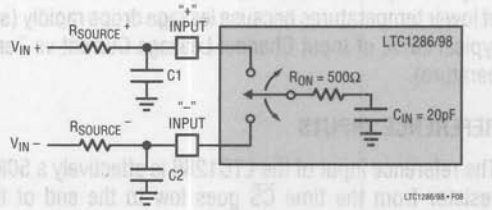

Figure 8. Analog Input Equivalent Circuit

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will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 64µs, the input current equals 1.56µA at V_{IN} = 5V. In this case, a filter resistor of 75Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

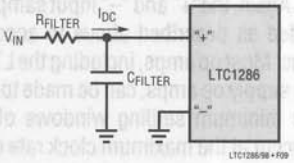

Figure 9. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 240Ω will cause a voltage drop of 240µV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The reference input of the LTC1286 is effectively a 50kΩ resistor from the time $\overline{CS}$ goes low to the end of the conversion. The reference input becomes a high impedence node at any other time (see Figure 10). Since the voltage on the reference input defines the voltage span of the A/D converter, the reference input should be driven by a reference with low R_{OUT} (ex. LT1004, LT1019 and LT1021) or a voltage source with low R_{OUT}.

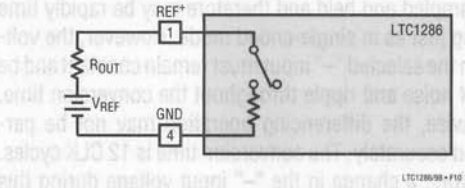

Figure 10. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1298 is limited to 4.5V because the V_{CC} supply and reference are internally tied together. However, the LTC1286 can operate with reference voltages below 1V.

The effective resolution of the LTC1286 can be increased by reducing the input span of the converter. The LTC1286 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Change in Linearity vs Reference Voltage and Change in Gain vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1286 has a larger effect on the output code. When the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Change in Offset vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 122µV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a

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0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1286.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1286 can be reduced to approximately 400μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 400μV noise is only 0.33LSB peak-to-peak. In this case, the LTC1286 noise will contribute virtually no uncertainty to the output code. However, for reduced references the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 2.5V reference this same 400μV noise is 0.66LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 1V, the 400μV noise becomes equal to 1.65LSBs and a stable code may be difficult to achieve. In this case averaging multiple readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used the more critical it becomes to have a clean, noise free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1286 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

DYNAMIC PERFORMANCE

The LTC1286/LTC1298 have exceptional sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1286 plot.

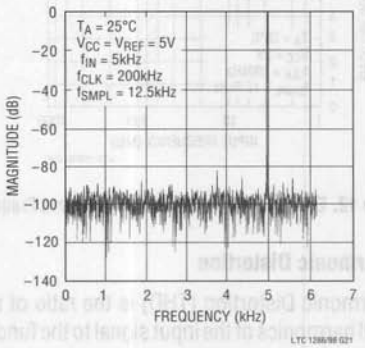

Figure 11. LTC1286 Non-Averaged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio (S/N + D) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 12 shows a typical spectral content with a 12.5kHz sampling rate.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N+D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 12.5kHz with a 5V supply, the LTC1286 maintains above 11 ENOBs at 10kHz input frequency. Above 10kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains low.

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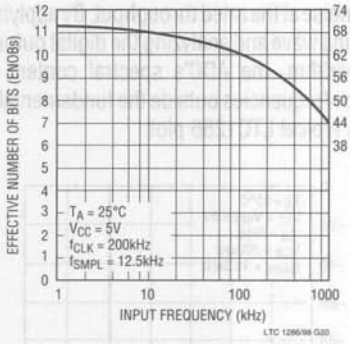

Figure 12. Effective Bits and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the Nth harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 7kHz input signal, the LTC1286/LTC1298 have typical THD of 80dB with V_{CC} = 5V.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20\log\left[\frac{\text{amplitude}\left(f_a \pm f_b\right)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 5kHz and 6kHz, the IMD of the LTC1286/LTC1298 is 73dB with a 5V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 11 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1286/LTC1298 have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency.

TYPICAL APPLICATIONS

MICROPROCESSOR INTERFACES

The LTC1286/LTC1298 can interface directly without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1286/LTC1298. Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts with the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU. The data is right justified into two memory locations. ANDing the second byte with OF_{HEX} clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

MC68HC11 Code

In this example the D_{IN} word configures the input MUX for a single-ended input to be applied to CH0. The conversion result is output MSB-first.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1286/LTC1298

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2,S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS†
HPC16000 Family	MICROWIRE/PLUS†
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port
Intel	
8051	Bit Manipulation on Parallel Port

* Requires external hardware

† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

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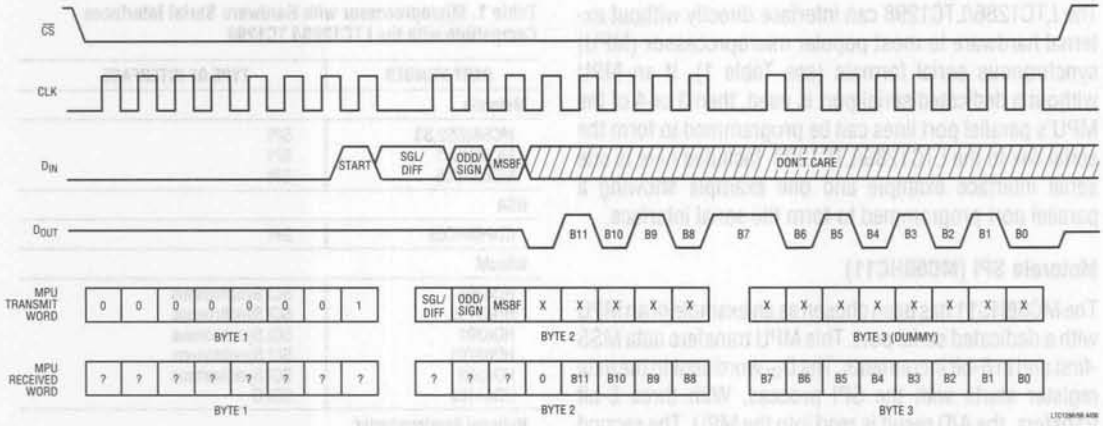
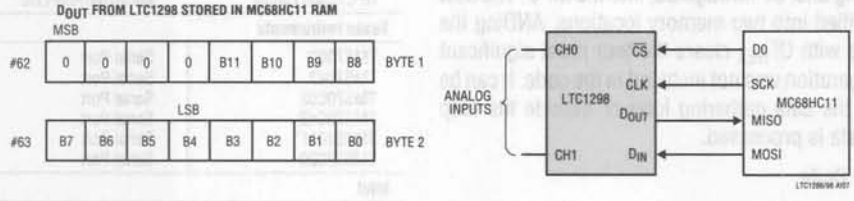
TYPICAL APPLICATIONS

Timing Diagram for Interface to the MC68HC11



Hardware and Software Interface to the MC68HC11



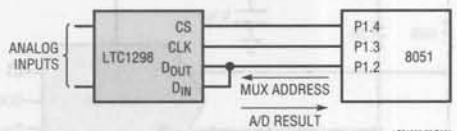
LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR	WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		LDAA	$51	LOAD DIN INTO ACC A FROM $51
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		STAA	$102A	LOAD DIN INTO SPI, START SCK
	STAA	$1009	LOAD DATA INTO PORT D DDR	WAIT2	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	#$01	LOAD DIN WORD INTO ACC A		BPL	WAIT2	CHECK IF TRANSFER IS DONE
	STAA	$50	LOAD DIN DATA INTO $50		LDAA	$102A	LOAD LTC1291 MSBs INTO ACC A
	LDAA	#$A0	LOAD DIN WORD INTO ACC A		STAA	$62	STORE MSBs IN $62
	STAA	$51	LOAD DIN DATA INTO $51		LDAA	$52	LOAD DUMMY INTO ACC A FROM $52
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	STAA	$52	LOAD DUMMY DIN DATA INTO $52				
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
					BPL	WAIT3	CHECK IF TRANSFER IS DONE
LOOP	BCLR	$08,X,#$01	DO GOES LOW (CS GOES LOW)		BSET	$08,X#$01	DO GOES HIGH (CS GOES HIGH)
	LDAA	$50	LOAD DIN INTO ACC A FROM $50		LDAA	$102A	LOAD LTC1291 LSBs IN ACC
	STAA	$102A	LOAD DIN INTO SPI, START SCK		STAA	$63	STORE LSBs IN $63
	LDAA	$1029	CHECK SPI STATUS REG		JMP	LOOP	START NEXT CONVERSION

TYPICAL APPLICATIONS

Interfacing to the Parallel Port of the INTEL 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1298 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1298 tied together as described in the SERIAL INTERFACE section. This saves one wire.

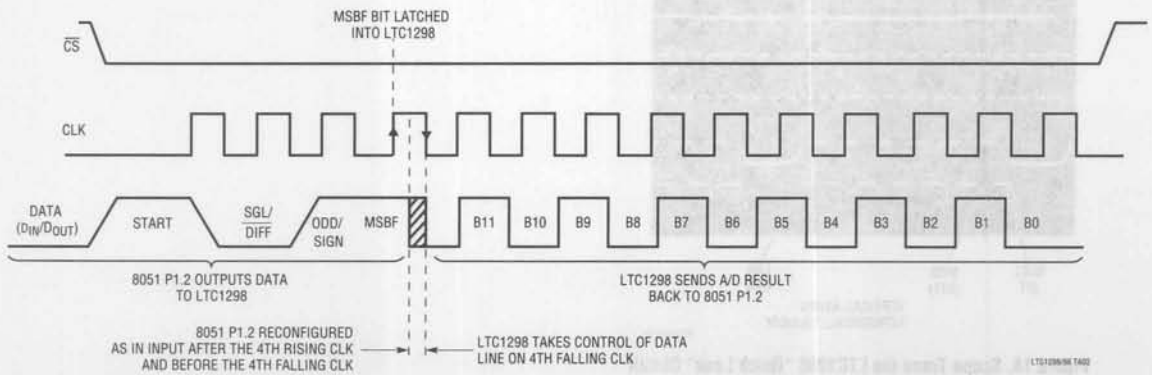
The 8051 first sends the start bit and MUX address to the LTC1298 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 12-bit A/D result over the same data line.



LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1298
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	SCLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1298
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
LOOP 2	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 2	Next bit
	MOV	R2, A	Store MSBs in R2
	CLR	A	Clear Acc.
	MOV	R4, #04	Load counter
LOOP 3	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 3	Next bit
	MOV	R4, #04	Load counter
LOOP 4	RRC	A	Rotate right into Acc.
	DJNZ	R4, LOOP 4	Next Rotate
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ goes high

D_{OUT} FROM 1298 STORED IN 8501 RAM

	MSB							
R2	B11	B10	B9	B8	B7	B6	B5	B4
	LSB							
R3	B3	B2	B1	B0	0	0	0	0



TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1286

Users can get a quick look at the function and timing of the LT1286 by using the following simple circuit (Figure 13). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74C161 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 14). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

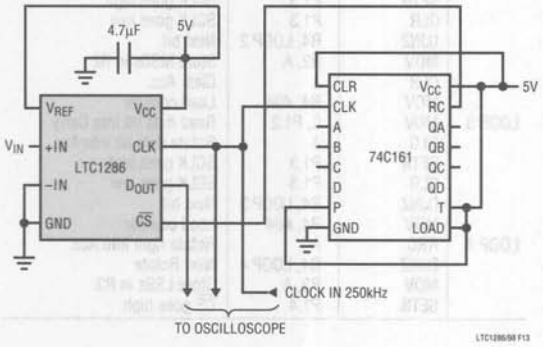


Figure 13. "Quick Look" Circuit for the LTC1286

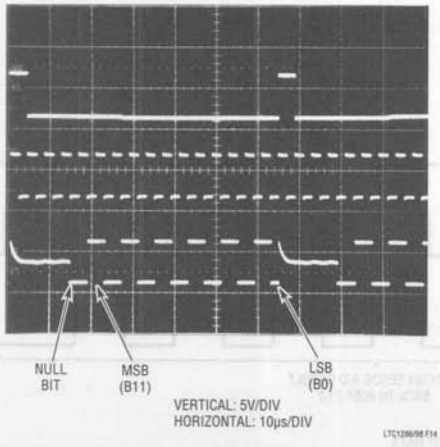


Figure 14. Scope Trace the LTC1286 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

Micropower Battery Voltage Monitor

A common problem in battery systems is battery voltage monitoring. This circuit monitors the 10 cell stack of NiCad or NiMH batteries found in laptop computers. It draws only 67µA from the 5V supply at f_{SMPL} = 0.1kHz and 25µA to 55µA from the battery. The 12-bits of resolution of the LTC1286 are positioned over the desired range of 8V to 16V. This is easily accomplished by using the ADC's differential inputs. Tying the –input to the reference gives an ADC input span of V_{REF} to $2V_{REF}$ (2.5V to 5V). The resistor divider then scales the input voltage for 8V to 16V.

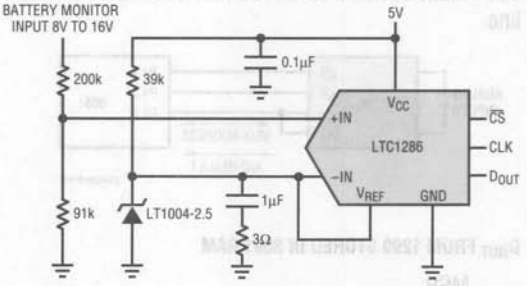


Figure 15. Micropower Battery Voltage Monitor

Single Chip 12-Bit Data Acquisition System

FEATURES

- Built-In Sample-and-Hold
- Single Supply 5V Operation
- Power Shutdown
- Direct 3- or 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- Two-Channel Analog Multiplexer
- Analog Inputs Common Mode to Supply Rails
- 8-Pin DIP Package

KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 12µs Max Over Temp.
- Low Supply Current:
  6.0mA (Typ) Active Mode
  10µA (Max) Shutdown Mode

DESCRIPTION

The LTC1291 is a data acquisition system that contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar A/D conversion. The input multiplexer can be configured for either single-ended or differential inputs. An on-chip sample-and-hold is included on the "+" input. When the LTC1291 is idle, it can be powered down in applications where low power consumption is desired. An external reference is not required because the LTC1291 takes its reference from the power supply (V_{CC}). All these features are packaged in an 8-pin DIP.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three or four wires. Given the accuracy, ease of use and small package size, this device is well suited for digitizing analog signals in remote applications where minimum number of interconnects, small physical size, and low power consumption are important.

LTCMOS™ is a trademark of Linear Technology Corporation

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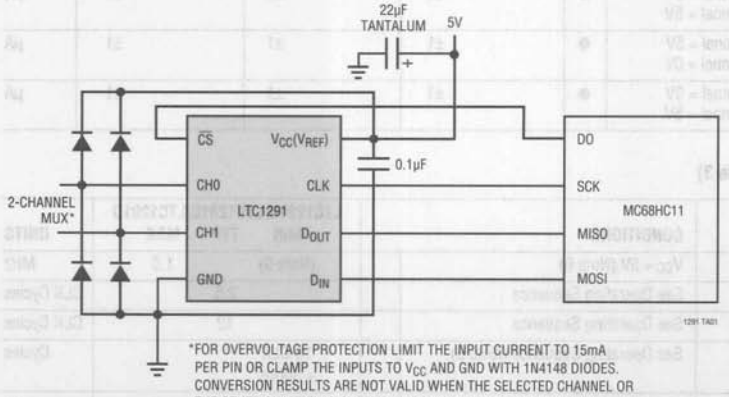
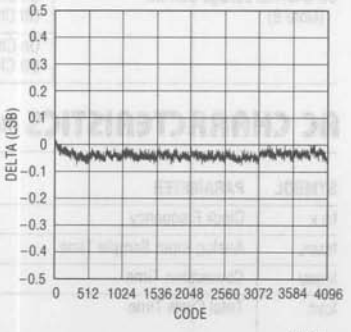
TYPICAL APPLICATION

2-Channel 12-Bit Data Acquisition System



*FOR OVERVOLTAGE PROTECTION LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR THE OTHER CHANNEL IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

Channel-to-Channel INL Matching



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V

Voltage

- Analog Inputs ..... −0.3V to V_{CC} + 0.3V
- Digital Inputs ..... −0.3V to 12V
- Digital Outputs ..... −0.3V to V_{CC} + 0.3V

Power Dissipation 500mW

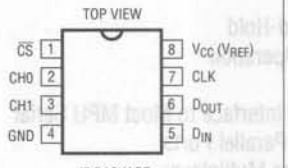
Operating Temperature Range

- LTC1291BC, LTC1291CC, LTC1291DC ..... 0°C to 70°C
- LTC1291BI, LTC1291CI, LTC1291DI ..... −40°C to 85°C
- LTC1291BM, LTC1291CM, LTC1291DM ..... −55°C to 125°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1291BMJ8
LTC1291CMJ8
LTC1291DMJ8
LTC1291BIJ8
LTC1291CIJ8
LTC1291DIJ8
LTC1291BIN8
LTC1291CIN8
LTC1291DIN8
LTC1291BCN8
LTC1291CCN8
LTC1291DCN8

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1291B MIN	LTC1291B TYP	LTC1291B MAX	LTC1291C MIN	LTC1291C TYP	LTC1291C MAX	LTC1291D MIN	LTC1291D TYP	LTC1291D MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Note 4 & 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±1.0			±2.0			±4.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed		●			12			12			12	Bits
Analog Input Range	(Note 7)						−0.05V to V_{CC} + 0.05V					V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		(Note 9)		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			2.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		18 CLK + 500ns			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
t_{dis}	Delay Time, $\overline{CS}\uparrow$ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDI}	Hold Time, D_{IN} after CLK↑	V_{CC} = 5V (Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid after CLK↓				130		ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{suDI}	Setup Time, D_{IN} Stable before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 5V (Note 6)		500			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		18			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel			100		pF
		Analog Inputs Off Channel			5		pF
		Digital Inputs			5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V		●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V		●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}		●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V		●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = –10µA				4.7		V
		V_{CC} = 4.75V, I_{OUT} = –360µA		●	2.4	4.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 1.6mA		●			0.4	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High		●			3	µA
		V_{OUT} = 0V, $\overline{CS}$ High		●			–3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}				20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High		●		6	12	mA
		$\overline{CS}$ High	LTC1291BC, LTC1291CC, LTC1291DC	●		5	10	µA
		Power shutdown CLK Off	LTC1291BI, LTC1291CI, LTC1291DI, LTC1291BM, LTC1291CM, LTC1291DM	●		5	15	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, CLK = 1.0MHz unless otherwise specified.

Note 4: One LSB is equal to V_{CC} divided by 4096. For example, when V_{CC} = 5V, 1LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

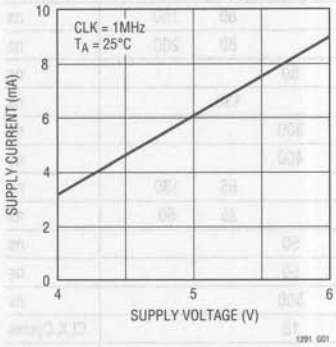
Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 8: Channel leakage current is measured after the channel selection.

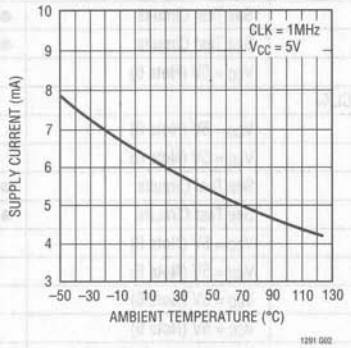
Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 125kHz$ at 125°C, $f_{CLK} \geq 30kHz$ at 85°C and $f_{CLK} \geq 3kHz$ at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

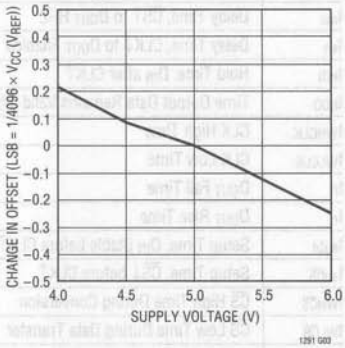
Supply Current vs Supply Voltage



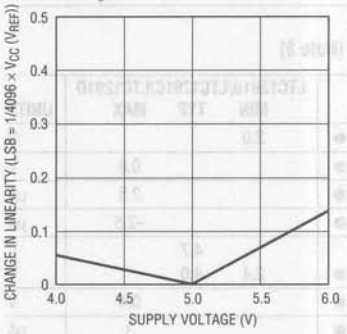
Supply Current vs Temperature



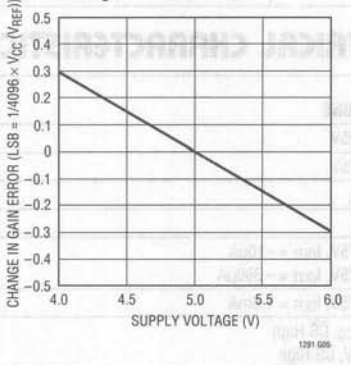
Change in Offset vs Supply Voltage



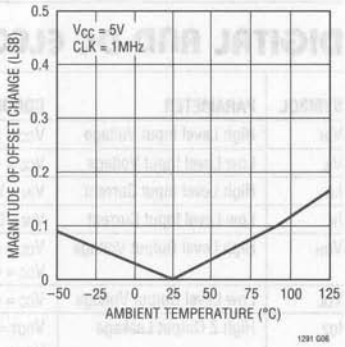
Change in Linearity vs Supply Voltage



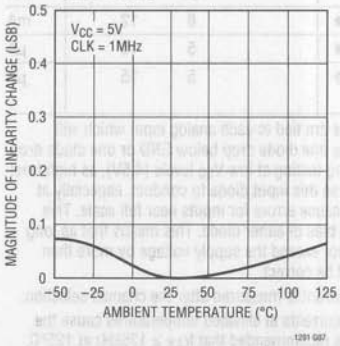
Change in Gain Error vs Supply Voltage



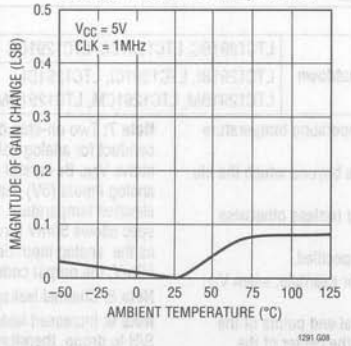
Change in Offset vs Temperature



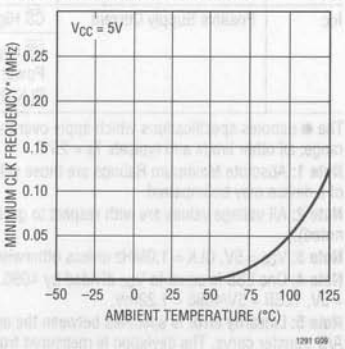
Change in Linearity vs Temperature



Change in Gain vs Temperature



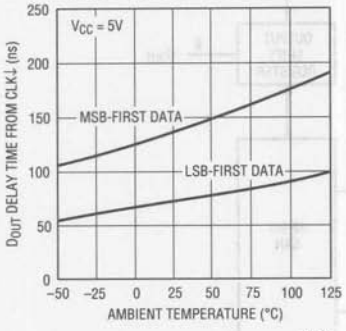
Minimum Clock Rate for 0.1 LSB Error



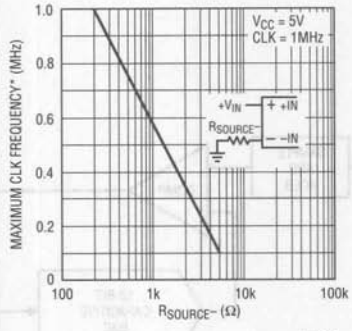
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

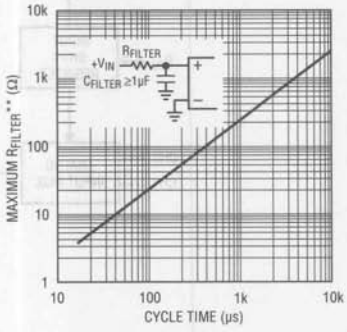
D_{OUT} Delay Time vs Temperature



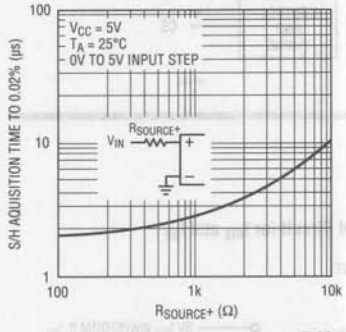
Maximum Clock Rate vs Source Resistance



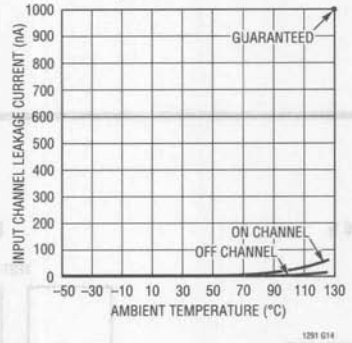
Maximum Filter Resistor vs Cycle Time



Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED.

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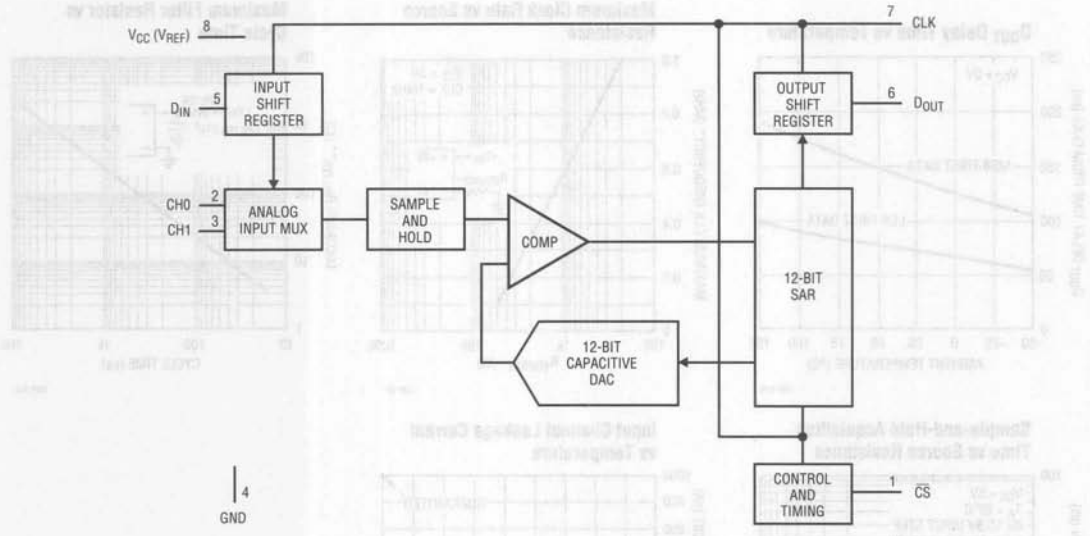
PIN FUNCTIONS

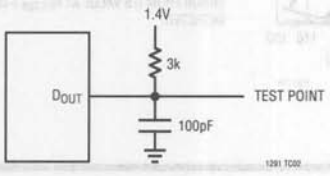
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1291.
2, 3	CH0, CH1	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	D_{IN}	Digital Data Input	The multiplexer address is shifted into this input.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	$V_{CC}(V_{REF})$	Positive Supply and Reference Voltage	This pin provides power and defines the span of the A/D converter. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

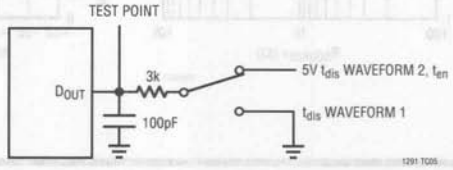


TEST CIRCUITS

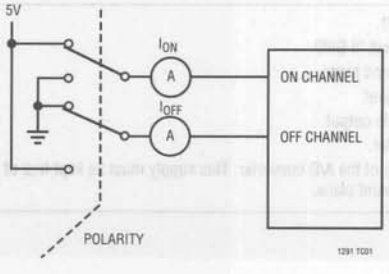
Load Circuit for t_{dDO}, t_r and t_f



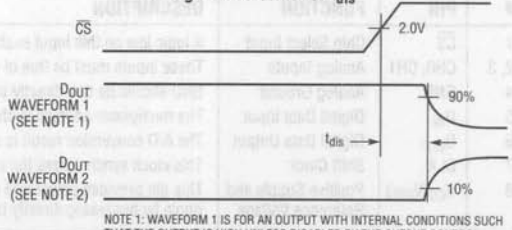
Load Circuit for t_{dis} and t_{en}



On and Off Channel Leakage Current



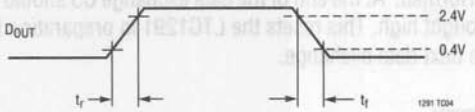
Voltage Waveforms for t_{dis}



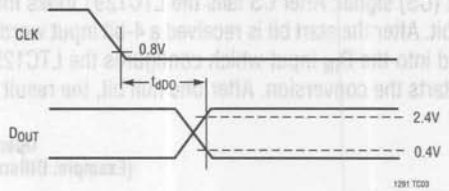
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

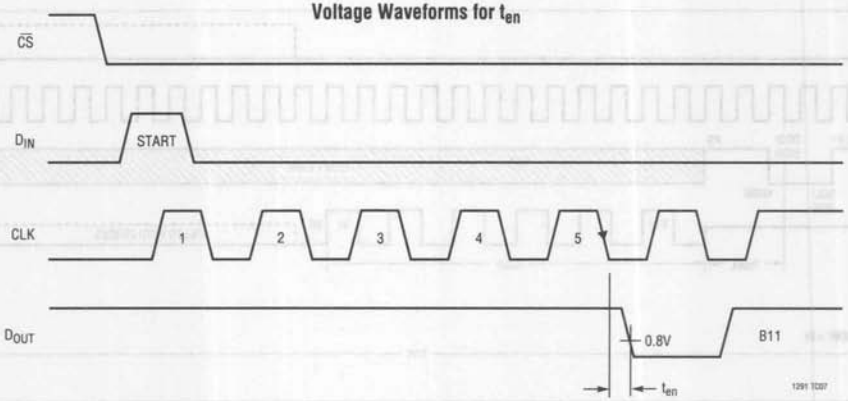
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for t_{en}



6

APPLICATIONS INFORMATION

The LTC1291 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1291 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

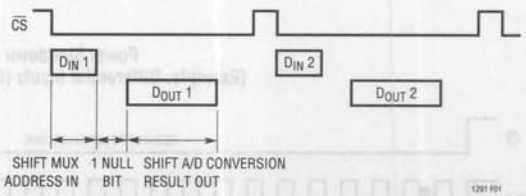


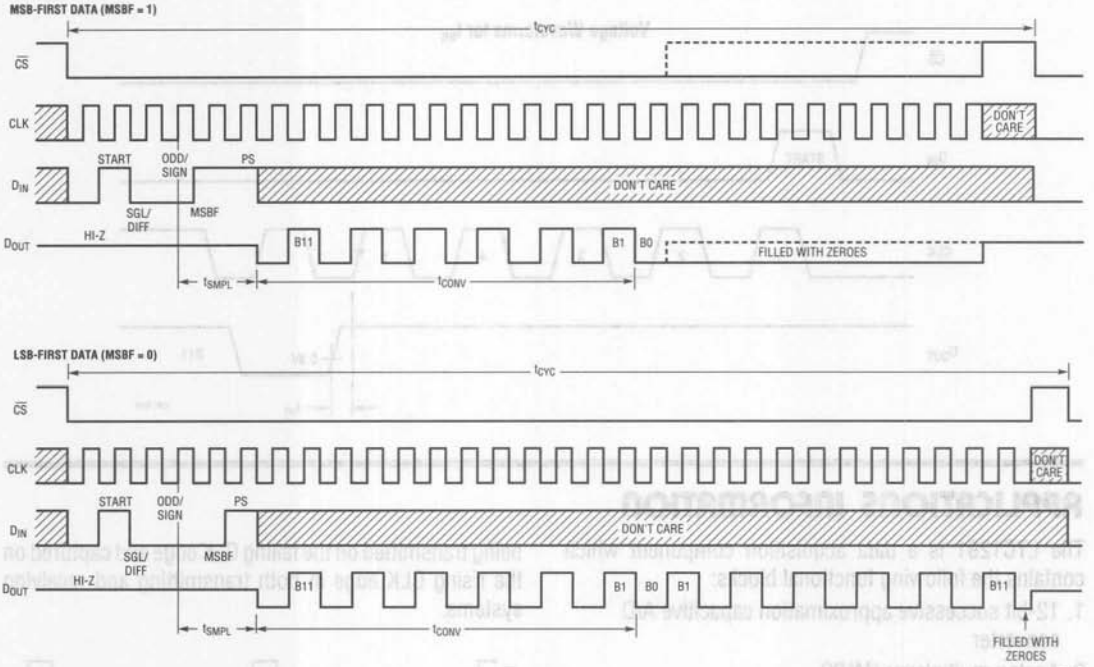
Figure 1

The input data is first received and then the A/D conversion result is transmitted (half duplex). Because of the half duplex operation D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and

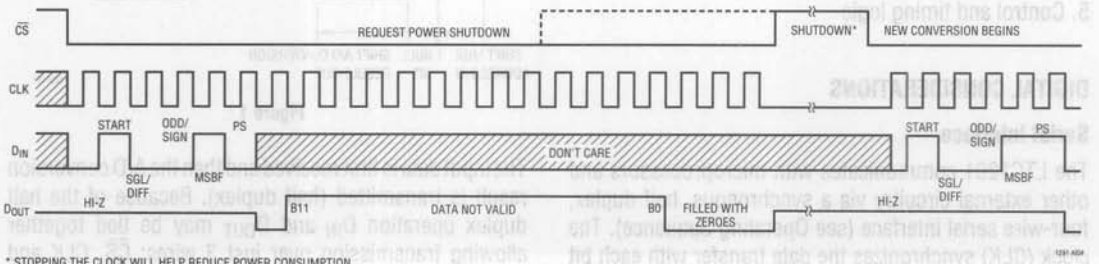
APPLICATIONS INFORMATION

DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1291 looks for a start bit. After the start bit is received a 4-bit input word is shifted into the D_{IN} input which configures the LTC1291 and starts the conversion. After one null bit, the result of the conversion appears MSB-first on the D_{OUT} line. The conversion result is output, bit by bit, as the conversion is performed. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1291 in preparation for the next data exchange.

Operating Sequence
(Example: Differential Inputs (CH0$^+$, CH1$^-$))



Power Shutdown Operating Sequence
(Example: Differential Inputs (CH0$^+$, CH1$^-$) and MSB-First Data)



* STOPPING THE CLOCK WILL HELP REDUCE POWER CONSUMPTION
$\overline{CS}$ CAN BE BROUGHT HIGH ONCE D_{IN} HAS BEEN CLOCKED IN

APPLICATIONS INFORMATION

Input Data Word

The 4-bit data word is clocked into the D_{IN} pin on the rising edge of the clock after chip select goes low and the start bit has been recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:

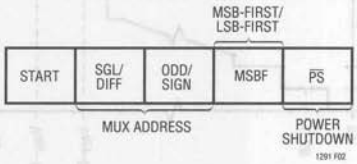


Figure 2. Input Data Word

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeroes which precede this logical one will be ignored. After the start bit is received the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

MUX Address

The bits of the input word following the START BIT assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND. Only the "+" inputs have sample-and-holds. Signals applied at the "–" inputs must not change more than the required accuracy during the conversion.

Multiplexer Channel Selection

MUX ADDRESS		CHANNEL #		
SGL/DIFF	ODD/SIGN	0	1	GND
1	0	+		–
1	1		+	–
0	0	+	–	
0	1	–	+	

MSB-First/LSB-First (MSBF)

The output data of the LTC1291 is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeroes will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line (see Operating Sequence).

Power Shutdown

The power shutdown feature of the LTC1291 is activated by making the $\overline{PS}$ bit a logical zero. If $\overline{CS}$ remains low after the PS bit has been received, a 12-bit D_{OUT} word with all logical ones will be shifted out followed by logical zeroes until $\overline{CS}$ goes high. Then the D_{OUT} line will go into its high impedance state. The LTC1291 will remain in the shutdown mode until the next $\overline{CS}$ cycle. There is no warm-up or wait period required after coming out of the power shutdown cycle so a conversion can commence after $\overline{CS}$ goes low (see Power Shutdown Operating Sequence).

APPLICATIONS INFORMATION

Output Code

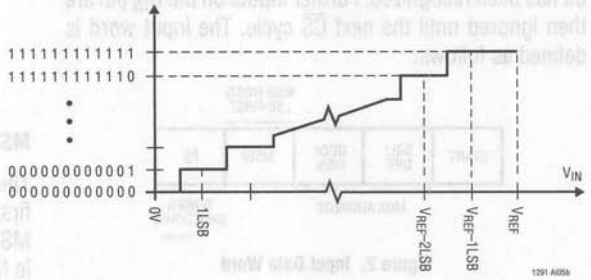
The LTC1291 performs a unipolar conversion. The following shows the output code and transfer curve:

Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
111111111111	V_{REF} – 1LSB	4.9988V
111111111110	V_{REF} – 2LSB	4.9976V
•	•	•
•	•	•
•	•	•
000000000001	1LSB	0.0012V
000000000000	0V	0V

1291 AI05a

Unipolar Transfer Curve



1291 AI05b

Microprocessor Interfaces

The LTC1291 can interface directly (without external hardware) to most popular microprocessors's (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1291. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU. The data is right justified in the two memory locations. ANDing the second byte with $0D_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1291**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

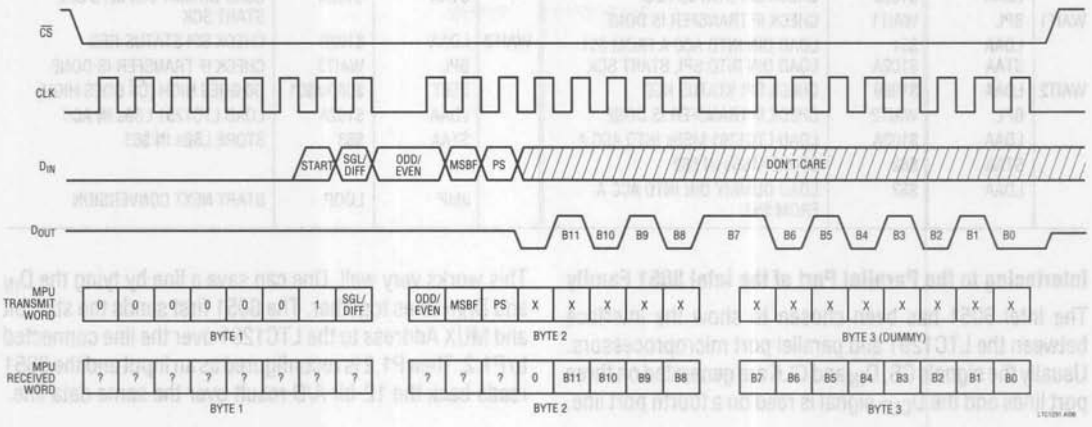
* Requires external hardware

** Contact factory for interface information for processors not on this list

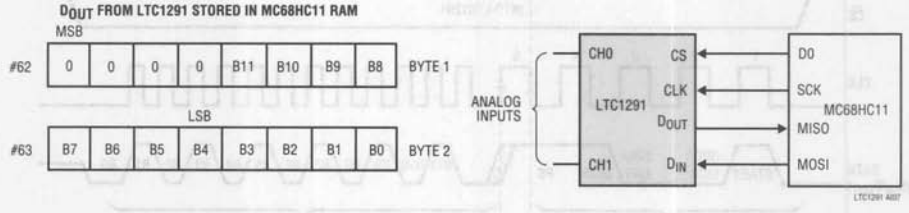
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

Timing Diagram for Interface to the MC68HC11



Hardware and Software Interface to Motorola MC68HC11



MC68HC11 CODE

In this example the D_{IN} word configures the input MUX for a single-ended input to be applied to CH0. The conversion result is output MSB-first.

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR
	STAA	$1028	LOAD DATA INTO SPCR ($1028)
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR
	STAA	$1009	LOAD DATA INTO PORT D DDR
	LDAA	#$03	LOAD DIN WORD INTO ACC A
	STAA	$50	LOAD DIN DATA INTO $50
	LDAA	#$60	LOAD DIN WORD INTO ACC A
	STAA	$51	LOAD DIN DATA INTO $51

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$52	LOAD DUMMY DIN DATA INTO $52
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
LOOP	BCLR	$08,X,#$01	D0 GOES LOW (CS GOES LOW)
	LDAA	$50	LOAD DIN INTO ACC A FROM $50
	STAA	$102A	LOAD DIN INTO SPI, START SCK

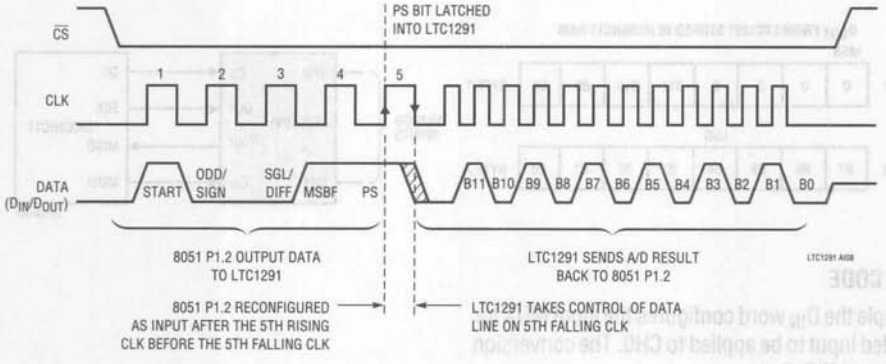
APPLICATIONS INFORMATION

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	$1029	CHECK SPI STATUS REG		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE				
	LDAA	$51	LOAD DIN INTO ACC A FROM $51	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
	STAA	$102A	LOAD DIN INTO SPI, START SCK		BPL	WAIT3	CHECK IF TRANSFER IS DONE
WAIT2	LDAA	$1029	CHECK SPI STATUS REG		BSET	$08,X#$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	BPL	WAIT2	CHECK IF TRANSFER IS DONE		LDAA	$102A	LOAD LTC1291 LSBs IN ACC
	LDAA	$102A	LOAD LTC1291 MSBs INTO ACC A		STAA	$63	STORE LSBs IN $63
	STAA	$62	STORE MSBs IN $62				
	LDAA	$52	LOAD DUMMY DIN INTO ACC A FROM $52		JMP	LOOP	START NEXT CONVERSION

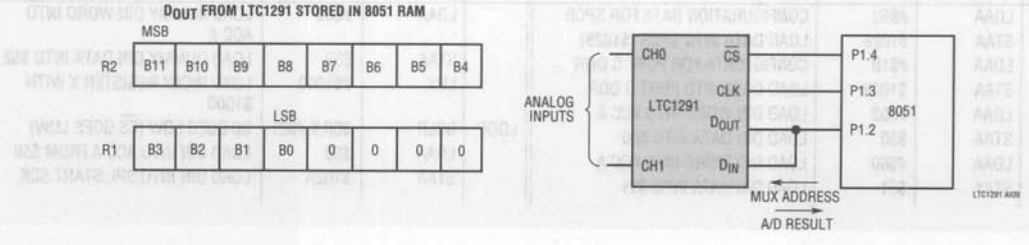
Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1291 and parallel port microprocessors. Usually the signals $\overline{CS}$, D_{IN} and CLK are generated on three port lines and the D_{OUT} signal is read on a fourth port line. This works very well. One can save a line by tying the D_{IN} and D_{OUT} lines together. The 8051 first sends the start bit and MUX Address to the LTC1291 over the line connected to P1.2. Then P1.2 is reconfigured as an input and the 8051 reads back the 12-bit A/D result over the same data line.

Timing Diagram for Interface to Intel 8051



Hardware and Software Interface to Intel 8051



APPLICATIONS INFORMATION

8051 Code

In this example the input MUX is configured to accept a differential input between CH0 and CH1. The result from the conversion is clocked out MSB-first.

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	SETB	P1.4	$\overline{CS}$ GOES HIGH		CLR	P1.3	CLK GOES LOW
CONT	MOV	A,#98H	DIN WORD FOR LTC1291		CLR	A	CLEAR ACC
	CLR	P1.4	$\overline{CS}$ GOES LOW		RLC	A	ROTATE DATA BIT (B3) INTO ACC
	MOV	R4,#05H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP1	RLC	A	ROTATE DIN BIT INTO CARRY		RLC	A	ROTATE DATA BIT (B2) INTO ACC
	CLR	P1.3	CLK GOES LOW		SETB	P1.3	CLK GOES HIGH
	MOV	P1.2,C	OUTPUT DIN BIT TO LTC1291		CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH		MOV	C,P1.2	READ DATA BIT INTO CARRY
	DJNZ	R4,LOOP1	NEXT DIN BIT		RLC	A	ROTATE DATA BIT (B1) INTO ACC
	MOV	P1,#04H	P1.2 BECOMES AN INPUT		SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW		CLR	P1.3	CLK GOES LOW
	MOV	R4,#09H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP	MOV	C,P1.2	READ DATA BIT INTO CARRY		SETB	P1.4	$\overline{CS}$ GOES HIGH
	RLC	A	ROTATE DATA BIT (B3) INTO ACC		RRC	A	ROTATE DATA BIT (B0) INTO ACC
	SETB	P1.3	CLK GOES HIGH		RRC	A	ROTAGE RIGHT INTO ACC
	CLR	P1.3	CLK GOES LOW		RRC	A	ROTAGE RIGHT INTO ACC
	DJNZ	R4,LOOP	NEXT DOUT BIT		RRC	A	ROTAGE RIGHT INTO ACC
	MOV	R2,A	STORE MSBS IN R2		MOV	R3,A	STORE LSBs IN R3
	MOV	C,P1.2	READ DATA BIT INTO CARRY		AJMP	CONT	START NEXT CONVERSION
	SETB	P1.3	CLK GOES HIGH				

Sharing the Serial Interface

The LTC1291 can share the same 3-wire serial interface with other peripheral components or other LTC1291s (Figure 3). The $\overline{CS}$ signals decide which LTC1291 is being addressed by MPU.

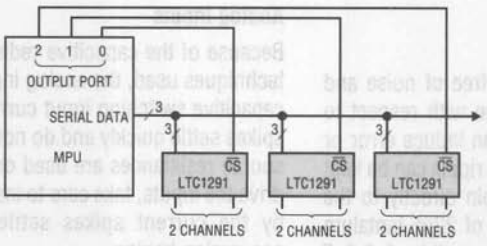


Figure 3. Several LTC1291s Sharing One 3-Wire Serial Interface

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

Grounding

The LTC1291 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length. Figure 4 shows an example of an ideal LTC1291 ground plane for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

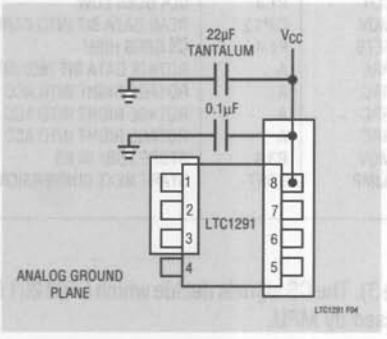


Figure 4. Example Ground Plane for the LTC1291

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during the conversion cycle can induce error or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. A 0.1µF ceramic disk capacitor should also be placed directly across V_{CC} (Pin 8) and GND (Pin 4) as close to the pins as possible. The V_{CC} supply should have a low output impedance such as that obtained from a voltage regulator (e.g., LT323A). Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

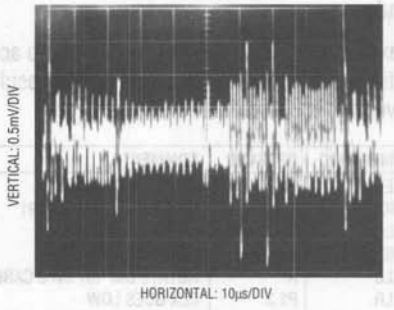


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

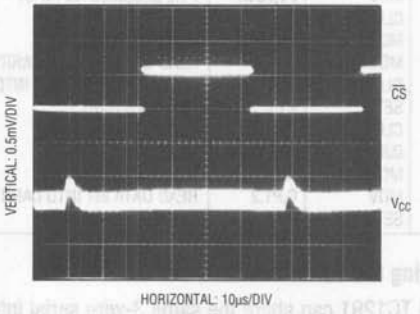


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1291 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

Minimizing Gain and Offset Error

Because the LTC1291's reference is taken from the power supply pin (V_{CC}) proper PC board layout and supply bypassing is important for attaining the best performance from the A/D converter. Any parasitic resistance in the V_{CC}

APPLICATIONS INFORMATION

or GND lead will cause gain errors and offset errors (Figure 7). For the best performance the LTC1291 should be soldered directly to the PC board. If the source can not be placed next to the pin and the gain parameter is important the pin should be Kelvin-sensed to eliminate parasitic resistances due to long PC traces. For example, 0.1Ω of resistance in the V_{CC} lead can typically cause 0.5LSB ($I_{CC} \times 0.1\Omega/V_{CC}$) of gain error for V_{CC} = 5V.

When the input MUX is selected for single-ended input the minus terminal is connected to GND internally on the die. Any parasitic resistance from the GND pin to the ground plane will lead to an offset voltage ($I_{CC} \times R_{P2}$).

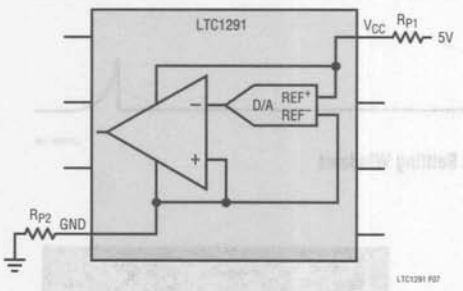


Figure 7. Parasitic Resistance in the V_{CC} and GND Leads

Source Resistance

The analog inputs of the LTC1291 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}). C_{IN} gets switched between "+" and "–" inputs once during each conversion cycle. Large external source resistors

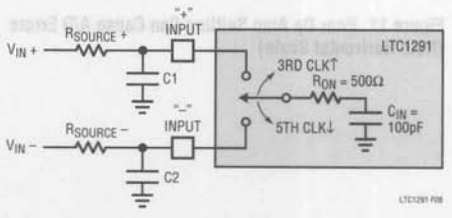


Figure 8. Analog Input Equivalent Circuit

and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 9). The sample period is 2.5 CLK cycles before a conversion starts. The voltage on the "+" input must settle completely within the sample period. Minimizing $R_{SOURCE+}$ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 2.5µs, **$R_{SOURCE+}$ < 1.0k and C1 < 20pF will provide adequate settle time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 9). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing $R_{SOURCE-}$ and C2 will improve settling time. If large "–" input source resistance must be used, the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **$R_{SOURCE-}$ < 250Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figure 9). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 2.5µs ("+" input) and 1µs ("–" input) that occurs at the maximum clock rate of 1MHz. Figures 10 and 11 show examples adequate and poor op amp settling.

APPLICATIONS INFORMATION

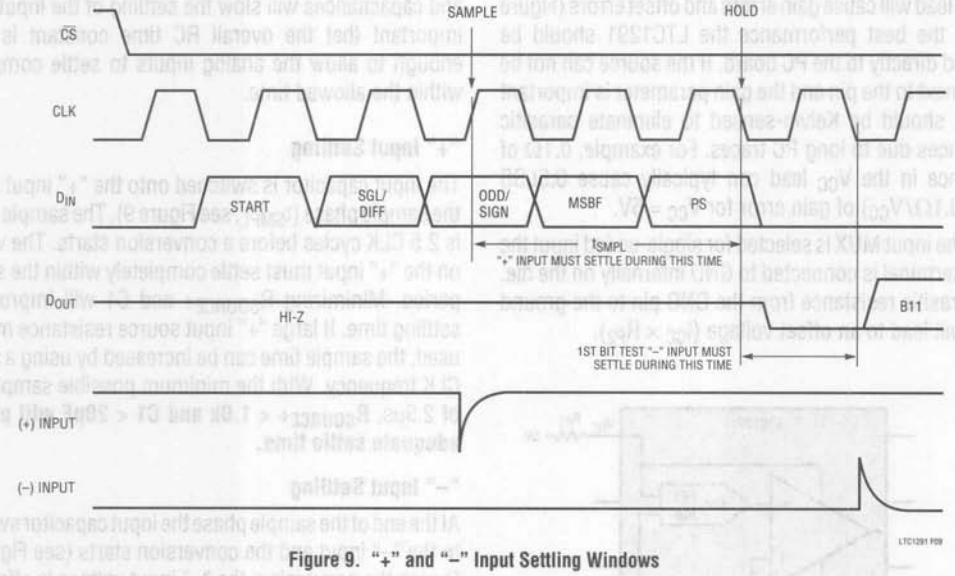


Figure 9. "+" and "–" Input Settling Windows

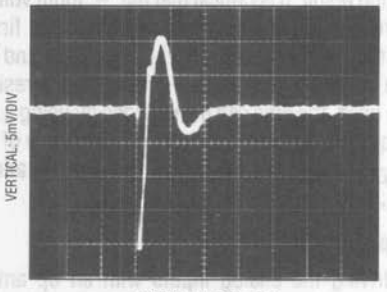


Figure 10. Adequate Settling of Op Amp Driving Analog Input

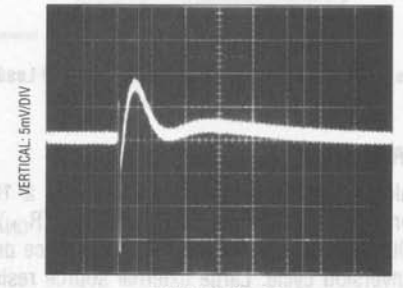


Figure 11. Poor Op Amp Settling Can Cause A/D Errors (Note Horizontal Scale)

APPLICATIONS INFORMATION

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 12. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and a large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 18.5µs, the input current equals 27µA at $V_{IN} = 5V$. Here a filter resistor of 4.5Ω will cause 0.1LSB of full-scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristics curve Maximum Filter Resistor vs Cycle Time.

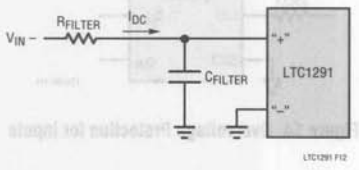


Figure 12. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1291 provides a built-in sample-and-hold (S/H) function on the +IN input for signals acquired in the single-ended mode (–IN pin grounded). The sample-and-hold allows the LTC1291 to convert rapidly varying signals (see typical performance characteristics curve of S/H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 9. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling edge of the PS bit is received. On this falling edge the S/H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time varying. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2pf_{(-IN)}V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (300µV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)} = \left(\frac{V_{ERROR(MAX)}}{2pV_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (300µV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz.

6

APPLICATIONS INFORMATION

Overvoltage Protection

Applying signals to the LTC1291's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1291. It can also happen if the input source is operating from supplies of larger value than the LTC1291 supply. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source.

There are two ways to protect the inputs. In Figure 13 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 250Ω when clocked at its maximum clock frequency of 1MHz. If the LTC1291 is clocked at the maximum clock frequency and 250Ω is not enough to current limit the input source then the clamp diodes are recommended (Figures 14 and 15). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the typical performance characteristics Maximum CLK Frequency vs Source Resistance).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

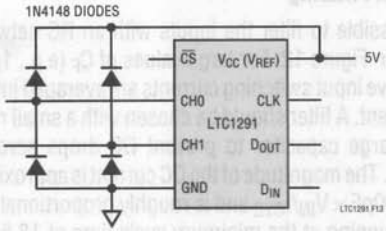


Figure 13. Overvoltage Protection for Inputs

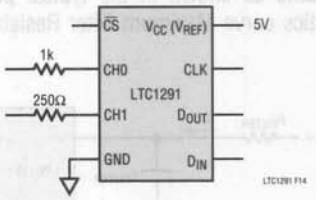


Figure 14. Overvoltage Protection for Inputs

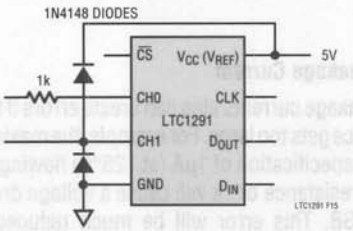


Figure 15. Overvoltage Protection for Inputs

APPLICATIONS INFORMATION

A "Quick Look" Circuit for the LTC1291

Users can get a quick look at the function and timing of the LTC1291 by using the following simple circuit (Figure 16). D_{IN} is tied to V_{CC}. This requires V_{IN} be applied to CH1 with respect to the ground plane. The data is output MSB-first. $\overline{CS}$ is driven at 1/64 the clock frequency by the 74HC393 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on a oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 17).

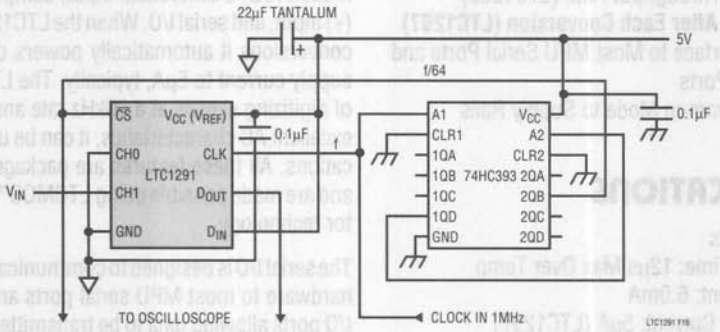


Figure 16. "Quick Look" Circuit for the LTC1291

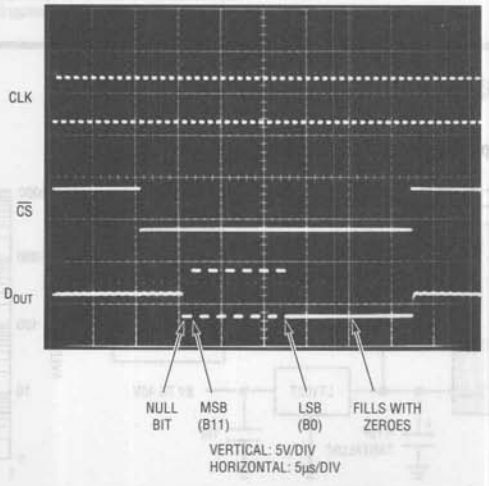


Figure 17. Scope Trace of the LTC1291 "Quick Look" Circuit Showing Output 101010101010 (AAA_{HEX})

Single Chip 12-Bit Data Acquisition Systems

FEATURES

- Built-In Sample-and-Hold
- **Single Supply 5V Operation**
- 60kHz Maximum Throughput Rate (LTC1292)
- **Power Shutdown After Each Conversion (LTC1297)**
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- Analog Inputs Common Mode to Supply Rails

KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 12µs Max Over Temp
- Low Supply Current: 6.0mA
- Shutdown Supply Current: 5µA (LTC1297)

DESCRIPTION

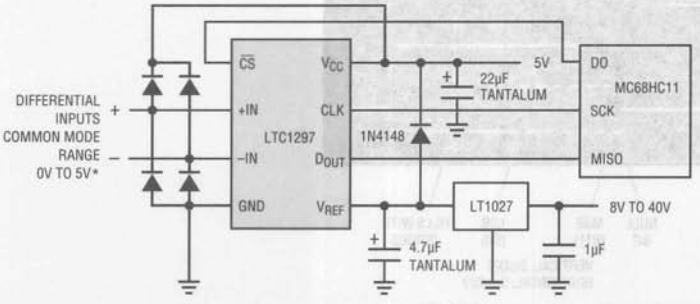
The LTC1292/LTC1297 are data acquisition systems that contain a 12-bit, switched-capacitor successive approximation A/D, a differential input, sample-and-hold on the (+) input, and serial I/O. When the LTC1297 is idle between conversions it automatically powers down reducing the supply current to 5µA, typically. The LTC1292 is capable of digitizing signals at a 60kHz rate and with the device's excellent AC characteristics, it can be used for DSP applications. All these features are packaged in an 8-pin DIP and are made possible using LTCMOS™ switched-capacitor technology.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three wires. Because of their accuracy, ease of use and small package size these devices are well suited for digitizing analog signals in remote applications where minimum number of interconnects and power consumption are important.

LTCMOS is trademark of Linear Technology Corporation

TYPICAL APPLICATION

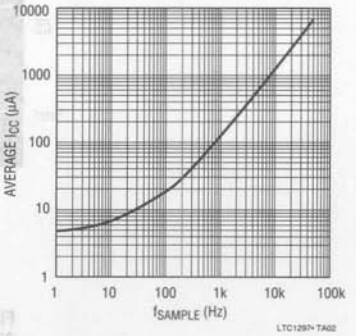
12-Bit Differential Input Data Acquisition System



*FOR OVERVOLTAGE PROTECTION LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN ANY INPUT IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

LTC1292/7 TA01

Power Supply Current vs Sampling Frequency



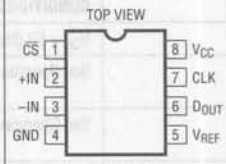
LTC1297• TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference Inputs ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1292/LTC1297BC, LTC1292/LTC1297CC, LTC1292/LTC1297DC ..... 0°C to 70°C
  LTC1292/LTC1297BI, LTC1292/LTC1297CI, LTC1292/LTC1297DI ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER	
LTC1292BIN8	LTC1297BIN8
LTC1292CIN8	LTC1297CIN8
LTC1292DIN8	LTC1297DIN8
LTC1292BCJ8	LTC1297BCJ8
LTC1292CCJ8	LTC1297CCJ8
LTC1292DCJ8	LTC1297DCJ8
LTC1292BCN8	LTC1297BCN8
LTC1292CCN8	LTC1297CCN8
LTC1292DCN8	LTC1297DCN8

For Military Temperature Ranges please contact factory.

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1292B LTC1297B MIN	TYP	MAX	LTC1292C LTC1297C MIN	TYP	MAX	LTC1292D LTC1297D MIN	TYP	MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Note 4 & 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±0.5			±1.0			±4.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed				12			12			12		Bits
Analog and REF Input Range	(Note 7)	●				−0.05V to V_{CC} + 0.05V						V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

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AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)			(Note 9)		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence	LTC1292 LTC1297			1.5CLK 0.5CLK+5.5µs		
t_{CONV}	Conversion Time	See Operating Sequence				12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)	LTC1292 LTC1297			14CLK+2.5µs 14CLK+6µs		
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits		●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits		●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits		●		80	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓					130		ns
t_f	D_{OUT} Fall Time	See Test Circuits		●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits		●		25	50	ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)			300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)			400			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before CLK↑ (LTC1297 Wakeup Time)	V_{CC} = 5V (Note 6)	LTC1292 LTC1297		50 5.5			ns µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V (Note 6)	LTC1292 LTC1297		2.5 0.5			µs µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)	LTC1292 LTC1297		14CLK 14CLK+5.5µs			
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs				100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA I_O = 360µA	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			20		mA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
I_{CC}	Positive Supply Current	$\overline{CS}$ High	LTC1292	●		6	12	mA
		$\overline{CS}$ Low	LTC1297	●		6	12	mA
		$\overline{CS}$ High Power Shutdown CLK Off	LTC1297BC, LTC1297CC, LTC1297DC	●		5	10	µA
			LTC1297BI, LTC1297CI, LTC1297DI LTC1297BM, LTC1297CM, LTC1297DM	●		5	15	µA
I_{REF}	Reference Current	$\overline{CS}$ High		●		10	50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, V_{REF} = 5V, CLK = 1.0MHz unless otherwise specified.

Note 4: One LSB is equal to V_{REF} divided by 4096. For example, when V_{REF} = 5V, 1LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

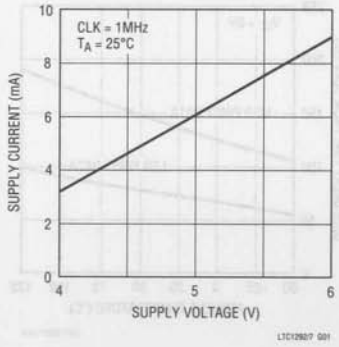
Note 8: Channel leakage current is measured after the channel selection.

Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 125kHz$ at 125°C, $f_{CLK} \geq 31kHz$ at 85°C, and $f_{CLK} \geq 3kHz$ at 25°C.

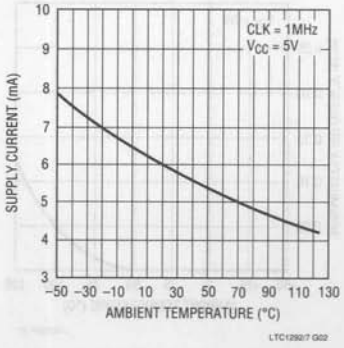
6

TYPICAL PERFORMANCE CHARACTERISTICS

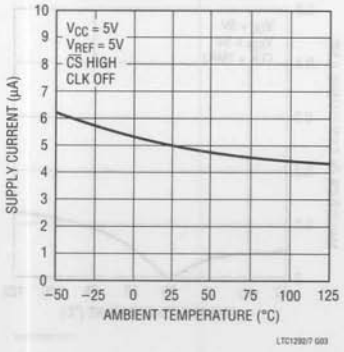
Supply Current vs Supply Voltage



Supply Current vs Temperature

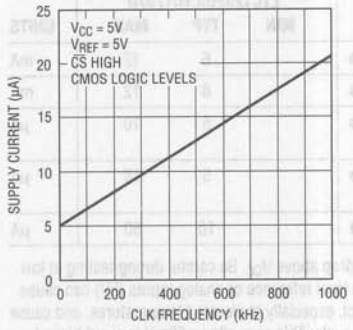


LTC1297 Supply Current (Power Shutdown) vs Temperature

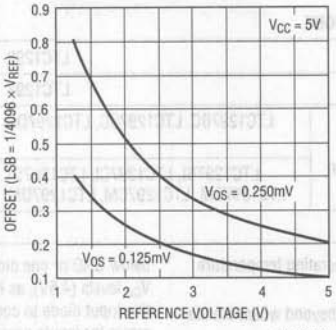


TYPICAL PERFORMANCE CHARACTERISTICS

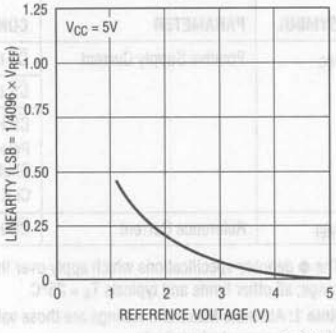
LTC1297 Supply Current (Power Shutdown) vs CLK Frequency



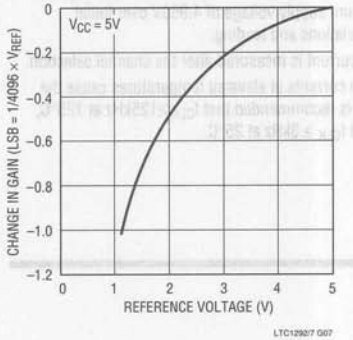
Unadjusted Offset Voltage vs Reference Voltage



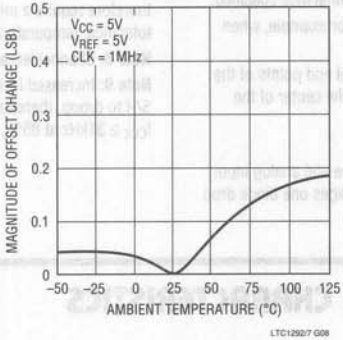
Change in Linearity vs Reference Voltage



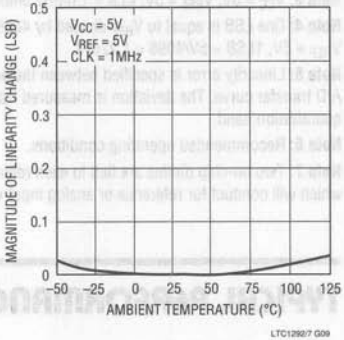
Change in Gain vs Reference Voltage



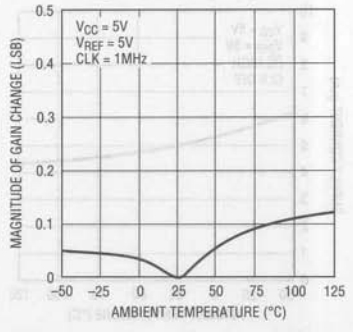
Change in Offset vs Temperature



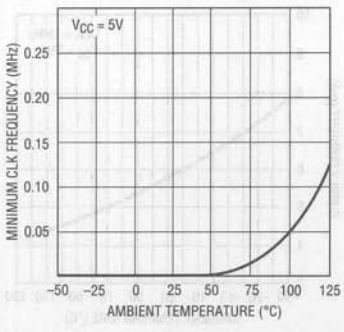
Change in Linearity vs Temperature



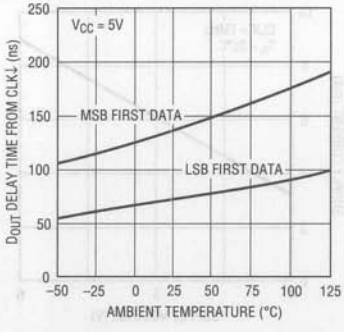
Change in Gain vs Temperature



Minimum Clock Rate for 0.1 LSB Error*



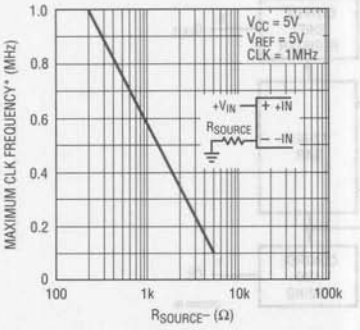
D_{OUT} Delay Time vs Temperature



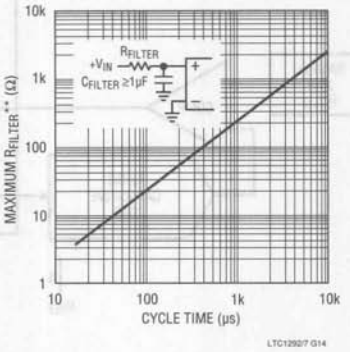
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED (NOTE 9).

TYPICAL PERFORMANCE CHARACTERISTICS

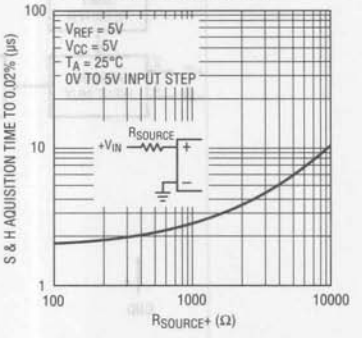
Maximum Clock Rate vs Source Resistance



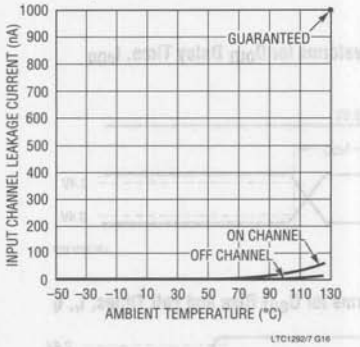
Maximum Filter Resistor vs Cycle Time



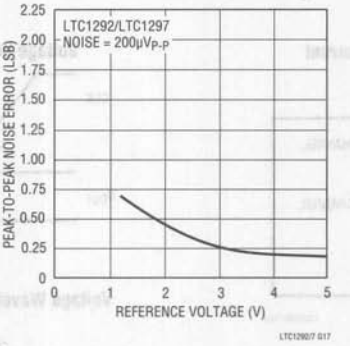
Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT $R_{FILTER} = 0\Omega$ IS FIRST DETECTED.

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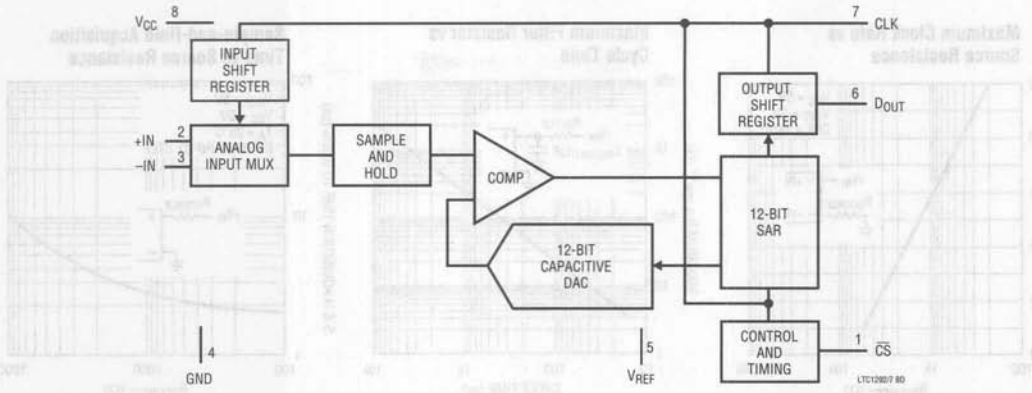
PIN FUNCTIONS

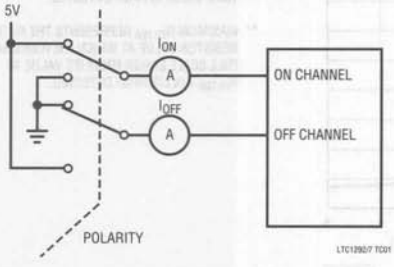
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1292/LTC1297. Power shutdown is activated on the LTC1297 when $\overline{CS}$ is brought high.
2, 3	+IN, –IN	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	V_{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

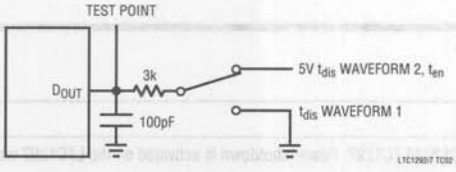


TEST CIRCUITS

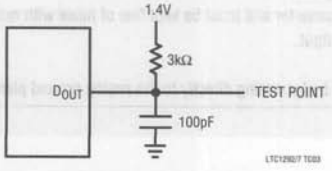
On and Off Channel Leakage Current



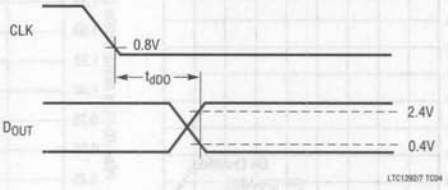
Load Circuit for t_{dis} and t_{en}



Load Circuit for t_{dDO}, t_r and t_f

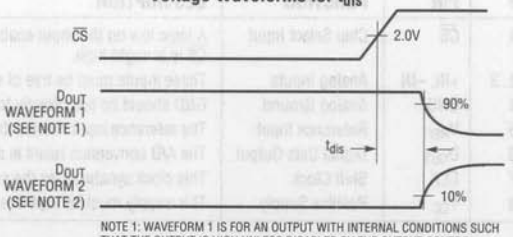


Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

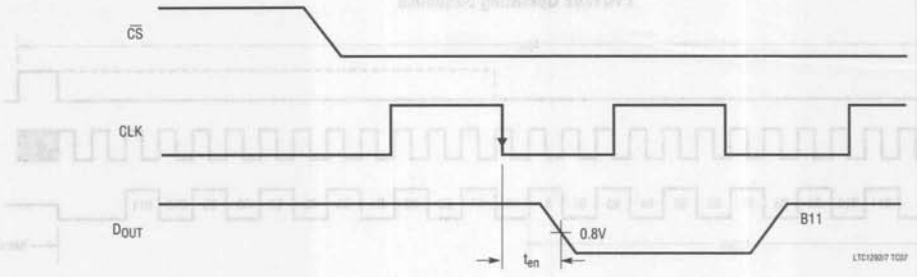
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

The LTC1292/LTC1297 are data acquisition components which contain the following functional blocks:

1. 12-Bit Succesive Approximation Capacitive A/D Converter
2. Differential Input
3. Sample-and-Hold (S/H)
4. Synchronous, Half-Duplex Serial Interface
5. Control and Timing Logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1292/LTC1297 communicate with microprocessors and other external circuitry via a synchronous, half-duplex, three-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge. The LTC1292/LTC1297 do not require a configuration input word and have no D_{IN} pin. They are permanently configured to have a single differential input and to perform a unipolar conversion. A falling $\overline{CS}$ initiates data transfer. To allow the LTC1297 to recover from the power shutdown mode, $t_{su\overline{CS}}$ has to be met. Then the first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line with a MSB-first sequence followed by a LSB-first sequence. With the half-duplex serial interface the D_{OUT} data is from the current conversion. This provides easy interface to MSB-first or LSB-first serial ports. Bringing $\overline{CS}$ high resets the LTC1292/LTC1297 for the next data exchange and puts the LTC1297 into its power shutdown mode.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1292/LTC1297**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

* Requires external hardware

** Contact factory for interface information for processors not on this list

† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

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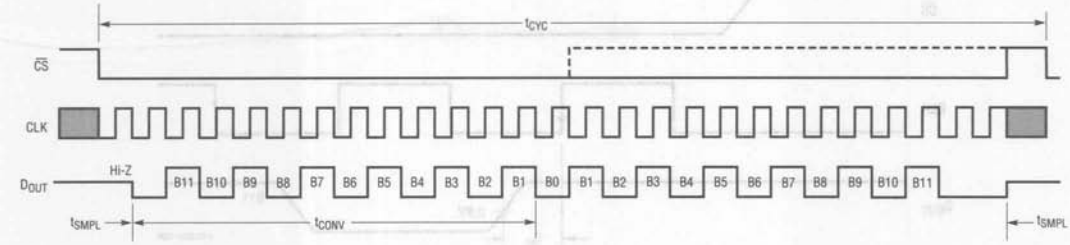
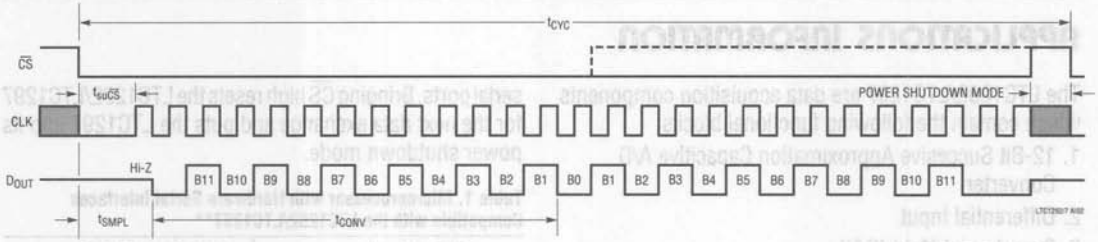
APPLICATIONS INFORMATION

LTC1292 Operating Sequence



LTC1297 Operating Sequence



Microprocessor Interfaces

The LTC1292/LTC1297 can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1292/LTC1297. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. A dummy D_{IN} word sent to the data register starts the SPI process. With two 8-bit transfers, the A/D result is read into the MPU (Figure 1). For the LTC1292 the first 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits B7 through B0 into

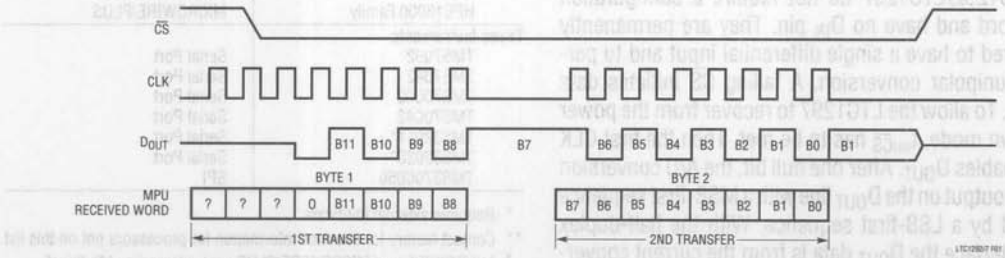


Figure 1. Data Exchange Between LTC1292 and MC68HC11

APPLICATIONS INFORMATION

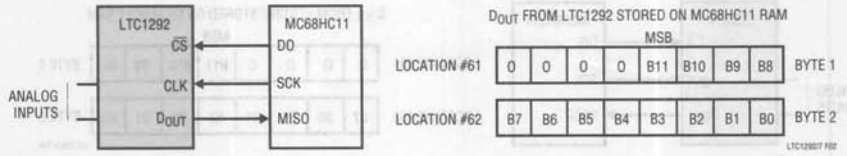


Figure 2. Hardware and Software Interface to Motorola MC68HC11 Microcontroller

MC68HC11 CODE for LTC1292 Interface

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR
	STAA	$1028	LOAD DATA INTO SPCR ($1028)
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR
	STAA	$1009	LOAD DATA INTO PORT D DDR
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$50	LOAD DUMMY DIN DATA INTO $50
LOOP	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
	LDAB	#$00	LOAD ACC B WITH $00
	LDAA	$50	LOAD DUMMY DIN INTO ACC A FROM $50
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	NOP		DELAY $\overline{CS}$ FALL TIME TO RIGHT JUSTIFY DATA
	STAB	$08, X	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	NOP		6 NOPS FOR TIMING
	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	$102A	LOAD LTC1292 MSBs INTO ACC A
	STAA	$61	STORE MSBs IN $61
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	NOPS		6 NOPS FOR TIMING
	BSET	$08,X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAA	$1029	CHECK SPI STATUS REGISTER
	LDAA	$102A	LOAD LTC1292 LSBs IN ACC
	STAA	$62	STORE LSBs IN $62
	JMP	LOOP	START NEXT CONVERSION

the MPU. The data is right-justified in the two memory locations (Figure 2). This was made possible by delaying the falling edge of $\overline{CS}$ till after the second CLK. ANDing the first byte with $0F_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

For the LTC1297 (Figure 3) a delay must be introduced to accommodate the setup time, $t_{su\overline{CS}}$, before the dummy D_{IN} word is sent to the data register. The first 8-bit transfer clocks B11 through B6 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits B5 through B0 into the MPU. Note B1 and B2 from the LSB-first data word have also been clocked in.

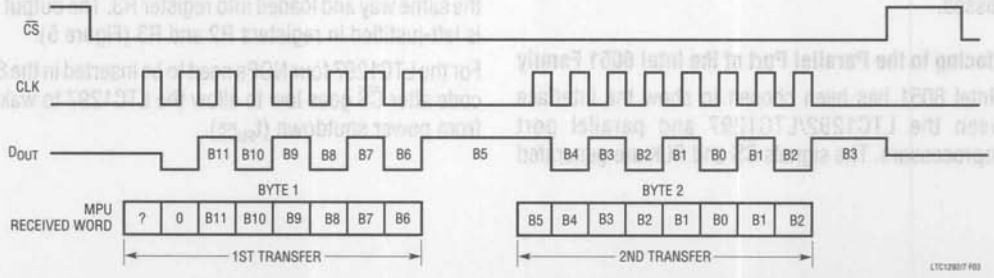


Figure 3. Data Exchange Between LTC1297 and MC68HC11

APPLICATIONS INFORMATION

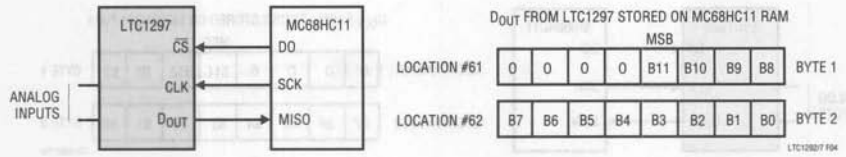


Figure 4. Hardware and Software Interface to Motorola MC68HC11 Microcontroller

MC68HC11 CODE for LTC1297 Interface

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR
	STAA	$1028	LOAD DATA INTO SPCR ($1028)
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR
	STAA	$1009	LOAD DATA INTO PORT D DDR
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$50	LOAD DUMMY DIN DATA INTO $0
LOOP	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
	LDAB	#$00	LOAD ACC B WITH $00
	LDAA	$50	LOAD DIN INTO ACC FROM $50
	BCLR	$08,X,$01	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	NOP		3 NOP FOR $t_{su\overline{CS}}$ TIMING
	NOP		
	NOP		
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START CLK
LOOP1	LDAA	$1029	CHECK SPI STATUS REG
	BPL	LOOP1	CHECK IF TRANSFER IS DONE
	LDAA	$102A	LOAD LTC1297 MSBs INTO ACC A
	STAA	$61	STORE MSBs IN $61
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
LOOP2	LDAA	$1029	CHECK SPI STATUS RES
	BPL	LOOP2	CHECK IF TRANSFER IS DONE
	BSET	$08X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAA	$102A	LOAD LTC1297 LSBs INTO ACC A
	STAA	$62	STORE LSBs IN $62
	ROR	$61	ROTATE RIGHT WITH CARRY
	ROR	$62	NEEDED TO RIGHT JUSTIFY
	ROR	$61	THE DATA IN $61 AND $62
	ROR	$62	
	JMP	LOOP	START NEXT CONVERSION

The data is right- justified in the two memory locations by rotating right twice (Figure 4). ANDing the first byte with $0F_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1292/LTC1297 and parallel port microprocessors. The signals $\overline{CS}$ and CLK are generated on two port lines and the D_{OUT} signal is read on a third port line. After a falling CLK edge each data bit is loaded into the carry bit and then rotated into the accumulator. Once the first 8 MSBs have been shifted into the accumulator they are loaded into register R2. The last four bits are shifted in the same way and loaded into register R3. The output data is left-justified in registers R2 and R3 (Figure 5).

For the LTC1297 four NOPs need to be inserted in the 8051 code after $\overline{CS}$ goes low to allow the LTC1297 to wake up from power shutdown ($t_{su\overline{CS}}$).

APPLICATIONS INFORMATION

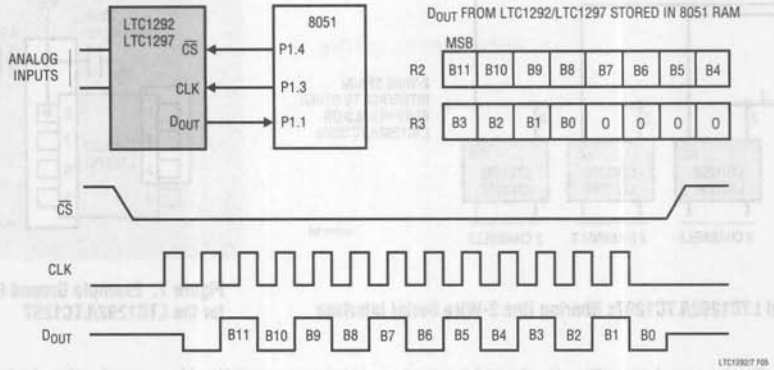


Figure 5. Hardware and Software Interface to Intel 8051 Processor

8051 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	P1,#02h	BIT 1 PORT 1 SET AS INPUT		CLR	A	CLEAR ACC
	CLR	P1.3	CLK GOES LOW		RLC	A	ROTATE DATA BIT (B3) INTO ACC
	SETB	P1.4	$\overline{CS}$ GOES HIGH			SETB	P1.3 CLK GOES HIGH
CONT	CLR	P1.4	$\overline{CS}$ GOES LO		CLR	P1.3	CLK GOES LOW
	NOP		4 NOP FOR LTC1297 $t_{su\overline{CS}}$ (Wakeup		MOV	C,P1.1	READ DATA BIT INTO CARRY
	NOP		Time) (Not Needed for LTC1292)		RLC	A	ROTATE DATA BIT (B2) INTO ACC
	NOP				SETB	P1.3	CLK GOES HIGH
	NOP				CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH		MOV	C,P1.1	READ DATA BIT INTO CARRY
	CLR	P1.3	CLK GOES LOW		RLC	A	ROTATE DATA BIT (B1) INTO ACC
	SETB	P1.3	CLK GOES HIGH		SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW		CLR	P1.3	CLK GOES LOW
	MOV	R4,#08H	LOAD COUNTER		MOV	C,P1.1	READ DATA BIT INTO CARRY
LOOP	MOV	C,P1.1	READ DATA BIT INTO CARRY		SETB	P1.4	$\overline{CS}$ GOES HIGH
	RLC	A	ROTATE DATA BIT INTO ACC		RRC	A	ROTATE DATA BIT (B0) INTO ACC
	SETB	P1.3	CLK GOES HIGH		RRC	A	ROTATE RIGHT INTO ACC
	CLR	P1.3	CLK GOES LOW		RRC	A	ROTATE RIGHT INTO ACC
	DJNZ	R4,LOOP	NEXT BIT		RRC	A	ROTATE RIGHT INTO ACC
	MOV	R2,A	STORE MSBs IN R2		MOV	R3,A	STORE LSBs IN R3
	MOV	C,P1.1	READ DATA BIT INTO CARRY		AJMP	CONT	START NEXT CONVERSION

Sharing the Serial Interface

The LTC1292/LTC1297 can share the same two-wire serial interface with other peripheral components or other LTC1292/LTC1297s (Figure 6). In this case, the $\overline{CS}$ signals decide which LTC1292 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1292/LTC1297 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance

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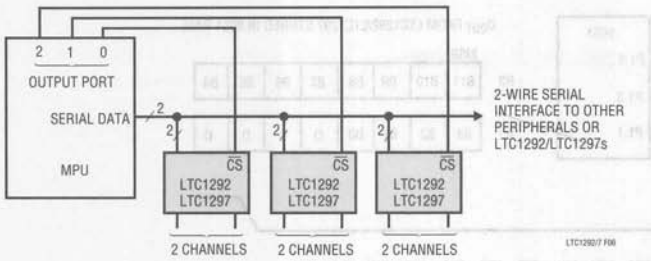

Figure 6. Several LTC1292/LTC1297s Sharing One 2-Wire Serial Interface

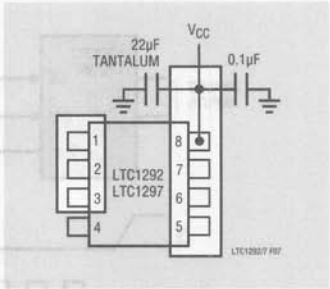

Figure 7. Example Ground Plane for the LTC1292/LTC1297

use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). Figure 7 shows an example of an ideal LTC1292/LTC1297 ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance such as obtained from a voltage regulator (e.g., LT323A). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Figures 8 and 9 show the effects of good and poor V_{CC} bypassing.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1292/LTC1297 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure that the transients caused by the current spikes settle completely before the conversion begins.

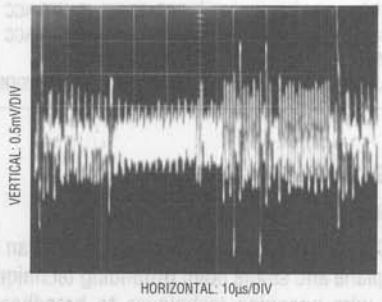

Figure 8. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

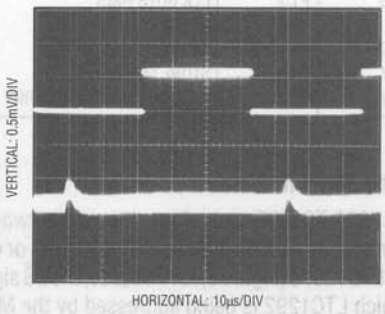

Figure 9. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

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Source Resistance

The analog inputs of the LTC1292/LTC1297 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) (Figures 10a and 10b). C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

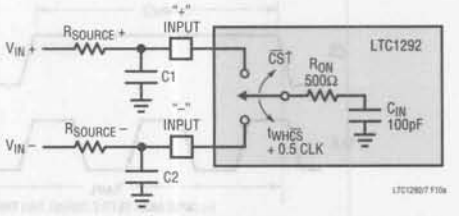

Figure 10a. Analog Input Equivalent Circuit for the LTC1292

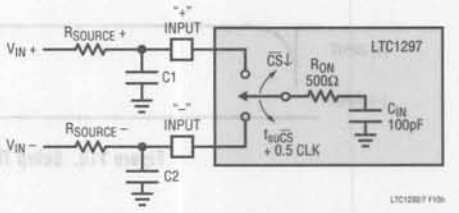

Figure 10b. Analog Input Equivalent Circuit for the LTC1297

"+" Input Settling

The input capacitor for the LTC1292 is switched onto the "+" input during the sample phase (t_{SMPL}, see Figures 11a, 11b and 11c). The sample period can be as short as t_{WHCS} + 1/2 CLK cycle or as long as t_{WHCS} + 1 1/2 CLK cycles before a conversion starts. This variability depends on where $\overline{CS}$ falls relative to CLK. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3.0µs, **R_{SOURCE}+ < 2.0k and C1 < 20pF will provide adequate settling time.**

The sample period for the LTC1297 starts on the falling edge of $\overline{CS}$ and ends on the falling edge of the first CLK (Figure 12). The length of the sample period is $t_{su\overline{CS}}$ +0.5 CLK cycles. Again, the voltage on the "+" input must settle completely within the sample period. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency or by increasing

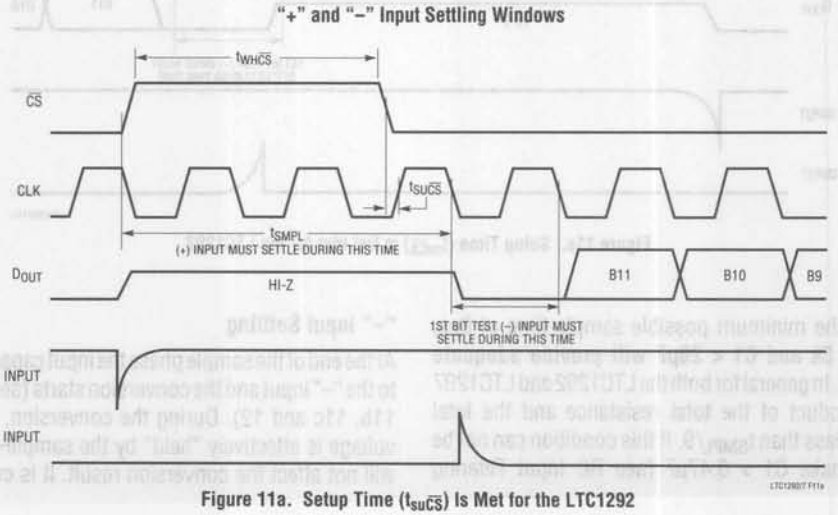

Figure 11a. Setup Time ($t_{su\overline{CS}}$) Is Met for the LTC1292

APPLICATIONS INFORMATION

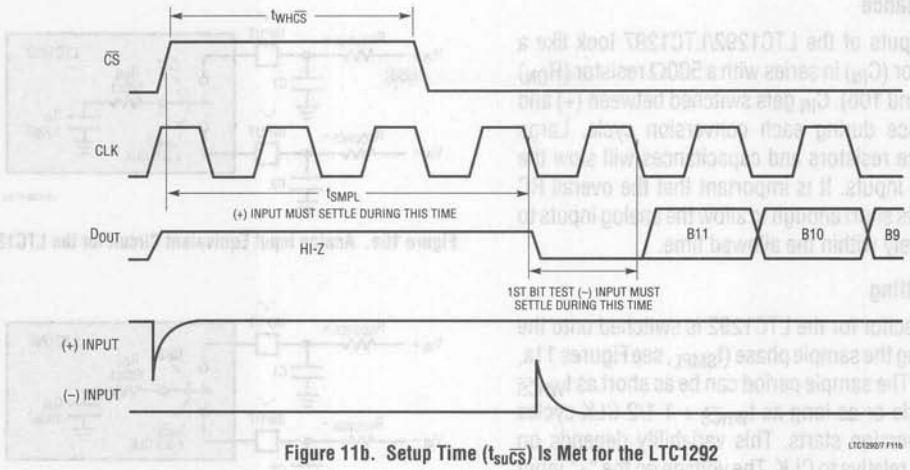

Figure 11b. Setup Time ($t_{su\overline{CS}}$) Is Met for the LTC1292

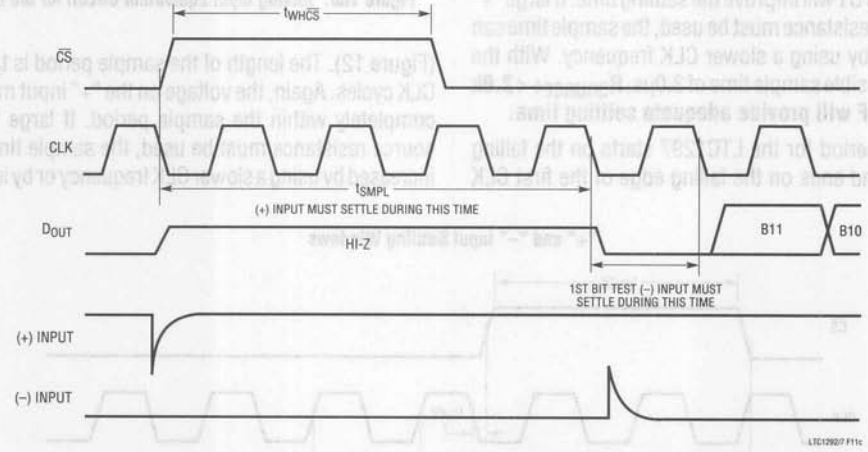

Figure 11c. Setup Time ($t_{su\overline{CS}}$) Is Not Met for the LTC1292

$t_{su\overline{CS}}$. With the minimum possible sample time of 6µs, **$R_{SOURCE+}$ < 5k and C1 < 20pF will provide adequate settling time.** In general for both the LTC1292 and LTC1297 keep the product of the total resistance and the total capacitance less than $t_{SMPL}/9$. If this condition can not be met, then make C1 > 0.47µF (see RC Input Filtering section).

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figures 11a, 11b, 11c and 12). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the

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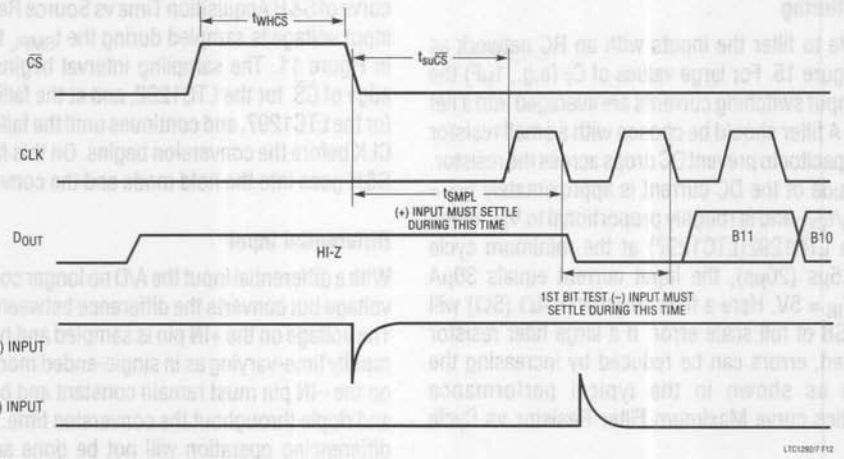

Figure 12. "+" and "–" Input Settling Windows for the LTC1297

"–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **R_{SOURCE}– < 250Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figures 11a, 11b, 11c and 12). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 3.0µs for the LTC1292 or 6.0µs for the LTC1297 ("+" input) and 1µs ("–" input) that occurs at the maximum clock rate of 1MHz. Figures 13 and 14 show examples of both adequate and poor op amp settling.

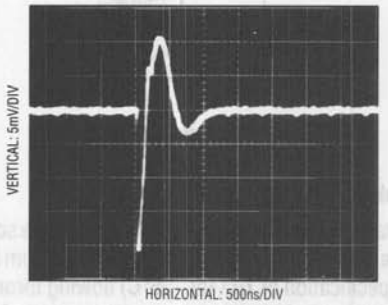

Figure 13. Adequate Settling of Op Amp Driving Analog Input

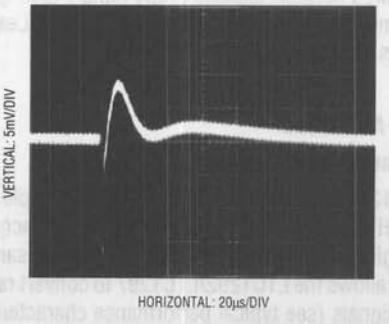

Figure 14. Poor Op Amp Settling Can Cause A/D Errors

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RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 15. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running the LTC1292(LTC1297) at the minimum cycle time of 16.5µs (20µs), the input current equals 30µA (25µA) at V_{IN} = 5V. Here a filter resistor of 4Ω (5Ω) will cause 0.1LSB of full scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristics curve Maximum Filter Resistor vs Cycle Time.

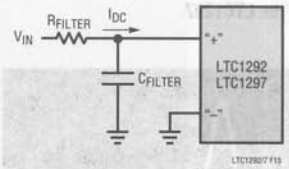

Figure 15. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1292/LTC1297 provide a built-in sample-and-hold (S&H) function on the +IN input for signals acquired in the single-ended mode (–IN pin grounded). The sample-and-hold allows the LTC1292/LTC1297 to convert rapidly varying signals (see typical performance characteristics curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 11. The sampling interval begins at the rising edge of $\overline{CS}$ for the LTC1292, and at the falling edge of $\overline{CS}$ for the LTC1297, and continues until the falling edge of the CLK before the conversion begins. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time-varying as in single-ended mode. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

1292/7 E1

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (300µV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

1292/7 E2

For 0.25LSB error (300µV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz.

Reference Input

The voltage on the reference input of the LTC1292/LTC1297 determine the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched-capacitor con-

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version technique (see Figure 16). During each bit test of the conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

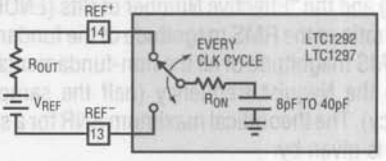

Figure 16. Reference Input Equivalent Circuit

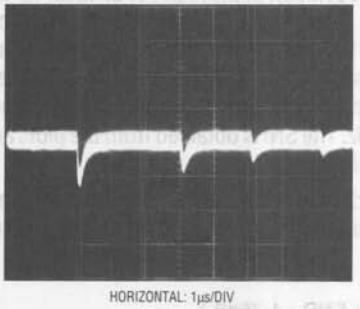

Figure 17. Adequate Reference Settling (LT1027)

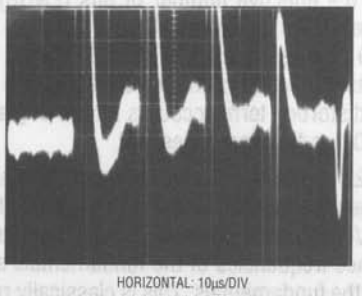

Figure 18. Poor Reference Settling Can Cause A/D Errors

Figures 17 and 18 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 1MHz most references and op amps can be made to settle within the 1µs bit time. For example the LT1027 will settle adequately. With a 10µF bypass capacitor at V_{REF} the LT1021 can also be used.

Reduced Reference Operation

The effective resolution of the LTC1292/LTC1297 can be increased by reducing the input span of the converter. The LTC1292/LTC1297 exhibit good linearity over a range of reference voltages (see typical performance characteristics curves of Change in Linearity vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and noise are factors that must be considered when operating at low V_{REF} values. The internal reference for V_{REF} has been tied to the GND pin. Any voltage drop from the GND pin to the ground plane will cause a gain error.

Offset with Reduced V_{REF}

The offset of the LTC1292/LTC1297 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.1LSB with a 5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the –IN input to the LTC1292/LTC1297.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1292/LTC1297 can be reduced to approximately 200µV_{P-P} using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference input but will

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become a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 5V reference, the 200µV noise is only 0.16LSB peak-to-peak. Here the LTC1292/LTC1297 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now, averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Gain Error Due to Reduced V_{REF}

The gain error of the LTC1292/LTC1297 is very good over a wide range of reference voltages. The error component that is seen in the typical performance characteristics curve Change in Gain Error vs Reference Voltage is due to the voltage drop on the GND pin from the device to the ground plane. To minimize this error the LTC1292/LTC1297 should be soldered directly onto the PC board. The internal reference point for V_{REF} is tied to GND. Any voltage drop in the GND pin will make the reference voltage, internal to the device, less than what is applied externally (Figure 19). This drop is typically 420µV due to the product of the pin resistance (R_{PIN}) and the LTC1292/LTC1297 supply current. For example, with V_{REF} = 1.25V this will result in a gain error change of –1.0LSB from the gain error measured with V_{REF} = 5V.

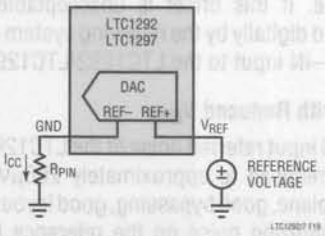

Figure 19. Parasitic Resistance in GND Pin

LTC1292 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/Ds in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "Effective Number of Bits (ENOB)." SNR is the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the non-fundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR depends on the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. Fast Fourier Transform (FFT) plots of the output spectrum of the LTC1292 are shown in Figures 20a and 20b. The input (f_{IN}) frequencies are 1kHz and 28kHz with the sampling frequency (f_S) at 58.8 kHz. The SNRs obtained from the plots are 73.0dB and 61.5dB.

By rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \left(\frac{SNR - 1.76dB}{6.02}\right)$$

This is the effective number of bits (ENOB). For the example shown in Figures 20a and 20b, N = 11.8 bits and 9.9 bits, respectively. Figure 21 shows a plot of ENOB as a function of input frequency. The 2nd harmonic distortion term accounts for the degradation of the ENOB as f_{IN} approaches $f_S/2$.

Figure 22 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

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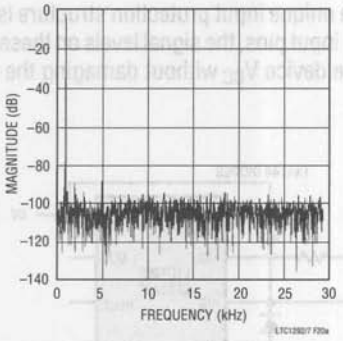


Figure 20a. f_{IN} = 1kHz, f_S = 58.8kHz, SNR = 73.0dB

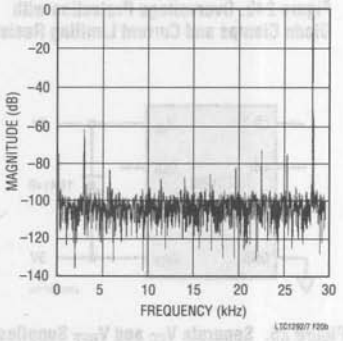


Figure 20b. f_{IN} = 28kHz, f_S = 58.8kHz, SNR = 61.5dB

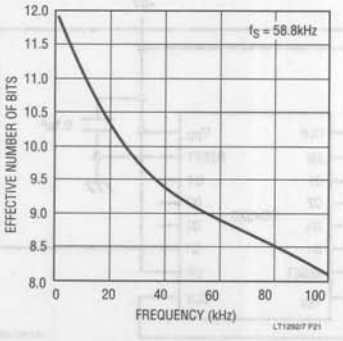


Figure 21. LTC1292 ENOB vs Input Frequency

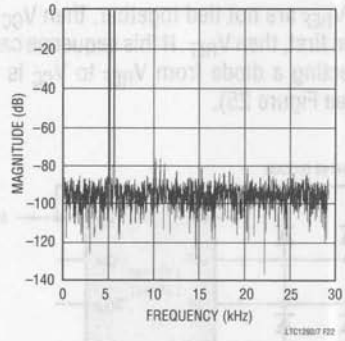


Figure 22. f_{IN1} = 5.1kHz, f_{IN2} = 5.6kHz, f_S = 58.8kHz

Overvoltage Protection

Applying signals to the LTC1292/LTC1297's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the devices. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1292/LTC1297. Another example is the input source is operating from different supplies of larger value than the LTC1292/LTC1297. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 23 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 250Ω when clocked at its maximum clock frequency of 1MHz. If the LTC1292/LTC1297 are clocked at the maximum clock frequency and 250Ω is not enough to current limit the input source, then the clamp diodes are recommended (Figures 24a and 24b). The reason for the limit on the resistor value is that the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the typical performance characteristics Maximum CLK Frequency vs Source Resistance).

APPLICATIONS INFORMATION

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met, connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 25).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

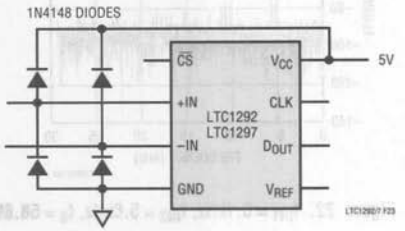


Figure 23. Overvoltage Protection with Clamp Diodes

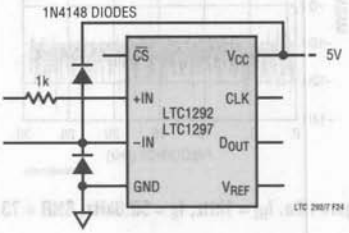


Figure 24b. Overvoltage Protection with Diode Clamps and Current Limiting Resistor

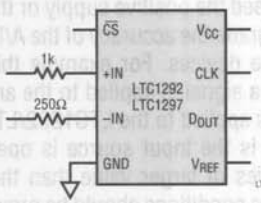


Figure 24a. Overvoltage Protection with Current Limiting Resistors

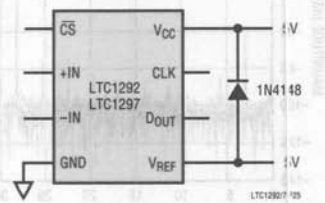


Figure 25. Separate V_{CC} and V_{REF} Supplies

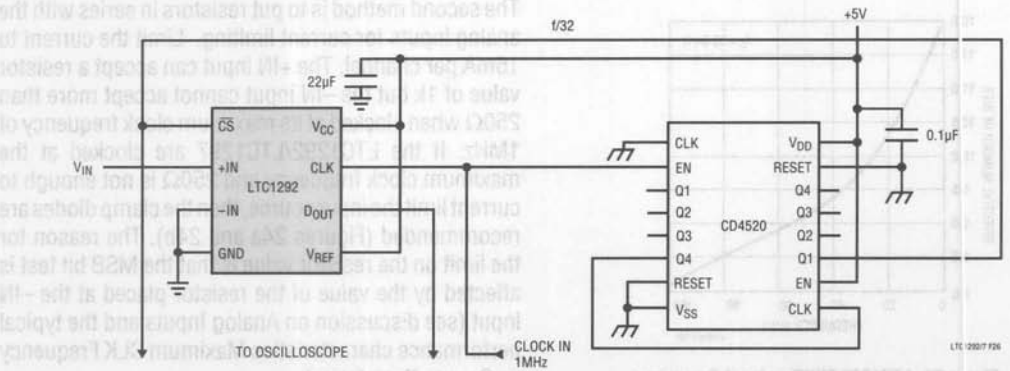


Figure 26. "Quick Look" Circuit for the LTC1292

APPLICATIONS INFORMATION

A "Quick Look" Circuit for the LTC1292

Users can get a quick look at the function and timing of the LTC1292 by using the "Quick Look" circuit in Figure 26. V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground plane. $\overline{CS}$ is driven at 1/32 the clock rate by the CD4520 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 27). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

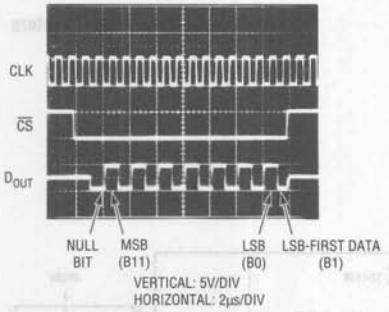


Figure 27. Scope Trace of the LTC1292 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

A "Quick Look" Circuit for the LTC1297

A circuit similar to the one used for the LTC1292 can be used for the LTC1297 (Figure 28). A one shot has been generated with NAND gates, a resistor and capacitor to satisfy the setup time $t_{su\overline{CS}}$. This can be eliminated if a slower clock is used. When $\overline{CS}$ goes low the one shot is triggered. This turns off the clock to the LTC1297 for a fixed time to meet $t_{su\overline{CS}}$. Once the clock starts D_{OUT} is shifted out one bit at a time. $\overline{CS}$ is driven at 1/64 the clock rate by the 74HC393. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set to trigger on the falling edge of $\overline{CS}$. See Figure 29.

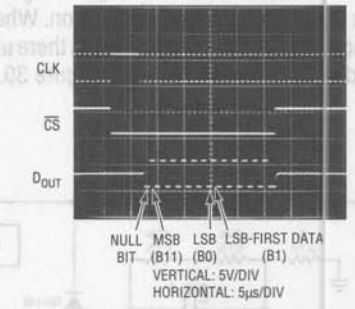


Figure 29. Scope Trace of the LTC1297 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

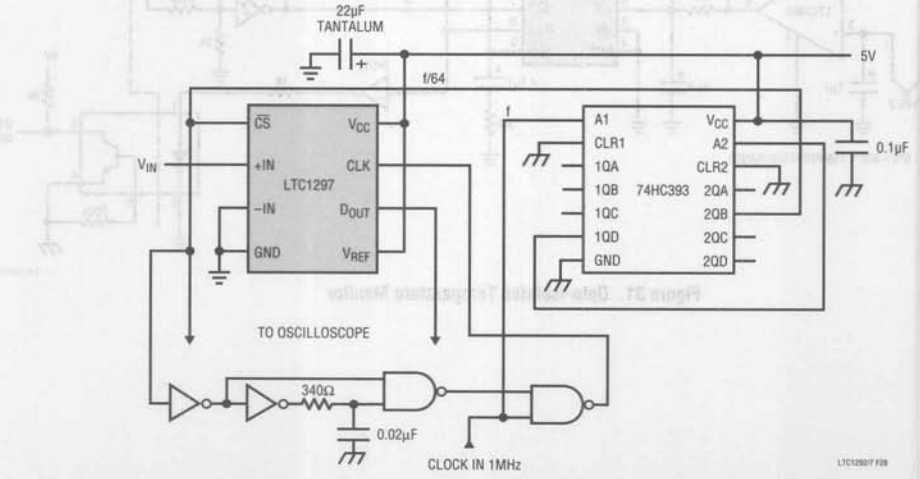


Figure 28. "Quick Look" Circuit for the LTC1297

APPLICATIONS INFORMATION

Opto-Isolated Temperature Monitor

Amplification of sensor outputs is often required to generate a signal large enough to be properly digitized. For example, a J-type thermocouple provides only 52µV/°C. The 5µV offset of the LTC1050 chopper op amp generates less than 0.1°C error (Figure 31). Cold junction compensation is provided by the LT1025A. (For more detail see LTC Design Note 5).

In the opto-isolated interface two signals are generated from one. This allows a two-wire interface to the LTC1292. A long high signal (>1ms) on the CLK IN input allows the 0.1µF capacitor to discharge taking $\overline{CS}$ high. This resets the A/D for the next conversion. When CLK IN starts toggling, $\overline{CS}$ goes low and stays there until the next extended CLK IN high time. See Figure 30.

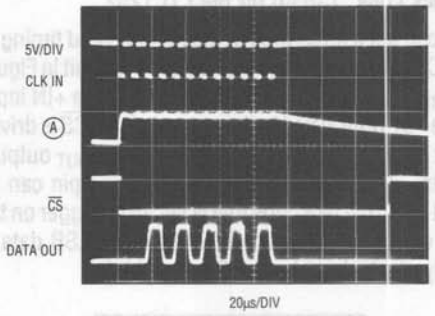


Figure 30. Opto-Isolated Temperature Monitor Digital Waveforms

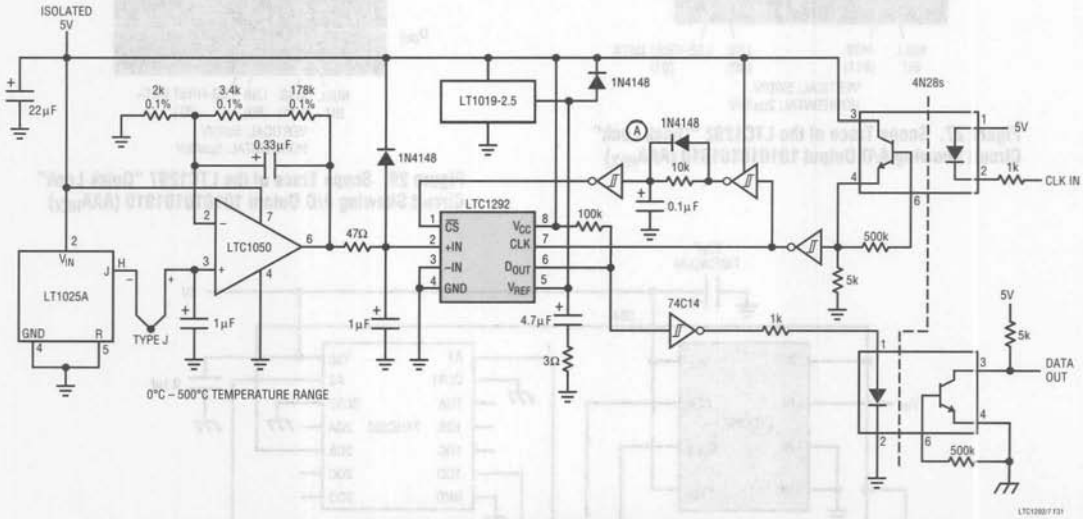


Figure 31. Opto-Isolated Temperature Monitor

Complete 12-Bit A/D Converter

FEATURES

- Industry-Standard 574A Compatible
- Complete 12-Bit A/D Converter with Reference and Clock
- Improved Reference Output Current Capability
- 25µs Maximum Conversion Time
- Fast Bus Access Time
- 8- or 16-Bit Microprocessor Interface
- Guaranteed Linearity over Temperature

APPLICATIONS

- Signal Processing
- Data Acquisition
- Process Monitoring and Control

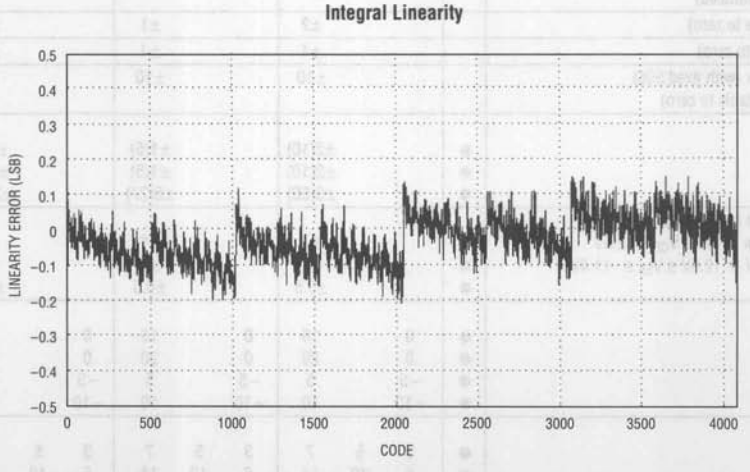
DESCRIPTION

The LT574A is a complete 12-bit A/D converter in the industry-standard 574A pinout. The 3-state output buffers interface directly to an 8- or 16-bit microprocessor bus. A high precision 10V reference and clock are included on-chip, and the device provides full-rated performance without external circuitry or clock signals.

The LT574A provides several advantages over other 574A type devices. External load driving capability of the reference has been improved to up to 8.5mA beyond the ADC current required. Maximum V_{CC} has been increased to 22V and the reference can source full load current at a V_{CC} of 11.4V without requiring an external buffer. The reference is trimmed to 10.00V with 0.2% maximum error and 5ppm/°C typical TC. Bus timing specifications are significantly faster than original 574A specifications, easing microprocessor interface concerns.

6

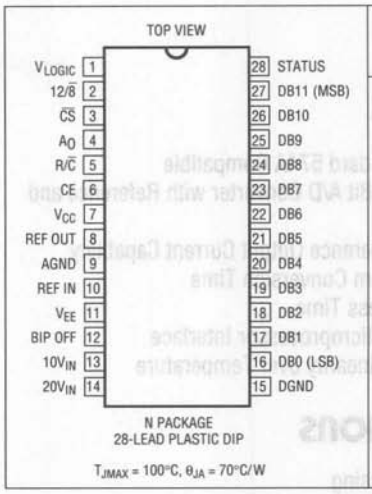
TYPICAL PERFORMANCE



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to 22V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} to Digital Common ..... 0V to 7V
Analog Common to Digital Common ..... ±1V
Digital Inputs to
Digital Common ..... –0.5V to V_{LOGIC} + 0.5V
Analog Inputs (REF In, BIP Off, $10V_{IN}$)
to Analog Common ..... V_{EE} to 16.5V
$20V_{IN}$ to Analog common ..... V_{EE} to 24V
REF Out ..... Indefinite Short to Analog Common
Momentary Short to V_{CC}
Power Dissipation 1000mW
Junction Temperature ..... 165°C
Operating Temperature Range
J, K, L Grades ..... 0°C to 70°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature ..... (Soldering, 10sec) 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
28-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT574AJN
LT574AKN
LT574ALN

CONVERTER ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V or 15V, V_{EE} = –12V, V_{LOGIC} = 5V, unless otherwise specified.

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
Resolution	●			12			12			12	Bits
Integral Linearity Error	●			±1			±0.5			±0.5	LSB
Differential Linearity Error (minimum resolution for which no missing codes are guaranteed)	●	11			12			12			Bits
Unipolar Offset (adjustable to zero)				±2			±1			±1	LSB
Bipolar Offset (adjustable to zero)				±4			±4			±2	LSB
Full Scale Calibration Error (with fixed 50Ω REF OUT to REF IN (adjustable to zero)				±10			±10			±4	LSB
Temperature Coefficients											
Unipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Bipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Full Scale Calibration	●			±9(50)			±5(27)			±2(10)	LSB(ppm/°C)
Supply Sensitivity (change in full scale calibration)											
$13.5V \le V_{CC} \le 16.5V$ or $11.4V \le V_{CC} \le 12.6V$	●			±2			±1			±1	LSB
$-16.5V \le V_{EE} \le -13.5V$ or $12.6V \le V_{EE} \le -11.4V$	●			±2			±1			±1	LSB
$4.5V \le V_{LOGIC} \le 5.5V$	●			±0.5			±0.5			±0.5	LSB
Input Ranges											
Unipolar	●	0		10	0		10	0		10	V
	●	0		20	0		20	0		20	V
Bipolar	●	–5		5	–5		5	–5		5	V
	●	–10		10	–10		10	–10		10	V
Input Impedance											
10V Span	●	3	5	7	3	5	7	3	5	7	kΩ
20V Span	●	6	10	14	6	10	14	6	10	14	kΩ

INTERNAL REFERENCE ELECTRICAL CHARACTERISTICS

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
REF OUT Voltage (no load)		9.98		10.02	9.98		10.02	9.99		10.01	V
Line Regulation, $11.4 \le V_{IN} \le 22V$			1	5		1	5		1	5	ppm/V
	●			10			10			10	ppm/V
Load Regulation (sourcing current), $0 \le I_{OUT} \le 10mA$			12	30		12	30		12	30	ppm/mA
	●			50			50			50	ppm/mA
Reference Temperature Coefficient	●			50			27			10	ppm/°C

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		LT574A, All Grades MIN	TYP	MAX	UNITS
	V_{LOGIC} Supply Range		●	4.5	5.0	5.5	V
	V_{EE} Supply Range		●	−11.4		−16.5	V
	V_{CC} Supply Range		●	11.4		22.0	V
	V_{LOGIC} Operating Current		●		27	40	mA
	V_{EE} Operating Current		●		−15	−25	mA
	V_{CC} Operating Current		●		1.7	3.5	mA
	Power Dissipation		●		390	700	mW
V_{IH}	Logic High Input Voltage	12/8, CE, A_0, R/$\overline{C}$, $\overline{CE}$	●	2.0		5.5	V
V_{IL}	Logic Low Input Voltage	12/8, CE, A_0, R/$\overline{C}$, $\overline{CE}$	●	−0.5		0.8	V
I_{IN}	Logic Input Current		●	−100		100	µA
C_{IN}	Digital Input Pin Capacitance				5		pF
V_{OH}	Logic Output Voltage	$I_{SOURCE} \le 600µA$		2.4			V
V_{OL}	Logic Low Output Voltage	$I_{SINK} \le 1.6mA$				0.4	V
	Leakage Current	High-Z State		−20		20	µA
C_{OUT}	Output Capacitance				5		pF

The ● denotes the specifications which apply over the full operating temperature range.

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = −15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	TYP	MAX	UNITS
Read Timing, Full Control Mode	t_{DD}	Access Time (from CE)		75	150	ns
	t_{HD}	Data Valid After CE Low	25			ns
	t_{HL}	Output Float Delay			150	ns
	t_{SSR}	$\overline{CS}$-to-CE Setup	50			ns
	t_{SRR}	R/$\overline{C}$-to-CE Setup	0			ns
	t_{SAR}	AO-to-CE Setup	50			ns
	t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
	t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
	t_{HAR}	A_0 Valid After CE Low	50			ns

6

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = –15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	TYP	MAX	UNITS
Convert Start Timing, Full Control Mode	t_{DSC}	STS Delay from CE			200	ns
	t_{HEC}	CE Pulse Width	50			ns
	t_{SSC}	$\overline{CS}$-to-CE Setup	50			ns
	t_{HSC}	$\overline{CS}$ Low During CE High	50			ns
	t_{SRC}	R/$\overline{C}$-to-CE Setup	50			ns
	t_{HRC}	R/$\overline{C}$ Low During CE High	50			ns
	t_{SAC}	AO-to-CE Setup	0			ns
	t_{HAC}	AO Valid During CE High	50			ns
	t_C	Conversion Time				
		8-Bit Cycle	10		17	µs
		12-Bit Cycle	15		25	µs
Stand-Alone Mode Timing	t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
	t_{DS}	STS Delay from R/$\overline{C}$			200	ns
	t_{HDR}	Data Valid after R/$\overline{C}$ Low	25			ns
	t_{HS}	STS Delay after Data Valid	25		600	ns
	t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
	t_{DDR}	Data Access Time			150	ns

BLOCK DIAGRAM

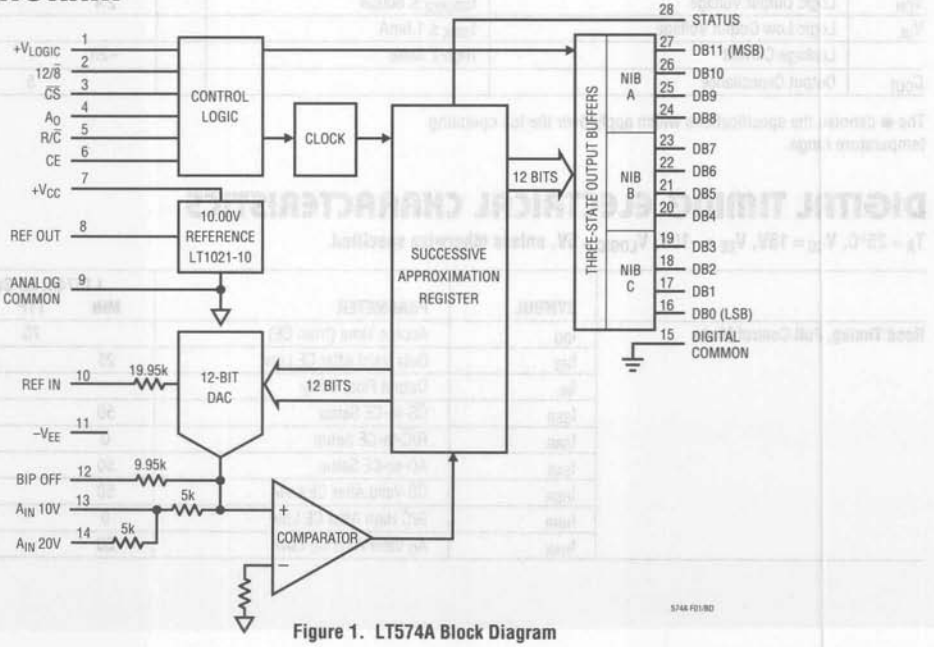


Figure 1. LT574A Block Diagram

SECTION 6—DATA CONVERSION

DIGITAL TO ANALOG CONVERTERS

LTC1257, Complete Single Supply 12-Bit Voltage Output DAC in SO-8 6-210

Complete Single Supply 12-Bit Voltage Output DAC in SO-8

FEATURES

- **8-Pin SO Package**
- **Buffered Voltage Output**
- **Built-In 2.048V Reference**
- 500µV/LSB with 2.048V Full Scale
- 1/2 LSB Max DNL Error
- Guaranteed 12-Bit Monotonic
- Three-Wire Cascadable Serial Interface
- Wide Single Supply Range: V_{CC} = 4.75V to 15.75V
- Low Power: I_{CC} Typ = 350µA with 5V Supply

APPLICATIONS

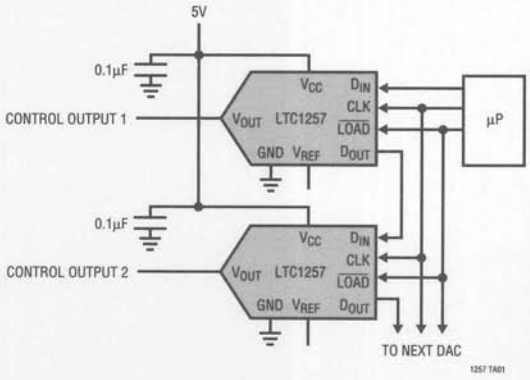
- Digital Offset/Gain Adjustment
- Industrial Process Control
- Automatic Test Equipment

DESCRIPTION

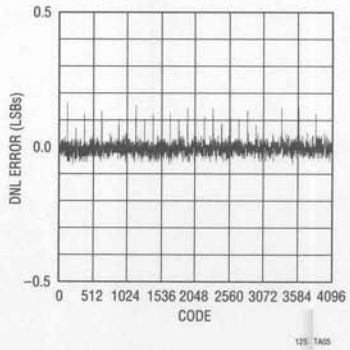
The LTC1257 is a complete single supply, 12-bit voltage output D/A converter (DAC) in an SO-8 package. The LTC1257 includes an output buffer amplifier, 2.048V voltage reference and an easy to use three-wire cascadable serial interface. An external reference can be used to override the internal reference and extend the output voltage range to 12V. The power supply current is a low 350µA when operating from a 5V supply, making the LTC1257 ideal for battery-powered applications. The space-saving 8-pin SO package and operation with no external components provide the smallest 12-bit D/A system available.

TYPICAL APPLICATION

Daisy Chained Control Outputs



Differential Nonlinearity vs Input Code

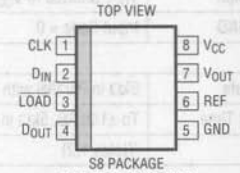


ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... −0.5V to 16.5V
TTL Input Voltage ..... −0.5V to V_{CC} + 0.5V
V_{OUT} ..... −0.5V to V_{CC} + 0.5V
REF ..... −0.5V to V_{CC} + 0.5V
Operating Temperature Range
LTC1257C ..... 0°C to 70°C
LTC1257I ..... −40°C to 85°C
Maximum Junction Temperature
Plastic Package ..... −65°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 125°C, θ_{JA} = 100°C/W



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1257CN8 LTC1257IN8
LTC1257CS8 LTC1257IS8
S8 PART MARKING
1257C 1257I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 15.75V, internal or external reference ($2.475V \le V_{REF} \le V_{CC} - 2.7V$), $I_{OUT} \le 2mA$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic	●			±0.5	LSB
INL	Integral Nonlinearity	LTC1257C	●			±3.5	LSB
		LTC1257I	●			±4.0	LSB
OFF	Offset Error	When Using Internal Reference, LTC1257C	●			±8	LSB
		When Using Internal Reference, LTC1257I	●			±10	LSB
		When Using External Reference, LTC1257C	●			±4	mV
		When Using External Reference, LTC1257I	●			±5	mV
OFF_{TC}	Offset Error Tempco	When Using Internal Reference (Note 1)	●		±0.02	±0.066	LSB/°C
		When Using External Reference (Note 1)	●		±15	±30	µV/°C
FSE	Full-Scale Error		●		0.5	±2	LSB
FSE_{TC}	Full-Scale Error Tempco	(Note 1)	●		±0.01	±0.02	LSB/°C
Reference							
	Reference Output Voltage	I_{OUT} = 0, LTC1257C	●	2.028	2.048	2.068	V
		I_{OUT} = 0, LTC1257I	●	2.018		2.078	V
	Reference Output Tempco	I_{OUT} = 0	●		±0.06		LSB/°C
	Reference Line Regulation	I_{OUT} = 0, LTC1257C	●			±0.4	LSB/V
		I_{OUT} = 0, LTC1257I	●			±0.7	LSB/V
	Reference Load Regulation	$0 \le I_{OUT} \le 100\mu A$	●			±1	LSB
	Reference Input Range	$V_{CC} > V_{REF} + 2.7V$	●	2.475		12	V
	Reference Input Resistance		●	8	14	18	kΩ
	Reference Input Capacitance	(Note 1)			15		pF
	Short-Circuit Current	V_{OUT} Shorted to GND	●			90	mA

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ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 15.75V, internal or external reference ($2.475V \le V_{REF} \le V_{CC} - 2.7V$), $I_{OUT} \le 2mA$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.75		15.75	V
I_{CC}	Supply Current	$4.75V \le V_{CC} \le 5.25V$	●		350	600	µA
		$4.75V \le V_{CC} \le 15.75V$	●		800	1500	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			60	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			60	mA
	Output Impedance to GND	Input Code = 0	●		150	300	Ω
AC Performance							
	Voltage Output Slew Rate	5kΩ in Parallel with 100pF	●	1.0			V/µs
	Voltage Output Settling Time	To ±1/2LSB, 5kΩ in Parallel with 100pF	●			6	µs
	Digital Feedthrough	(Notes 1,2)			50		nV/s
Digital I/O							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage	$I_{OUT} = -1mA$, D_{OUT} Only	●	$V_{CC} - 1$			V
V_{OL}	Digital Output Low Voltage	$I_{OUT} = 1mA$, D_{OUT} Only	●		0.4		V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 1)	●			10	pF
Switching (Note 1)							
t1	D_{IN} Valid to CLK Setup		●	150			ns
t2	D_{IN} Valid to CLK Hold		●	0			ns
t3	CLK High Time		●	350			ns
t4	CLK Low Time		●	350			ns
t5	$\overline{LOAD}$ Pulse Width		●	150			ns
t6	LSB CLK to $\overline{LOAD}$		●	0			ns
t7	$\overline{LOAD}$ High to CLK		●	0			ns
t8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150	ns
f_{CLK}	Maximum Clock Frequency					1.4	MHz

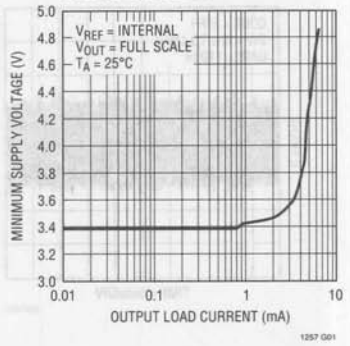
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Guaranteed by design; not subject to test.

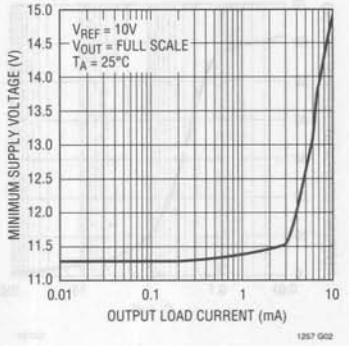
Note 2: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

TYPICAL PERFORMANCE CHARACTERISTICS

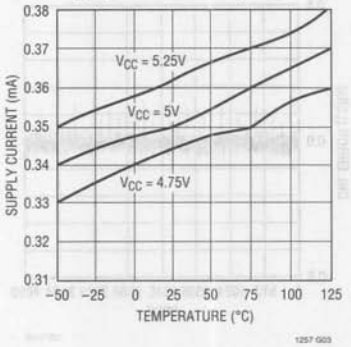
Minimum Supply Voltage vs Load Current #1



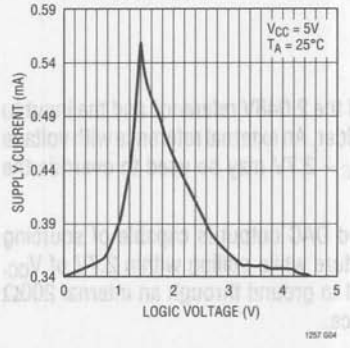
Minimum Supply Voltage vs Load Current #2



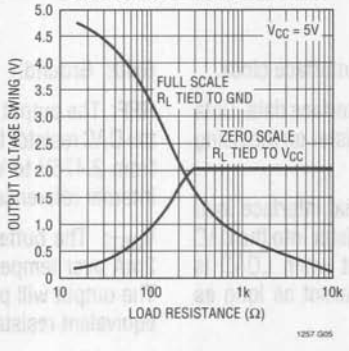
Supply Current vs Temperature



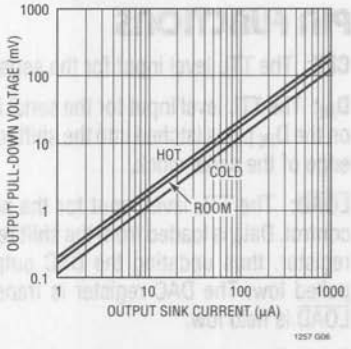
Supply Current vs Logic Input Voltage



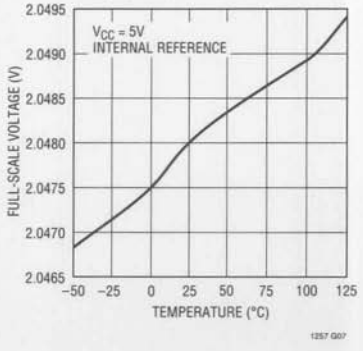
Output Swing vs Load Resistance



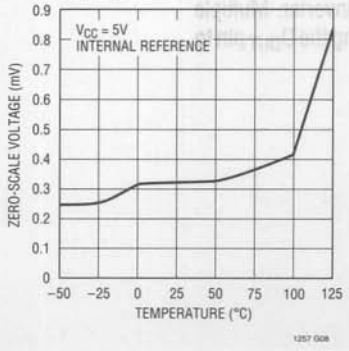
Pull-Down Voltage vs Output Sink Current Capability



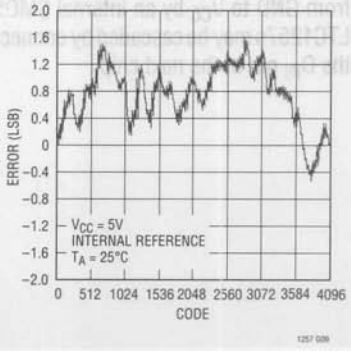
Full-Scale Voltage vs Temperature



Zero-Scale Voltage vs Temperature



Integral Nonlinearity (INL)



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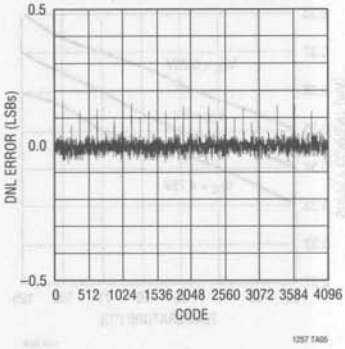
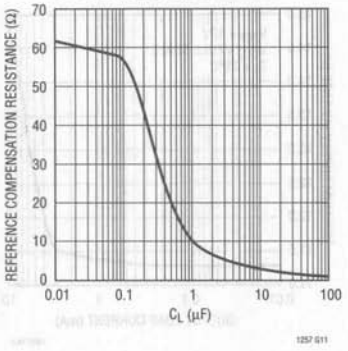
TYPICAL PERFORMANCE CHARACTERISTICS

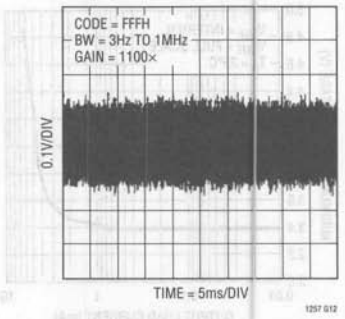
Differential Nonlinearity (DNL)



Reference Compensation Resistance vs C_L



Broadband Noise



PIN FUNCTIONS

CLK: The TTL level input for the serial interface clock.

D_{IN}: The TTL level input for the serial interface data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{LOAD}$: The TTL level input for the serial interface load control. Data is loaded from the shift register into the DAC register, thus updating the DAC output when $\overline{LOAD}$ is pulled low. The DAC register is transparent as long as $\overline{LOAD}$ is held low.

D_{OUT}: The output of the shift register which becomes valid on the rising edge of the serial clock. The D_{OUT} pin is driven from GND to V_{CC} by an internal CMOS inverter. Multiple LTC1257s may be cascaded by connecting the D_{OUT} pin to the D_{IN} pin of the next chip.

GND: Ground.

REF: The output of the 2.048V reference and the input to the DAC resistor ladder. An external reference with voltage from 2.475V to V_{CC} – 2.7V may be used to override the internal reference.

V_{OUT}: The buffered DAC output is capable of sourcing 2mA over temperature while pulling within 2.7V of V_{CC}. The output will pull to ground through an internal 200Ω equivalent resistance.

V_{CC}: The positive supply input. 4.75V ≤ V_{CC} ≤ 15.75V. Requires a bypass capacitor to ground.

DEFINITIONS

LSB: The least significant bit or the ideal voltage difference between two successive codes.

$LSB = (V_{FS} - V_{OS})/2^n - 1$
n = The number of digital input bits
V_{OS} = The zero code error or offset of the DAC
V_{FS} = The full-scale output voltage of the DAC measured when all bits are set to 1

Resolution: The resolution is the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

INL: End-point integral nonlinearity is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below ground, the linearity is measured between full-scale and the first code that guarantees a positive output. The INL error at a given input code is calculated as follows:

$INL = (V_{OUT} - V_{IDEAL})/LSB$
$V_{IDEAL} = (Code \times LSB) + V_{OS}$
V_{OUT} = The output voltage of the DAC measured at the given input code

DNL: Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$DNL = (\Delta V_{OUT} - LSB)/LSB$
ΔV_{OUT} = The measured voltage difference between two adjacent codes

Offset Error: The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below ground. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

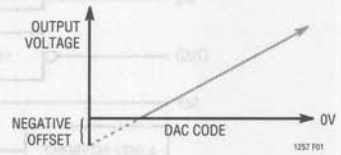


Figure 1. Effect of Negative Offset

The offset of the part is measured at the first code that produces an output voltage 0.5LSB greater than the previous code:

$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$

Full-Scale Error: Full-scale error is the difference between the ideal and measured DAC output voltages with all bits set to one (Code = 4095). The full-scale error includes the offset error and is calculated as follows:

$FSE = (V_{OUT} - V_{IDEAL})/LSB$
$V_{IDEAL} = [V_{REF} \times (1 - 2^{-n})] - V_{OS}$
V_{REF} = The reference voltage, either internal or external

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV × sec.

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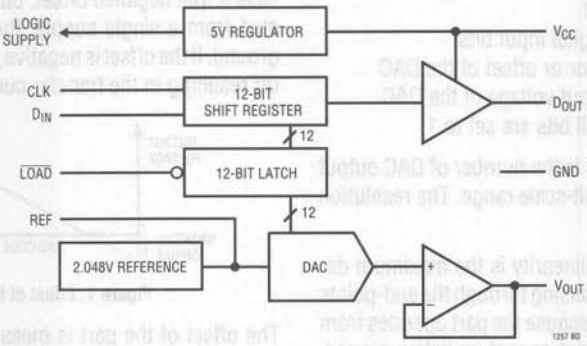
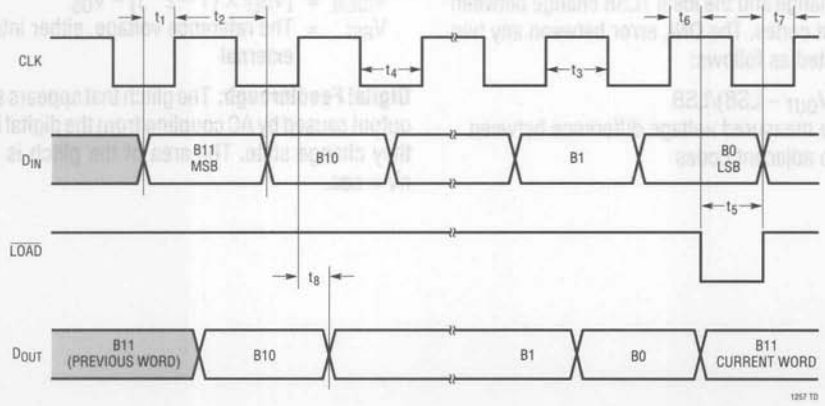
BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first and the LSB last. The DAC register loads the data from the shift register when $\overline{LOAD}$ is pulled low, and remains transparent until $\overline{LOAD}$ is pulled high and the data is latched.

An internal 5V regulator provides the supply for the digital logic. By limiting the internal digital signal swings to 5V, digital noise is reduced. The buffered output of the 12-bit shift register is available on the D_{OUT} pin which will swing from GND to V_{CC}.

Multiple LTC1257s may be daisy chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the clock and load signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{LOAD}$ signal is pulled low to update all of them simultaneously. The maximum clocking rate is 1.4MHz.

Reference

The LTC1257 includes an internal 2.048V reference, making 1LSB equal to 500μV. The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The external reference must be greater than 2.475V and less than V_{CC} – 2.7V, and be capable of driving the 10k minimum DAC resistor ladder.

If the reference output is driving a large capacitive load, a series resistor must be added to insure stability. For any capacitive load greater than 1μF, a 10Ω series resistor will suffice.

Voltage Output

The LTC1257 voltage output is able to pull within 2.7V of V_{CC} while sourcing 2mA. A internal NMOS transistor with a 200Ω equivalent impedance pulls the output to ground. The output is protected against short circuits and is able to drive up to a 500pF capacitive load without oscillation. If digital noise on the output causes a problem, a simple 100Ω, 0.1μF RC circuit can be used to filter the noise.

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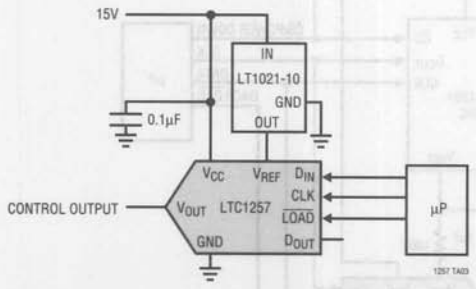
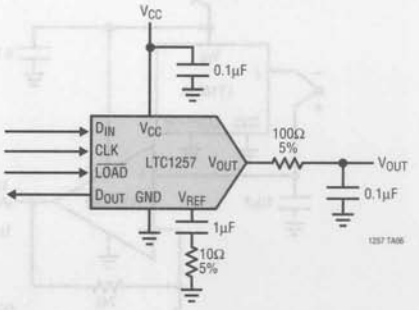
TYPICAL APPLICATIONS

DAC with External Reference

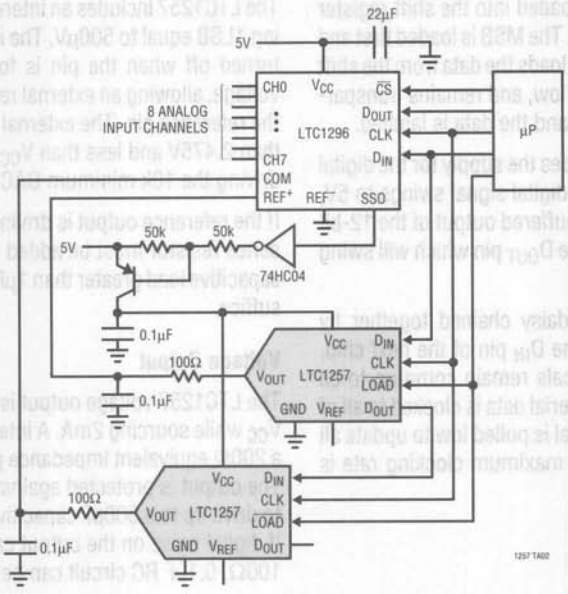


Filtering V_{REF} and V_{OUT}

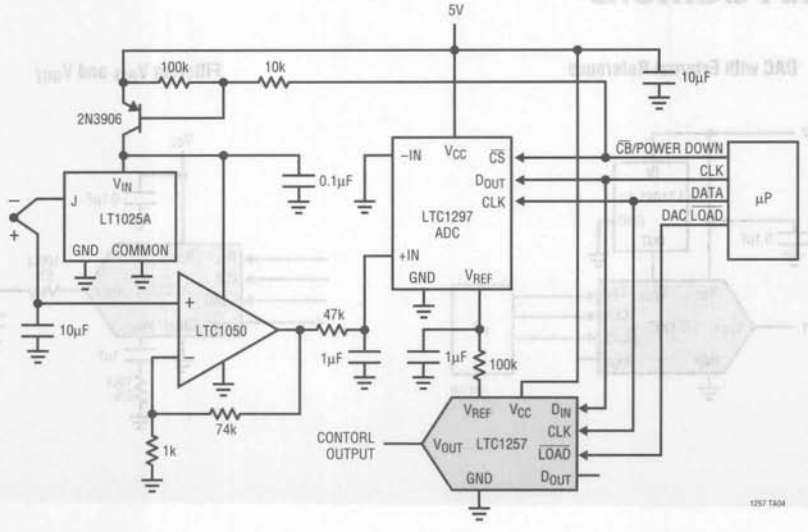


TYPICAL APPLICATIONS

Auto Ranging 8-Channel ADC with Shutdown

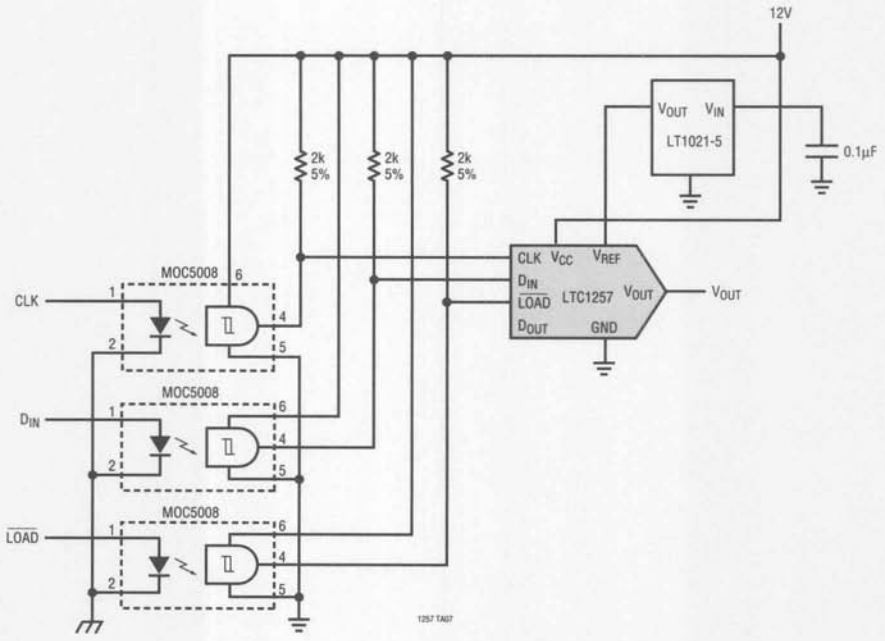


12-Bit Single 5V Control System with Shutdown



TYPICAL APPLICATIONS

Driving LTC1257 with Opto-Isolators



SECTION 7—VOLTAGE REFERENCES

SECTION 7—VOLTAGE REFERENCES

INDEX 7-2
SELECTION GUIDES 7-3
PROPRIETARY PRODUCTS
LT1034-1.2/LT1034-2.5, Micropower Dual Reference 7-5

VOLTAGE REFERENCES

Listed by Temperature Drift (T.C.) and Initial Accuracy

1.25V Output

T.C.	ACCURACY
*LT1034B-1.2	*LT1004-1.2
*LT1034-1.2	*LT1034B-1.2
*LT1004-1.2	*LT1034-1.2
*LM385B-1.2	*LM385B-1.2
*LM385-1.2	*LM385-1.2

2.5V Output

T.C.	ACCURACY
LT1019C-2.5	LT580M
LT1009C-2.5	LT1019C-2.5
LT580M	LT1009-2.5
LT1034B-2.5	LT580L
LT580L	LT1034-2.5
*LT1004C-2.5	LT580K
LT1034-2.5	*LT1004C-2.5
LT580K	*LM385B-2.5
*LM385B-2.5	*LM385-2.5
LM336B-2.5	LT580J
*LM385-2.5	LM336B-2.5
LM336-2.5	LM336-2.5

4.5V Output

T.C.	ACCURACY
LT1019C-4.5	LT1019C-4.5

5.0V Output

T.C.	ACCURACY
LT1027A-5	LT1027A-5
LT1027B-5	LT1027B-5
LT1027C-5	LT1027C-5
LT1027D-5	LT1021C-5
LT1021B-5	LT1027D-5
LT1027E-5	LT1027E-5
LT1019-5	REF-02E
LT1029A	LT1019-5
REF-02E	LT1021B-5
REF-02H	LT1021D-5
LT1021C-5	LT1029A
LT1021D-5	REF-02H
LT1029	LT1029
REF-02C	REF-02C
REF-02D	REF-02D

6.9V to 6.95V Output

T.C.	ACCURACY
LTZ1000	LM329A
LM399A	LTZ1000
LM399	LM329B
LM329A	LM329C
LM329B	LM329D
LM329C	LM299A

7V Output

T.C.	ACCURACY
LT1021B-7	LT1021B-7
LT1021D-7	LT1021D-7
LT1034	LT1034

10V Output

T.C.	ACCURACY
LT1021C-10	LT1021B-10
LT1031C	LT1031B-10
LT581K	REF-01E
LT1019-10	LT1031C
LT1031D	LT581K
LT581J	LT1019-10
REF-01E	LT1021C-10
LT1021B-10	LT1021D-10
LT1021D-10	LT1031D
LT1031B	REF-01H
REF-01H	LT581J
REF-01C	REF-01C

*Micropower

VOLTAGE REFERENCE SELECTION GUIDE

Commercial 0°C to 70°C

VOLTAGE V_Z (V)	VOLTAGE TOLERANCE MAXIMUM T_A = 25°C	PART NUMBER	TEMPETATURE DRIFT, ppm/°C OR mV CHANGE	MIL/IND TEMP	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	PACKAGE TYPE	IMPORTANT FEATURES
1.235	±0.32%	LT1004-1.2	20ppm (typ)	M, I	10µA to 20mA	H, S, Z	Micropower
	±1%	LT1034B-1.2	20ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034-1.2	40ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±2%	LM385-1.2	20ppm (typ)	M, I	15µA to 20mA	H, Z	Micropower
	±1%	LM385B-1.2	20ppm (typ)	M	15µA to 20mA	H, Z	Micropower
2.5	±0.8%	LT1004-2.5	20ppm (typ)	M, I	20µA to 20mA	H, S, Z	Micropower
	±0.2%	LT1009	6mV (max)	M, I	400µA to 10mA	H, Z	Precision
	±0.4%	LT1009S8	25ppm (max)	M, I	400µA to 20mA	S	Precision
	±0.05%	LT1019A-2.5	5ppm (max)	M	1.0mA	H, N	Precision Bandgap
	±0.2%	LT1019-2.5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1034B-2.5	20ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034-2.5	40ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±4%	LM336-2.5	6mV (max)	M	400µA to 10mA	H, Z	General Purpose
	±2%	LM336B-2.5	6mV (max)	M	400µA to 10mA	H, Z	General Purpose
	±3%	LM385-2.5	20ppm (typ)	M, I	20µA to 20mA	H, Z	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	M	20µA to 20mA	H, Z	Micropower
	±3%	LT580J	85ppm (max)		1.5mA	H	3 Terminal Low Drift
	±1%	LT580K/K	40ppm (max)	M	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580L/U	25ppm (max)	M	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580M	10ppm (max)		1.5mA	H	3 Terminal Low Drift
4.5	±0.05%	LT1019A-4.5	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-4.5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
5.0	±0.05%	LT1019A-5	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1021B-5	5ppm (max)	M, I	1.2mA	H, N	Very Low Drift
	±0.05%	LT1021C-5	20ppm (max)	M, I	1.2mA	H, N	Very Tight Initial Tolerance
	±1%	LT1021D-5	20ppm (max)	M, I	1.2mA	H, J, N, S	Low Cost, High Performance
	±0.02%	LT1027A	2ppm (max)		2mA	H	Precision, Enhanced Dynamics
	±0.05%	LT1027B	2ppm (max)		2mA	H, N	Precision, Enhanced Dynamics
	± 0.05%	LT1027C	3ppm (max)		2mA	H, N	Precision, Enhanced Dynamics
	± 0.05%	LT1027D	5ppm (max)		2mA	N, H, S	Precision, Enhanced Dynamics
	± 0.1%	LT1027E	7.5ppm (max)		2mA	N, H, S	Precision, Enhanced Dynamics
	±0.2%	LT1029A	20ppm (max)	M	700µA to 10mA	H, Z	Precision Bandgap
	±1%	LT1029	34ppm (max)	M	700µA to 10mA	H, Z	Precision Bandgap
	±1%	REF02C	65ppm (max)		1.6mA	H, J, N	Precision Bandgap
	±2%	REF02D	250ppm (max)		2.0mA	H, J, N	Bandgap
	±0.3%	REF02E/A	8.5ppm (max)	M	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF02H	25ppm (max)		1.4mA	H, J, N	Precision Bandgap
6.9	±3%	LM329A	10ppm (max)	M	600µA to 15mA	H, Z	Low Drift
	±5%	LM329B	20ppm (max)	M	600µA to 15mA	H, Z	Low Drift
	±5%	LM329C	50ppm (max)	M	600µA to 15mA	H, Z	General Purpose
	±5%	LM329D	100ppm (max)		600µA to 15mA	H, Z	General Purpose
	±4%	LTZ1000	0.1ppm		4mA	H	Ultra Low Drift, 2ppm Long Term Stability*
6.95	±5%	LM399	2ppm (max)	M	500µA to 10mA	H	Ultra Low Drift
	±5%	LM399A	1ppm (max)	M	500µA to 10mA	H	Ultra Low Drift
7.0	±0.7%	LT1021B-7	5ppm (max)	M	1.0mA	H, N	Low Drift/Noise, Exc Stability
	±0.7%	LT1021D-7	20ppm (max)	M	1.0mA	H, N, S	Low Cost, High Performance
10.0	±0.05%	LT1019A-10	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-10	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±0.5%	LT1021B-10	5ppm (max)	M, I	1.7mA	H, N	Very Low Drift
	±0.05%	LT1021C-10	20ppm (max)	M, I	1.7mA	H, N	Very Tight Initial Tolerance
	±0.5%	LT1021D-10	20ppm (max)	M, I	1.7mA	H, N, S	Low Cost, High Performance
	±0.05%	LT1031B	5ppm (max)	M	1.7mA	H	Very Low Drift
	±0.1%	LT1031C	15ppm (max)	M	1.7mA	H	Very Tight Initial Tolerance
	±0.2%	LT1031D	25ppm (max)	M	1.7mA	H	Low Cost, High Performance
	±0.3%	LT581J/S	30ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±0.1%	LT581K/T	15ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±0.05%	LT581L/U	5ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±1%	REF01C	65ppm (max)	M	1.6mA	H, J, N	Precision Bandgap
	±0.3%	REF01E/A	8.5ppm (max)	M	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF01H	25ppm (max)		1.4mA	H, J, N	Precision Bandgap

*LTZ1000 requires external control and biasing circuits.

FEATURES

- *Guaranteed* 20 ppm/°C Drift
- 1.2V 1% Initial Tolerance
- 20μA to 20mA Operation
- 1Ω Dynamic Impedance
- 7V, 100μA Reference

APPLICATIONS

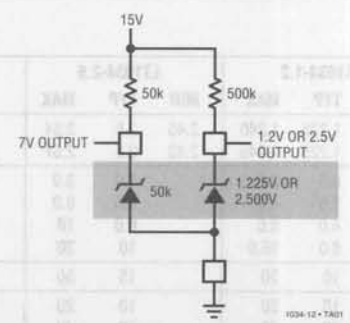
- Portable Meters
- Precision Regulators
- Calibrators

DESCRIPTION

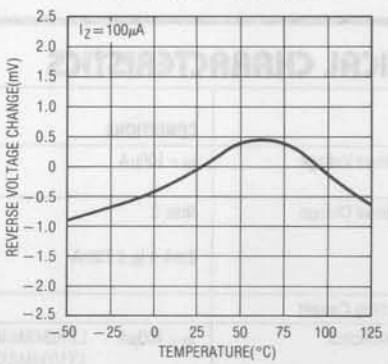
The LT1034 is a micropower, precision 1.2V/2.5V reference combined with a 7V auxiliary reference. The 1.2V/2.5V reference is a trimmed, thin-film, band-gap voltage reference with 1% initial tolerance and guaranteed 20ppm/°C temperature drift. Operating on only 20μA, the LT1034 offers guaranteed drift, low temperature cycling hysteresis and good long term stability. The low dynamic impedance makes the LT1034 easy to use from unregulated supplies. The 7V reference is a subsurface zener device for less demanding applications.

The LT1034 reference can be used as a high performance upgrade of the LM385 or LT1004, where guaranteed temperature drift is desired.

TYPICAL APPLICATION



Temperature Drift LT1034C-1.2



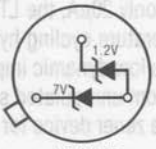
7

ABSOLUTE MAXIMUM RATINGS

Operating Current 20mA
Forward Current (Note 1) 20mA
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature ..... –65°C to 150°C

Operating Temperature Range
LT1034BM, M ..... –55°C to 125°C
LT1034BI, I ..... –40°C to 85°C
LT1034BC, C ..... 0°C to 70°C

PACKAGE/ORDER INFORMATION

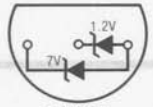


H PACKAGE
TO-46 METAL CAN
BOTTOM VIEW

T_{JMAX} = 150°C, θ_{JA} = 440°C/W, θ_{JC} = 80°C/W

ORDER PART NUMBER

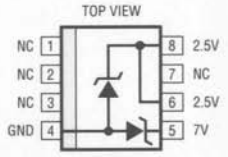
LT1034BMH-1.2
LT1034MH-1.2
LT1034BCH-1.2
LT1034CH-1.2
LT1034BMH-2.5
LT1034MH-2.5
LT1034BCH-2.5
LT1034CH-2.5



Z PACKAGE
TO-92 PLASTIC
BOTTOM VIEW

T_{JMAX} = 100°C, θ_{JA} = 160°C/W

LT1034BCZ-1.2
LT1034CZ-1.2
LT1034BCZ-2.5
LT1034CZ-2.5
LT1034IZ-1.2
LT1034IZ-2.5



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1034CS8-1.2
LT1034CS8-2.5
LT1034IS8-2.5

PART MARKING

3401 (1.2V VERSION)
3402 (2.5V VERSION)
34I02 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1034-1.2 MIN	LT1034-1.2 TYP	LT1034-1.2 MAX	LT1034-2.5 MIN	LT1034-2.5 TYP	LT1034-2.5 MAX	UNITS
Reverse Breakdown Voltage	I_R = 100µA	25°C	1.210	1.225	1.240	2.46	2.5	2.54	V
		●	1.205	1.225	1.245	2.43	2.5	2.57	V
Reverse Breakdown Change with Current	Note 3	25°C		0.5	2.0		1.0	3.0	mV
		●		1.0	4.0		1.5	6.0	mV
	2mA ≤ I_R ≤ 20mA	25°C		4.0	8.0		6.0	16	mV
		●		6.0	15.0		10	20	mV
Minimum Operating Current		●		10	20		15	30	µA
Temperature Coefficient	I_R = 100µA LT1034BM/BC	●		10	20		10	20	ppm/°C
	LT1034M/I/C	●		20	40		20	40	ppm/°C
Reverse Dynamic Impedance (Note 2)	I_R = 100µA	25°C		0.25	1.0		0.5	1.5	Ω
		●		0.50	2.0		1.0	2.5	Ω
Low Frequency Noise	I_R = 100µA, 0.1Hz ≤ F ≤ 10Hz	●		4			6		µVp-p
Long Term Stability	I_R = 100µA, T = 25°C	25°C		20			20		ppm/√khrs

ELECTRICAL CHARACTERISTICS 7V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	IR = 100μA	25°C	6.8	7.0	7.3	V
		●	6.75	7.0	7.4	V
Reverse Breakdown Change with Current	100μA ≤ IR ≤ 1mA	25°C		90	140	mV
	100μA ≤ IR ≤ 1mA	●		100	190	mV
	1mA ≤ IR ≤ 20mA	25°C		160	250	mV
	1mA ≤ IR ≤ 20mA	●		200	350	mV
Temperature Coefficient	IR = 100μA	●		40		ppm/°C
Long Term Stability	IR = 100μA	25°C		20		ppm

The ● denotes specifications that apply over the operating temperature range.

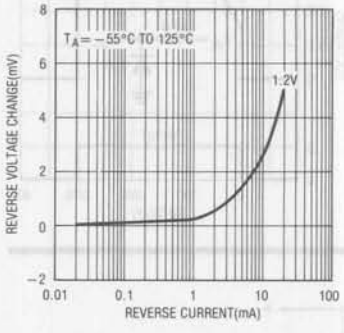
Note 1: Forward biasing either diode will affect the operation of the other diode.

Note 2: This parameter guaranteed by "reverse breakdown change with current" test.

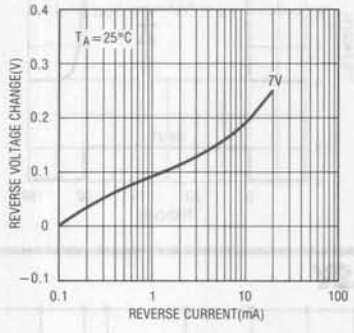
Note 3: For the LT1034-1.2, 20μA ≤ I_R ≤ 2mA. For the LT1034-2.5, 30μA ≤ I_R ≤ 2mA.

TYPICAL PERFORMANCE CHARACTERISTICS

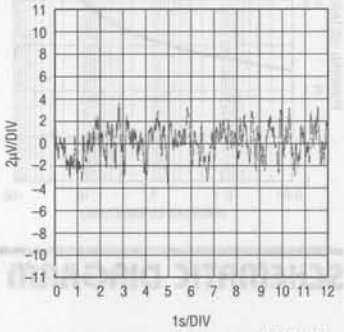
Reverse Voltage Change 1.2V



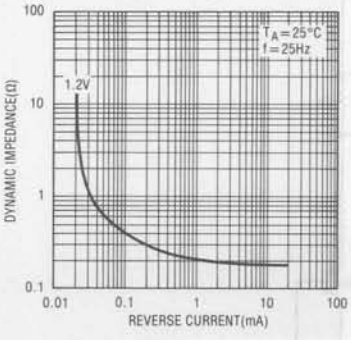
Reverse Voltage Change 7V



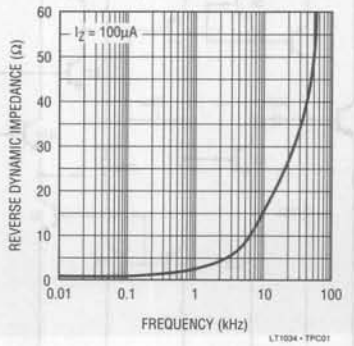
0.1Hz to 10Hz Noise 1.2V



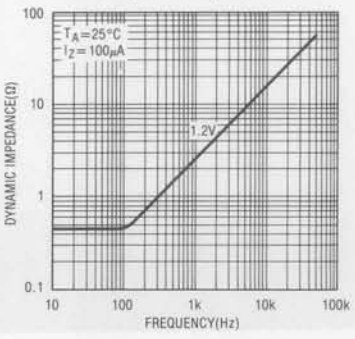
Reverse Dynamic Impedance 1.2V



Reverse Dynamic Impedance 2.5V



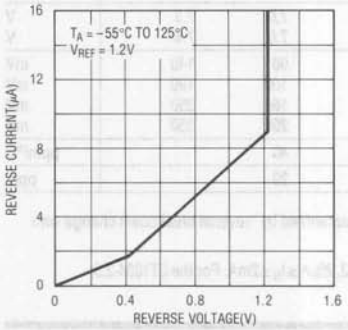
Reverse Dynamic Impedance 7V



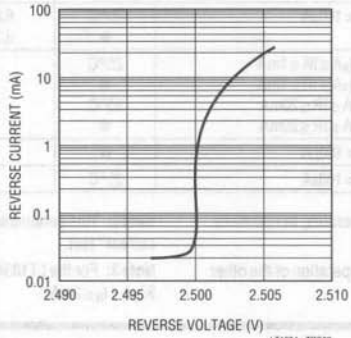
7

TYPICAL PERFORMANCE CHARACTERISTICS

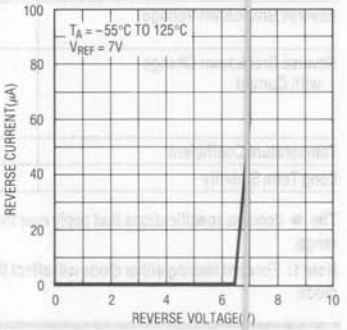
Reverse Characteristics 1.2V



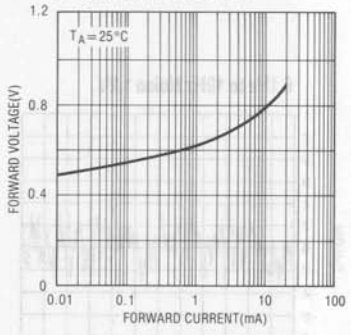
Reverse Characteristics 2.5V



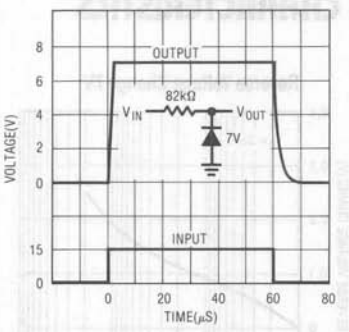
Reverse Characteristics 7V



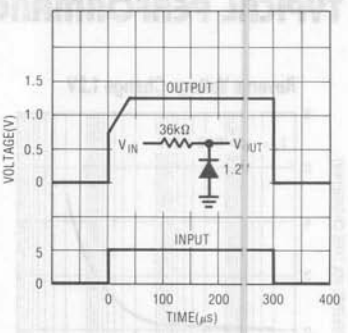
Forward Characteristics



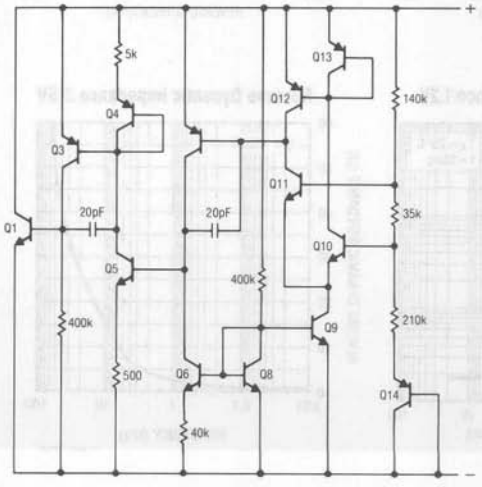
Response Time



Response Time



SCHEMATIC DIAGRAM 1.2V



LINEAR TECHNOLOGY

SECTION 8—MONOLITHIC FILTERS

8

SECTION 8—MONOLITHIC FILTERS

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SELECTION GUIDES 8-3

PROPRIETARY PRODUCTS

LTC1062, 5th Order Lowpass Filter 8-5

LTC1063, DC Accurate, Clock-Tunable 5th Order Butterworth Lowpass Filter 8-16

LTC1064-7, Linear Phase, 8th Order Lowpass Filter 8-28

LTC1065, DC Accurate, Clock-Tunable Linear Phase 5th Order Bessel Lowpass Filter 8-39

LTC1066-1, 14-Bit DC Accurate Clock-Tunable, 8th Order Elliptic or Linear Phase Lowpass Filter 8-51

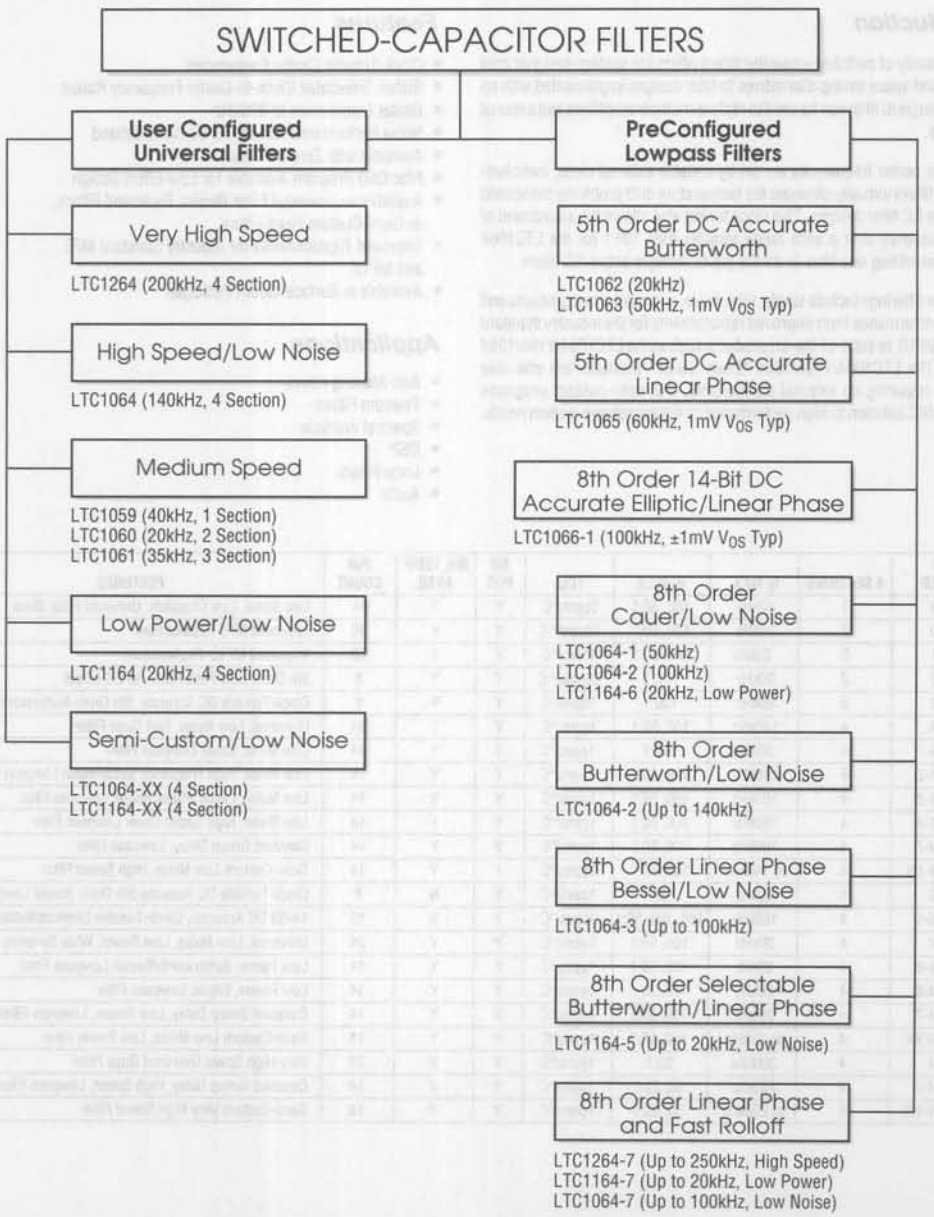
LTC1164-5, Low Power 8th Order Pin Selectable Butterworth or Bessel Lowpass Filter 8-67

LTC1164-6, Low Power 8th Order Pin Selectable Elliptic or Linear Phase Lowpass Filter 8-78

LTC1164-7, Low Power, Linear Phase 8th Order Lowpass Filter 8-89

LTC1264, High Speed, Quad Universal Filter Building Block 8-100

LTC1264-7, Linear Phase, Group Delay Equalized, 8th Order Lowpass Filter 8-115


SWITCHED-CAPACITOR FILTERS
User Configured Universal Filters
Very High Speed
LTC1264 (200kHz, 4 Section)
High Speed/Low Noise
LTC1064 (140kHz, 4 Section)
Medium Speed
LTC1059 (40kHz, 1 Section)
LTC1060 (20kHz, 2 Section)
LTC1061 (35kHz, 3 Section)
Low Power/Low Noise
LTC1164 (20kHz, 4 Section)
Semi-Custom/Low Noise
LTC1064-XX (4 Section)
LTC1164-XX (4 Section)
PreConfigured Lowpass Filters
5th Order DC Accurate Butterworth
LTC1062 (20kHz)
LTC1063 (50kHz, 1mV V_{OS} Typ)
5th Order DC Accurate Linear Phase
LTC1065 (60kHz, 1mV V_{OS} Typ)
8th Order 14-Bit DC Accurate Elliptic/Linear Phase
LTC1066-1 (100kHz, ±1mV V_{OS} Typ)
8th Order Cauer/Low Noise
LTC1064-1 (50kHz)
LTC1064-2 (100kHz)
LTC1164-6 (20kHz, Low Power)
8th Order Butterworth/Low Noise
LTC1064-2 (Up to 140kHz)
8th Order Linear Phase Bessel/Low Noise
LTC1064-3 (Up to 100kHz)
8th Order Selectable Butterworth/Linear Phase
LTC1164-5 (Up to 20kHz, Low Noise)
8th Order Linear Phase and Fast Rolloff
LTC1264-7 (Up to 250kHz, High Speed)
LTC1164-7 (Up to 20kHz, Low Power)
LTC1064-7 (Up to 100kHz, Low Noise)

ANALOG FILTER SELECTION GUIDE

Introduction

The LTC family of switched-capacitor filters offers the system designer cost effective and space saving alternatives to filter designs implemented with op amps. A single IC filter can be used to replace multiple amplifiers and external capacitors.

Since their center frequencies are set by a stable external clock, switched-capacitor filters virtually eliminate the temperature drift problems associated with active RC filter designs. This clock tuning also allows the adjustment of corner frequency over a wide range (greater than 10^6:1 for the LTC1064 family), permitting one filter to do the job of multiple active RC filters.

LTC's filter offerings include single, dual, triple, and quad block products and range in performance from improved replacements for the industry standard MF5 and MF10, to state-of-the-art products such as the LTC1064/1164/1264 families. The LTC1064/1164/1264 "Dash Series" products are one chip solutions requiring no external components. Our semi-custom programs offer an ASIC solution to high performance or higher volume system needs.

Features

- Clock-Tunable Center Frequencies
- Stable, Selectable Clock-to-Center Frequency Ratios
- Center Frequencies to 300kHz
- Noise Performance As Low As 80µV, Wideband
- Available with Zero DC Offset
- FilterCAD Program Available for Low-Effort Design
- Available as Universal Filter Blocks, Dedicated Filters, or Semi-Custom Fixed Filters
- Improved Replacements for Industry Standard MF5 and MF10
- Available in Surface Mount Packages

Applications

- Anti-Aliasing Filters
- Telecom Filters
- Spectral Analysis
- DSP
- Loop Filters
- Audio

PART NUMBER	# SECTIONS	f_0 MAX	fO/fCLK	TCf_0	SO PKG	MIL TEMP AVAIL	PIN COUNT	FEATURES
LTC1059	1	40kHz	100, 50:1	5ppm/°C	Y	Y	14	Low Noise, Low Crosstalk, Universal Filter Block
LTC1060	2	20kHz	100, 50:1	10ppm/°C	Y	Y	20	Improved MF5 Replacement
LTC1061	3	35kHz	100, 50:1	1ppm/°C	Y	Y	20	Improved MF10 Replacement
LTC1062	2	20kHz	100:1	10ppm/°C	Y	Y	8	5th Order Low Pass Filter, No DC Offset
LTC1063	3	50kHz	100:1	1ppm/°C	Y	N	8	Clock-Tunable DC Accurate 5th Order Butterworth Lowpass
LTC1064	4	140kHz	100, 50:1	1ppm/°C	Y	Y	24	Universal, Low Noise, Fast Quad Filter
LTC1064-1	4	50kHz	100:1	1ppm/°C	Y	Y	14	Low Noise, Cauer Lowpass Filter
LTC1064-2	4	140kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Noise, High Frequency Butterworth Lowpass Filter
LTC1064-3	4	100kHz	150, 75:1	1ppm/°C	Y	Y	14	Low Noise, Linear Phase Bessel Lowpass Filte
LTC1064-4	4	100kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Noise, High Speed Cauer Lowpass Filter
LTC1064-7	4	100kHz	100, 50:1	1ppm/°C	Y	Y	14	Constant Group Delay, Lowpass Filter
LTC1064-XX	4	to 140kHz	100, 50:1	1ppm/°C	Y	Y	14	Semi-Custom Low Noise, High Speed Filter
LTC1065	3	50kHz	100:1	1ppm/°C	Y	N	8	Clock-Tunable DC Accurate 5th Order Bessel Lowpass
LTC1066-1	4	100kHz	160, 100, 50:1	1ppm/°C	Y	N	18	14-Bit DC Accurate, Clock-Tunable Elliptical/Butterworth
LTC1164	4	20kHz	100, 50:1	1ppm/°C	Y	Y	24	Universal, Low Noise, Low Power, Wide Dynamic Range Filter
LTC1164-5	4	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Power, Butterworth/Bessel Lowpass Filte
LTC1164-6	4	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Power, Elliptic Lowpass Filter
LTC1164-7	4	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Constant Group Delay, Low Power, Lowpass Filter
LTC1164-XX	4	to 20kHz	100, 50:1	1ppm/°C	Y	Y	14	Semi-Custom Low Noise, Low Power Filter
LTC1264	4	300kHz	20:1	1ppm/°C	Y	Y	24	Very High Speed Universal Quad Filter
LTC1264-7	4	250kHz	50, 25:1	1ppm/°C	Y	Y	14	Constant Group Delay, High Speed, Lowpass Filter
LTC1264-XX	4	to 250kHz	50, 25:1	1ppm/°C	Y	Y	14	Semi-Custom Very High Speed Filter

5th Order Lowpass Filter

FEATURES

- Lowpass Filter with No DC Error
- Low Passband Noise
- Operates DC to 20kHz
- Operates on a Single 5V Supply or Up to ±8V
- 5th Order Filter
- Maximally Flat Response
- Internal or External Clock
- Cascadable for Faster Rolloff
- Buffer Available
- 8 Pin DIP Package

APPLICATIONS

- 60Hz Lowpass Filters
- Anti-Aliasing Filter
- Low Level Filtering
- Rolling Off AC Signals from High DC Voltages
- Digital Voltmeters
- Scales
- Strain Gauges

DESCRIPTION

The LTC1062 is a 5th order all pole maximally flat lowpass filter with no DC error. Its unusual architecture puts the filter outside the DC path so DC offset and low frequency noise problems are eliminated. This makes the LTC1062 very useful for lowpass filters where DC accuracy is important.

The filter input and output are simultaneously taken across an external resistor. The LTC1062 is coupled to the signal through an external capacitor. This R,C reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is typically 100:1, allowing the clock ripple to be easily removed.

Two LTC1062s can be cascaded to form a 10th order quasi max flat lowpass filter. The device can be operated with single or dual supplies ranging from ±2.5V to ±9V.

The LTC1062 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

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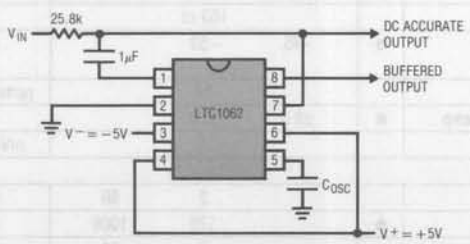
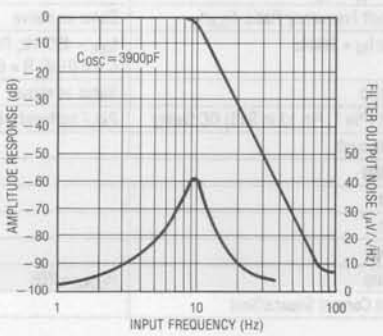
TYPICAL APPLICATION

10Hz 5th Order Butterworth Lowpass Filter



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50K POT FROM PIN 5 TO GROUND.

Filter Amplitude Response and Noise

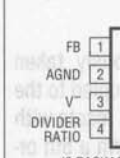


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage at Any Pin ..... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature Range
LTC1062M ..... $-55°C \le T_A \le 125°C$
LTC1062C ..... $-40°C \le T_A \le 85°C$
Storage Temperature Range ..... −65°C to 150°C

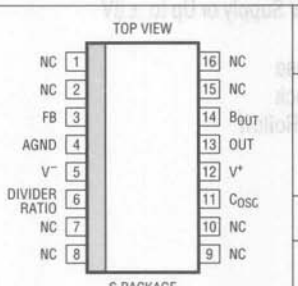
PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD HERMETIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N)

N8 PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1062MJ8
LTC1062CJ8
LTC1062CN8



S PACKAGE
16-LEAD PLASTIC SOL
T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC1062CS
PART MARKING
LTC1062CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 5V, V^- = −5V, T_A = 25°C unless otherwise specified, AC output measured at pin 7, Figure 1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Current	C_{OSC} (Pin 5 to V^-, Pin 11 in S16) = 100pF			4.5	7	mA
		●			10	mA
Input Frequency Range				0k - 20k		Hz
Filter Gain at f_{IN} = 0	f_{CLK} = 100kHz, Pin 4, (Pin 6 in S16) at V^+			0.00		dB
$f_{IN} = 0.5f_C$ (Note1)	C = 0.01µF, R = 25.78k			−0.02	−0.3	dB
$f_{IN} = f_C$		●	−2	−3.00		dB
$f_{IN} = 2f_C$		●	−28	−30.00		dB
$f_{IN} = 4f_C$		●	−52	−60.00		dB
Clock to Cutoff Frequency Ratio, f_{CLK}/f_C	Same as above			100 ±1		%
Filter Gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+	●	−45	−52		dB
	C = 0.01µF, R = 6.5k					
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7, Pin 13 in S16) DC Swing	Pin 7 buffered with an external op amp	●	±3.5	±3.8		V
Clock Feedthrough				1		mV_{P-P}
Internal Buffer						
Bias Current				2	50	pA
Bias Current		●		170	1000	pA
Offset Voltage				2	20	mV
Voltage Swing	R_{LOAD} = 20k	●	±3.5	±3.8		V
Short-Circuit Current Source/Sink				40/3		mA

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5V$, $V^- = -5V$, $T_A = 25°C$ unless otherwise specified, AC output measured at pin 7, Figure 1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock (Note 3)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-, Pin 11 in S16) = 100pF		25	32	50	kHz
	C_{OSC} (Pin 5 to V^-, Pin 11 in S16) = 100pF	●	15		65	kHz
Max Clock Frequency				4		MHz
Pin 5 (Pin 11 in S16) Souce or Sink Current		●		40	80	µA

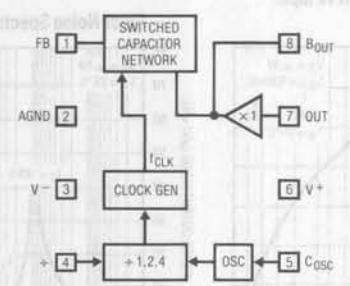
The ● denotes specifications which apply over the full operating temperature range.

Note 1: f_C is the frequency where the gain is –3dB with respect to the input signal.

Note 2: The LTC1062M operates from $-55° \le T_A \le 125°C$, the LTC1062C operates from $-40°C \le T_A \le 85°C$.

Note 3: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. For the J8, N8 package, when pin 4 = V^+, ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^-, ratio = 4.

BLOCK DIAGRAM (J8 or N8 package)

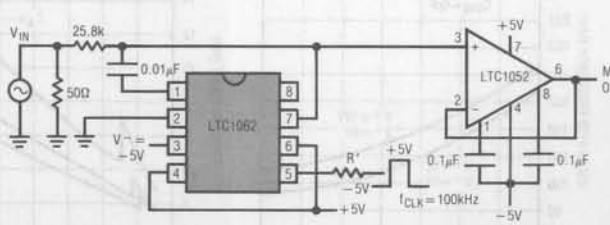


BY CONNECTING PIN 4 TO V^+, AGND, OR V^-, THE OUTPUT FREQUENCY OF THE INTERNAL CLOCK GENERATOR IS THE OSCILLATOR FREQUENCY DIVIDED BY 1,2,4. THE (f_{CLK}/f_C) RATIO OF 100:1 IS WITH RESPECT TO THE INTERNAL CLOCK GENERATOR OUTPUT FREQUENCY. PIN 5 CAN BE DRIVEN WITH AN EXTERNAL CMOS LEVEL CLOCK. THE LTC1062 CAN ALSO BE SELF-CLOCKED BY CONNECTING AN EXTERNAL CAPACITOR (C_{OSC}) TO GROUND (OR TO V^- IF C_{OSC} IS POLARIZED). UNDER THIS CONDITION AND WITH ±5V SUPPLIES, THE INTERNAL OSCILLATOR FREQUENCY IS:

$f_{OSC} = 140kHz\ [33pF/(33pF + C_{OSC})]$.

For Adjusting Oscillator Frequency, Insert a 50K Pot in Series with C_{OSC}. Use Two Times Calculated C_{OSC}.

AC TEST CIRCUIT



FOR BEST MAX. FLAT APPROXIMATION, THE INPUT R,C SHOULD BE SUCH AS:

$$\frac{1}{2\pi RC} = \frac{f_{CLK}}{100} \times 1.63$$

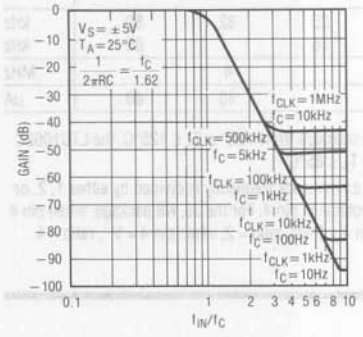
A 0.5K RESISTOR, R', SHOULD BE USED IF THE BIPOLAR EXTERNAL CLOCK IS APPLIED BEFORE THE POWER SUPPLIES TURN ON.

Figure 1.

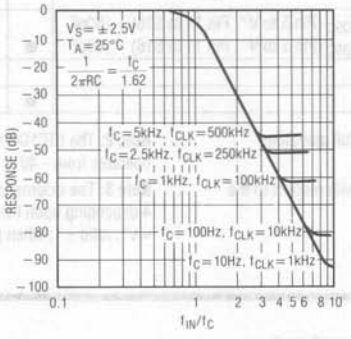
8

TYPICAL PERFORMANCE CHARACTERISTICS

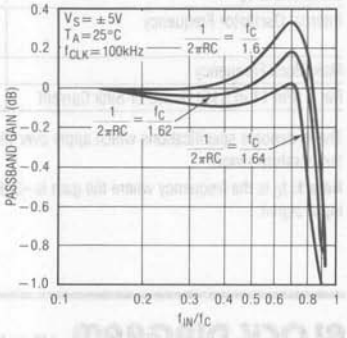
Amplitude Response Normalized to the Cutoff Frequency



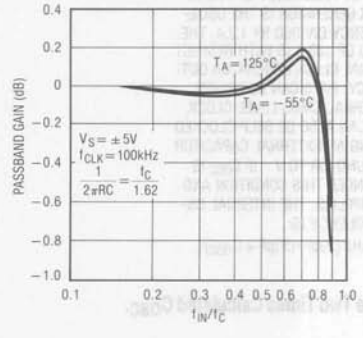
Amplitude Response Normalized to the Cutoff Frequency



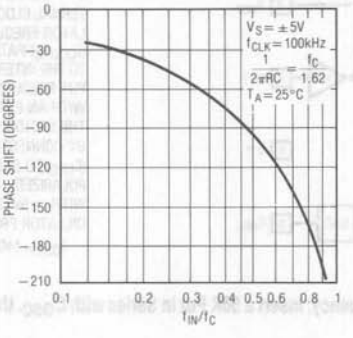
Passband Gain vs Input Frequency



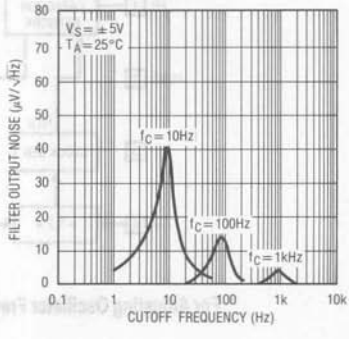
Passband Gain vs Input Frequency



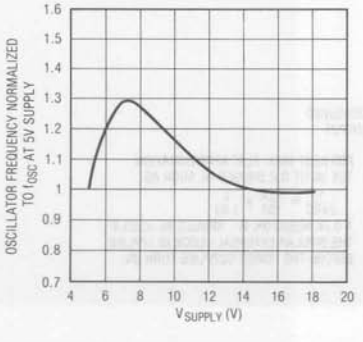
Passband Phase Shift vs Input Frequency



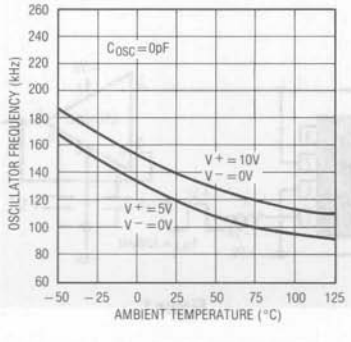
Filter Noise Spectral Density



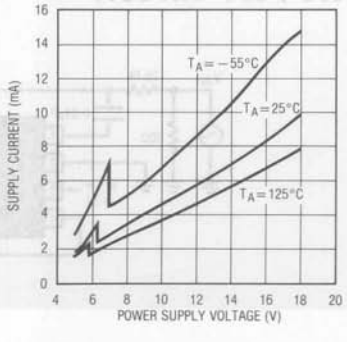
Normalized Oscillator Frequency, f_{OSC} vs Supply Voltage



Oscillator Frequency, f_{OSC} vs Ambient Temperature



Power Supply Current vs Power Supply Voltage



APPLICATIONS INFORMATION

Filter Input Voltage Range

Every node of the LTC1062 typically swings within 1V of either voltage supply, positive or negative. With the appropriate external (R,C) values, the amplitude response of all the internal or external nodes does not exceed a gain of 0 dB with the exception of pin 1. The amplitude response of the feedback node (pin 1) is shown in Figure 2. For an input frequency around $0.8 \times f_C$, the gain is 1.7 V/V and, with ±5V supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform occur, but the filter will not get damaged nor will it oscillate. Also, the absolute maximum input voltage should not exceed the power supplies.

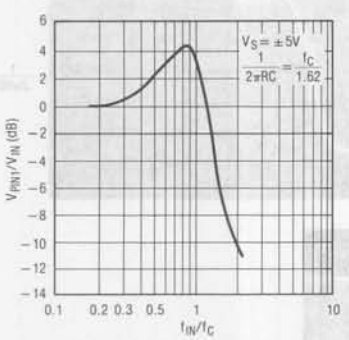


Figure 2. Amplitude Response of Pin 1

Internal Buffer

The internal buffer out (pin 8) and pin 1 are part of the signal AC path. Excessive capacitive loading will cause gain errors in the passband, especially around the cutoff frequency. The internal buffer gain at DC is typically 0.006dB. The internal buffer output can be used as a filter output, however it has a few millivolts of DC offset. The temperature coefficient of the internal buffer is typically 1μV/°C.

Filter Attenuation

The LTC1062 rolloff is typically 30dB/octave. When the clock, and the cutoff frequencies increase, the filter's maximum attenuation decreases. This is shown in the Typical Performance Characteristics. The decrease of the maximum attenuation, is due to the roll off at higher frequencies of the loop gains of the various internal feedback paths and not to the increase of the noise floor. For instance, for a 100kHz clock and 1kHz cutoff frequency, the maximum attenuation is about 64dB. A 4kHz, 1Vrms input signal will be predictably attenuated by 60dB at the output. A 6kHz, 1Vrms input signal will be attenuated by 64dB and not by 77dB as an ideal 5th order maximum flat filter would have dictated. The LTC1062 output at 6kHz will be about 630μVrms. The measured rms noise from DC to 17kHz was 100μVrms which is 16dB below the filter output.

C_{OSC}, Pin 5

The C_{OSC}, pin 5, can be used with an external capacitor, C_{OSC}, connected from pin 5 to ground. If C_{OSC} is polarized it should be connected from pin 5 to the negative supply, pin 3. C_{OSC} lowers the internal oscillator frequency. If pin 5 is floating, an internal 33pF capacitor plus the external interpin capacitance set the oscillator frequency around 140kHz with ±5V supply. An external C_{OSC} will bring the oscillator frequency down by the ratio (33pF)/(33pF + C_{OSC}). The typical performance characteristics curves provide the necessary information to get the internal oscillator frequency for various power supply ranges. Pin 5 can also be driven with an external CMOS clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 5, they will, in reality, drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1062 C_{OSC} pins. The typical trip levels of the internal Schmitt trigger which input is pin 5, are given below.

V SUPPLY	$V_{th}+$	$V_{th}-$
±2.5V	+0.9V	−1V
±5V	+1.3V	−2.1V
±6V	+1.7V	−2.5V
±7V	+1.75V	−2.9V

8

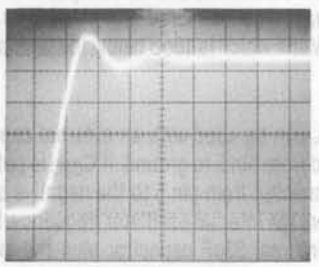
APPLICATIONS INFORMATION

Divide By 1, 2, 4 (Pin 4)

By connecting pin 4 to V^+, to mid supplies or to V^-, the clock frequency driving the internal switched capacitor network is the oscillator frequency divided by 1, 2, 4, respectively. Note that the f_{CLK}/f_C ratio of 100:1 is with respect to the internal clock generator output frequency. The internal divider is useful for applications where octave tuning is required. The ÷2 threshold is typically ±1V from the mid supply voltage.

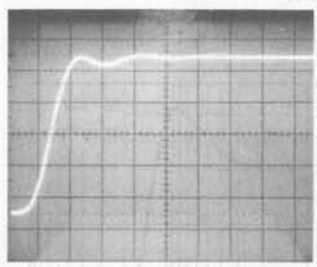
Transient Response

Figure 3 shows the LTC1062 response to a 1V input step.

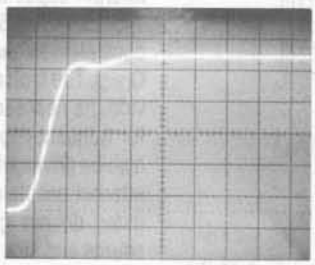


200mV/VERT DIV
50ms/HORIZ DIV, $f_c = 10Hz$
5ms/HORIZ DIV, $f_c = 100Hz$
0.5ms/HORIZ DIV, $f_c = 1kHz$

$$\frac{1}{2\pi RC} = \frac{f_c}{1.62}$$



$$\frac{1}{2\pi RC} = \frac{f_c}{1.94}$$



$$\frac{1}{2\pi RC} = \frac{f_c}{2.11}$$

Figure 3. Step Response to a 1V Peak Input Step

Filter Noise

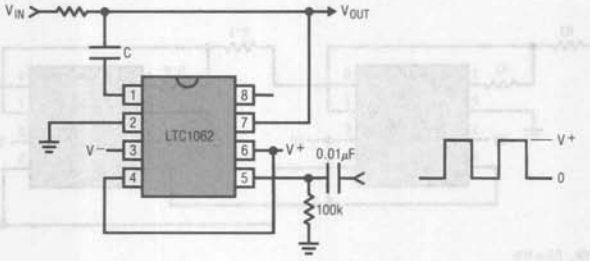
The filter wideband rms noise is typically 100μVrms for ±5V supply and it is nearly independent from the value of the cutoff frequency. For single 5V supply the rms noise is 80μVrms. Sixty-two percent of the wideband noise is in the passband, that is from DC to f_C. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below $0.1 \times f_C$. This is shown in the typical performance characteristics section. Table 1 shows the LTC1062 rms noise for different noise bandwidths.

Table 1

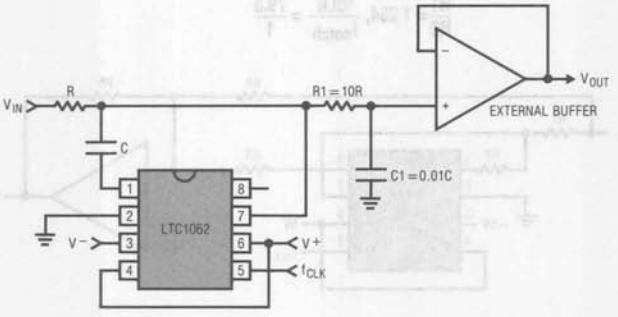
NOISE BW	rms NOISE $V_S = \pm 5V$
DC – $0.1 \times f_C$	2μV
DC – $0.25 \times f_C$	8μV
DC – $0.5 \times f_C$	20μV
DC – $1 \times f_C$	62μV
DC – $2 \times f_C$	100μV

TYPICAL APPLICATIONS

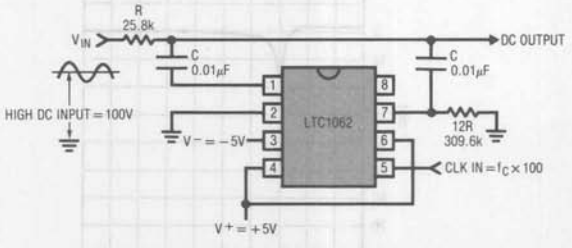
AC Coupling an External CMOS Clock Powered from a Single Positive Supply, V+



Adding an External (R1, C1) to Eliminate the Clock Feedthrough and to Improve the High Frequency Attenuation Floor

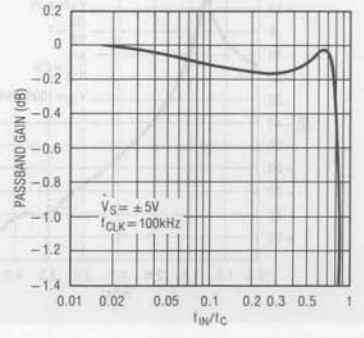


Filtering AC Signals from High DC Voltages



EX: f_{CLK} = 100kHz, f_C = 1kHz. THE FILTER ACCURATELY PASSES THE HIGH DC INPUT AND ACTS AS 5th ORDER LP FILTER FOR THE AC SIGNALS RIDING ON THE DC.

Passband Amplitude Response for the High DC Accurate 5th Order Filter



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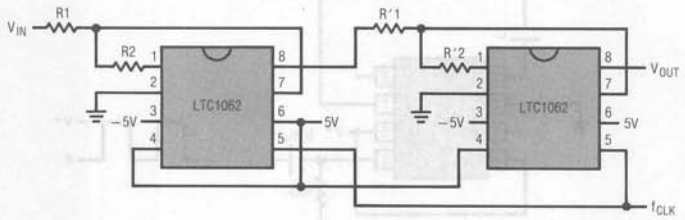
TYPICAL APPLICATIONS

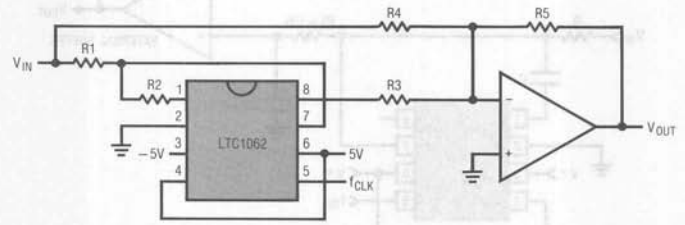
Cascading Two LTC1062s to Form a Very Selective Clock Sweepable Bandpass Filter



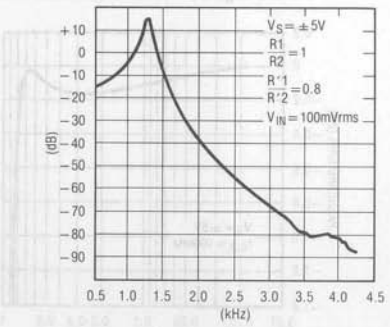
R1 = 10k, R2 = 10k
R'1 = 10k, R'2 = 12.5k

Clock Tunable Notch Filter
For simplicity use R3 = R4 = R5 = 10k;

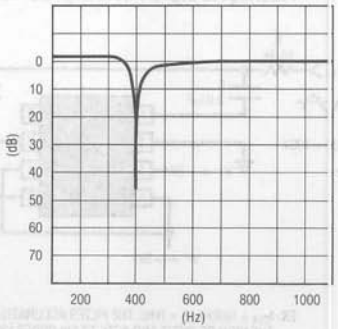
$$\frac{R1}{R2} = 1.234, \frac{f_{CLK}}{f_{notch}} = \frac{79.3}{1}$$



Frequency Response of the Bandpass Filter

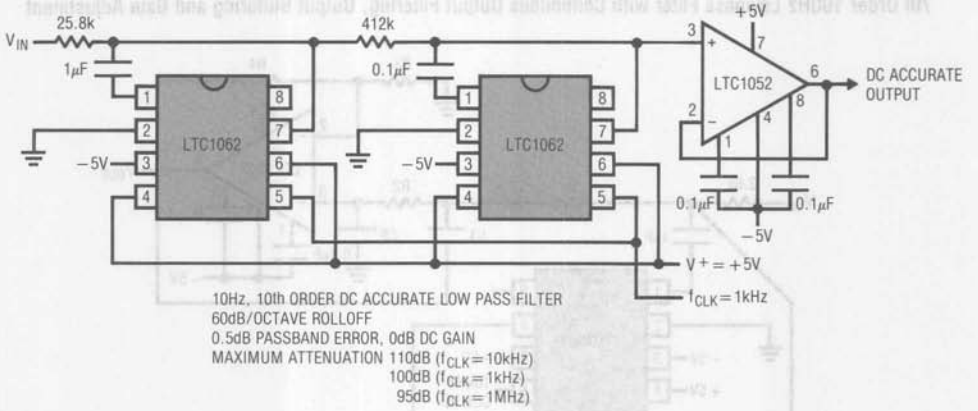


Frequency Response of the Notch Filter



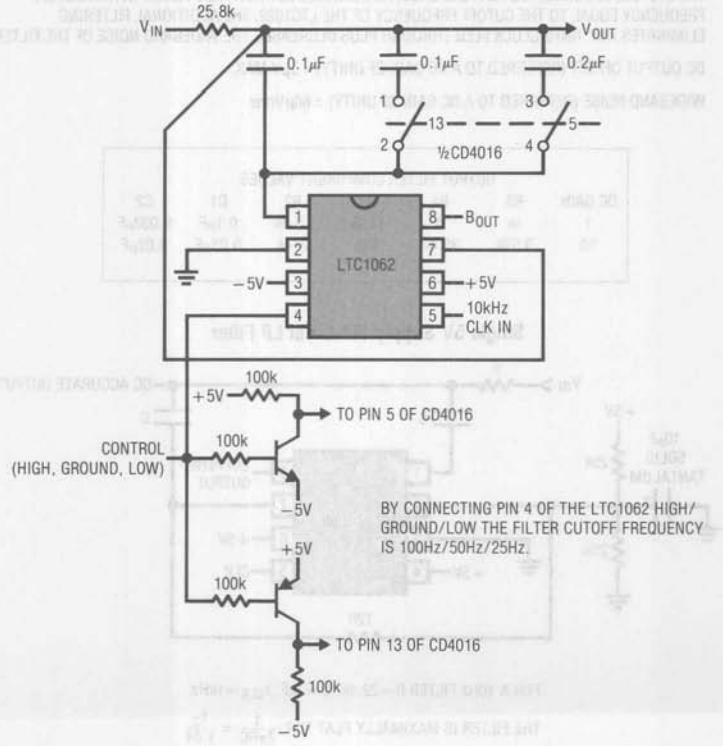
TYPICAL APPLICATIONS

Simple Cascading Technique



10Hz, 10th ORDER DC ACCURATE LOW PASS FILTER
60dB/OCTAVE ROLLOFF
0.5dB PASSBAND ERROR, 0dB DC GAIN
MAXIMUM ATTENUATION 110dB (f_{CLK} = 10kHz)
100dB (f_{CLK} = 1kHz)
95dB (f_{CLK} = 1MHz)

100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter



BY CONNECTING PIN 4 OF THE LTC1062 HIGH/GROUND/LOW THE FILTER CUTOFF FREQUENCY IS 100Hz/50Hz/25Hz.

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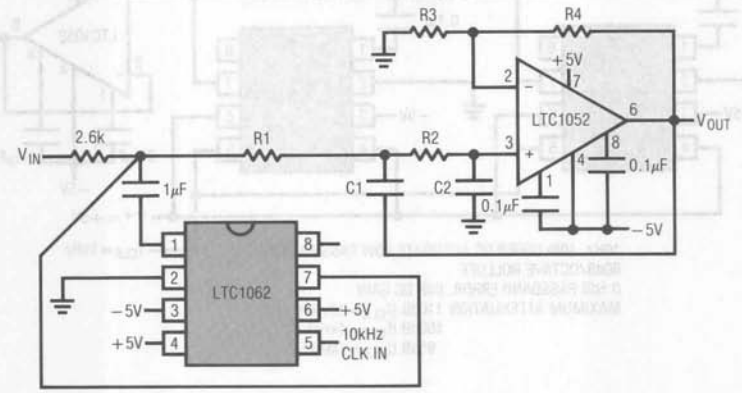
TYPICAL APPLICATIONS

7th Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment



THE LTC1052 IS CONNECTED AS A 2nd ORDER SALLEN AND KEY LOWPASS FILTER WITH A CUTOFF FREQUENCY EQUAL TO THE CUTOFF FREQUENCY OF THE LTC1062. THE ADDITIONAL FILTERING ELIMINATES ANY 10kHz CLOCK FEED THROUGH PLUS DECREASES THE WIDEBAND NOISE OF THE FILTER.

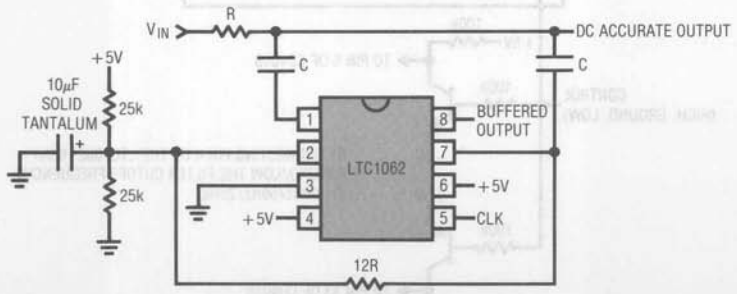
DC OUTPUT OFFSET (REFERRED TO A DC GAIN OF UNITY) = 5μV MAX.

WIDEBAND NOISE (REFERRED TO A DC GAIN OF UNITY) ≃ 60μVrms

OUTPUT FILTER COMPONENT VALUES

DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1μF	0.033μF
10	3.57k	32.4k	46k	274k	0.01μF	0.02μF

Single 5V Supply 5th Order LP Filter

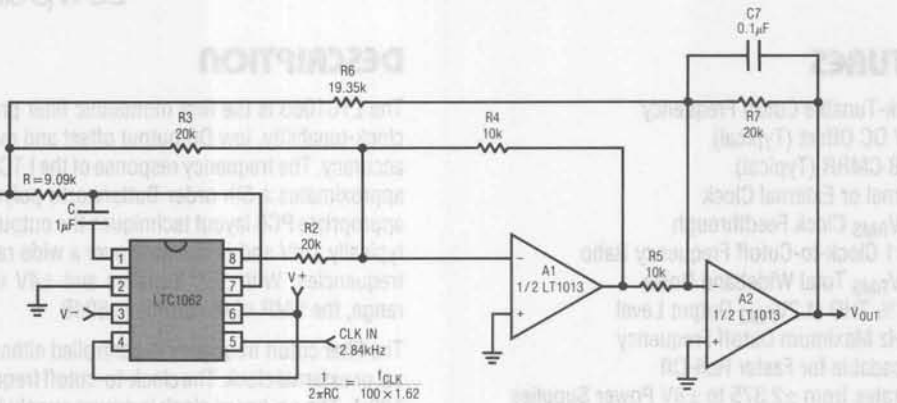


FOR A 10Hz FILTER R = 29.4k, C = 1μF, f_{CLK} = 1kHz

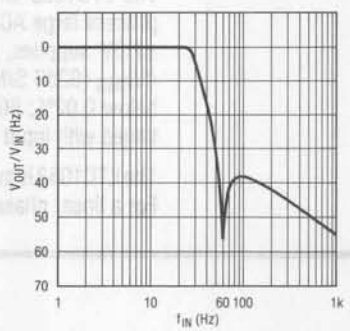
THE FILTER IS MAXIMALLY FLAT FOR $\frac{1}{2\pi RC} = \frac{f_C}{1.84}$

TYPICAL APPLICATIONS

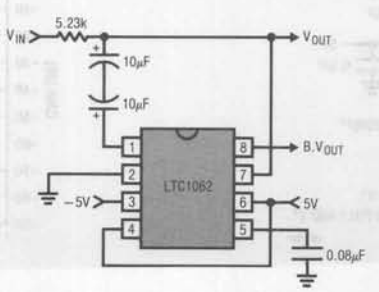
A Lowpass Filter with a 60Hz Notch



Frequency Response of the Above Lowpass Filter with the Notch $f_{NOTCH} = \frac{f_{CLK}}{47.3}$



A Low Frequency, 5Hz FIlter using Back-to-Back Solid Tantalum Capacitors



8

DC Accurate, Clock-Tunable 5th Order Butterworth Lowpass Filter

FEATURES

- Clock-Tunable Cutoff Frequency
- 1mV DC Offset (Typical)
- 80dB CMRR (Typical)
- Internal or External Clock
- $50\mu V_{RMS}$ Clock Feedthrough
- 100:1 Clock-to-Cutoff Frequency Ratio
- $95\mu V_{RMS}$ Total Wideband Noise
- 0.01% THD at $2V_{RMS}$ Output Level
- 50kHz Maximum Cutoff Frequency
- Cascadable for Faster Roll-Off
- Operates from ±2.375 to ±8V Power Supplies
- Self-Clocking with 1 RC

APPLICATIONS

- Audio
- Strain Gauge Amplifiers
- Anti-Aliasing Filters
- Low Level Filtering
- Digital Voltmeters
- 60Hz Lowpass Filters
- Smoothing Filters
- Reconstruction Filters

DESCRIPTION

The LTC1063 is the first monolithic filter providing both clock-tunability, low DC output offset and over 12-bit DC accuracy. The frequency response of the LTC1063 closely approximates a 5th order Butterworth polynomial. With appropriate PCB layout techniques the output DC offset is typically 1mV and is constant over a wide range of clock frequencies. With ±5V supplies and ±4V input voltage range, the CMR of the device is 80dB.

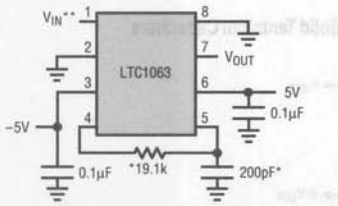
The filter cutoff frequency is controlled either by an internal or external clock. The clock-to-cutoff frequency ratio is 100:1. The on-board clock is power supply independent, and it is programmed via an external RC. The $50\mu V_{RMS}$ clock feedthrough is considerably reduced over existing monolithic filters.

The LTC1063 wideband noise is $95\mu V_{RMS}$, and it can process large AC input signals with low distortion. With ±7.5V supplies, for instance, the filter handles up to $4V_{RMS}$ (92dB S/N ratio) while the standard 1kHz THD is below 0.02%; 80dB dynamic ranges (S/N +THD) is obtained with input levels between $1V_{RMS}$ and $2.3V_{RMS}$.

The LTC1063 is available in 8-pin miniDIP and 16-pin SOL. For a linear phase response, see LTC1065 data sheet.

TYPICAL APPLICATION

2.5kHz 5th Order Lowpass Filter

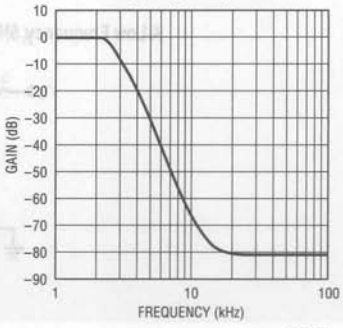


* SELF-CLOCKING SCHEME

** IF THE INPUT VOLTAGE CAN EXCEED V+, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V+.

1063 TA01

Frequency Response



1063 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Voltage at Any Input .... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Burn-In Voltage 16V

Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

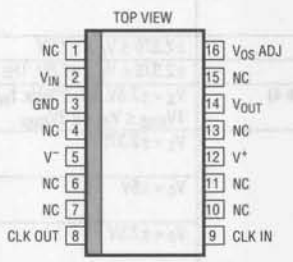
PACKAGE/ORDER INFORMATION

J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER

LTC1063CN8
LTC1063CJ8
LTC1063MJ8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 100°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1063CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Cutoff Frequency Ratio (f_{CLK}/f_C)	±2.375V ≤ V_S ≤ ±7.5V			100±0.5		
Maximum Clock Frequency (Note 1)	V_S = ±7.5V			5		MHz
	V_S = ±5V			4		MHz
	V_S = ±2.5V			3		MHz
Minimum Clock Frequency (Note 2)	±2.5V ≤ V_S ≤ ±7.5V, T_A < 85°C			30		Hz
Input Frequency Range			0		0.9f_{CLK}	
Filter Gain	V_S = ±5V, f_{CLK} = 25kHz, f_C = 250Hz					
	f_{IN} = 250Hz		–3.5	–3.0	–2.5	dB
		●	–3.6	–3.0	–2.4	dB
	V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz					
	f_{IN} = 100Hz			0		dB
	f_{IN} = 1kHz = 0.2f_C		–0.06	–0.01	0.04	dB
		●	–0.075	–0.01	0.055	dB
	f_{IN} = 2.5kHz = 0.5f_C		–0.09	0.16	0.41	dB
		●	–0.14	0.16	0.46	dB
	f_{IN} = 4kHz = 0.8f_C		–0.5	–0.2	0.1	dB
		●	–0.6	–0.2	0.2	dB
	f_{IN} = 5kHz = f_C		–3.5	–3.0	–2.5	dB
		●	–3.6	–3.0	–2.4	dB
	f_{IN} = 20kHz = 4f_C		–57.5	–60.0	–62.0	dB
		●	–57.0	–60.0	–62.5	dB

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ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $f_{CLK} = 500kHz$, $f_C = 5kHz$, $R_L = 10k$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain	$V_S = \pm 2.375V$, $f_{CLK} = 500kHz$, $f_C = 5kHz$					
	$f_{IN} = 1kHz$		−0.066	0.004	0.074	dB
		●	−0.081	0.004	0.089	dB
	$f_{IN} = 2.5kHz$		−0.24	0.16	0.56	dB
		●	−0.29	0.16	0.61	dB
	$f_{IN} = 4kHz$		−0.6	−0.2	0.2	dB
		●	−0.7	−0.2	0.3	dB
	$f_{IN} = 5kHz$		−3.5	−3.0	−2.5	dB
		●	−3.6	−3.0	−2.4	dB
Clock Feedthrough	$\pm 2.375 \le V_S \le \pm 7.5V$			50		μV_{RMS}
Wideband Noise (Note 3)	$\pm 2.375 \le V_S \le \pm 7.5V$, $1Hz < f < f_{CLK}$			100		μV_{RMS}
THD + Wideband Noise (Note 4)	$V_S = \pm 7.5V$, $f_C = 20kHz$, $f_{IN} = 1kHz$, $1V_{RMS} \le V_{IN} \le 2.3V_{RMS}$			−80		dB
Filter Output ± DC Swing	$V_S = \pm 2.375V$		1.6/−2.0	1.7/−2.2		V
		●	1.4/−1.8			V
	$V_S = \pm 5V$		4.0/−4.5	4.3/−4.8		V
		●	3.8/−4.3			V
	$V_S = \pm 7.5V$		6.5/−7.0	6.8/−7.3		V
		●	6.3/−6.8			V
Input Bias Current				10		nA
Dynamic Input Impedance				800		MΩ
Output DC Offset (Note 5)	$V_S = \pm 2.375V$			2		mV
	$V_S = \pm 5V$			0	±5	mV
	$V_S = \pm 7.5V$			−4		mV
Output DC Offset Drift	$V_S = \pm 2.375V$			10		µV/°C
	$V_S = \pm 5V$			20		µV/°C
	$V_S = \pm 7.5V$			25		µV/°C
Self-Clocking Frequency (f_{OSC})	R (Pin 4 to 5) = 20k, C (Pin 5 to GND) = 470pF					
	$V_S = \pm 2.375V$		99	105	112	kHz
	LTC1063CN, CS, CJ	●	95	103	111	kHz
	LTC1063MJ	●	92	100	114	kHz
	$V_S = \pm 5V$		102	108	114	kHz
	LTC1063CN, CS, CJ	●	98	106	114	kHz
	LTC1063MJ	●	97	105	114	kHz
	$V_S = \pm 7.5V$		104	110	116	kHz
	LTC1063CN, CS, CJ	●	101	109	116	kHz
	LTC1063MJ	●	100	108	116	kHz
External CLK Pin Logic Thresholds	$V_S = \pm 2.375V$ Min Logical "1"			1.43		V
	Max Logical "0"			0.47		V
	$V_S = \pm 5V$ Min Logical "1"			3		V
	Max Logical "0"			1		V
	$V_S = \pm 7.5V$ Min Logical "1"			4.5		V
	Max Logical "0"			1.5		V
Power Supply Current	$V_S = \pm 2.375V$, $f_{CLK} = 500kHz$			2.7	4.0	mA
	LTC1063CN, CS, CJ	●			5.5	mA
	LTC1063MJ	●			6.0	mA
	$V_S = \pm 5V$, $f_{CLK} = 500kHz$			5.5	8	mA
	LTC1063CN, CS, CJ	●			11	mA
	LTC1063MJ	●			12	mA
	$V_S = \pm 7.5V$, $f_{CLK} = 500kHz$			7.0	11	mA
	LTC1063CN, CS, CJ	●			14.5	mA
	LTC1063MJ	●			16.0	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The maximum clock frequency criterion is arbitrarily defined as: The frequency at which the filter AC response exhibits ≥ 1dB of gain peaking.

Note 2: At limited temperature ranges (i.e., $T_A \leq 50°C$) the minimum clock frequency can be as low as 10Hz. The minimum clock frequency is arbitrarily defined as: the clock frequency at which the output DC offset changes by more than 1mV.

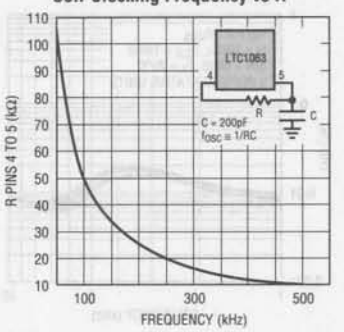
Note 3: The wideband noise specification does not include the clock feedthrough.

Note 4: To properly evaluate the filter's harmonic distortion an inverting output buffer is recommended as shown in the Test Circuit. An output buffer is not necessarily needed when measuring output DC offset or wideband noise.

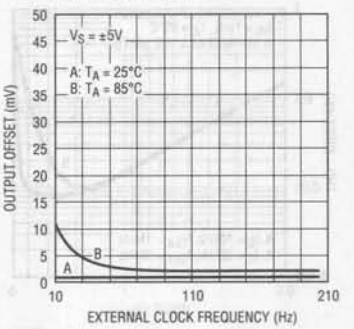
Note 5: The output DC offset is optimized for ±5V supply. The output DC offset shifts when the power supplies change; however this phenomenon is repeatable and predictable.

TYPICAL PERFORMANCE CHARACTERISTICS

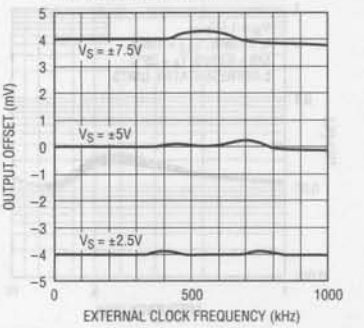
Self-Clocking Frequency vs R



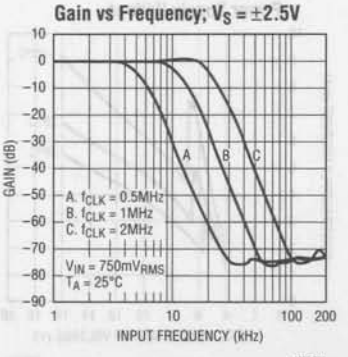
Output Offset vs Clock, Low Clock Rates



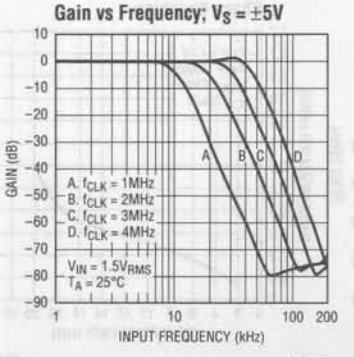
Output Offset vs Clock, Medium Clock Rates



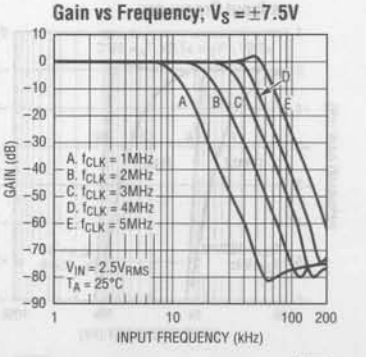
Gain vs Frequency; $V_S = \pm 2.5V$



Gain vs Frequency; $V_S = \pm 5V$



Gain vs Frequency; $V_S = \pm 7.5V$



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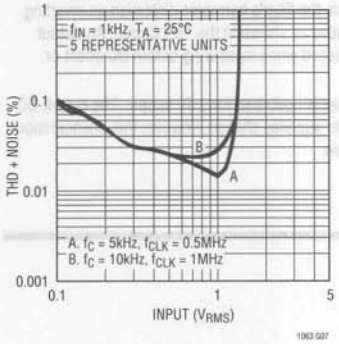
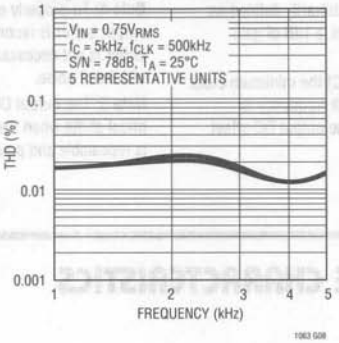
TYPICAL PERFORMANCE CHARACTERISTICS

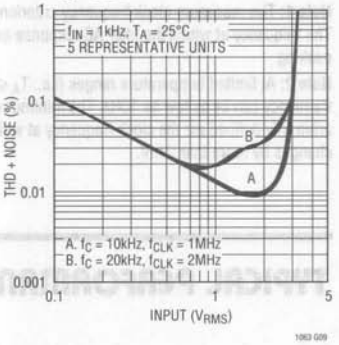
THD + Noise vs Input Voltage; V_S = Single 5V



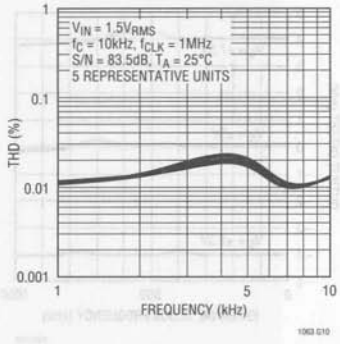
THD vs Frequency; V_S = Single 5V



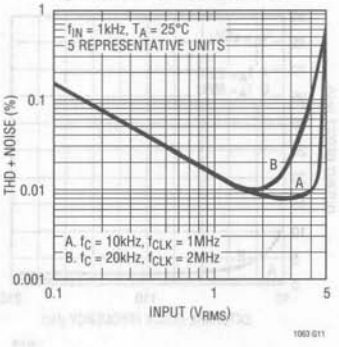
THD + Noise vs Input Voltage; V_S = ±5V



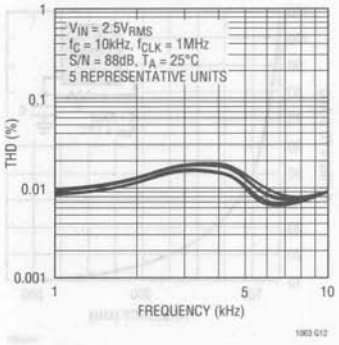
THD vs Frequency; V_S = ±5V



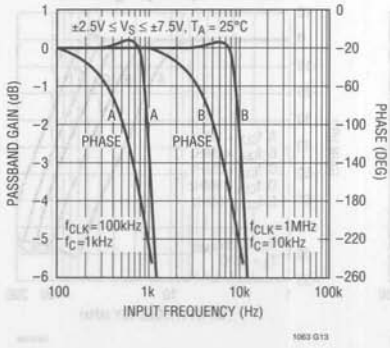
THD + Noise vs Input Voltage; V_S = ±7.5V



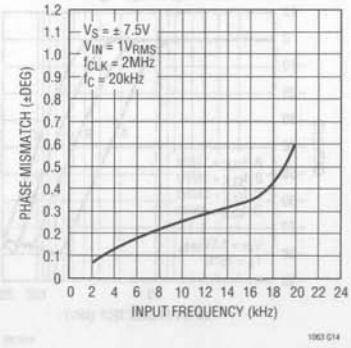
THD vs Frequency; V_S = ±7.5V



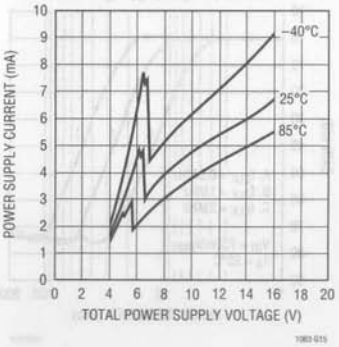
Passband Gain and Phase vs Input Frequency



Phase Matching

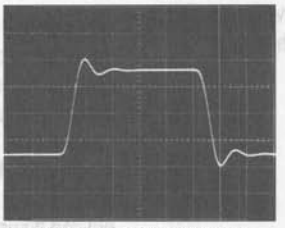


Power Supply Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



HORIZONTAL: 0.1ms/DIV, VERTICAL: 2V/DIV
$V_S = \pm 5V$, $f_C = 10kHz$, $V_{IN} = 1kHz \pm 3V_P$
SQUARE WAVE

1063 G15

PIN FUNCTIONS

Power Supply Pins (Pins 6, 3, N Package)

The positive and negative supply pin should be bypassed with a high quality 0.1µF ceramic capacitor. In applications where the clock pin (5) is externally swept to provide several cutoff frequencies, the output DC offset variation is minimized by connecting an additional 1µF solid tantalum capacitor in parallel with the 0.1µF disc ceramic. This technique was used to generate the graphs of the output DC offset variation versus clock; they are illustrated in the Typical Performance Characteristics section.

When the power supply voltage exceeds ±7V, and when V^- is applied before V^+, if V^+ is allowed to go below ground, connect a signal diode between the positive supply pin and ground to prevent latch-up (see Typical Applications).

Ground Pin (Pin 2, N Package)

The ground pin merges the internal analog and digital ground paths. The potential of the ground pin is the reference for the internal switched-capacitor resistors, and the reference for the external clock. The positive input of the internal op amp is also tied to the ground pin.

For dual supply operation, the ground pin should be connected to a high quality AC and DC ground. A ground plane, if possible, should be used. A poor ground will degrade DC offset and it will increase clock feedthrough, noise and distortion.

A small amount of AC current flows out of the ground pin whether or not the internal oscillator is used. The frequency of the ground current equals the frequency of the internal or external clock. The average value of this current is approximately 55µA, 110µA, 170µA for ±2.5V, ±5V and ±7.5V supplies respectively.

For single supply operation, the ground pin should be preferably biased at half supply (see Typical Applications).

V_{OS} Adjust Pin (Pin 8, N Package)

The V_{OS} adjust pin can be used to trim any small amount of output DC offset voltage or to introduce a desired output DC level. The DC gain from the V_{OS} adjust pin to the filter output pin equals two.

Any DC voltage applied to this pin will reflect at the output pin of the filter multiplied by two.

If the V_{OS} adjust pin is not used, it should be shorted to the ground pin. The DC bias current flowing into the V_{OS} adjust pin is typically 10pA.

Pin 8 should always be connected to an AC ground; AC signals applied to this pin will degrade the filter response.

Input Pin (Pin 1, N Package)

Pin 1 is the filter input and it is connected to an internal switched-capacitor resistor. If the input pin is left floating, the filter output will saturate. The DC input impedance of pin 1 is very high; with ±5V supplies and 1MHz clock, the DC input impedance is typically 1GΩ. A resistor, R_{IN}, in series, with the input pin will not alter the value of the

8

PIN FUNCTIONS

filter's DC output offset (Figure 1). R_{IN} should, however, be limited to a maximum value (Table 1), otherwise the filter's passband flatness will be affected. Refer to the Applications Information section for more details.

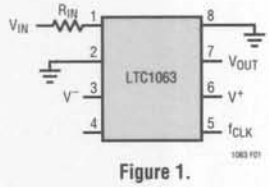


Figure 1.

Table 1. $R_{IN(MAX)}$ vs Clock and Power Supply

	$R_{IN(MAX)}$		
	$V_S = \pm 7.5V$	$V_S = \pm 5V$	$V_S = \pm 2.5V$
f_{CLK} = 4MHz	2.2k	–	–
f_{CLK} = 3MHz	3.4k	2.9k	–
f_{CLK} = 2MHz	5.5k	5k	2.7k
f_{CLK} = 1MHz	11k	11k	9.2k
f_{CLK} = 500kHz	24k	23k	21k
f_{CLK} = 100kHz	120k	120k	110k

Output Pin (Pin 7, N Package)

Pin 7 is the filter output. This pin can typically source over 20mA and sink 2mA. Pin 7 should not drive long coax cables, otherwise the filter's total harmonic distortion will degrade.

Clock Input Pin (Pin 5, N Package)

An external clock when applied to pin 5 tunes the filter cutoff frequency. The clock-to-cutoff frequency ratio is 100:1. The high (V_{HIGH}) and low (V_{LOW}) clock logic threshold levels are illustrated in Table 2. Square wave clocks with duty cycles between 30% and 50% are strongly recommended. Sinewave clocks are not recommended.

Table 2. Clock Pin Threshold Levels

POWER SUPPLY	V_{HIGH}	V_{LOW}
$V_S = \pm 2.5V$	1.5V	0.5V
$V_S = \pm 5V$	3V	1V
$V_S = \pm 7.5V$	4.5V	1.5V
$V_S = \pm 8V$	4.8V	1.6V
V_S = 5V, 0V	4V	3V
V_S = 12, 0V	9.6V	7.2V
V_S =15V, 0V	12V	9V

Clock Output Pin (Pin 4, N Package)

Any external clock applied to the clock input pin appears at the clock output pin. The duty cycle of the clock output equals the duty cycle of the external clock applied to the clock input pin. The clock output pin swings to the power supply rails. When the LTC1063 is used in a self-clocking mode, the clock of the internal oscillator appears at the clock output pin with a 30% duty cycle. The clock output pin can be used to drive other LTC1063s or other ICs. The maximum capacitance, $C_{L(MAX)}$, the clock output pin can drive is illustrated in Figure 3.

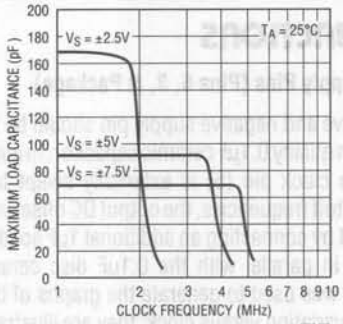


Figure 3. Maximum Load Capacitance at the Clock Output Pin

TEST CIRCUIT

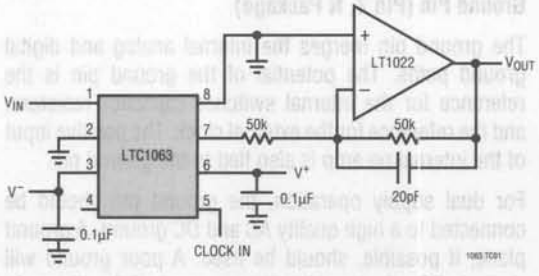


Figure 2. Test Circuit for THD

APPLICATIONS INFORMATION

Self-Clocking Operation

The LTC1063 features an internal oscillator which can be tuned via an external RC. The LTC1063's internal oscillator is primarily intended for generation of clock frequencies below 500kHz. The first curve of the Typical Performance Characteristics section shows how to quickly choose the value of the RC for a given frequency. More precisely, the frequency of the internal oscillator is equal to:

$$f_{CLK} = K/RC$$

For clock frequencies (f_{CLK}) below 100kHz, K equals 1.07. Figure 4b shows the variation of the parameter K versus clock frequency and power supply. First choose the desired clock frequency, (f_{CLK} < 500kHz), then through Figure 4b pick the right value of K, set C = 200pF and solve for R.

Example 1: f_{CUTOFF} = 2kHz, f_{CLK} = 200kHz, V_S = ±5V, T_A = 25°C, K = 1.0, C = 200pF

then, $R = (1.0)/(200kHz \times 204pF) = 24.5k$.

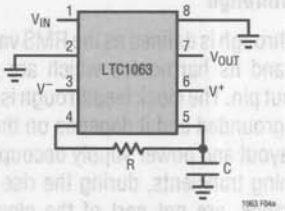


Figure 4a.

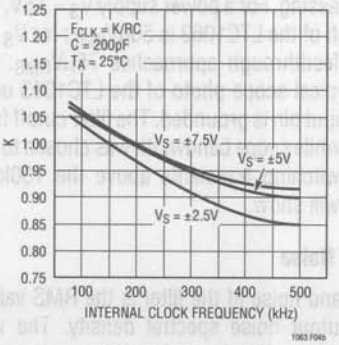


Figure 4b. f_{CLK} vs K

Note a 4pF parasitic capacitance is assumed in parallel with the external 200pF timing capacitor. Figure 5 shows the clock frequency variation from –40°C to 85°C. The 200kHz clock of Example 1 will change by –1.75% at 85°C.

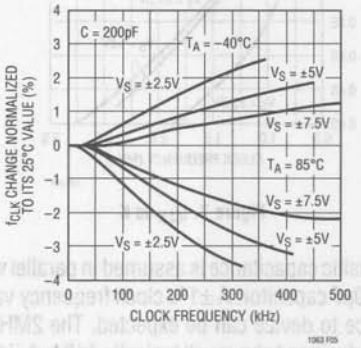


Figure 5. f_{CLK} vs Temperature

For a very limited temperature range, the internal oscillator of the LTC1063 can be used to generate clock frequencies above 500kHz (Figures 6 and 7). The data of Figure 6 is derived from several devices. For a given external (RC) value, the observed device-to-device clock frequency variation was ±1% (V_S = ±5V), and ±1.25% for V_S = ±2.5V.

Example 2: f_{CUTOFF} = 20kHz, f_{CLK} = 2MHz, V_S = ±7.5V, T_A = 25°C, C = 10pF

from Figure 6, K = 0.575,

and, $R = (0.575)/(2MHz \times 14pF) = 20.5k$.

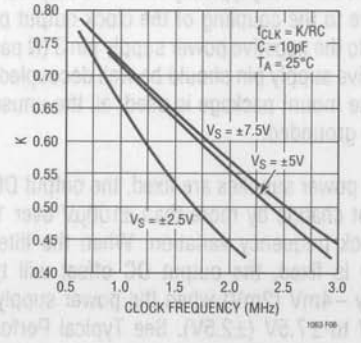


Figure 6. f_{CLK} vs K

APPLICATIONS INFORMATION

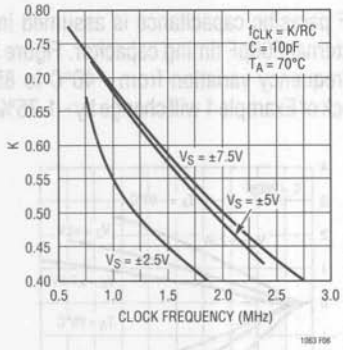


Figure 7. f_{CLK} vs K

A 4pF parasitic capacitance is assumed in parallel with the external 10pF capacitor. A ±1% clock frequency variation from device to device can be expected. The 2MHz clock frequency designed above will typically drift to 1.74MHz at 70°C (Figure 7).

The internal clock of the LTC1063 can be overridden by an external clock provided that the external clock source can drive the timing capacitor, C, which is connected from the clock input pin to ground.

Output Offset

The DC output offset of the LTC1063 is trimmed to typically less than ±1mV . The trimming is done at V_S = ±5V. To obtain optimum DC offset performance, appropriate PC layout techniques should be used and the filter IC should be soldered to the PC board. A socket will degrade the output DC offset by typically 1mV. The output DC offset is sensitive to the coupling of the clock output pin 4 (N package) to the negative power supply pin 3 (N package). The negative supply pin should be well decoupled. When the surface mount package is used, all the unused pins should be grounded.

When the power supplies are fixed, the output DC offset should not change by more than ±100µV over 10Hz to 1MHz clock frequency variation. When the filter clock frequency is fixed, the output DC offset will typically change by −4mV (2mV) when the power supply varies from ±5V to ±7.5V (±2.5V). See Typical Performance Characteristics.

Common-Mode Rejection Ratio

The common-mode rejection ratio is defined as the change of the output DC offset with respect to the DC change of the input voltage applied to the filter.

$$CMRR = 20\log(\Delta V_{OS\ OUT}/\Delta V_{IN})(dB)$$

Table 3 illustrates the common-mode rejection for three power supplies and three temperatures. The common-mode rejection improves if the output offset is adjusted to approximately 0V. The output offset can be adjusted via pin 8 (N package) (see Typical Applications).

Table 3. CMRR Data, f_{CLK} = 100kHz

POWER SUPPLY	ΔV_{IN}	−40°C	25°C	85°C	25°C (V_{OS} Nulled)
±2.5V	±1.8V	76dB	78dB	76dB	85dB
±5V	±4V	74dB	79dB	75dB	82dB
±7.5V	±6V	70dB	72dB	74dB	76dB

The above data is valid for clock frequencies up to 800kHz, 900kHz, 1MHz, for V_S = ±2.5V, ±5V, ±7.5V respectively.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics which are present at the filter's output pin. The clock feedthrough is tested with the filter input grounded and it depends on the quality of the PC board layout and power supply decoupling. Any parasitic switching transients, during the rise and fall of the incoming clock, are not part of the clock feedthrough specifications; their amplitude strongly depends on scope probing techniques as well as ground quality and power supply bypassing. For a power supply V_S = ±5V, the clock feedthrough of the LTC1063 is 50µV_{RMS}; for V_S = ±7.5V, the clock feedthrough approaches 75µV_{RMS}. Figure 8 shows a typical scope photo of the LTC1063 output pin when the input pin is grounded. The filter cutoff frequency was 1kHz, while scope bandwidth was chosen to be 1MHz such as switching transients above the 100kHz clock frequency will show.

Wideband Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise data is used to determine the operating signal-to-

APPLICATIONS INFORMATION

noise ratio at a given distortion level. The wideband noise (μV_{RMS}) is nearly independent of the value of the clock frequency and excludes the clock feedthrough. The LTC1063's typical wideband noise is $95\mu V_{RMS}$. Figure 9 shows the same scope photo as Figure 8 but with a more sensitive vertical scale: The clock feedthrough is imbedded in the filter's wideband noise. The peak-to-peak wideband noise of the filter can be clearly seen; it is approximately $500\mu V_{P-P}$. Note that $500\mu V_{P-P}$ equals the $95\mu V_{RMS}$ wideband noise of the part, multiplied by a crest factor or 5.25.

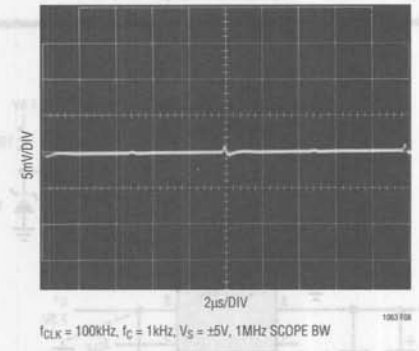


Figure 8. LTC1063 Output Clock Feedthrough + Noise

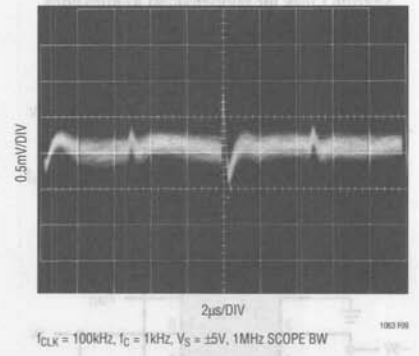


Figure 9. LTC1063 Output Clock Feedthrough + Noise

Aliasing

Aliasing is an inherent phenomenon of sampled data filters and it primarily occurs when the frequency of an input signal approaches the sampling frequency. For the LTC1063, an input signal whose frequency is in the range of f_{CLK} ±6% will generate an alias signal into the filter's passband and stopband. Table 4 shows details.

Example: LTC1063, f_{CLK} = 20kHz, f_C = 200kHz,
f_{IN} = (19.6kHz, $100mV_{RMS}$)
f_{ALIAS} = (400Hz, $3.16mV_{RMS}$)

An input RC can be used to attenuate incoming signals close to the filter clock frequency (Figure 10). A Butterworth passband response will be maintained if the value of the input resistor follows Table 1.

Table 4. Aliasing Data

INPUT FREQUENCY	OUTPUT FREQUENCY	OUTPUT AMPLITUDE REFERENCED TO INPUT SIGNAL
$0.9995f_{CLK}$	$0.0005f_{CLK}$	0 dB
$0.995f_{CLK}$	$0.005f_{CLK}$	0 dB
$0.99f_{CLK}$	$0.01f_{CLK}$	−3 dB
$0.9875f_{CLK}$	$0.0125f_{CLK}$	−10.2 dB
$0.985f_{CLK}$	$0.015f_{CLK}$	−17.7 dB
$0.9825f_{CLK}$	$0.0175f_{CLK}$	−24.3 dB
$0.98f_{CLK}$	$0.02f_{CLK}$	−30 dB
$0.975f_{CLK}$	$0.025f_{CLK}$	−40 dB
$0.97f_{CLK}$	$0.03f_{CLK}$	−48 dB
$0.965f_{CLK}$	$0.035f_{CLK}$	−54.5 dB
$0.96f_{CLK}$	$0.04f_{CLK}$	−60.4 dB
$0.955f_{CLK}$	$0.045f_{CLK}$	−65.5 dB
$0.95f_{CLK}$	$0.05f_{CLK}$	−70.16 dB
$0.94f_{CLK}$	$0.06f_{CLK}$	−78.25 dB
$0.93f_{CLK}$	$0.07f_{CLK}$	−85.3 dB
$0.9f_{CLK}$	$0.1f_{CLK}$	−100.3 dB

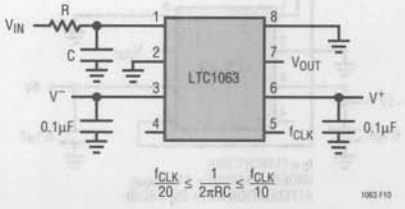


Figure 10. Adding an Input Anti-Aliasing RC

8

APPLICATIONS INFORMATION

Group Delay

The group delay of the LTC1063 closely approximates the delay of an ideal 5-pole Butterworth lowpass filter (Figure 11, Curve A). To linearize the group delay of the LTC1063 (Figure 11, Curve B), use an input resistor about six times higher than the maximum value of R_{IN}, shown in Table 1. The passband response of the group delay corrected filter approximates a 5-pole Bessel response while its transition band rolls off like a Butterworth.

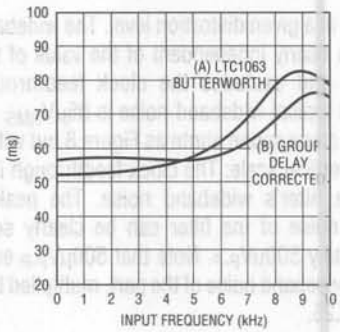
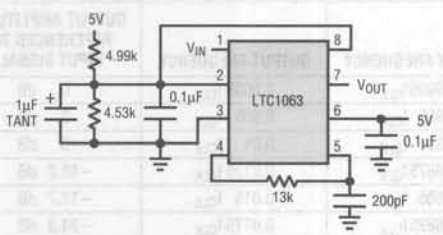


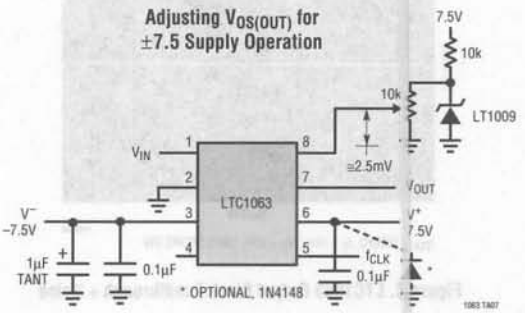
Figure 11. Group Delay

TYPICAL APPLICATIONS

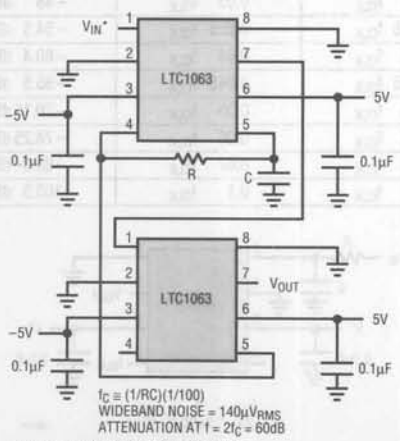
Single 5V Supply Operation (f_C = 3.4kHz)



Adjusting $V_{OS(OUT)}$ for ±7.5 Supply Operation

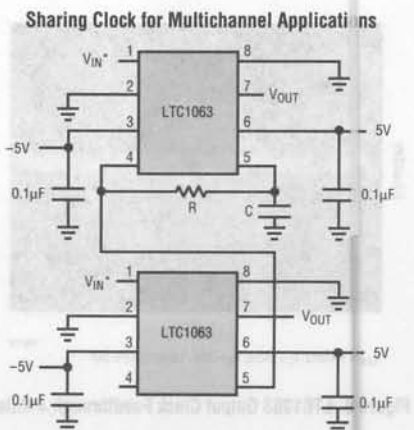


Cascading Two LTC1063s for Steeper Roll-Off



* IF THE INPUT VOLTAGE CAN EXCEED V⁺, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V⁺.

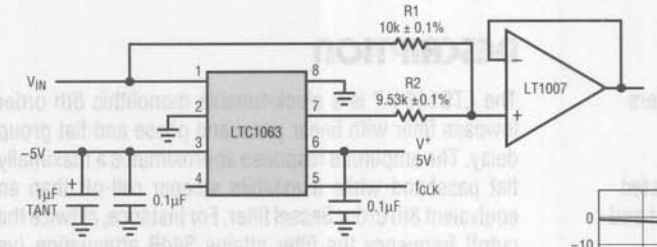
Sharing Clock for Multichannel Applications



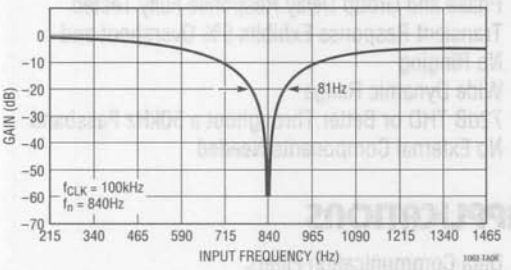
* IF THE INPUT VOLTAGE CAN EXCEED V⁺, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V⁺.

TYPICAL APPLICATIONS

Low Noise DC Accurate Clock-Tunable Notch



- $f_{NOTCH} = \frac{f_{CLK}}{119.04}$
- NOTCH DEPTH > 50dB
- OUPUT DC OFFSET = $\frac{(LTC1063)V_{OS}}{2} \cong 500\mu V$
- OUTPUT NOISE = $50\mu V_{RMS}$
- $\frac{f_{NOTCH}}{f(-20dB)BW} = \frac{10.4}{1}$



8

Linear Phase, 8th Order Lowpass Filter

FEATURES

- Steeper Roll-Off Than 8th Order Bessel Filters
- f_{CUTOFF} up to 100kHz
- Phase Equalized Filter in 14-Pin Package
- Phase and Group Delay Response Fully Tested
- Transient Response Exhibits 5% Overshoot and No Ringing
- Wide Dynamic Range
- 72dB THD or Better Throughout a 50kHz Passband
- No External Components Needed

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase-Matched Filters

DESCRIPTION

The LTC1064-7 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband while it exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 34dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency the filter attains 68dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1064-7 is tuned via an external TTL or CMOS clock.

The LTC1064-7 features wide dynamic range. With single 5V supply, the S/N + THD is 76dB. Optimum 92dB S/N is obtained with ±7.5V supplies.

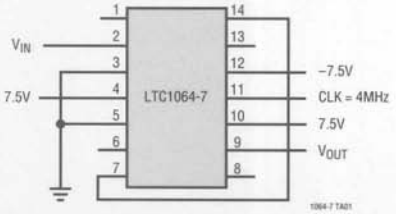
The clock-to-cutoff frequency ratio of the LTC1064-7 can be set to 50:1 (pin 10 to V^+) or 100:1 (pin 10 to V^-).

When the filter operates at clock-to-cutoff frequency ratio of 50:1, the input is double-sampled to lower the risk of aliasing.

The LTC1064-7 is pin-compatible with the LTC1064-X series, LTC1164-7 and LTC1264-7.

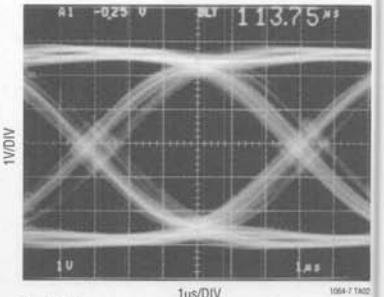
TYPICAL APPLICATION

80kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

Eye Diagram



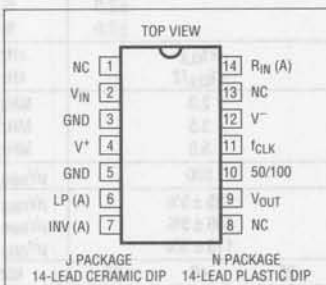
V_S = ±7.5V
f_{CLK} = 4MHz
RATIO = 50:1

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16V
Power Dissipation 400mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1064-7C ..... –40°C to 85°C
LTC1064-7M ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

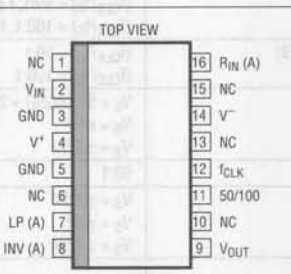


J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER
LTC1064-7CN LTC1064-7CJ LTC1064-7MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1064-7CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 10kHz or 20kHz, f_{CLK} = 1MHz, TTL or CMOS level (maximum clock rise and fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF}					
	f_{TEST} = 5kHz, (f_{CLK}/f_C) = 50:1	●	–0.60	0.10	0.65	dB
Gain at 0.5 f_{CUTOFF} (Note 4)	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 50:1	●	–0.90	–0.35	0.15	dB
	f_{TEST} = 5kHz, (f_{CLK}/f_C) = 100:1	●	–1.30	–0.35	1.25	dB
Gain at 0.75 f_{CUTOFF} (Note 1)	f_{TEST} = 15kHz, (f_{CLK}/f_C) = 50:1	●	–2.0	–1.0	–0.35	dB
Gain at f_{CUTOFF}	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 50:1	●	–4.50	–3.4	–2.50	dB
	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 100:1	●	–5.75	–4.5	–3.75	dB
Gain at 2 f_{CUTOFF}	f_{TEST} = 40kHz, (f_{CLK}/f_C) = 50:1	●	–36.5	–34.0	–31.75	dB
	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 100:1	●	–37.0	–34.5	–31.75	dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 100:1		–6.5	–4.3	–3.5	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1		–0.9	–0.3	0.25	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1		–4.5	–3.3	–2.00	dB
Phase Factor (F) Phase = 180° – F (f/f_C) (Note 1)	0.1Hz ≤ f ≤ f_{CUTOFF}					
	(f_{CLK}/f_C) = 50:1			430 ± 2.0		Deg
	(f_{CLK}/f_C) = 100:1			421 ± 2.5		Deg
	(f_{CLK}/f_C) = 50:1	●	422	430	437	Deg
	(f_{CLK}/f_C) = 100:1	●	414	421	429	Deg
Phase Nonlinearity (Notes 1, 3)	(f_{CLK}/f_C) = 50:1			±1.0		%
	(f_{CLK}/f_C) = 100:1			±1.0		%
	(f_{CLK}/f_C) = 50:1	●			±2.0	%
	(f_{CLK}/f_C) = 100:1	●			±2.0	%

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ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $R_L = 10k$, $T_A = 25°C$, $f_{CUTOFF} = 10kHz$ or $20kHz$, $f_{CLK} = 1MHz$, TTL or CMOS level (maximum clock rise and fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay (t_d) $t_d = (F/360)(1/f_C)$ (Note 2)	$(f_{CLK}/f_C) = 50:1$, $f \le f_{CUTOFF}$			59.7 ± 0.5		µs
	$(f_{CLK}/f_C) = 100:1$, $f \le f_{CUTOFF}$			117.0 ± 1.0		µs
	$(f_{CLK}/f_C) = 50:1$, $f \le f_{CUTOFF}$	●	58.6	59.7	60.7	µs
	$(f_{CLK}/f_C) = 100:1$, $f \le f_{CUTOFF}$	●	115.0	117.0	119.0	µs
Group Delay Deviation (Notes 2, 3)	$(f_{CLK}/f_C) = 50:1$, $f \le f_{CUTOFF}$			±1.0		%
	$(f_{CLK}/f_C) = 100:1$, $f \le f_{CUTOFF}$			±1.0		%
	$(f_{CLK}/f_C) = 50:1$, $f \le f_{CUTOFF}$	●			±2.0	%
	$(f_{CLK}/f_C) = 100:1$, $f \le f_{CUTOFF}$	●			±2.0	%
Input Frequency Range (Table 9)	$(f_{CLK}/f_C) = 50:1$			$<f_{CLK}$		kHz
	$(f_{CLK}/f_C) = 100:1$			$<f_{CLK}/2$		kHz
Maximum f_{CLK}	$V_S = 5V$ (AGND = 2V)			2.0		MHz
	$V_S = \pm 5V$			3.5		MHz
	$V_S = \pm 7.5V$			5.0		MHz
Clock Feedthrough ($f \ge f_{CLK}$)	50:1			200		μV_{RMS}
Wideband Noise ($1Hz \le f \le f_{CLK}$)	$V_S = \pm 2.5V$			95 ± 5%		μV_{RMS}
	$V_S = \pm 5V$			105 ± 5%		μV_{RMS}
	$V_S = \pm 7.5V$			115 ± 5%		μV_{RMS}
Input Impedance			25	40	70	kΩ
Output DC Voltage Swing (Note 5)	$V_S = \pm 2.375V$		±1.0	±1.2		V
	$V_S = \pm 5V$	●	±2.1	±3.2		V
	$V_S = \pm 7.5V$	●	±3.0	±5.0		V
Output DC Offset	50:1, $V_S = \pm 5V$			±150	±220	mV
	100:1, $V_S = \pm 5V$			±150		mV
Output DC Offset TempCo	50:1, $V_S = \pm 5V$			±200		µV/°C
	100:1, $V_S = \pm 5V$			±200		µV/°C
Power Supply Current	$V_S = \pm 2.375V$, $T_A = 25°C$			11	22	mA
		●			22	mA
	$V_S = \pm 5V$, $T_A = 25°C$			14	25	mA
		●			30	mA
	$V_S = \pm 7.5V$, $T_A = 25°C$			17	30	mA
		●			35	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as $f \le f_C$; f_C = cutoff frequency.

Figure 1 curve shows the typical phase response of an LTC1064-7 operating at f_{CLK} = 1MHz, ratio = 50:1, f_C = 20kHz and it closely matches an ideal straight line. The phase shift is described by: phase shift = $180° - F(f/f_C)$; $f \le f_C$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor allows the calculation of the phase at a given frequency. Example: The phase shift at 14kHz of the LTC1064-7 shown in Figure 1 is:

phase shift = 180° – 430° (14kHz/20kHz) ± nonlinearity = –121° ± 1% or –121° ± 1.20°.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: Phase deviation and group delay deviation for LTC1064-7MJ is ±4%.

Note 4: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 5: The AC swing is typically $11V_{P-P}$, $7V_{P-P}$, $2.8V_{P-P}$, with ±7.5V, ±5V, ±2.5V Supply respectively. For more information refer to the THD + Noise vs Input graphs.

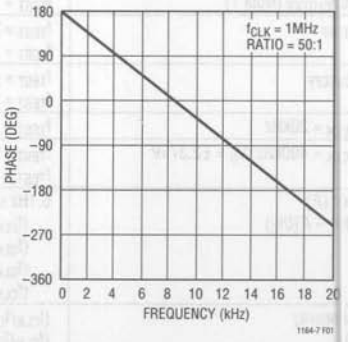
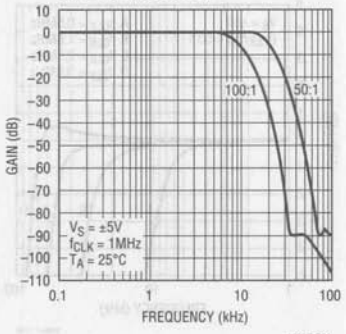


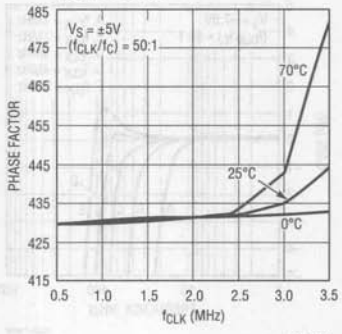
Figure 1. Phase Response in the Passband (Note 1)

TYPICAL PERFORMANCE CHARACTERISTICS

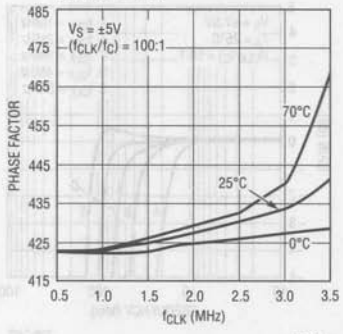
Gain vs Frequency



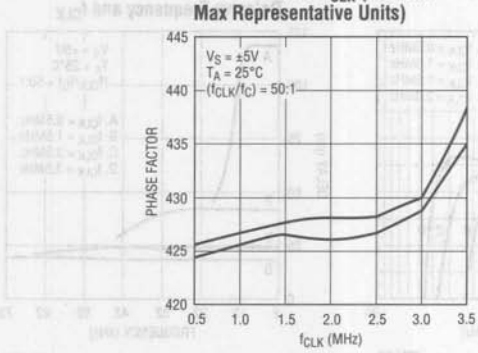
Phase Factor vs f_{CLK} (Typical Unit)



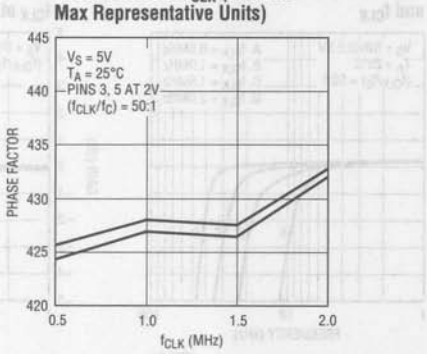
Phase Factor vs f_{CLK} (Typical Unit)



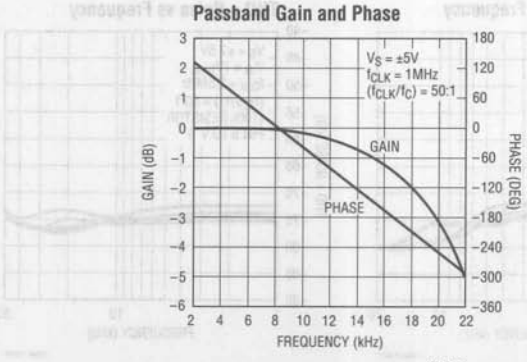
Phase Factor vs f_{CLK} (Min and Max Representative Units)



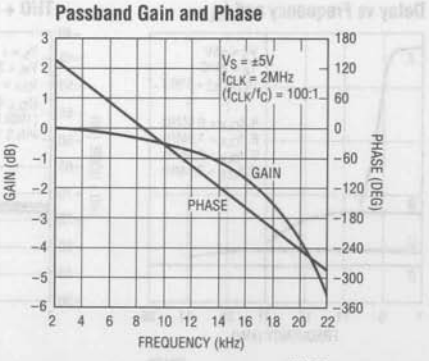
Phase Factor vs f_{CLK} (Min and Max Representative Units)



Passband Gain and Phase



Passband Gain and Phase



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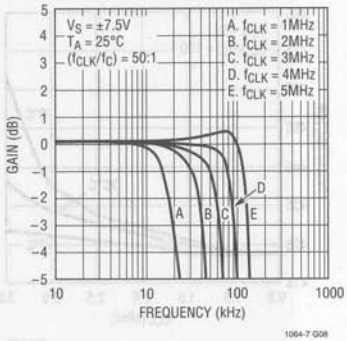
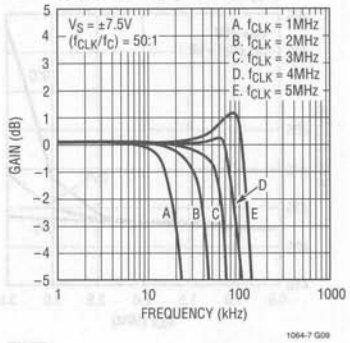
TYPICAL PERFORMANCE CHARACTERISTICS

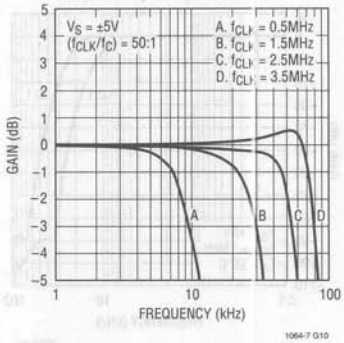
Passband Gain vs Frequency and f_{CLK}



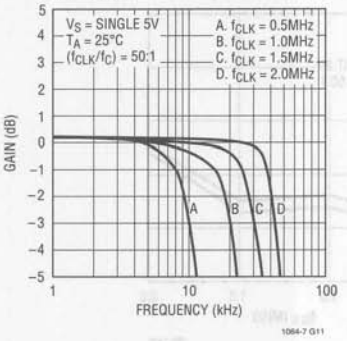
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



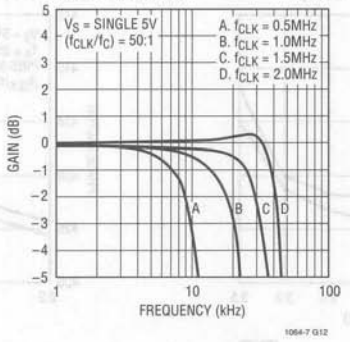
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



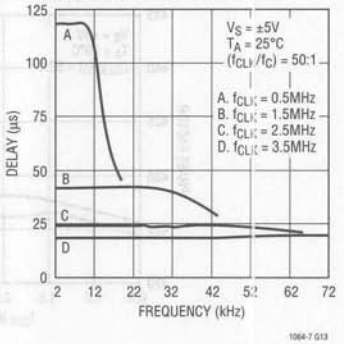
Passband Gain vs Frequency and f_{CLK}



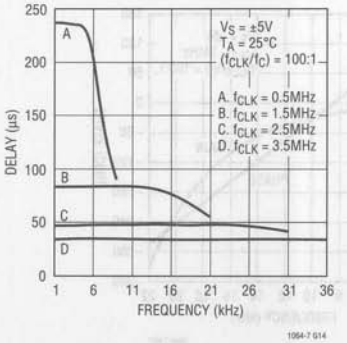
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



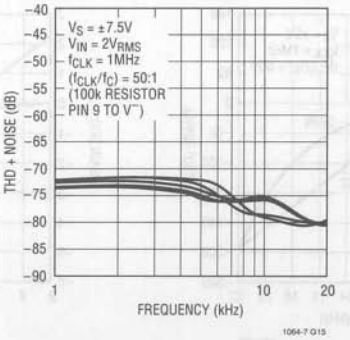
Delay vs Frequency and f_{CLK}



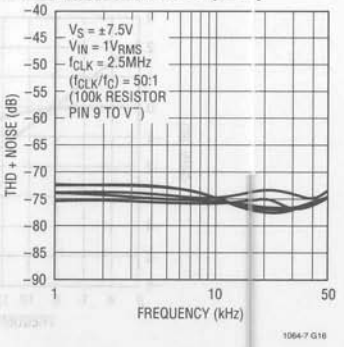
Delay vs Frequency and f_{CLK}



THD + Noise vs Frequency

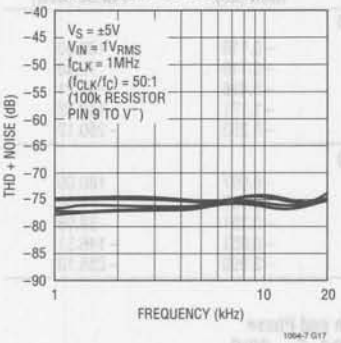


THD + Noise vs Frequency

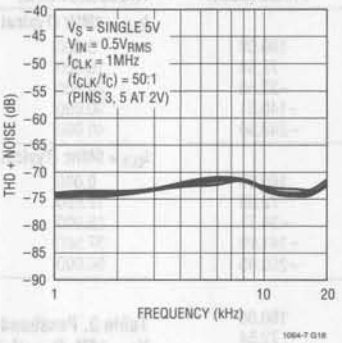


TYPICAL PERFORMANCE CHARACTERISTICS

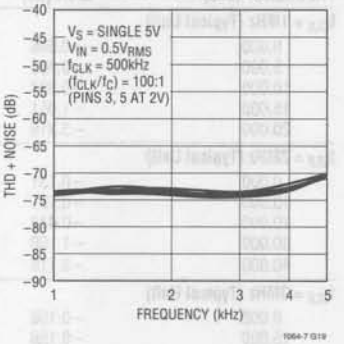
THD + Noise vs Frequency



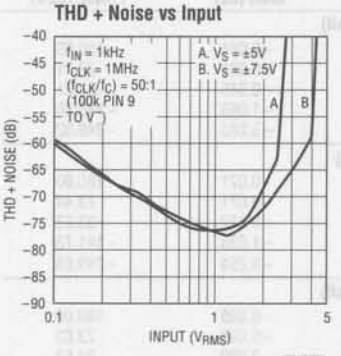
THD + Noise vs Frequency



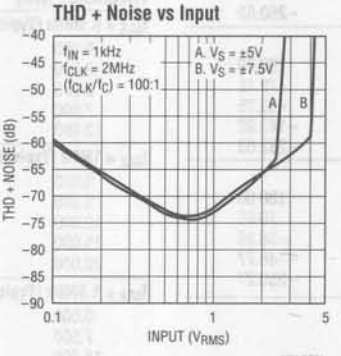
THD + Noise vs Frequency



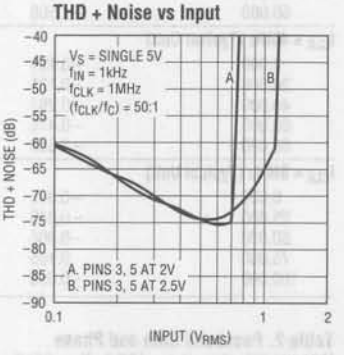
THD + Noise vs Input



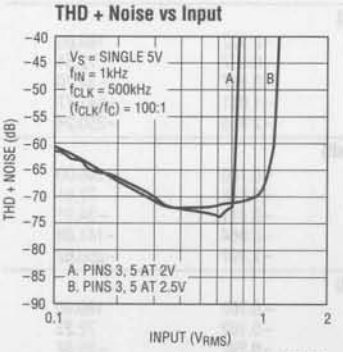
THD + Noise vs Input



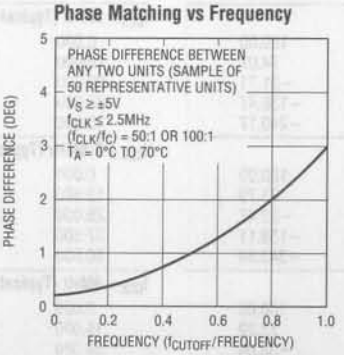
THD + Noise vs Input



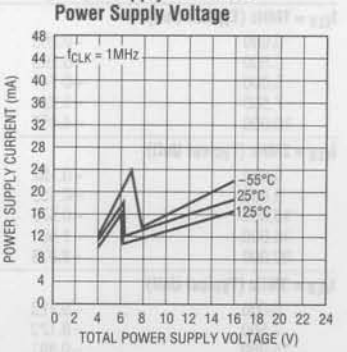
THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage



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TYPICAL PERFORMANCE CHARACTERISTICS

Table 1. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.086	180.00
5.000	−0.086	73.54
10.000	−0.334	−33.60
15.000	−1.051	−140.81
20.000	−3.316	−249.30
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.131	180.00
10.000	−0.131	72.88
20.000	−0.442	−34.71
30.000	−1.108	−141.99
40.000	−3.115	−250.45
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.156	180.00
15.000	−0.156	72.54
30.000	−0.459	−35.01
45.000	−0.941	−141.95
60.000	−2.508	−250.53
f_{CLK} = 4MHz (Typical Unit)		
0.000	−0.121	180.00
20.000	−0.121	72.12
40.000	−0.292	−35.75
60.000	−0.476	−142.92
80.000	−1.539	−252.63
f_{CLK} = 5MHz (Typical Unit)		
0.000	−0.045	180.00
25.000	−0.045	70.85
50.000	−0.006	−38.25
75.000	0.185	−146.77
100.000	−0.356	−259.27

Table 2. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 100:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.203	180.00
2.500	−0.203	74.07
5.000	−0.741	−31.71
7.500	−1.831	−136.47
10.000	−4.451	−240.17
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.152	180.00
5.000	−0.152	73.79
10.000	−0.575	−32.47
15.000	−1.501	−138.11
20.000	−3.973	−243.84
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.123	180.00
7.500	−0.123	73.32
15.000	−0.481	−33.64
22.500	−1.312	−140.14
30.000	−3.654	−247.11
f_{CLK} = 4MHz (Typical Unit)		
0.000	−0.116	180.00
10.000	−0.116	72.49
20.000	−0.436	−35.21
30.000	−1.171	−142.33
40.000	−3.353	−250.12
f_{CLK} = 5MHz (Typical Unit)		
0.000	−0.097	180.00
12.500	−0.097	71.00
25.000	−0.351	−38.08
37.500	−0.951	−146.51
50.000	−2.999	−256.13

Table 3. Passband Gain and Phase
$V_S = \pm 5V$, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	−0.081	180.00
2.500	−0.081	73.71
5.000	−0.345	−33.31
7.500	−1.063	−140.36
10.000	−3.283	−248.52
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.071	180.00
5.000	−0.071	73.44
10.000	−0.322	−33.83
15.000	−1.036	−141.13
20.000	−3.284	−249.68
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	−0.095	180.00
7.500	−0.095	73.03
15.000	−0.392	−34.53
22.500	−1.075	−141.89
30.000	−3.155	−250.45
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.127	180.00
10.000	−0.127	72.81
20.000	−0.447	−34.70
30.000	−1.041	−141.77
40.000	−2.856	−250.24
f_{CLK} = 2.5MHz (Typical Unit)		
0.000	−0.126	180.00
12.500	−0.126	72.61
25.000	−0.411	−34.91
37.500	−0.864	−141.88
50.000	−2.397	−250.62
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.102	180.00
15.000	−0.102	72.23
30.000	−0.292	−35.64
45.000	−0.546	−142.96
60.000	−1.769	−252.73

TYPICAL PERFORMANCE CHARACTERISTICS

Table 3. Passband Gain and Phase
$V_S = \pm 5V$, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 3.5MHz (Typical Unit)		
0.000	−0.054	180.00
17.500	−0.054	71.07
35.000	−0.108	−38.00
52.500	−0.137	−146.68
70.000	−1.104	−258.97

Table 4. Passband Gain and Phase
$V_S = \pm 5V$, $(f_{CLK}/f_C) = 100:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	−0.186	180.00
1.250	−0.186	74.10
2.500	−0.726	−31.65
3.750	−1.805	−136.48
5.000	−4.402	−240.33
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.184	180.00
2.500	−0.184	74.02
5.000	−0.712	−31.80
7.500	−1.785	−136.61
10.000	−4.387	−240.43
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	−0.145	180.00
3.750	−0.145	73.84
7.500	−0.596	−32.32
11.250	−1.556	−137.73
15.000	−4.047	−242.95
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.116	180.00
5.000	−0.116	73.64
10.000	−0.494	−32.93
15.000	−1.361	−139.03
20.000	−3.761	−245.57
f_{CLK} = 2.5MHz (Typical Unit)		
0.000	−0.101	180.00
6.250	−0.101	73.17
12.500	−0.452	−33.93
18.750	−1.273	−140.58
25.000	−3.611	−247.80
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.105	180.00
7.500	−0.105	72.36
15.000	−0.445	−35.47
22.500	−1.228	−142.70
30.000	−3.509	−250.58
f_{CLK} = 3.5MHzMHz (Typical Unit)		
0.000	−0.104	180.00
8.750	−0.104	70.81
17.500	−0.437	−38.39
26.250	−1.188	−146.85
35.000	−3.478	−256.10

Table 5. Passband Gain and Phase
V_S = Single 5V, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	−0.134	180.00
2.500	−0.134	73.52
5.000	−0.391	−33.67
7.500	−1.109	−140.92
10.000	−3.351	−249.32
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.148	180.00
5.000	−0.148	73.07
10.000	−0.423	−34.63
15.000	−1.111	−142.25
20.000	−3.241	−251.03
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	−0.157	180.00
7.500	−0.157	72.73
15.000	−0.456	−34.83
22.500	−0.981	−142.08
30.000	−2.687	−251.09
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.188	180.00
10.000	−0.188	71.37
20.000	−0.304	−37.52
30.000	−0.513	−146.11
40.000	−1.824	−257.46

Table 6. Passband Gain and Phase
V_S = Single 5V, $(f_{CLK}/f_C) = 100:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	−0.243	180.00
1.250	−0.243	73.91
2.500	−0.776	−31.98
3.750	−1.861	−136.98
5.000	−4.483	−240.90
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.208	180.00
2.500	−0.208	73.76
5.000	−0.678	−32.47
7.500	−1.679	−137.87
10.000	−4.221	−242.65
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	−0.115	180.00
3.750	−0.115	73.26
7.500	−0.473	−33.73
11.250	−1.314	−140.40
15.000	−3.715	−247.66
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.209	180.00
5.000	−0.209	71.18
10.000	−0.499	−37.85
15.000	−1.281	−146.27
20.000	−3.695	−255.38

8

PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

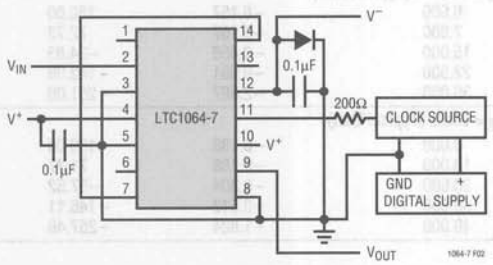


Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

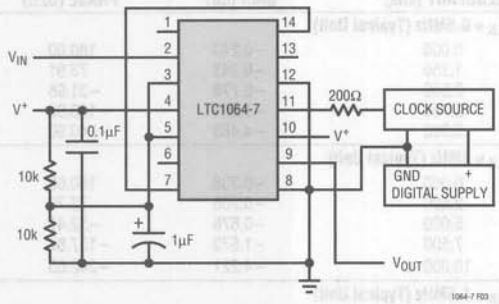


Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.1µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ −2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Suppl = 5V	≥ 1.45V	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 3 should be connected to the analog ground plane. For single supply operation pin 3 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, pin 3 should be biased at 2V. This minimizes passband gain and phase variations.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and pin 10 at V^- gives a 100:1 ratio. For single supply operation the ratio is 50:1 when pin 10 is at V^+ and 100:1 when pin 10 is at ground. When pin 10 is not tied to ground, it should be bypassed to analog ground

PIN FUNCTIONS

with a 0.1μF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/μs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 40k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pins (1, 5, 8, 13)

Pins 1, 5, 8 and 13 are not connected to any internal circuit point on the device and should preferably be tied to analog ground.

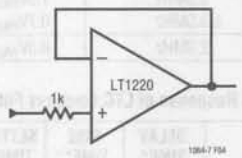


Figure 4. Buffer for Filter Output

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	50:1	100:1
Single 5V	$90\mu V_{RMS}$	$100\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$300\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$650\mu V_{RMS}$

Note: The clock feedthrough at single 5V is imbedded in the wideband noise of the filter. Clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1064-7 wideband noise at ±5V supply is $105\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

8

APPLICATIONS INFORMATION

Speed Limitations

To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN} vs V_S and Clock

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	5.0MHz	$1.8V_{RMS}$ (f_{IN} > 80kHz)
	4.5MHz	$2.3V_{RMS}$ (f_{IN} > 80kHz)
	4.0MHz	$2.7V_{RMS}$ (f_{IN} > 80kHz)
	≥3.5MHz	$1.4V_{RMS}$ (f_{IN} > 500kHz)
±5V	3.5MHz	$1.6V_{RMS}$ (f_{IN} > 80kHz)
	≥3.0MHz	$0.7V_{RMS}$ (f_{IN} > 400kHz)
Single 5V	2.0MHz	$0.5V_{RMS}$ (f_{IN} > 250kHz)

Table 10. Transient Response of LTC Lowpass Filters

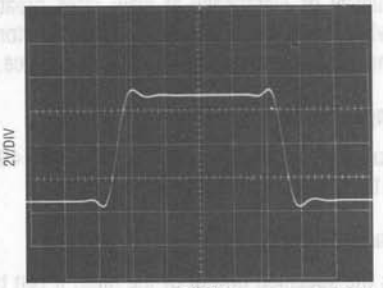
LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.2/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.2/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.4/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.3/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.5/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.5/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

Table 11. Aliasing (f_{CLK} = 100kHz)

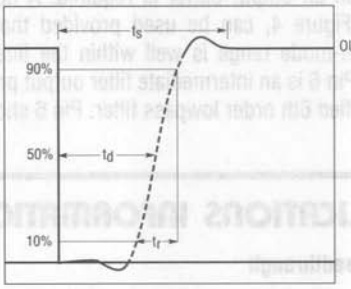
INPUT FREQUENCY (V_{IN} = $1V_{RMS}$, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = $1V_{RMS}$) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
50:1, f_{CUTOFF} = 2kHz		
190 (or 210)	–76.1	10.0
195 (or 205)	–51.9	5.0
196 (or 204)	–36.3	4.0
197 (or 203)	–18.4	3.0
198 (or 202)	–3.0	2.0
199.5 (or 200.5)	–0.2	0.5
100:1, f_{CUTOFF} = 1kHz		
97 (or 103)	–74.2	3.0
97.5 (or 102.5)	–53.2	2.5
98 (or 102)	–36.9	2.0
98.5 (or 101.5)	–19.6	1.5
99 (or 101)	–5.2	1.0
99.5 (or 100.5)	–0.7	0.5

Transient Response



V_S = ±7.5V, f_{IN} = 2kHz ±3V
f_{CLK} = 1MHz, RATIO = 50:1

Figure 5.



RISE TIME (t_r) = $\frac{0.39}{f_{CUTOFF}}$ ±5%

SETTLING TIME (t_s) = $\frac{2.2}{f_{CUTOFF}}$ ±5%
(TO 1% of OUTPUT)

DELAY TIME (t_d) = GROUP DELAY = $\frac{1.2}{f_{CUTOFF}}$
(TO 50% OF OUTPUT)

1064-7 F06

Figure 6.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1064-7 case at 100:1, an input signal whose frequency is in the range of f_{CLK}±3%, will be aliased back into the filter's passband. If, for instance, an LTC1064-7 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz, 10mV input signal, a 2kHz, 143µV_{RMS} alias signal will appear at its output. When the LTC1064-7 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 11 shows details.

DC Accurate, Clock-Tunable Linear Phase 5th Order Bessel Lowpass Filter

FEATURES

- Clock-Tunable Cutoff Frequency
- 1mV DC Offset (Typical)
- 80dB CMR (Typical)
- Internal or External Clock
- $50\mu V_{RMS}$ Clock Feedthrough
- 100:1 Clock-to-Cutoff Frequency Ratio
- $80\mu V_{RMS}$ Total Wideband Noise
- 0.004% Noise + THD at $2V_{RMS}$ Output Level
- 50kHz Maximum Cutoff Frequency
- Cascadable for Faster Roll-Off
- Operates from ±2.375V to ±8V Power Supplies
- Self-Clocking with 1 RC

APPLICATIONS

- Audio
- Strain Gauge Amplifiers
- Anti-Aliasing Filters
- Low Level Filtering
- Digital Voltmeters
- Smoothing Filters
- Reconstruction Filters

DESCRIPTION

The LTC1065 is the first monolithic filter providing both clock-tunability with low DC output offset and over 12-bit DC accuracy. The frequency response of the LTC1065 closely approximates a 5th order Bessel polynomial. With appropriate PCB layout techniques the output DC offset is typically 1mV and is constant over a wide range of clock frequencies. With ±5V supplies and ±4V input voltage range, the CMR of the device is typically 80dB.

The filter cutoff frequency is controlled either by an internal or external clock. The clock-to-cutoff frequency ratio is 100 : 1. The on-board clock is nearly power supply independent and it is programmed via an external RC. The $50\mu V_{RMS}$ clock feedthrough of the device is considerably lower than other existing monolithic filters.

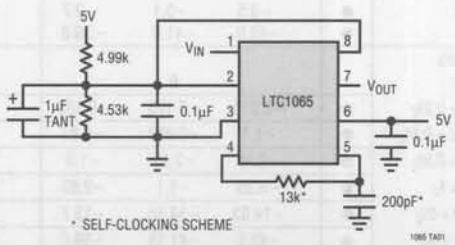
The LTC1065 wideband noise is $80\mu V_{RMS}$ and it can process large AC input signals with low distortion. With ±7.5V supplies, for instance, the filter handles up to $4V_{RMS}$ (94dB S/N ratio) while the standard 1kHz THD is below 0.005%; 87dB dynamic range (S/N + THD) is obtained with input levels between $2V_{RMS}$ and $2.5V_{RMS}$.

The LTC1065 is available in 8-pin miniDIP and 16-pin SOL. For a Butterworth response, see LTC1063 data sheet. The LTC1065 is pin compatible with the LTC1063.

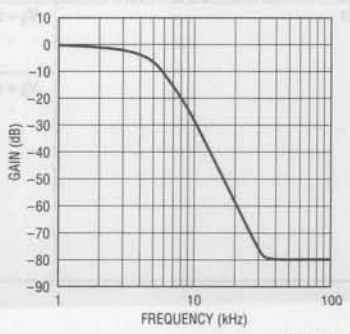
8

TYPICAL APPLICATION

3.4kHz Single 5V Supply Bessel Lowpass Filter



Frequency Response

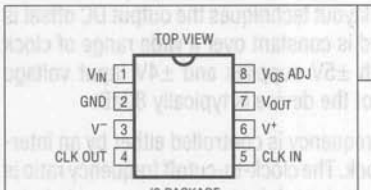


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Voltage at Any Input .... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Burn-In Voltage 16V
Storage Temperature Range ..... −65°C to 150°C

Operating Temperature Range
LTC1065C ..... −40°C to 85°C
LTC1065M ..... −55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

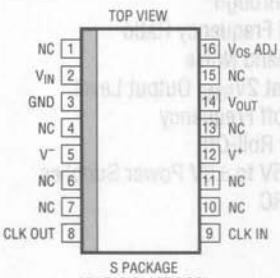


J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER

LTC1065CN8
LTC1065MJ8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 100°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1065CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Cutoff Frequency Ratio (f_{CLK}/f_C)	±2.375V ≤ V_S ≤ ±7.5V			100±0.5		
Maximum Clock Frequency (Note 1)	V_S = ±7.5V			5		MHz
	V_S = ±5V			4		MHz
	V_S = ±2.5V			3		MHz
Minimum Clock Frequency (Note 2)	±2.5V ≤ V_S ≤ ±7.5V, T_A < 85°C			30		Hz
Input Frequency Range			0		0.9f_{CLK}	
Filter Gain	V_S = ±5V, f_{CLK} = 25kHz, f_C = 250Hz					
	f_{IN} = 250Hz	●	−3.5	−3.1	−2.7	dB
	f_{IN} = 1kHz	●	−43.0	−41.0	−39.0	dB
	V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz					
	f_{IN} = 100Hz			0		dB
	f_{IN} = 1kHz = 0.2f_C	●	−0.215	−0.175	−0.135	dB
	f_{IN} = 2.5kHz = 0.5f_C	●	−1.1	−0.972	−0.84	dB
	f_{IN} = 4kHz = 0.8f_C	●	−2.35	−2.13	−1.9	dB
	f_{IN} = 5kHz = f_C	●	−3.35	−3.1	−2.83	dB
	f_{IN} = 10kHz = 2f_C	●	−14.63	−14.15	−13.7	dB
	f_{IN} = 20kHz = 4f_C	●	−43.0	−41.15	−39.0	dB

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain	V_S = ±2.375V, f_{CLK} = 500kHz, f_C = 5kHz					
	f_{IN} = 1kHz	●	−0.225	−0.185	−0.145	dB
	f_{IN} = 2.5kHz	●	−1.1	−1.0	−0.83	dB
	f_{IN} = 4kHz	●	−2.35	−2.15	−1.9	dB
	f_{IN} = 5kHz	●	−3.35	−3.1	−2.83	dB
	f_{IN} = 10kHz	●	−14.63	−14.1	−13.7	dB
Clock Feedthrough	±2.375V ≤ V_S ≤ ±7.5V			50		μV_{RMS}
Wideband Noise (Note 3)	±2.375V ≤ V_S ≤ ±7.5V, 1Hz < f < f_{CLK}			80		μV_{RMS}
THD + Wideband Noise (Note 4)	V_S = ±7.5V, f_C = 20kHz, f_{IN} = 1kHz, $2V_{RMS} \le V_{IN} \le 2.5V_{RMS}$			−87		dB
Filter Output ± DC Swing	V_S = ±2.375V		1.5/−2.0	1.7/−2.2		V
		●	1.3/−1.8			V
	V_S = ±5V		4.0/−4.5	4.3/−4.8		V
		●	3.8/−4.3			V
	V_S = ±7.5V		6.5/−7.0	6.8/−7.3		V
		●	6.3/−6.8			V
Input Bias Current				10		nA
Dynamic Input Impedance				800		MΩ
Output DC Offset (Note 5)	V_S = ±2.375V			2		mV
	V_S = ±5V			0	±5	mV
	V_S = ±7.5V			−4		mV
Output DC Offset Drift	V_S = ±2.375V			10		µV/°C
	V_S = ±5V			20		µV/°C
	V_S = ±7.5V			25		µV/°C
Self-Clocking Frequency (f_{OSC})	R (Pin 4 to 5) = 20k, C (Pin 5 to GND) = 470pF					
	V_S = ±2.375V		99	103	112	kHz
	LTC1065C	●	95	103	112	kHz
	LTC1065M	●	92	100	112	kHz
	V_S = ±5V		100	106	112	kHz
	LTC1065C	●	98	106	114	kHz
	LTC1065M	●	97	105	114	khz
	V_S = ±7.5V		102	106	114	kHz
	LTC1065C	●	101	109	116	kHz
	LTC1065M	●	100	108	116	kHz
External CLK Pin Logic Thresholds	V_S = ±2.375V Min Logical "1"			1.43		V
	Max Logical "0"			0.47		V
	V_S = ±5V Min Logical "1"			3		V
	Max Logical "0"			1		V
	V_S = ±7.5V Min Logical "1"			4.5		V
	Max Logical "0"			1.5		V
Power Supply Current	V_S = ±2.375V, f_{CLK} = 500kHz			2.5	4.0	mA
	LTC1065C	●			5.5	mA
	LTC1065M	●			6.0	mA
	V_S = ±5V, f_{CLK} = 500kHz			5.5	9	mA
	LTC1065C	●			11	mA
	LTC1065M	●			12	mA
	V_S = ±7.5V, f_{CLK} = 500kHz			7.0	12.0	mA
	LTC1065C	●			14.5	mA
	LTC1065M	●			16.0	mA

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ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The maximum clock frequency is arbitrarily defined as: the frequency at which the filter AC response exhibits ≥ 1dB of gain peaking.

Note 2: At limited temperature ranges (i.e., $T_A \leq 50°C$) the minimum clock frequency can be as low as 10Hz. The typical minimum clock frequency is arbitrarily defined as: the clock frequency at which the output DC offset changes by more than 1mV.

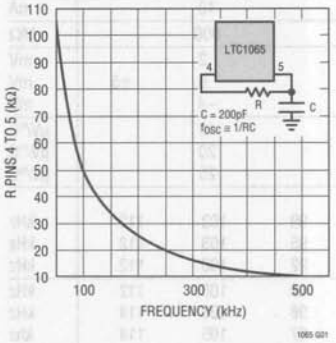
Note 3: The wideband noise specification does not include the clock feedthrough.

Note 4: To properly evaluate the filter's harmonic distortion an inverting output buffer is recommended. An output buffer (although recommended) is not necessarily needed when measuring output DC offset or wideband noise (see Figure 3).

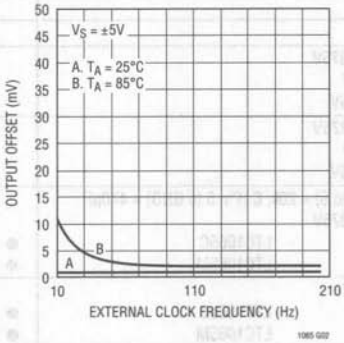
Note 5: The output DC offset is optimized for ±5V supply. The output DC offset shifts when the power supplies change; however this phenomenon is repeatable and predictable.

TYPICAL PERFORMANCE CHARACTERISTICS

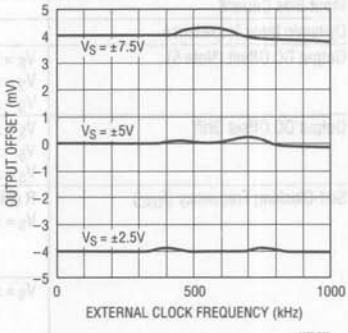
Self-Clocking Frequency vs R



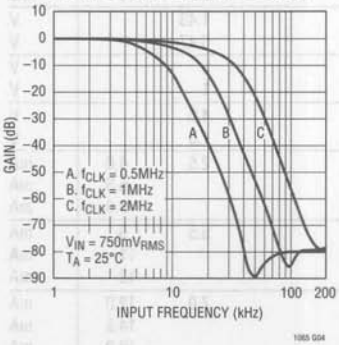
Output Offset vs Clock, Low Clock Rates



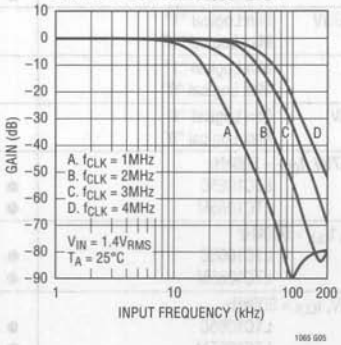
Output Offset vs Clock, Medium Clock Rates



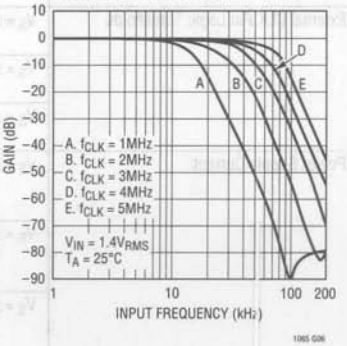
Gain vs Frequency; $V_S = \pm 2.5V$



Gain vs Frequency; $V_S = \pm 5V$

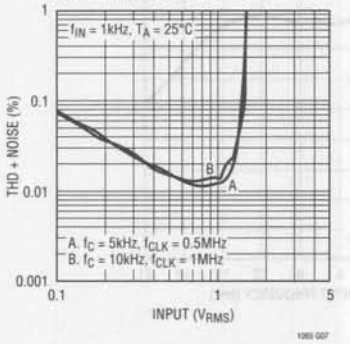


Gain vs Frequency; $V_S = \pm 7.5V$

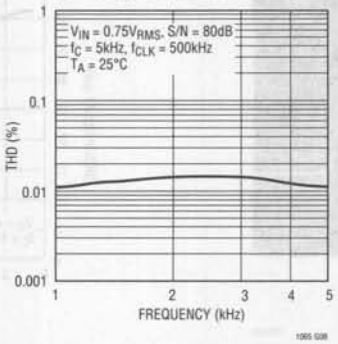


TYPICAL PERFORMANCE CHARACTERISTICS

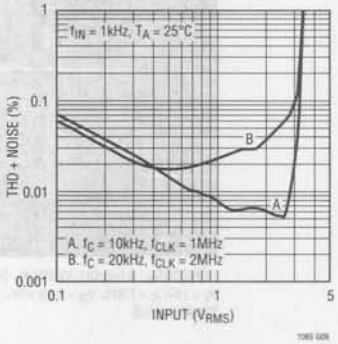
THD + Noise vs Input Voltage; V_S = Single 5V, AGND = 2V



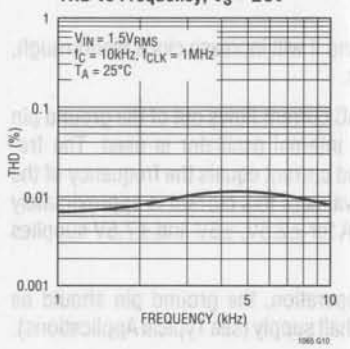
THD vs Frequency; V_S = Single 5V, AGND = 2V



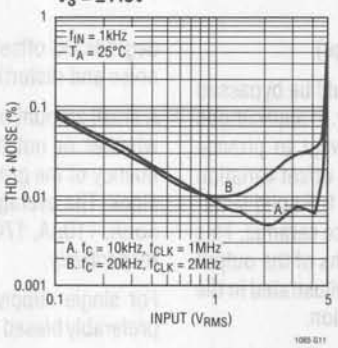
THD + Noise vs Input Voltage; V_S = ±5V



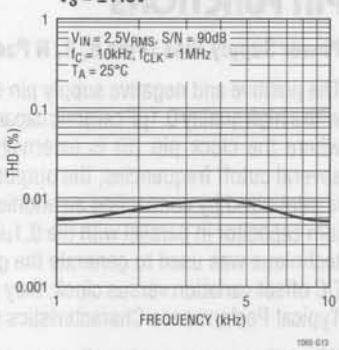
THD vs Frequency; V_S = ±5V



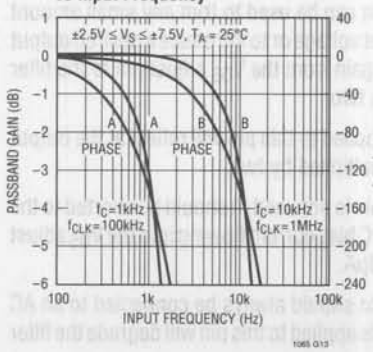
THD + Noise vs Input Voltage; V_S = ±7.5V



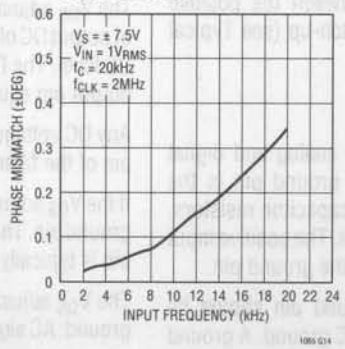
THD vs Frequency; V_S = ±7.5V



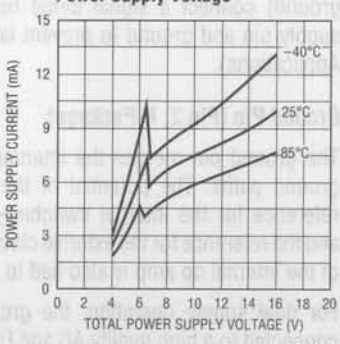
Passband Gain and Phase vs Input Frequency



Typical Phase Matching Device to Device



Power Supply Current vs Power Supply Voltage



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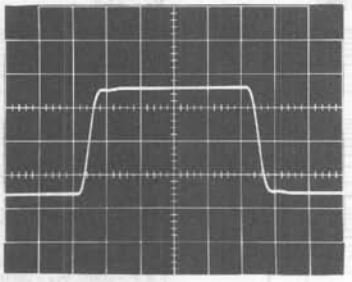
TYPICAL PERFORMANCE CHARACTERISTICS

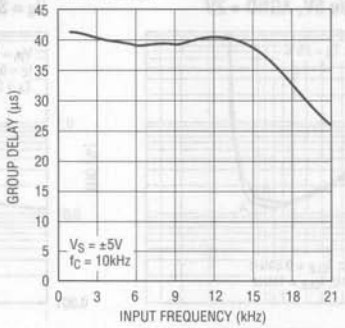
Transient Response



HORIZONTAL: 0.1ms/DIV, VERTICAL: 2V/DIV
$V_S = \pm 5V$, $f_C = 10kHz$, $V_{IN} = 1kHz \pm 3V_P$
SQUARE WAVE

1065 G16

Group Delay



1065 G17

PIN FUNCTIONS

Power Supply Pins (Pins 6, 3, N Package)

The positive and negative supply pin should be bypassed with a high quality 0.1µF ceramic capacitor. In applications where the clock pin (5) is externally swept to provide several cutoff frequencies, the output DC offset variation is minimized by connecting an additional 1µF solid tantalum capacitor in parallel with the 0.1µF disc ceramic. This technique was used to generate the graphs of the output DC offset variation versus clock; they are illustrated in the Typical Performance Characteristics section.

When the power supply voltage exceeds ±7V, and when V^- is applied before V^+ (if V^+ is allowed to go below ground) connect a signal diode between the positive supply pin and ground to prevent latch-up (see Typical Applications).

Ground Pin (Pin 2, N Package)

The ground pin merges the internal analog and digital ground paths. The potential of the ground pin is the reference for the internal switched-capacitor resistors, and the reference for the external clock. The positive input of the internal op amp is also tied to the ground pin.

For dual supply operation, the ground pin should be connected to a high quality AC and DC ground. A ground plane, if possible, should be used. A poor ground will degrade DC offset and it will increase clock feedthrough, noise and distortion.

A small amount of AC current flows out of the ground pin whether or not the internal oscillator is used. The frequency of the ground current equals the frequency of the clock. The average value of this current is approximately 55µA, 110µA, 170µA for ±2.5V, ±5V and ±7.5V supplies respectively.

For single supply operation, the ground pin should be preferably biased at half supply (see Typical Applications).

V_{OS} Adjust Pin (Pin 8, N Package)

The V_{OS} adjust pin can be used to trim any small amount of output DC offset voltage or to introduce a desired output DC level. The DC gain from the V_{OS} adjust pin to the filter output pin equals two.

Any DC voltage applied to this pin will reflect at the output pin of the filter multiplied by two.

If the V_{OS} adjust pin is not used, it should be shorted to the ground pin. The DC bias current flowing into the V_{OS} adjust pin is typically 10pA.

The V_{OS} adjust pin should always be connected to an AC ground; AC signals applied to this pin will degrade the filter response.

PIN FUNCTIONS

Input Pin (Pin 1, N Package)

Pin 1 is the filter input and it is connected to an internal switched-capacitor resistor. If the input pin is left floating, the filter output will saturate. The DC input impedance of pin 1 is very high; with ±5V supplies and 1MHz clock, the DC input impedance is typically 1GΩ. A resistor R_{IN} in series with the input pin will not alter the value of the filter's DC output offset (Figure 1). R_{IN} should however, be limited to a maximum value (Table 1), otherwise the filter's pass-band will be affected. Refer to the Applications Information section for more details.

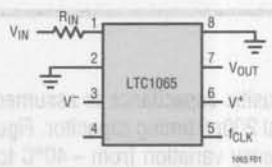


Figure 1.

Table 1. $R_{IN(MAX)}$ vs Clock and Power Supply

	$R_{IN(MAX)}$		
	$V_S = \pm 7.5V$	$V_S = \pm 5V$	$V_S = \pm 2.5V$
f_{CLK} = 4MHz	1.82k	–	–
f_{CLK} = 3MHz	3.01k	2.49k	–
f_{CLK} = 2MHz	4.32k	3.65k	2.37k
f_{CLK} = 1MHz	9.09k	8.25k	7.5k
f_{CLK} = 500kHz	17.8k	16.9k	16.9k
f_{CLK} = 100kHz	95.3k	90.9k	90.9k

Output Pin (Pin 7, N Package)

Pin 7 is the filter output. This pin can typically source over 20mA and sink 2mA. Pin 7 should not drive long coax cables, otherwise the filter's total harmonic distortion will degrade. The maximum load the filter output can drive and still maintain the distortion levels, shown in the Typical Performance Characteristics, is 20k.

Clock Input Pin (Pin 5, N Package)

An external clock, when applied to pin 5, tunes the filter cutoff frequency. The clock-to-cutoff frequency ratio is 100:1. The high (V_{HIGH}) and low (V_{LOW}) clock logic threshold levels are illustrated in Table 2. Square wave clocks with duty cycles between 30% and 50% are strongly recommended. Sinewave clocks are not recommended.

Table 2. Clock Pin Threshold Levels

POWER SUPPLY	V_{HIGH}	V_{LOW}
$V_S = \pm 2.5V$	1.5V	0.5V
$V_S = \pm 5V$	3V	1V
$V_S = \pm 7.5V$	4.5V	1.5V
$V_S = \pm 8V$	4.8V	1.6V
V_S = 5V, 0V	4V	3V
V_S = 12V, 0V	9.6V	7.2V
V_S =15V, 0V	12V	9V

Clock Output Pin (Pin 4, N Package)

Any external clock applied to the clock input pin appears at the clock output pin. The duty cycle of the clock output equals the duty cycle of the external clock applied to the clock input pin. The clock output pin swings to the power supply rails. When the LTC1065 is used in a self-clocking mode, the clock of the internal oscillator appears at the clock output pin with a 30% duty cycle. The clock output pin can be used to drive other LTC1065s or other ICs. The maximum capacitance, $C_{L(MAX)}$, the clock output pin can drive is illustrated in Figure 2.

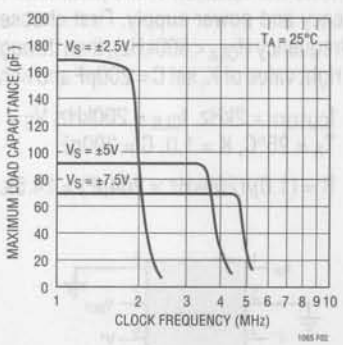


Figure 2. Maximum Load Capacitance at the Clock Output Pin

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TEST CIRCUIT

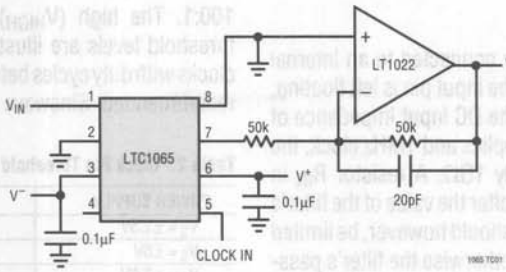

Figure 3. Test Circuit for THD

APPLICATIONS INFORMATION

Self-Clocking Operation

The LTC1065 features an internal oscillator which can be tuned via an external RC. The LTC1065's internal oscillator is primarily intended for generation of clock frequencies below 500kHz. The first curve of the Typical Performance Characteristics section shows how to quickly choose the value of the RC for a given frequency. More precisely, the frequency of the internal oscillator is equal to:

$$f_{CLK} = K/RC$$

For clock frequencies (f_{CLK}) below 100kHz, K equals 1.07. Figure 4b shows the variation of the parameter K versus clock frequency and power supply. First choose the desired clock frequency (f_{CLK} < 500kHz), then through Figure 4b pick the right value of K, set C = 200pF and solve for R.

Example 1: f_{CUTOFF} = 2kHz, f_{CLK} = 200kHz, V_S = ±5V, T_A = 25°C, K = 1.0, C = 200pF

then, $R = (1.0)/(200kHz \times 204pF) = 24.5k$.

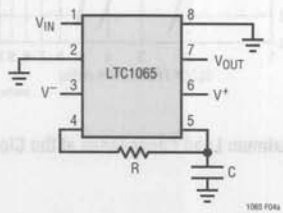

Figure 4a.

Note a 4pF parasitic capacitance is assumed in parallel with the external 200pF timing capacitor. Figure 5 shows the clock frequency variation from –40°C to 85°C. The 200kHz clock of Example 1 will change by –1.75% at 85°C.

For a limited temperature range, the internal oscillator of the LTC1065 can be used to generate clock frequencies above 500kHz (Figures 6 and 7). The data of Figure 6 is derived from several devices. For a given external (RC) value, the observed device-to-device clock frequency variation was ±1% (V_S = ±5V), and ±1.25% for V_S = ±2.5V.

Example 2: f_{CUTOFF} = 20kHz, f_{CLK} = 2MHz, V_S = ±7.5V, T_A = 25°C, C = 10pF

from Figure 6, K = 0.575,

and, $R = (0.575)/(2MHz \times 14pF) = 20.5k$.

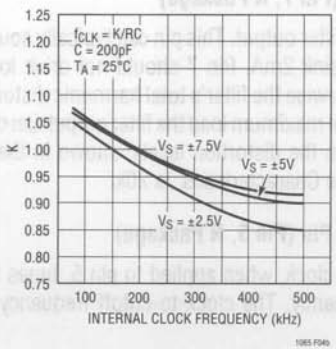

Figure 4b. f_{CLK} vs K

APPLICATIONS INFORMATION

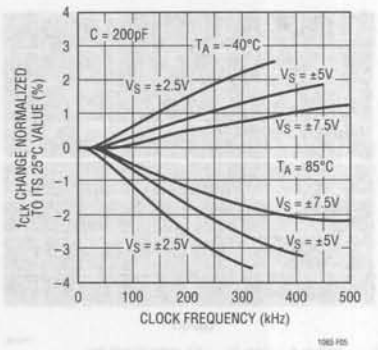

Figure 5. f_{CLK} vs Temperature

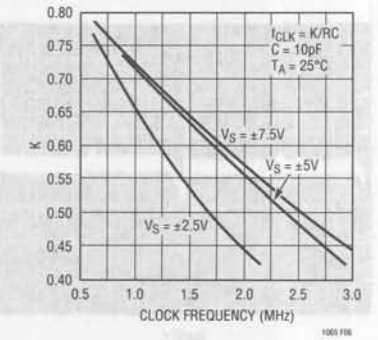

Figure 6. f_{CLK} vs K

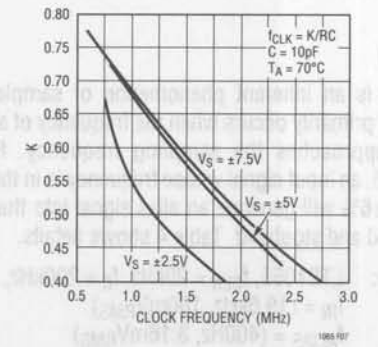

Figure 7. f_{CLK} vs K

A 4pF parasitic capacitance is assumed in parallel with the external 10pF capacitor. A ±1% clock frequency variation from device to device can be expected. The 2MHz clock frequency designed above will typically drift to 1.74MHz at 70°C (Figure 7).

The internal clock of the LTC1065 can be overridden by an external clock provided that the external clock source can drive the timing capacitor C, which is connected from the clock input pin to ground.

Output Offset

The DC output offset of the LTC1065 is trimmed to typically less than ±1mV. The trimming is done at V_S = ±5V. To obtain optimum DC offset performance, appropriate PC layout techniques should be used and the filter IC should be soldered to the PC board. A socket will degrade the output DC offset by typically 1mV. The output DC offset is sensitive to the coupling of the clock output pin 4 (N package) to the negative power supply pin 3 (N package). The negative supply pin should be well decoupled. When the surface mount package is used, all NC pins should be grounded. When the output DC voltage is measured with a voltmeter, the filter output pin should be buffered. Long test leads should be avoided.

With fixed power supplies, the output DC offset should not change by more than ±100µV over 10Hz to 1MHz clock frequency variation. When the filter clock frequency is fixed, the output DC offset will typically change by –4mV (2mV) when the power supply varies from ±5V to ±7.5V (±2.5V). See Typical Performance Characteristics.

Common-Mode Rejection

The common-mode rejection is defined as the change of the output DC offset with respect to the DC change of the input voltage applied to the filter.

$$CMR = 20\log(\Delta V_{OS\ OUT}/\Delta V_{IN})(dB)$$

Table 3 illustrates the common-mode rejection for three power supplies and three temperatures. The common-mode rejection improves if the output offset is adjusted to approximately 0V. The output offset can be adjusted via pin 8 (N package). See Typical Applications.

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APPLICATIONS INFORMATION

Table 3. CMR Data, f_{CLK} = 100kHz

POWER SUPPLY	ΔV_{IN}	–40°C	25°C	85°C	25°C (V_{OS} Nulled)
±2.5V	±1.8V	84dB	83dB	80dB	83dB
±5V	±4V	82dB	78dB	77dB	78dB
±7.5V	±6V	80dB	77dB	76dB	80dB

The above data is valid for clock frequencies up to 800kHz, 900kHz, 1MHz, for V_S = ±2.5V, ±5V, ±7.5V respectively.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics which are present at the filter's output pin. The clock feedthrough is tested with the filter input grounded and it depends on the quality of the PC board layout and power supply decoupling. Any parasitic switching transients during the rise and fall of the incoming clock, are not part of the clock feedthrough specifications; their amplitude strongly depends on scope probing techniques as well as ground quality and power supply bypassing. For a power supply V_S = ±5V, the clock feedthrough of the LTC1065 is 50μV_{RMS}; for V_S = ±7.5V, the clock feedthrough approaches 75μV_{RMS}. Figures 8 and 9 show a typical scope photo of the LTC1065 output pin when the input pin is grounded. The filter cutoff frequency was 1kHz, while scope bandwidth was chosen to be 1MHz so that switching transients above the 100kHz clock frequency would show.

Wideband Noise

The wideband noise data is used to determine the operating signal-to-noise ratio at a given distortion level. The wideband noise (μV_{RMS}) is nearly independent of the value of the clock frequency and excludes the clock feedthrough. The LTC1065's typical wideband noise is 80μV_{RMS}. Figure 9 shows the same scope photo as Figure 8 but with a more sensitive vertical scale. The clock feedthrough is imbedded in the filter's wideband noise. The peak-to-peak wideband noise of the filter can be clearly seen; it is approximately 420μV_{P-P}. Note that 420μV_{P-P} equals the 80μV_{RMS} wideband noise of the part multiplied by a crest factor of 5.25.

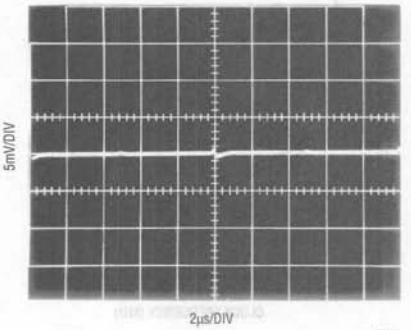


Figure 8. LTC1065 Output Clock Feedthrough + Noise

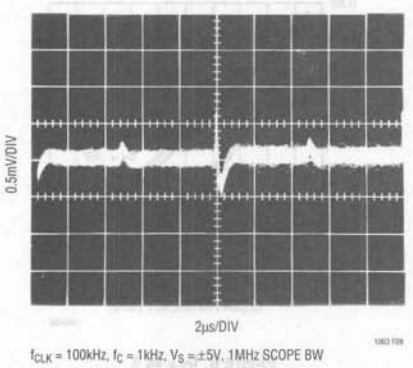


Figure 9. LTC1065 Output Clock Feedthrough + Noise

Aliasing

Aliasing is an inherent phenomenon of sampled data filters. It primarily occurs when the frequency of an input signal approaches the sampling frequency. For the LTC1065, an input signal whose frequency is in the range of f_{CLK} ±6% will generate an alias signal into the filter's passband and stopband. Table 4 shows details.

Example: LTC1065, f_{CLK} = 20kHz, f_C = 200kHz,
f_{IN} = (19.6kHz, 100mV_{RMS})
f_{ALIAS} = (400Hz, 3.16mV_{RMS})

APPLICATIONS INFORMATION

Table 4. Aliasing Data

INPUT FREQUENCY	OUTPUT FREQUENCY	OUTPUT AMPLITUDE REFERENCED TO INPUT SIGNAL
0.9995 f_{CLK}	0.0005 f_{CLK}	−0.01 dB
0.995 f_{CLK}	0.005 f_{CLK}	−0.98 dB
0.99 f_{CLK}	0.01 f_{CLK}	−3.13 dB
0.9875 f_{CLK}	0.0125 f_{CLK}	−4.79 dB
0.985 f_{CLK}	0.015 f_{CLK}	−7.21 dB
0.9825 f_{CLK}	0.0175 f_{CLK}	−10.43 dB
0.98 f_{CLK}	0.02 f_{CLK}	−14.14 dB
0.975 f_{CLK}	0.025 f_{CLK}	−21.84 dB
0.97 f_{CLK}	0.03 f_{CLK}	−28.98 dB
0.965 f_{CLK}	0.035 f_{CLK}	−35.31 dB
0.96 f_{CLK}	0.04 f_{CLK}	−40.94 dB
0.955 f_{CLK}	0.045 f_{CLK}	−45.96 dB
0.95 f_{CLK}	0.05 f_{CLK}	−50.46 dB
0.94 f_{CLK}	0.06 f_{CLK}	−58.29 dB
0.93 f_{CLK}	0.07 f_{CLK}	−64.90 dB
0.9 f_{CLK}	0.1 f_{CLK}	−80.20 dB

An input RC can be used to attenuate incoming signals close to the filter clock frequency (Figure 10). A Bessel passband response will be maintained if the value of the input resistor follows Table 1.

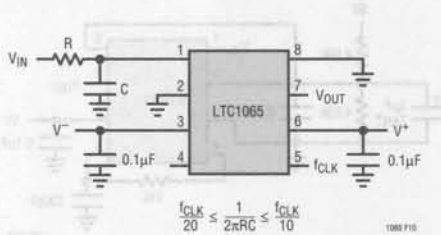
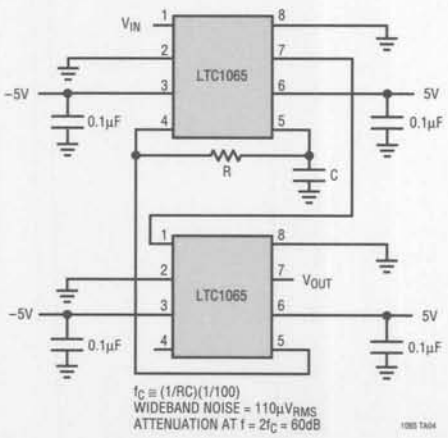


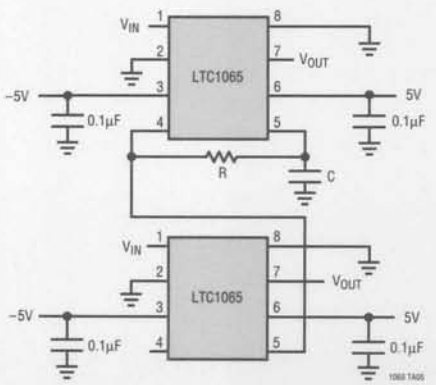
Figure 10. Adding an Input Anti-Aliasing RC

TYPICAL APPLICATIONS

Cascading Two LTC1065s for Steeper Roll-Off



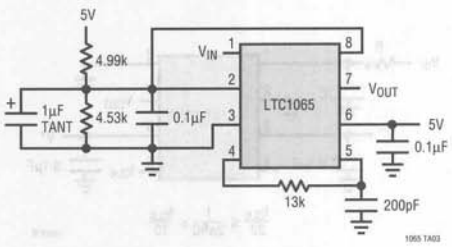
Sharing Clock for Multichannel Applications



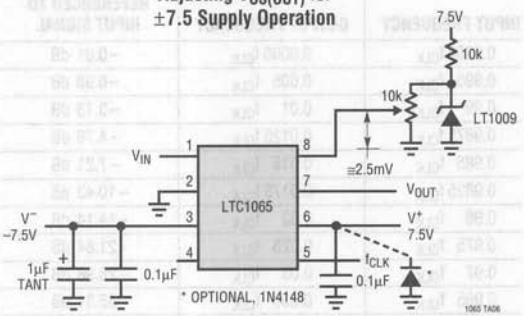
8

TYPICAL APPLICATIONS

Single 5V Supply Operation (f_C = 3.4kHz)



Adjusting $V_{OS(OUT)}$ for ±7.5 Supply Operation



14-Bit DC Accurate Clock-Tunable, 8th Order Elliptic or Linear Phase Lowpass Filter

FEATURES

- **DC Gain Linearity: 14 Bits**
- **Maximum DC Offset: ±1.5mV**
- **DC Offset TempCo: 7μV/°C**
- Device Fully Tested at f_{CUTOFF} = 80kHz
- Maximum Cutoff Frequency: 120kHz (V_S = ±8V)
- Drives 1kΩ Load with 0.02% THD or Better
- Signal-to-Noise Ratio: 90dB
- Input Impedance: 500MΩ
- Selectable Elliptic or Linear Phase Response
- Operates from Single 5V up to ±8V Power Supplies

APPLICATIONS

- Instrumentation
- Data Acquisition Systems
- Anti-Aliasing Filters
- Smoothing Filters
- Audio Signal Processing

DESCRIPTION

The LTC1066-1 is an 8th order elliptic lowpass filter which simultaneously provides clock-tunability and DC accuracy. The unique and proprietary architecture of the filter allows 14 bits of DC gain linearity and a maximum of 1.5mV DC offset. An external RC is required for DC accurate operation. With ±7.5V supplies, a 20k resistor and a 1μF capacitor, the cutoff frequency can be tuned from 800Hz to 100kHz. A clock-tunable 10Hz to 100kHz operation can also be achieved (see Typical Application section).

The filter does not require any external active components such as input/output buffers. The input/output impedance is 500MΩ/0.1Ω and the output of the filter can source or sink 40mA. When pin 8 is connected to V^+, the clock-to-cutoff frequency ratio is 50:1 and the input signal is sampled twice per clock cycle to lower the risk of aliasing. For frequencies up to $0.75f_{CUTOFF}$, the passband ripple is ±0.15dB. The gain at f_{CUTOFF} is –1dB and the filter's stopband attenuation is 80dB at $2.3f_{CUTOFF}$. Linear phase operation is also available with a clock-to-cutoff frequency ratio of 100:1 when pin 8 is connected to ground.

The LTC1066-1 is available in an 18-pin SOL package.

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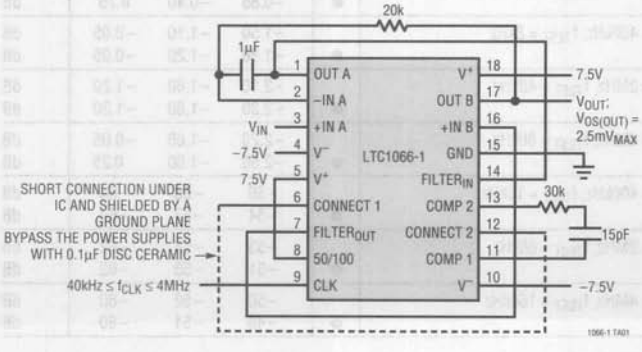
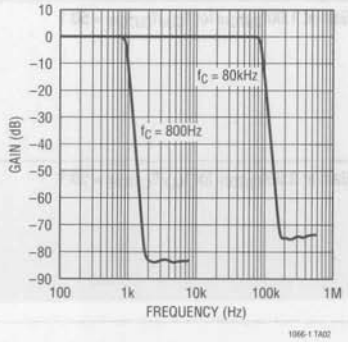
TYPICAL APPLICATION

Clock-Tunable, DC Accurate, 800Hz to 80kHz Elliptic Lowpass Filter



Amplitude Response

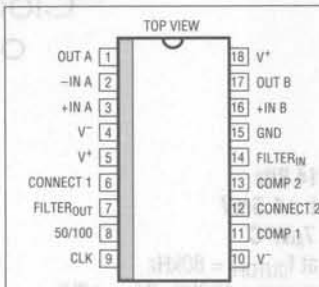


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 700mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Maximum Clock Frequency
$V_S = \pm 8V$ 6.1MHz
$V_S = \pm 7.5V$ 5.4MHz
$V_S = \pm 5V$ 4.1MHz
V_S = Single 5V 1.8MHz
Operating Temperature Range* ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

* For an extended operating temperature range contact LTC Marketing for details.

PACKAGE/ORDER INFORMATION



S PACKAGE
18-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 75°C/W

ORDER PART NUMBER
LTC1066-1CS

Consult factory for other package options and for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (See Test Circuit)

$V_S = \pm 7.5V$, $R_L = 1k$, $T_A = 25°C$, f_{CLK} signal level is TTL or CMOS (maximum clock rise or fall time ≤ 1μs) unless otherwise specified. All AC gain measurements are referenced to passband gain.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain ($0.01f_{CUTOFF}$ to $0.25f_{CUTOFF}$)	f_{CLK} = 400kHz, f_{TEST} = 2kHz	●	–0.18	0.16	0.36	dB
Passband Ripple ($0.01f_{CUTOFF}$ to $0.75f_{CUTOFF}$) for f_{CLK}/f_{CUTOFF} = 50:1	$f_{CUTOFF} \leq$ 50kHz (See Note on Test Circuit)			±0.15		dB
Gain at $0.50f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 4kHz		–0.09	0.02	0.09	dB
		●	–0.14	0.05	0.14	dB
	f_{CLK} = 2MHz, f_{TEST} = 20kHz		–0.16	–0.05	0.02	dB
		●	–0.22	–0.10	0.02	dB
Gain at $0.75f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 6kHz		–0.18	–0.05	0.05	dB
		●	–0.22	–0.10	0.05	dB
	f_{CLK} = 2MHz, f_{TEST} = 30kHz		–0.36	–0.20	0.05	dB
		●	–0.45	–0.30	0.05	dB
	f_{CLK} = 4MHz, f_{TEST} = 60kHz		–0.65	–0.30	0.25	dB
		●	–0.85	–0.40	0.75	dB
Gain at $1.00f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 8kHz		–1.50	–1.10	–0.05	dB
		●	–1.80	–1.20	–0.05	dB
	f_{CLK} = 2MHz, f_{TEST} = 40kHz		–2.10	–1.60	–1.20	dB
		●	–2.30	–1.60	–1.20	dB
	f_{CLK} = 4MHz, f_{TEST} = 80kHz		–2.20	–1.60	–0.05	dB
		●	–2.50	–1.60	0.25	dB
Gain at $2.00f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 16kHz		–56	–58	–64	dB
		●	–54	–57	–64	dB
	f_{CLK} = 2MHz, f_{TEST} = 80kHz		–53	–56	–62	dB
		●	–51	–55	–62	dB
	f_{CLK} = 4MHz, f_{TEST} = 160kHz		–50	–52	–60	dB
		●	–48	–51	–60	dB

ELECTRICAL CHARACTERISTICS (See Test Circuit)

$V_S = \pm 7.5V$, $R_L = 1k$, $T_A = 25°C$, f_{CLK} signal level is TTL or CMOS (maximum clock rise or fall time ≤ 1μs) unless otherwise specified. All AC gain measurements are referenced to passband gain.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Gain at f_{CUTOFF} for f_{CLK} = 20kHz, $V_S = \pm 7.5V$		f_{CLK}/f_{CUTOFF} = 50:1, f_{TEST} = 400Hz	●	−1.75	−1.25	−0.50	dB
Gain at f_{CUTOFF} for $V_S = \pm 2.375V$, f_{CLK}/f_{CUTOFF} = 50:1		f_{CLK} = 1MHz, f_{TEST} = 20kHz	●	−1.75	−0.70	0.10	dB
Gain at 70kHz for $V_S = \pm 5V$, f_{CLK}/f_{CUTOFF} = 50:1		f_{CLK} = 4MHz, f_{TEST} = 70kHz	●		1.00	1.40	dB
Linear Phase Response f_{CLK}/f_{CUTOFF} = 100:1, Pin 8 at GND	Phase at $0.25f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 1kHz	 ●	−48.5 −48.0	−50.0 −50.0	−51.5 −52.0	Deg Deg
	Gain at $0.25f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 1kHz	●	−0.65	−0.25	0.25	dB
	Phase at $0.50f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 2kHz	 ●	−97.5 −97.0	−99.5 −99.5	−101.5 −102.0	Deg Deg
	Gain at $0.50f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 2kHz	●	−0.75	−0.50	−0.10	dB
	Phase at $0.75f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 3kHz	 ●	−148.0 −147.5	−150.5 −150.5	−152.5 −153.0	Deg Deg
	Gain at $0.75f_{CUTOFF}$	f_{CLK} = 400kHz, f_{TEST} = 3kHz	●	−1.40	−1.00	−0.60	dB
	Phase at f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 4kHz	 ●	−208.0 −207.5	−210.0 −210.0	−212.5 −213.0	Deg Deg
	Gain at f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 4kHz	●	−2.10	−1.80	−1.60	dB
Input Bias Current		$V_S = \pm 2.375V$	 ●		60 70	 135	nA nA
Input Offset Current		$V_S = \pm 2.375V$ $V_S \geq \pm 5V$ (Note 2)	● ●		±10 ±10	±40 ±45	nA nA
Input Offset Current TempCo		$\pm 2.375V \leq V_S \leq \pm 7.5V$			40		pA/°C
Output Voltage Offset TempCo		$\pm 2.375V \leq V_S \leq \pm 7.5V$			7		μV/°C
Output Offset Voltage		$V_S = \pm 2.375V$, f_{CLK} = 400kHz	 ●		±0.5 ±1.0	 ±1.5	mV mV
		$V_S \geq \pm 5V$ (Note 2)	 ●		±0.5 ±1.0	 ±1.5	mV mV
Common-Mode Rejection		$V_S = \pm 7.5V$ $V_{CM} = -5V$ to 5V	 ●	90 84	96 90		dB dB
Power Supply Rejection		$V_S = \pm 2.5V$ to $\pm 7.5V$	 ●	80 78	84 82		dB dB
Input Voltage Range and Output Voltage Swing		$V_S = \pm 2.375V$, $R_L = 1k$	 ●	±1.2 ±1.1	±1.4		V V
		$V_S = \pm 5V$, $R_L = 1k$	 ●	±3.4 ±3.2	±3.6		V V
		$V_S = \pm 7.5V$, $R_L = 1k$	 ●	±5.4 ±5.0	±5.8		V V
Output Short-Circuit Current		$\pm 2.375V \leq V_S \leq \pm 7.5V$				±40	mA
Power Supply Current (Note 1)		$V_S = \pm 2.375V$	 ●		14 16	16 19	mA mA
		$V_S = \pm 5V$	 ●		22 23	26 29	mA mA
		$V_S = \pm 7.5V$	 ●		25 26	30 33	mA mA
Power Supply Range				±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The maximum current over temperature is at 0°C. At 70°C the maximum current is less than its maximum value at 25°C.

Note 2: Guaranteed by design and test correlation.

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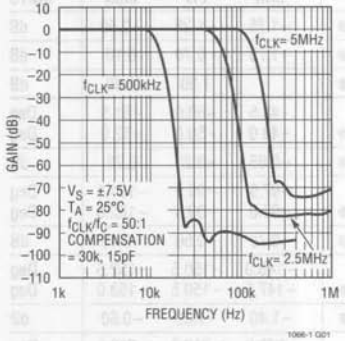
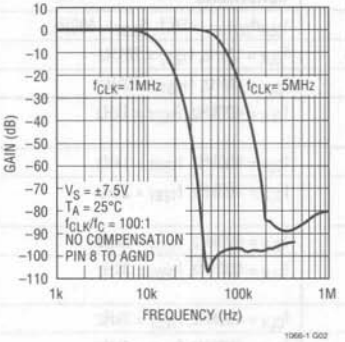
TYPICAL PERFORMANCE CHARACTERISTICS

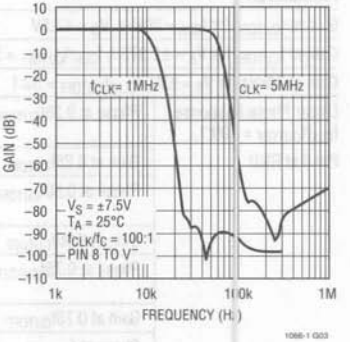
Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 50:1$



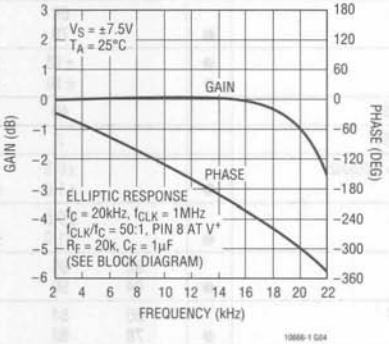
Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 100:1$



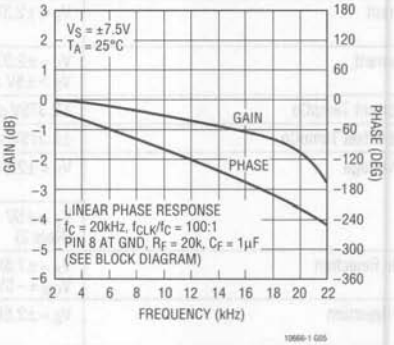
Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 100:1$



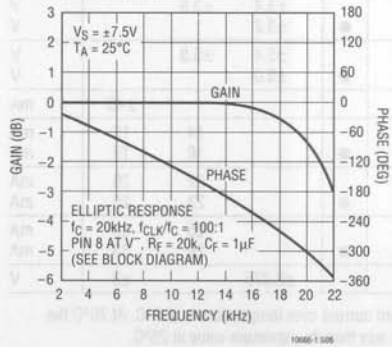
Passband Gain and Phase vs Frequency



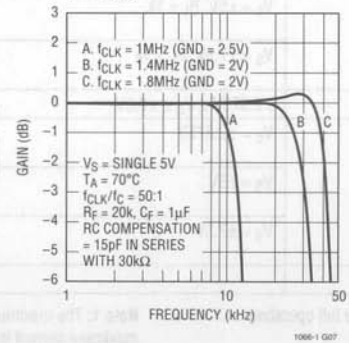
Passband Gain and Phase vs Frequency



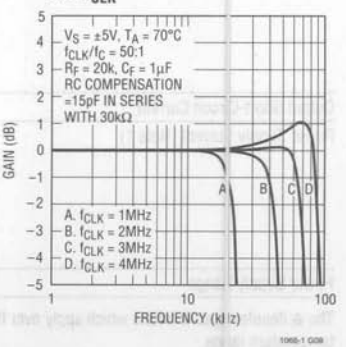
Passband Gain and Phase vs Frequency



Passband Gain vs Frequency and f_{CLK}

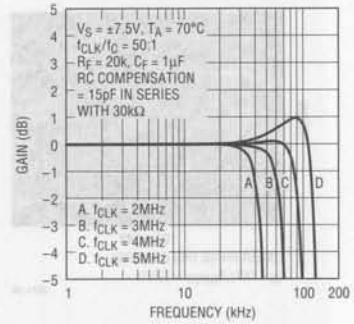


Passband Gain vs Frequency and f_{CLK}

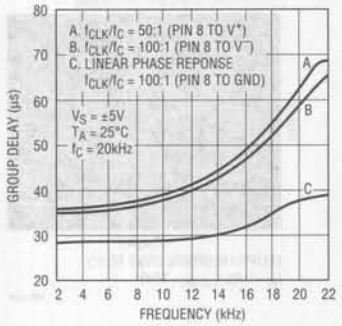


TYPICAL PERFORMANCE CHARACTERISTICS

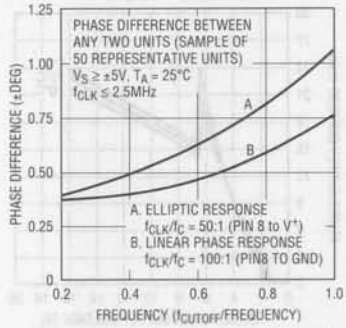
Passband Gain vs Frequency



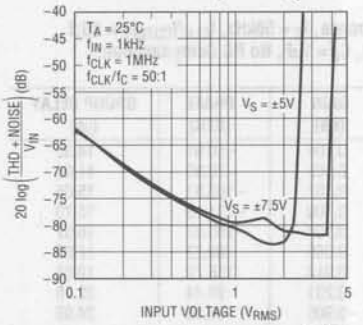
Group Delay vs Frequency



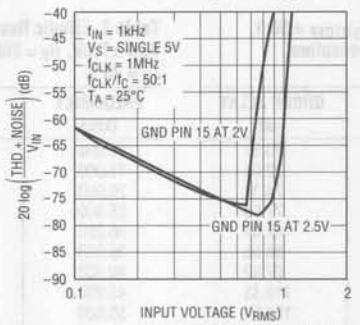
Phase Matching vs Frequency



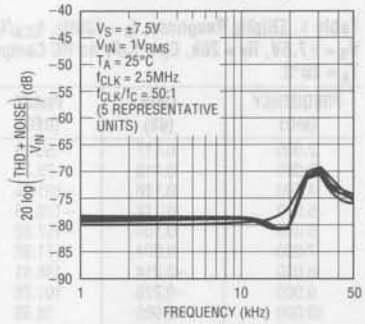
THD + Noise vs Input Voltage



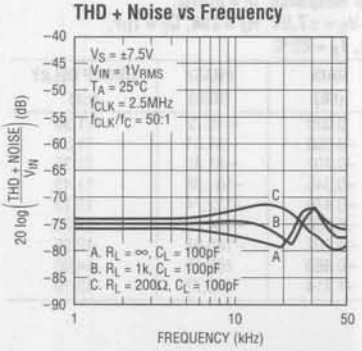
THD + Noise vs Input Voltage



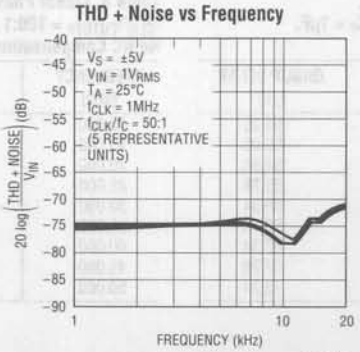
THD + Noise vs Frequency



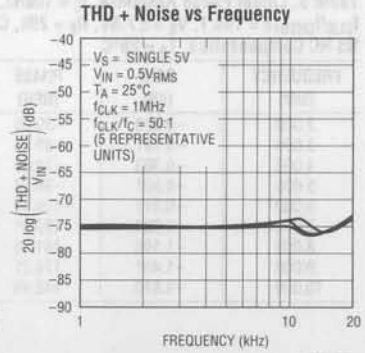
THD + Noise vs Frequency



THD + Noise vs Frequency



THD + Noise vs Frequency



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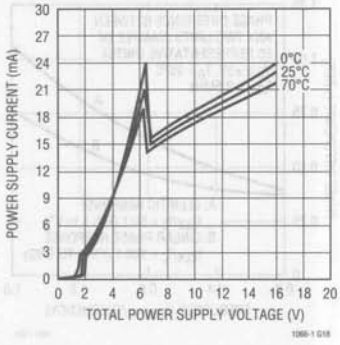
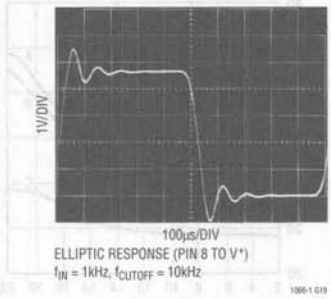
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Current vs Power Supply Voltage



Transient Response



Transient Response

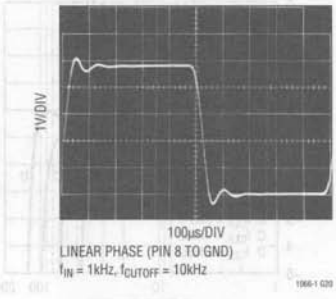


Table 1. Elliptic Response, f_C = 10kHz, f_{CLK}/f_{CUTOFF} = 50:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
2.000	0.117	−50.09	70.52
3.000	0.118	−75.75	72.04
4.000	0.116	−101.96	74.32
5.000	0.112	−129.25	77.59
6.000	0.104	−157.82	82.04
7.000	0.074	171.68	88.56
8.000	−0.014	138.41	97.80
9.000	−0.278	101.26	110.33
10.000	−0.986	58.98	124.91

Table 2. Elliptic Response, f_C = 50kHz, f_{CLK}/f_{CUTOFF} = 50:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
10.000	0.104	−50.91	14.32
15.000	0.105	−76.95	14.61
20.000	0.107	−103.51	15.05
25.000	0.109	−131.13	15.70
30.000	0.107	−160.03	16.57
35.000	0.089	169.22	17.85
40.000	0.014	135.72	19.66
45.000	−0.231	98.44	22.10
50.000	−0.905	56.15	24.93

Table 3. Linear Phase Response, f_C = 10kHz, f_{CLK}/f_{CUTOFF} = 100:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
2.000	−0.020	−39.96	55.25
3.000	−0.181	−59.76	55.03
4.000	−0.383	−79.60	54.98
5.000	−0.601	−99.34	55.28
6.000	−0.811	−119.40	56.34
7.000	−1.004	−139.91	58.56
8.000	−1.196	−161.56	62.34
9.000	−1.451	175.21	67.29
10.000	−1.910	149.99	72.31

Table 4. Linear Phase Response, f_C = 50kHz, f_{CLK}/f_{CUTOFF} = 100:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
10.000	0.039	−40.72	11.30
15.000	−0.068	−61.01	11.31
20.000	−0.202	−81.42	11.36
25.000	−0.345	−101.88	11.48
30.000	−0.479	−122.74	11.73
35.000	−0.594	−144.09	12.20
40.000	−0.701	−166.68	12.99
45.000	−0.860	169.15	14.06
50.000	−1.214	142.72	15.19

PIN FUNCTIONS

Power Supply Pins (5, 18, 4, 10)

The power supply pins should be bypassed with a 0.1µF capacitor to an adequate analog ground. The bypass capacitors should be connected as close as possible to the power supply pins. The V^+ pins (5, 18) and the V^- pins (4, 10) should always be tied to the same positive supply and negative supply value respectively. Low noise linear supplies are recommended. Switching power supplies are not recommended as they will lower the filter dynamic range.

When the LTC1066-1 is powered up with dual supplies and, if V^+ is applied prior to a floating V^-, connect a signal diode (1N4148) between pin 10 and ground to prevent power supply reversal and latch-up. A signal diode (1N4148) is also recommended between pin 5 and ground if the negative supply is applied prior to the positive supply and the positive supply is floating. Note, in most laboratory supplies, reversed biased diodes are always connected between the supply output terminals and ground, and the above precautions are not necessary. However, when the filter is powered up with conventional 3-terminal regulators, the diodes are recommended.

Analog Ground Pin (15)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 15 should be connected to the analog ground plane. For single supply operation pin 15 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (see Typical Applications). For single 5V operation and for $f_{CLK} \geq 1.4MHz$, pin 15 should be biased at 2V. This minimizes passband gain and phase variations.

Clock Input Pin (9)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 5 shows the clock's low and high level threshold values for a dual or single supply operation. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the left side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 9 will slow down the rise and fall times of the clock to further reduce charge coupling.

Table 5. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

50:1/100:1 Pin (8)

The DC level at pin 8 determines the ratio of the clock to the filter cutoff frequency. When pin 8 is connected to V^+ the clock-to-cutoff frequency ratio (f_{CLK}/f_{CUTOFF}) is 50:1 and the filter response is elliptic. The design of the internal switched-capacitor filter was optimized for a 50:1 operation.

When pin 8 is connected to ground (or 1/2 supply for single supply operation), the f_{CLK}/f_{CUTOFF} ratio is equal to 100:1 and the filter response is pseudolinear phase (see Group Delay vs Frequency in Typical Performance Characteristic section).

When pin 8 is connected to V^- (or ground for single supply operation), the f_{CLK}/f_{CUTOFF} ratio is 100:1 and the filter response is transitional Butterworth elliptic. The Typical Performance Characteristics provide all the necessary information.

If the DC level at pin 8 is mechanically switched, a 10k resistor should be connected between pin 8 and the DC source.

Input Pins (2, 3, 14, 16)

Pin 3 (+IN A) and pin 2 (–IN A) are the positive and negative inputs of an internal high performance op amp A

PIN FUNCTIONS

(see Block Diagram). Input bias current flows out of pins 2 and 3. Pin 16 (+IN B) is the positive input of a high performance op amp B which is internally connected as a unity-gain follower. Op amp B buffers the switched-capacitor network output. The input capacitance of both op amps is 10pF.

Pin 14 ($FILTER_{IN}$) is the input of a switched-capacitor network. The input impedance of pin 14 is typically 11k.

Output Pins (1, 7, 17)

Pins 1 and 17 are the outputs of the internal high performance op amps A and B. Pin 1 is usually connected to the internal switched-capacitor filter network input pin 14. Pin 17 is the buffered output of the filter and it can drive loads as heavy as 200Ω (see THD + Noise curves under Typical Performance Characteristics). Pin 7 is the internal switched-capacitor network output and it can typically sink or source 1mA.

Compensation Pins (11, 13)

Pins 11 and 13 are the AC compensation pins. If compensation is needed, an external 30k resistor in series with a 15pF capacitor should be connected between pins 11 and 13. Compensation is recommended for the following cases shown in Table 6.

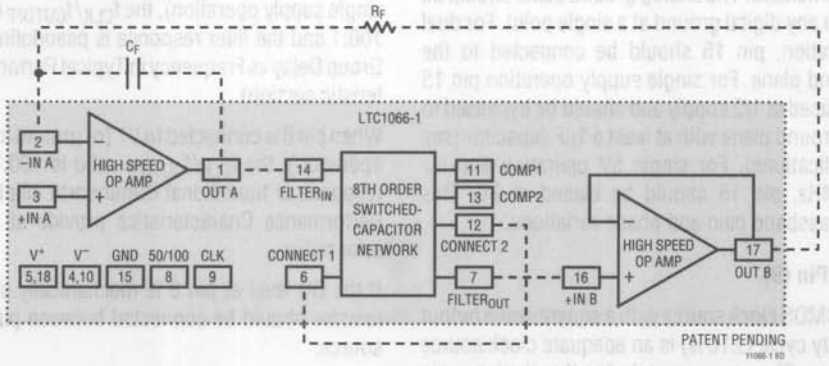
Table 6. Cases Where an RC Compensation (15pF in Series with 30kΩ pins 11, 13) is Recommended, f_{CLK}/f_{CUTOFF} = 50:1

V_S = Single 5V (AGND = 2V)	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 28kHz $f_{CUTOFF} \geq$ 24kHz
V_S = ±5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 60kHz $f_{CUTOFF} \geq$ 50kHz
V_S = ±7.5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 70kHz $f_{CUTOFF} \geq$ 60kHz

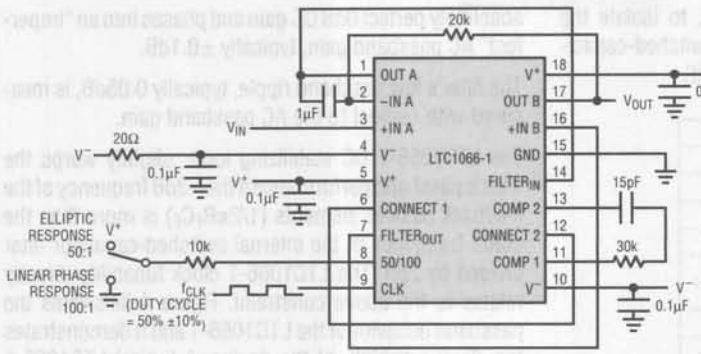
Connect Pins (6, 12)

Pin 6 (CONNECT 1) and pin 12 (CONNECT 2) should be shorted. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane. Pin 6 should be 0.2 inches away from any other circuit trace.

BLOCK DIAGRAM



TEST CIRCUIT



NOTE: RC COMPENSATION BETWEEN PINS 11 AND 13 IS REQUIRED ONLY FOR CLOCK-TUNABLE OPERATION FOR:
50kHz < $f_{CUTOFFs}$ ≤ 100kHz.

THE TEST SPECIFICATIONS FOR:
f_{CLK} = 2MHz, f_{CUTOFF} = 40kHz, AND
f_{CLK} = 4MHz, f_{CUTOFF} = 80kHz
INCLUDE THE EFFECTS OF RC COMPENSATION.

COMPENSATION DOES NOT INFLUECE THE SPECIFICATIONS FOR:
f_{CLK} = 400kHz, f_{CUTOFF} = 8kHz.

FOR CLOCK-TUNABLE $f_{CUTOFFs}$ FROM 2kHz TO 50kHz COMPENSATION IS NOT REQUIRED AND THE FILTER'S PASSBAND PERFORMANCE IS REPRESENTED BY THE TYPICAL SPECIFICATIONS AT:
f_{CLK} = 400kHz, f_{CUTOFF} = 8kHz.

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APPLICATIONS INFORMATION

DC PERFORMANCE

The DC performance of the LTC1066-1 is dictated by the DC characteristics of the input precision op amp.

1. DC input voltages in the vicinity of the filter's half of the total power supply are processed with exactly 0dB (or 1V/V) of gain.

2. The typical DC input voltage ranges are equal to:

   $V_{IN} = \pm 5.8V$, $V_S = \pm 7.5V$
   $V_{IN} = \pm 3.6V$, $V_S = \pm 5V$
   $V_{IN} = \pm 1.4V$, $V_S = \pm 2.5V$

   With an input DC voltage range of $V_{IN} = \pm 5V$, ($V_S = \pm 7.5V$), the measured CMRR was 100dB. Figure 1 shows the DC gain linearity of the filter exceeding the requirements of a 14-bit, 10V full scale system.

3. The filter output DC offset $V_{OS(OUT)}$ is measured with the input grounded and with dual power supplies. The $V_{OS(OUT)}$ is typically ±0.1mV and it is optimized for the filter connection shown in the test circuit figure. The filter output offset is equal to:

   $$V_{OS(OUT)} = V_{OS}\,(\text{op amp A}) - I_{BIAS} \times R_F = 0.1mV\,(\text{Typ})$$

4. The $V_{OS(OUT)}$ temperature drift is typically 7µV/°C ($T_A > 25°C$), and –7µV/°C ($T_A < 25°C$).

5. The $V_{OS(OUT)}$ temperature drift can be improved by using an input resistor R_{IN} equal to the feedback resistor R_F, however, the absolute value of $V_{OS(OUT)}$ will increase. For instance, if a 20k resistor is added in series with pin 3 (see Test Circuit), the output V_{OS} drift will be improved by 2µV/°C to 3µV/°C, however, the $V_{OS(OUT)}$ may increase by $1mV_{(MAX)}$.

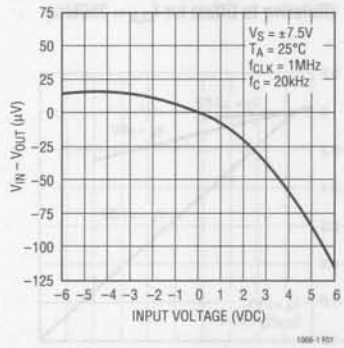

Figure 1. DC Gain Linearity

6. The filter DC output offset voltage $V_{OS(OUT)}$ is independent from the filter clock frequency ($f_{CLK} \leq 250kHz$).

   Figures 2 and 3 show the $V_{OS(OUT)}$ variation for three different power supplies and for clock frequencies up to 5MHz. Both figures were traced with the LTC1066-1 soldered into the PC board. Power supply decoupling is very important, especially with ±7.5V supplies. If necessary connect a small resistor (20Ω) between pins 5

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APPLICATIONS INFORMATION

and 18, and between pins 10 and 4, to isolate the precision op amp supply pin from the switched-capacitor network supply (see the Test Circuit).

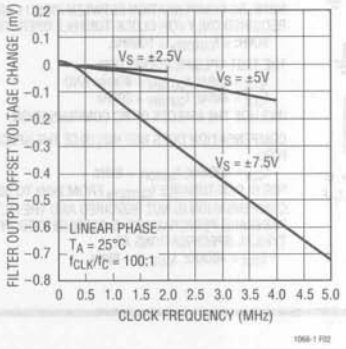


Figure 2. Output Offset Change vs Clock (Relative to Offset for f_{CLK} = 250kHz)

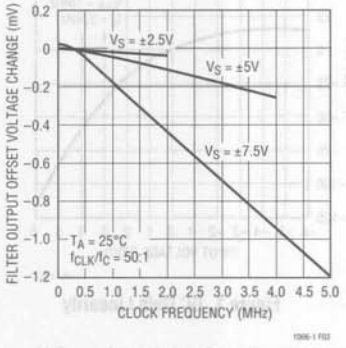


Figure 3. Output Offset Change vs Clock (Relative to Offset for f_{CLK} = 250kHz)

AC PERFORMANCE

AC (Passband) Gain

The passband gain of the LTC1066-1 is equal to the passband gain of the internal switched-capacitor lowpass filter, and it is measured at $f = 0.25f_{CUTOFF}$. Unlike conventional monolithic filters, the LTC1066-1 starts with an absolutely perfect 0dB DC gain and phases into an "imperfect" AC passband gain, typically ±0.1dB.

The filter's low passband ripple, typically 0.05dB, is measured with respect to the AC passband gain.

The LTC1066-1 DC stabilizing loop slightly warps the filter's passband performance if the –3dB frequency of the feedback passive elements ($1/2\pi R_F C_F$) is more than the cutoff frequency of the internal switched-capacitor filter divided by 250. The LTC1066-1 clock tunability directly relates to the above constraint. Figure 4 illustrates the passband behavior of the LTC1066-1 and it demonstrates the clock tunability of the device. A typical LTC1066-1 device was used to trace all four curves of Figure 4. Curve D, for instance, has nearly zero ripple and 0.04dB passband gain. Curve D's 20kHz cutoff is much higher than the 8Hz cutoff frequency of the $R_F C_F$ feedback network, so its passband is free from any additional error due to $R_F C_F$ feedback elements. Curve B illustrates the passband error when the 1MHz clock of curve D is lowered to 100kHz. A 0.1dB error is added to the filter's original AC gain of 0.04dB.

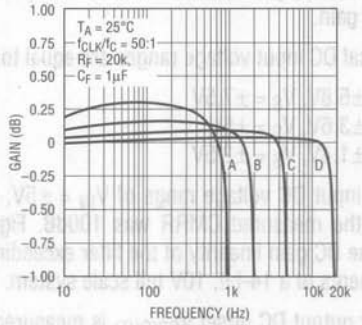


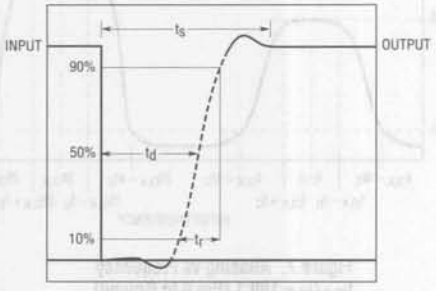
Figure 4. Passband Behavior

APPLICATIONS INFORMATION

Transient Response and Settling Time

The LTC1066-1 exhibits two different transient behaviors. First, during power-up the DC correcting loop will settle after the voltage offset of the internal switched-capacitor network is stored across the feedback capacitor C_F (see Block Diagram). It takes approximately five time constants ($5R_FC_F$) for settling to 1%. Second, following DC loop settling, the filter reaches steady state. The filter transient response is then defined by the frequency characteristics of the internal switched-capacitor lowpass filter. Figure 5 shows details.

DC loop settling is also observed if, at steady state, the DC offset of the internal switched-capacitor network suddenly changes. A sudden change may occur if the clock frequency is instantaneously stepped to a value above 1MHz.



	50:1 ELLIPTIC	100:1 LINEAR PHASE
RISE TIME (t_r)	$\frac{0.43}{f_{CUTOFF}}$ ±5%	$\frac{0.43}{f_{CUTOFF}}$ ±5%
SETTLING TIME (t_s)	$\frac{3.4}{f_{CUTOFF}}$ ±5%	$\frac{2.05}{f_{CUTOFF}}$ ±5%
DELAY TIME (t_d)	$\frac{0.709}{f_{CUTOFF}}$ ±5%	$\frac{0.556}{f_{CUTOFF}}$ ±5%

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Figure 5. Transient Response

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown on Table 7.

Table 7. Clock Feedthrough

POWER SUPPLY	50:1	100:1
Single 5V	70μV_{RMS}	90μV_{RMS}
±5V	100μV_{RMS}	200μV_{RMS}
±7.5V	160μV_{RMS}	650μV_{RMS}

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and cannot be reduced with post filtering. For instance, the LTC1066-1 wideband noise at ±5V supply is 100μV_{RMS}, 95μV_{RMS} of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise. Table 8 lists the typical wideband noise for each supply.

Table 8. Wideband Noise

POWER SUPPLY	50:1	100:1 (Pin 8 to GND)
Single 5V	90μV_{RMS}	80μV_{RMS}
±5V	100μV_{RMS}	85μV_{RMS}
±7.5V	106μV_{RMS}	90μV_{RMS}

Speed Limitations

To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN}

INPUT FREQUENCY	MAXIMUM V_{IN}
≥250kHz	0.50V_{RMS}
≥700kHz	0.25V_{RMS}

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APPLICATIONS INFORMATION

Aliasing

In a sampled-data system the sampling theorem says that if an input signal has any frequency components greater than one half the sampling frequency, aliasing errors will appear at the output. In practice, aliasing is not always a serious problem. High order switched-capacitor lowpass filters are inherently band limited and significant aliasing occurs only for input signals centered around the clock frequency and its multiples.

Figure 6 shows the LTC1066-1 aliasing response when operated with a clock-to-cutoff frequency ratio of 50:1. With a 50:1 ratio LTC1066-1 samples its input twice during one clock period and the sampling frequency is equal to two times the clock frequency.

The figure also shows the maximum aliased output generated for inputs in the range of $2f_{CLK} \pm f_C$. For instance, if the LTC1066-1 is programmed to produce a cutoff frequency of 20kHz with 1MHz clock, a 10mV, 1.02MHz input signal will cause a 10μV aliased signal at 20kHz. This signal will be buried in the noise. Maximum aliasing will occur only for input signals in the narrow range of 2MHz ±20kHz or multiples of 2MHz.

Figure 7 shows the LTC1066-1 aliased response when operated with a clock-to-cutoff frequency ratio of 100:1 (linear phase response with pin 8 to ground).

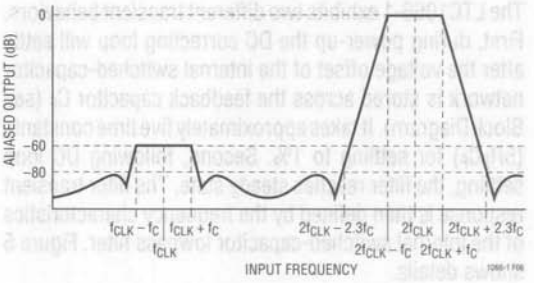


Figure 6. Aliasing vs Frequency
f_{CLK}/f_C = 50:1 (Pin 8 to V⁺)
Clock is a 50% Duty Cycle Square Wave

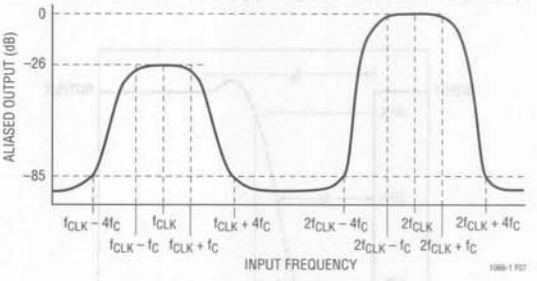
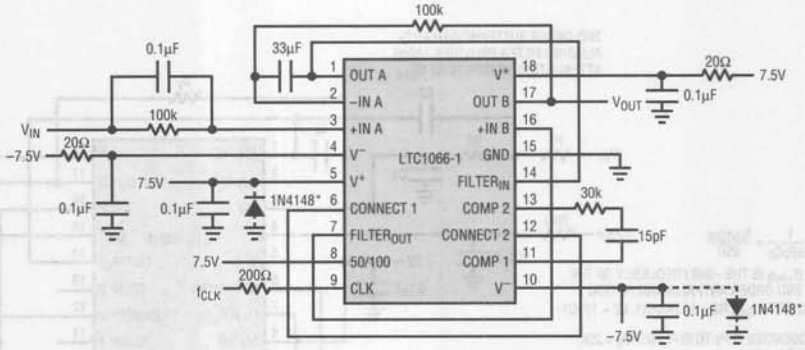


Figure 7. Aliasing vs Frequency
f_{CLK}/f_C = 100:1 (Pin 8 to Ground)
Clock is a 50% Duty Cycle Square Wave

TYPICAL APPLICATIONS

Dual Supply Operation
DC Accurate, *10Hz to 100kHz*, Clock-Tunable, 8th Order Elliptic Lowpass Filter
f_{CLK}/f_C = 50:1



MAXIMUM OUTPUT VOLTAGE OFFSET = ±5.5mV, DC LINEARITY = ±0.0063%, T_A = 25°C.
THE PINS 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.
RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR $f_{CUTOFF} \geq$ 60kHz.
THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5 OR EQUIVALENT).
* PROTECTION DIODES, 1N4148 ARE OPTIONAL. SEE PIN DESCRIPTIONS.

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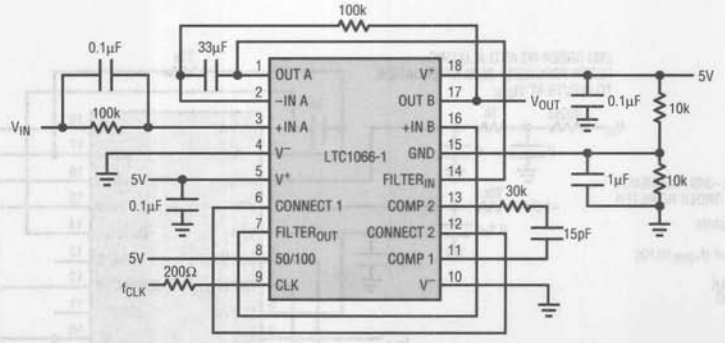
Single 5V Supply Operation
DC Accurate, *10Hz to 36kHz*, Clock-Tunable, 8th Order Elliptic Lowpass Filter
f_{CLK}/f_C = 50:1



INPUT LINEAR RANGE = 1.4V to 3.6V, DC LINEARITY = ±0.0063%.
THE PINS 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.
RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR $f_{CUTOFF} \geq$ 24kHz.
THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5)

1066-1 TA04

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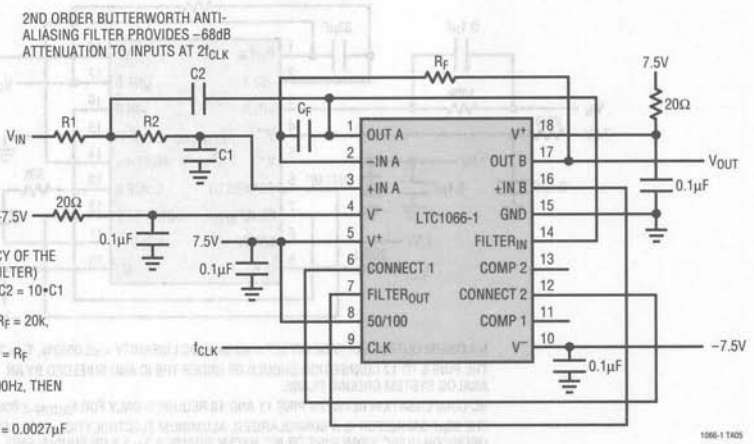
TYPICAL APPLICATIONS

DC Accurate Lowpass Filter with Input Anti-Aliasing ($f_{CLK} \leq 250kHz$)



$f_{CUTOFF} = \frac{f_{CLK}}{50}, \frac{1}{2\pi R_F C_F} = \frac{f_{CUTOFF}}{250}$

$f_{-3dB} = 2 \bullet f_{CUTOFF}$ (f_{-3dB} IS THE –3dB FREQUENCY OF THE 2ND ORDER ANTI-ALIASING FILTER)

$\frac{1}{2\pi(R1 + R2)C1} = 0.707 \bullet f_{-3dB}$, R2 = 17.946•R1, C2 = 10•C1

FOR CUTOFF FREQUENCIES 2kHz TO 5kHz, SET R_F = 20k, C_F = 1µF AND R1 + R2 ≤ 2k

FOR CUTOFF FREQUENCIES <2kHz, SET R1 + R2 = R_F

FOR EXAMPLE:

IF THE CUTOFF FREQUENCY OF LTC1066-1 IS 500Hz, THEN

f_{-3dB} = 1000Hz

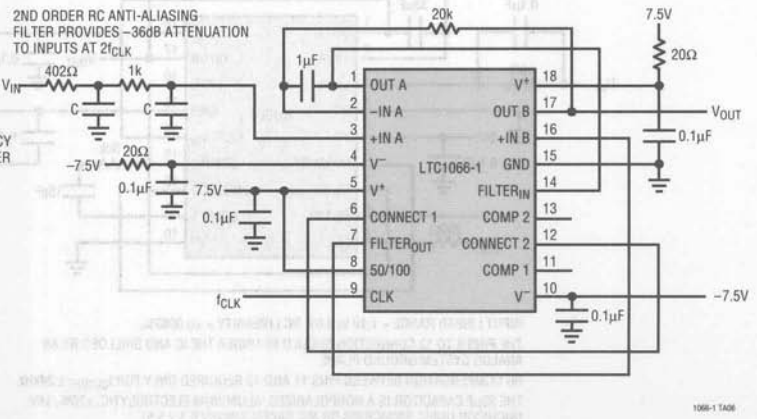
$\frac{1}{2\pi R_F C_F}$ = 2Hz, SET R_F = 80.6k, C_F = 1µF AND C1 = 0.0027µF

R1 + R2 = 80.6k, R1 = 4.22k AND R2 = 76.8k ROUNDED TO NEAREST 1% VALUE.

C2 = 0.027µF ROUNDED TO NEAREST STANDARD VALUE.

NOTE: R_F SHOULD BE ≤100k TO MINIMIZE DC OFFSET TO ±5.5mV

DC Accurate Lowpass Filter with Input Anti-Aliasing ($f_{CLK} > 250kHz$)



f_{-3dB} IS THE –3dB FREQUENCY OF THE 2ND ORDER RC FILTER

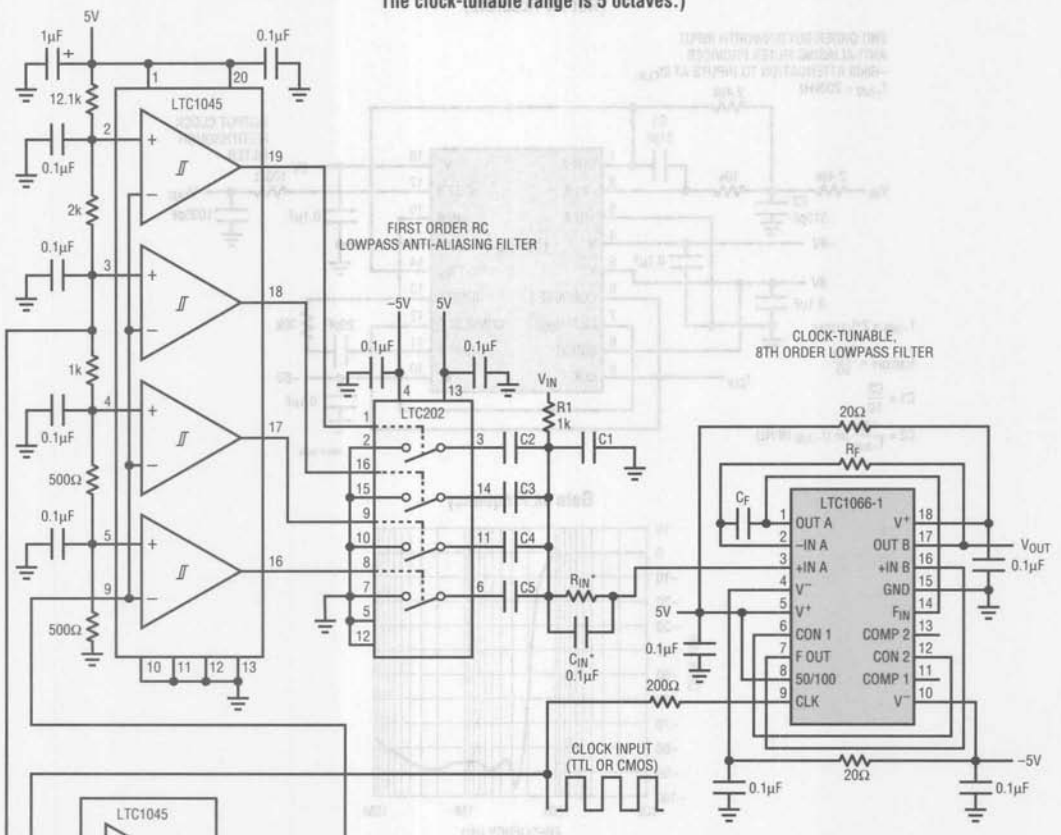
$f_{-3dB} = 5 \bullet f_{CUTOFF}$

$C = \frac{100}{f_{-3dB}}$ µF (f_{-3dB} IN Hz)

$f_{CUTOFF} = \frac{f_{CLK}}{50}$

TYPICAL APPLICATIONS

DC Accurate Clock-Tunable Lowpass Filter with Tunable Input Anti-Aliasing Filter (Circuit provides at least –20dB attenuation to input frequencies at $2f_{CLK}$. The clock-tunable range is 5 octaves.)



CLOCK FREQUENCY DETECTOR

COMPONENT CALCULATIONS FOR A CLOCK-TUNABLE RANGE OF FIVE OCTAVES:

DEFINITIONS: 1. THE CUTOFF FREQUENCY OF LTC1066-1 IS ABBREVIATED AS f_C
2. $f_{C(LOW)}$ IS THE LOWEST CUTOFF FREQUENCY OF INTEREST
3. A RANGE OF FIVE OCTAVES IS FROM $f_{C(LOW)}$ TO $32f_{C(LOW)}$

COMPONENT CALCULATIONS:

$$\frac{1}{2\pi R_F C_F} = \frac{f_{C(LOW)}}{125}\ ;\ R_{IN}^* = R_F \text{ (IF } R_F \text{ CAN BE CHOSEN TO BE 20k, } R_{IN} \text{ AND } C_{IN} \text{ ARE OMITTED. } f_{C(LOW)}/125 \text{ ALLOWS FOR 0.2dB GAIN PEAK IN THE PASSBAND)}$$

$$C1 = \frac{1}{f_{C(LOW)}}\ \mu F\ (f_{C(LOW)} \text{ IN Hz})\ ;\ R1 = 1k$$

$$C2 = C1,\ C3 = 2 \bullet C1,\ C4 = 4 \bullet C1,\ C5 = 8 \bullet C1$$

$$C_P = 50pF;\ R_P = \frac{10^5}{50 \bullet f_{C(LOW)}}\ k$$

$$C_A = 0.047\mu F;\ R_A = \frac{5 \times 10^5}{50 \bullet f_{C(LOW)}}\ k$$

EXAMPLE: LET'S CHOOSE A FIVE OCTAVE RANGE FROM 1kHz TO 32kHz. $f_{C(LOW)}$ = 1kHz (1000Hz). LET C_F = 1µF, THEN R_F CALCULATES TO BE 20k. R_{IN} AND C_{IN} OMITTED; R1 = 1k, C1 = 0.001µF, C2 = 0.001µF, C3 = 0.0022µF, C4 = 0.0039µF, C5 = 0.0082µF. C_P = 50pF, R_P = 2k, C_A = 0.047µF, R_A = 10k

1066-1 TA08

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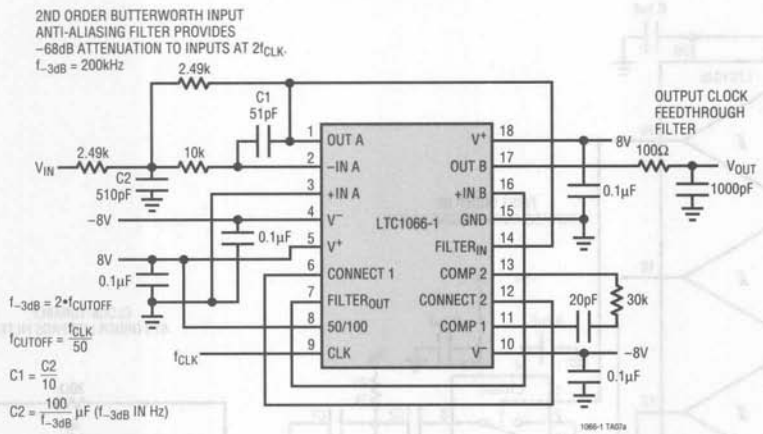
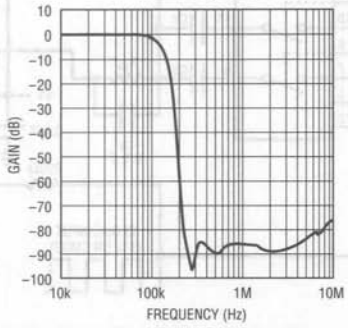
TYPICAL APPLICATIONS

100kHz Elliptic Lowpass Filter with Input Anti-Aliasing and Output Clock Feedthrough Filters (Not DC Accurate)



Gain vs Frequency



Low Power 8th Order Pin Selectable Butterworth or Bessel Lowpass Filter

FEATURES

- Pin Selectable Butterworth or Bessel Response
- 4mA Supply Current with ±5V Supplies
- f_{CUTOFF} up to 20kHz
- 100μV_{RMS} Wideband Noise
- THD < 0.02% (50:1, V_S = ±7.5V, V_{IN} = 2V_{RMS})
- Operates with a Single 5V Supply (1V_{RMS} Input Range)
- 60μV_{RMS} Clock Feedthrough (Single 5V Supply)
- Operates up to ±8V Supplies
- TTL/CMOS-Compatible Clock Input
- No External Components

APPLICATIONS

- Anti-Aliasing Filters
- Battery-Operated Instruments
- Telecommunications Filters
- Smoothing Filters

DESCRIPTION

The LTC1164-5 is a monolithic 8th order filter; it approximates either a Butterworth or a Bessel lowpass response. The LTC1164-5 features clock-tunable cutoff frequency and low power consumption (4.5mA with ±5V supplies and 2.5mA with single 5V supply).

Low power operation is achieved without compromising noise or distortion performance. With ±5V supplies and 10kHz cutoff frequency, the operating signal-to-noise ratio is 86dB and the THD throughout the passband is 0.015%. Under the same conditions, a 77dB signal-to-noise ratio and distortion is obtained with a single 5V supply while the clock feedthrough is kept below the noise level. The maximum signal-to-noise ratio is 92dB.

The LTC1164-5 approximates an 8th order Butterworth response with a clock-to-cutoff frequency ratio of 100:1 (pin 10 to V^-) or 50:1 double-sampled (pin 10 to V^+ and pin 1 shorted to pin 13). Double-sampling allows the input signal frequency to reach the clock frequency before any aliasing occurrence. An 8th order Bessel response can also be approximated with a clock-to-cutoff frequency ratio of 140:1 (pin 10 to ground). With ±7.5V supply, ±5V supply and single 5V supply, the maximum clock frequency of the LTC1164-5 is 1.5MHz, 1MHz, and 1MHz respectively. The LTC1164-5 is pin-compatible with the LTC1064-2 and LTC1064-3.

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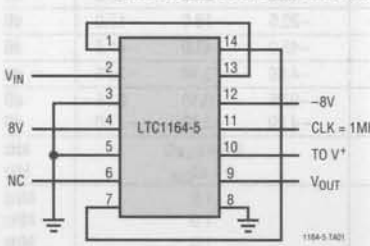
TYPICAL APPLICATION

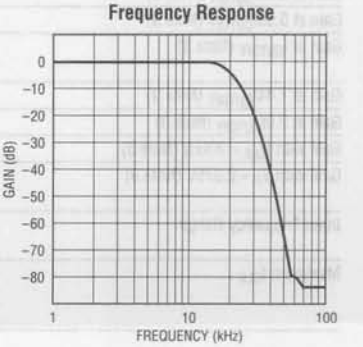
Butterworth 20kHz Anti-Aliasing Filter



WIDEBAND NOISE = 110μV_{RMS}
THD IN PASSBAND < 0.02% AT V_{IN} = 2V_{RMS}

NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. FOR 50:1 OPERATION CONNECT PIN 1 TO PIN 13 AS SHOWN. FOR 100:1 OR 150:1 OPERATION PINS 1 AND 13 SHOULD FLOAT. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

Frequency Response

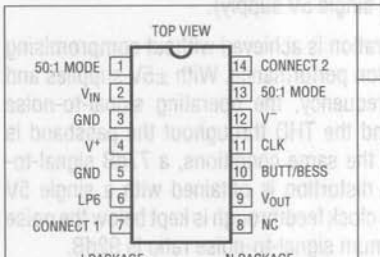


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V

Operating Temperature Range ..... 0°C to 70°C
LTC1164-5C ..... –40°C to 85°C
LTC1164-5M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

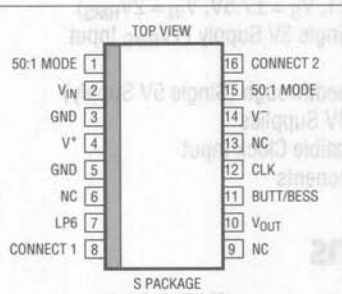


J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER
LTC1164-5CN LTC1164-5CJ LTC1164-5MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1164-5CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, f_{CLK} = 400kHz, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1164-5C MIN	TYP	MAX	UNITS
Passband Gain 0.1Hz at 0.25f_{CUTOFF} (Note 3)	f_{IN} = 1kHz, (f_{CLK}/f_C) = 100:1	●	–0.5	–0.10	0.25	dB
	f_{IN} = 1kHz, (f_{CLK}/f_C) = 50:1	●	–0.5	0.10	0.25	dB
Gain at 0.50f_{CUTOFF} (Note 3)	f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1	●	–0.45	–0.20	0.17	dB
	f_{IN} = 4kHz, (f_{CLK}/f_C) = 50:1	●	–0.35	–0.10	0.40	dB
Gain at 0.90f_{CUTOFF} (Note 3)	f_{IN} = 3.6kHz, (f_{CLK}/f_C) = 100:1	●	–2.50	–1.90	–1.0	dB
Gain at 0.95f_{CUTOFF} (Note 3)	f_{IN} = 3.8kHz, (f_{CLK}/f_C) = 100:1			–2.60		dB
Gain at f_{CUTOFF} (Note 3)	f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1	●	–4.10	–3.40	–2.75	dB
	f_{IN} = 8kHz, (f_{CLK}/f_C) = 50:1	●	–4.20	–3.80	–2.75	dB
Gain at 1.44f_{CUTOFF} (Note 3)	f_{IN} = 5.76kHz, (f_{CLK}/f_C) = 100:1	●	–20.5	–19.0	–17.0	dB
Gain at 2.0f_{CUTOFF} (Note 3)	f_{IN} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–45.0	–43.0	–41.0	dB
Gain with f_{CLK} = 20kHz (Note 3)	f_{IN} = 200Hz, (f_{CLK}/f_C) = 100:1	●	–4.50	–3.40	–2.75	dB
Gain with V_S = 2.375V (Note 3)	f_{IN} = 400kHz, f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1		–0.25	–0.10	0.35	dB
	f_{IN} = 400kHz, f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1		–4.20	–3.40	–2.00	dB
Input Frequency Range	(f_{CLK}/f_C) = 100:1			0 – <$f_{CLK}/2$		kHz
	(f_{CLK}/f_C) = 50:1			0 – <f_{CLK}		kHz
Maximum f_{CLK}	$V_S \geq$ ±7.5V			1.5		MHz
	V_S = ±5.0V			1.0		MHz
	V_S = Single 5V (GND = 2V)			1.0		MHz

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, f_{CLK} = 400kHz, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1164-5C MIN	TYP	MAX	UNITS
Clock Feedthrough	Input at GND, f = f_{CLK}, Square Wave					
	±5V, (f_{CLK}/f_C) = 100:1			200		μV_{RMS}
	±5V, (f_{CLK}/f_C) = 50:1			100		μV_{RMS}
Wideband Noise	Input at GND, 1Hz ≥ f < f_{CLK}					
	±5V, (f_{CLK}/f_C) = 100:1			100 ± 5%		μV_{RMS}
	±5V, (f_{CLK}/f_C) = 50:1			115 ± 5%		μV_{RMS}
Input Impedance			70	100	140	kΩ
Output DC Voltage Swing	V_S = ±2.375V	●	±1.25	±1.50		V
	V_S = ±5.0V	●	±3.70	±4.10		V
	V_S = ±7.5V	●	±5.40	±5.90		V
Output DC Offset	V_S = ±5V, (f_{CLK}/f_C) = 100:1			±50	±160	mV
Output DC Offset TempCo	V_S = ±5V, (f_{CLK}/f_C) = 100:1			±100		µV/°C
Power Supply Current	V_S = ±2.375V, T_A ≥ 25°C			2.5	4.0	mA
		●			4.5	mA
	V_S = ±5.0V, T_A ≥ 25°C			4.5	7.0	mA
		●			8.0	mA
	V_S = ±7.5V, T_A ≥ 25°C			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

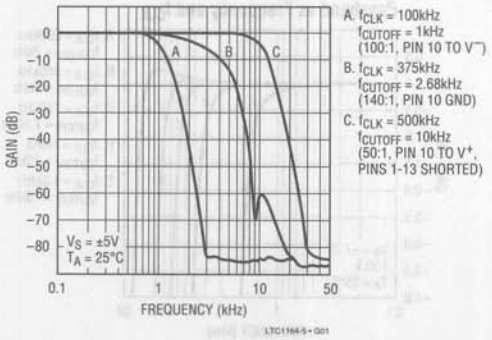
Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any pin to voltages greater than V^+ or less than V^- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-5.

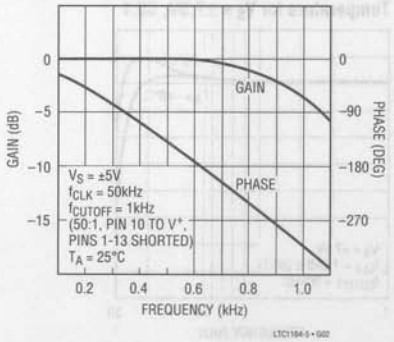
Note 3: All gains are measured relative to passband gain. The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



Passband Gain and Phase vs Frequency



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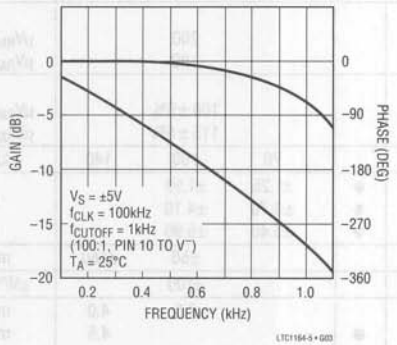
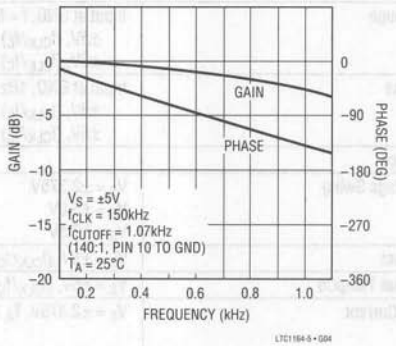
TYPICAL PERFORMANCE CHARACTERISTICS

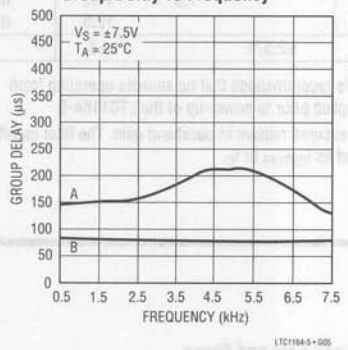
Passband Gain and Phase vs Frequency



Passband Gain and Phase vs Frequency

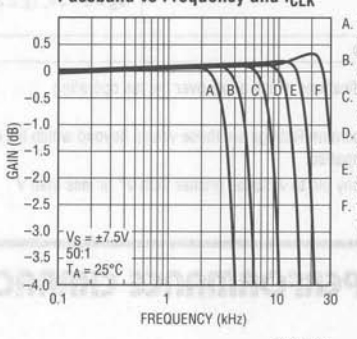


Group Delay vs Frequency



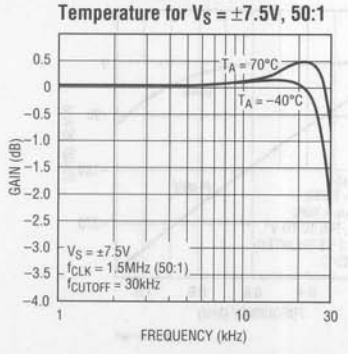
A. f_{CLK} = 500kHz (BUTTERWORTH 100:1) f_{CUTOFF} = 5kHz
B. f_{CLK} = 750kHz (BESSEL 140:1) f_{CUTOFF} = 5.36kHz

Passband vs Frequency and f_{CLK}

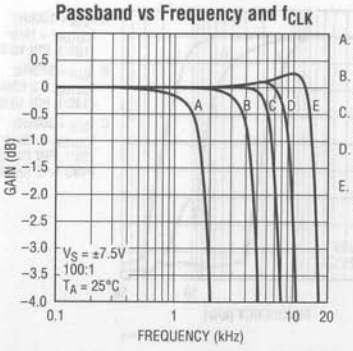


A. f_{CLK} = 200kHz f_{CUTOFF} = 4kHz
B. f_{CLK} = 300kHz f_{CUTOFF} = 6kHz
C. f_{CLK} = 500kHz f_{CUTOFF} = 10kHz
D. f_{CLK} = 750kHz f_{CUTOFF} = 15kHz
E. f_{CLK} = 1MHz f_{CUTOFF} = 20kHz
F. f_{CLK} = 1.5MHz f_{CUTOFF} = 30kHz

Maximum Passband over Temperature for V_S = ±7.5V, 50:1



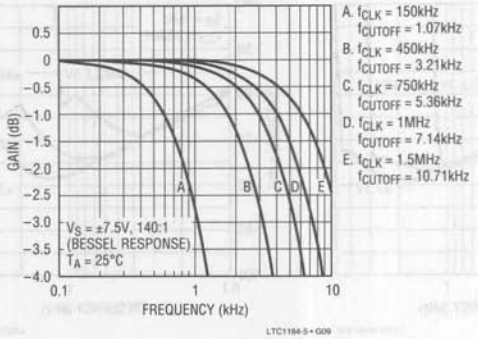
Passband vs Frequency and f_{CLK}



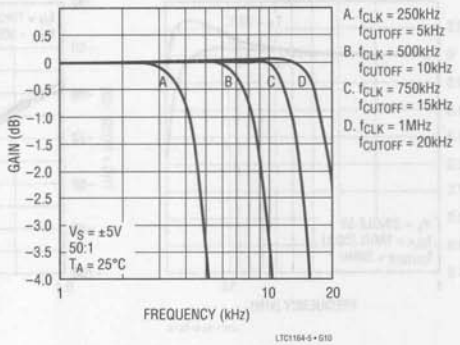
A. f_{CLK} = 200kHz f_{CUTOFF} = 2kHz
B. f_{CLK} = 500kHz f_{CUTOFF} = 5kHz
C. f_{CLK} = 750kHz f_{CUTOFF} = 7.5kHz
D. f_{CLK} = 1MHz f_{CUTOFF} = 10kHz
E. f_{CLK} = 1.5MHz f_{CUTOFF} = 15kHz

TYPICAL PERFORMANCE CHARACTERISTICS

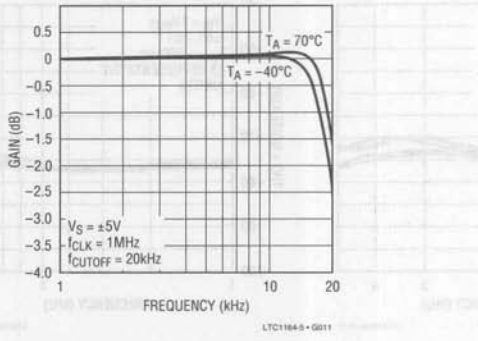
Passband vs Frequency and f_{CLK}



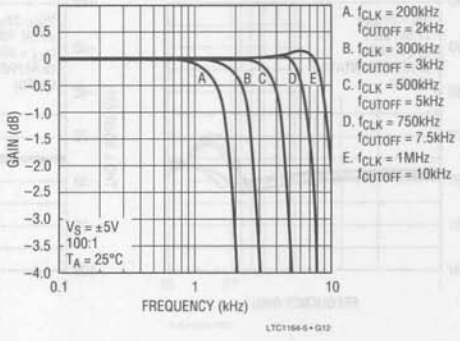
Passband vs Frequency and f_{CLK}



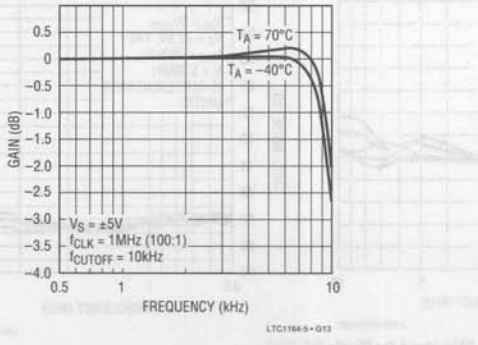
Maximum Passband over Temperature for V_S = ±5V, 50:1



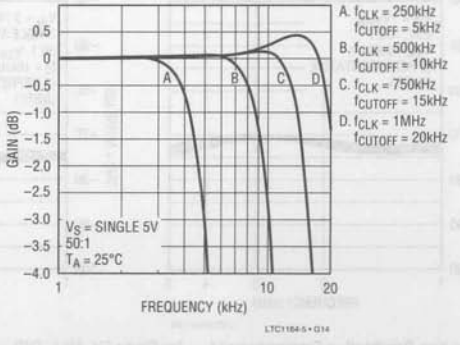
Passband vs Frequency and f_{CLK}



Maximum Passband over Temperature for V_S = ±5V, 100:1



Passband vs Frequency and f_{CLK}



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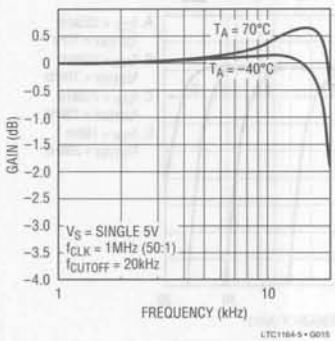
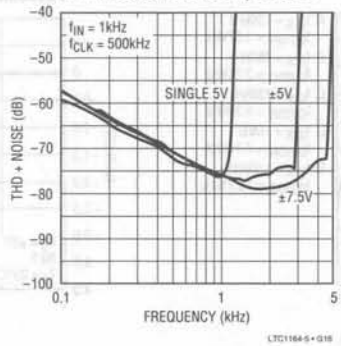
TYPICAL PERFORMANCE CHARACTERISTICS

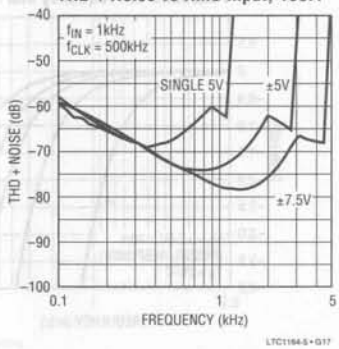
Maximum Passband over Temperature for Single 5V, 50:1*



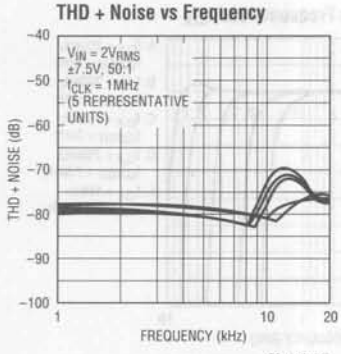
THD + Noise vs RMS Input, 50:1



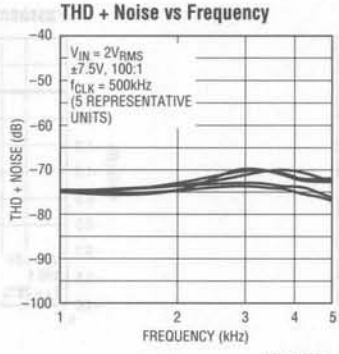
THD + Noise vs RMS Input, 100:1



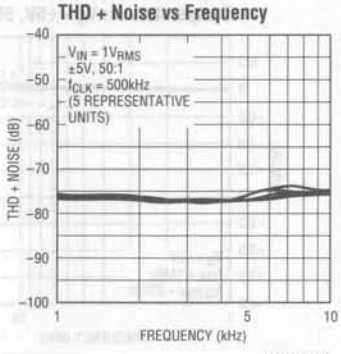
THD + Noise vs Frequency



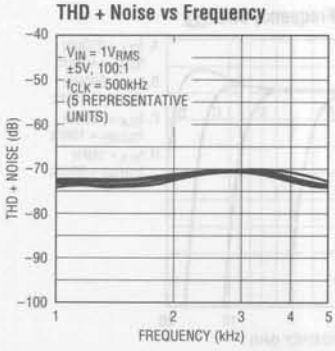
THD + Noise vs Frequency



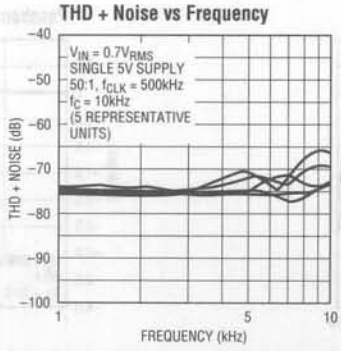
THD + Noise vs Frequency



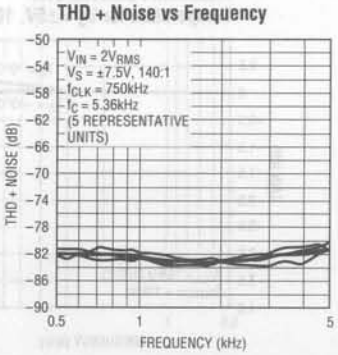
THD + Noise vs Frequency



THD + Noise vs Frequency



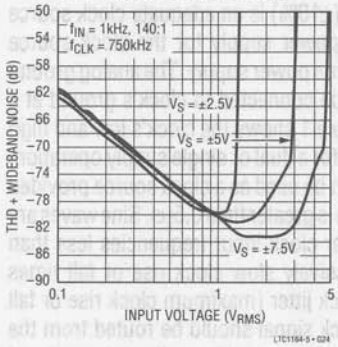
THD + Noise vs Frequency



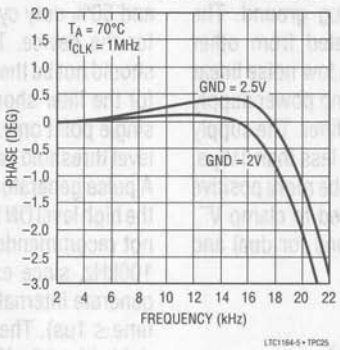
* See also Passband vs Frequency and f_{CLK} for Single 5V, 50:1; THD + Noise vs RMS Input for Single 5V, 50:1; and Maximum Passband for Single 5V, 50:1, for Two Ground Bias Levels.

TYPICAL PERFORMANCE CHARACTERISTICS

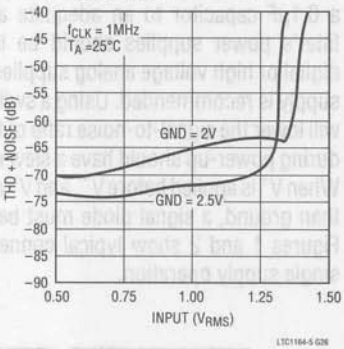
THD + Noise vs Input Voltage



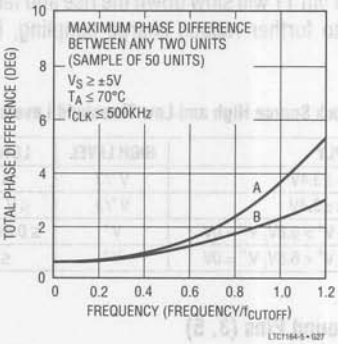
Maximum Passband for Single 5V, 50:1, for Two Ground Bias Levels



THD + Noise vs RMS Input for Single 5V, 50:1

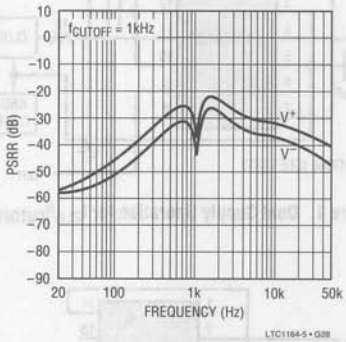


Phase Matching vs Frequency

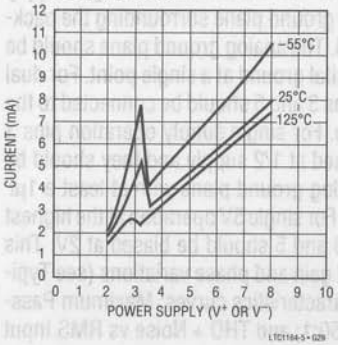


A. BUTTERWORTH (f_{CLK}/f_{CUTOFF} = 100:1 OR 50:1)
B. BESSEL (f_{CLK}/f_{CUTOFF} = 140:1)

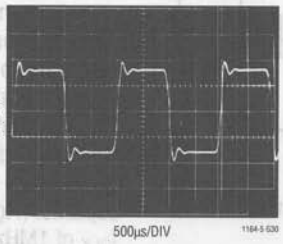
Power Supply Rejection Ratio vs Frequency



Power Supply Current vs Power Supply Voltage

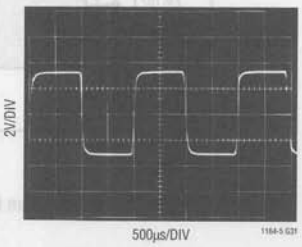


Transient Response V_{IN} = ±3V, 500Hz Square Wave



BUTTERWORTH RATIO = 100:1
f_{CLK} = 500kHz
f_C = 5kHz
V_S = ±7.5V

Transient Response V_{IN} = ±3V, 500Hz Square Wave



BESSEL RATIO = 140:1
f_{CLK} = 700kHz
f_C = 5kHz
V_S = ±7.5V

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PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^-, and V^- can be more positive than ground, a signal diode must be used to clamp V^-. Figures 1 and 2 show typical connections for dual and single supply operation.

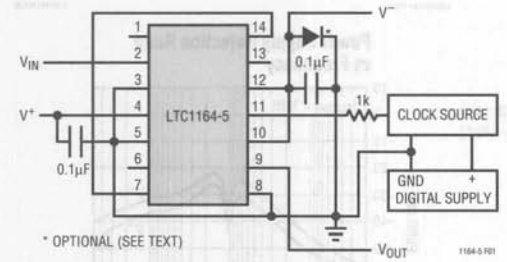


Figure 1. Dual Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

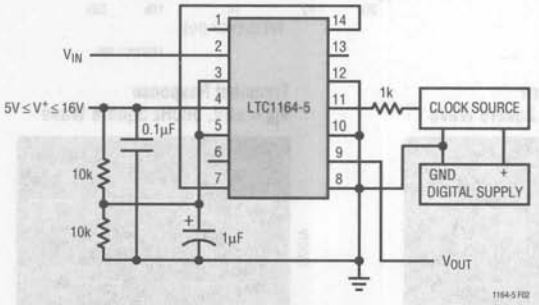


Figure 2. Single Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold value for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling, Figures 1 and 2.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply > ±3.4V	$V^+/3$	≤ 0.5V
Dual Supply ≤ ±3.4V	$V^+/3$	≤ V^- + 0.5V
Single Supply V^+ > 6.8V, V^- = 0V	V^+	≤ 0.5V + 1/2V^+
Single Supply V^+ < 6.8V, V^- = 0V	V^+	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation pins 3 and 5 should be biased at 1/2 supply and they should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 2). For single 5V operation at the highest f_{CLK} of 1MHz, pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations (see Typical Performance Characteristics curves: Maximum Passband for Single 5V, 50:1; and THD + Noise vs RMS Input for Single 5V, 50:1).

PIN FUNCTIONS

Butterworth/Bessel Pin (10)

The DC level at pin 10 determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and a Butterworth response (pins 1 to 13 are shorted for 50:1 only). Pin 10 at V^- gives a 100:1 Butterworth response. Pin 10 at ground gives a Bessel response and a ratio of 140:1. For single supply operation the ratio is 50:1 when pin 10 is at V^+ (pins 1 to 13 shorted), 100:1 when pin 10 is at ground, and 140:1 when at 1/2 supply. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1μF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/μs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 100k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source or sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 3, can be used provided that its input common mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

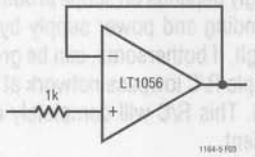


Figure 3. Buffer for Filter Output

External Connection Pins (7, 14, and 1, 13)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane. When the clock to cutoff frequency ratio is set at 50:1, pin 1 should be shorted to pin 13; if not, the passband will exhibit 1dB of gain peaking and it will deviate from a Butterworth response. Pin 1 is the inverting input of an internal op amp and it should preferably be 0.2 inches away from any other circuit trace.

NC Pin (8)

Pin 8 is not connected to any internal circuit point on the device and should be preferably tied to analog ground.

8

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as, the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and, it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown on Table 2.

Table 2. Output Clock Feedthrough

V_S	50:1	100:1
±2.5V	$60\mu V_{RMS}$	$60\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$150\mu V_{RMS}$	$500\mu V_{RMS}$

Note: The clock feedthrough at ±2.5V supplies is imbedded in the wideband noise of the filter. The clock waveform is a square wave.

APPLICATIONS INFORMATION

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transient.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1164-5 wideband noise at ±2.5V supply is 100μV_{RMS}, 95μV_{RMS} of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μRMS) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LTC1164-5 optimizes AC performance versus power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown on Table 3.

Table 3. Maximum V_{IN} vs V_S and f_{CLK}

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
V_S = ±7.5V	1.5MHz	$1V_{RMS}$ (f_{IN} > 35kHz) $0.5V_{RMS}$ (f_{IN} > 250kHz)
V_S = ±7.5V	1.0MHz	$3V_{RMS}$ (f_{IN} > 25kHz) $0.7V_{RMS}$ (f_{IN} > 250kHz)
V_S = ±5.0V	1.0MHz	$2.5V_{RMS}$ (f_{IN} > 25kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)
Single 5V	1.0MHz	$0.7V_{RMS}$ (f_{IN} > 25kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-5 case at 100:1, an input signal whose frequency is in the range of f_{CLK} ±2.5% will be aliased back into the filter's passband. If, for instance, an LTC1164-5 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz 10mV input signal, a 2kHz 56μV alias signal will appear at its output. When the LTC1164-5 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 4 shows details.

Table 4. Aliasing Data (f_{CLK} = 100kHz, V_S = ±5V)

INPUT FREQUENCY (V_{IN} = $1V_{RMS}$)	OUTPUT LEVEL (Relative to Input)	OUTPUT FREQUENCY (Aliased Frequency)
(f_{CLK}/f_C) = 100:1, f_{CUTOFF} = 1kHz		
97.0kHz	–102.0dB	3.0kHz
97.5kHz	–65.0dB	2.5kHz
98.0kHz	–45.0dB	2.0kHz
98.5kHz	–23.0dB	1.5kHz
99.0kHz	–4.0dB	1.0kHz
99.5kHz	–0.3dB	0.5kHz
(f_{CLK}/f_C) = 50:1, f_{CUTOFF} = 2kHz		
197.0kHz	–23.0dB	3.0kHz
197.5kHz	–12.0dB	2.5kHz
198.0kHz	–5.0dB	2.0kHz
198.5kHz	–1.8dB	1.5kHz
199.0kHz	–1.0dB	1.0kHz
199.5kHz	–0.8dB	0.5kHz

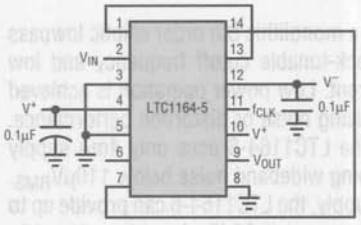
Table 5. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

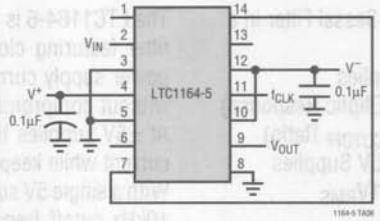
* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

TYPICAL APPLICATIONS

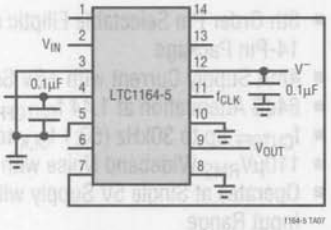
8th Order Butterworth Lowpass Filter
f_{CLK}/f_C = 50:1



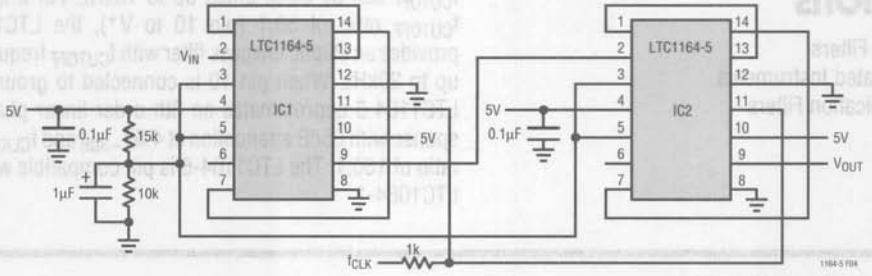
8th Order Butterworth Lowpass Filter
f_{CLK}/f_C = 100:1



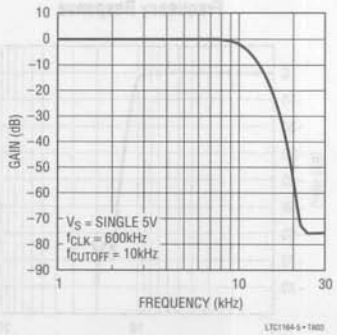
8th Order Linear Phase Lowpass Filter
f_{CLK}/f_C = 140:1



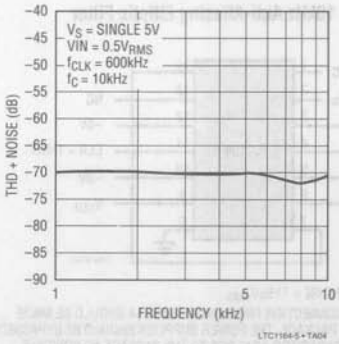
Single 5V, I_S = 5.2mA, 16th Order Clock-Tunable Lowpass Filter,
f_{CLK}/f_{CUTOFF} = 60:1, –75dB Attenuation at 2.3 f_{CUTOFF}



Gain vs Frequency



THD + Noise vs Frequency



8

Low Power 8th Order Pin Selectable Elliptic or Linear Phase Lowpass Filter

FEATURES

- 8th Order Pin Selectable Elliptic or Bessel Filter in a 14-Pin Package
- 4mA Supply Current with ±5V Supplies
- 64dB Attenuation at 1.44 f_{CUTOFF} (Elliptic Response)
- f_{CUTOFF} up to 30kHz (50:1 f_{CLK} to f_{CUTOFF} Ratio)
- 110μV_{RMS} Wideband Noise with ±5V Supplies
- Operates at Single 5V Supply with 1V_{RMS} Input Range
- Operates up to ±8V Supplies
- TTL/CMOS Compatible Clock Input
- No External Components

APPLICATIONS

- Anti-Aliasing Filters
- Battery-Operated Instruments
- Telecommunication Filters

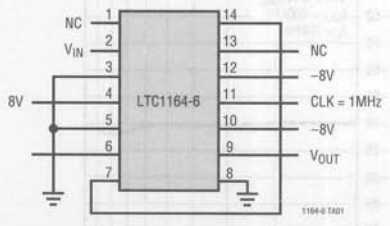
DESCRIPTION

The LTC1164-6 is a monolithic 8th order elliptic lowpass filter featuring clock-tunable cutoff frequency and low power supply current. Low power operation is achieved without compromising noise or distortion performance. At ±5V supplies the LTC1164-6 uses only 4mA supply current while keeping wideband noise below 110μV_{RMS}. With a single 5V supply, the LTC1164-6 can provide up to 10kHz cutoff frequency and 80dB signal-to-noise ratio while consuming only 2.5mA.

The LTC1164-6 provides an elliptic lowpass rolloff with stopband attenuation of 64dB at 1.44 f_{CUTOFF} and an f_{CLK}-to-f_{CUTOFF} ratio of 100:1 (pin 10 to V^-). For a ratio of 100:1, f_{CUTOFF} can be clock-tuned up to 10kHz. For a f_{CLK}-to-f_{CUTOFF} ratio of 50:1 (pin 10 to V^+), the LTC1164-6 provides an elliptic lowpass filter with f_{CUTOFF} frequencies up to 20kHz. When pin 10 is connected to ground, the LTC1164-6 approximates an 8th order linear phase response with 65dB attenuation at 4.5 f_{-3dB} and f_{CLK}/f_{-3dB} ratio of 160:1. The LTC1164-6 is pin compatible with the LTC1064-1.

TYPICAL APPLICATION

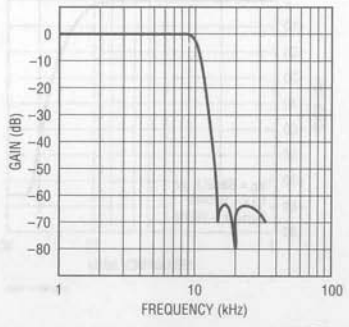
10kHz Anti-Aliasing Elliptic Filter



WIDEBAND NOISE = 115μV_{RMS}

NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

Frequency Response

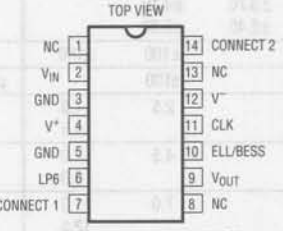


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V

Operating Temperature Range
LTC1164-6C ..... –40°C to 85°C
LTC1164-6M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



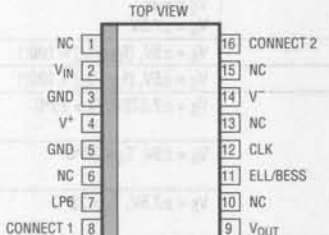
J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER

LTC1164-6CN
LTC1164-6CJ
LTC1164-6MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1164-6CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CLK} = 400kHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified. (f_{CLK}/f_{CUTOFF}) = 4kHz at 100:1 and 8kHz at 50:1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain 0.1Hz to 0.25 f_{CUTOFF} (Note 4)	f_{IN} = 1kHz, (f_{CLK}/f_C) = 100:1	●	–0.50	–0.15	0.25	dB
Passband Ripple with V_S = Single 5V	1Hz to 0.8 f_C (Table 2)			0.1 to –0.3		dB
Gain at 0.50 f_{CUTOFF} (Note 3)	f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1	●	–0.45	–0.10	0.10	dB
Gain at 0.90 f_{CUTOFF} (Note 3)	f_{IN} = 3.6kHz, (f_{CLK}/f_C) = 100:1	●	–0.75	–0.30	0.10	dB
Gain at 0.95 f_{CUTOFF} (Note 3)	f_{IN} = 3.8kHz, (f_{CLK}/f_C) = 100:1	●	–1.40	–0.70	–0.40	dB
Gain at f_{CUTOFF} (Note 3)	f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1	●	–3.50	–2.70	–2.30	dB
	f_{IN} = 8kHz, (f_{CLK}/f_C) = 50:1	●	–3.00	–2.10	–1.50	dB
Gain at 1.44 f_{CUTOFF} (Note 3)	f_{IN} = 5.76kHz, (f_{CLK}/f_C) = 100:1	●	–69	–64	–58	dB
Gain at 2.0 f_{CUTOFF} (Note 3)	f_{IN} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–69	–64	–58	dB
Gain with f_{CLK} = 20kHz	f_{IN} = 200Hz, (f_{CLK}/f_C) = 100:1		–3.50	–2.70	–2.30	dB
Gain with V_S = ±2.375V	f_{IN} = 400kHz, f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1		–0.50	–0.10	0.30	dB
	f_{IN} = 400kHz, f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1		–3.30	–2.50	–2.00	dB
Input Frequency Range (Tables 3, 4)	(f_{CLK}/f_C) = 100:1			0 – <f_{CLK}/2		kHz
	(f_{CLK}/f_C) = 50:1			0 – <f_{CLK}		kHz
Maximum f_{CLK} (Table 3)	V_S ≥ ±7.5V			1.5		MHz
	V_S ≤ ±5V			1.0		MHz
	V_S = Single 5V, AGND = 2V			1.0		MHz

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ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $R_L = 10k$, $T_A = 25°C$, $f_{CLK} = 400kHz$, TTL or CMOS level (maximum clock rise or fall time $\leq 1\mu s$) and all gain measurements are referenced to passband gain, unless otherwise specified. (f_{CLK}/f_{CUTOFF}) = 4kHz at 100:1 and 8kHz at 50:1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Feedthrough	Input at GND, f = f_{CLK}, Square Wave					
	$V_S = \pm 7.5V$, (f_{CLK}/f_C) = 100:1			500		μV_{RMS}
	$V_S = \pm 5V$, (f_{CLK}/f_C) = 50:1			200		μV_{RMS}
Wideband Noise	Input at GND, $1Hz \leq f < f_{CLK}$					
	$V_S = \pm 7.5V$			115 ± 5%		μV_{RMS}
	$V_S = \pm 2.5V$			100 ± 5%		μV_{RMS}
Input Impedance			45	75	110	kΩ
Output DC Voltage Swing	$V_S = \pm 2.375V$	●	±1.25	±1.50		V
	$V_S = \pm 5V$	●	±3.70	±4.10		V
	$V_S = \pm 7.5V$	●	±5.40	±5.90		V
Output DC Offset	$V_S = \pm 5V$, (f_{CLK}/f_C) = 100:1			±100	±160	mV
Output DC Offset TempCo	$V_S = \pm 5V$, (f_{CLK}/f_C) = 100:1			±100		µV/°C
Power Supply Current	$V_S = \pm 2.375V$, $T_A > 25°C$			2.5	4.0	mA
		●			4.5	mA
	$V_S = \pm 5V$, $T_A > 25°C$			4.5	7.0	mA
		●			8.0	mA
	$V_S = \pm 7.5V$, $T_A > 25°C$			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

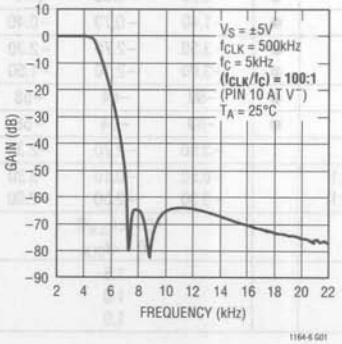
Note 2: Connecting any pin to voltages greater than V^+ or less than V^- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-6.

Note 3: All gains are measured relative to passband gain.

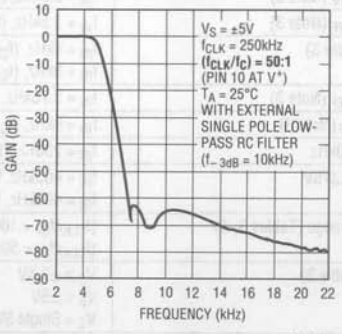
Note 4: The cutoff frequency of the filter is abbreviated as f_{CUTOFF} or f_C.

TYPICAL PERFORMANCE CHARACTERISTICS

Stopband Gain vs Frequency (Elliptic Response)

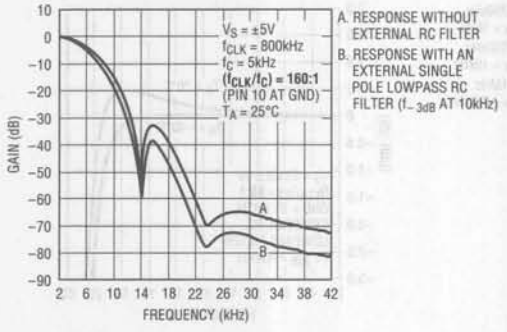


Stopband Gain vs Frequency (Elliptic Response)

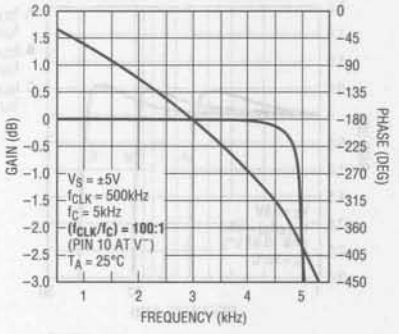


TYPICAL PERFORMANCE CHARACTERISTICS

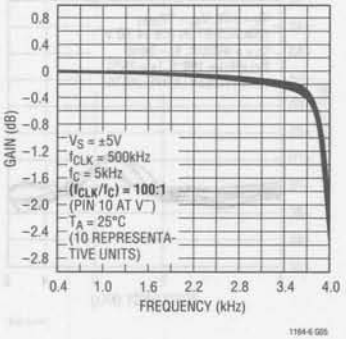
Stopband Gain vs Frequency (Linear Phase Response)



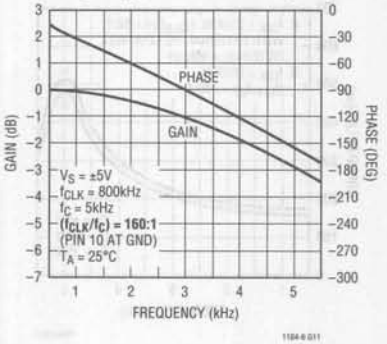
Passband Gain and Phase vs Frequency



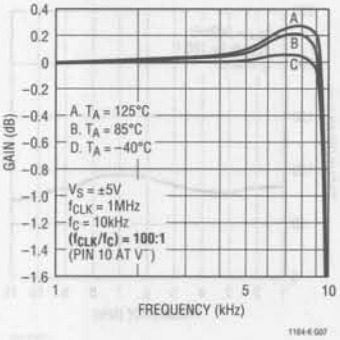
Passband Gain vs Frequency



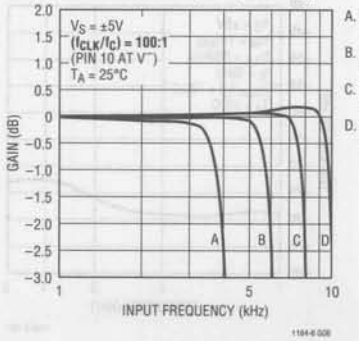
Passband Gain and Phase vs Frequency (Linear Phase Response)



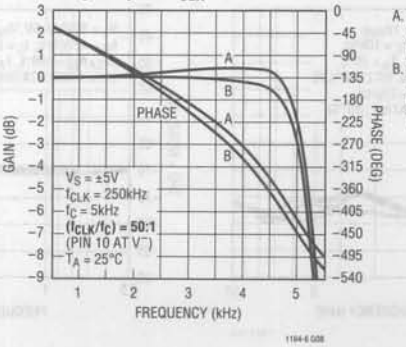
Maximum Passband over Temperature



Passband vs Frequency and f_{CLK}



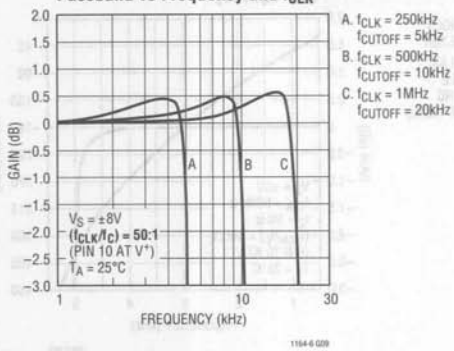
Passband Gain and Phase vs Frequency and f_{CLK}



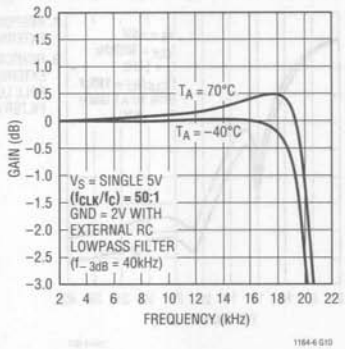
8

TYPICAL PERFORMANCE CHARACTERISTICS

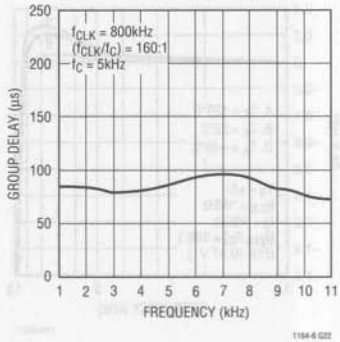
Passband vs Frequency and f_{CLK}



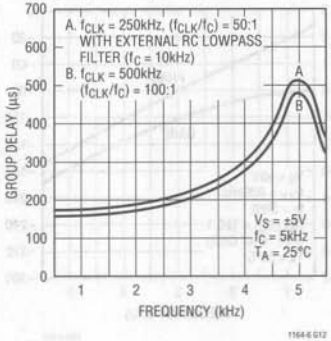
Maximum Passband over Temperature



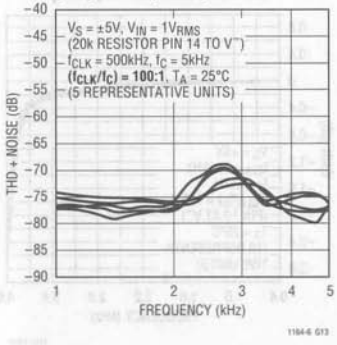
Group Delay vs Frequency (Linear Phase Response)



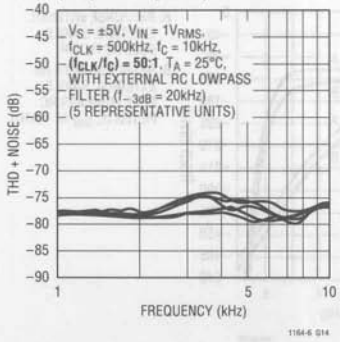
Group Delay vs Frequency (Elliptic Response)



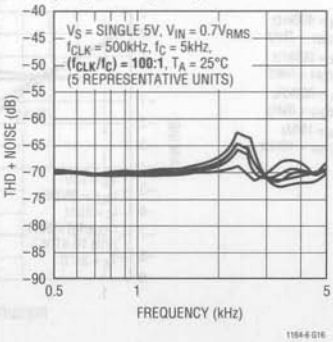
THD + Noise vs Frequency (Elliptic Response)



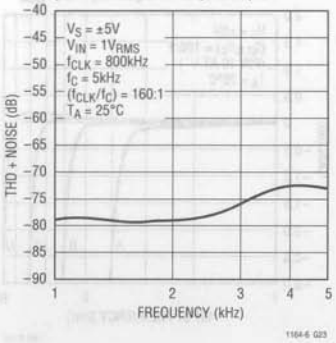
THD + Noise vs Frequency (Elliptic Response)



THD + Noise vs Frequency (Elliptic Response)

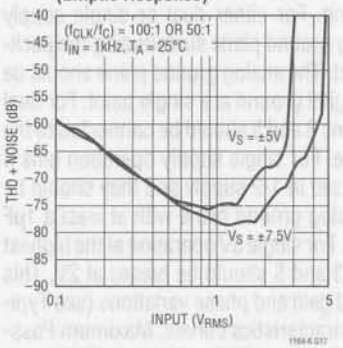


THD + Noise vs Frequency (Linear Phase Response)

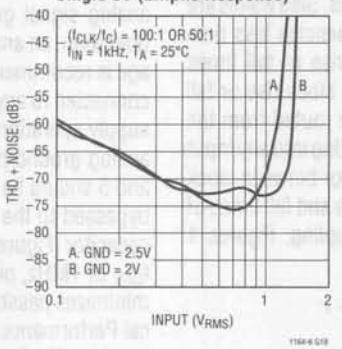


TYPICAL PERFORMANCE CHARACTERISTICS

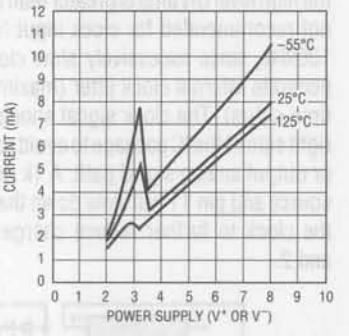
THD + Noise vs RMS Input (Elliptic Response)



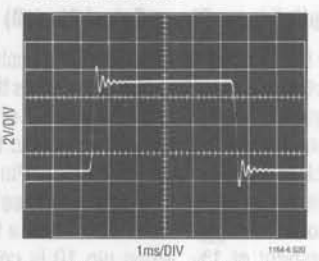
THD + Noise vs RMS Input for Single 5V (Elliptic Response)



Power Supply Current vs Power Supply Voltage

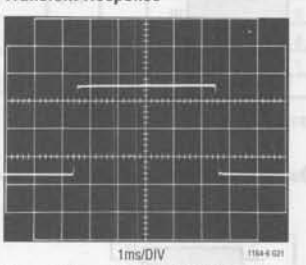


Transient Response



V_S = ±7.5V, V_{IN} = ±3V 100Hz SQUARE WAVE
f_{CLK} = 500kHz, (f_{CLK}/f_C) = 100:1, f_{CUTOFF} = 5kHz
ELLIPTIC RESPONSE

Transient Response



V_S = ±7.5V, V_{IN} = ±3V 100Hz SQUARE WAVE
f_{CLK} = 800kHz, (f_{CLK}/f_C) = 160:1, f_{CUTOFF} = 5kHz
LINEAR PHASE RESPONSE

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PIN FUNCTIONS (14-Lead Dual-In-Line Package)

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- could go above ground, a signal diode must be used to clamp V^-. Figures 1 and 2 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high

PIN FUNCTIONS (14-Lead Dual-In-Line Package)

level threshold value for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling, Figures 1 and 2.

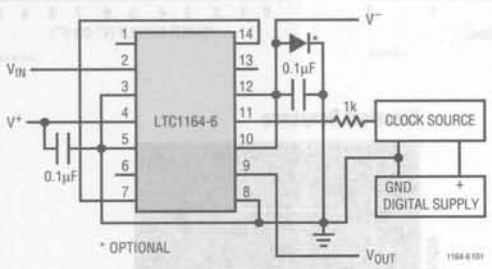

Figure 1. Dual Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

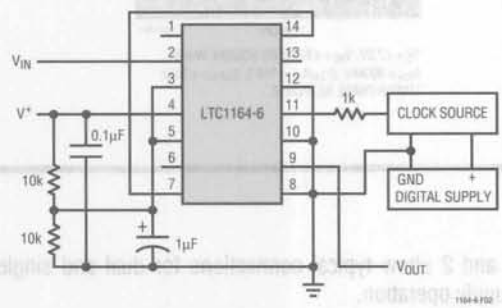

Figure 2. Single Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation pins 3 and 5 should be biased at 1/2 supply and they should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 2). For single 5V operation at the highest f_{CLK} of 1MHz, pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations (see Typical Performance Characteristics curves: Maximum Passband for Single 5V, 50:1; and THD + Noise vs RMS Input for Single 5V, 50:1).

Elliptic/Linear Phase Select Pin (10)

The DC level at this pin selects the desired filter response, elliptic or linear phase and determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 connected to V^- provides an elliptic lowpass filter with clock-to-f_{CUTOFF} ratio of 100:1. Pin 10 connected to analog ground provides a linear phase lowpass filter with a clock- to-f_{-3dB} ratio of 160:1 and a transient response overshoot of 1%. When pin 10 is connected to V^+ the clock-to-f_{CUTOFF} ratio is 50:1 and the filter response is elliptic. Bypassing pin 10 to analog ground reduces the output DC offsets. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source or sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 3,

PIN FUNCTIONS (14-Lead Dual-In-Line Package)

can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

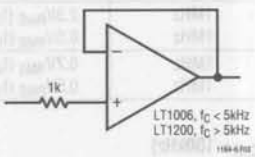

Figure 3. Buffer for Filter Output

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pin (1, 8, 13)

Pins 1, 8, and 13 are not connected to any internal circuit point on the device and should preferably be tied to analog ground.

APPLICATIONS INFORMATION

Passband Response

The passband response of the LTC1164-6 is optimized for a f_{CLK}/f_{CUTOFF} ratio of 100:1. Minimum passband ripple occurs from 1Hz to 80% of f_{CUTOFF}. Athough the passband of the LTC1164-6 is optimized for ratio f_{CLK}/f_{CUTOFF} of 100:1, if a ratio of 50:1 is desired, connect a single pole lowpass RC ($f_{-3dB} = 2\ f_{CUTOFF}$) at the output of the filter. The RC will make the passband gain response as flat as the 100:1 case. If the RC is omitted, and clock frequencies are below 500kHz the passband gain will peak by 0.4dB at 90% f_{CUTOFF}.

Table 2. Typical Passband Ripple with Single 5V Supply (f_{CLK}/f_C) = 100:1, GND = 2V, 30kHz, Fixed Single Pole, Lowpass RC Filter at Pin 9 (See Typical Applications)

PASSBAND FREQUENCY	PASSBAND GAIN (REFERENCED TO 0dB)			
	f_{CUTOFF} = 1kHz	f_{CUTOFF} = 10kHz		
% of f_{CUTOFF}	T_A = 25°C (dB)	T_A = 0°C (dB)	T_A = 25°C (dB)	T_A = 70°C (dB)
10	0.00	0.00	0.00	0.00
20	−0.02	0.00	0.01	0.01
30	−0.05	−0.01	−0.01	0.01
40	−0.10	−0.02	−0.02	0.02
50	−0.13	−0.03	−0.01	0.03
60	−0.15	−0.01	0.01	0.05
70	−0.18	−0.01	0.01	0.07
80	−0.25	−0.08	−0.05	0.02
90	−0.39	−0.23	−0.18	−0.05
f_{CUTOFF}	−2.68	−2.79	−2.74	−2.68

The gain peaking can approximate a $\sin\chi/\chi$ correction for some applications. (See Typical Performance Characteristics curve, Passband vs Frequency and f_{CLK} at f_{CLK}/f_C = 50:1.)

When the LTC1164-6 operates with a single 5V supply and its cutoff frequency is clock-tuned to 10kHz, an output single pole RC filter can also help maintain outstanding passband flatness from 0°C to 70°C. Table 2 shows details.

Clock Feedthrough

Clock feedthrough is defined as, the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and, it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 3.

Table 3. Clock Feedthrough

V_S	50:1	100:1
±2.5V	60μV_{RMS}	60μV_{RMS}
±5V	100μV_{RMS}	200μV_{RMS}
±7.5V	150μV_{RMS}	500μV_{RMS}

Note: The clock feedthrough at ±2.5V supplies is imbedded in the wideband noise of the filter. (The clock signal is a square wave.)

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APPLICATIONS INFORMATION

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transient.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1164-6 wideband noise at ±2.5V supply is 100μV_{RMS}, 90μV_{RMS} of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LTC1164-6 optimizes AC performance versus power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown on Table 4.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-6 case, an input signal whose frequency is in the range of f_{CLK} ±4%, will be aliased back into the filter's passband. If, for instance, an LTC1164-6 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98.5kHz, 10mV_{RMS} input signal, a 1.5kHz, 10μV_{RMS} alias signal will appear at its output. When the LTC1164-6 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 5 shows details.

Table 4. Maximum V_{IN} vs V_S and f_{CLK}

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	1.5MHz	$1V_{RMS}$ (f_{IN} > 35kHz)
	1MHz	$3V_{RMS}$ (f_{IN} > 25kHz)
	≥1MHz	$0.7V_{RMS}$ (f_{IN} > 250kHz)
±5V	1MHz	$2.5V_{RMS}$ (f_{IN} > 25kHz)
	1MHz	$0.5V_{RMS}$ (f_{IN} > 100kHz)
Single 5V	1MHz	$0.7V_{RMS}$ (f_{IN} > 25kHz)
	1MHz	$0.5V_{RMS}$ (f_{IN} > 100kHz)

Table 5. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = $1V_{RMS}$) (kHz)	OUTPUT LEVEL (Relative to Input) (dB)	OUTPUT FREQUENCY (Aliased Frequency) (kHz)
f_{CLK}/f_C = 100:1, f_{CUTOFF} = 1kHz		
96 (or 104)	−75.0	4.0
97 (or 103)	−68.0	3.0
98 (or 102)	−65.0	2.0
98.5 (or 101.5)	−60.0	1.5
99 (or 101)	−3.2	1.0
99.5 (or 100.5)	−0.5	0.5
f_{CLK}/f_C = 50:1, f_{CUTOFF} = 2kHz		
192 (or 208)	−76.0	8.0
194 (or 206)	−68.0	6.0
196 (or 204)	−63.0	4.0
198 (or 202)	−3.4	2.0
199 (or 201)	−1.3	1.0
199.5(or 200.5)	−0.9	0.5

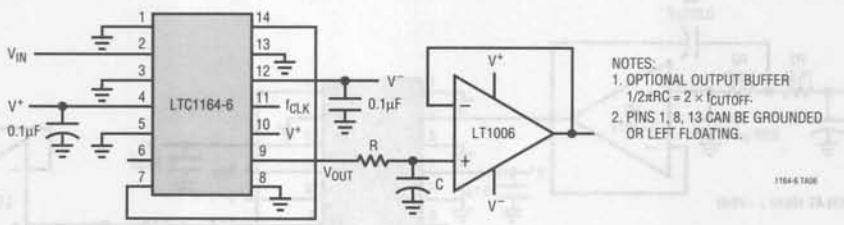
Table 6. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Linear Phase	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Linear Phase	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

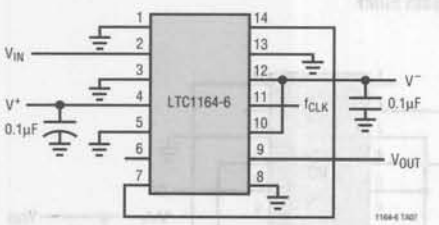
* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

TYPICAL APPLICATIONS

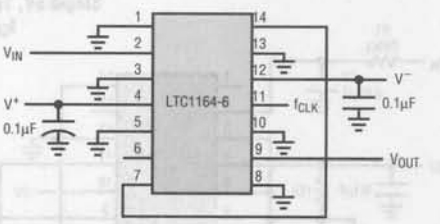
8th Order Elliptic Lowpass Filter
(f_{CLK}/f_C) = 50:1



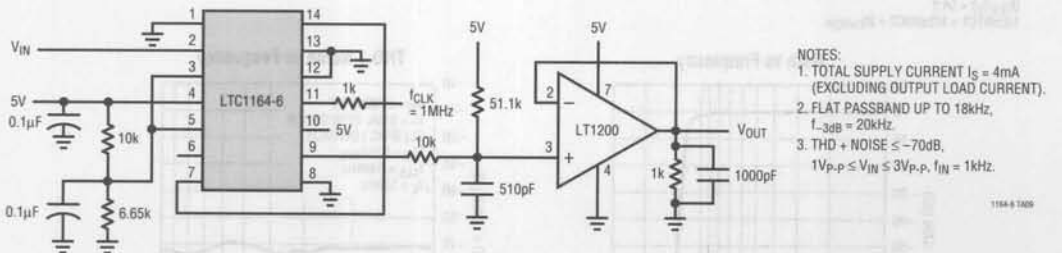
8th Order Elliptic Lowpass Filter
(f_{CLK}/f_C) = 100:1



8th Order Linear Phase Lowpass Filter
(f_{CLK}/f_C) = 160:1



8th Order 20kHz Cutoff, Elliptic Filter Operating with a Single 5V Supply and Driving 1k, 1000pF Load



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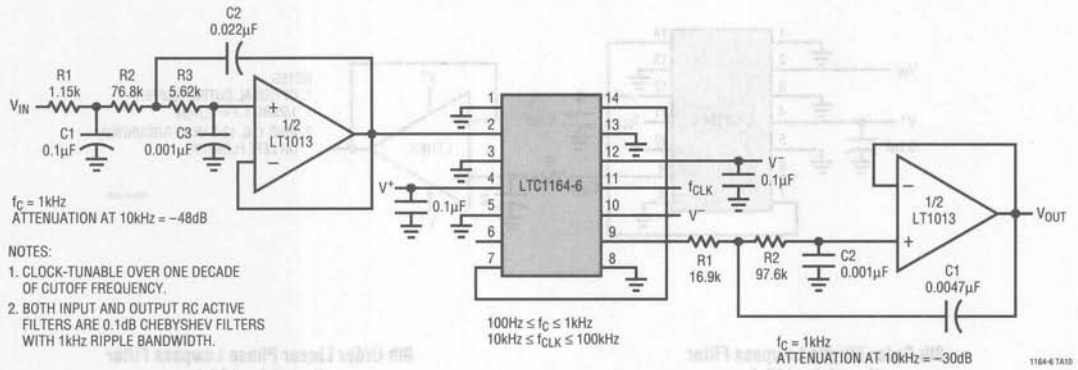
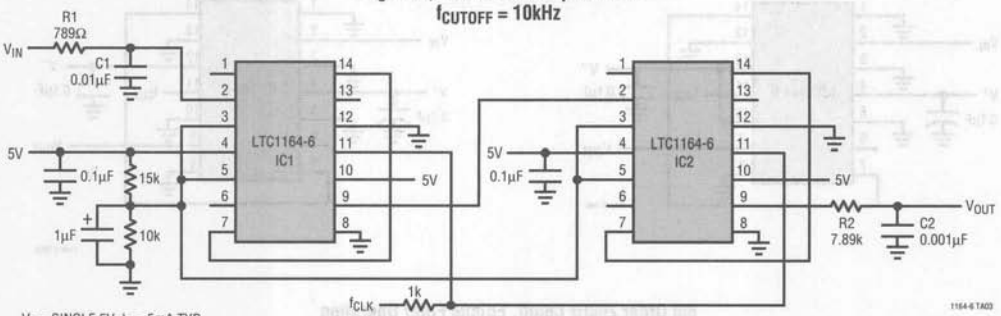
TYPICAL APPLICATIONS

8th Order Low Power, Clock-Tunable Elliptic Filter with Active RC Input Anti-Aliasing Filter and Output Smoothing Filter



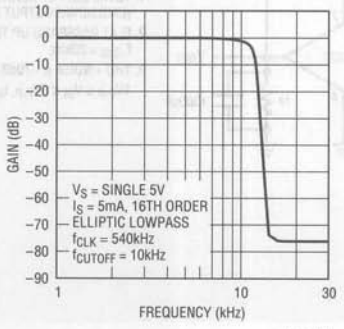
NOTES:
1. CLOCK-TUNABLE OVER ONE DECADE OF CUTOFF FREQUENCY.
2. BOTH INPUT AND OUTPUT RC ACTIVE FILTERS ARE 0.1dB CHEBYSHEV FILTERS WITH 1kHz RIPPLE BANDWIDTH.

Single 5V, 16th Order Lowpass Filter f_{CUTOFF} = 10kHz

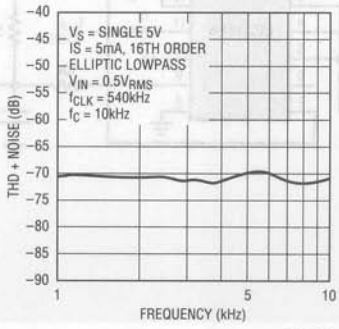


V_S = SINGLE 5V, I_S = 5mA TYP
16TH ORDER LOWPASS FILTER
FIXED f_{CUTOFF}, f_{CLK} = 540kHz
f_{CUTOFF} = 10kHz
(f_{CLK}/f_C) = 54:1
$1/2\pi R1C1 = 1/2\pi R2C2 = 2f_{CUTOFF}$

Gain vs Frequency



THD + Noise vs Frequency



Low Power, Linear Phase 8th Order Lowpass Filter

FEATURES

- Better Than Bessel Roll-Off
- f_{CUTOFF} up to 20kHz, Single 5V Supply
- I_{SUPPLY} = 2.5mA (Typ), Single 5V Supply
- 75dB THD + Noise with Single 5V Supply
- Phase and Group Delay Response Fully Tested
- Transient Response with No Ringing
- Wide Dynamic Range
- No External Components Needed

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase Matched Filters

DESCRIPTION

The LTC1164-7 is a low power, clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 34dB attenuation (vs12dB for Bessel), while at three times the cutoff frequency the filter attains 68dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1164-7 is tuned via an external TTL or CMOS clock.

Low power is achieved without sacrificing dynamic range. With single 5V supply, the S/N + THD is up to 75dB. Optimum 91dB S/N is obtained with ±7.5V supplies.

The clock-to-cutoff frequency ratio of the LTC1164-7 can be set to 50:1 (pin 10 to V^+) or 100:1 (pin 10 to V^-).

When the filter operates at the clock-to-cutoff frequency ratio of 50:1, the input is double-sampled to lower the risk of aliasing.

The LTC1164-7 is pin-compatible with the LTC1064-X series and LTC1264-7.

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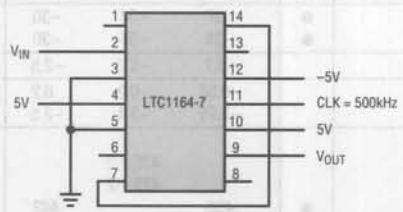
TYPICAL APPLICATION

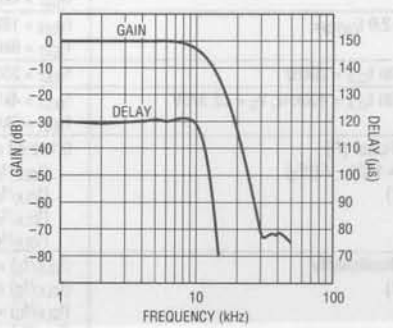
10kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

1164-7 TA01

Frequency Response



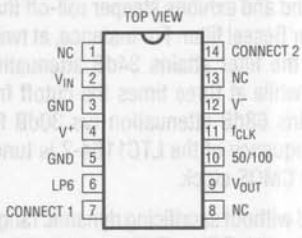
1164-7 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16V
Power Dissipation 400mW
Burn-In Voltage 16V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1164-7C ..... –40°C to 85°C
LTC1164-7M ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



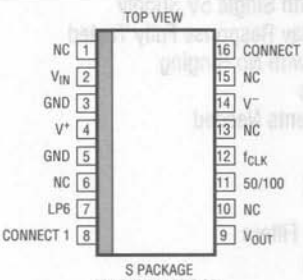
J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER

LTC1164-7CN
LTC1164-7CJ
LTC1164-7MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1164-7CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 8kHz or 4kHz, f_{CLK} = 400kHz, TTL or CMOS level and all gain measurements are referenced to passband gain, unless otherwise specified. (Maximum clock rise or fall time ≤ 1µs)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF}					
	f_{TEST} = 2kHz, (f_{CLK}/f_C) = 50:1 (Note 4)	●	–0.50	–0.10	0.30	dB
Gain at 0.50 f_{CUTOFF} (Note 3)	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1	●	–0.50	–0.20	0.30	dB
	f_{TEST} = 2kHz, (f_{CLK}/f_C) = 100:1	●	–0.85	–0.65	0.15	dB
Gain at 0.75 f_{CUTOFF}	f_{TEST} = 6kHz, (f_{CLK}/f_C) = 50:1	●	–1.2	–1.1	0.1	dB
Gain at f_{CUTOFF}	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1	●	–4.1	–3.4	–1.9	dB
	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 100:1	●	–5.5	–5.2	–2.5	dB
Gain at 2.0 f_{CUTOFF}	f_{TEST} = 16kHz, (f_{CLK}/f_C) = 50:1	●	–37	–34	–30	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–38	–34	–30	dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 100:1		–5.7	–5.2	–2.5	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1		–0.50	–0.2	0.2	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1		–3.75	–3.4	–2.5	dB
Phase Factor (F) Phase = 180° – F(f/f_C) (Note 1)	0.1Hz ≤ f ≤ f_{CUTOFF}					
	(f_{CLK}/f_C) = 50:1			435 ± 2		Deg
	(f_{CLK}/f_C) = 100:1			428 ± 2		Deg
	(f_{CLK}/f_C) = 50:1	●	430		442	Deg
	(f_{CLK}/f_C) = 100:1	●	423		434	Deg
Phase Nonlinearity (Note 1)	(f_{CLK}/f_C) = 50:1			±1.0		%
	(f_{CLK}/f_C) = 100:1			±1.0		%
	(f_{CLK}/f_C) = 50:1	●			±2.0	%
	(f_{CLK}/f_C) = 100:1	●			±2.5	%

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $R_L = 10k$, $T_A = 25°C$, $f_{CUTOFF} = 8kHz$ or $4kHz$, $f_{CLK} = 400kHz$, TTL or CMOS level and all gain measurements are referenced to passband gain, unless otherwise specified. (Maximum clock rise or fall time $\leq 1\mu s$)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay (t_d)	$(f_{CLK}/f_C) = 50:1$, $f \geq f_{CUTOFF}$			151.0 ± 1		μs
$t_d = (1/360)(f/f_C)$	$(f_{CLK}/f_C) = 100:1$, $f \geq f_{CUTOFF}$			297.2 ± 1		μs
(Note 2)	$(f_{CLK}/f_C) = 50:1$, $f \geq f_{CUTOFF}$	●	149.3		153.5	μs
	$(f_{CLK}/f_C) = 100:1$, $f \geq f_{CUTOFF}$	●	293.8		301.4	μs
Group Delay Deviation	$(f_{CLK}/f_C) = 50:1$, $f \geq f_{CUTOFF}$			± 1.0		%
(Note 2)	$(f_{CLK}/f_C) = 100:1$, $f \geq f_{CUTOFF}$			± 1.0		%
	$(f_{CLK}/f_C) = 50:1$, $f \geq f_{CUTOFF}$	●			± 2.0	%
	$(f_{CLK}/f_C) = 100:1$, $f \geq f_{CUTOFF}$	●			± 2.5	%
Input Frequency Range (Table 9)	$(f_{CLK}/f_C) = 50:1$			$< f_{CLK}$		kHz
	$(f_{CLK}/f_C) = 100:1$			$< f_{CLK}/2$		kHz
Maximum f_{CLK}	V_S = Single 5V (Pins 3 and 5 at 2V)			1		MHz
	$V_S = \pm 5V$			1		MHz
	$V_S = \pm 7.5V$			1		MHz
Clock Feedthrough ($f = f_{CLK}$)	50:1, $\pm 5V$, Input at GND			100		μV_{RMS}
Wideband Noise	$V_S = \pm 2.5V$			$95 \pm 5\%$		μV_{RMS}
($1Hz \leq f < f_{CLK}$)	$V_S = \pm 5V$			$105 \pm 5\%$		μV_{RMS}
	$V_S = \pm 7.5V$			$115 \pm 5\%$		μV_{RMS}
Input Impedance			35	55	90	kΩ
Output DC Voltage Swing (Note 4)	$V_S = \pm 2.375V$		± 1.25	± 1.4		V
	$V_S = \pm 5V$	●	± 3.70	± 3.9		V
	$V_S = \pm 7.5V$	●	± 5.40	± 6.1		V
Output DC Offset	50:1, $V_S = \pm 5V$			± 100	± 220	mV
	100:1, $V_S = \pm 5V$			± 100		mV
Output DC Offset TempCo	50:1, $V_S = \pm 5V$			± 200		$\mu V/°C$
	100:1, $V_S = \pm 5V$			± 200		$\mu V/°C$
Power Supply Current	$V_S = \pm 2.375V$, $T_A = 25°C$			2.5	4.0	mA
		●			4.5	mA
	$V_S = \pm 5V$, $T_A = 25°C$			4.5	7.0	mA
		●			8.0	mA
	$V_S = \pm 7.5V$, $T_A = 25°C$			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			± 2.375		± 8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as $f \leq f_C$; f_C = cutoff frequency.

Figure 1 curve shows the typical phase response of an LTC1164-7 operating at $f_{CLK} = 400kHz$, $f_C = 8kHz$ and it closely matches an ideal straight line. The phase shift is described by: phase shift = $180° - F(f/f_C)$; $f \leq f_C$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency. Example: The phase shift at 7kHz of the LTC1164-7 shown in Figure 1 is: phase shift = $180° - 434°$ (7kHz/10kHz) ± nonlinearity = $-123.8° \pm 1\%$ or $-123.9° \pm 1.24°$.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 4: The AC swing is typically $11V_{P-P}$, $7V_{P-P}$, $2.8V_{P-P}$ for $\pm 7.5V$, $\pm 5V$, $\pm 2.5V$ supply respectively. For more information refer to the THD + Noise vs Input graphs.

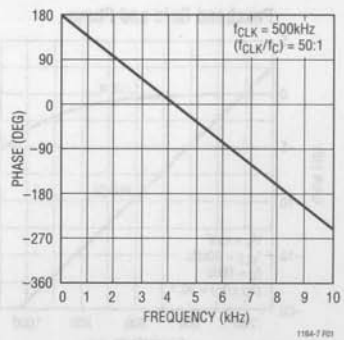
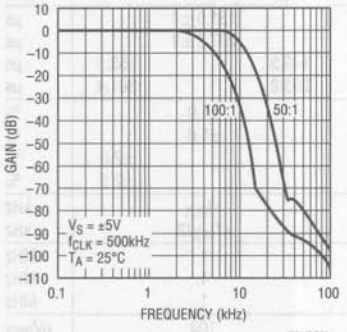


Figure 1. Phase Response in the Passband (Note 1)

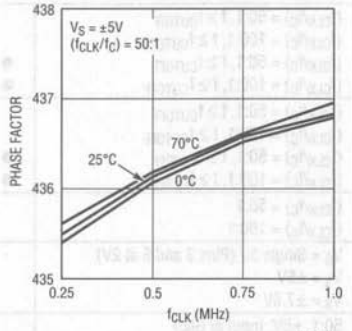
8

TYPICAL PERFORMANCE CHARACTERISTICS

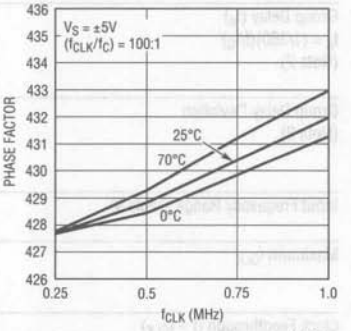
Gain vs Frequency



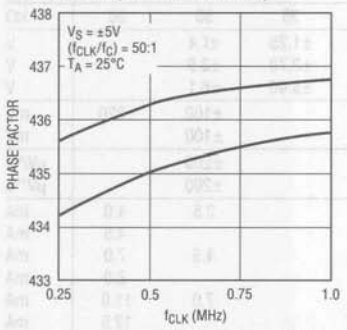
Phase Factor vs f_{CLK} (Typical Unit)



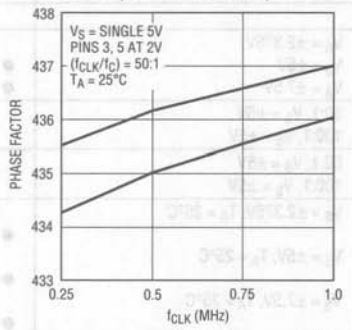
Phase Factor vs f_{CLK} (Typical Unit)



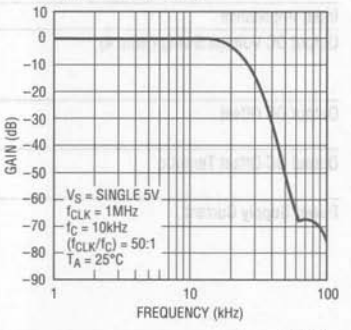
Phase Factor vs f_{CLK} (Min and Max Representative Units)



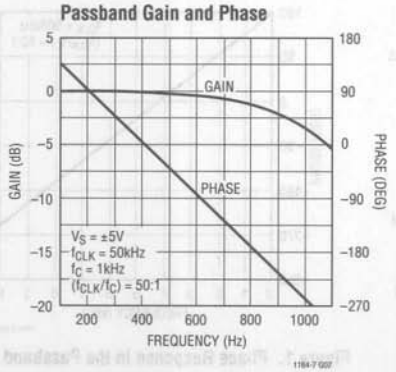
Phase Factor vs f_{CLK} (Min and Max Representative Units)



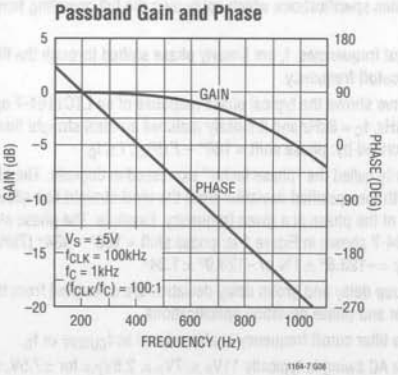
Gain vs Frequency



Passband Gain and Phase

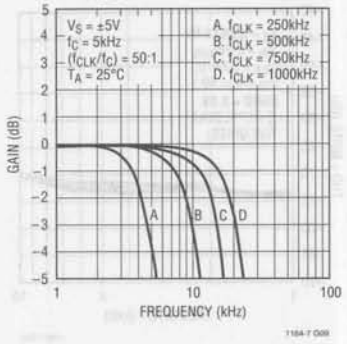


Passband Gain and Phase

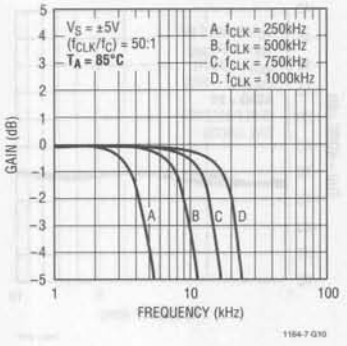


TYPICAL PERFORMANCE CHARACTERISTICS

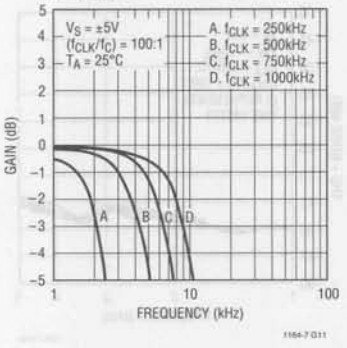
Passband Gain vs Frequency and f_{CLK}



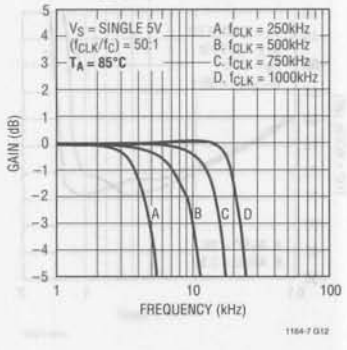
Passband Gain vs Frequency and f_{CLK}



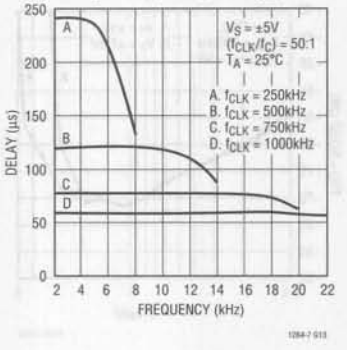
Passband Gain vs Frequency and f_{CLK}



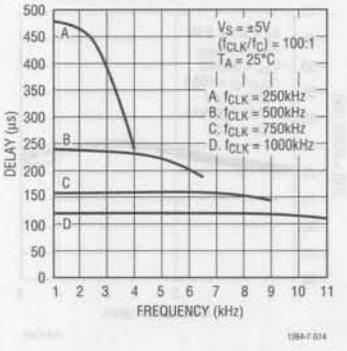
Passband Gain vs Frequency and f_{CLK}



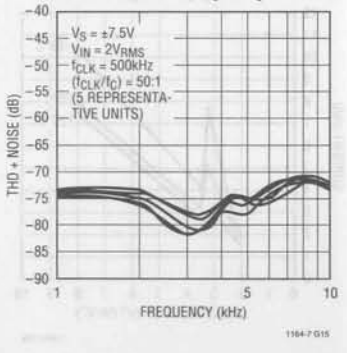
Delay vs Frequency and f_{CLK}



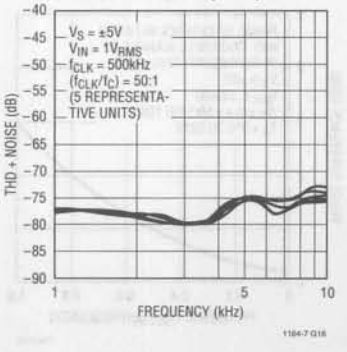
Delay vs Frequency and f_{CLK}



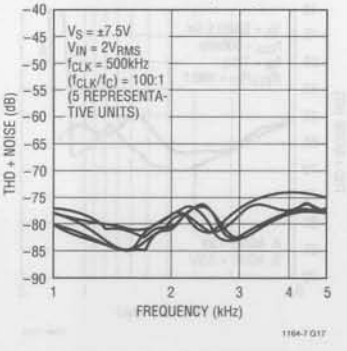
THD + Noise vs Frequency



THD + Noise vs Frequency



THD + Noise vs Frequency



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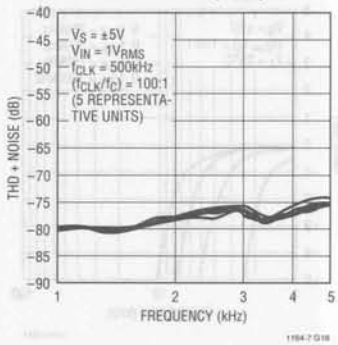
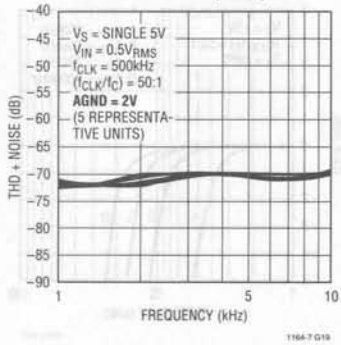
TYPICAL PERFORMANCE CHARACTERISTICS

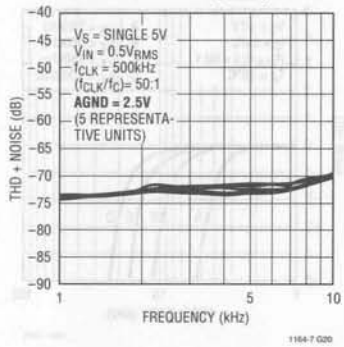
THD + Noise vs Frequency



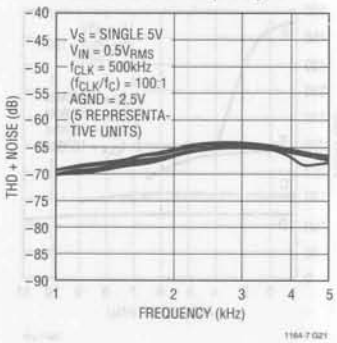
THD + Noise vs Frequency



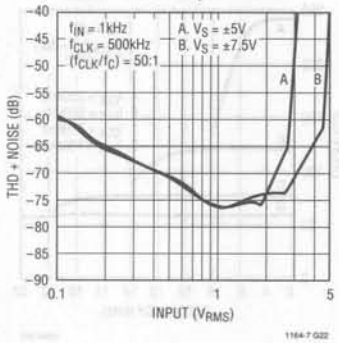
THD + Noise vs Frequency



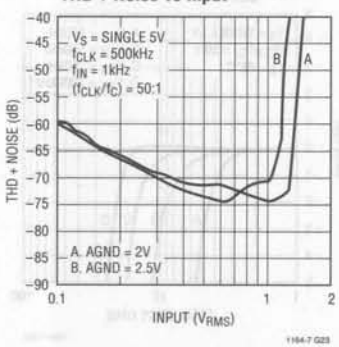
THD + Noise vs Frequency



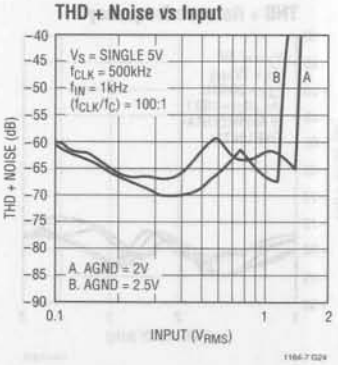
THD + Noise vs Input



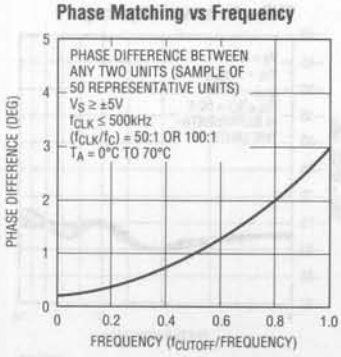
THD + Noise vs Input



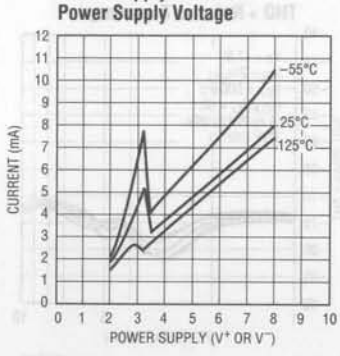
THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Table 1. Passband Gain and Phase
V_S = ±7.5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.085	180.00
1.250	−0.085	71.51
2.500	−0.261	−37.31
3.750	−1.092	−146.38
5.000	−3.647	−255.45
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.091	180.00
2.500	−0.091	71.36
5.000	−0.251	−37.57
7.500	−1.028	−146.78
10.000	−3.488	−256.16
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.106	180.00
3.750	−0.106	71.26
7.500	−0.264	−37.65
11.250	−0.943	−146.88
15.000	−3.206	−256.58
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.131	180.00
5.000	−0.131	71.11
10.000	−0.291	−37.71
15.000	−0.853	−146.87
20.000	−2.864	−256.81

Table 2. Passband Gain and Phase
V_S = ±7.5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.201	180.00
0.625	−0.201	71.39
1.250	−0.727	−36.79
1.875	−2.075	−143.66
2.500	−5.205	−247.79
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.176	180.00
1.250	−0.176	71.34
2.500	−0.645	−36.88
3.750	−1.945	−143.93
5.000	−5.032	−248.52
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.161	180.00
1.875	−0.161	71.32
3.750	−0.574	−37.04
5.625	−1.789	−144.45
7.500	−4.779	−249.82
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.157	180.00
2.500	−0.157	71.23
5.000	−0.538	−37.28
7.500	−1.666	−145.02
10.000	−4.527	−251.13

Table 3. Passband Gain and Phase
V_S = ±5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.071	180.00
1.250	−0.071	71.48
2.500	−0.243	−37.29
3.750	−1.068	−146.34
5.000	−3.609	−255.40
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.081	180.00
2.500	−0.081	71.35
5.000	−0.236	−37.52
7.500	−0.981	−146.71
10.000	−3.371	−256.13
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.105	180.00
3.750	−0.105	71.26
7.500	−0.261	−37.62
11.250	−0.883	−146.80
15.000	−3.008	−256.57
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.134	180.00
5.000	−0.134	70.99
10.000	−0.292	−37.75
15.000	−0.771	−146.83
20.000	−2.571	−256.88

Table 4. Passband Gain and Phase
V_S = ±5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.189	180.00
0.625	−0.189	71.39
1.250	−0.707	−36.75
1.875	−2.048	−143.60
2.500	−5.711	−247.74
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.159	180.00
1.250	−0.159	71.35
2.500	−0.603	−36.85
3.750	−1.872	−144.00
5.000	−4.926	−248.80
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.149	180.00
1.875	−0.149	71.28
3.750	−0.536	−37.13
5.625	−1.704	−144.72
7.500	−4.621	−250.48
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.151	180.00
2.500	−0.151	71.10
5.000	−0.511	−37.52
7.500	−1.581	−145.45
10.000	−4.336	−252.01

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TYPICAL PERFORMANCE CHARACTERISTICS

Table 5. Passband Gain and Phase
V_S = Single 5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.085	180.00
1.250	−0.085	71.54
2.500	−0.252	−37.15
3.750	−1.056	−146.12
5.000	−3.562	−255.22
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.101	180.00
2.500	−0.101	71.39
5.000	−0.251	−37.38
7.500	−0.947	−146.44
10.000	−3.252	−256.02
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.133	180.00
3.750	−0.133	71.16
7.500	−0.291	−37.56
11.250	−0.826	−146.55
15.000	−2.789	−256.52
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.162	180.00
5.000	−0.162	70.89
10.000	−0.307	−37.78
15.000	−0.647	−146.67
20.000	−2.201	−257.06

Table 6. Passband Gain and Phase
V_S = Single 5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	−0.283	180.00
0.625	−0.283	71.35
1.250	−0.799	−37.01
1.875	−2.143	−143.96
2.500	−5.271	−248.03
f_{CLK} = 500kHz (Typical Unit)		
0.000	−0.252	180.00
1.250	−0.252	71.28
2.500	−0.676	−37.16
3.750	−1.917	−144.46
5.000	−4.936	−249.40
f_{CLK} = 750kHz (Typical Unit)		
0.000	−0.231	180.00
1.875	−0.231	70.94
3.750	−0.603	−37.72
5.625	−1.704	−145.55
7.500	−4.535	−251.81
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.212	180.00
2.500	−0.212	70.83
5.000	−0.532	−38.11
7.500	−1.497	−146.47
10.000	−4.115	−253.92

PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 1k resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

PIN FUNCTIONS

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

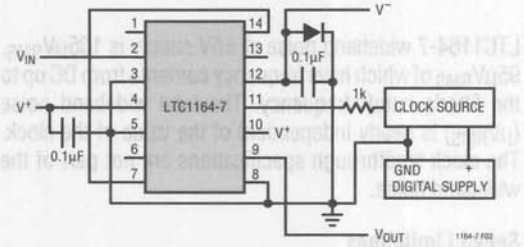

Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

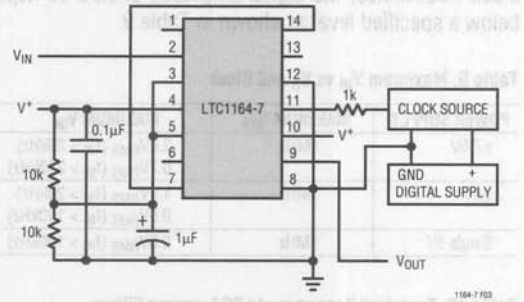

Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation, pins 3 and 5 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and pin 10 at V^- gives a 100:1 ratio. For single supply operation the ratio is 50:1 when pin 10 is at V^+ and 100:1 when pin 10 is at ground. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1µF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source/sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

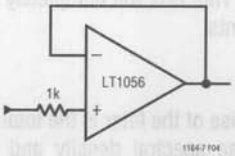

Figure 4. Buffer for Filter Output

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PIN FUNCTIONS

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pins (1, 8, 13)

Pins 1, 8 and 13 are not connected to any internal circuit point on the device and should be preferably tied to analog ground.

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	50:1	100:1
Single 5V	$70\mu V_{RMS}$	$70\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$500\mu V_{RMS}$

Note: The clock feedthrough at Single 5V is imbedded in the wideband noise of the filter. The clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter's passband and cannot be reduced with post filtering. For instance, the LTC1164-7 wideband noise at ±5V supply is $105\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LT1164-7 optimizes AC performance vs power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN} vs V_S and Clock

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	1MHz	$2.0V_{RMS}$ (f_{IN} > 20kHz) $0.7V_{RMS}$ (f_{IN} > 250kHz)
±5V	1MHz	$1.4V_{RMS}$ (f_{IN} > 20kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)
Single 5V	1MHz	$0.5V_{RMS}$ (f_{IN} > 100kHz)

Table 10. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

APPLICATIONS INFORMATION

Transient Response

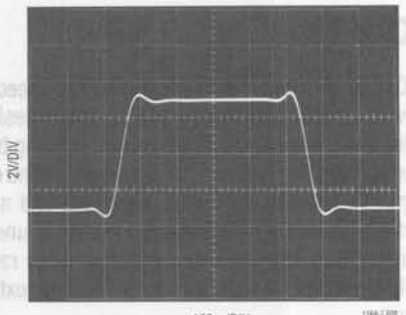


Figure 5.

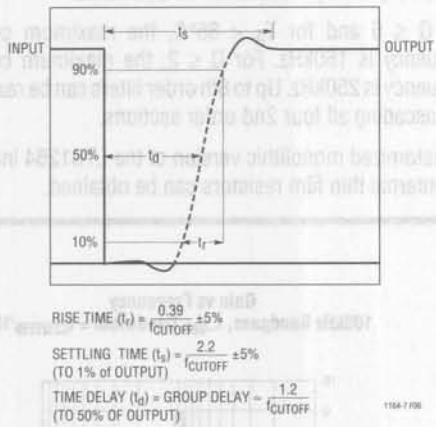


Figure 6.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-7 case at 100:1, an input signal whose frequency is in the range of f_{CLK} ±3%, will be aliased back into the filter's passband.

If, for instance, an LTC1164-7 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz 10mV input signal, a 2kHz, 143µV_{RMS} alias signal will appear at its output. When the LTC1164-7 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 11 shows details.

Table 11. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = 1V_{RMS}, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = 1V_{RMS}) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
50:1, f_{CUTOFF} = 2kHz		
190 (or 210)	–76.1	10.0
195 (or 205)	–51.9	5.0
196 (or 204)	–36.3	4.0
197(or 203)	–18.4	3.0
198 (or 202)	–3.0	2.0
199.5 (or 200.5)	–0.2	0.5
100:1, f_{CUTOFF} = 1kHz		
97 (or 103)	–74.2	3.0
97.5 (or 102.5)	–53.2	2.5
98 (or 102)	–36.9	2.0
98.5 (or 101.5)	–19.6	1.5
99 (or 101)	–5.2	1.0
99.5 (or 100.5)	–0.7	0.5

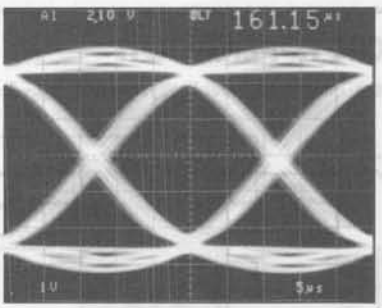


Figure 7. Eye Diagram

8

High Speed, Quad Universal Filter Building Block

FEATURES

- High Speed, Up to 250kHz Center Frequency
- Four Identical Filters in a 0.3" Wide Package
- Clock-to-Center Frequency Ratio of 20:1
- Double-Sampling, Improved Aliasing
- Operates from ±2.37V to ±8V Power Supplies
- Customized Version with Internal Resistors Available
- Low Noise
- Low Harmonic Distortion

APPLICATIONS

- Digital Communications
- Spread Spectrum Communications
- Spectral Analysis
- Loran Receivers
- Instrumentation

DESCRIPTION

The LTC1264 consists of four identical, high speed 2nd order switched-capacitor filter building blocks designed for center frequencies up to 250kHz. Each building block, together with three to five resistors, can provide 2nd order functions like lowpass, highpass, bandpass and notch. The center frequency of each 2nd order section is tuned via an external clock. The clock-to-center frequency ratio is internally set to 20:1, but it can be modified via external resistors.

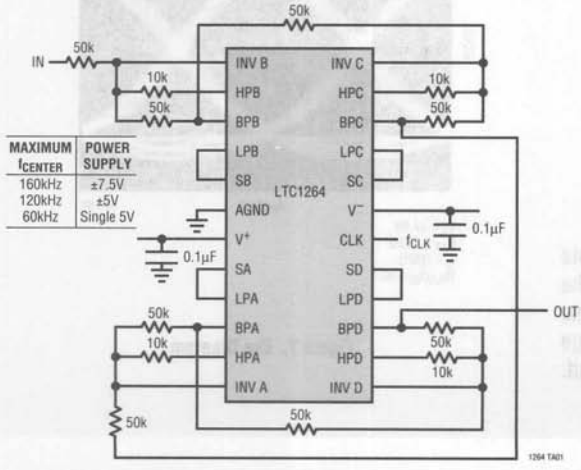
The aliasing performance of the LTC1264 is improved by double-sampling each 2nd order section. Input signal frequencies can reach up to twice the clock frequency before any alias products will be detectable.

For $Q \leq 5$ and for $T_A < 85°C$, the maximum center frequency is 160kHz. For $Q \leq 2$, the maximum center frequency is 250kHz. Up to 8th order filters can be realized by cascading all four 2nd order sections.

A customized monolithic version of the LTC1264 including internal thin film resistors can be obtained.

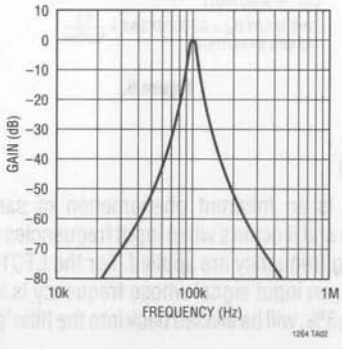
TYPICAL APPLICATION

Clock-Tunable 8th Order Bandpass Filter, $f_{CENTER} = f_{CLK}/20$



MAXIMUM f_{CENTER}	POWER SUPPLY
160kHz	±7.5V
120kHz	±5V
60kHz	Single 5V

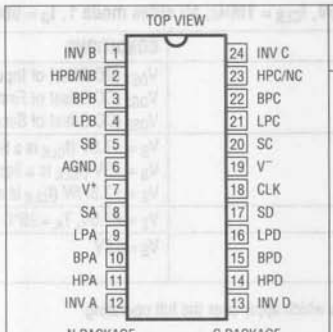
Gain vs Frequency
100kHz Bandpass, f_{-3dB} Bandwidth = $f_{CENTER}/10$



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
24-LEAD PLASTIC DIP

S PACKAGE
24-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1264CN
LTC1264CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

(Internal Op Amps) T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			±2.375		±8	V
Voltage Swings	V_S = ±2.375V, R_L = 5k			±1.5		V
	V_S = ±5V, R_L = 5k		±3.2	±3.7		V
		●	±3.1			V
	V_S = ±7.5, R_L = 5k			±6		V
Output Short-Circuit Current (Source/Sink)				3		mA
DC Open-Loop Gain				80		dB
GBW Product				7		MHz
Slew Rate				10		V/µs

(Complete Filter) V_S = ±5V, f_{CLK} = 1MHz, all sides mode 1, f_0 = 50kHz, Q = 5, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_0 (Note 1)	V_S = ±7.5V, T_A < 85°C, Q < 2			0.1 - 250		kHz
	V_S = ±5V, T_A < 85°C, Q < 2			0.1 - 200		kHz
	V_S = ±2.5V, T_A < 85°C, Q < 2			0.1 - 100		kHz
Clock-to-Center Frequency Ratio, f_{CLK}/f_0				20:1		
Center Frequency Error (Note 3)	V_S = ±7.5V			±0.1	±0.7	%
		●			±0.8	%
	V_S = ±5V			±0.2	±0.8	%
		●			±1.0	%
	V_S = ±2.375V			–1.6		%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S ≥ ±5V			0.4	0.8	%
		●			1.0	%
Q Accuracy	V_S = ±5V			–2.7		%
		●			7.0	%
f_0 Temperature Coefficient	f_{CLK} < 2MHz			±1		ppm/°C
Q Temperature Coefficient	f_{CLK} < 2MHz			5		ppm/°C

8

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $f_{CLK} = 1MHz$, all sides mode 1, $f_0 = 50kHz$, $Q = 5$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Offset Voltage (Note 2)	V_{OS1} (DC Offset of Input Inverter)	●			±20	mV
	V_{OS2} (DC Offset of First Integrator)	●			±45	mV
	V_{OS3} (DC Offset of Second Integrator)	●			±45	mV
Clock Feedthrough	$V_S = \pm 7.5V$ (f_{CLK} is a Square Wave)			160		μV_{RMS}
	$V_S = \pm 5V$ (f_{CLK} is a Square Wave)			120		μV_{RMS}
	$V_S = \pm 2.375V$ (f_{CLK} is a Square Wave)			90		μV_{RMS}
Maximum Clock Frequency	$V_S = \pm 7.5V$, $T_A = 25°C$			6		MHz
Power Supply Current	$V_S = \pm 5V$		9	14	25	mA
		●			30	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Please refer to Typical Maximum Q vs Clock Frequency graphs.

Note 2: Calculations of output DC offsets of one 2nd order section. Also see Block Diagram.

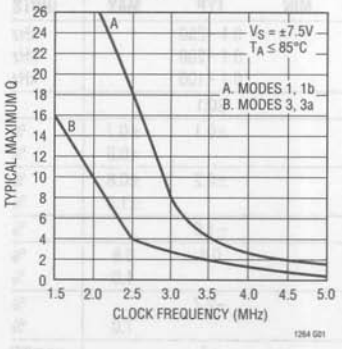
Note 3: The center frequency f_0, error is calculated as

$$\frac{f_0(\text{measured}) - f_0(\text{ideal})}{f_0\ (\text{ideal})} \times 100$$

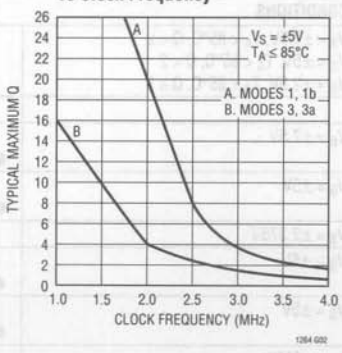
MODE	V_{OSN} PINS 2, 11, 14, 23	V_{OSBP} PINS 3, 10, 15, 22	V_{OSLP} PINS 4, 9, 16, 21
1	$V_{OS1}[(1Q) + 1 \|\|H_{OLP}\|\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$=(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

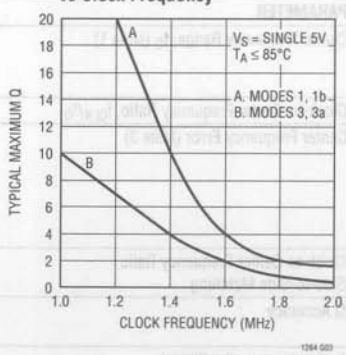
Typical Maximum Q vs Clock Frequency



Typical Maximum Q vs Clock Frequency

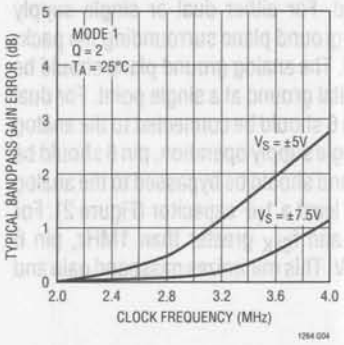


Typical Maximum Q vs Clock Frequency

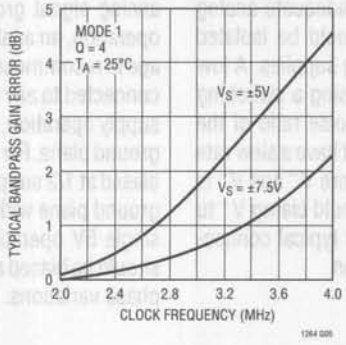


TYPICAL PERFORMANCE CHARACTERISTICS

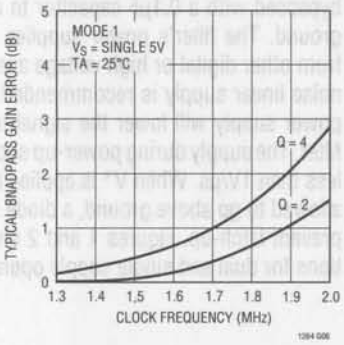
Typical Bandpass Gain Error vs Clock Frequency



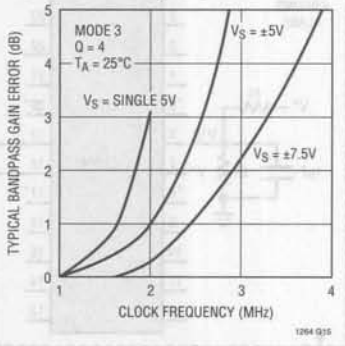
Typical Bandpass Gain Error vs Clock Frequency



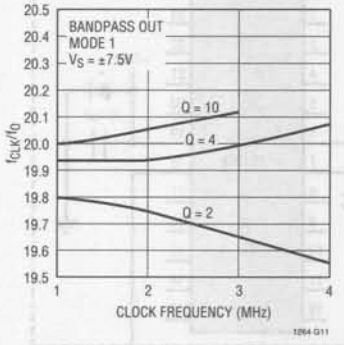
Typical Bandpass Gain Error vs Clock Frequency



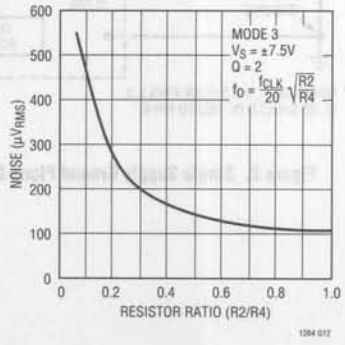
Typical Bandpass Gain Error vs Clock Frequency



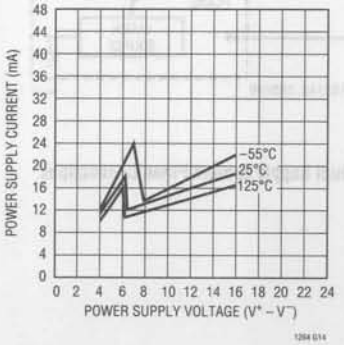
Ratio (f_{CLK}/f_O) vs Clock Frequency



Noise vs R2/R4 Ratio



Power Supply Current vs Supply Voltage



8

PIN FUNCTIONS

Power Supply Pins (7, 19)

The V^+ (pin 7) and the V^- (pin 19) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a diode should clamp V^- to prevent latch-up. Figures 1 and 2 show typical connections for dual and single supply operation.

Analog Ground Pin (6)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 6 should be connected to the analog ground plane. For single supply operation, pin 6 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 2). For single 5V operation and f_{CLK} greater than 1MHz, pin 6 should be biased at 2V. This minimizes passband gain and phase variations.

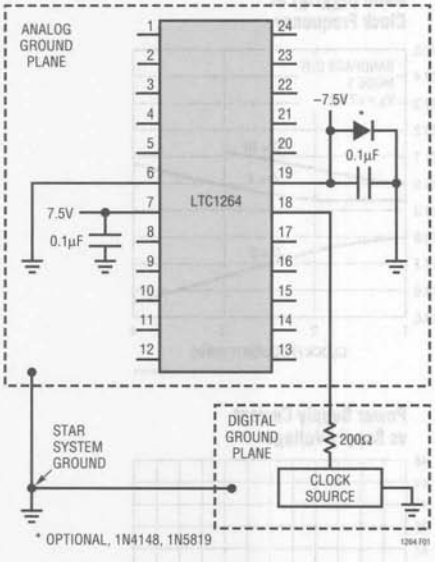


Figure 1. Dual Supply Ground Plane Connections

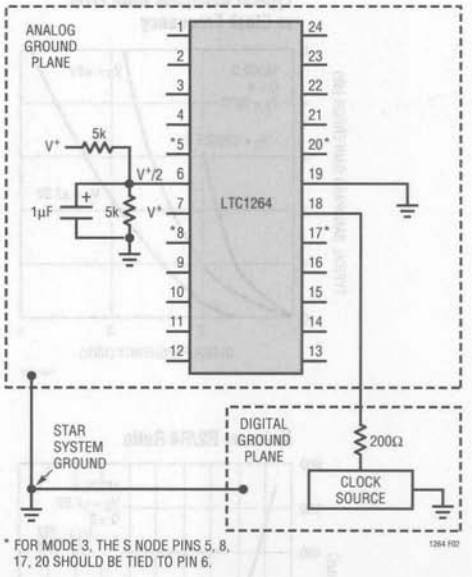


Figure 2. Single Supply Ground Plane Connections

PIN FUNCTIONS

Clock Input Pin (18)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for a dual or single supply operation.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ −2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

A pulse generator can be used as a clock source provided the high level ON-time is greater than 0.2µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 1 and 2).

Output Pins (2,3,4,9,10,11,14,15,16,21,22,23)

Each 2nd order section of the LTC1264 has three outputs which typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion performance of any filter design. When evaluating the distortion or noise performance of a particular filter design implemented with an LTC1264, the final output of the filter should be buffered with a wideband noninverting high slew rate amplifier (Figure 3).

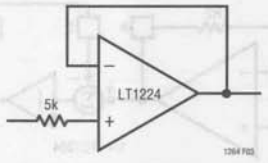


Figure 3. Wideband Buffer

Inverting Input Pins (1,12,13,24)

These pins are the high impedance inverting inputs of internal op amps and they are susceptible to stray capacitive connections to low impedance signal outputs and power supply lines.

Summing Input Pins (5,8,17,20)

The summing pins connections determine the circuit topology (mode) of each 2nd order section. Please refer to Modes of Operation.

8

MODES OF OPERATION

For the definition of filter functions please refer to the LTC1060 data sheet.

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 20:1. Figure 4 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency. Mode 1 is faster than Mode 3.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b (Figure 5) two additional resistors R5 and R6 are added to alternate the amount of voltage fed back from the lowpass output into the input of the SA (SB, SC or SD) switched-capacitor summer. This allows the filter's clock-to-center frequency ratio to be adjusted beyond 20:1. Mode 1b maintains the speed advantages of Mode 1 and should be considered an

MODES OF OPERATION

optimum mode for high Q designs with f_{CLK} to f_{CUTOFF} (or f_{CENTER}) ratios greater than 20:1.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

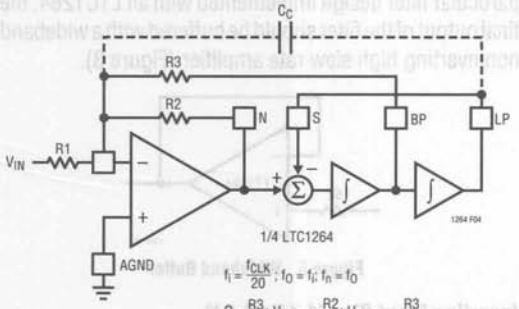


Figure 4. Mode 1, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

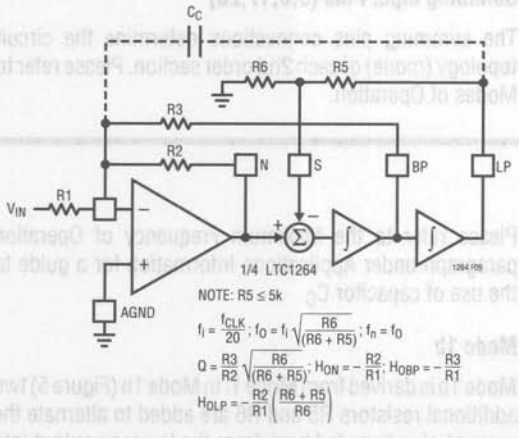


Figure 5. Mode 1b, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 3

In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 20:1. Figure 6 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass, and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, and highpass filters.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, shown in Figure 7. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than 20:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has a notch output which depends on the clock frequency, and the notch frequency is therefore less than the center frequency, f_O.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

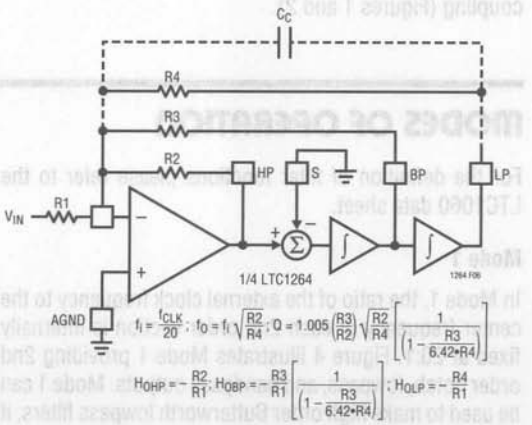
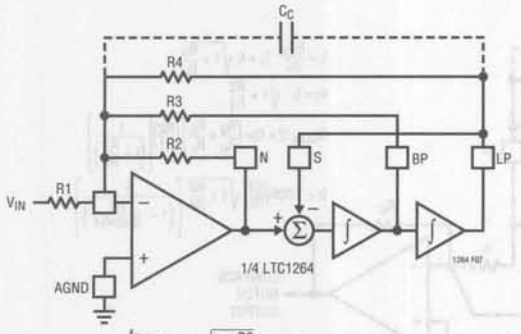


Figure 6. Mode 3, 2nd Order Section Providing Highpass, Bandpass and Lowpass Outputs

MODES OF OPERATION



$$f_I = \frac{f_{CLK}}{20};\ f_O = f_I\sqrt{1+\frac{R2}{R4}};\ f_n = f_O$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{1+\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{6.42 \cdot R4}\right)}\right]$$

$$H_{OHP} = -\frac{R2}{R1}\ (\text{AC GAIN, } f > f_n);\ H_{OHPn} = -\frac{R2}{R1}\left[\frac{1}{\left(1+\frac{R2}{R4}\right)}\right]\ (\text{DC GAIN, } f < f_n)$$

$$H_{OBP} = -\frac{R3}{R1}\left[\frac{1}{\left(1-\frac{R3}{6.42 \cdot R4}\right)}\right];\ H_{OLP} = H_{OHPn}$$

Figure 7. Mode 2, 2nd Order Filter Providing Highpass Notch, Bandpass and Lowpass Outputs

Mode 3a

This is an extension of Mode 3 where the highpass and lowpass output are summed through two external resistors R_H and R_L to create a notch. This is shown in Figure 8. Mode 3a is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 8 is not always required. When cascading the sections of the LTC1264, the highpass and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2n

This mode extends the circuit topology of Mode 3a to Mode 2 (Figure 9) where the highpass notch and lowpass outputs are summed through two external resistors R_H and R_L to create a lowpass output with a notch higher in frequency than the notch in Mode 2. This mode, shown in Figure 8, is most useful in lowpass elliptic designs. When cascading the sections of the LTC1264, the highpass notch and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

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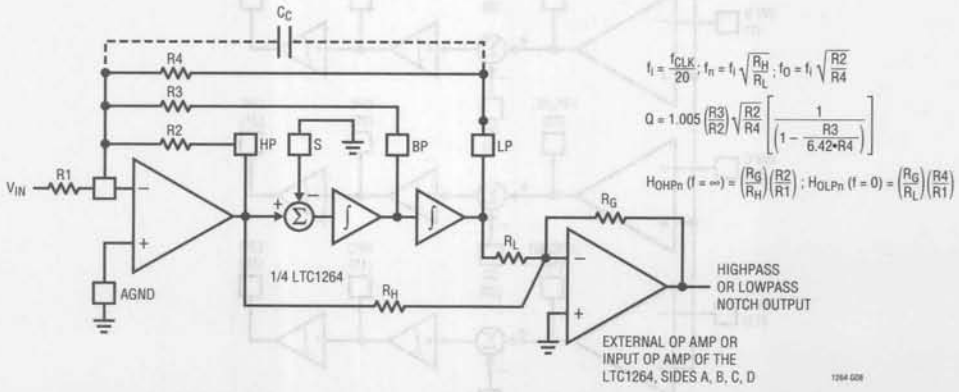


$$f_I = \frac{f_{CLK}}{20};\ f_n = f_I\sqrt{\frac{R_H}{R_L}};\ f_O = f_I\sqrt{\frac{R2}{R4}}$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{6.42 \cdot R4}\right)}\right]$$

$$H_{OHPn}\ (f=\infty) = \left(\frac{R_G}{R_H}\right)\left(\frac{R2}{R1}\right);\ H_{OLPn}\ (f=0) = \left(\frac{R_G}{R_L}\right)\left(\frac{R4}{R1}\right)$$

Figure 8. Mode 3a, 2nd Order Filter Providing a Highpass Notch or Lowpass Notch Output

MODES OF OPERATION

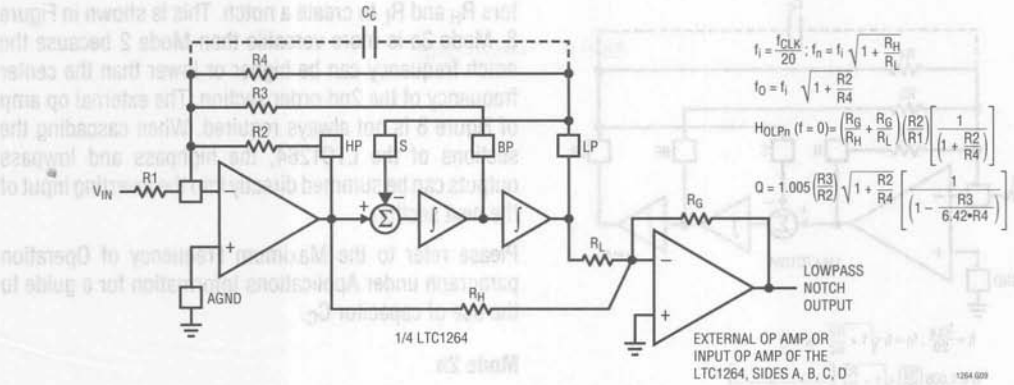
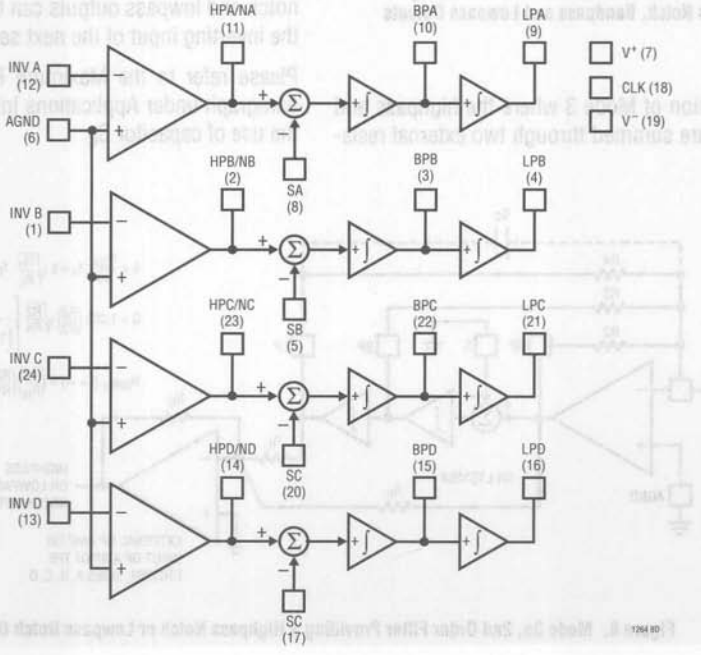


Figure 9. Mode 2n, 2nd Order Filter Providing a Lowpass Notch Output

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operating Limits

The Typical Maximum Q vs Clock Frequency and Bandpass Gain Error graphs, under Typical Performance Characteristics, define an upper limit of operating Q for each LTC1264 2nd order section. These graphs indicate the power supply, f_{CLK} and Q value conditions under which a filter implemented with an LTC1264 will remain stable when operated at temperatures of 85°C or less. For a 2nd order section, a bandpass gain error of 3dB or less is arbitrarily defined as a condition for stability.

When the passband gain error begins to exceed 1dB, the use of capacitor C_C will reduce the gain error (capacitor C_C is connected from the lowpass node to the inverting node of a 2nd order section). Please refer to Figures 4 through 9. The value of C_C can be best determined experimentally, and as a guide it should be about 5pF for each 1dB of gain error and not to exceed 15pF. When operating LTC1264 very near the limits defined by the Typical Performance Characteristics graphs, passband gain variations of 2dB or more should be expected.

Speed Limitations

To avoid op amp slew rate limiting, the signal amplitude should be kept below a specified level as shown in Table 2.

Table 2. Maximum V_{IN} vs V_S and Clock

V_S	MAXIMUM CLOCK	MAXIMUM V_{IN}
±7.5V	4MHz to 5MHz	$0.5V_{RMS}$ $f_{IN} \geq 400kHz$
±5V	3MHz to 4MHz	$0.5V_{RMS}$ $f_{IN} \geq 250kHz$
Single 5V	1MHz to 2MHz	$0.35V_{RMS}$ $f_{IN} \geq 160kHz$

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins. The clock feedthrough is tested with the filter's input grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques, the typical values of clock feedthrough are listed under Electrical Characteristics.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple RC lowpass network at the final filter output. This RC will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering.

The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

For a specific filter design, the total noise depends on the Q of each section and the cascade sequence. Table 3 shows typical 2nd order section noise (gain = 1) for Q values and supplies operating at 25°C. Noise increases by 20% at the highest operating temperatures.

Table 3. 2nd Order Section Noise (μV_{RMS}) for Modes 1, 1b, 2 or 3 (R2 = R4)

Q	V_S = ±2.5V	V_S = ±5V	V_S = ±7.5V
1	$40\mu V_{RMS}$	50	60
2	$50\mu V_{RMS}$	60	75
3	$60\mu V_{RMS}$	75	95
4	$75\mu V_{RMS}$	90	115
5	$90\mu V_{RMS}$	110	135

Aliasing

Aliasing is an inherent phenomenon of switched-capacitor filters and it occurs when the frequency of input signals approaches the sampling frequency. The input signals that produce the strongest aliased components have a frequency, f_{IN}, such as ($f_{SAMPLING} - f_{IN}$) falls into the filter's passband. For the LTC1264 the sampling frequency is twice f_{CLK}. If the input signal spectrum is not band-limited, aliasing may occur.

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APPLICATIONS INFORMATION

For example, for an LTC1264 bandpass filter with f_{CENTER} = 100kHz and f_{CLK} = 2MHz, a 3.9MHz, 10mV input will produce a 100kHz, 10mV output. A 1st or 2nd order prefilter will reduce aliasing to acceptable levels in most cases.

A GUIDE TO BANDPASS DESIGN

Filter design tools like FCAD require design specification inputs such as passband ripple, attenuation, passband width and stopband width in order to calculate filter parameters f_0, Q, f_n or poles and zeroes. The results of these filter approximations most often require Q values which make excessive demands on the gain-bandwidth products of active filter realizations. The active filter designer should define a gain response so that the filter's mathematical approximation has practical requirements. Table 4 is a guide to practical design specifications for realizing bandpass filters with LTC1264 (please also refer to the Typical Maximum Q vs Clock Frequency and Bandpass Gain Error graphs under Typical Performance Characteristics).

A Bandpass Design Example

Filter Type:	Bandpass
Filter Response:	Butterworth
Passband Ripple:	3dB
Attenuation:	60dB
Center Frequency:	40kHz (f_{CENTER})
Passband Width:	10kHz
Stopband Width:	60kHz

Implementing the Bandpass Design

With the LTC1264 in Mode 1b, Butterworth and Chebyshev bandpass designs with f_{CLK} to f_{CENTER} ratios greater than 20:1 are possible.

First choose the clock frequency which in Mode 1b must be greater than 20 times the bandpass center frequency of 40kHz. For this example, let's choose f_{CLK} to be 1MHz. Table 6 lists the resistors for for the bandpass design example and Figure 11 shows the complete circuit.

Table 4. Bandpass Design Specifications (f_{CENTER} is center frequency of passband.)

PASSBAND RIPPLE (dB)	PASSBAND WIDTH (Hz)	STOPBAND WIDTH (Hz)	ATTENUATION (dB)
≤ 3dB for Butterworth	≥ f_{CENTER}/20	≥ 5 × Passband	–40 to –60
≤ 0.1 for Chebyshev	≥ f_{CENTER}/20	≥ 5 × Passband	–40 to –60

Note: Reducing passband ripple or attenuation will decrease Q values. The filter order may also increase.

Table 5. Calculated Filter Parameters

STAGE	f_0	Q
1	38.1201kHz	4.3346
2	41.9726kHz	4.3346
3	35.6418kHz	10.5221
4	44.8911kHz	10.5221

Table 6. Calculated Mode 1b Resistors to Nearest 1% Value Using Table 5 Filter Parameters and Figure 10 Equations

STAGE	R1	R2	R3	R5	R6
1	52.3k	10k	56.2k	5k	6.98k
2	47.5k	10k	51.1k	5k	11.8k
3	56.2k	10k	147k	5k	5.11k
4	44.2k	10k	118k	5k	20.5k

$$R2 = 10k$$

$$R5 = 5k$$

$$f_I = \frac{f_{CLK}}{20}$$

$$R1 = \frac{R3}{H_{OBP}} \text{ (FOR BANDPASS)}$$

$$R6 = \frac{R5 \bullet f_0^2}{(f_I^2 - f_0^2)}$$

$$H_{OBP} = \sqrt{Q^2\left[\left(\frac{f_0}{f_{CENTER}}\right) - \left(\frac{f_{CENTER}}{f_0}\right)\right]^2 + 1}$$

$$R3 = \frac{R2 \bullet Q}{\sqrt{\frac{R6}{(R6 + 5)}}}$$

1264 F10

Figure 10. Equations for Resistors in Mode 1b Operation

APPLICATIONS INFORMATION

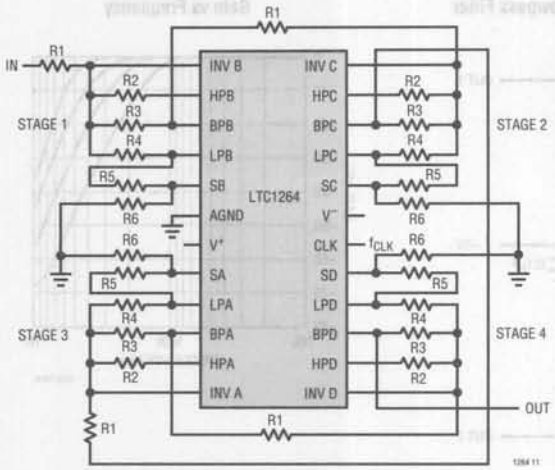


Figure 11. Mode 1b Bandpass Filter

Figures 12 and 13 show the gain response graphs of the 40kHz Butterworth bandpass design described above. The passband gain response graph (Figure 12) shows a 40kHz gain of –0.4dB and a tilted passband from 37kHz to 43kHz. These errors are due to the 1% resistors used and the side-to-side matching of the LTC1264 f_{CLK}-to-f_{CENTER} ratio which typically is 0.4%. To adjust for 0dB gain at 40kHz, reduce the value of R1 in the first stage by 5%. To adjust for a flat passband, adjust by ±1% the value of R6 in stages 3 and 4. Adjusting R6 compensates for the side-to-side matching errors. Please refer to Figure 5 equations defining f_0 and Q as a function of R6.

The sequence of 2nd order stages and the bandpass gain H_{OBP} of each stage will determine the gain peaks at the filter's intermediate outputs. A given internal output can have several dB more gain than the final filter output. Gain peaks occur around the corners of the passband. The gain peaks can be reduced by increasing the R1 resistor of the first stage and decreasing the R1 resistor of the last stage by the same amount (multiplying the R1 resistor of the first stage and dividing the R1 resistor of the last stage by 2 for narrowband filter, and by 5 for wideband filter is a good rule of thumb). This adjustment may, however, increase the filter's passband noise.

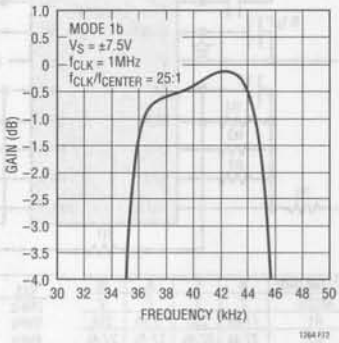


Figure 12. Passband Gain vs Frequency 40kHz Butterworth Bandpass

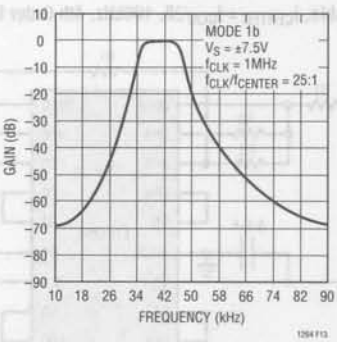
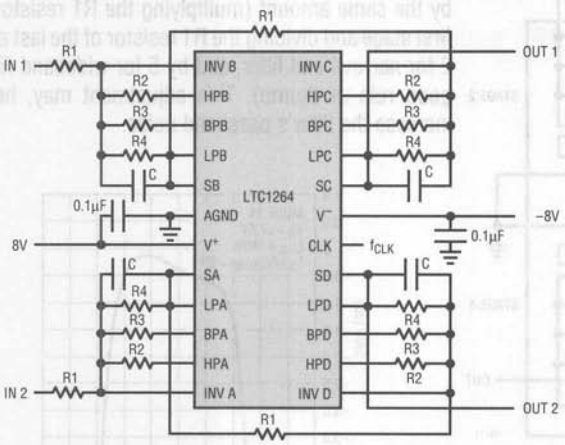


Figure 13. Gain vs Frequency 40kHz Butterworth Bandpass

8

TYPICAL APPLICATIONS

Linear Phase Clock-Tunable to 400kHz, Dual 4th Order Lowpass Filter



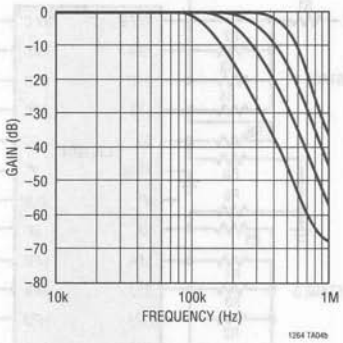
LTC1264 SIDE	B	C	A	D
MODE	2	2	2	2
R1	17.8k	20k	17.8k	20k
R2	27.4k	27.4k	27.4k	27.4k
R3	19.6k	21k	19.6k	21k
R4	51.1k	75k	51.1k	75k
C	5pF	5pF	5pF	5pF

f_{CLK}	f_{-3dB} (V_S = ±8V)
2MHz	125kHz
3MHz	200kHz
4MHz	275kHz
5MHz	400kHz

$T_A \leq 50°C$

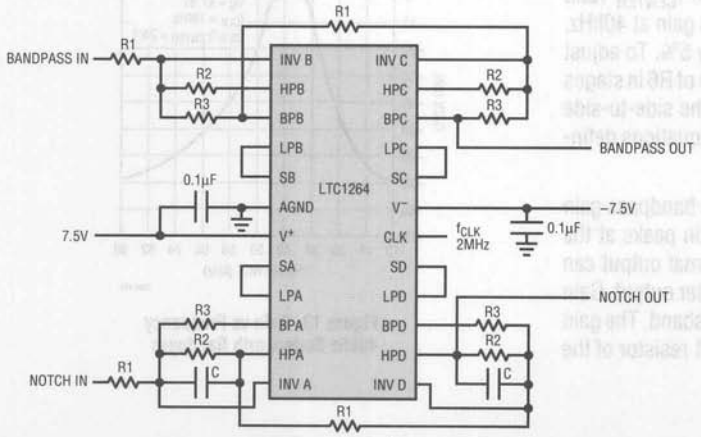
1264 TA04a

Gain vs Frequency



1264 TA04b

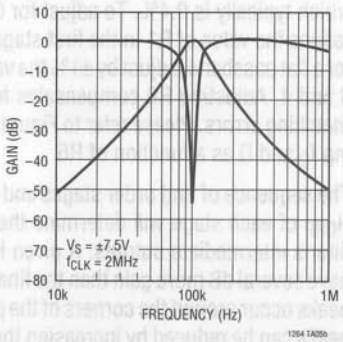
Clock-Tunable, $f_{CENTER} = f_{CLK}/20$, 100kHz, 4th Order Bandpass and Notch Filters



LTC1264 SIDE	B	C	A	D
MODE	1	1	1	1
R1	20k	20k	10k	10k
R2	10k	10k	10k	10k
R3	20k	20k	20k	20k
C			10pF	10pF

1264 TA05a

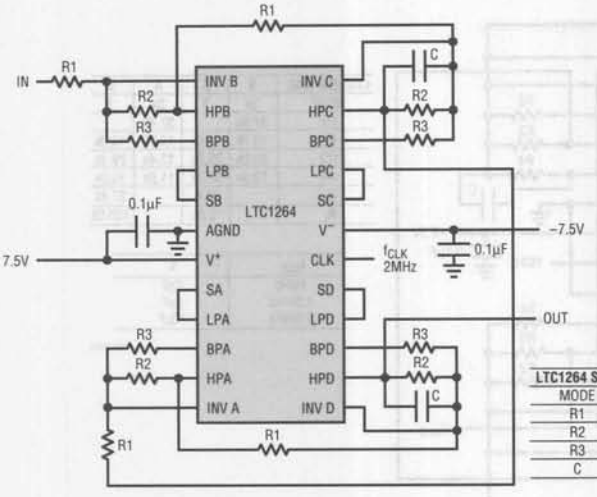
Gain vs Frequency



1264 TA05b

TYPICAL APPLICATIONS

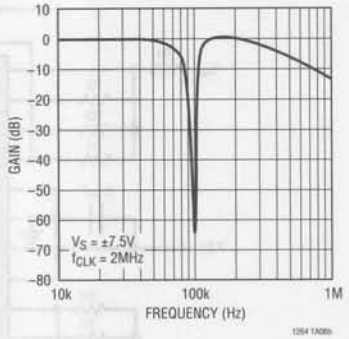
100kHz, 8th Order Notch Filter, f_{CLK}/f_{CENTER} = 20:1



LTC1264 SIDE	B	C	A	D
MODE	1	1	1	1
R1	36.5k	3.92k	7.5k	9.09k
R2	10k	10k	10k	10k
R3	50k	27.4k	50k	50k
C		30pF		30pF

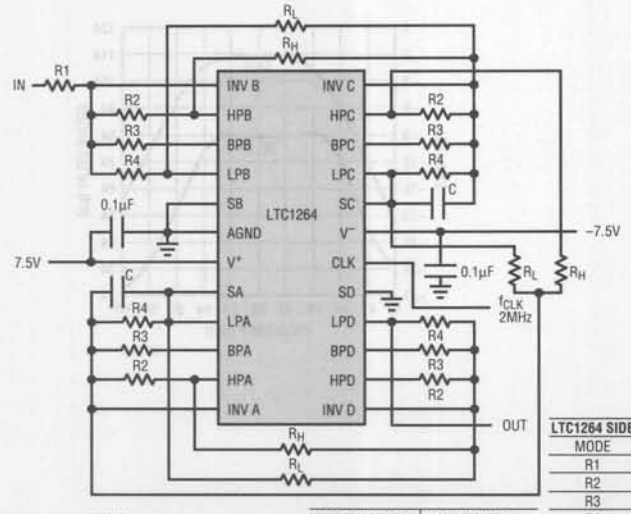
1264 TA06a

Gain vs Frequency



1264 TA06b

Clock-Tunable, 8th Order Elliptic Lowpass Filter, f_{CLK}/f_{CUTOFF} = 20:1

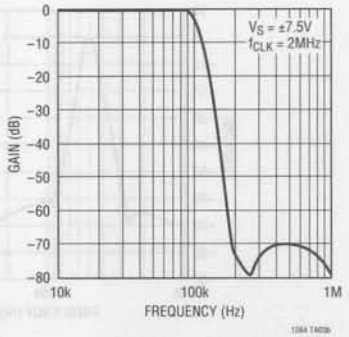


LTC1264 SIDE	B	C	A	D
MODE	3a	2n	2n	3
R1	27.4k			
R2	23.7k	20k	20k	29.4k
R3	20k	37.4k	37.4k	19.1k
R4	28k	100k	100k	48.7k
R_H	137k	100k	130k	
R_L	27.4k	31.6k	24.3k	
C		3pF	3pF	

1264 TA03a

POWER SUPPLY	MAXIMUM f_{CLK}
±7.5V	3.6MHz (C = 10pF)
±5V	2.0MHz (C = 10pF)
SINGLE 5V	1.6MHz (C = 10pF)

Gain vs Frequency



1264 TA03b

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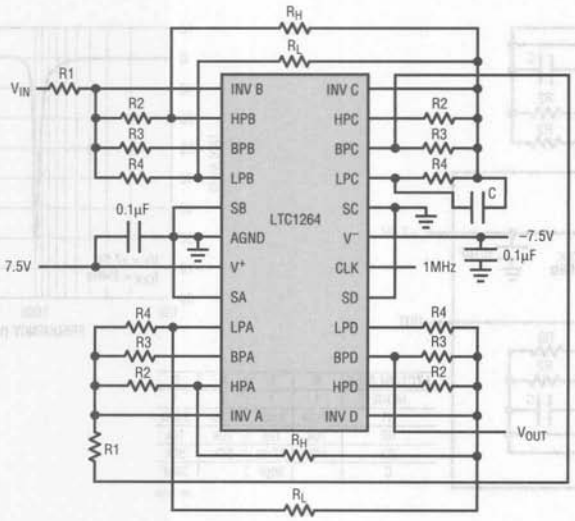
TYPICAL APPLICATIONS

8th Order Bandpass Filter, Linear Phase

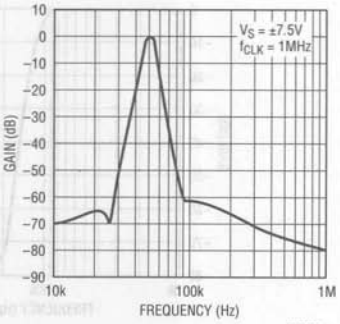


LTC1264 SIDE	B	C	A	D
MODE	3a	3	3a	3
R1	97.6k		32.4k	
R2	10.7k	12.4k	10.7k	10.0k
R3	39.2k	39.2k	12.4k	29.4k
R4	13.3k	10.7k	11.5k	10.0k
R_H		53.6		27.4k
R_L		15.0k		100.0k

f_{CLK}	C
1MHz	0pF
1.5MHz	5pF
2.0MHz	10pF

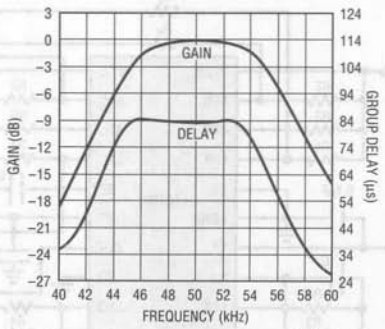
1264 TA07a

50kHz Bandpass Filter, Linear Phase Gain vs Frequency



1264 TA07b

Passband Gain and Group Delay



1264 TA07c

Linear Phase, Group Delay Equalized, 8th Order Lowpass Filter

FEATURES

- Steeper Roll-Off Than Bessel Filters
- High Speed: $f_C \leq 200kHz$
- Phase Equalized Filter in a 14-Pin Package
- Phase and Group Delay Response Fully Tested
- Transient Response Exhibits 5% Overshoot and No Ringing
- 65dB THD or Better Throughout a 100kHz Passband
- No External Components Needed

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase Matched Filters

DESCRIPTION

The LTC1264-7 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 28dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency the filter attains 55dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1264-7 is tuned via an external TTL or CMOS clock.

The clock-to-cutoff frequency ratio of the LTC1264-7 can be set to 25:1 (pin 10 to V^+) or 50:1 (pin 10 to V^-).

When the filter operates at clock-to-cutoff frequency ratio of 25:1, the input is double-sampled to lower the risk of aliasing.

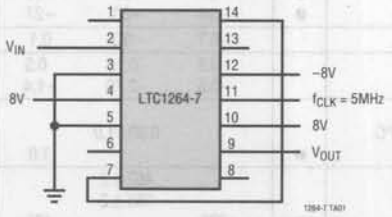
The LTC1264-7 is optimized for speed. Depending on the operating conditions, cutoff frequencies between 200kHz and 250kHz can be obtained. (Please refer to the Passband vs Clock Frequency graphs.)

The LTC1264-7 is pin-compatible with the LTC1064-X series.

8

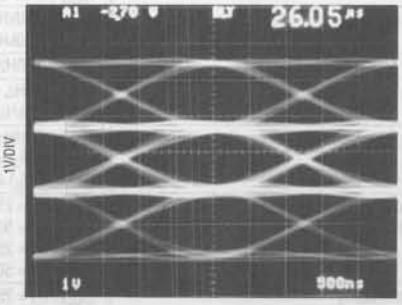
TYPICAL APPLICATION

200kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

4-Level PAM Eye Diagram



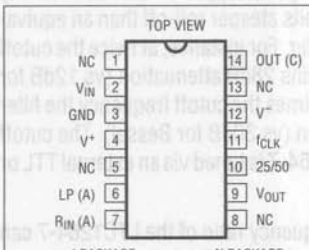
f_{CLK} = 5MHz
f_C = 200kHz

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Power Dissipation 400mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1264-7C ..... –40°C to 85°C
LTC1264-7M ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

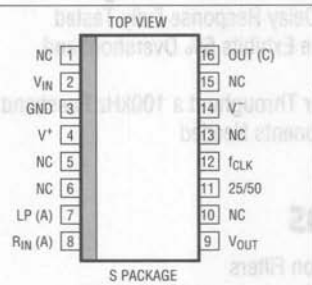


J PACKAGE
14-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)

N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER

LTC1264-7CN
LTC1264-7CJ
LTC1264-7MJ



S PACKAGE
16-LEAD PLASTIC SOL
T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1264-7CS

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 100kHz or 50kHz, f_{CLK} = 2.5MHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF} f_{TEST} = 25kHz, (f_{CLK}/f_C) = 25:1	 ●	 –0.50	 –0.10	 0.50	 dB
Gain at 0.50 f_{CUTOFF} (Note 3)	f_{TEST} = 50kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 25kHz, (f_{CLK}/f_C) = 50:1	● ●	–0.50 –0.65	 –0.15	0.20 0.30	dB dB
Gain at 0.75 f_{CUTOFF}	f_{TEST} = 75kHz, (f_{CLK}/f_C) = 25:1	●	–1.5	–1.0	0.1	dB
Gain at f_{CUTOFF}	f_{TEST} = 100kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 50kHz, (f_{CLK}/f_C) = 50:1	● ●	–3.7 –4.5	–3.0 –3.0	–1.9 –2.3	dB dB
Gain at 2.0 f_{CUTOFF}	f_{TEST} = 200kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 100kHz, (f_{CLK}/f_C) = 50:1	● ●	–34 –34	–28 –30	–20 –27	dB dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 50:1		–0.7	–0.3	0.1	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 16kHz, (f_{CLK}/f_C) = 25:1	 	–0.2 –3.5	0.15 –2.70	0.5 –1.4	dB dB
Gain with f_{CLK} = 4MHz	f_{TEST} = 160kHz, V_{IN} = 1V_{RMS} (f_{CLK}/f_C) = 25:1, T_A = 0°C to 70°C (f_{CLK}/f_C) = 25:1	 ●	 	 0.00±1.0 	 3.0	 dB dB
Phase Factor (F) Phase = 180° – F (f/f_C) (Note 1)	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	 ● ●	 392 374	407 ± 2 388 ± 2 	 423 414	Deg Deg Deg Deg
Phase Nonlinearity (Note 1)	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	 ● ●	 	±1.0 ±1.0 	 ±2.0 ±2.0	% % % %

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 100kHz or 50kHz, f_{CLK} = 2.5MHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay (t_d)	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF}			11.3		µs
$t_d = (F/360)(1/f_C)$;	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}			21.6		µs
(Note 2, 3)	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF}	●	10.9		11.7	µs
	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	●	20.8		22.9	µs
Group Delay Ripple	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF}			±1.0		%
(Note 2)	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}			±1.0		%
	(f_{CLK}/f_C) = 25:1, f ≤ f_{CUTOFF}	●			±2.0	%
	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	●			±2.0	%
Input Frequency Range	(f_{CLK}/f_C) = 25:1			<f_{CLK}		kHz
(Table 9, 10)	(f_{CLK}/f_C) = 50:1			<$f_{CLK}/2$		kHz
Maximum f_{CLK}	V_S = Single 5V (GND = 2V)			2		MHz
	V_S = ±5V			3		MHz
	V_S = ±7.5V			5		MHz
Clock Feedthrough	25:1, ±7.5V, f = f_{CLK}			120		μV_{RMS}
Wideband Noise	V_S = Single 5V			140 ± 5%		μV_{RMS}
(1Hz ≤ f < f_{CLK})	V_S = ±5V			160 ± 5%		μV_{RMS}
	V_S = ±7.5V			175 ± 5%		μV_{RMS}
Input Impedance			30	50	75	kΩ
Output DC Voltage Swing	V_S = ±2.375V			±1.0		V
(Note 4)	V_S = ±5V	●	±2.0	±2.3		V
	V_S = ±7.5V	●	±3.0	±3.8		V
Output DC Offset	25:1, V_S = ±5V			±100	±220	mV
(f_{CLK} = 1MHz)	50:1, V_S = ±5V			±100	±220	mV
Output DC Offset TempCo	25:1, V_S = ±5V			±200		µV/°C
	50:1, V_S = ±5V			±200		µV/°C
Power Supply Current	V_S = ±2.375V			11	22	mA
(f_{CLK} = 1MHz)		●			22	mA
	V_S = ±5V			14	25	mA
		●			30	mA
	V_S = ±7.5V			17	30	mA
		●			35	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as f ≤ f_C; f_C = cutoff frequency.

Figure 1 curve (A) shows the typical phase response of an LTC1264-7 operating at f_{CLK} = 2.5MHz, f_C = 100kHz. An endpoint straight line, curve (B), depicts the ideal linear phase response of the filter. It is described by: phase shift = 180° – $F(f/f_C)$; f ≤ f_C.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency. Note, the maximum phase nonlinearity, Figure 1, occurs at the vicinity of f = 0.25 f_C and = 0.75 f_C. Example: The phase shift at 70kHz of the LTC1264-7 shown in Figure 1 is: phase shift = 180° – 407° (70kHz/100kHz) ± nonlinearity = –104.9° ± 1% or –104.9° ± 1.05°.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 4: The AC swing is typically $9V_{P-P}$, $5.6V_{P-P}$, $1.8V_{P-P}$ with ±7.5V, ±5V, ±2.5V supply respectively. For more information refer to the THD + Noise vs Input graphs.

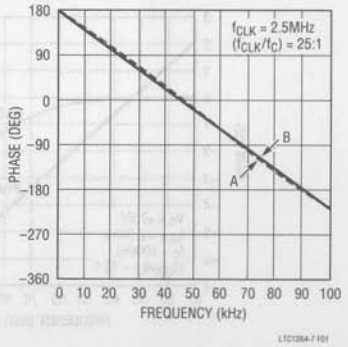


Figure 1. Phase Response in the Passband (Note 1)

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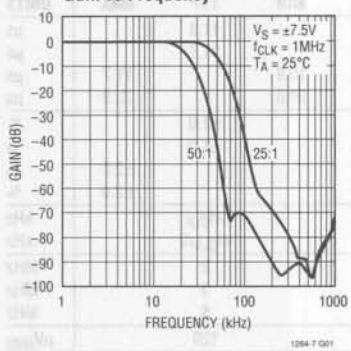
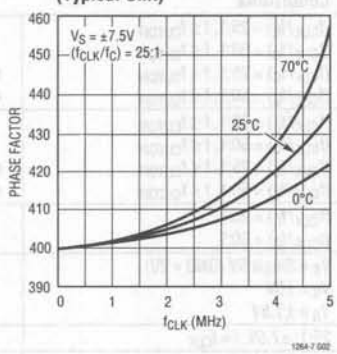
TYPICAL PERFORMANCE CHARACTERISTICS

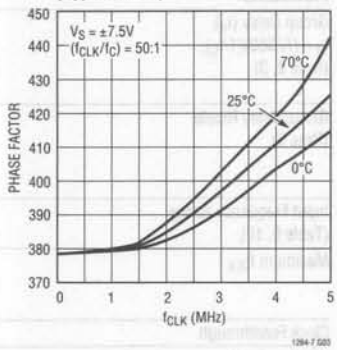
Gain vs Frequency



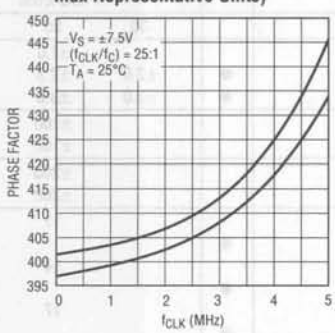
Phase Factor vs f_{CLK} (Typical Unit)



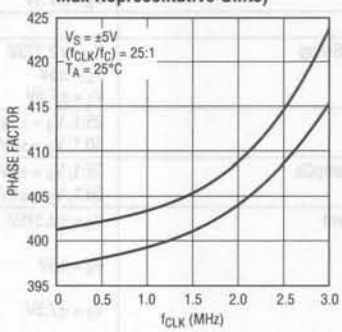
Phase Factor vs f_{CLK} (Typical Unit)



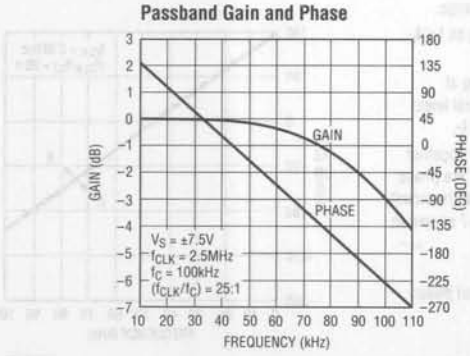
Phase Factor vs f_{CLK} (Min and Max Representative Units)



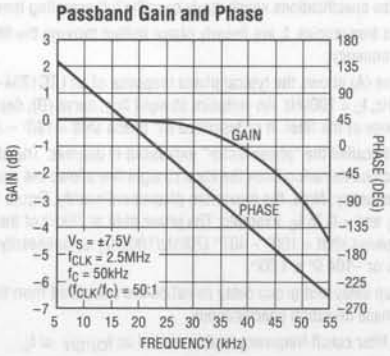
Phase Factor vs f_{CLK} (Min and Max Representative Units)



Passband Gain and Phase

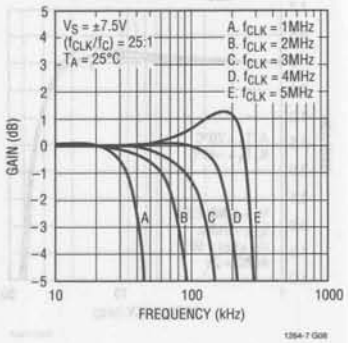


Passband Gain and Phase

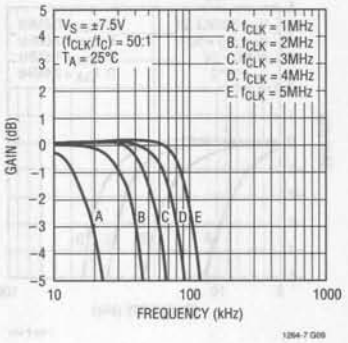


TYPICAL PERFORMANCE CHARACTERISTICS

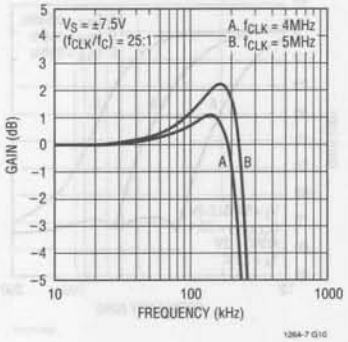
Passband Gain vs f_{CLK}



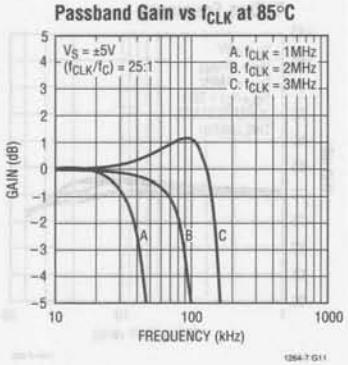
Passband Gain vs f_{CLK}



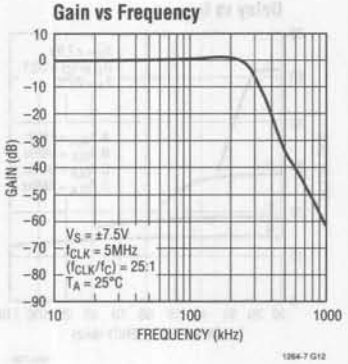
Passband Gain vs f_{CLK} at 85°C



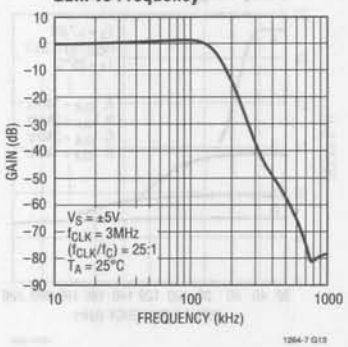
Passband Gain vs f_{CLK} at 85°C



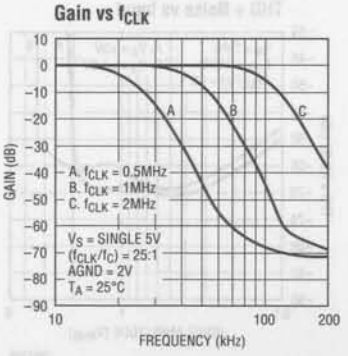
Gain vs Frequency



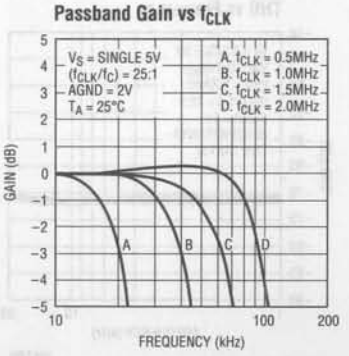
Gain vs Frequency



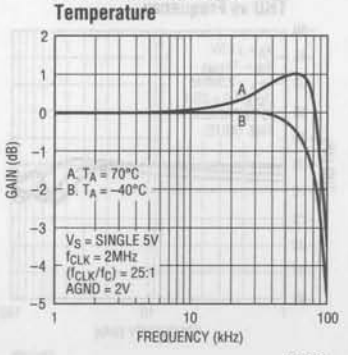
Gain vs f_{CLK}



Passband Gain vs f_{CLK}



Maximum Passband vs Temperature



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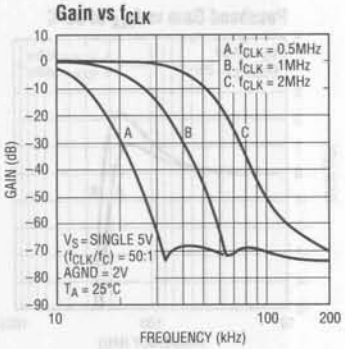
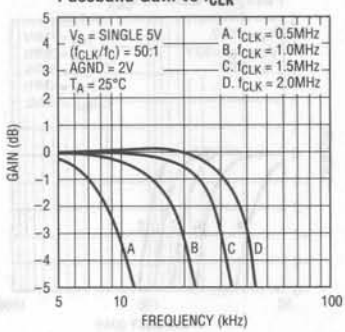
TYPICAL PERFORMANCE CHARACTERISTICS

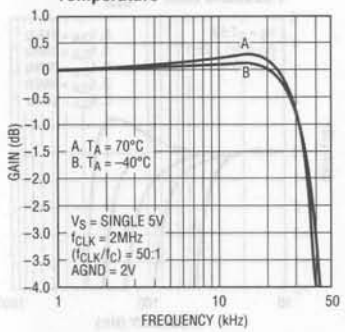
Gain vs f_{CLK}



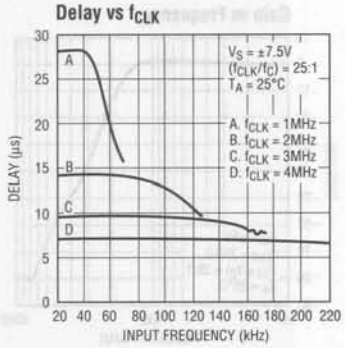
Passband Gain vs f_{CLK}



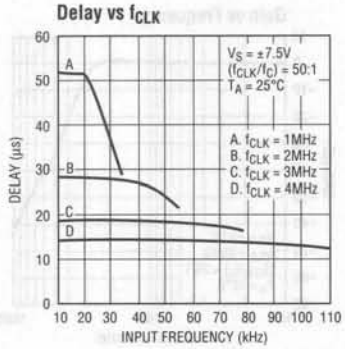
Maximum Passband vs Temperature



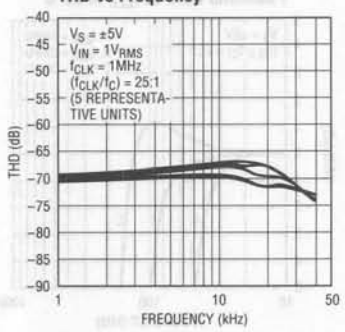
Delay vs f_{CLK}



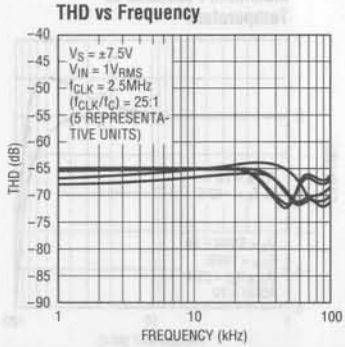
Delay vs f_{CLK}



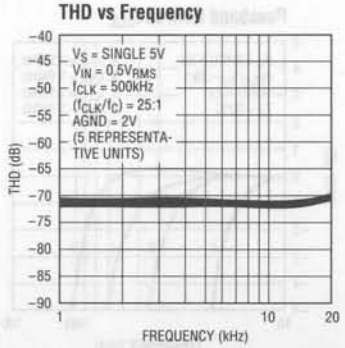
THD vs Frequency



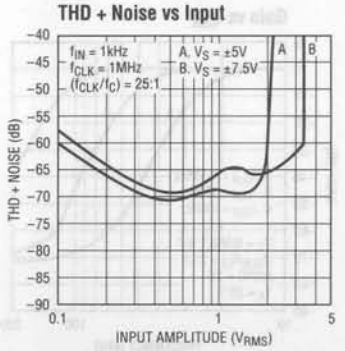
THD vs Frequency



THD vs Frequency

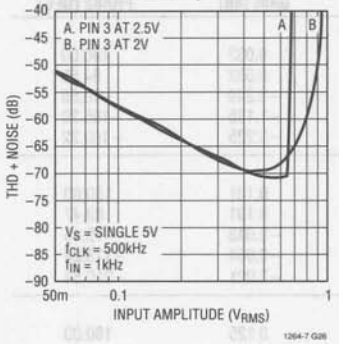


THD + Noise vs Input

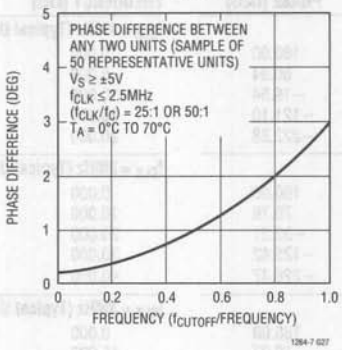


TYPICAL PERFORMANCE CHARACTERISTICS

THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage

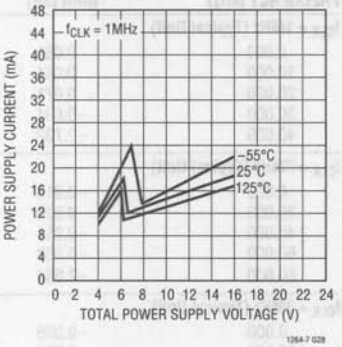


Table 1. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 25:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.064	180.00
10.000	0.064	81.14
20.000	0.058	–19.18
30.000	–0.639	–120.63
40.000	–2.741	–221.78
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.006	180.00
20.000	–0.006	79.42
40.000	–0.164	–22.13
60.000	–0.958	–124.09
80.000	–3.003	–225.01
f_{CLK} = 3MHz (Typical Unit)		
0.000	–0.067	180.00
30.000	–0.067	77.49
60.000	–0.287	–25.54
90.000	–0.944	–128.51
120.000	–2.545	–230.19
f_{CLK} = 4MHz (Typical Unit)		
0.000	–0.031	180.00
40.000	–0.031	75.23
80.000	–0.078	–30.06
120.000	–0.332	–135.27
160.000	–1.275	–239.76
f_{CLK} = 5MHz (Typical Unit)		
0.000	0.073	180.00
50.000	0.073	71.77
100.000	0.365	–37.11
150.000	0.686	–146.19
200.000	0.521	–255.85

Table 2. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.048	180.00
5.000	–0.048	84.51
10.000	–0.351	–10.87
15.000	–1.253	–105.53
20.000	–3.348	–199.61
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.008	180.00
10.000	–0.008	83.39
20.000	–0.237	–13.09
30.000	–1.105	–108.91
40.000	–3.238	–204.09
f_{CLK} = 3MHz (Typical Unit)		
0.000	0.044	180.00
15.000	0.044	81.04
30.000	–0.065	–18.64
45.000	–0.863	–118.48
60.000	–3.022	–217.67
f_{CLK} = 4MHz (Typical Unit)		
0.000	0.071	180.00
20.000	0.071	78.04
40.000	0.039	–25.06
60.000	–0.664	–128.54
80.000	–2.755	–231.42
f_{CLK} = 5MHz (Typical Unit)		
0.000	0.089	180.00
25.000	0.089	74.36
50.000	0.141	–32.41
75.000	–1.437	–139.33
100.000	–2.421	–246.01

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TYPICAL PERFORMANCE CHARACTERISTICS

Table 3. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 25:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.081	180.00
10.000	0.081	80.94
20.000	0.071	−19.54
30.000	−0.631	−121.10
40.000	−2.732	−222.28
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.016	180.00
20.000	−0.016	78.78
40.000	−0.211	−23.21
60.000	−0.968	−125.42
80.000	−2.864	−226.47
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.006	180.00
30.000	−0.006	76.07
60.000	−0.044	−28.54
90.000	−0.369	−133.27
120.000	−1.507	−237.35

Table 4. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.032	180.00
5.000	0.032	84.60
10.000	−0.249	−10.65
15.000	−1.135	−105.20
20.000	−3.225	−199.22
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.101	180.00
10.000	0.101	82.47
20.000	−0.043	−15.45
30.000	−0.864	−113.28
40.000	−3.021	−210.54
f_{CLK} = 3MHz (Typical Unit)		
0.000	0.125	180.00
15.000	0.125	77.88
30.000	0.043	−25.31
45.000	−0.753	−128.74
60.000	−2.987	−231.29

Table 5. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 25:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	0.161	180.00
5.000	0.161	81.47
10.000	0.166	−18.52
15.000	−0.515	−119.79
20.000	−2.598	−220.82
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.125	180.00
10.000	0.125	80.23
20.000	0.043	−20.75
30.000	−0.706	−122.53
40.000	−2.781	−223.59
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	0.061	180.00
15.000	0.061	78.49
30.000	−0.096	−23.82
45.000	−0.741	−126.47
60.000	−2.432	−228.12
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.151	180.00
20.000	0.151	75.03
40.000	0.321	−31.15
60.000	0.203	−137.86
80.000	−0.838	−244.58

Table 6. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	0.075	180.00
2.500	0.075	84.79
5.000	−0.217	−10.40
7.500	−1.108	−105.10
10.000	−3.198	−199.26
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.114	180.00
5.000	0.114	83.96
10.000	−0.122	−11.88
15.000	−0.988	−107.02
20.000	−3.111	−201.63
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	0.174	180.00
7.500	0.174	81.36
15.000	0.066	−17.84
22.500	−0.744	−117.12
30.000	−2.949	−215.79
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.232	180.00
10.000	0.232	75.98
20.000	0.219	−29.26
30.000	−0.599	−134.63
40.000	−3.031	−239.09

PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.1µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ −2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 3 should be connected to the analog ground plane. For single supply operation pin 3 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, pin 3 should be biased at 2V. This minimizes passband gain and phase variations.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 25:1 ratio and pin 10 at V^- gives a 50:1 ratio. For single supply operation the ratio is 25:1 when pin 10 is at V^+ and 50:1 when pin 10 is at ground. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1µF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

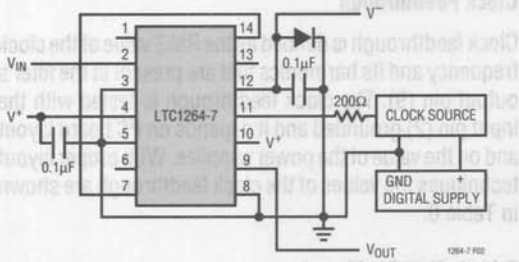

Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 25:1

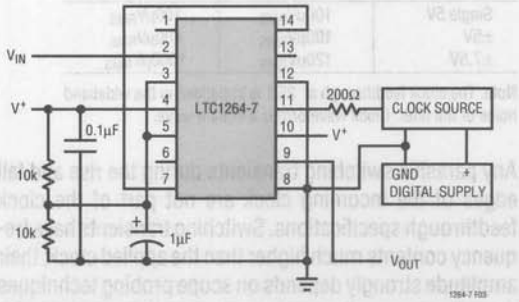

Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 25:1

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PIN FUNCTIONS

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

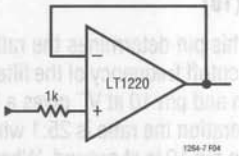

Figure 4. Buffer for Filter Output

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pin (1, 5, 8, 13)

Pins 1, 5, 8 and 13 are not connected to any internal circuit point on the device and should be preferably tied to analog ground.

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	25:1	50:1
Single 5V	$100\mu V_{RMS}$	$100\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$400\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$1000\mu V_{RMS}$

Note: The clock feedthrough at 25:1 is imbedded in the wideband noise of the filter. Clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1264-7 wideband noise at ±5V supply is $160\mu V_{RMS}$, $145\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

APPLICATIONS INFORMATION

Table 9. Maximum V_{IN} vs V_S and Clock

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	5.0MHz	$1.6V_{RMS}$ ($f_{IN} \geq 160kHz$)
	4.5MHz	$2.0V_{RMS}$ ($f_{IN} \geq 160kHz$)
	4.0MHz	$2.5V_{RMS}$ ($f_{IN} \geq 160kHz$)
	≥3.5MHz	$1.6V_{RMS}$ ($f_{IN} \geq 500kHz$)
±5V	3.0MHz	$1.6V_{RMS}$ ($f_{IN} \geq 100kHz$)
	≥3.0MHz	$0.7V_{RMS}$ ($f_{IN} \geq 500kHz$)
Single 5V	2.0MHz	$0.5V_{RMS}$ ($f_{IN} \geq 400kHz$)

Transient Response

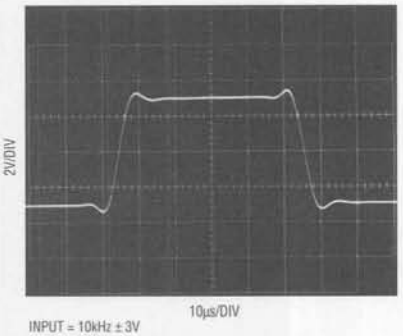

Figure 5.

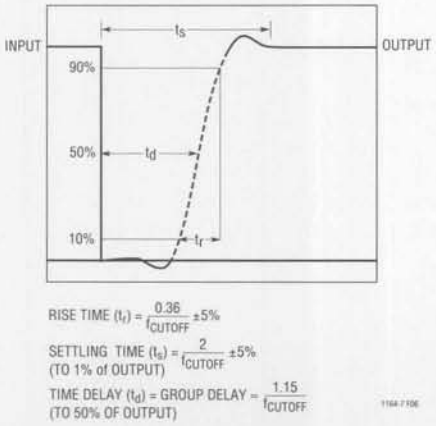

Figure 6.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1264-7 case at 50:1, an input signal whose frequency is in the range of $f_{CLK} \pm 10\%$, will be aliased back into the filter's passband. If, for instance, an LTC1264-7 operating with a 100kHz clock and 2kHz cutoff frequency receives a 95kHz 10mV input signal, a 5kHz $56\mu V_{RMS}$ alias signal will appear at its output. When the LTC1264-7 operates with a clock-to-cutoff frequency of 25:1, aliasing occurs at twice the clock frequency. Table 10 shows details.

Table 10. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = $1V_{RMS}$, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = $1V_{RMS}$) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
25:1, f_{CUTOFF} = 4kHz		
175 (or 225)	–76	25
180 (or 220)	–69	20
185 (or 215)	–62	15
190 (or 210)	–43	10
195 (or 205)	–7	5
50:1, f_{CUTOFF} = 2kHz		
75 (or 125)	–96	25
80 (or 120)	–90	20
85 (or 115)	–82	15
90 (or 110)	–72	10
95 (or 105)	–45	5
99 (or 101)	0	1

Table 11. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

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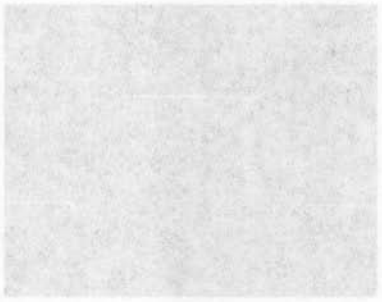

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

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PROPRIETARY PRODUCTS
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LTC694-3.3/LTC695-3.3, 3.3V Microprocessor Supervisory Circuits 9-19

LTC Family of Supervisory Circuit Products

FUNCTION	1235	690	691	692	693	694/694-3.3	695/695-3.3	699	1232
Pushbutton Reset	X								X
Battery Backup Switching-**UL Recognized**	X	X	X	X	X	X	X		
Conditional Battery Backup	X								
RAM Write Protect	X		X		X		X		
Watchdog Timer	X	X	X	X	X	X	X	X	X
Power Fail Warning	X	X	X	X	X	X	X		
Power Up/Down Reset	X	X	X	X	X	X	X	X	X
Reset Threshold (V)	4.65	4.65	4.65	4.40	4.40	4.65/2.90	4.65/2.90	4.65	4.62[1]
Reset Pulse Width (ms)	200	50	50	200	200	200	200	200	610
Guaranteed V_{CC} Reset Level (V)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Supply Current (µA)	600	600	600	600	600	600	600	600	500
Packages: Plastic	16	8	16	8	16	8	16	8	8
Ceramic DIP		8	16			8	16		
SOIC	16[2]	8[3]	16[2]	8[3]	16[2]	8[3]	16[2]	8[3]	8[3]
Temperature Ranges	C	C, I	C, I	C, I	C, I	C, I	C, I	C	C

Notes: 1. 4.62V or 4.37V threshold selectable
2. 0.3" wide SOL package
3. 0.15" wide SO package
4. Temperature ranges: C = 0°C to 70°C I = –40°C to 85°C M = –55°C to 125°C

Definitions of Functions

Pushbutton Reset: Provides a manual reset input, usually triggered by a pushbutton switch, which is debounced and will initiate the usual reset sequence.

Battery Backup Switching: When V_{CC} drops below the battery voltage, V_{OUT} is connected to V_{BATT} and the device is placed in standby mode to conserve power. This provides backup power to the CMOS RAM while consuming less than 1µA of supply current. LTC devices are UL recognized for lithium battery backup.

Conditional Battery Backup: Electrically disconnects the battery during shipment and storage to prevent unnecessary discharge. Disconnection is done by detecting the power down sequencing of the supply and battery inputs.

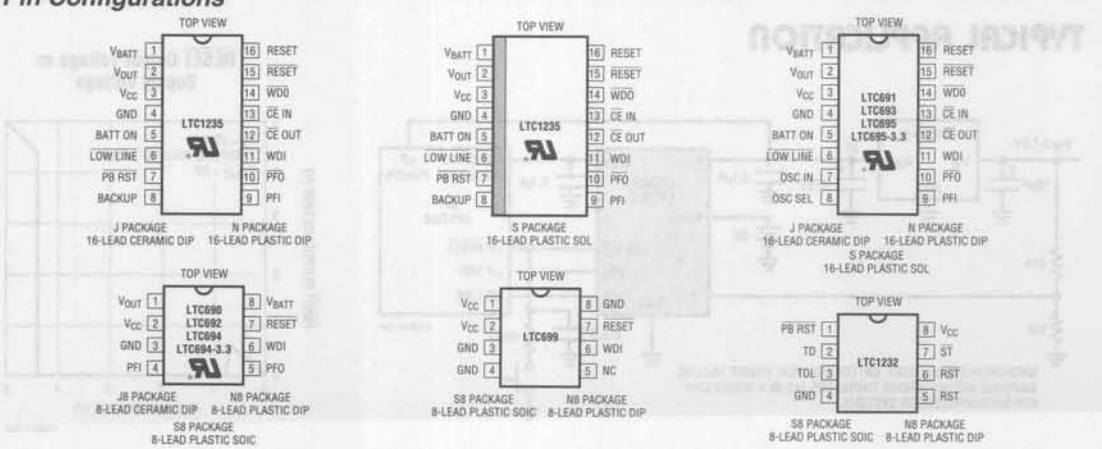
RAM Write Protect: The system RAM enable line is gated by the supervisory circuit. When the supply voltage drops below the reset voltage threshold, the enable line is inhibited, preventing erroneous data from being written into the RAM when V_{CC} is at an invalid level. The maximum enable delay for LTC's supervisors is 45ns.

Watchdog Timer: Monitors the activity of the µP. The processor must toggle this input line before the given timeout period expires, or a reset will be initiated. This function is intended to prevent µP's from becoming accidentally stalled in microcode loops indefinitely.

Power Fail Warning: Provides early warning to the µP of an impending power failure by monitoring the unregulated power supply. This gives the processor time to perform shutdown activities before all regulated power is lost.

Power Up/Down Reset: Resets the µP when the power supply line drops below the preset threshold. LTC's supervisors will hold the reset line low down to supply voltages of 1.0V, providing a reliable reset through V_{CC} voltages which may allow the processor to begin operation.

Pin Configurations



Microprocessor Supervisory Circuits

FEATURES

- UL Recognized
- *Guaranteed* Reset Assertion at V_{CC} = 1V
- 1.5mA Maximum Supply Current
- Fast (35ns Max.) On-Board Gating of RAM Chip Enable Signals
- SO8 and SO16 Packaging
- 4.40V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms or Adjustable
- Minimum External Component Count
- 1µA Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature
- Superior Upgrade for MAX690 Family

APPLICATIONS

- Critical µP Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

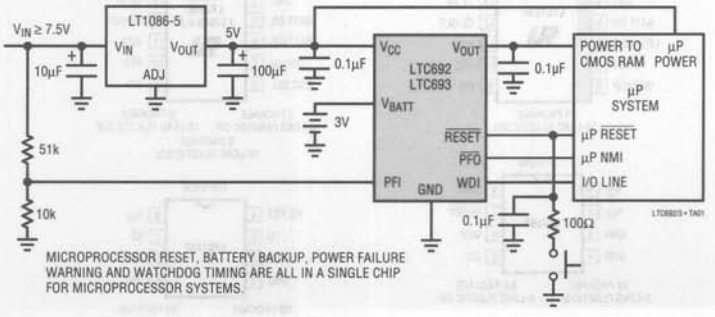
DESCRIPTION

The LTC692/LTC693 provide complete power supply monitoring and battery control functions for microprocessor reset, battery backup, CMOS RAM write protection, power failure warning and watchdog timing. A precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the reset outputs are forced to active states and the Chip Enable output unconditionally write-protects external memory. In addition, the $\overline{\text{RESET}}$ output is guaranteed to remain logic low even with V_{CC} as low as 1V.

The LTC692/LTC693 power the active CMOS RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, powers the RAMs in standby through an efficient PMOS switch.

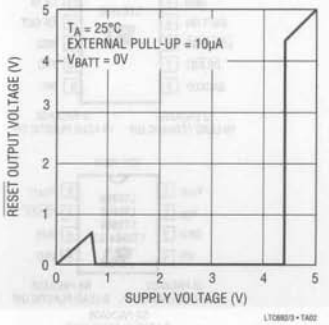
For an early warning of impending power failure, the LTC692/LTC963 provide an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to a preset time-out period.

TYPICAL APPLICATION



MICROPROCESSOR RESET, BATTERY BACKUP, POWER FAILURE WARNING AND WATCHDOG TIMING ARE ALL IN A SINGLE CHIP FOR MICROPROCESSOR SYSTEMS.

$\overline{\text{RESET}}$ Output Voltage vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Terminal Voltage
- V_{CC} ..... −0.3V to 6.0V
- V_{BATT} ..... −0.3V to 6.0V
- All Other Inputs ..... −0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

V_{OUT} Output Current ..... Short Circuit Protected
Power Dissipation 500mW
Operating Temperature Range
- LTC692C/LTC693C ..... 0°C to 70°C
- LTC692I/LTC693I ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

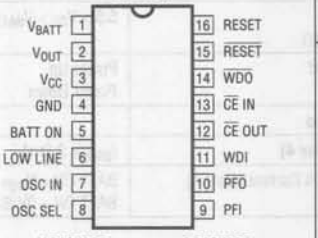
PACKAGE/ORDER INFORMATION (Note 3)

N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 110°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 180°C/W (S)
S8 Package Conditions: PCB Mount on FR4 Material, Still Air at 25°C, Copper Trace

ORDER PART NUMBER
LTC692CN8
LTC692IN8
LTC692CS8
LTC692IS8

S8 PART MARKING
692
692I



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 130°C/W (N, S)
S16 Package Conditions: PCB Mount on FR4 Material, Still Air at 25°C, Copper Trace

ORDER PART NUMBER
LTC693CN
LTC693IN
LTC693CS
LTC693IS

Consult factory for Military grade parts.

PRODUCT SELECTION GUIDE

	PINS	RESET THRESHOLD (V)	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSHBUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC692	**8**	**4.40**	**X**	**X**	**X**			
LTC693	**16**	**4.40**	**X**	**X**	**X**	**X**		
LTC690	8	4.65	X	X	X			
LTC691	16	4.65	X	X	X	X		
LTC694	8	4.65	X	X	X			
LTC695	16	4.65	X	X	X	X		
LTC699	8	4.65	X					
LTC1232	8	4.37/4.62	X				X	
LTC1235	16	4.65	X	X	X	X	X	X
LTC694-3.3	8	2.90	X	X	X			
LTC695-3.3	16	2.90	X	X	X	X		

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ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range V_{CC} V_{BATT}			 4.50 2.00		 5.50 4.00	 V V
V_{OUT} Output Voltage	I_{OUT} = 1mA	 ●	V_{CC} – 0.05 V_{CC} – 0.10	V_{CC} – 0.005 V_{CC} – 0.005		V V
	I_{OUT} = 50mA		V_{CC} – 0.50	V_{CC} – 0.250		V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT}		V_{BATT} – 0.1	V_{BATT} – 0.02		V
Supply Current (Exclude I_{OUT})	I_{OUT} ≤ 50mA	 ●		0.6 0.6	1.5 2.5	mA mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V	 ●		0.04 0.04	1 5	µA µA
Battery Standby Current (+ = Discharge, – = Charge)	5.5 > V_{CC} > V_{BATT} + 0.2V	 ●	–0.1 –1.0		0.02 0.10	µA µA
Battery Switchover Threshold V_{CC} – V_{BATT}	Power Up Power Down			70 50		mV mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 4)	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current (Note 4)	BATT ON = V_{OUT} Sink Current BATT ON = 0V Source Current		 0.5	35 1	 25	mA µA
Reset and Watchdog Timer						
Reset Voltage Threshold		●	4.25	4.40	4.50	V
Reset Threshold Hysteresis				40		mV
Reset Active Time (Note 5)	OSC SEL HIGH, V_{CC} = 5V	 ●	160 140	200 200	240 280	ms ms
Watchdog Time-Out Period, Internal Oscillator	Long Period, V_{CC} = 5V	 ●	1.2 1.0	1.6 1.6	2.00 2.25	sec sec
	Short Period, V_{CC} = 5V	 ●	80 70	100 100	120 140	ms ms
Watchdog Time-Out Period, External Clock (Note 6)	Long Period Short Period		4032 960		4097 1025	Clock Cycles
Reset Active Time PSRR				1		ms/V
Watchdog Time-Out Period PSRR, Internal OSC				1		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3.5V	●	200			ns
$\overline{\text{RESET}}$ Output Voltage At V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V			4	200	mV
$\overline{\text{RESET}}$ and $\overline{\text{LOW LINE}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1µA, V_{CC} = 5V	 	 3.5		0.4 	V V
RESET and $\overline{\text{WDO}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1µA, V_{CC} = 4.25V	 	 3.5		0.4 	V V

ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
RESET, $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, $\overline{\text{LOW LINE}}$ Output Short-Circuit Current (Note 4)	Output Source Current Output Sink Current		1	3 25	25	µA mA
WDI Input Threshold	Logic Low Logic High		 3.5		0.8	V V
WDI Input Current	WDI = V_{OUT} WDI = 0V	● ●	 –50	4 –8	50	µA µA
Power Fail Detector						
PFI Input Threshold	V_{CC} = 5V	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				±0.01	±25	nA
$\overline{\text{PFO}}$ Output Voltage (Note 4)	I_{SINK} = 3.2mA I_{SOURCE} = 1µA		 3.5		0.4	V V
$\overline{\text{PFO}}$ Short Circuit Source Current (Note 4)	PFI = HIGH, $\overline{\text{PFO}}$ = 0V PFI = LOW, $\overline{\text{PFO}}$ = V_{OUT}		1	3 25	25	µA mA
PFI Comparator Response Time (falling)	ΔV_{IN} = –20mV, V_{OD} = 15mV			2		µs
PFI Comparator Response Time (rising) (Note 4)	ΔV_{IN} = 20mV, V_{OD} = 15mV with 10kΩ Pull-Up			40 8		µs µs
Chip Enable Gating						
$\overline{\text{CE}}$ IN Threshold	V_{IL} V_{IH}		 2.0		0.8	V V
$\overline{\text{CE}}$ IN Pullup Current (Note 7)				3		µA
$\overline{\text{CE}}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1µA, V_{CC} = 0V		 V_{OUT} – 1.50 V_{OUT} – 0.05		0.4	V V V
$\overline{\text{CE}}$ Propagation Delay	V_{CC} = 5V, C_L = 20pF	 ●		20 20	35 45	ns ns
$\overline{\text{CE}}$ OUT Output Short Circuit Current	Output Source Current Output Sink Current			30 35		mA mA
Oscillator						
OSC IN Input Current (Note 7)				±2		µA
OSC SEL Input Pull-Up Current (Note 7)				5		µA
OSC IN Frequency Range	OSC SEL = 0V	●	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, C_{OSC} = 47pF			4		kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range, consult the factory.

Note 4: The output pins of BATT ON, $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, $\overline{\text{WDO}}$, $\overline{\text{RESET}}$ and RESET have weak internal pull-ups of typically 3µA. However, external pull-up resistors may be used when higher speed is required.

Note 5: The LTC692/LTC693 have minimum reset active times of 140ms (200ms typically). The reset active time of the LTC693 can be adjusted (see Table 2 in Applications Information Section).

Note 6: The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer (See BLOCK DIAGRAM). Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 clocks plus one clock of jitter.

Note 7: The input pins of $\overline{\text{CE}}$ IN, OSC IN and OSC SEL have weak internal pull-ups which pull to the supply when the input pins are floating.

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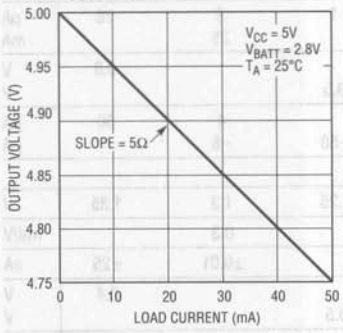
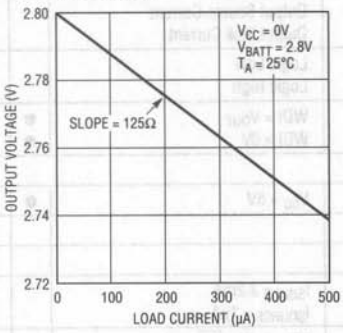
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} vs I_{OUT}



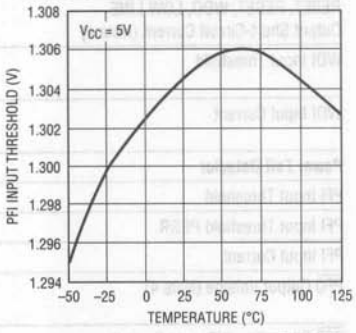
LTC692/3 • TPC01

V_{OUT} vs I_{OUT}



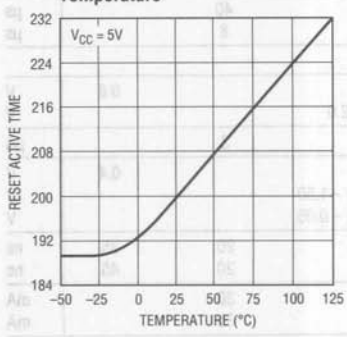
LTC692/3 • TPC02

Power Failure Input Threshold vs Temperature



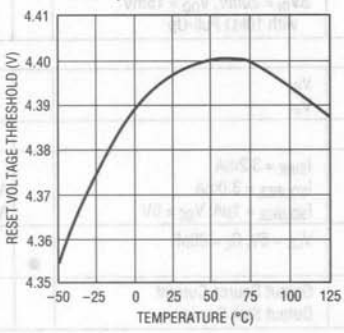
LTC692/3 • TPC03

Reset Active Time vs Temperature



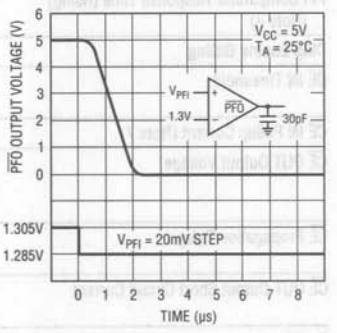
LTC692/3 • TPC04

Reset Voltage Threshold vs Temperature



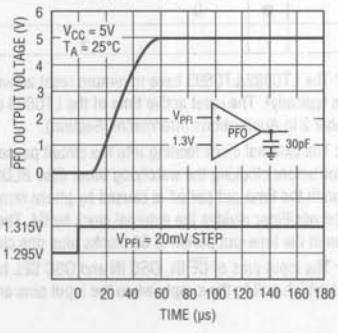
LTC692/3 • TPC05

Power Fail Comparator Response Time



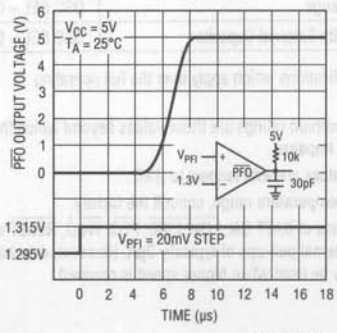
LTC692/3 • TPC06

Power Fail Comparator Response Time



LTC692/3 • TPC07

Power Fail Comparator Response Time with Pull-Up Resistor



LTC692/3 • TPC08

PIN FUNCTIONS

V_{CC}: 5V Supply Input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

V_{OUT}: Voltage Output for Backed Up Memory. Bypass with a capacitor of 0.1µF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical ON resistance of 5Ω. When V_{CC} is lower than V_{BATT}, V_{OUT} is internally switched to V_{BATT}. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{BATT}: Backup Battery Input. When V_{CC} falls below V_{BATT}, auxiliary power connected to V_{BATT}, is delivered to V_{OUT} through PMOS switch, M2. If backup battery or auxiliary power is not used, V_{BATT} should be connected to GND.

GND: Ground Pin.

BATT ON: Battery On Logic Output from Comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{OUT} is internally switched to V_{BATT}.

PFI: Power Failure Input. PFI is the noninverting input to the Power Fail Comparator, C3. The inverting input is internally connected to a 1.3V reference. The Power Failure Output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

$\overline{PFO}$: Power Failure Output from C3. $\overline{PFO}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{PFO}$ is forced low.

$\overline{RESET}$: Logic Output for µP Reset Control. Whenever V_{CC} falls below either the reset voltage threshold (4.40V typically) or V_{BATT}, $\overline{RESET}$ goes active low. After V_{CC} returns to 5V, reset pulse generator forces $\overline{RESET}$ to remain active low for a minimum of 140ms. When the watchdog timer is enabled but not serviced prior to a preset time-out period, reset pulse generator also forces $\overline{RESET}$ to active low for a minimum of 140ms for every preset time-out period (see Figure 11). The reset active time is adjustable on the LTC693. An external pushbutton reset can be used in connection with the $\overline{RESET}$ output. See Pushbutton Reset in the Applications Information section.

RESET: RESET is an Active High Logic Ouput. It is the inverse of $\overline{RESET}$.

$\overline{LOW\ LINE}$: Logic Output from Comparator C1. $\overline{LOW\ LINE}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (4.40V typically), $\overline{LOW\ LINE}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{LOW\ LINE}$ returns high (see Figure 1). $\overline{LOW\ LINE}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

WDI: Watchdog Input. WDI is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{RESET}$ and $\overline{WDO}$ low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 11).

$\overline{WDO}$: Watchdog Logic Output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{WDO}$ goes low. $\overline{WDO}$ is set high whenever there is a transition on the WDI pin, or $\overline{LOW\ LINE}$ goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

$\overline{CE}$ IN: Logic Input to the Chip Enable Gating Circuit. $\overline{CE}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information Section and Figure 5 for additional information.

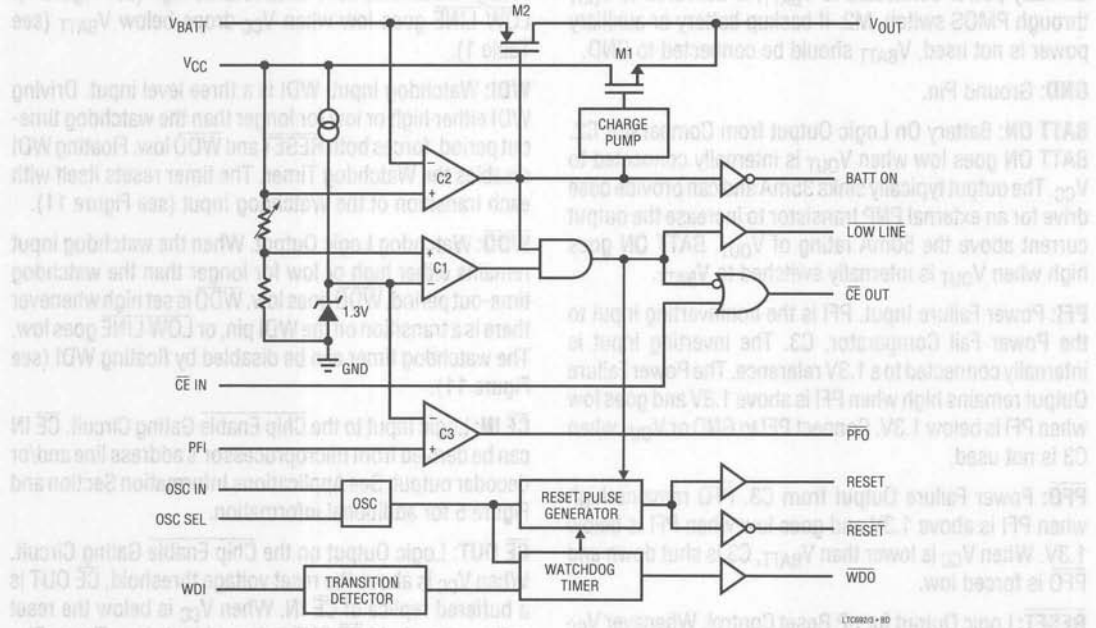
$\overline{CE}$ OUT: Logic Output on the Chip Enable Gating Circuit. When V_{CC} is above the reset voltage threshold, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN. When V_{CC} is below the reset voltage threshold $\overline{CE}$ OUT is forced high (see Figure 5).

OSC SEL: Oscillator Selection Input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low allows OSC IN to be driven from an external clock signal or an external capacitor to be connected between OSC IN and GND.

PIN FUNCTIONS

OSC IN: Oscillator Input. OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In this configuration the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula (see Applications Information section). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 200ms typical. OSC IN selects between the 1.6 seconds and 100ms typical watchdog time-out periods. In both cases the time-out period immediately after a reset is 1.6 seconds typical.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Microprocessor Reset

The LTC692/LTC693 use a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the reset voltage threshold, the $\overline{RESET}$ output is forced to active low state. The reset voltage threshold accounts for a 10% variation on V_{CC}, so the $\overline{RESET}$ output becomes active low when V_{CC} falls below 4.50V (4.40V typical). On power-up, the $\overline{RESET}$ signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. The reset active time is adjustable on the LTC693. On power-down, the $\overline{RESET}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{RESET}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at the V_{CC} pin do not activate the $\overline{RESET}$ output. Response time is typically 10µs. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

The LTC693 has two additional outputs: RESET and $\overline{LOW\ LINE}$. RESET is an active high output and is the inverse of $\overline{RESET}$. $\overline{LOW\ LINE}$ is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, $\overline{LOW\ LINE}$ goes low. $\overline{LOW\ LINE}$ returns high as soon as V_{CC} rises above the reset voltage threshold.

Battery Switchover

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. When V_{CC} rises to 70mV above V_{BATT}, the battery switchover comparator, C2, connects V_{OUT} to V_{CC} through a charge pumped NMOS power switch, M1. When V_{CC} falls to 50mV above V_{BATT}, C2 connects V_{OUT} to V_{BATT} through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT}. The response time of C2 is approximately 20µs.

During normal operation, the LTC692/LTC693 use a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical "on" resistance of 5Ω. The V_{OUT} pin should be bypassed with a capacitor of 0.1µF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout ($V_{CC} - V_{OUT}$ voltage differential) is desired, the LTC693 should be used. This product provides BATT ON output to drive the base of the external PNP transistor (Figure 2). If higher currents are needed with the LTC692, a high current Schottky diode can be connected from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

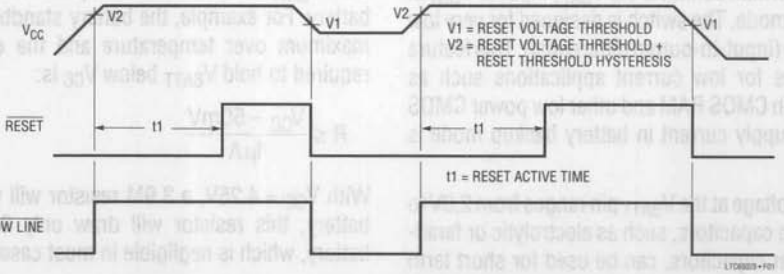


Figure 1. Reset Active Time

APPLICATIONS INFORMATION

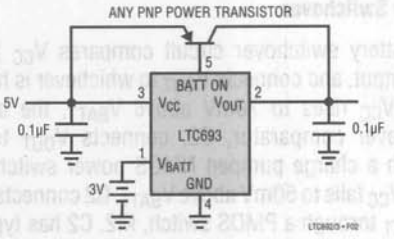


Figure 2. Using BATT ON to Drive External PNP Transistor

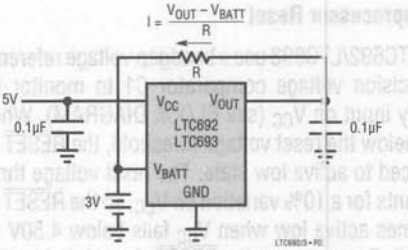


Figure 3. Charging External Battery Through V_{OUT}

The LTC692/LTC693 are protected for safe area operation with a short circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for long periods of time, thermal shutdown turns the power switch off until the device cools down. The threshhold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. The LTC692/LTC693 use a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by the V_{BATT} pin is strictly junction leakage.

A 125Ω PMOS switch connects the V_{BATT} input to V_{OUT} in battery backup mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. The supply current in battery backup mode is 1µA maximum.

The operating voltage at the V_{BATT} pin ranges from 2.0V to 4.0V. High value capacitors, such as electrolytic or farad-size double layer capacitors, can be used for short term memory backup instead of a battery. The charging resistor for the rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists when the resistor is connected to V_{CC} (Figure 3).

Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur while the battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC692/LTC693 switch to battery backup. V_{OUT} pulls V_{BATT} low and the devices go back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature and the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \leq \frac{V_{CC} - 50mV}{1\mu A}$$

With V_{CC} = 4.25V, a 3.9M resistor will work. With a 3V battery, this resistor will draw only 0.77µA from the battery, which is negligible in most cases.

APPLICATIONS INFORMATION

If battery connections are made through long wires, a 10Ω to 100Ω series resistor and a 0.1μF capacitor are recommended to prevent any overshoot beyond V_{CC} due to the lead inductance (Figure 4).

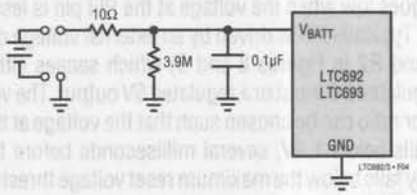


Figure 4. 10Ω/0.1μF combination eliminates inductive overshoot and prevents spurious resets during battery replacement.

Table 1 shows the state of each pin during battery backup. When the battery switchover section is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Memory Protection

The LTC693 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Two additional pins, $\overline{CE}$ IN and $\overline{CE}$ OUT, control the Chip Enable or Write inputs of CMOS RAM. When V_{CC} is 5V, $\overline{CE}$ OUT follows $\overline{CE}$ IN with a typical propagation delay of 20ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{CE}$ OUT is forced high, independent of $\overline{CE}$ IN. $\overline{CE}$ OUT is an alternative signal to drive the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery backed up CMOS RAM. $\overline{CE}$ OUT can also be used to drive the $\overline{Store}$ or $\overline{Write}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 5 shows the timing diagram of $\overline{CE}$ IN and $\overline{CE}$ OUT.

$\overline{CE}$ IN can be derived from the microprocessor's address decoder output. Figure 6 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC692 by using $\overline{RESET}$ as shown in Figure 7.

Table 1. Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1μA maximum.
BATT ON	Logic high. The open-circuit output voltage is equal to V_{OUT}.
PFI	Power Failure Input is ignored.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
WDI	Watchdog Input is ignored.
$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{CE}$ IN	Chip Enable Input is ignored.
$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

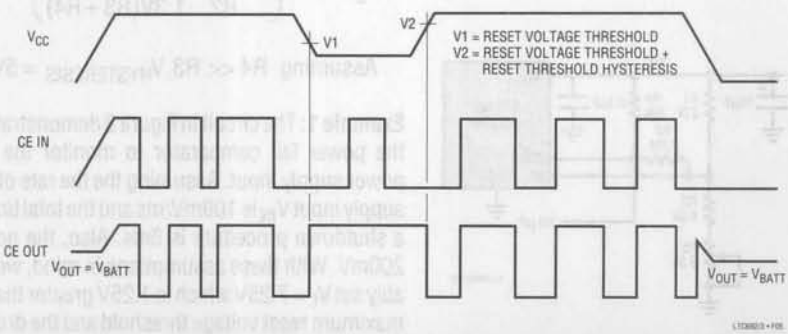


Figure 5. Timing Diagram for $\overline{CE}$ IN and $\overline{CE}$ OUT

APPLICATIONS INFORMATION

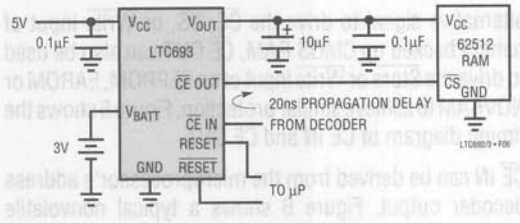


Figure 6. A Typical Nonvolatile CMOS RAM Application

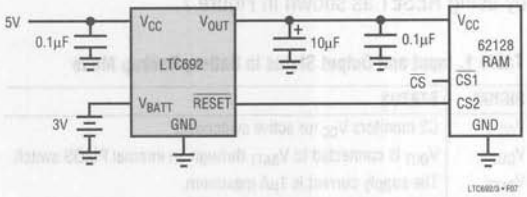


Figure 7. Write Protect for RAM with the LTC692

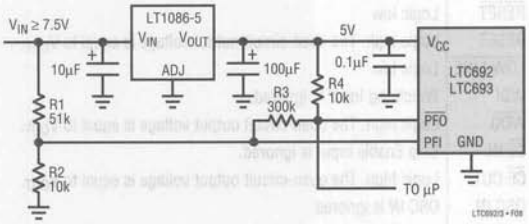


Figure 8. Monitoring *Unregulated* DC Supply with the LTC692/LTC693 Power Fail Comparator

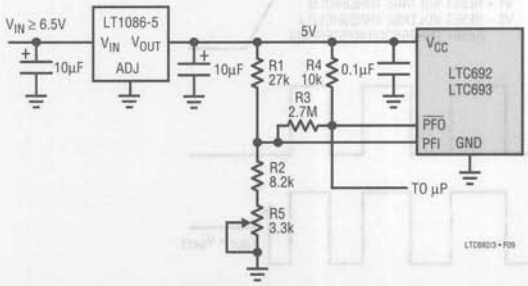


Figure 9. Monitoring *Regulated* DC Supply with the LTC692/LTC693 Power Fail Comparator

Power Fail Warning

The LTC692/LTC693 generate a Power Failure Output ($\overline{PFO}$) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. $\overline{PFO}$ goes low when the voltage at the PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage at the PFI pin falls below 1.3V, several milliseconds before the 5V supply falls below the maximum reset voltage threshold of 4.50V. $\overline{PFO}$ is normally used to interrupt the microprocessor to execute shutdown procedure between $\overline{PFO}$ and $\overline{RESET}$ or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{PFO}$ output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When $\overline{PFO}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right)$$

When $\overline{PFO}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1+\frac{R1}{R2}-\frac{(5V-1.3V)R1}{1.3V(R3+R4)}\right)$$

$$\text{Assuming } R4 << R3, V_{HYSTERESIS} = 5V\frac{R1}{R3}$$

Example 1: The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shutdown procedure is 8ms. Also, the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 7.25V which is 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage of LT1086-5 (4.5V + 1.5V) and $V_{HYSTERESIS}$ = 850mV.

APPLICATIONS INFORMATION

$$V_{HYSTERESIS} = 5V\frac{R1}{R3} = 850mV$$

$$R3 \approx 5.88\ R1$$

Choose R3 = 300k and R1 = 51k. Also select R4 = 10k which is much smaller than R3.

$$7.25V = 1.3V\left(1+\frac{51k}{R2}-\frac{(5V-1.3V)51k}{1.3V(310k)}\right)$$

R2 = 10.1k, Choose nearest 5% resistor 10k and recalculate V_L,

$$V_L = 1.3V\left(1+\frac{51k}{10k}-\frac{(5V-1.3V)51k}{1.3V(310k)}\right) = 7.32V$$

$$V_H = 1.3V\left(1+\frac{51k}{10k}+\frac{51k}{300k}\right) = 8.151V$$

$$\frac{(7.32V-6.25V)}{100mV/ms} = 10.7ms$$

$$V_{HYSTERESIS} = 8.151V - 7.32V = 831mV$$

The 10.7ms allows enough time to execute shutdown procedure for microprocessor and 831mV of hysteresis would prevent $\overline{PFO}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 9 can be used to measure the regulated 5V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{PFO}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 4.6V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 10). If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

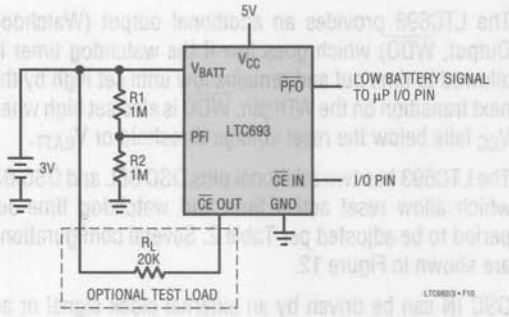


Figure 10. Backup Battery Monitor with Optional Test Load

Watchdog Timer

The LTC692/LTC693 provide a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within a seleced time-out period, $\overline{RESET}$ is forced to active low for a minimum of 140ms. The reset active time is adjustable on the LTC693. Since many systems cannot service the watchdog timer immediately after a reset, the LTC693 has longer time-out period (1.0 second minimum) right after a reset is issued. The normal time-out period (70ms minimum) becomes effective following the first transition of WDI after $\overline{RESET}$ is inactive. The watchdog time-out period is fixed at a 1.0 second minimum on the LTC692. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as $\overline{RESET}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog timer is reset and begins to time-out again. To ensure the watchdog timer does not time-out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog timer can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

9

APPLICATIONS INFORMATION

The LTC693 provides an additional output (Watchdog Output, $\overline{WDO}$) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{WDO}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The LTC693 has two additonal pins OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 12.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 140ms minimum. OSC IN selects between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

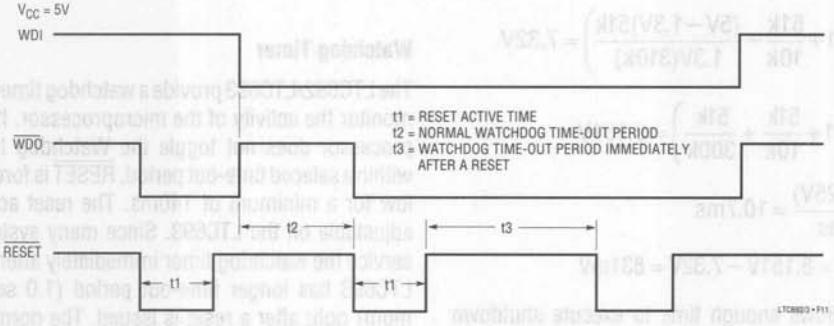


Figure 11. Watchdog Time-out Period and Reset Active Time

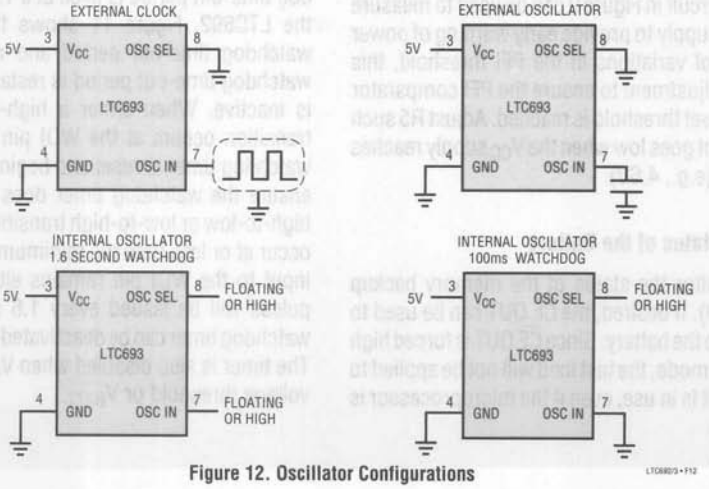


Figure 12. Oscillator Configurations

APPLICATIONS INFORMATION

Table 2. LTC693 Reset Active Time and Watchdog Time-Out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC693
Low	External Clock Input	1024 clks	4096 clks	2048 clks
Low	External Capacitor*	$\frac{400ms}{70pF} \times C$	$\frac{1.6\ sec}{70pF} \times C$	$\frac{800ms}{70pF} \times C$
Floating or High	Low	100ms	1.6 sec	200ms
Floating or High	Floating or High	1.6 sec	1.6 sec	200ms

*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is F_{OSC} (Hz) = $\frac{184,000}{C(pF)}$

Pushbutton Reset

The LTC692/LTC693 do not provide a logic input for direct connection to a pushbutton. However, a pushbutton in series with a 100Ω resistor connected to the $\overline{RESET}$ output pin (Figure 13) provides an alternative for manual reset. Connecting a 0.1µF capacitor to the $\overline{RESET}$ pin debounces the pushbutton input.

The 100Ω resistor in series with the pushbutton is required to prevent the ringing, due to the capacitance and lead inductance, from pulling the $\overline{RESET}$ pins of the MPU and LTC692/LT693 below ground.

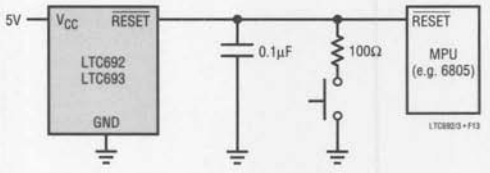
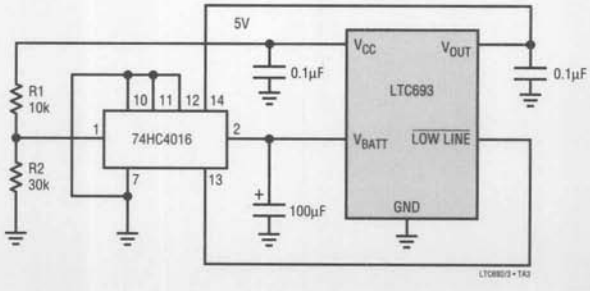


Figure 13. The External Pushbutton Reset

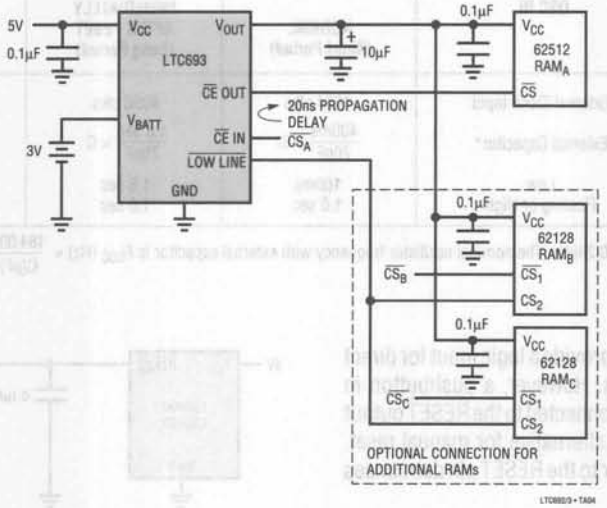
TYPICAL APPLICATIONS

Capacitor Backup with 74HC4016 Switch



TYPICAL APPLICATIONS

Write Protect for Additional RAMs



3.3V Microprocessor Supervisory Circuits

FEATURES

- *Guaranteed* Reset Assertion at V_{CC} = 1V
- Pin Compatible with LTC694/LTC695 for 3.3V Systems
- 200µA Typical Supply Current
- Fast (30ns Typ) On-Board Gating of RAM Chip Enable Signals
- SO-8 and SO-16 Packages
- 2.90V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms or Adjustable
- Minimum External Component Count
- 1µA Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature

APPLICATIONS

- 3.3V Low Power Systems
- Critical µP Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

DESCRIPTION

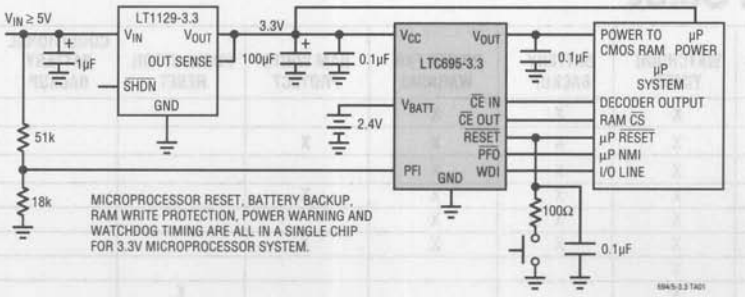
The LTC694-3.3/LTC695-3.3 provide complete 3.3V power supply monitoring and battery control functions. These include power-on reset, battery backup, RAM write protection, power failure warning and watchdog timing. The devices are pin compatible upgrades of the LTC694/LTC695 that are optimized for 3.3V systems. Operating power consumption has been reduced to 0.6mW (typical) and 3µW maximum in battery backup mode. Microprocessor reset and memory write protection are provided when the supply falls below 2.9V. The $\overline{\text{RESET}}$ output is guaranteed to remain logic low with V_{CC} as low as 1V.

The LTC694-3.3/LTC695-3.3 power the active RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, powers the RAMs in standby through an efficient PMOS switch.

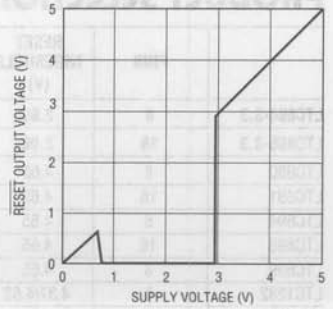
For an early warning of impending power failure, the LTC694-3.3/LTC695-3.3 provide an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to a preset time-out period.

9

TYPICAL APPLICATION



RESET Output Voltage vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

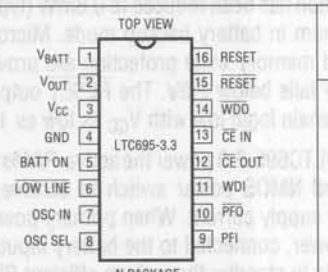
Terminal Voltage
- V_{CC} ..... −0.3V to 6V
- V_{BATT} ..... −0.3V to 6V
- All Other Inputs ..... −0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} 100mA
- V_{BATT} 25mA
- GND 10mA

V_{OUT} Output Current ..... Short-Circuit Protected
Power Dissipation 500mW
Operating Temperature Range
- LTC694C-3.3/LTC695C-3.3 ..... 0°C to 70°C
- LTC694I-3.3/LTC695I-3.3 ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION (Note 3)

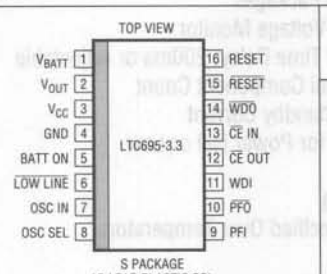


N PACKAGE
16-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC695CN-3.3
LTC695IN-3.3

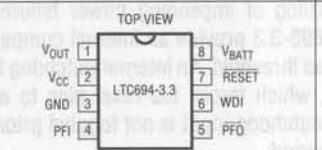


S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

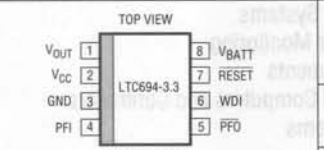
LTC695CS-3.3
LTC695IS-3.3



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

LTC694CN-3.3
LTC694IN-3.3



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 110°C, θ_{JA} = 180°C/W

LTC694CS-3.3
LTC694IS-3.3

S8 PART MARKING

694
694I

Consult factory for Military grade parts.

PRODUCT SELECTION GUIDE

	PINS	RESET THRESHOLD (V)	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSHBUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC694-3.3	**8**	**2.90**	**X**	**X**	**X**			
LTC695-3.3	**16**	**2.90**	**X**	**X**	**X**	**X**		
LTC690	8	4.65	X	X	X			
LTC691	16	4.65	X	X	X	X		
LTC694	8	4.65	X	X	X			
LTC695	16	4.65	X	X	X	X		
LTC699	8	4.65	X					
LTC1232	8	4.37/4.62	X				X	
LTC1235	16	4.65	X	X	X	X	X	X

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{BATT} = 2V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range						
V_{CC}		●	3.0		5.50	V
V_{BATT}		●	1.5		2.75	V
V_{OUT} Output Voltage	I_{OUT} = 1mA		V_{CC} – 0.1	V_{CC} – 0.01		V
		●	V_{CC} – 0.2	V_{CC} – 0.01		V
	I_{OUT} = 50mA	●	V_{CC} – 0.8	V_{CC} – 0.4		V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT}	●	V_{BATT} – 0.1	V_{BATT} – 0.02		V
Supply Current (Exclude I_{OUT})	I_{OUT} ≤ 50mA, V_{CC} = 3.6V			0.2	0.6	mA
		●		0.2	1.0	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2V			0.04	1	µA
		●		0.04	5	µA
Battery Standby Current (+ = Discharge, – = Charge)	3.6V > V_{CC} > V_{BATT} + 0.2V		–0.02		0.02	µA
		●	–0.10		0.10	µA
Battery Switchover Threshold (V_{CC} – V_{BATT})	Power Up			70		mV
	Power Down			50		mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 4)	I_{SINK} = 800µA	●			0.3	V
BATT ON Output Short-Circuit Current (Note 4)	BATT ON = V_{OUT}, Sink Current			25		mA
	BATT ON = 0V, Source Current	●	0.5	1	25	µA
Reset and Watchdog Timer						
Reset Voltage Threshold		●	2.8	2.9	3.0	V
Reset Threshold Hysteresis				40		mV
Reset Active Time	OSC SEL HIGH, V_{CC} = 3V		160	200	240	ms
		●	140	200	280	ms
Watchdog Time-Out Period, Internal Oscillator	Long Period, V_{CC} = 3V		1.2	1.6	2.0	sec
		●	1.0	1.6	2.25	sec
	Short Period, V_{CC} = 3V		80	100	120	ms
		●	70	100	140	ms
Watchdog Time-Out Period, External Clock (Note 5)	Long Period, V_{CC} = 3V	●	4032		4097	Clock
	Short Period, V_{CC} = 3V	●	960		1025	Cycles
Reset Active Time PSRR				4		ms/V
Watchdog Time-Out Period PSRR, Internal OSC	Short Period			2		ms/V
	Long Period			32		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3V	●	200			ns
$\overline{RESET}$ Output Voltage at V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V	●		4	200	mV
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage (Note 4)	I_{SINK} = 400µA, V_{CC} = 2.8V	●			0.3	V
	I_{SOURCE} = 1µA, V_{CC} = 3V	●	2.3			V
RESET and $\overline{WDO}$ Output Voltage (Note 4)	I_{SINK} = 400µA, V_{CC} = 3V	●			0.3	V
	I_{SOURCE} = 1µA, V_{CC} = 2.8V	●	2.3			V
RESET, $\overline{RESET}$, $\overline{WDO}$, $\overline{LOW\ LINE}$ Output Short-Circuit Current (Note 4)	Output Source Current	●	1	3	25	µA
	Output Sink Current			9		mA

9

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{BATT} = 2V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
WDI Input Threshold	Logic Low	●			0.4	V
	Logic High	●	2.3			V
WDI Input Current	WDI = V_{OUT}	●		4	50	µA
	WDI = 0V	●	–50	–8		µA
Power Fail Detector						
PFI Input Threshold		●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current		●		±0.01	±25	nA
$\overline{PFO}$ Output Voltage (Note 4)	I_{SINK} = 800µA	●			0.3	V
	I_{SOURCE} = 1µA	●	2.3			V
$\overline{PFO}$ Short-Circuit Source Current (Note 4)	PFI = HIGH, $\overline{PFO}$ = 0V	●	1	3	25	µA
	PFI = LOW, $\overline{PFO}$ = V_{OUT}			17		mA
PFI Comparator Response Time (Falling)	ΔV_{IN} = –20mV, V_{OD} = 15mV			2		µs
PFI Comparator Response Time (Rising) (Note 4)	ΔV_{IN} = 20mV, V_{OD} = 15mV			40		µs
	with 10kΩ Pullup			8		µs
Chip Enable Gating						
$\overline{CE}$ IN Threshold	V_{IL}				0.45	V
	V_{IH}		1.9			V
$\overline{CE}$ IN Pullup Current (Note 6)				3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 800µA	●			0.3	V
	I_{SOURCE} = 400µA	●	V_{OUT} – 0.50			V
	I_{SOURCE} = 1µA, V_{CC} = 0V	●	V_{OUT} – 0.05			V
$\overline{CE}$ IN Propagation Delay	C_L = 20pF	●		30	50	ns
$\overline{CE}$ OUT Output Short-Circuit Current	Output Source Current			15		mA
	Output Sink Current			20		mA
Oscillator						
OSC IN Input Current (Note 6)				±2		µA
OSC SEL Input Pullup Current (Note 6)				5		µA
OSC IN Frequency Range	OSC SEL = 0V	●	0		125	kHz
	OSC SEL = 0V, C_{OSC} = 47pF			4		kHz

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range parts, consult the factory.

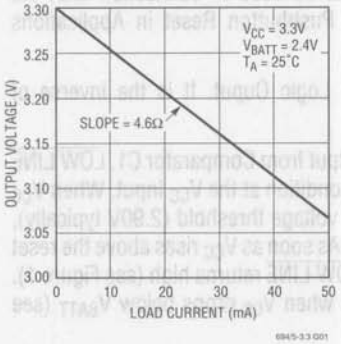
Note 4: The output pins of BATT ON, $\overline{LOW\ LINE}$, $\overline{PFO}$, $\overline{WDO}$, $\overline{RESET}$ and RESET have weak internal pullups of typically 3µA. However, external pullup resistors may be used when higher speed is required.

Note 5: The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer. Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 plus one clock of jitter.

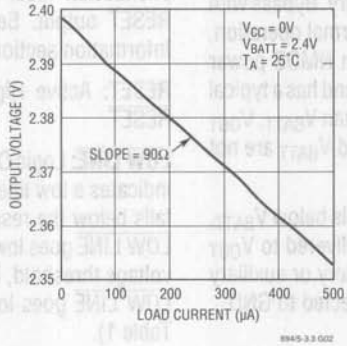
Note 6: The input pins of $\overline{CE}$ IN, OSC IN and OSC SEL have weak internal pullups which pull to the supply when the input pins are floating.

TYPICAL PERFORMANCE CHARACTERISTICS

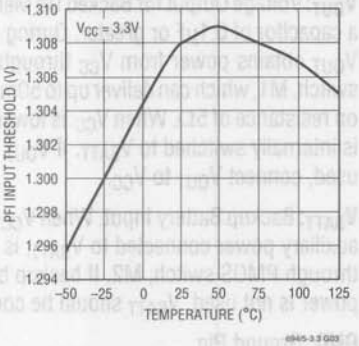
Output Voltage vs Load Current



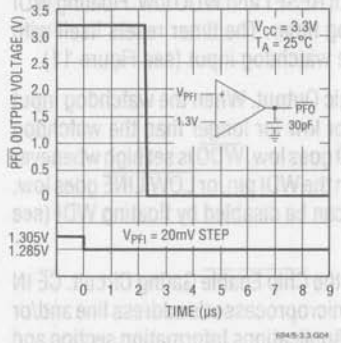
Output Voltage vs Load Current



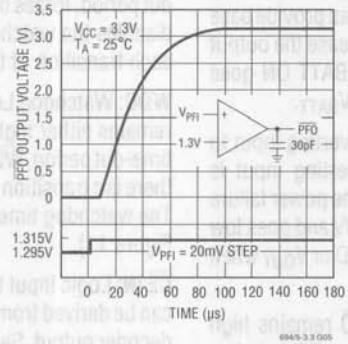
Power Failure Input Threshold vs Temperature



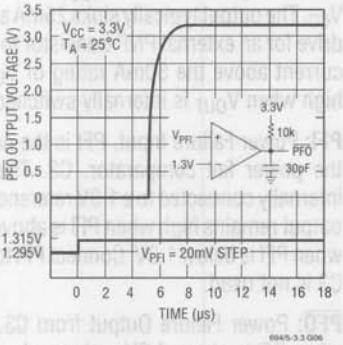
Power Fail Comparator Response Time



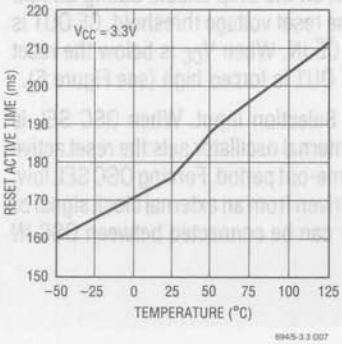
Power Fail Comparator Response Time



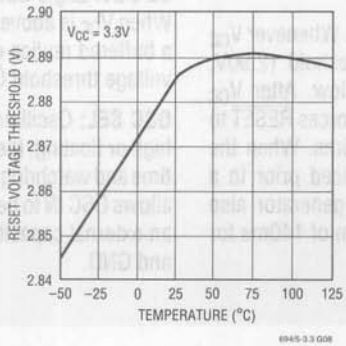
Power Fail Comparator Response Time with Pullup Resistor



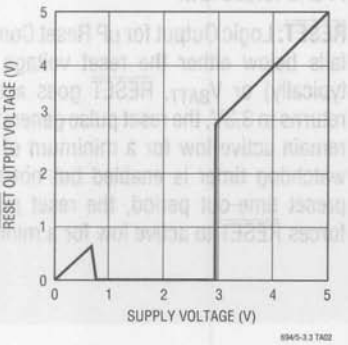
Reset Active Time vs Temperature



Reset Voltage Threshold vs Temperature



RESET Output Voltage vs Supply Voltage



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PIN FUNCTIONS

V_{CC}: 3.3V Supply Input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

V_{OUT}: Voltage Output for Backed Up Memory. Bypass with a capacitor of 0.1µF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V_{CC} is lower than V_{BATT}, V_{OUT} is internally switched to V_{BATT}. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{BATT}: Backup Battery Input. When V_{CC} falls below V_{BATT}, auxiliary power connected to V_{BATT}, is delivered to V_{OUT} through PMOS switch, M2. If backup battery or auxiliary power is not used, V_{BATT} should be connected to GND.

GND: Ground Pin.

BATT ON: Battery On Logic Output from Comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 25mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{OUT} is internally switched to V_{BATT}.

PFI: Power Failure Input. PFI is the noninverting input to the power fail comparator, C3. The inverting input is internally connected to a 1.3V reference. The power failure output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

$\overline{PFO}$: Power Failure Output from C3. $\overline{PFO}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{PFO}$ is forced low.

$\overline{RESET}$: Logic Output for µP Reset Control. Whenever V_{CC} falls below either the reset voltage threshold (2.90V, typically) or V_{BATT}, $\overline{RESET}$ goes active low. After V_{CC} returns to 3.3V, the reset pulse generator forces $\overline{RESET}$ to remain active low for a minimum of 140ms. When the watchdog timer is enabled but not serviced prior to a preset time-out period, the reset pulse generator also forces $\overline{RESET}$ to active low for a minimum of 140ms for every preset time-out period (see Figure 11). The reset active time is adjustable on the LTC695-3.3. An external pushbutton reset can be used in connection with the $\overline{RESET}$ output. See Pushbutton Reset in Applications Information section.

RESET: Active High Logic Ouput. It is the inverse of $\overline{RESET}$.

$\overline{LOW\ LINE}$: Logic Output from Comparator C1. $\overline{LOW\ LINE}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (2.90V typically), $\overline{LOW\ LINE}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{LOW\ LINE}$ returns high (see Figure 1). $\overline{LOW\ LINE}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

WDI: Watchdog Input. WDI is a three-level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{RESET}$ and $\overline{WDO}$ low. Floating WDI disables the watchdog timer. The timer resets itself with each transition of the watchdog input (see Figure 11).

$\overline{WDO}$: Watchdog Logic Output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{WDO}$ goes low. $\overline{WDO}$ is set high whenever there is a transition on the WDI pin, or $\overline{LOW\ LINE}$ goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

$\overline{CE}$ IN: Logic Input to the Chip Enable Gating Circuit. $\overline{CE}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information section and Figure 5 for additional information.

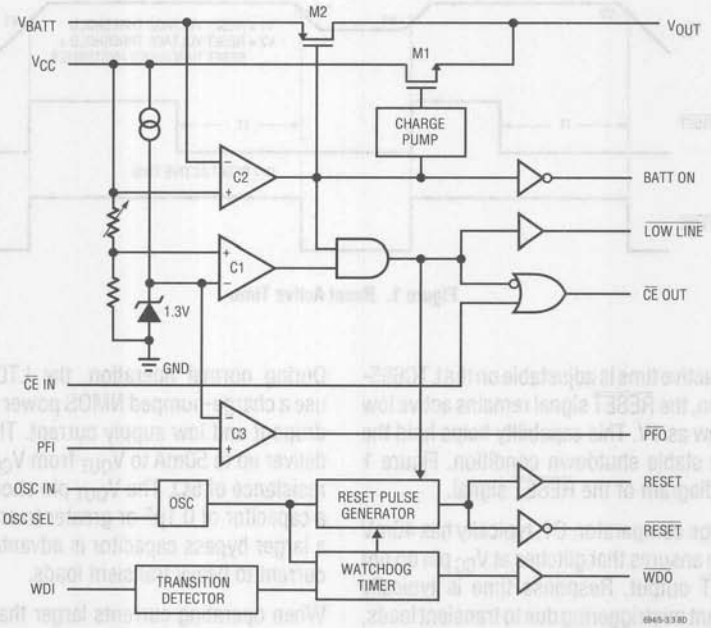
$\overline{CE}$ OUT: Logic Output on the Chip Enable Gating Circuit. When V_{CC} is above the reset voltage threshold, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN. When V_{CC} is below the reset voltage threshold $\overline{CE}$ OUT is forced high (see Figure 5).

OSC SEL: Oscillator Selection Input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low, allows OSC IN to be driven from an external clock signal or an external capacitor can be connected between OSC IN and GND.

PIN FUNCTIONS

OSC IN: Oscillator Input. OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In this configuration the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula (see Applications Information section). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 200ms typical for the LTC695-3.3. OSC IN selects between the 1.6 seconds and 100ms typical watchdog time-out periods. In both cases, the time-out period immediately after a reset is 1.6 seconds typical.

BLOCK DIAGRAM



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APPLICATIONS INFORMATION

Microprocessor Reset

The LTC694-3.3/LTC695-3.3 use a bandgap voltage reference and a precision voltage comparator C1 to monitor the 3.3V supply input on V_{CC} (see Block Diagram). When V_{CC} falls below the reset voltage threshold, the $\overline{RESET}$ output is forced to active low state. The reset voltage threshold accounts for a 10% variation on V_{CC}, so the $\overline{RESET}$ output becomes active low when V_{CC} falls below 3.0V (2.9V typical). On power-up, the $\overline{RESET}$ signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. The reset active time is adjustable on the LTC695-3.3. On power-down, the $\overline{RESET}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{RESET}$ signal.

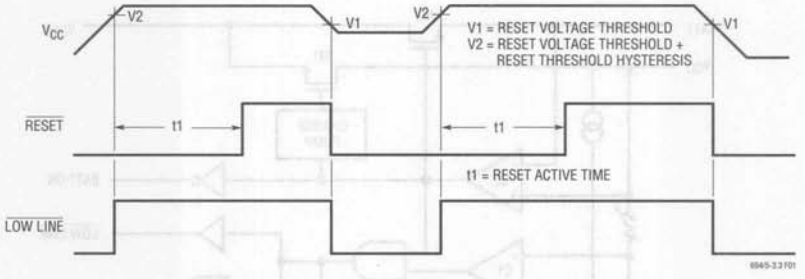


Figure 1. Reset Active Time

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the $\overline{RESET}$ output. Response time is typically 10µs. To help prevent mistriggering due to transient loads, the V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

The LTC695-3.3 has two additional outputs: RESET and $\overline{LOW\ LINE}$. RESET is an active high output and is the inverse of $\overline{RESET}$. $\overline{LOW\ LINE}$ is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, $\overline{LOW\ LINE}$ goes low. $\overline{LOW\ LINE}$ returns high as soon as V_{CC} rises above the reset voltage threshold.

Battery Switchover

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. When V_{CC} rises to 70mV above V_{BATT}, the battery switchover comparator, C2, connects V_{OUT} to V_{CC} through a charge-pumped NMOS power switch, M1. When V_{CC} falls to 50mV above V_{BATT}, C2 connects V_{OUT} to V_{BATT} through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT}. The response time of C2 is approximately 20µs.

During normal operation, the LTC694-3.3/LTC695-3.3 use a charge-pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical on resistance of 5Ω. The V_{OUT} pin should be bypassed with a capacitor of 0.1µF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout ($V_{CC} - V_{OUT}$ voltage differential) is desired, the LTC695-3.3 should be used. This product provides BATT ON output to drive the base of an external PNP transistor (Figure 2). If higher currents are needed with the LTC694-3.3, a high current Schottky diode can be connected from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

APPLICATIONS INFORMATION

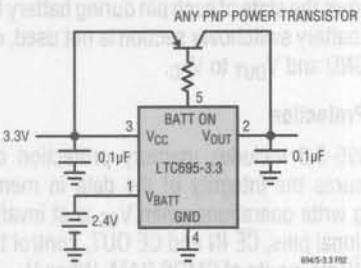


Figure 2. Using BATT ON to Drive External PNP Transistor

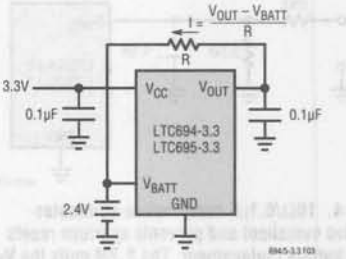


Figure 3. Charging External Battery Through V_{OUT}

The LTC694-3.3/LTC695-3.3 are protected for safe area operation with short-circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for a long period of time, thermal shutdown turns the power switch off until the device cools down. The threshhold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. The LTC694-3.3/LTC695-3.3 use a charge-pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by V_{BATT} pin is strictly junction leakage.

A 125Ω PMOS switch connects the V_{BATT} input to V_{OUT} in battery backup mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. The supply current in battery backup mode is 1µA maximum.

The operating voltage at the V_{BATT} pin ranges from 1.5V to 2.75V. The charging resistor for rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists when the resistor is connected to V_{CC} (Figure 3).

Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur while the battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC694-3.3/LTC695-3.3 switch to battery backup. V_{OUT} pulls V_{BATT} low and the device goes back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature so the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \leq \frac{V_{CC} - 50mV}{1\mu A}$$

With V_{CC} = 3V, a 2.7M resistor will work. With a 2V battery, this resistor will draw only 0.7µA from the battery, which is negligible in most cases.

If battery connections are made through long wires, a 10Ω to 100Ω series resistor and a 0.1µF capacitor are recommended to prevent any overshoot beyond V_{CC} due to the lead inductance (Figure 4).

9

APPLICATIONS INFORMATION

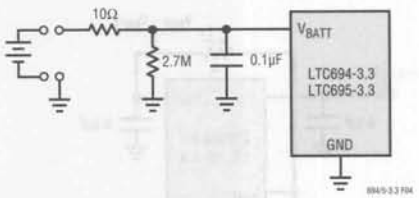


Figure 4. 10Ω/0.1µF combination eliminates inductive overshoot and prevents spurious resets during battery replacement. The 2.7M pulls the V_{BATT} pin to ground while the battery is removed, eliminating spurious resets.

Table 1. Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1µA maximum.
BATT ON	Logic high. The open-circuit output voltage is equal to V_{OUT}.
PFI	Power Failure Input is ignored.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
WDI	Watchdog Input is ignored.
$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{CE}$ IN	$\overline{Chip\ Enable}$ Input is ignored.
$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

Table 1 shows the state of each pin during battery backup. When the battery switchover section is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Memory Protection

The LTC695-3.3 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when V_{CC} is at invalid level. Two additional pins, $\overline{CE}$ IN and $\overline{CE}$ OUT, control the $\overline{Chip\ Enable}$ or $\overline{Write}$ inputs of CMOS RAM. When V_{CC} is 3.3V, $\overline{CE}$ OUT follows $\overline{CE}$ IN with a typical propagation delay of 30ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{CE}$ OUT is forced high, independent of $\overline{CE}$ IN. $\overline{CE}$ OUT is an alternative signal to drive the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery backed up CMOS RAM. $\overline{CE}$ OUT can also be used to drive the $\overline{Store}$ or $\overline{Write}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 5 shows the timing diagram of $\overline{CE}$ IN and $\overline{CE}$ OUT.

$\overline{CE}$ IN can be derived from the microprocessor's address decoder output. Figure 6 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC694-3.3 by using $\overline{RESET}$ as shown in Figure 7.

Power Fail Warning

The LTC694-3.3/LTC695-3.3 generate a Power Failure Output ($\overline{PFO}$) for early warning of failure in the microprocessor's power supply. This is accomplished by

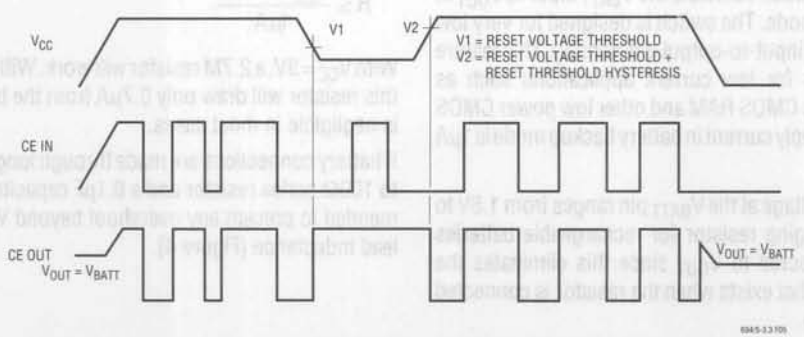


Figure 5. Timing Diagram for $\overline{CE}$ IN and $\overline{CE}$ OUT

APPLICATIONS INFORMATION

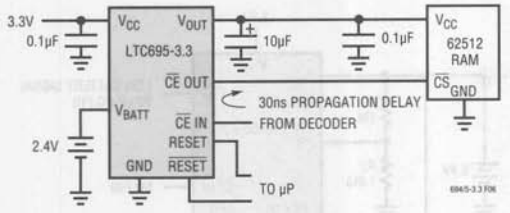


Figure 6. A Typical Nonvolatile CMOS RAM Application

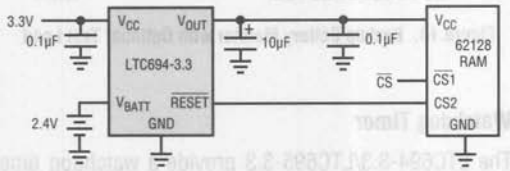


Figure 7. Write Protect for RAM with LTC694-3.3

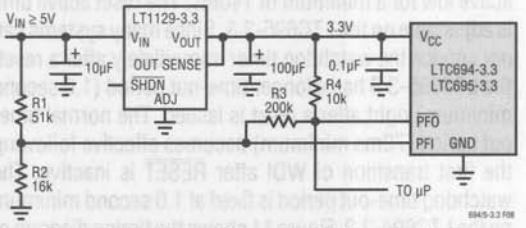


Figure 8. Monitoring *Unregulated* DC Supply with the LTC694-3.3/LTC695-3.3's Power Fail Comparator

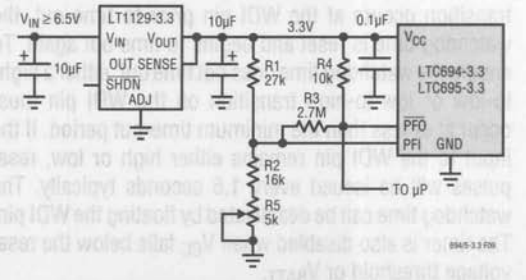


Figure 9. Monitoring *Regulated* DC Supply with the LTC694-3.3/LTC695-3.3's Power Fail Comparator

comparing the power failure input (PFI) with an internal 1.3V reference.

$\overline{PFO}$ goes low when the voltage at the PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 3.3V output. The voltage divider ratio can be chosen such that the voltage at the PFI pin falls below 1.3V several milliseconds before the 3.3V supply falls below the maximum reset voltage threshold 3.0V. $\overline{PFO}$ is normally used to interrupt the microprocessor to execute shutdown procedure between $\overline{PFO}$ and $\overline{RESET}$ or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{PFO}$ output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When $\overline{PFO}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right)$$

When $\overline{PFO}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1+\frac{R1}{R2}-\frac{(3.3V-1.3V)R1}{1.3V(R3+R4)}\right)$$

$$\text{Assuming } R4 << R3, V_{HYSTERESIS} = 3.3V\frac{R1}{R3}$$

Example 1: The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shutdown procedure is 8ms. Also the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 5V which is 1.6V greater than the sum of maximum reset voltage threshold and the dropout voltage of the LT1129-3.3 (3V + 0.4V) and $V_{HYSTERESIS}$ = 850mV.

9

APPLICATIONS INFORMATION

$$V_{HYSTERESIS} = 3.3V\frac{R1}{R3} = 850mV$$

$$R3 \approx 3.88\ R1$$

Choose R3 = 200k and R1 = 51k. Also select R4 = 10k which is much smaller than R3.

$$5V = 1.3V\left(1+\frac{51k}{R2}-\frac{(3.3V-1.3V)51k}{1.3V(210k)}\right)$$

R2 = 15.8k, Choose nearest 5% resistor 16k and recalculate V_L,

$$V_L = 1.3V\left(1+\frac{51k}{16k}-\frac{(3.3V-1.3V)51k}{1.3V(210k)}\right) = 4.96V$$

$$V_H = 1.3V\left(1+\frac{51k}{16k}+\frac{51k}{200k}\right) = 5.77V$$

$$\frac{(4.96V-3.4V)}{100mV/ms} = 15.6ms$$

$V_{HYSTERESIS}$ = 5.77V – 4.96V = 810mV

The 15.6ms allows enough time to execute shutdown procedure for microprocessor and 810mV of hysteresis would prevent $\overline{PFO}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 9 can be used to measure the regulated 3.3V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{PFO}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 3.1V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 10). If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

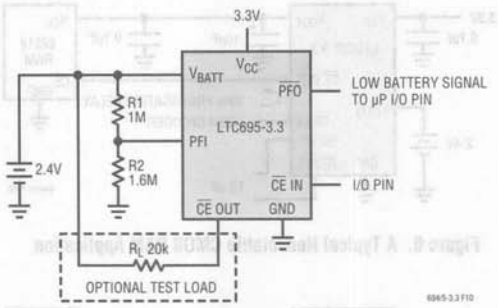


Figure 10. Backup Battery Monitor with Optional Test Load

Watchdog Timer

The LTC694-3.3/LTC695-3.3 provide a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the watchdog input (WDI) within a seleced time-out period, $\overline{RESET}$ is forced to active low for a minimum of 140ms. The reset active time is adjustable on the LTC695-3.3. Since many systems can not service the watchdog timer immediately after a reset, the LTC695-3.3 has a longer time-out period (1.0 second minimum) right after a reset is issued. The normal time-out period (70ms minimum) becomes effective following the first transition of WDI after $\overline{RESET}$ is inactive. The watchdog time-out period is fixed at 1.0 second minimum on the LTC694-3.3. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as $\overline{RESET}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

APPLICATIONS INFORMATION

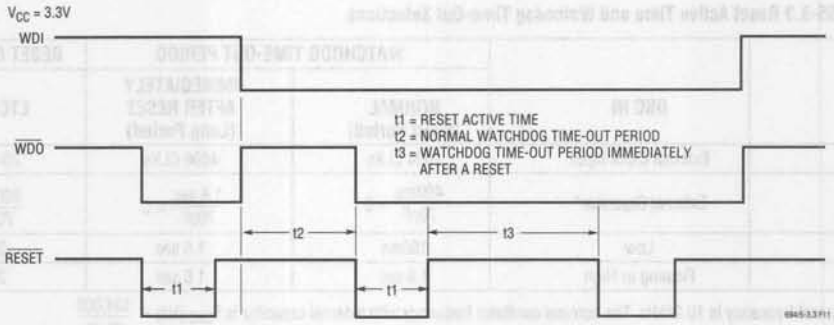


Figure 11. Watchdog Time-Out Period and Reset Active Time

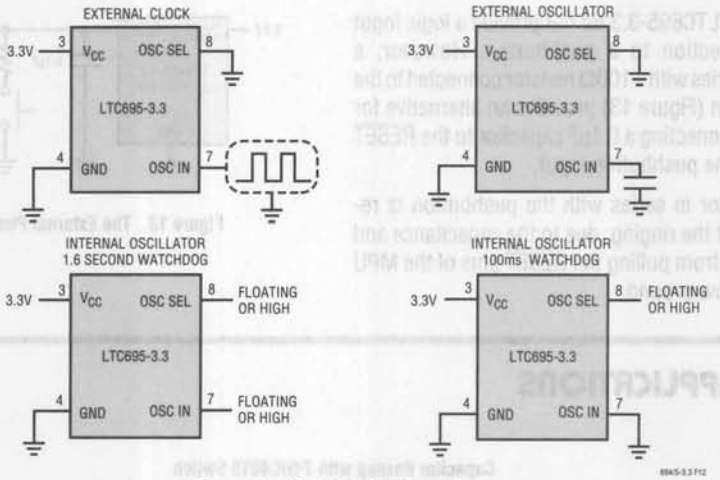


Figure 12. Oscillator Configurations

The LTC695-3.3 provides an additional output (Watchdog Output, $\overline{WDO}$) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{WDO}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The LTC695-3.3 has two additonal pins, OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 12.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 140ms minimum for the LTC695-3.3. OSC IN selects between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

APPLICATIONS INFORMATION

Table 2. LTC695-3.3 Reset Active Time and Watchdog Time-Out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC695-3.3
Low	External Clock Input	1024 CLKs	4096 CLKs	2048 CLKs
Low	External Capacitor*	$\frac{400ms}{70pF} \times C$	$\frac{1.6\ sec}{70pF} \times C$	$\frac{800ms}{70pF} \times C$
Floating or High	Low	100ms	1.6 sec	200ms
Floating or High	Floating or High	1.6 sec	1.6 sec	200ms

*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $F_{OSC}\ (Hz) = \frac{184,000}{C(pF)}$

Pushbutton Reset

The LTC694-3.3/LTC695-3.3 do not provide a logic input for direct connection to a pushbutton. However, a pushbutton in series with a 100Ω resistor connected to the $\overline{RESET}$ output pin (Figure 13) provides an alternative for manual reset. Connecting a 0.1µF capacitor to the $\overline{RESET}$ pin debounces the pushbutton input.

The 100Ω resistor in series with the pushbutton is required to prevent the ringing, due to the capacitance and lead inductance, from pulling the $\overline{RESET}$ pins of the MPU and LTC69X below ground.

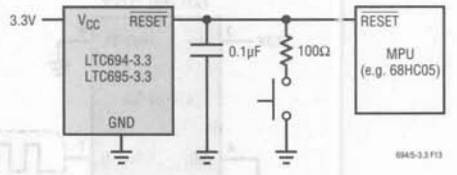
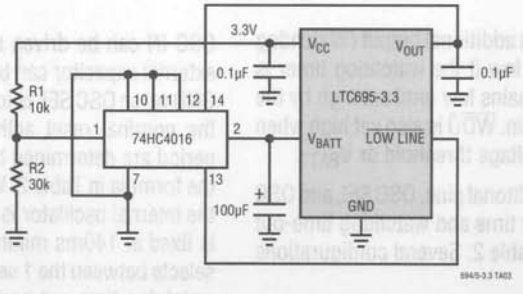


Figure 13. The External Pushbutton Reset

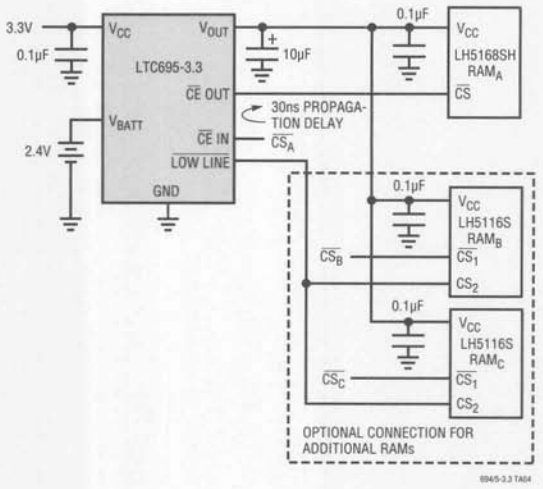
TYPICAL APPLICATIONS

Capacitor Backup with 74HC4016 Switch



TYPICAL APPLICATIONS

Write Protect for Additional RAMs



9

SECTION 10—COMPARATORS

SECTION 10—COMPARATORS

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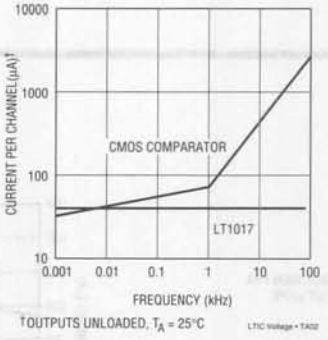
PROPRIETARY PRODUCTS
LT1017/LT1018, Micropower Dual Comparator 10-4

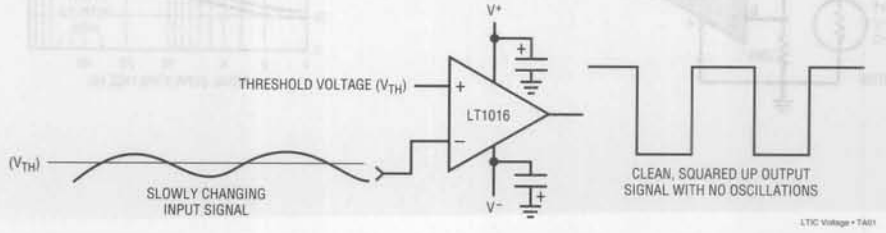
Comparators

Response Time	V_{OS} (MAX) 20mV	3mV	2.5mV	2mV	1.5mV	1mV	0.5mV	TTL OUTPUTS	ECL OUTPUTS	DUAL	GROUND SENSE	MICRO-POWER	ADDITIONAL COMMENTS
100µs							LTC1040			LTC1040	LTC1040	LTC1040	Sampling: Consumes 1.5µW at 1 Sample/Sec.
							LTC1041				LTC1041	LTC1041	Bang-Bang Controller: 1.5µW at 1 Sample/Sec.
						LTC1042					LTC1042	LTC1042	Sampling Window Comp.: 1.5µW at 1 Sample/Sec.
15µs						LT1017				LT1017	LT1017	LT1017	60µA Max. I_{CC}/Operates to 1.1V
4µs						LT1018				LT1018	LT1018	LT1018	250µA Max. I_{CC}/Operates to 1.1V
250ns					LT1011		LT1011A						12-Bit Accurate
14ns	LT1015							LT1015		LT1015			High Speed Two-Channel Line Receiver
		LT1116						LT1116			LT1116		Ground Sense/Single Supply
12ns			LT1016					LT1016					No Min. Input Slew Rate Requirement/Latched Output
6.5ns				LT685					LT685				Latched Outputs

LT1017 Provides Lower Power Operation than CMOS as Input Frequency Increases



LT1016 Doesn't Oscillate with Slowly Changing Input Signals



10

Micropower Dual Comparator

FEATURES

- Maximum Offset Voltage 1mV
- Maximum Bias Current 15nA
- Typical Output Drive 70mA
- Operates from 1.1V to 40V
- Internal Pull-Up Current
- Output Can Drive Loads Above V+
- 30μA Supply Current (LT1017)
  110μA Supply Current (LT1018)

APPLICATIONS

- Power Supply Monitors
- Relay Driving
- Oscillators

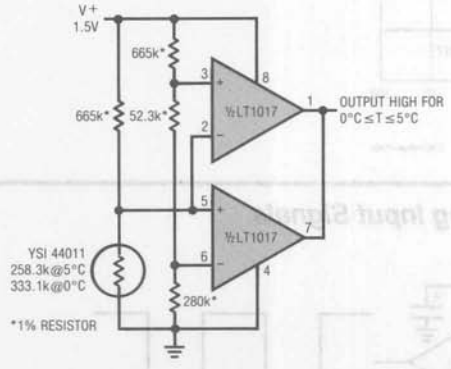
DESCRIPTION

The LT1017 and LT1018 are general purpose micropower comparators. The LT1017 is optimized for lowest operating power while the LT1018 operates at higher power and higher speed. Both devices can operate from a single 1.1V cell up to 40V. The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. The output stage is also designed to allow driving loads connected to a supply more positive than the device, as can comparators with open collector output stages.

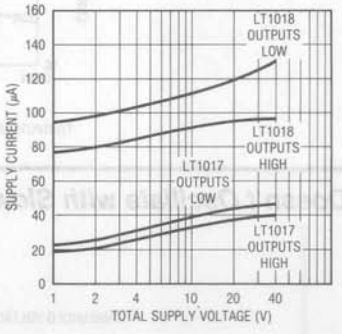
Input specifications are also excellent. On-chip trimming minimizes offset voltage, while high gain and common-mode rejection ratio keep other input-referred errors low. Common-mode voltage range includes ground. Special circuitry prevents false output states even if the input is overdriven.

The LT1017 and LT1018 are pin compatible with older dual comparators such as 393 type devices.

1.5V Powered Refrigerator Alarm



Supply Current



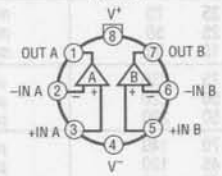
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 40V
Differential Input Voltage 40V
Input Voltage ..... –0.3V to 40V
Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LT1017M, LT1018M ..... –55°C to 125°C
LT1017C, LT1018C ..... 0°C to 70°C
LT1017I, LT1018I ..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

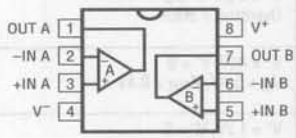


H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

ORDER PART NUMBER
LT1017MH
LT1017CH
LT1018MH
LT1018CH

TOP VIEW

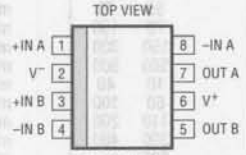


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1017CN8
LT1018CN8

TOP VIEW



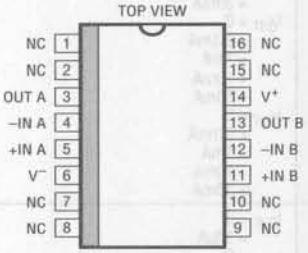
S8 PACKAGE
8-LEAD PLASTIC SO
(0.150" BODY WIDTH)

NOTE: PINOUT ON S8 PACKAGE DOES NOT MATCH 8 PIN DIP PINOUT.

T_{JMAX} = 100°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1017CS8
LT1017IS8
LT1018CS8

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1017CS8
LT1017CS
LT1018CS
LT1017IS
LT1017IS8

PART MARKING
1017CS
1018CS
1017IS

10

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1017 MIN	LT1017 TYP	LT1017 MAX	LT1018 MIN	LT1018 TYP	LT1018 MAX	UNITS
Offset Voltage (Note 1)	±0.75V ≤ V_S ≤ ±20V	25°C		0.4	1		0.4	1	mV
		●		0.5	1.4		0.5	1.4	mV
		125°C			1.5		0.7	1.5	mV
Bias Current	±0.75V ≤ V_S ≤ ±20V	25°C		5	15		15	75	nA
		●		7	25		18	100	nA
		125°C		10	40			110	nA
Offset Current	±0.75V ≤ V_S ≤ ±20V	25°C		0.4	2		1	8	nA
		●		0.5	3		1.6	12	nA
		125°C			12			20	nA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1017 MIN	LT1017 TYP	LT1017 MAX	LT1018 MIN	LT1018 TYP	LT1018 MAX	UNITS
Common-Mode Rejection Ratio	$V_S = \pm 20V$, $-20V \le V_{CM} \le 19.1V$	25°C	105	115		105	115		dB
		●	100	115		100	115		dB
		125°C	86	100		95	110		dB
Power Supply Rejection Ratio	$\pm 0.75V \le V_S \le \pm 20V$	25°C	96	110		96	110		dB
		●	95	105		95	105		dB
		125°C	86			86	100		dB
Gain	No Load, $V_{OUT} = \pm 19.9V$ (Note 2)	25°C	110	115		110	125		dB
		●	105	115		105	120		dB
		125°C	100			100			dB
	$R_L = 4k$, $V_{OUT} = \pm 19V$	25°C	100	110		100	110		dB
		●	94			94			dB
Output Sink Current	$V^+ = 4.5V$, $V^- = 0$ Overdrive > 30mV	25°C	30	65		35	70		mA
		●	25	50		25	50		mA
		125°C	10	20		10	30		mA
Output Source Current	$V^+ = 40V$, $V^- = 0$ $V_{IN} = 5mV$, $V_{OUT} = 0.4V$	25°C	30	75		75	250		µA
		●	25	70		50	220		µA
		125°C	25	75		50	200		µA
Output Source Current	$V^+ = 1.2V$, $V^- = 0$ $V_{IN} = 5mV$, $V_{OUT} = 0.4V$	25°C	25	35		70	140		µA
		●	15	20		45	120		µA
		125°C	25	40		40	110		µA
Negative Output Saturation	$I_{OUT} = 0$ $V^+ = 4.5V$, $V^- = 0$	25°C		5	20		5	15	mV
	$= 0.1mA$ $V_{IN} = -10mV$	25°C		35	60		35	60	mV
	$= 1mA$	25°C		60	120		60	120	mV
	$= 10mA$	25°C		120	200		120	250	mV
	$= 30mA$	25°C		350	600		350	700	mV
	$I_{OUT} = 0$	●		5	20		8	20	mV
	$= 0.1mA$	●		40	75		35	70	mV
	$= 1mA$	●		75	150		70	150	mV
	$= 10mA$	●		150	300		150	300	mV
	$= 30mA$	●		600	900		500	900	mV
	$I_{OUT} = 0$	125°C		25	50		10	40	mV
	$= 0.1mA$	125°C		60	100		60	100	mV
	$= 1mA$	125°C		100	200		110	200	mV
	$= 10mA$	125°C		300	600		300	400	mV
	$= 30mA$	125°C					900		mV
Positive Output Saturation	$I_{OUT} = 0$	25°C		40	80		35	80	mV
	$= 10\mu A$	25°C		175	250		175	250	mV
	$= 0$	●		45	90		45	90	mV
	$= 10\mu A$	●		190	300		190	300	mV
	$= 0$	125°C		50	100		50	100	mV
	$= 10\mu A$	125°C			300			300	mV
Leakage Current	$V_S = 5V$, $V_{OUT} = 40V$ $V_{IN} = 100mV$	25°C		0.5	3		1	8	µA
		●		0.6	3		1.8	10	µA
		125°C			5			15	µA
Supply Current	$V_S = 5V$	25°C		30	60		110	250	µA
		●		40	80		110	250	µA
		125°C			80			300	µA
	$V_S = 40V$	25°C		40	90		130	250	µA
		●		55	100		140	270	µA
		125°C			100			300	µA
Minimum Operating Voltage	$I_{OUT} = 1mA$	25°C			1.15			1.2	V
		●			1.15			1.2	V
		125°C			1.15			1.2	V

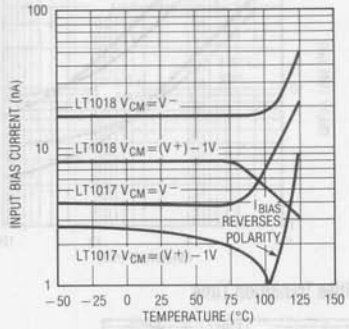
The ● denotes specifications which apply over operating temperature range of –55°C to 85°C for M grade parts and 0°C to 70°C for C grade parts.

Note 1: Offset voltage is guaranteed over a common-mode voltage range of $V^- \le V_{IN} \le (V^+ - 0.9V)$.

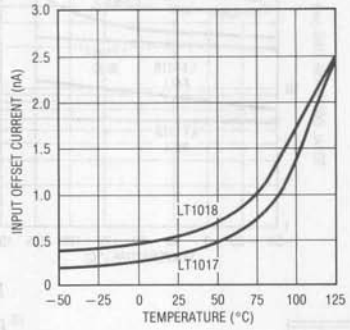
Note 2: No load gain is guaranteed but not tested (LT1017 only).

TYPICAL PERFORMANCE CHARACTERISTICS

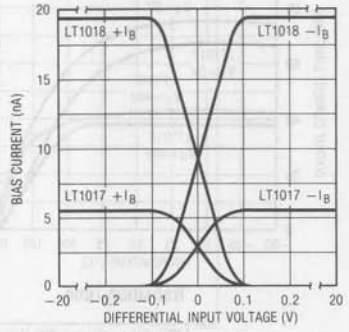
Input Bias Current



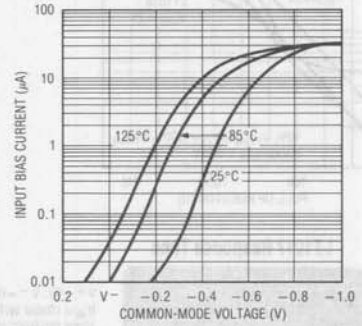
Input Offset Current



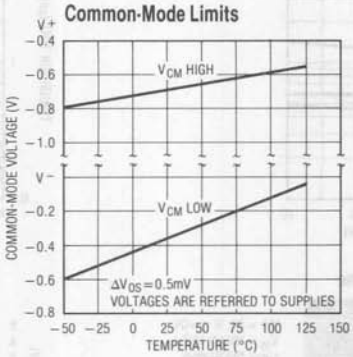
Bias Current vs Differential Input



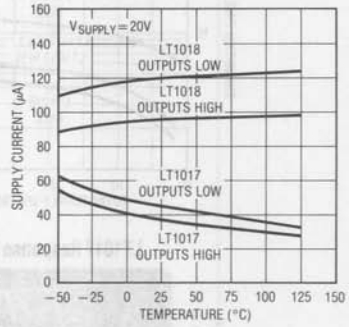
Input Bias Current with Inputs Driven Below the Supply



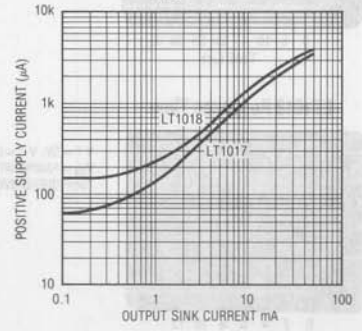
Common-Mode Limits



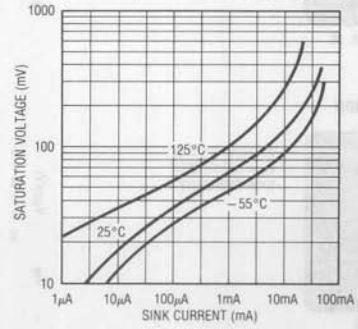
Supply Current



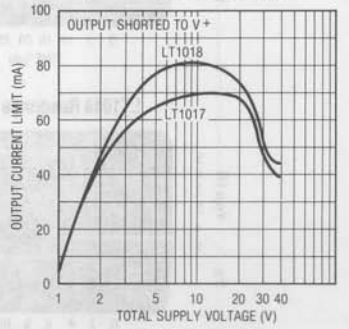
Positive Supply Current



NPN Output Saturation Voltage



Output Sinking Current Limit



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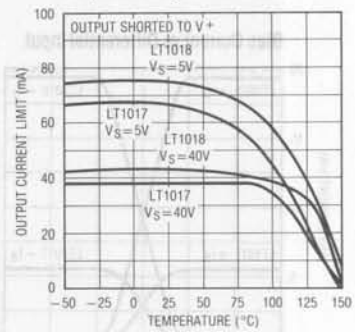
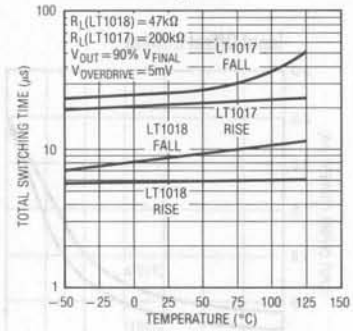
TYPICAL PERFORMANCE CHARACTERISTICS

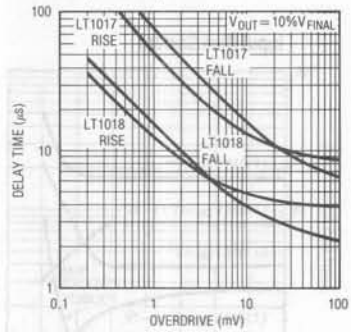
Output Sinking Current Limit



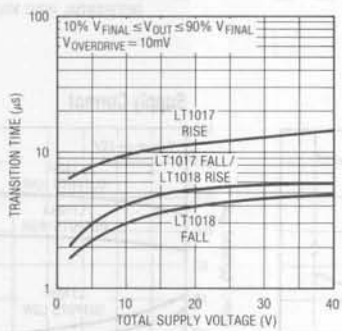
Total Switching Time



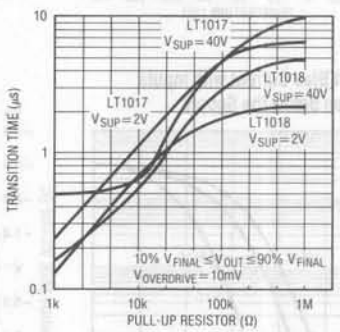
Output Delay



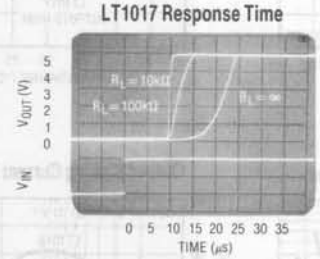
Transition Time



Positive Transition Time

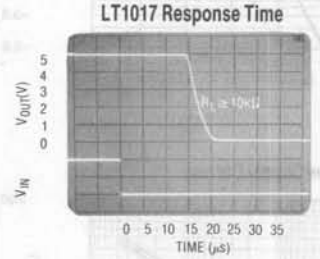


LT1017 Response Time



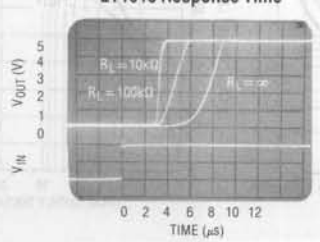
V+ = 5V; V− = 0V
VIN = 100mV WITH
10mV OVERDRIVE

LT1017 Response Time



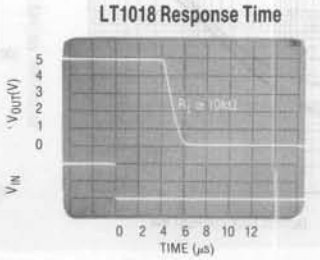
V+ = 5V; V− = 0V
VIN = 100mV WITH
10mV OVERDRIVE

LT1018 Response Time



V+ = 5V; V− = 0V
VIN = 100mV WITH
10mV OVERDRIVE

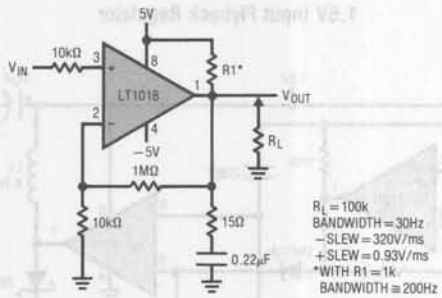
LT1018 Response Time



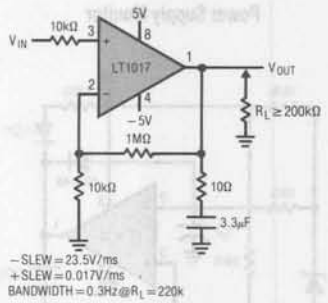
V+ = 5V; V− = 0V
VIN = 100mV WITH
10mV OVERDRIVE

APPLICATIONS

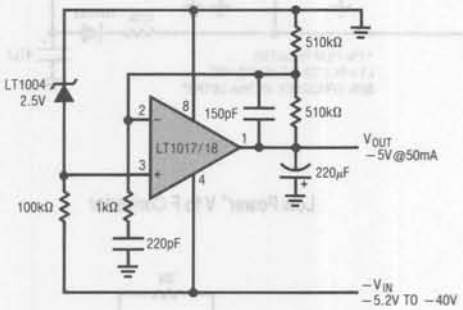
LT1018 Op Amp, $A_V = 100$



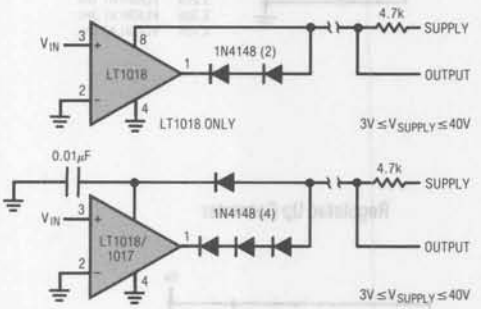
LT1017 Op Amp, $A_V = 100$



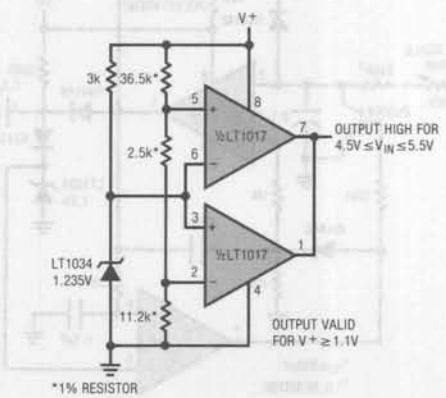
Negative Voltage Regulator



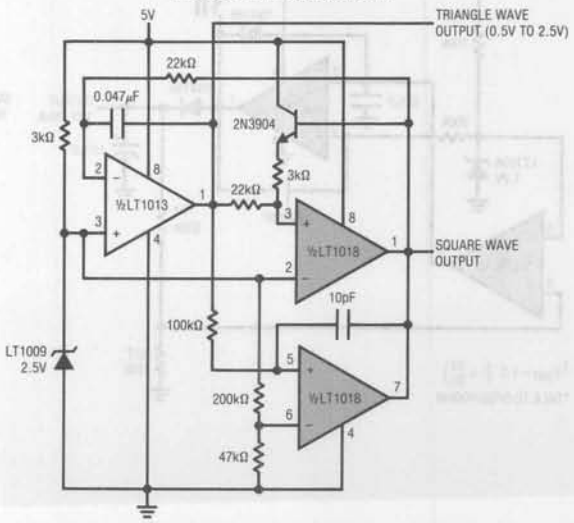
2-Wire Comparator



5V Power Supply Monitor



Precise Tri-Wave Generator



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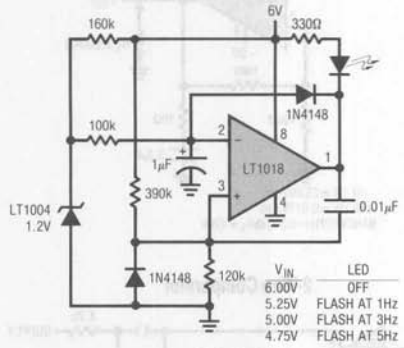
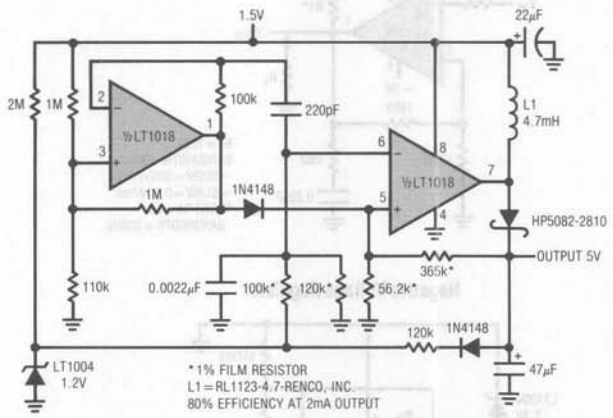
APPLICATIONS

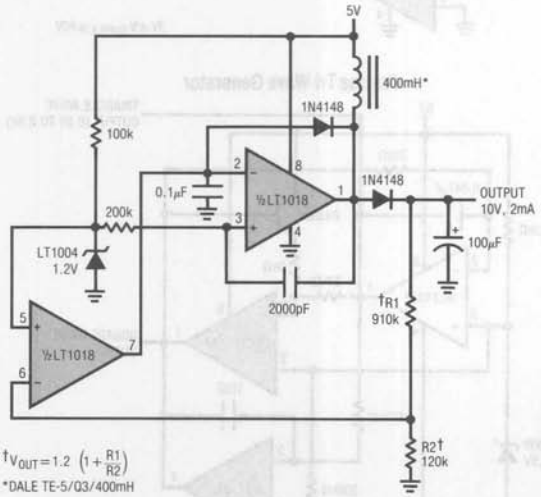
Power Supply Monitor



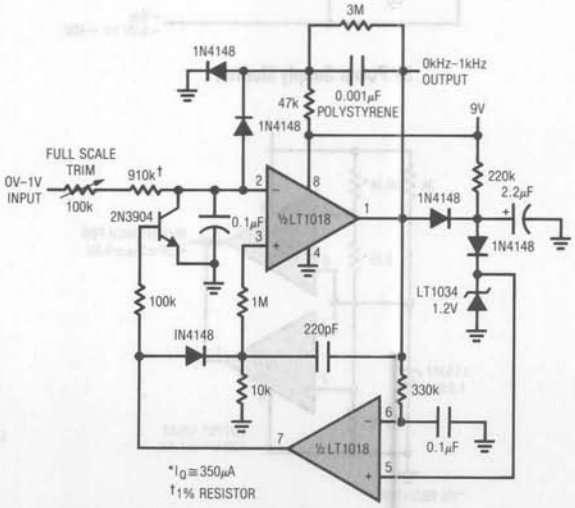
1.5V Input Flyback Regulator



Regulated Up Converter

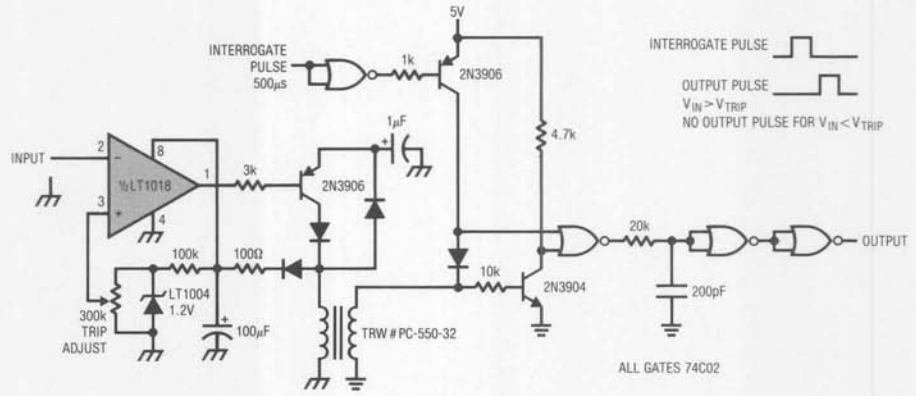


Low Power* V to F Converter

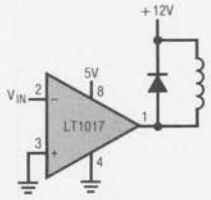


APPLICATIONS

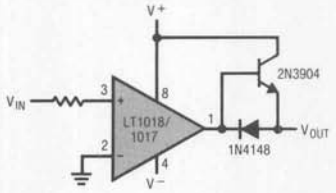
Fully Isolated Limit Comparator



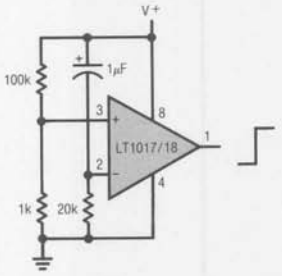
Driving Relays



Increasing Positive Output Current



Delay On Power Up



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LTC221/LTC222, Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches ..... '92DB 11-15

LT1025, Micropower Thermocouple Cold Junction Compensator ..... '90DB 11-7

LTC1043, Dual Precision Instrumentation Switched Capacitor Building Block ..... '90DB 11-15

LTC1043CS, Dual Precision Instrumentation Switched Capacitor Building Block ..... '90DB 11-31

LT1088, Wideband RMS-DC Converter Building Block ..... '90DB 11-33

Analog Switches

Family Features

- Micropower: 40µA Max Supply Current
- Single 5V or ±15V Operation
- 8pC Charge Injection
- Low ON Resistance
- Low Leakage
- Guaranteed Break Before Make

PART NUMBER	NUMBER OF CHANNELS	LATCHED INPUTS	MAX ON RESISTANCE	MAX INPUT AND OUTPUT OFF LEAKAGE	MAX SUPPLY CURRENT	MAX T_{ON}/T_{OFF}	FEATURES
LTC201A	4		125Ω	5nA	40µA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG201A. Single 5V to ±15V Supply Operation
LTC202	4		125Ω	5nA	40µA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG202. Single 5V to ±15V Supply Operation
LTC203	4		125Ω	5nA	40µA	400ns/300ns	Low ON Resistance, Charge Injection, Supply Current
LTC221	4	X	90Ω	5nA	40µA	400ns/300ns	Lower Charge Injection, Supply Current Than DG221
LTC222	4	X	90Ω	5nA	40µA	400ns/300ns	Lower Charge Injection, Supply Current Than DG222

Other Products

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LF198(A)/LF398(A)	Sample-and-Hold Amplifier	H, J8, N8, S	12-Bit Accurate (LF198A), 6µs Acquisition Time, 0.005% Max Gain Error.
LM134/LM334	Adjustable Current Source	H, Z, S8	1µA to 10mA Adjustment Range, Floating Current Source, 0.02%/V Regulation, Can Be Used as Temperature Sensor.
LT1025	Thermocouple Cold Junction Compensator	J8, N8	Provides 0°C Cold Junction Compensation of Types E, J, K, R, S, T Thermocouples. Low Supply Current (80µA) and Operates with Single 4V to 36V DC Supply.
LT1088	RMS to DC Converter	D, N	Thermal RMS to DC Conversion Permits 1% Accuracy to 50MHz, 2% to 100MHz and Handles Crest Factor up to 50:1.
LTC1043	Precision Switched-Capacitor Building Block	D, N, S	120dB CMRR, when Used as Instrumentation Front End, Allows Switched-Capacitor Design Techniques at Board Level.
LTK001	Thermocouple Cold Junction Compensator Matched Amplifier	J, N	LT1025 with Matched Amplifier (LTKA00 or LTKA01) Provides Lower Error Specs than Using Worst Case Errors of LT1025 and Standard Precision Op Amp.

NOTES

SECTION 12—MILITARY PRODUCTS

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NOTE

Military product data sheets are available from your local LTC Sales Representative, or by calling LTC Communications at (800) 637-5545.

LINEAR TECHNOLOGY MILITARY PRODUCTS/ PROGRAMS

Linear Technology Corporation (LTC) offers a comprehensive range of high performance analog/linear integrated circuits including; Data Converters, Interface devices, High Speed Amplifiers, Precision Operational Amplifiers, Comparators, Voltage References, DC-DC Converters, Switches, Voltage Regulators, Switching Regulators, PWMs, and other special function products serving the rigorous demands of the military marketplace.

The Company's specification system, quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification for Microcircuits), MIL-STD-976 (Certification Requirements for Microcircuits), MIL-STD-883 (Test Methods and Procedures for Microelectronics) and more recently the ISO 9000 (Internal Standards for Quality Management).

In addition, the Company has introduced a line of radiation tolerant devices which are offered with two different in-house levels of enhanced reliability processing to serve ground, air and/or space applications, including customer generated Source Controlled Drawings (SCDs) for a variety of missions.

LTC's military programs include:

- JAN Class S
- JAN Class B
- Standard Military Drawings (SMDs)
- 883
- Hi-Rel (SCDs)
- LTC "RH", Radiation hardened devices

LTC JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In August 1984, LTC was visited by a team of Defense Electronics Supply Center (DESC) personnel. This team spent almost four days auditing LTC and at the end of the visit they awarded the Company "Class B Line Certification." *This was a first for any company to receive this distinction on their first audit!*

In early 1985, LTC joined the ranks of the eighteen existing QPL suppliers. Of these eighteen, only a handful of suppliers participate in the linear military JAN market. LTC believes its analog design experience and manufacturing strength has and will continue to make significant contributions to this market.

LTC 's first QPL listing was achieved in February 1985, one year after the Company made JAN Class B a corporate goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to MIL-M-38510 and MIL-STD-883 specifications. Since that time the Company has been re-audited to the latest revisions of these specifications and has maintained an uninterrupted certification record for the manufacture of JAN QPL products.

In November 1987, LTC was audited by a team from DESC, Naval Weapons Support Center and Aerospace Corporation and was awarded "Class S Line Certification."

LTC 's policy of providing JAN linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 85,000 for all types of components (contrasted to approximately 8,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapons systems and equipment now in the field.

LTC maintains its JAN product offerings under the current revision of MIL-I-38535, Appendix A. LTC now offers 45 products listed on the Class B Qualified Parts List (Part 1) and 40 products on the Class S Qualified Parts List (Part 1). To receive an updated copy of LTC's current JAN QPL product offering, contact your local LTC sales office or LTC Military Marketing.

For JAN Flows see Figure 1 and Figure 2.

LTC Standard Military Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

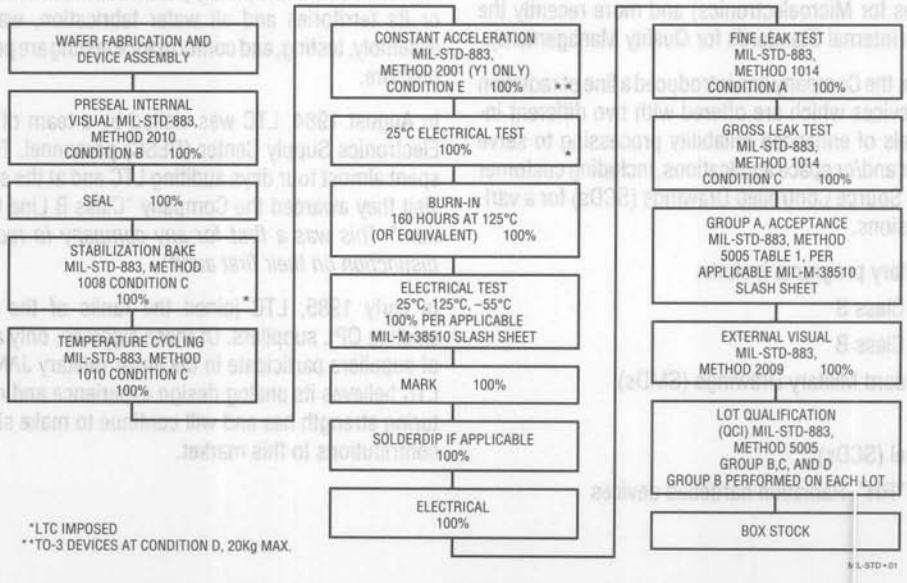

Figure 1. MIL-M-38510 Class B Flow

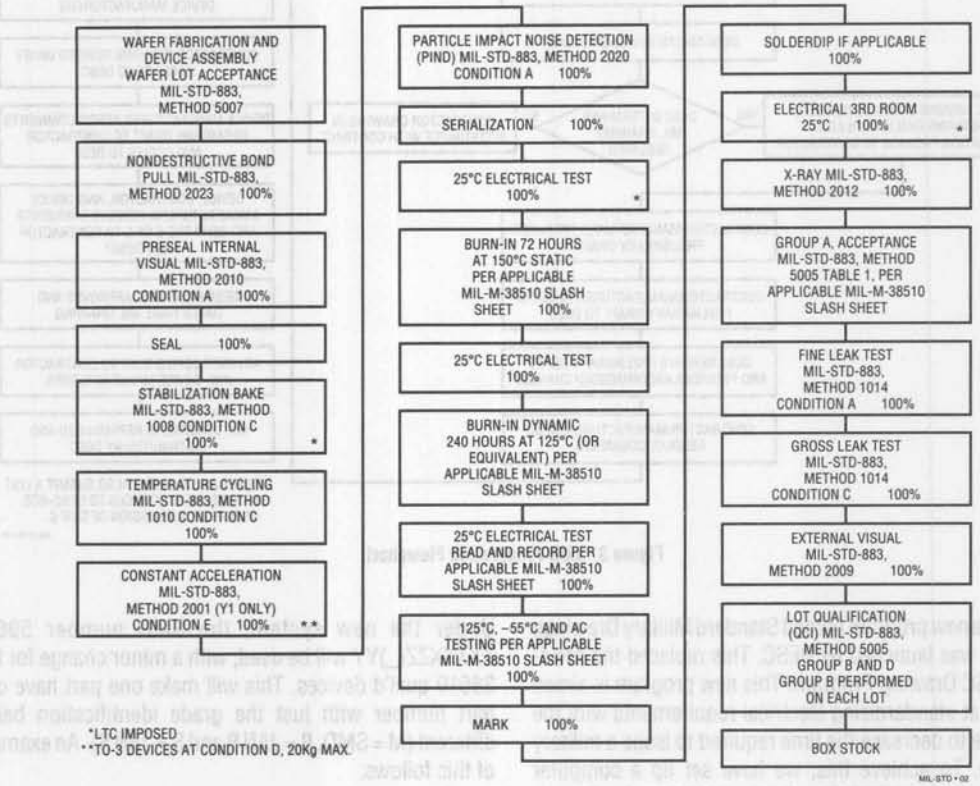

Figure 2. MIL-M-38510 Class S Flow

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 QPL. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.

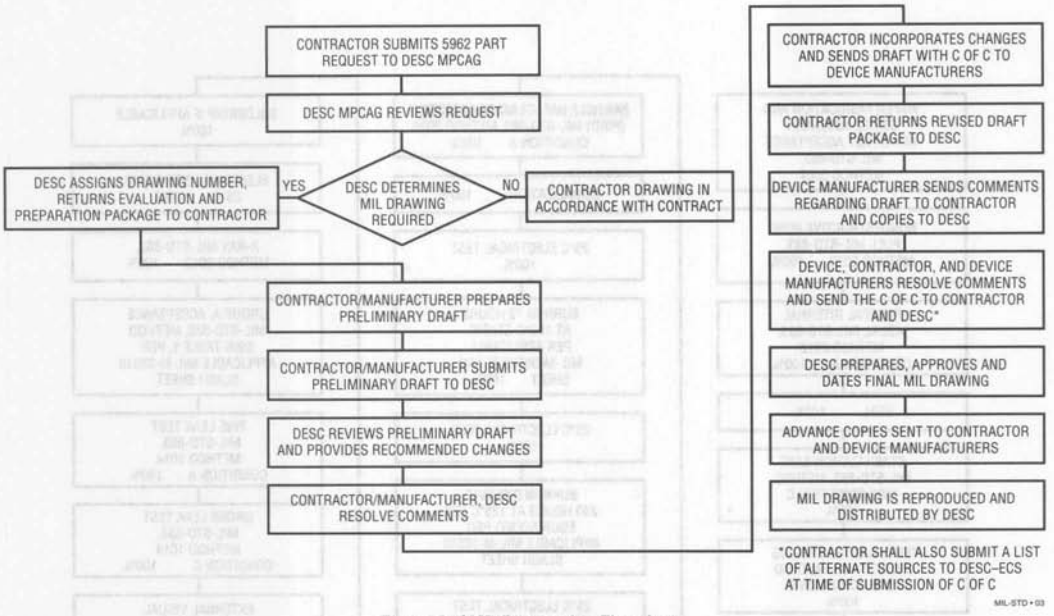

Figure 3. SMD Preparation Flowchart

In 1986 a new program named Standard Military Drawings (SMDs) was launched by DESC. This replaced the previous DESC Drawing Program. This new program is aimed directly at standardizing electrical requirements with the objective to decrease the time required to issue a military drawing. To achieve this, we have set up a computer link-up with the DESC Standardized Mil Drawing Group. LTC is actively supporting this Standard Military Drawing program and we are working closely with DESC and OEMs to participate in this government plan toward a greater level of standardization in military specifications.

LTC has over 134 devices listed on DESC and Mil drawings, and we are actively supporting these standardization programs by having parts available off the shelf from LTC and from distribution outlets.

For SMD Flow see Figure 3.

SMDs Get A New Part Numbering System

A new numbering system has been introduced to standardize the part numbering system for JAN 38510 and SMD (Standard Military Drawing) products.

Under the new system, the SMD number 5962-XXXXXZZ(_)YY will be used, with a minor change for the 38510 qual'd devices. This will make one part have one part number with just the grade identification being different (M = SMD, B = JAN B and S = JAN S). An example of this follows:

Old System

LTC PART NUMBER	"OLD" SMD NO.	JAN PART NUMBER
LT1021CMH-5/883	5962-8876202GA	JM38510/12407BGA

New System

LTC PART NUMBER	"NEW" SMD ONE PART NUMBER SYSTEM
LT1021CMH-5/883	5962-8876202(M, B or S)GA

This was implemented on January 1, 1990, for all SMDs and slash sheets created after this date. Devices listed or approved in the past will retain their respective existing part numbers.

LTC MIL-STD-883 Product

The semicondutcor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883. Requirements for compliant 883 components are now defined very specifically in paragraph 1.2.1 of this document.

MIL-STD-883 is a test procedures and methods document which is revised periodically and defines the conditions for two categories of product, Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative.

On December 31, 1984, a key clause was added to MIL-STD-883, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising."

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510, and, by extension, MIL-I-38535, Appendix A.

LTC can state that all of its 883 products are in full compliance with the latest revision of MIL-STD-883. We have over 333 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

Table 1. LTC 883 Group A Sampling Plan

		883	
TEST	CONDITION	SAMPLE SIZE	ACCEPT
DC Parametric	$T_A = 25°C$	116	0
DC Parametric	$T_A = -55°C$	116	0
	$+125°C$	116	0
AC Parametric	$T_A = 25°C$	116	0

LTC Hi-Rel (SCDs)

LTC recognizes the need for Source Controlled Drawings (SCDs) and the Company's DESC-certified line is well equipped to handle these requirements for space and hi-rel applications. The Company has a comprehensive specification review procedure and emphasis is placed on compliance to test methods and procedures. Over 8,000 specifications have been reviewed to date with fast feedback to our customers.

LTC has serviced SCD orders including "S" level specifications with an emphasis on compliance with customer purchase order requirements and on-time delivery performance. A dedicated SL traveller is initiated to baseline the manufacturing and test flow requirements to service each order.

LTC's Product Marketing Group can provide you with more details on a case-by-case basis.

LTC's Radiation Hardness Program

LTC has developed a proprietary design/wafer fabrication process for RAD HARD (RH prefix) products, complemented by a separate set of RH data sheets. Each RH data sheet specifies the end point electrical test requirements for Total Dose irradiation testing performed on a sample basis in accordance with MIL-STD-883 Method 1019. We offer in certain cases, the option of using the slash sheet electricals for the pre-radiation test limits instead of the LTC RH data sheet electricals. But in all cases the post-radiation electricals are per LTC's RH data sheets.

Due to the unique wafer processing required to make RH products, the RH products are not totally compliant with all the Class S requirements of MIL-STD-883. Since MIL-STD-883 specifically prohibits the marking of non-compliant products with the 883 compliance (c) indicator, LTC's RH products are marked with the LTC RH prefix part number or with a special mark specified by the customer.

Military Market Commitment

LTC is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U.S. defense electronics contractors who have qualified and approved our products. LTC is committed to being the best and most proficient high quality supplier of analog military components.

883 CERTIFICATE OF CONFORMANCE — LEVEL B

QUALITY ASSURANCE INSPECTOR	
DATE	SIGNATURE

LTC Part Number _____

Lot Traceability No. _____

Purchase Order No. _____

Customer Name _____ P/N _____ Qty _____

Date Code _____ Shipper # _____ Traveller Lot # _____

Group A = _____ Group B = _____ Group C = _____ Group D = _____

Group B/3 Re-Inspection Date, If Applicable _____

LINEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE PURCHASE ORDER COMPLY WITH YOUR SPECIFICATIONS AND REQUIREMENTS OF MIL-STD-883. ALL SUPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR INSPECTION. THE MAJOR ELEMENTS OF THE 883C PROGRAM ARE SHOWN BELOW.

Operation	Screening Procedure MIL-STD-883, Method 5004	
Internal Visual	Method 2010, Condition B	
Stabilization Bake	Method 1008, Condition C	
Temperature Cycling	Method 1010, Condition C, 10 cycles –65°C to 150°C	
Constant Acceleration	Method 2001, Condition E, 30k g Y1 axis (TO-3 PKG at 20k g)	
Fine Leak	Method 1014, Condition A	
Gross Leak	Method 1014, Condition C	
Burn-in	Method 1015, 160 hrs at 125°C (or equivalent)	
Final Electrical	+25°C DC (per LTC Data Sheet) PDA = 5%	
	+125°C or 150°C DC	
	–55°C DC	
	+25°C AC	
QA Acceptance	Method 5005	Group A (sample/lot)
Quality Conformance		Group B (sample/lot)
		Group C (sample every 6 months/Generic Group)
		Group D (sample every 6 months/Package Family)
External Visual	Method 2009	

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

EXAMPLE

FORM No. 00-03-6072

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP A DATA
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

	ACC #	S/S	# FAILED	DATE TESTED	OPER NUMBER
SUBGROUP 1 Static tests at 25°C	0	116			
SUBGROUP 2 Static tests at maximum rated operating temperature	0	116			
SUBGROUP 3 Static tests at minimum rated operating temperature	0	116			
SUBGROUP 4 Dynamic tests at 25°C	0	116			
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	0	116			
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	0	116			
SUBGROUP 7 Functional tests at 25°C	0	116			
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	0	116			
SUBGROUP 9 Switching tests at 25°C	0	116			
SUBGROUP 10 Switching tests at maximum rated operating temperature	0	116			
SUBGROUP 11 Switching tests at minimum rated operating temperature	0	116			

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6037

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 2 Resistance to Solvents	2015			0	3			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245°C ± 5°C	10	0				
SUBGROUP 5 Bond Strength	2011	C or D	15	0				

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6006

EXAMPLE

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP C DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
CT. GROUP: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test Electrical Endpoints	1005	T_A = 125°C (1000 Hours or Equiv.) Test #	5	0	45			

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6007

EXAMPLE

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class S)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1				0	3			
Physical Dimensions	2016							
Internal Water-Vapor Content	1018	5000 ppm Max						
SUBGROUP 2								
Resistance to Solvents	2015			0	3			
Internal Visual and Mechanical	2013, 2014	Design and Construction Requirements		0	2			
Bond Strength	2011	C or D	10	0	22 Wires			
Die Shear Test	2019			0	3			
SUBGROUP 3								
Solderability	2003 or 2022	Soldering Temp. of 245°C ±5°C	10	0	22 Leads			
SUBGROUP 4								
Lead Integrity	2004	B_2 (Lead Fatigue)	5	0	45 Leads			
Seal	1014							
Fine								
Gross								
Lid Torque	2024	Glass Frit Seal Only						
SUBGROUP 5								
Electrical End-Points		Test #	5	0	45			
Steady State Life	1005	C, D, or E						
Electrical End-Points		Test #						
SUBGROUP 6								
Electrical End-Points		Test #	15	0	15			
Temperature Cycling	1010	C 100 Cycles						
Constant Acceleration	2001	E Y_1 Only						
Seal	1014	(TO-3 at Condition D, 20Kg)						
Fine								
Gross								
Electrical End-Points		Test #						
SUBGROUP 7								
ESD Classification	3015	Qual or Re-Design Only	15	N/A	—			

EXAMPLE

QA APPROVAL: _____ DATE: _____

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LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP D DATA (Class B or S)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1			15	0	15			
Physical Dimensions	2016							
SUBGROUP 2			5	0	45 Leads			
Lead Integrity	2004	B_2 (Lead Fatigue)						
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3			15	0	15			
Thermal Shock	1011	B 15 Cycles						
Temperature Cycle	1010	C 100 Cycles						
Moisture Resistance	1004							
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1004/ 1010							
Electrical End-Points		Test #						
SUBGROUP 4			15	0	15			
Mechanical Shock	2002	B						
Vibration, Variable Frequency	2007	A						
Constant Acceleration	2001	E Y1 Only						
Fine Leak	1014							
Gross Leak	1014	(TO-3 at						
Visual Examination	1010/ 1011	Condition D, 20Kg)						
Electrical End-Points		Test #						
SUBGROUP 5			15	0	15			
Salt Atmosphere	1009	A						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1009	Visual Criteria						
SUBGROUP 6				0	3			
Internal Water-Vapor	1018	5000 ppm Max						
SUBGROUP 7			15	0	15			
Adhesion of Lead Finish	2025							
SUBGROUP 8				0	5			
Lid Torque	2024	Glass Frit Seal Only						

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN S QPL

JM38510/10103SGA (LM101AH)
JM38510/10103SHA (LM101AW)
JM38510/10103SPA (LM101AJ8)
JM38510/10104SCA (LM108AJ)
JM38510/10104SGA (LM108AH)
JM38510/10104SHA (LM108AW)
JM38510/10104SPA (LM108AJ8)
JM38510/10107SGA (LM118H)
JM38510/10304SGA (LM111H)
JM38510/10306SCA (LM119J)
JM38510/10306SIA (LM119H)
JM38510/10306SHA (LM119W)
JM38510/10307SCA (LT119AJ)
JM38510/10307SIA (LT119AH)
JM38510/10307SHA (LT119AW)
JM38510/11401SPA (LF155J8)
JM38510/11402SGA (LF156H)
JM38510/11402SPA (LF156J8)
JM38510/11404SGA (LF155AH)
JM38510/11404SPA (LF155AJ8)
JM38510/11405SGA (LF156AH)
JM38510/11405SPA (LF156AJ8)
JM38510/11703SXA (LM117H)
JM38510/11704SYA (LM117K)
JM38510/11803SXA (LM137H)
JM38510/11804SYA (LM137K)
JM38510/12407SGA (LT1021-5H)
JM38510/12408SGA (LT1021-7H)
JM38510/12409SGA (LT1021-10H)
JM38510/12501SGA (LF198H)
JM38510/13501SGA (OP07AH)
JM38510/13501SPA (OP07AJ8)
JM38510/13502SGA (OP07H)
JM38510/13502SPA (OP07J8)
JM38510/13503SGA (OP27AH)
JM38510/13503SPA (OP27AJ8)
JM38510/14802SXA (LT1009H)

JAN B QPL

JM38510/10103BCA (LM101AJ)
JM38510/10103BGA (LM101AH)
JM38510/10103BHA (LM101AW)
JM38510/10103BPA (LM101AJ8)
JM38510/10104BCA (LM108AJ)
JM38510/10104BGA (LM108AH)
JM38510/10104BPA (LM108AJ8)
JM38510/10106BEA (LH2108AD)
JM38510/10107BCA (LM118J)
JM38510/10107BGA (LM118H)
JM38510/10107BHA (LM118W)
JM38510/10107BPA (LM118J8)
JM38510/10304BGA (LM111H)
JM38510/10306BIA (LM119H)
JM38510/10306BCA (LM119J)
JM38510/10306BHA (LM119W)
JM38510/10307BCA (LT119AJ)
JM38510/10307BIA (LT119AH)
JM38510/10307BHA (LT119AW)
JM38510/11401BGA (LF155H)
JM38510/11401BPA (LF156J8)
JM38510/11402BGA (LF156H)
JM38510/11402BHA (LF156W)
JM38510/11402BPA (LF156J8)
JM38510/11404BGA (LF155AH)
JM38510/11404BPA (LF155AJ8)
JM38510/11405BGA (LF156AH)
JM38510/11405BHA (LF156W)
JM38510/11405BPA (LF156AJ8)
JM38510/11703BXA (LM117H)
JM38510/11704BYA (LM117K)
JM38510/11706BYA (LM138K)
JM38510/11803BXA (LM137H)
JM38510/11804BYA (LM137K)
JM38510/12407BGA (LT1021-5H)
JM38510/12408BGA (LT1021-7H)
JM38510/12409BGA (LT1021-10H)
JM38510/12501BGA (LF198H)
JM38510/13501BGA (OP07AH)
JM38510/13501BPA (OP07AJ8)
JM38510/13502BGA (OP07H)
JM38510/13502BPA (OP07J8)
JM38510/13503BGA (OP27AH)
JM38510/13503BPA (OP27AJ8)
JM38510/14802BXA (LT1009H)

DESC Drawings

7703401XA (LM117H)
7703401YA (LM117K)
7703402XA (LM117HVH)
7703402YA (LM117HVK)
7703403XA (LM137H)
7703403YA (LM137K)
7703404XA (LM137HVH)
7703404YA (LM137HVK)
7703405XA (LT117AH)
7703405YA (LT117AK)
7703406XA (LT137AH)
7703406YA (LT137AK)
7703407XA (LT117AHVH)
7703407YA (LT117AHVK)
7703408XA (LT137AHVH)
7703408YA (LT137AHVK)
7802801EA (SG1524J)
8203601GA (OP07AH)
8203601PA (OP07AJ8)
8203602GA (OP07H)
8203602PA (OP07J8)
8418001XA (LM136AH-2.5)
8551401GA (REF02AH)
8551401PA (REF02AJ8)
8551501VA (LT1526J)
8600801EA (LT685)
8601401CA (LM119J)
8601401HA (LM119W)
8601401IA (LM119H)
8601402CA (LT119AJ)
8601402HA (LT119AW)
8601402IA (LT119AH)
8687702XA (LT111AH)
8687702PA (LT111AJ8)

Standard Military Drawings (SMD)

5962-3870701MGA (LTC1044MH)
5962-3870702MPA (LTC1044MJ)
5962-8680601EA (LT1846J)
5962-8680602EA (LT1847J)
5962-8684501IA (LT1016MH)
5962-8684501PA (LT1016MJ8)
5962-8686101XA (LT580SH)
5962-8686102XA (LT580TH)
5962-8686103XA (LT580UH)
5962-8687701GA (LT111AH)
5962-8687701PA (LT111AJ8)
5962-8688201XA (LH0070-0H)
5962-8688202XA (LH0070-1H)
5962-8688203XA (LH0070-2H)
5962-8688701CA (OP227AJ)
5962-8757801GA (LT1007AMH)
5962-8757801PA (LT1007AMJ8)
5962-8759401XA (LT185H-1.2)
5962-8759402XA (LM185H-2.5)
5962-8760401GA (LM10H)
5962-8760401PA (LM10J8)
5962-8766601XA (LT1080MJ)
5962-8766602EA (LT1081MJ)
5962-8767501XA (LM150K)
5962-8767502XA (LT150AK)
5962-8771501CA (LT1002AMJ)
5962-8773801GA (LT1001MH)
5962-8773801PA (LT1001MJ8)
5962-87738036A (LT1001AMH)
5962-87738036PA (LT1001AMJ)
5962-8774101XA (LT1033MK)
5962-8777501YA (LM123K)
5962-8777502YA (LM123AK)
5962-8853701GA (OP37AH)
5962-8853701PA (OP37AJ8)
5962-8853702GA (OP37BH)
5962-8853702PA (OP37BJ8)
5962-8853703GA (OP37CH)
5962-8853703PA (OP37CJ8)
5962-8856101XA (LM199AH)
5962-8856102XA (LM199H)
5962-8856201XA (LT1010MH)
5962-8856201YA (LT1010MK)
5962-8856701GA (LT1037AMH)
5962-8856701PA (LT1037AMJ8)
5962-8859701XA (LT1004MH-1.2)
5962-8859702XA (LT1004MH-2.5)
5962-8860001GA (LT1021BMH-10)
5962-8860002GA (LT1021CMH-10)
5962-8860003GA (LT1021DMH-10)
5962-8862201GA (LT1028MH)
5962-8862201PA (LT1028MJ8)
5962-8862202GA (LT1028AMH)
5962-8862202PA (LT1028AMJ8)
5962-8864101RA (LTC1060AMJ)
5962-8864102RA (LTC1060MJ)
5962-8864601XA (LT1085MK)
5962-8864701GA (LT1021BMH-7)
5962-8864702GA (LT1021DMH-7)
5962-8875101VA (LT1039MJ)
5962-8875102EA (LT1039MJ16)
5962-8876001GA (LT1013AMH)
5962-8876001PA (LT1013AMJ8)
5962-8876002GA (LT1013MH)
5962-8876002PA (LT1013MJ8)
5962-8876201GA (LT1021BMH-5)
5962-8876202GA (LT1021CMH-5)
5962-8876203GA (LT1021DMH-5)
5962-8944001CA (LT1032MJ)
5962-8948301LA (LTC1064MJ)
5962-8950401GA (LT1017MH)
5962-8950401PA (LT1017MJ8)
5962-8950402GA (LT1018MH)
5962-8950402PA (LT1018MJ8)
5962-8951101EA (LT1525AJ)
5962-8951102EA (LT1527AJ)
5962-8952101XA (LT1084MK)
5962-8956201GA (LT1054MH)
5962-8956201PA (LT1054MJ8)
5962-8958101GA (REF01AH)
5962-8958101PA (REF01AJ8)
5962-8961001XA (LT1009MH)
5962-8962201GA (LT1022AMH)
5962-8962202GA (LT1022MH)
5962-8967701CA (LT1014AMJ)
5962-8967702CA (LT1014MJ)
5962-8978201CA (LTC1052MJ)
5962-8978201GA (LTC1052MH)
5962-8978201PA (LTC1052MJ8)
5962-8980201XA (LT1031BMH)
5962-8980202XA (LT1031CMH)
5962-8980203XA (LT1031DMH)
5962-8983002RA (LTC1290BMJ)
5962-8983003RA (LTC1290CMJ)
5962-8983004RA (LTC1290DMJ)
5962-8987301YA (LT1003MK)
5962-8989701CA (LT1058AMJ)
5962-8989701XA (LT1058AML)
5962-8989702CA (LT1058MJ)
5962-8992101XA (LM129AH)
5962-8992102XA (LM129BH)
5962-8992103XA (LM129CH)
5962-8997601GA (LT1055AMH)
5962-8997602GA (LT1056AMH)
5962-8997603GA (LT1055MH)
5962-8997604GA (LT1056MH)
5962-8998101XA (LT1086MK)
5962-8998101YA (LT1086MH)
5962-9050701XA (LM134H-3)
5962-9050702XA (LM134H-6)
5962-9050703XA (LM134H)
5962-9051901XA (LT1029AMH)
5962-9051902XA (LT1029MH)
5962-9054501RA (LTC1045MJ)
5962-9056801CA (OP237AJ)
5962-9056802CA (OP237CJ)
5962-9059501GA (LT1019AMH-10)
5962-9059502GA (LT1019AMH-5)
5962-9059503GA (LT1019AMH-4.5)
5962-9059504GA (LT1019AMH-2.5)
5962-9059505GA (LT1019MH-10)
5962-9059506GA (LT1019MH-5)
5962-9059507GA (LT1019MH-4.5)
5962-9059508GA (LT1019MH-2.5)
5962-9062701GA (LT1011AMH)
5962-9062701PA (LT1011AMJ8)
5962-9062702GA (LT1011MH)
5962-9062702PA (LT1011MJ8)
5962-9064901CA (LTC1064-4MJ)
5962-9064901XA (LTC1064-4ML)
5962-9069301MCA (LTC1064-1MJ/883)
5962-9069302MCA (LTC1064-1AMJ/883)
5962-9073902MXA (LT1084-5MK)
5962-9073903MXA (LT1085-5MK)
5962-9073904MXA (LT1086-5MK)
5962-9081701MGA (LT1057AMH)
5962-9081701MPA (LT1057AMJ8)
5962-9081702MGA (LT1057MH)
5962-9081702MPA (LT1057MJ8)
5962-9082501MYA (LT1070MK)
5962-9082502MYA (LT1071MK)
5962-9082503MYA (LT1072MK)
5962-9082503MPA (LT1072MJ8)
5962-9082504MYA (LT1070HVMK)
5962-9082505MYA (LT1071HVMK)
5962-9082506MYA (LT1072HVMK)
5962-9084101MCA (LT1020MJ)
5962-9084201MGA (LT1012MH)
5962-9084201MPA (LT1012MJ8)
5962-9084202MGA (LT1012AMH)
5962-9084202MPA (LT1012AMJ8)
5962-9159501MPA (LTC1062MJ8)
5962-9161901MPA (LTC1042MK)
5962-9163201MCA (LT1079MJ)
5962-9163202MCA (LT1079AMJ)
5962-9163203MCA (LT1078MJ)
5962-9163204MCA (LT1078AMJ)
5962-9163204MGA (LT1078AMH)
5962-9163204MPA (LT1078AMJ8)
5962-9172901MVA (LT1180MJ)
5962-9172902MEA (LT1181MJ)
5962-9172903MVA (LT1280MJ)
5962-9172904MEA (LT1281MJ)
5962-9207901MPA (LT1172MJ8)
5962-9207902MPA (LT1172MJ8)
5962-9208001MPA (LTC485MJ8)
5962-9305701MPA (LTC1291CMJ)
5962-9305702MPA (LTC1292CMJ)
5962-9305703MEA (LTC1293CMJ)
5962-9305704MRA (LTC1294CMJ)
5962-9311901MYA (LT1076MK)
5962-9311902MYA (LT1076HVMK)
5962-9318401MPA (LT1229MJ8)
5962-9318402MCA (LT1232OMJ)
5962-9319001MPA (LT1241MJ8)
5962-9319002MPA (LT1242MJ8)
5962-9319003MPA (LT1243MJ8)
5962-9319004MPA (LT1244MJ8)
5962-9319005MPA (LT1245MJ8)
5962-9321201MPA (LT1111MJ8)
5962-9322401MPA (LT1120MJ8)
5962-9323801MCA (LT1125MJ)
5962-9323802MPA (LT1124MJ)
5962-9323803MCA (LT1125AMJ)
5962-9323804MPA (LT1124AMJ)
5962-9451601MPA (LT118AJ8)

Radiation Hardened

RH07
RH27C
RH37C
RH101A
RH108A
RH111
RH117
RH118
RH119
RH129
RH137
RH1009
RH1011
RH1013
RH1014
RH1021-5
RH1021-7
RH1021-10
RH1056

12

MILITARY PARTS LIST

883 Operational Amplifiers	LF155AH/883	LM101AJ8/883	LT1007AMH/883	LT1078AMH/883	LTC1050AMJ/883	OP-07AJ8/883	OP-37AJ8/883
	LF155H/883	LM107H/883	LT1007AMJ8/883	LT1078AMJ8/883	LTC1050MH/883	OP-07H/883	OP-37BJ8/883
	LF156AH/883	LM107J8/883	LT1007MH/883	LT1078MH/883	LTC1050MJ8/883	OP-07J8/883	OP-37CH/883
	LF156H/883	LM108AH/883	LT1007MJ8/883	LT1078MJ8/883	LTC1050MJ/883	OP-15AH/883	OP-37CJ8/883
	LF156J8/883	LM108H/883	LT1008MH/883	LT1079AMJ/883	LTC1051AMH/883	OP-15BH/883	OP-227AJ/883
	LF156W/883	LM108AJ8/883	LT1012AMH/883	LT1079MJ/883	LTC1051AMJ8/883	OP-15CH/883	OP-227CJ/883
	LF412AMH/883	LT118AH/883	LT1012MD/883	LT1124AMJ8/883	LTC1051MJ8/883	OP-15CJ8/883	OP-237AJ/883
	LF412MH/883	LT118AJ8/883	LT1012MH/883	LT1124MJ8/883	LTC1052MH/883	OP-16AH/883	OP-237CJ/883
	LF412AMJ8/883	LT1001AMH/883	LT1013AMH/883	LT1125AMJ8/883	LTC1052MJ/883	OP-16BH/883	
	LF412MJ8/883	LT1001AMJ8/883	LT1013AMJ8/883	LT1125MJ8/883	LTC1052MJ8/883	OP-16CH/883	
	LH0070-0H/883	LT1001MH/883	LT1013MH/883	LT1126AMJ8/883	LTC1150MJ8/883	OP-16CJ8/883	
	LH0070-1H/883	LT1001MJ8/883	LT1013MJ8/883	LT1126MJ8/883	OP-05AH/883	OP-27AH/883	
	LH0070-2H/883	LT1002AMJ/883	LT1014AMJ/883	LT1127AMJ8/883	OP-05AJ8/883	OP-27AJ8/883	
	LH2108AD/883	LT1002MJ/883	LT1014MJ/883	LT1127MJ/883	OP-05H/883	OP-27BJ8/883	
	LH2108D/883	LT1006AMH/883	LT1024AMD/883	LT1172MJ8/883	OP-05J8/883	OP-27BH/883	
	LM10H/883	LT1006AMJ8/883	LT1024MD/883	LT1228MJ8/883	OP-05AW/883	OP-27CH/883	
	LM10J8/883	LT1006MH/883	LT1055AMH/883	LTC1050AMH/883	OP-05W/883	OP-27CJ8/883	
	LM101AH/883	LT1006MJ8/883	LT1055MH/883	LTC1050AMJ8/883	OP-07AH/883	OP-37AH/883	
883 High Speed Op Amps	LM118H/883	LT1028AMH/883	LT1037AMJ8/883	LT1057AMH/883	LT1058AML/883	LT1191MJ8/833	LT1223MJ8/883
	LM118J8/883	LT1028AMJ8/883	LT1037MH/883	LT1057AMJ8/883	LT1058MJ/883	LT1192MJ8/883	LT1229MJ8/883
	LM118W/883	LT1028MH/883	LT1037MJ8/883	LT1057MH/883	LT1187MJ8/883	LT1193MJ8/883	LT1230MJ/883
	LT1022AMH/883	LT1028MJ8/883	LT1056AMH/883	LT1057MJ8/883	LT1189MJ8/883	LT1194MJ8/883	
	LT1022MH/883	LT1037AMH/883	LT1056MH/883	LT1058AMJ/883	LT1190MJ8/883	LT1195MJ8/883	
883 Regulators	LM117H/883	LM137HVK/883	LT117AK/883	LT150AK/883	LT1035MK/883	LT1076HVMK/883	LT1086MH/883
	LM117HVH/883	LM137K/883	LT123AK/883	LT1003MK/883	LT1036MK/883	LT1083MK-5/883	LT1086MK/883
	LM117HVK/883	LM138K/883	LT137AH/883	LT1005MK/883	LT1054MJ8/883	LT1083MK-12/883	LT1086MK-5/883
	LM117K/883	LM150K/883	LT137AHVH/883	LT1020MJ/883	LT1054MH/883	LT1084MK/883	LT1086MK-12/883
	LM123K/883	LT117AH/883	LT137AHVK/883	LT1026MJ8/883	LT1074MK/883	LT1084MK-5/883	LT1120MJ8/883
	LM137H/883	LT117AHVH/883	LT137AK/883	LT1026MH8/883	LT1074HVMK/883	LT1084MK-12/883	
	LM137HVH/883	LT117AHVK/883	LT138AK/883	LT1033MK/883	LT1076MK/883	LT1085MK/883	
883 References	LM129AH/883	LM199AH/883	LT1004MH-2.5/883	LT1021BMH-5/883	LT1031BMH/883	REF-01J8/883	
	LM129BH/883	LM199AH-20/883	LT1009MH/883	LT1021CMH-5/883	LT1031CMH/883	REF-02AH/883	
	LM129CH/883	LM199H/883	LT1019AMH-2.5/883	LT1021DMH-5/883	LT1031DMH/883	REF-02AJ8/883	
	LM134H/883	LT580SH/883	LT1019AMH-4.5/883	LT1021BMH-7/883	LT1034BMH-1.2/883	REF-02H/883	
	LM134H-3/883	LT580TH/883	LT1019AMH-5/883	LT1021DMH-7/883	LT1034BMH-2.5/883	REF-02J8/883	
	LM134H-6/883	LT580UH/883	LT1019AMH-10/883	LT1021BMH-10/883	LT1034MH-1.2/883		
	LM136AH-2.5/883	LT581SH/883	LT1019MH-2.5/883	LT1021CMH-10/883	LT1034MH-2.5/883		
	LM136H-2.5/883	LT581TH/883	LT1019MH-4.5/883	LT1021DMH-10/883	REF-01AH/883		
	LM185H-1.2/883	LT581UH/883	LT1019MH-5/883	LT1029AMH/883	REF-01AJ8/883		
	LM185H-2.5/883	LT1004MH-1.2/883	LT1019MH-10/883	LT1029MH/883	REF-01H/883		
883 Comparators	LM111H/883	LM119W/883	LT119AJ/883	LT1011AMJ8/883	LT1016MJ/883	LT1017MJ8/883	
	LM111J8/883	LT111AH/883	LT685MH/883	LT1011MH/883	LT1016MJ8/883	LT1018MH/883	
	LM119H/883	LT111AJ8/883	LT685MJ/883	LT1011MJ8/883	LT1016ML/883	LT1018MJ8/883	
	LM119J/883	LT119AH/883	LT1011AMH/883	LT1016MH/883	LT1017MH/883	LTC1042MJ8/883	
883 Switched-Mode Control Circuits	LT1070MK/883	LT1072MK/883	LT1242MJ8/883	LT1524J/883	LT1846J/883	SG1527AJ/883	
	LT1070HVMK/883	LT1072HVMK/883	LT1243MJ8/883	LT1525AJ/883	LT1847J/883		
	LT1071MK/883	LT1072MJ8/883	LT1244MJ8/883	LT1526J/883	SG1524J/883		
	LT1071HVMK/883	LT1241MJ8/883	LT1245MJ8/883	LT1527AJ/883	SG1525AJ/883		
883 Interface	LT1032MJ/883	LT1080MJ/883	LT1180AMJ/883	LT1280MJ/883	LTC1045MJ/883		
	LT1039MJ/883	LT1081MJ/883	LT1181AMJ/883	LT1281MJ/883			
	LT1039MJ16/883	LT1180MJ/883	LT1181MJ/883	LTC485MJ8/883			
883 Filters	LTC1059AMJ/883	LTC1061AMJ/883	LTC1064MJ/883	LTC1064-2ML/883	LTC1164AMJ/883		
	LTC1059MJ/883	LTC1061MJ/883	LTC1064-1AMJ/883	LTC1064-4MJ/883	LTC1164-5MJ/883		
	LTC1060AMJ/883	LTC1062MJ8/883	LTC1064-1MJ/883	LTC1064-4ML/883	LTC1164-7MJ/883		
	LTC1060MJ/883	LTC1063MJ8/883	LTC1064-2MJ/883	LTC1164MJ/883			
883 Data Converters	LTC1094MJ/883	LTC1290DMJ/883	LTC1293DMJ/883	LTC1294DMJ/883			
	LTC1290BMJ/883	LTC1293BMJ/883	LTC1294BMJ/883				
	LTC1290CMJ/883	LTC1293CMJ/883	LTC1294CMJ/883				
Other 883	LF198AH/883	LT1010MK/883	LTC1043MD/883				
	LF198H/883	LTC201AMJ/883	LTC1044MH/883				
	LT1010MH/883	LTC1041MJ8/883	LTC1044MJ8/883				

SECTION 13—NEW PRODUCTS

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SECTION 13—NEW PRODUCTS

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PRELIMINARY

LT1106

Micropower Step-Up DC/DC Converter for PCMCIA Card Flash Memory

November 1993

FEATURES

- 60mA Output Current at 12V from 3V Supply
- Shutdown to 10µA
- Programmable 12V or 5V Output
- Up to 85% Efficiency
- 750µA Quiescent Current
- Low V_{CESAT} Switch: 300mV at 0.5A Typical
- Uses Low Value, Thin, Surface Mount Inductors
- Ultra-Thin 20-Lead TSSOP Package

APPLICATIONS

- PCMCIA Card Flash Memory VPP Generator
- Portable Computers
- Portable Instruments
- DC/DC Converter Module Replacements

DESCRIPTION

The LT1106 is the industry's first DC/DC converter designed for use on Type I and Type II PCMCIA cards. The device senses the VPP1 and VPP2 lines at the PCMCIA socket and generates a regulated 12V, 60mA programming supply if the socket does not provide it. Internal logic simplifies the interface to PCMCIA card microcontrollers. One input selects a 12V or 5V regulated output, while another input controls micropower shutdown. Two logic outputs indicate when the selected programming voltage is valid and whether the input supply is 3.3V or 5V.

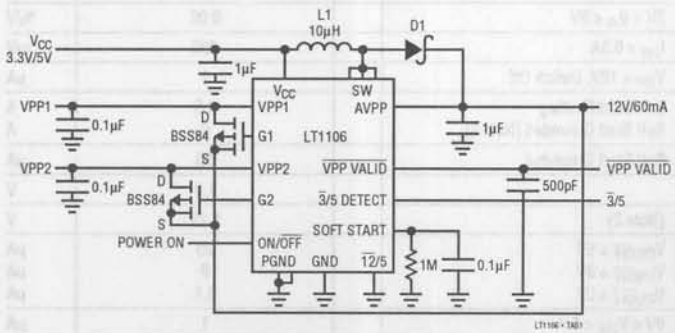
The regulator features Burst Mode™ operation with a 0.5A, 300mV switch for efficiency up to 85%. High frequency 500kHz switching permits the use of small value, flat inductors that fit neatly on PCMCIA cards. The device requires just 1µF of input and output capacitance.

Quiescent current is 750µA which drops to 350µA when the card runs off the socket supply. The shutdown pin reduces supply current to only 10µA. The device includes a soft start feature which limits supply current transients when the card is inserted into a hot socket.

Burst Mode™ is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

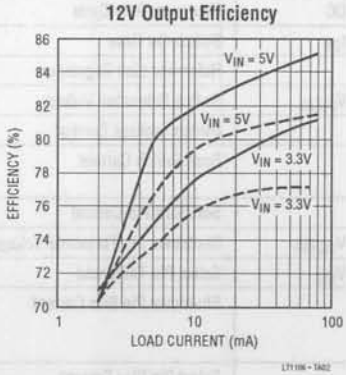
12V, 60mA Flash Memory Programming Supply



FOR TYPE I CARDS: — —
L1 = COILTRONICS CTX02-11238
D1 = 4 BAT54Cs IN PARALLEL (PHILIPS), 1.1mm MAXIMUM HEIGHT

FOR TYPE II CARDS: ——
L1 = MURATA ERIE LQH3C100K04M00
D1 = PHILIPS PRLL5818, 2.1mm MAXIMUM HEIGHT

12V Output Efficiency



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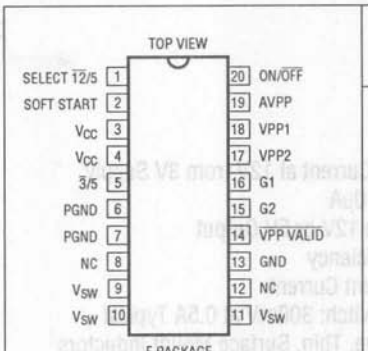
ABSOLUTE MAXIMUM RATINGS

V_{CC} Voltage 7V
V_{SW} Voltage 20V
AVPP Voltage 20V
VPP1, VPP2 Voltage 20V
G1, G2 Voltage 20V
$V_{ON/\overline{OFF}}$ Voltage 7V
V_{SEL} Voltage 7V
I_{LIM} Voltage 7V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



F PACKAGE
20-LEAD PLASTIC TSSOP

ORDER PART NUMBER
LT1106CF

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	$V_{ON/\overline{OFF}}$ = 3V, V_{SEL} = 0.2V, AVPP = 12V		750		µA
I_{SD}	Shutdown Mode Current	$V_{ON/\overline{OFF}}$ = 0.2V		9		µA
I_D	Doze Mode Current	$V_{ON/\overline{OFF}}$ = 3V, V_{SEL} = 0.2V, VPP1 = 12V or VPP2 = 12V		350		µA
V_{CC}	Input Voltage Range		2		6	V
AVPP	Output Sense Voltage	V_{SEL} = 3V, VPP1 and VPP2 Floating V_{SEL} = 0.2V, VPP1 and VPP2 Floating	4.8 11.5	5.0 12.0	5.2 12.5	V V
	Output Referred Comparator Hysteresis	V_{SEL} = 3V, AVPP = 5V V_{SEL} = 0.2V, AVPP = 12V		15 36		mV mV
	Oscillator Frequency	Current Limit Not Asserted		500		kHz
DC	Maximum Duty Cycle			90		%
t_{ON}	Switch-On Time	Current Limit Not Asserted		1.8		µs
	Reference Line Regulation	2V < V_{IN} < 6V		0.06		%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 0.5A		300		mV
	Switch Leakage Current	V_{SW} = 12V, Switch Off		1		µA
	Peak Switch Current	Soft Start Floating Soft Start Grounded (Note 1)		0.5 0		A A
	Soft Start Pin Current	Soft Start Grounded		50		µA
$V_{ON/\overline{OFF}}$	Shutdown Pin Threshold Voltage			1.5		V
V_{SEL}	Select Pin Threshold	(Note 2)		1.25		V
	Shutdown Pin Bias Current	$V_{ON/\overline{OFF}}$ = 5V $V_{ON/\overline{OFF}}$ = 3V $V_{ON/\overline{OFF}}$ = 0V		20 9 0.1		µA µA µA
	Select Pin Bias Current	0V < V_{SEL} < 5V		1		µA
VPP1, VPP2	Input Sense Voltage Threshold	$V_{ON/\overline{OFF}}$ = V_{CC}		11.7		V

ELECTRICAL CHARACTERISTICS

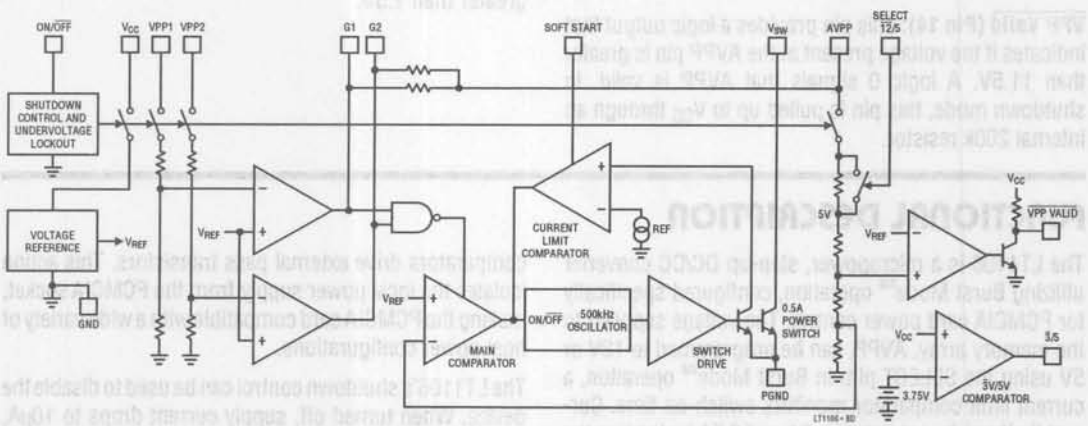
T_A = 25°C, V_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Input Current at AVPP	$V_{ON/\overline{OFF}} = V_{CC}$		50		µA
		$V_{ON/\overline{OFF}} = 0.2V$		1		µA
	Input Current at VPP1 and VPP2	$V_{ON/\overline{OFF}} = V_{CC}$		60		µA
		$V_{ON/\overline{OFF}} = 0.2V$		1		µA
$\overline{VPP\ Valid}$	Input Threshold			11.5		V
	Output High	I_{LOAD} = 2.5µA, 200k Internal Pull-Up		V_{CC} – 0.5		V
	Output Low	I_{LOAD} = 100µA		0.13		V
V_{SC}	Input Supply Comparator Threshold			3.75		V
	Input Supply Comparator $\overline{3/5}$ Output Level High	I_{LOAD} = 50µA, V_{CC} = 5V		V_{CC} – 1.2		V
	Input Supply Comparator $\overline{3/5}$ Output Level Low	I_{LOAD} = 50µA, V_{CC} = 3V		0.8		V
	Off State Current at Gate Drive Outputs G1 and G2	VPP1 = 10V, V_{G1} = 12V, or VPP2 = 10V, V_{G2} = 12V or $V_{ON/\overline{OFF}}$ = 0V		1.5		µA

Note 1: When the soft start pin is grounded, the current limit comparator forces the on-chip oscillator to run at minimum duty cycle.

Note 2: Do not pull the select pin below ground.

BLOCK DIAGRAM



PIN FUNCTIONS

SELECT (Pin 1): Tie to V_{IN} or a logic 1 for 5V output; tie to GND or logic 0 for 12V output. The logic threshold for this pin is 1.25V. Do not pull the SELECT pin below ground.

Soft Start (Pin 2): Sets Peak Switch Current. Float this pin for normal 0.5A peak. Tie this pin to GND through a resistor greater than 1k to limit the switch current from 0.125A to 0.5A. Connecting a capacitor from soft start to GND reduces switch current during startup. The initial current limit with the soft start pin at 0V is about 0A which increases as the external capacitor charges from 0V to 0.2V. Select the capacitance for a given soft start duration. About 50µA flows from the soft start pin to ground.

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PIN FUNCTIONS

V_{CC} (Pins 3, 4): Input Supply. Both pins should be tied together and decoupled close to the package with a 1µF tantalum capacitor connected to GND (Pin 13).

$\overline{3}/5$ (Pin 5): Supply Comparator Output. This pin provides a logic signal indicating the value of the input supply at the V_{CC} pin. If V_{CC} is greater than 3.75V the $\overline{3}/5$ pin is driven high. Likewise, if V_{CC} is less than 3.75V the $\overline{3}/5$ pin is driven low.

PGND (Pins 6, 7): Power Ground. Connect these pins together directly at the package. Large current flows in these pins so it is highly recommended to make their PC board traces to the common ground plane as wide as possible.

V_{SW} (Pins 9, 10, 11): Connected to the collector of the internal power switch. High currents flow with fast edges on these pins. To reduce radiated noise minimize the PCB trace area connected to these pins.

GND (Pin 13): Clean Analog Ground. V_{CC} should be decoupled to this point. Connect to PGND under package.

$\overline{\text{VPP Valid}}$ (Pin 14): This pin provides a logic output that indicates if the voltage present at the AVPP pin is greater than 11.5V. A logic 0 signals that AVPP is valid. In shutdown mode, this pin is pulled up to V_{CC} through an internal 200k resistor.

G1, G2 (Pins 16, 15): External MOSFET Gate Drives. When VPP1 or VPP2 is greater than 11.7V, G1 or G2 is driven to about 0.8V. When VPP1 or VPP2 is less than 11.7V, the drives assume a high impedance state pulled up to the AVPP pin through an internal 100k resistor.

VPP1, VPP2 (Pins 18, 17): Programming Power Inputs. The LT1106 senses both VPP1 and VPP2 supplies at the PCMCIA card socket. If VPP1 or VPP2 is greater than 11.7V, the LT1106 operates in Doze Mode—the switching regulator turns off and drive to external P-channel MOSFETs turns on. Supply current in Doze Mode is about 350µA. Input current into VPP1 and VPP2 is about 1µA when the device is shut down.

AVPP (Pin 19): Output Sense Pin. This pin connects to a 1M resistive divider that sets the output voltage.

ON/$\overline{\text{OFF}}$ (Pin 20): Shutdown Control. When pulled below 1.5V, this pin disables the LT1106 and reduces supply current to 10µA. The part is enabled when ON/$\overline{\text{OFF}}$ is greater than 1.5V.

FUNCTIONAL DESCRIPTION

The LT1106 is a micropower, step-up DC/DC converter utilizing Burst Mode™ operation, configured specifically for PCMCIA card power control. The voltage supplied to the memory array, AVPP, can be programmed to 12V or 5V using the SELECT pin. In Burst Mode™ operation, a current limit comparator monitors switch-on time. Current limit can be set between 0A and 0.5A by loading the soft start pin with a resistor. Connecting a small capacitor to this pin momentarily forces current limit to zero at device turn on, which reduces supply current transients on startup.

If either the VPP1 or VPP2 inputs have the specified 12V ±5% programming voltage, the DC/DC converter enters Doze Mode, a low power state (350µA), in which the VPP comparators drive external pass transistors. This action isolates the local power supply from the PCMCIA socket, making the PCMCIA card compatible with a wide variety of host power configurations.

The LT1106's shutdown control can be used to disable the device. When turned off, supply current drops to 10µA, and sense inputs at VPP1, VPP2 and AVPP assume high impedance states with µA levels of leakage.

An input supply comparator monitors V_{CC}, signaling whether the supply voltage is 3.3V or 5V. This comparator remains functional while the device is disabled. The $\overline{\text{VPP VALID}}$ comparator indicates when a valid programming voltage is available at the memory array.

Rail-to-Rail Input Rail-to-Rail Output Zero-Drift Op Amp

March 1994

FEATURES

- Input Common-Mode Range Includes Both Rails
- Output Swings Rail to Rail
- Output Will Drive 1kΩ Load
- No External Components Required
- Supply Current: 2.2mA Max
- Shutdown Pin Drops Supply Current to 5μA Max
- Input Offset Voltage: 10μV Max
- Input Offset Drift: 100nV/°C Max
- Minimum CMRR: 115dB
- Output Configurable to Drive Any Capacitive Load
- Operates from 2.7V to 14V Total Supply Voltage

APPLICATIONS

- High Resolution Data Acquisition Systems
- Rail-to-Rail Buffer Amplifiers
- Low Supply Voltage Transducer Amplifiers
- High Accuracy Instrumentation
- Supply Current Sensing in Either Rail
- Single Negative Supply Operation

DESCRIPTION

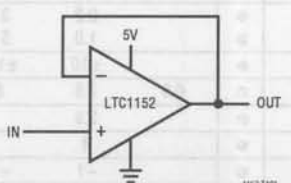
The LTC1152 is a high performance, low power zero-drift op amp featuring an input stage common-mode range which include both power supply rails and an output stage that provides rail-to-rail swing, even into heavy loads. The wide input common-mode range is achieved with a high frequency on-board charge pump. This technique eliminates the crossover distortion and limited CMRR imposed by competing technologies.

The LTC1152 shares the excellent DC performance specs of LTC's other zero-drift amplifiers. Typical offset voltage is 1μV, typical offset drift is 10nV/°C, CMRR and PSRR are 130dB and 120dB typically, and open-loop gain is 130dB, 0.1Hz to 10Hz noise is $2\mu V_{P-P}$, gain-bandwidth product is 1MHz, and slew rate is 1V/μs, all with supply current of 2.2mA max over temperature. The LTC1152 also includes a shutdown feature which drops supply current to 1μA typ and puts the output stage in a high impedance state.

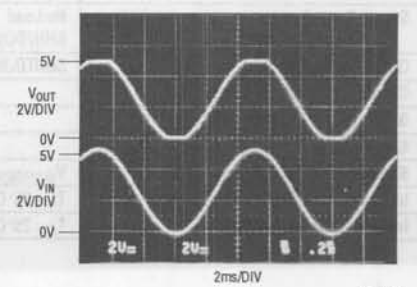
The LTC1152 is available in plastic 8-pin DIP and 8-pin SO packages and uses the standard op amp pinout, allowing it to be a plug-in replacement for many standard op amps.

TYPICAL APPLICATION

Rail-to-Rail Buffer



Input and Output Waveforms



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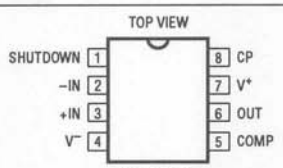
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V+ to V–) 14V
Input Voltage ..... $V^+ + 0.3V$ to $V^- - 0.3V$
Amplifier Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LTC1152C ..... 0°C to 70°C
LTC1152I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 110°C, θ_{JC} = 130°C/W (N8)
T_{JMAX} = 110°C, θ_{JC} = 200°C/W (S8)

ORDER PART NUMBER
LTC1152CN8 LTC1152CS8 LTC1152IN8 LTC1152IS8
S8 PART MARKING
1152 1152I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 5V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±1	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±10	±100	nV/°C
	Long Term Offset Drift				±50		nV/√Mo
I_B	Input Bias Current	T_A = 25°C (Note 2)			±10	±100	pA
			●			±1000	pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 2)			±20	±200	pA
						±500	pA
e_n	Input Noise Voltage (Note 3)	R_S =100Ω, 0.1Hz to 10Hz			2		μV_{P-P}
		R_S = 100Ω, 0.1Hz to 1Hz			0.5		μV_{P-P}
i_n	Input Noise Current	f = 10Hz			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V, T_A = 25°C	●	115	130		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V		110	120		dB
			●	105			dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.5V to 4.5V	●	110	130		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	R_L = 1k	●	4	4.50		V
		R_L = 1k, V_S = ±2.5V	●	±2	2.20		V
		R_L = 100k, V_S = ±2.5V			±2.49		V
SR	Slew Rate	R_L = 10k, C_L = 50pF, V_S = ±2.5V			1		V/µs
GBW	Gain-Bandwidth Product	R_L = 10k, C_L = 50pF, V_S = ±2.5V			1		MHz
I_S	Supply Current	No Load	●		2.2	3.0	mA
		SHUTDOWN = 0V	●		1.0	5.0	µA
I_{OSD}	Output Leakage Current	SHUTDOWN = 0V	●		±10	±100	nA
V_{CP}	Charge Pump Output Voltage		●	6.5	7.5	8	V
V_{IL}	Shutdown Pin Input Low Voltage		●		2.5		V
V_{IH}	Shutdown Pin Input High Voltage		●		4		V
I_{IN}	Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 0V	●		–1	–5	µA
f_{CP}	Internal Charge Pump Frequency	T_A = 25°C			4.7		MHz
f_{SMPL}	Internal Sampling Frequency	T_A = 25°C			2.3		kHz

ELECTRICAL CHARACTERISTICS

V_S = 3V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±1	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±10	±100	nV/°C
I_B	Input Bias Current	T_A = 25°C (Note 2)			±5	±100	pA
			●			±1000	pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 2)			±10	±200	pA
						±500	pA
e_n	Input Noise Voltage (Note 3)	R_S =100Ω, 0.1Hz to 10Hz			2		μV_{P-P}
		R_S = 100Ω, 0.1Hz to 1Hz			0.75		μV_{P-P}
i_n	Input Noise Current	f = 10Hz			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3V, T_A = 25°C	●	110	130		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.5V to 2.5V	●	106	130		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	R_L = 1k	●	2	2.20		V
		R_L = 100k, V_S = ±1.5V	●	±2	±1.48		V
SR	Slew Rate	R_L = 10k, C_L = 50pF, V_S = ±1.5V			1		V/µs
GBW	Gain-Bandwidth Product	R_L = 10k, C_L = 50pF, V_S = ±1.5V			1		MHz
I_S	Supply Current	No Load	●		1.8	2.5	mA
		SHUTDOWN = 0V	●		1.0	5.0	µA
I_{OSD}	Output Leakage Current	SHUTDOWN = 0V	●		±10		nA
V_{CP}	Charge Pump Output Voltage		●	3.6	4.5	5	V
V_{IL}	Shutdown Pin Input Low Voltage		●		1.2		V
V_{IH}	Shutdown Pin Input High Voltage		●		2.3		V
I_{IN}	Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 0V	●		−1		µA
f_{CP}	Internal Charge Pump Frequency	T_A = 25°C			4.2		MHz
f_{SMPL}	Internal Sampling Frequency	T_A = 25°C			2.1		kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

Note 2: At T ≤ 0°C these parameters are guaranteed by design and not tested.

Note 3: 0.1Hz to 10Hz noise is specified DC coupled in a 10s window; 0.1Hz to 1Hz noise is specified in a 100s window with an RC highpass filter at 0.1Hz. For 100% tested parts, contact LTC Marketing Dept.

Note 4: All output swing measurements are taken with the load resistor connected from output to ground. For single supply tests, only the positive swing is specified (negative swing will be 0V due to the pull-down effect of the load resistor). For dual supply operation, both positive and negative swing are specified.

APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LTC1152 is a rail-to-rail input common mode, rail-to-rail output swing op amp. Most CMOS op amps (including the entire LTC zero-drift amplifier line), and even a few bipolar op amps can, and do, claim rail-to-rail output swing. One obvious use for such a device is to provide a unity gain buffer for 0V to 5V signals running from a single 5V power supply. This is not possible with the vast majority of so-called "rail-to-rail" op amps; although the output can swing to both rails, the negative input (which is connected to the output) will exceed the common-mode input range of the device at some point (generally about 1.5V below the positive supply), opening the feedback loop and causing unpredictable and sometimes bizarre behavior.

The LTC1152 is an exception to this rule. It features both rail-to-rail output swing and rail-to-rail input common-mode range (CMR); the input CMR actually extends beyond either rail by about 0.3V. This allows unity-gain buffer circuits to operate with any input signal within the

APPLICATIONS INFORMATION

power supply rails; input signal swing is limited only by the output stage swing into the load. Additionally, signals occurring at either rail (power supply current sensing, for example) can be amplified without any special circuitry.

Internal Charge Pump

The LTC1152 achieves its rail-to-rail input CMR by using a charge pump to generate an internal voltage approximately 2V higher than V^+. The input stages of the op amp are run from this higher voltage, making signals at V^+ appear to be 2V below the front end's power supply. The charge pump is entirely contained within the LTC1152; no external components are required. A small amount of residual charge pump switching noise will be present on the output of the LTC1152. This feedthrough is at 4.7MHz, higher than the gain-bandwidth of the LTC1152 and will generally not cause any problems. Very sensitive applications can reduce this feedthrough by connecting a capacitor from the CP pin (pin 8) to V^+ (pin 7); a 0.1µF capacitor will reduce charge pump feedthrough to negligible levels. The LTC1152 includes an internal diode from pin 8 to pin 7 to prevent external parasitic capacitance from lengthening start-up time. This diode can stand short-term peak currents of about 50mA, allowing it to quickly charge external capacitance to ground or V^-. Large capacitors (>1µF) should not be connected between pin 8 and ground or V^- to prevent excessive diode current from flowing at start-up. The LTC1152 can withstand continuous short-circuits between pin 8 and V^+; however, short-circuiting pin 8 to ground or V^- will cause large amounts of current to flow through the diode, destroying the LTC1152. Don't do it.

Output Drive and Compensation

The LTC1152 features an enhanced output stage that can sink and source 10mA while maintaining rail-to-rail output swing. Additionally, the LTC1152 is unity-gain stable with capacitive load up to 1000pF. Larger capacitive loads can be driven by externally compensating the LTC1152. Adding 1000pF between COMP (pin 5) and OUT (pin 6) allows capacitive loads of up to 1µF; 0.1µF between pins 5 and 6 allows the LTC1152 to drive infinite capacitive loads.

Shutdown

The LTC1152 includes a shutdown pin (pin 1). When this pin is at V^+, the LTC1152 operates normally. An internal 1µA pull-up keeps the pin high if it is left floating. When pin 1 is pulled low the part enters shutdown mode. Supply current drops to 1µA, all internal clocking stops and the output enters a high impedance state. During shutdown the voltage at the CP pin (pin 8) will drop to 0.5V below V^+. When pin 1 is brought high again a short time will elapse before the charge pump regains full voltage. During this time the LTC1152 will operate normally, but the input CMR may not include V^+. Pin 1 is compatible with CMOS logic running from the same supply as the LTC1152. Additionally, the input trip levels allow ground referenced CMOS logic signals to interface directly to pin 1 when the LTC1152 is running from ±5V or ±3V supplies. The internal 1µ pull-up also allows pin 1 to interface with open-collector/open-drain devices or discrete transistors.

Zero-Drift Operation

The LTC1152 is a zero-drift op amp. Like other LTC zero-drift op amps, it features virtually error-free DC performance, very little drift over time and temperature, and very low noise at low frequencies. It will exhibit aliasing behavior and clock ripple at frequencies near the internal 2.3kHz sampling frequency. These effects are generally quite small and will not affect most applications. For a more detailed explanation of zero-drift amplifier behavior, see the LTC1051/LTC1053 data sheet.

INITIAL RELEASE
Final Electrical Specifications

LTC1159/LTC1159-3.3/LTC1159-5

High Efficiency Synchronous Step-Down Switching Regulators

May 1994

FEATURES

- Operation from 4V to 40V Input Voltage
- Ultra-High Efficiency: Up to 95%
- 20μA Supply Current in Shutdown
- High Efficiency Maintained Over Wide Current Range
- Current Mode Operation for Excellent Line and Load Transient Response
- Very Low Dropout Operation: 100% Duty Cycle
- Short-Circuit Protection
- Synchronous FET Switching for High Efficiency
- Adaptive Non-Overlap Gate Drives
- Available in SSOP and SO Packages

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

DESCRIPTION

The LTC1159 series is a family of synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture.

A separate pin and on-board switch allow the MOSFET driver power to be derived from the regulated output voltage providing significant efficiency improvement when operating at high input voltages. The constant off-time current-mode architecture maintains constant ripple current in the inductor and provides excellent line and load transient response. The output current level is user programmable via an external current sense resistor.

The LTC1159 automatically switches to power saving Burst Mode operation when load current drops below approximately 15% of maximum current. Standby current is only 300μA while still regulating the output and shutdown current is a low 20μA.

Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

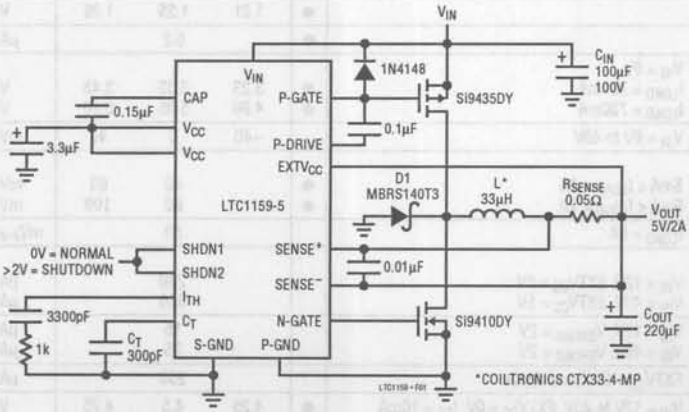
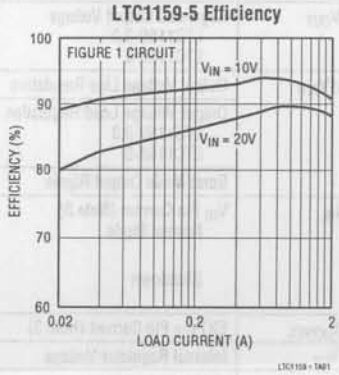


Figure 1. High Efficiency Step-Down Regulator



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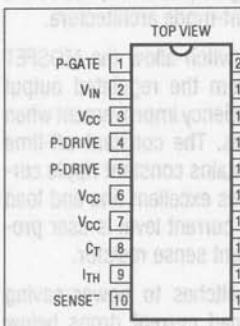
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –15V to 60V
V_{CC} Output Current (Pin 3) 50mA
Continuous Pin Currents (Any Pin) 50mA
Sense Voltages ..... –0.3V to 13V
Shutdown Voltages 7V
$EXTV_{CC}$ Input Voltage 15V

Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

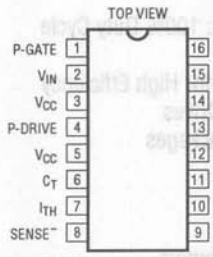


G PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1159CG
LTC1159CG-3.3
LTC1159CG-5



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD PLASTIC SOIC

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 80°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1159CN
LTC1159CN-3.3
LTC1159CN-5
LTC1159CS
LTC1159CS-3.3
LTC1159CS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{SHDN1} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		●	1.21	1.25	1.29	V
I_{FB}	Feedback Current (LTC1159 Only)		●		0.2		µA
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1159-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1159-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 40V		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1159-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1159-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_{IN}	V_{IN} Pin Current (Note 3)						
	Normal Mode	V_{IN} = 12V, $EXTV_{CC}$ = 5V			200		µA
		V_{IN} = 40V, $EXTV_{CC}$ = 5V			300		µA
	Shutdown	V_{IN} = 12V, V_{SHDN2} = 2V			15		µA
		V_{IN} = 40V, V_{SHDN2} = 2V			25		µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 3)	$EXTV_{CC}$ = 5V, Sleep Mode			250		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA	●	4.25	4.5	4.75	V
$V_{IN} – V_{CC}$	V_{CC} Dropout Voltage	V_{IN} = 4V, $EXTV_{CC}$ = Open, I_{CC} = 10mA			300	400	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{SHDN1} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{EXT} - V_{CC}$	$EXTV_{CC}$ Switch Drop	V_{IN} = 12V, $EXTV_{CC}$ = 5V, I_{SWITCH} = 10mA			250	350	mV
$V_{P-GATE} - V_{IN}$	P-Gate to Source Voltage (Off)	V_{IN} = 12V V_{IN} = 40V		−0.2 −0.2	0 0		V V
$V_{SENSE^+} - V_{SENSE^-}$	Current Sense Threshold Voltage LTC1159	 V_{SENSE^-} = 5V, V_{FB} = 1.32V (Forced) V_{SENSE^-} = 5V, V_{FB} = 1.15V (Forced)	 ●	 130	 25 150	 170	 mV mV
	LTC1159-3.3	V_{SENSE^-} = 3.4V (Forced) V_{SENSE^-} = 3.1V (Forced)	 ●	 130	25 150	 170	mV mV
	LTC1159-5	V_{SENSE^-} = 5.2V (Forced) V_{SENSE^-} = 4.7V (Forced)	 ●	 130	25 150	 170	mV mV
V_{SNDN1}	SHDN1 Threshold LTC1159CG, LTC1159-3.3, LTC1159-5			0.6	0.8	2	V
V_{SHDN2}	SHDN2 Threshold			0.8	1.4	2	V
I_{SHDN2}	Shutdown 2 Input Current	V_{SHDN2} = 5V			12	20	µA
I_{CT}	C_T Pin Discharge Current	V_{OUT} in Regulation V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins P-Drive and N-Gate), V_{IN} = 6V			100	200	ns

−40°C ≤ T_A ≤ 85°C (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage LTC1159-3.3 LTC1159-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA	 3.17 4.85	 3.30 5.05	 3.43 5.25	 V V
I_{IN}	V_{IN} Pin Current (Note 3) Normal	 V_{IN} = 12V, $EXTV_{CC}$ = 5V V_{IN} = 40V, $EXTV_{CC}$ = 5V		 200 300		 µA µA
	Shutdown	V_{IN} = 12V, V_{SHDN2} = 2V V_{IN} = 40V, V_{SHDN2} = 2V		15 25		µA µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 3)	$EXTV_{CC}$ = 5V, Sleep Mode		250		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA		4.5		V
$V_{SENSE^+} - V_{SENSE^-}$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)	 125	25 150	 175	mV mV
V_{SHDN2}	SHDN2 Threshold		0.8	1.4	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V	3.5	5	6.5	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1159CG, LTC1159CG-3.3, LTC1159CG-5: $T_J = T_A + (P_D \times 135°C/W)$
LTC1159CN, LTC1159CN-3.3, LTC1159CN-5: $T_J = T_A + (P_D \times 80°C/W)$
LTC1159CS, LTC1159CS-3.3, LTC1159CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: On LTC1159 versions which have a SHDN1 pin, it must be at ground potential for testing.

Note 3: The LTC1159 V_{IN} and $EXTV_{CC}$ current measurements exclude MOSFET driver currents. When V_{CC} power is derived from the output via $EXTV_{CC}$, the input current increases by ($I_{GATECHG}$ × Duty Cycle)/(Efficiency). See Typical Performance Characteristics and Applications Information.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 5: The LTC1159, LTC1159-3.3, and LTC1159-5 are not tested and not quality assurance sampled at −40°C and 85°C. These specifications are guaranteed by design and/or correlation.

Note 6: The logic-level power MOSFETs shown in Figure 1 are rated for $V_{DS(MAX)}$ = 30V. For operation at V_{IN} > 30V, use standard threshold MOSFETs with $EXTV_{CC}$ powered from a 12V supply. See Applications Information.

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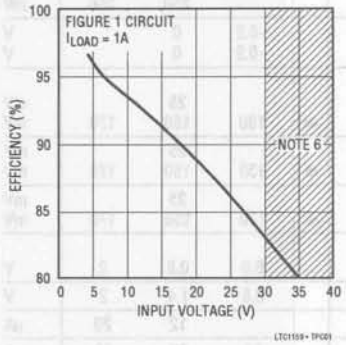
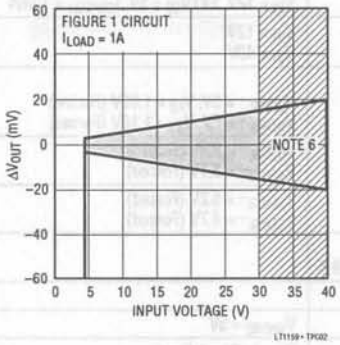
TYPICAL PERFORMANCE CHARACTERISTICS

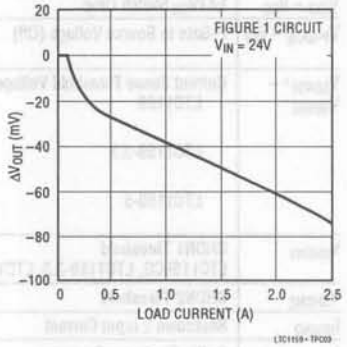
Efficiency vs Input Voltage



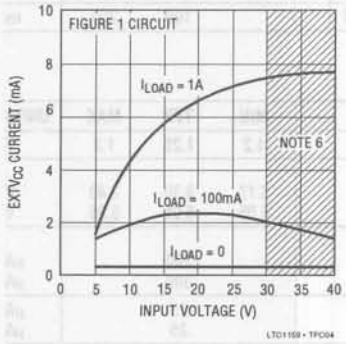
Line Regulation



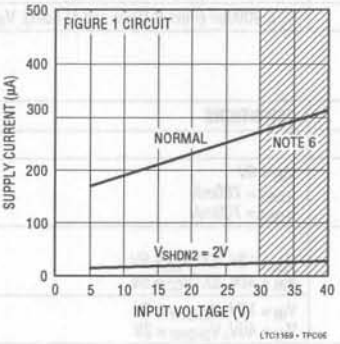
Load Regulation



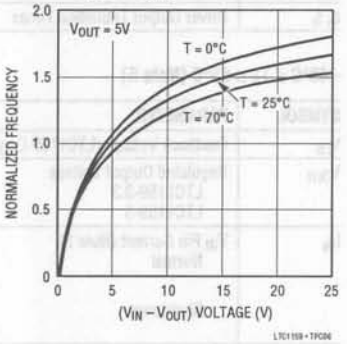
$EXTV_{CC}$ Pin Current



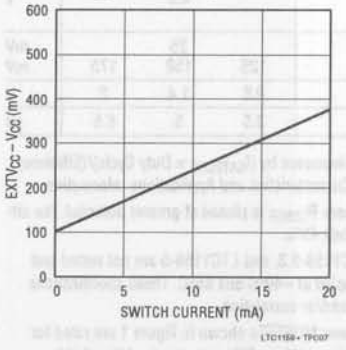
V_{IN} Pin Current



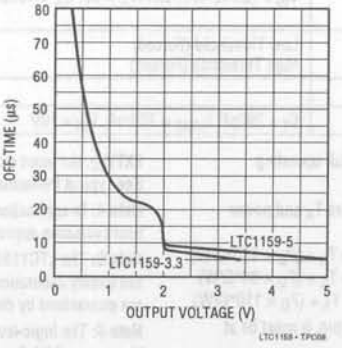
Operating Frequency vs ($V_{IN} - V_{OUT}$)



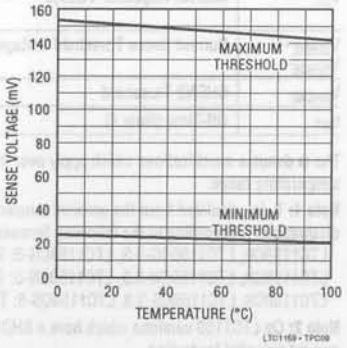
$EXTV_{CC}$ Switch Drop



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

V_{IN}: Main Supply Input Pin.

S-GND: Small Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

P-GND: Driver Power Grounds. Connect to source of N-channel MOSFET and the (–) terminal of C_{IN}.

V_{CC}: Outputs of internal 4.5V linear regulator, $EXTV_{CC}$ switch, and supply inputs for driver and control circuits. The driver and control circuits are powered from the higher of the 4.5V regulator or $EXTV_{CC}$ voltage. Must be closely decoupled to power ground.

C_T: External capacitor C_T from this pin to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

I_{TH}: Gain Amplifier Decoupling Point. The current comparator threshold increases with the I_{TH} pin voltage.

V_{FB}: For the LTC1159 adjustable version, the V_{FB} pin receives the feedback voltage from an external resistive divider used to set the output voltage.

Sense⁻: Connects to internal resistive divider which sets the output voltage in fixed output versions. The Sense⁻ pin is also the (–) input of the current comparator.

Sense⁺: The (+) Input for the Current Comparator. A built-in offset between the Sense⁺ and Sense⁻ pins, in conjunction with R_{SENSE}, sets the current trip threshold.

N-Gate: High Current Drive for the Bottom N-Channel MOSFET. The N-Gate pin swings from ground to V_{CC}.

P-Gate: Level-Shifted Gate Drive Signal for the Top P-Channel MOSFET. The voltage swing at the P-gate pin is from V_{IN} to $V_{IN} - V_{CC}$.

P-Drive: High Current Gate Drive for the Top P-Channel MOSFET. The P-drive pin(s) swing(s) from V_{CC} to ground.

CAP: Charge Compensation Pin. A capacitor to V_{CC} provides charge required by the P-gate level-shift capacitor during supply transitions. *The charge compensation capacitor must be larger than the gate drive capacitor.*

SHDN1: This pin shuts down the control circuitry only (V_{CC} is not affected). Taking SHDN1 pin high turns off the control circuitry and holds both MOSFETs off. This pin must be at ground potential for normal operation.

SHDN2: Master Shutdown Pin. Taking SHDN2 high shuts down V_{CC} and all control circuitry.

OPERATION (Refer to Functional Diagram)

The LTC1159 uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the C_T pin.

The output voltage is sensed either by an internal voltage divider connected to the Sense⁻ pin (LTC1159-3.3 and LTC1159-5) or an external divider returned to the V_{FB} pin (LTC1159). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1159 automatically switches between two modes of operation, burst and continuous.

A low dropout 4.5V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry during start-up. During normal operation, the LTC1159 family powers the drivers and control from the output via the $EXTV_{CC}$ pin to improve efficiency. The N-gate pin is referenced to ground and drives the N-channel MOSFET gate directly. The P-channel gate drive must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the P-drive signal via an internal 550k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between the Sense⁺ and Sense⁻ pins connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-gate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor C_T is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-gate output is high, turning on the N-channel MOSFET.

OPERATION (Refer to Functional Diagram)

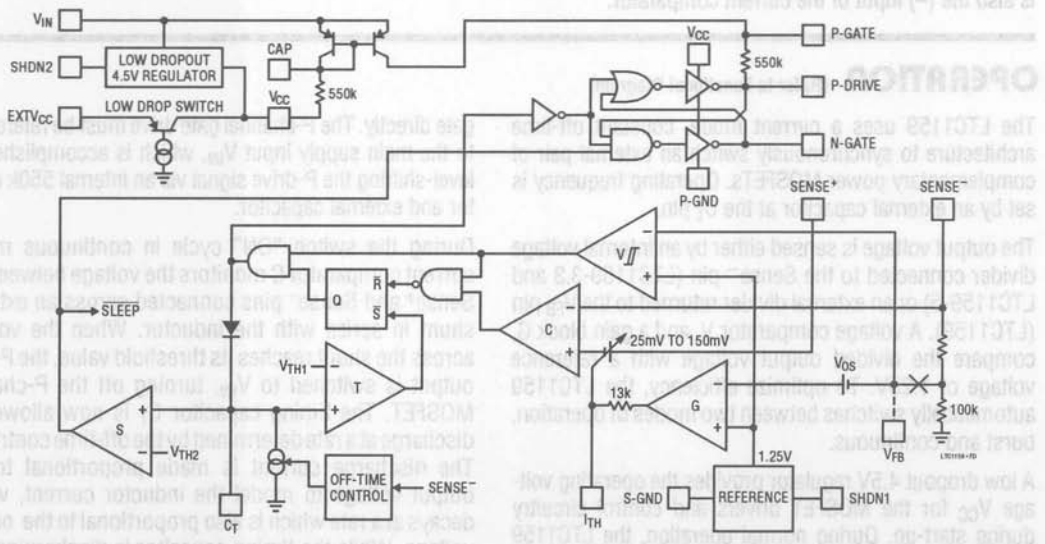
When the voltage on C_T has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-gate output to go low (turning off the N-channel MOSFET) and the P-gate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats. As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several milliamps (with the MOSFETs switching) to 300μA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset is incorporated in the gain stage.

To prevent both the external MOSFETs from being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

FUNCTIONAL DIAGRAM Internal divider broken at V_{FB} for adjustable versions.



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The LTC1159 Compared to the LTC1148/LTC1149 Families

The LTC1159 family is closest in operation to the LTC1149 and shares much of the applications information. In addition to reduced quiescent and shutdown currents, the LTC1159 adds an internal switch which allows the driver and control sections to be powered from an external source for higher efficiency. This change affects Power MOSFET Selection, $EXTV_{CC}$ Pin Connection, Important Information About LTC1159 Adjustable Applications, and Efficiency Considerations found in this section.

The basic LTC1159 application circuit shown in Figure 1 is limited to a maximum input voltage of 30V due to MOSFET breakdown. If the application does not require greater than 18V operation, then the LTC1148 or LTC1148HV should be used. For higher input voltages where quiescent and shutdown current are not critical, the LTC1149 may be a better choice since it is set up to drive standard threshold MOSFETs.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1159 current comparator has a threshold range which extends from a minimum of $0.025V/R_{SENSE}$ to a maximum of $0.15V/R_{SENSE}$. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 0.025V/R_{SENSE}$ (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1159 and external component values yields:

$$R_{SENSE} = \frac{100}{I_{MAX}}\ m\Omega$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1159 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1159 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

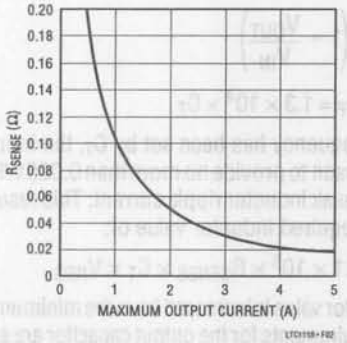

Figure 2. R_{SENSE} vs Maximum Output Current

L and C_T Selection for Operating Frequency

The LTC1159 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{7.8 \times 10^{-5}}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

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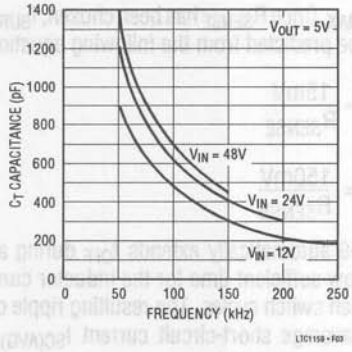

Figure 3. Timing Capacitor Selection

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $t_{OFF} = 1.3 \times 10^4 \times C_T$

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $0.025V/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the LTC1159 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses go down but copper (I^2R) losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1159. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

Power MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1159: a P-channel MOSFET for the main switch and an N-channel MOSFET for the synchronous switch.

The peak-to-peak drive levels are set by the V_{CC} voltage on the LTC1159. This voltage is typically 4.5V during start-up and 5V to 7V during normal operation (see $EXTV_{CC}$ Pin Connection). Consequently, *logic-level threshold MOSFETs must be used in most LTC1159 family applications*. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V, in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1159 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET dissipations at maximum output current are given by:

Kool Mμ is a registered trademark of Magnetics, Inc.

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$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P) R_{DS(ON)} + k(V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the P-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The N-channel MOSFET losses are the greatest at high input voltage or during a short circuit when the N-channel duty cycle is nearly 100%.

The term $(1 + \partial)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\partial = 0.007/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant k = 5 can be used for the LTC1159 to estimate the relative contributions of the two terms in the P-channel dissipation equation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead time between the conduction of the two power MOSFETs. D1 prevents the body diode of the N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX} [V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1159:

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. Manufacturers such as Nichicon, Chemicon, and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode operation to be activated when the LTC1159 would normally be in continuous operation. The effect is most

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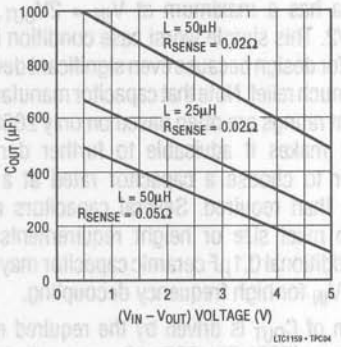

Figure 4. Minimum Suggested C_{OUT}

pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

Checking Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} external components shown in the Figure 1 circuit will provide adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

$EXTV_{CC}$ Pin Connection

The LTC1159 contains an internal PNP switch connected between the $EXTV_{CC}$ and V_{CC} pins. The switch closes and supplies the V_{CC} power whenever the $EXTV_{CC}$ pin is higher in voltage than the 4.5V internal regulator. This allows the MOSFET driver and control power to be derived from the output during normal operation and from the internal regulator when the output is out of regulation (start-up, short circuit).

Significant efficiency gains can be realized by powering V_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other low voltage regulators, additional circuitry is required to derive V_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open. This will cause V_{CC} to be powered only from the internal 4.5V regulator resulting in reduced MOSFET gate drive levels and an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected Directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.5V. This can be done either with the inductive boost winding shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics and generally provides the highest efficiency at the expense of a slightly higher parts count.

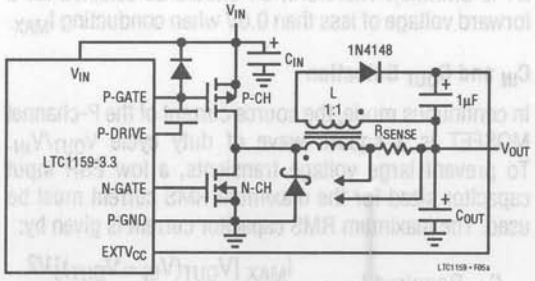

Figure 5a. Inductive Boost Circuit for $EXTV_{CC}$

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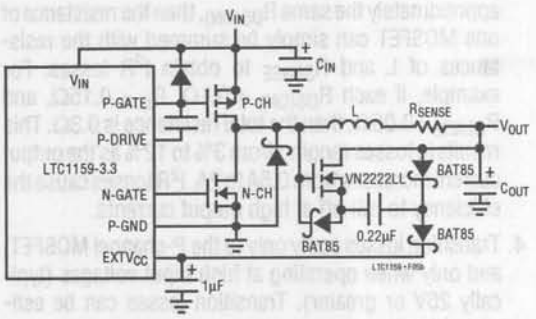

Figure 5b. Capacitive Charge Pump for $EXTV_{CC}$

4. $EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 12V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. *When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.* The LTC1149 family should also be considered for applications which require the use of standard threshold MOSFETs.

Important Information About LTC1159 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1159 adjustable version is used with an external resistive divider from V_{OUT} to the V_{FB} pin (Figure 6). The regulated voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) 1.25V$$

The V_{FB} pin is extremely sensitive to pickup from the inductor switching node. Care should be taken to isolate the feedback network from the inductor, and the 100pF capacitor should be connected between the V_{FB} and S-GND pins next to the package.

In LTC1159N and LTC1159S applications with V_{OUT} > 5.5V, the V_{CC} pin may self-power through the Sense pins when SHDN2 is taken high, preventing shutdown. In these applications, a pull-down must be added to the $Sense^-$ pin as shown in Figure 6. This pull-down effectively takes the place of the SHDN1 pin, ensuring complete shutdown. Note: For versions in which both the SHDN1 and SHDN2 pins are available (LTC1159G and all fixed output versions), the two pins are simply connected to each other and driven together to guarantee complete shutdown.

The Figure 6 circuit cannot be used to regulate a V_{OUT} which is greater than the maximum voltage allowed on the LTC1159 Sense pins (13V). In applications with V_{OUT} > 13V, R_{SENSE} must be moved to the ground side of the output capacitor and load. This operates the current sense comparator at 0V common mode, increasing the off-time approximately 40% and requiring the use of a smaller timing capacitor C_T.

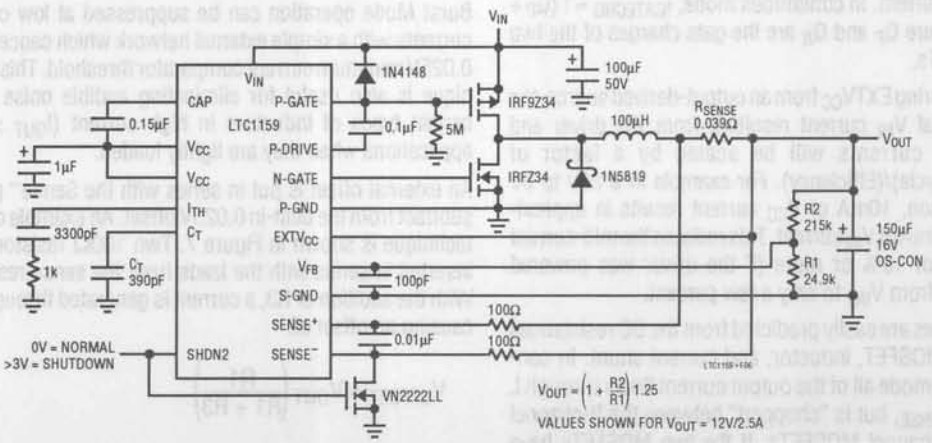

Figure 6. High Efficiency Adjustable Regulator with 5.5V < V_{OUT} < 13V

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1159 circuits: 1) LTC1159 V_{IN} current, 2) LTC1159 V_{CC} current, 3) I^2R losses, and 4) P-channel transition losses.

1. LTC1159 V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<1%) loss which increases with V_{IN}.
2. LTC1159 V_{CC} current is the sum of the MOSFET driver and control circuit currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} \approx f\ (Q_P + Q_N)$, where Q_P and Q_N are the gate charges of the two MOSFETs.

   By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For example in a 20V to 5V application, 10mA of V_{CC} current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.
3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.1\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.
4. Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 5(V_{IN})^2(I_{MAX})(C_{RSS})(f)$$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead time, and inductor core losses, generally account for less than 2% total additional loss.

Auxiliary Windings – Suppressing Burst Mode Operation

The LTC1159 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 0.025V minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the $Sense^-$ pin to subtract from the built-in 0.025V offset. An example of this technique is shown in Figure 7. Two 100Ω resistors are inserted in series with the leads from the sense resistor. With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

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If V_{OFFSET} > 0.025V, the minimum threshold will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be reduced:

$$R_{SENSE} \approx \frac{75}{I_{MAX}}\ m\Omega$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across the Sense⁻ and Sense⁺ pins.

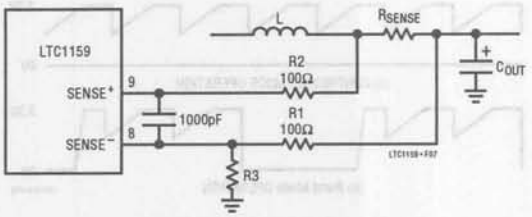

Figure 7. Suppressing Burst Mode Operation

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1159. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1159 signal ground must connect separately to the (–) plate of C_{OUT}. The other ground pin(s) should return to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2) Does the LTC1159 Sense⁻ pin connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3) Are the Sense⁻ and Sense⁺ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between the two Sense pins should be as close as possible to the LTC1159. Up to 100Ω may be

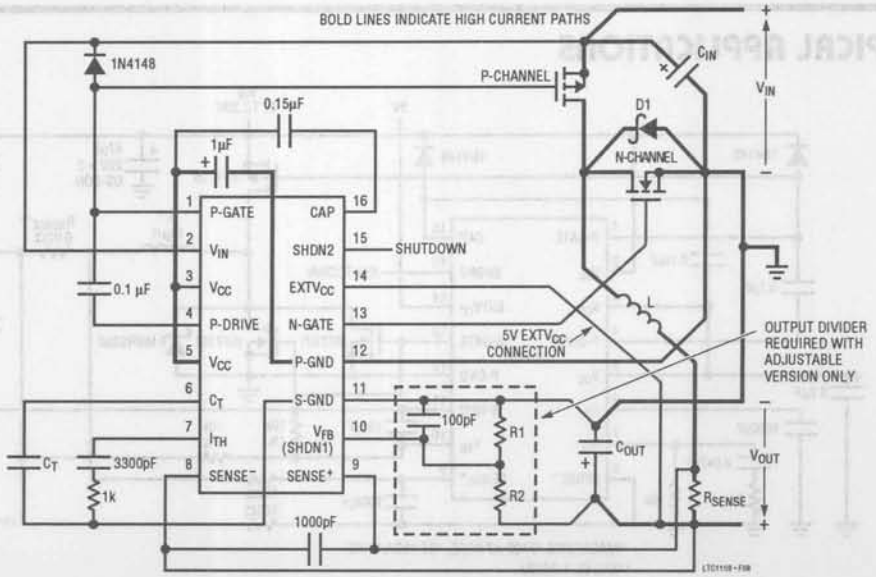

Figure 8. LTC1159 Layout Diagram (N and S Packages)

APPLICATIONS INFORMATION

placed in series with each sense lead to help decouple the Sense pins. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.
5) Is the V_{CC} decoupling capacitor connected closely between the V_{CC} pins of the LTC1159 and power ground? This capacitor carries the MOSFET driver peak currents.
6) In adjustable versions, the feedback pin is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.
7) Is the SHDN1 pin actively pulled to ground during normal operation? SHDN1 is a high impedance pin and must not be allowed to float.

Troubleshooting Hints

Since efficiency is critical to LTC1159 applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pin .

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a. When the load current is low ($I_{LOAD} < I_{BURST}$), Burst Mode operation should occur with the C_T waveform periodically falling to ground as shown in Figure 9b.

If the C_T pin is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

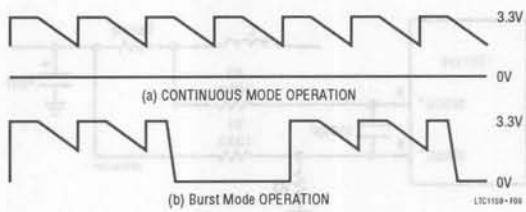

Figure 9. C_T Pin 6 Waveforms

TYPICAL APPLICATIONS

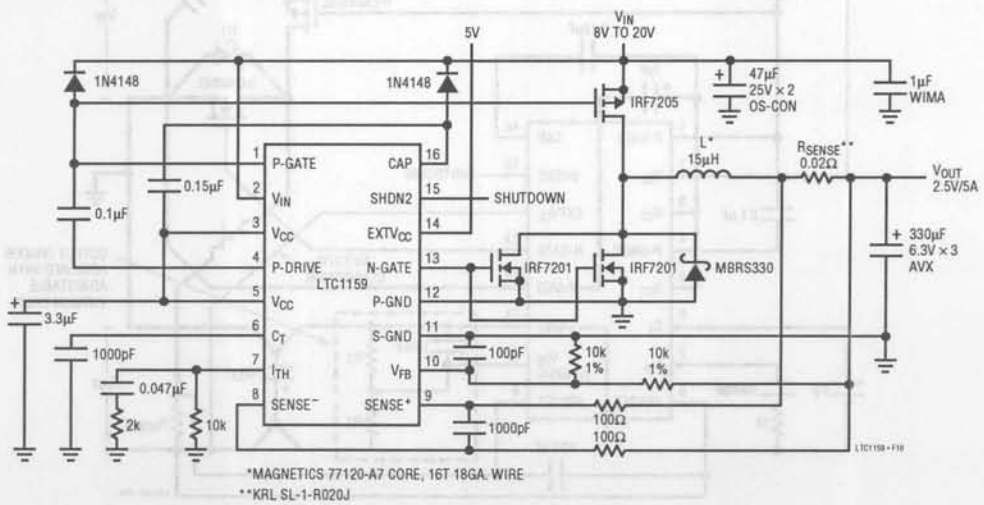

Figure 10. High Efficiency 8V to 20V Input 2.5/5A Output Regulator

TYPICAL APPLICATIONS

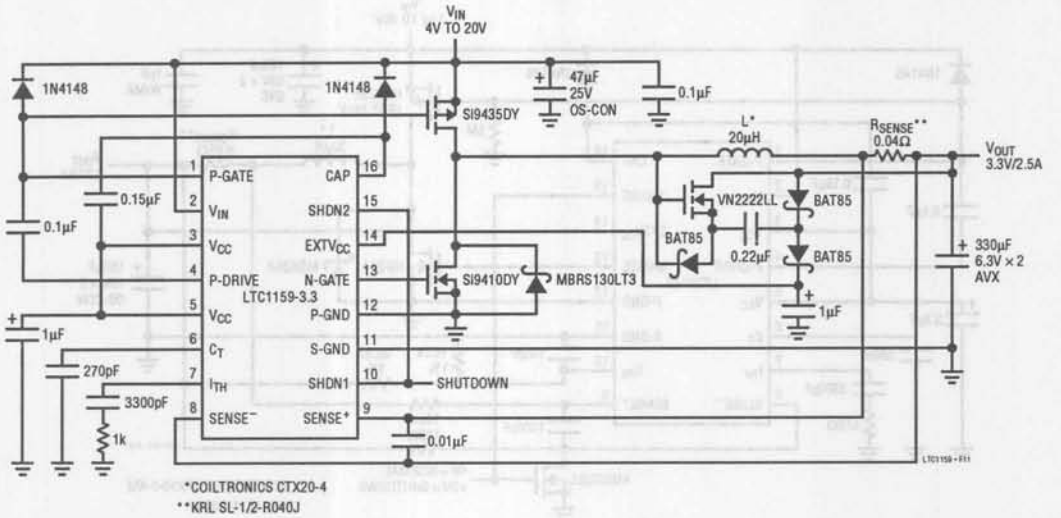

Figure 11. 5:1 Input Range (4V to 20V) High Efficiency 3.3V/2.5A Regulator

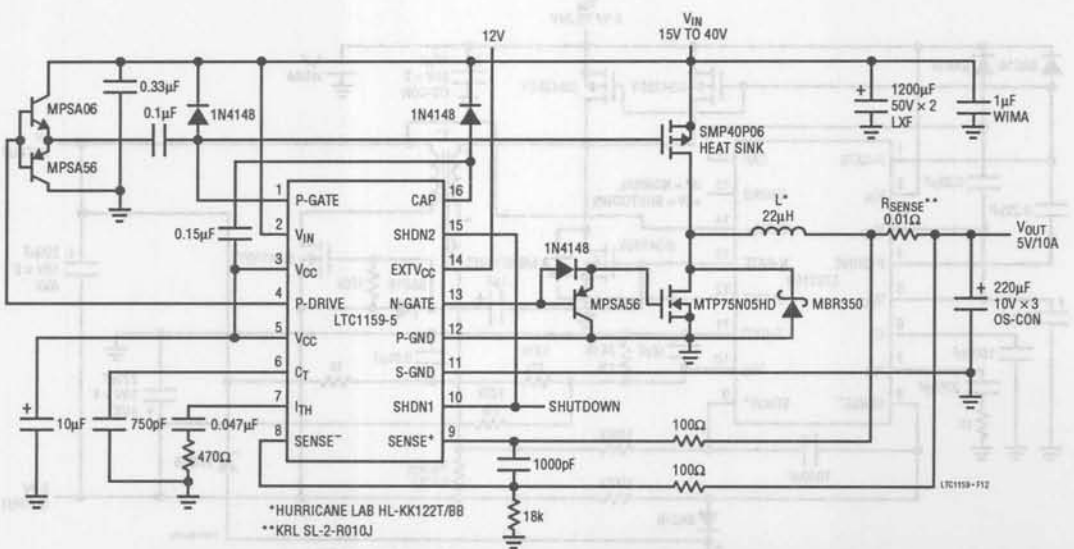

Figure 12. High Current, High Efficiency 15V to 40V Input 5V/10A Output Regulator

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TYPICAL APPLICATIONS

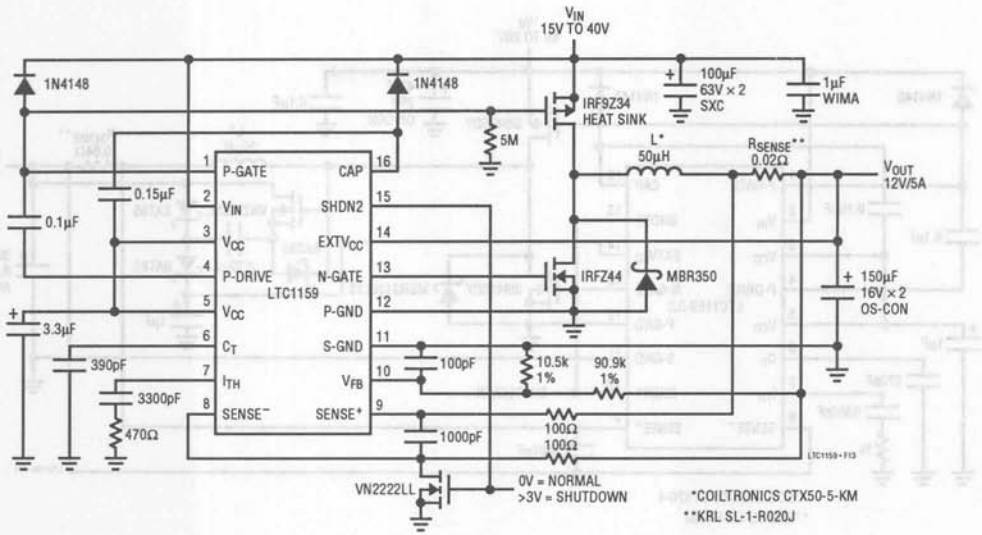


Figure 13. High Efficiency 15V to 40V Input 12V/5A Output Regulator

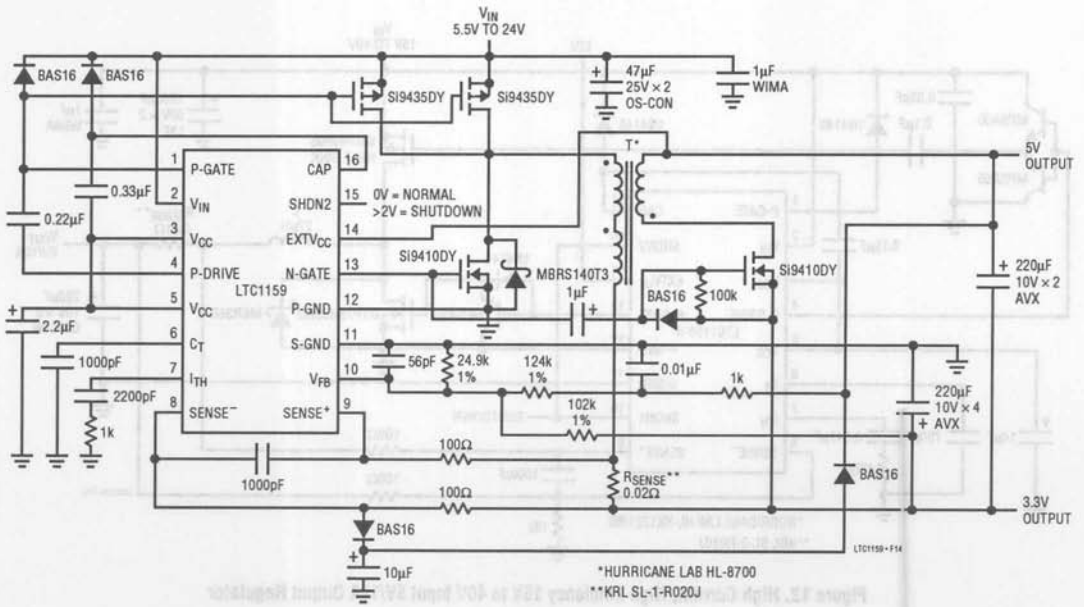


Figure 14. 17W Dual Output High Efficiency 5V and 3.3V Regulator

LT1182/LT1183

CCFL/LCD Contrast Dual Switching Regulator

June 1994

FEATURES

- Wide Input Voltage Range: 3V to 30V
- Low Quiescent Current: 4.5mA per Regulator
- High Switching Frequency: 200kHz
- CCFL Switch: 1.25A / LCD Switch: 625mA
- Grounded or Floating Bulb Configurations
- Open Bulb Protection
- Positive or Negative Contrast Capability

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Automotive Displays
- Retail Terminals

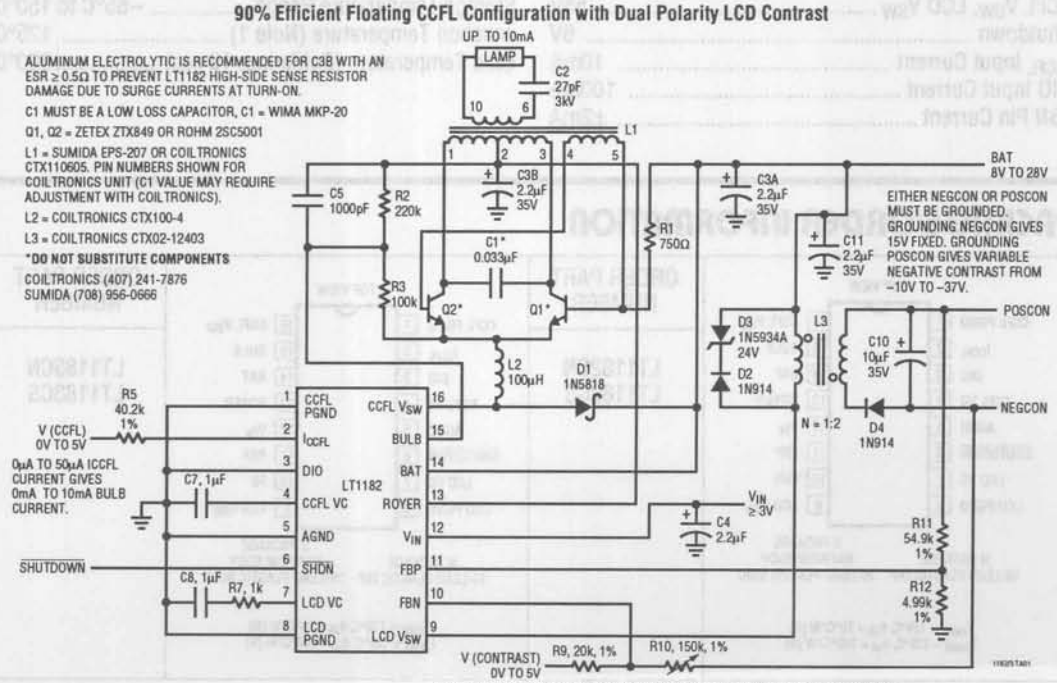
DESCRIPTION

The LT1182/LT1183 are dual current-mode switching regulators that provide the control function for Cold Cathode Fluorescent Lighting and Liquid Crystal Display Contrast. Two high current, high efficiency switches are included on the die along with an oscillator, reference, output drive logic, control blocks and protection circuitry. The LT1183 brings out the internal reference and ties the inputs of the LCD contrast error amplifier together in comparison to the LT1182. The LT1182/LT1183 are available in 16-pin narrow body SOIC and 16-pin plastic DIP.

The LT1182/LT1183 operate with supply voltages from 3V to 30V and draw only 9mA quiescent current. A shutdown pin reduces total supply current to less than 50µA for

TYPICAL APPLICATION

90% Efficient Floating CCFL Configuration with Dual Polarity LCD Contrast



NOTE: GND V (CONTRAST) IF ONLY POSITIVE CONTRAST VOLTAGES ARE GENERATED.

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DESCRIPTION

standby operation. A 200kHz switching frequency minimizes the size of required magnetic components. The use of current-mode switching techniques with cycle by cycle limiting gives high reliability and simple loop frequency compensation.

The CCFL regulator typically drives an inductor that acts as a switched-mode current source for a current-driven Royer class converter with efficiencies as high as 90%. The control loop forces the CCFL PWM to modulate the inductor's average current to maintain constant current in the lamp. The constant current value, and thus lamp intensity, is programmable. This drive technique provides a wide range of intensity control. A unique bulb current programming block allows either grounded or floating bulb configurations. Grounded circuits directly sense one-half of actual bulb current. Floating circuits directly sense Royer primary-side supply current. Floating circuits provide differential drive to the bulb and significantly reduce the loss from stray bulb to frame capacitance, thereby extending illumination range.

The LCD Contrast regulator is typically configured as a flyback converter and generates a bias supply for contrast control. The supply's variable output permits adjustment of display contrast. A unique error amplifier and the choice of flyback allows either positive or negative LCD Contrast voltages to be generated with minor circuit changes.

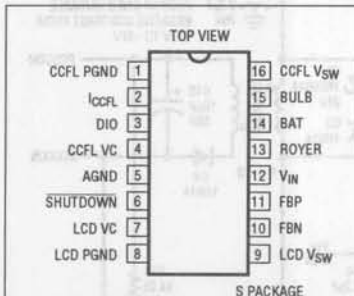
The LT1184 will be available in the near future which provides only the CCFL function. Consult factory for further details.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, BAT, Royer, Bulb 30V
CCFL V_{SW}, LCD V_{SW} 55V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current 100mA
FBN Pin Current ..... ±2mA

Operating Ambient Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 1) ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

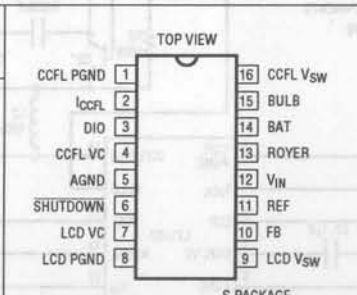


N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
NARROW BODY
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LT1182CN
LT1182CS



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
NARROW BODY
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LT1183CN
LT1183CS

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, CCFL VC = LCD VC = 0.5V, CCFL V_{SW} = LCD V_{SW} = ICCFL = $\overline{\text{Shutdown}}$ = Open, DIO = FBN = FBP = GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	3V ≤ V_{IN} ≤ 30V	●		9	14	mA
$I_{\overline{SHDN}}$	$\overline{\text{Shutdown}}$ Supply Current	$\overline{\text{Shutdown}}$ = 0V, CCFL VC = LCD VC = Open (Note 2)			40	60	µA
	$\overline{\text{Shutdown}}$ Input Bias Current	$\overline{\text{Shutdown}}$ = 0V, CCFL VC = LCD VC = Open			3		µA
	$\overline{\text{Shutdown}}$ Threshold Voltage		●	0.7	0.85	1.0	V
f	Switching Frequency	Measured at CCFL V_{SW}, I_{SW} = 50mA, FBN = FBP = 1V			200		kHz
		CCFL VC = LCD VC = Open, ICCFL = 100µA	●		200		kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW} and LCD V_{SW}			85		%
	Input Operating Voltage		●	3.0		30	V
BV	Switch Breakdown Voltage	I_{SW} = 2mA, Measured at CCFL V_{SW} and LCD V_{SW}	●	55	70		V
	CCFL Switch Leakage Current	V_{SW} = 12V				2.0	µA
		V_{SW} = 30V				5.0	µA
	LCD Switch Leakage Current	V_{SW} = 12V				2.0	µA
		V_{SW} = 30V				5.0	µA
	I_{CCFL} Summing Voltage	3V ≤ V_{IN} ≤ 30V			0.45		V
			●		0.45		V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			3		mV
	CCFL VC Offset Sink Current		●		0		µA
	ΔCCFL VC Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 0µA to 100µA	●		5		µA/µA
	CCFL VC to DIO Current Servo Ratio	DIO = 5mA Out of Pin, Current Measured at CCFL VC		97	100	103	µA/mA
	CCFL VC Low Clamp Voltage	Royer = 1A			0.1		V
	CCFL VC High Clamp Voltage	I_{CCFL} = 100µA			2.0		V
	CCFL VC Switching Threshold	CCFL V_{SW} DC = 0%			0.95		V
	CCFL High-Side Sense Current Transfer Ratio	Royer = 1A, Current Measured at CCFL VC CCFL VC = 1.5V		480	500	520	µA/A
	CCFL High-Side Sense Line Regulation	Royer = 1A, BAT = 5V to 30V CCFL VC = 1.5V			0.1		%/V
	CCFL High-Side Sense Supply Current	Measured at BAT, Royer	●		120		µA
	Bulb Protect Servo Voltage	I_{CCFL} = 100µA, CCFL VC = 0µA at 1.5V	●	6.65	7.0	7.35	V
	Bulb Input Bias Current	I_{CCFL} = 100µA, CCFL VC = 0µA at 1.5V			5		µA
I_{LIM1}	CCFL Switch Current Limit	Duty Cycle = 50%	●	1.25	2.0	3.0	A
		Duty Cycle = 80% (Note 3)	●	1.05	1.7	2.6	A
V_{SAT1}	CCFL Switch On Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW1}}$	Supply Current Increase During CCFL Switch On Time	CCFL I_{SW} = 1A			25		mA/A
	Switch Minimum On Time	Measured at CCFL V_{SW} and LCD V_{SW}			0.45		µs
REF1	LCD FBP Reference Voltage	Measured at FBP of LCD Error Amplifier, FBN = 1V,		1.224	1.244	1.264	V
		LCD VC = 0.8V	●		1.244		V
	FBP Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V, LCD VC = 0.8V	●		0.01		%/V
	FBP Input Bias Current	FBP = REF1, FBN = 1V, LCD VC = 0.8V			0.35	0.75	µA
			●		0.35	1.1	µA
	LCD FBN Offset Voltage	Measured at FBN of LCD Error Amplifier, FBP = GND,		–15	–10	–5	mV
		LCD VC = 0.8V	●		–10		mV
	FBN Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V	●		0.01		%/V

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, CCFL VC = LCD VC = 0.5V, CCFL V_{SW} = LCD V_{SW} = ICCFL = $\overline{\text{Shutdown}}$ = Open, DIO = FBN = FBP = GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	FBN Input Bias Current	FBN = FBN Offset Voltage, FBP = GND, LCD VC = 0.8V		–2.0	–1.0		µA
			●	–3.0	–1.0		µA
g_m	FBP to LCD VC Transconductance	ΔI LCD VC = ±25µA, LCD VC = 1.5V, FBN = 1V			1000		µmhos
			●		1000		µmhos
	FBN to LCD VC Transconductance	ΔI LCD VC = ±25µA, LCD VC = 1.5V, FBP = GND			900		µmhos
			●		900		µmhos
	LCD Error Amplifier Source Current	FBP = FBN = 1V or 0.25V			100		µA
			●		100		µA
	LCD Error Amplifier Sink Current	FBP = FBN = 1.5V or –0.25V			90		µA
			●		90		µA
	LCD VC High Clamp Voltage	FBP = FBN = 1V			2		V
	LCD VC Low Clamp Voltage	FBP = FBN = 1.5V			0.1		V
	LCD VC Switching Threshold	FBP = FBN = 1V, LCD V_{SW} DC = 0%			0.95		V
V_{REF}	Reference Voltage	Measured at REF (Pin 11) on LT1183		1.224	1.244	1.264	V
			●		1.244		V
	Reference Output Impedance	Measured at REF (Pin 11) on LT1183			30		Ω
	V_{REF} – ICCFL Summing Voltage			0.782	0.794	0.806	V
			●		0.794		V
I_{LIM2}	LCD Switch Current Limit	Duty Cycle = 50%	●	0.625	1.0	1.5	A
		Duty Cycle = 80% (Note 3)	●	0.50	0.85	1.3	A
V_{SAT2}	LCD Switch On Resistance	LCD I_{SW} = 0.5A	●		0.9	1.5	Ω
$\frac{\Delta I_Q}{\Delta I_{SW2}}$	Supply Current Increase During LCD Switch On Time	LCD I_{SW} = 0.5A			25		mA/A

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1182CN/LT1183CN: $T_J = T_A + (P_D \times 70°C/W)$

LT1182CS/LT1183CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 2: Does not include switch leakage.

Note 3: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 0.833\ (2 - DC)$ for the CCFL regulator and $I_{LIM} = 0.417\ (2 - DC)$ for the LCD Contrast regulator due to internal slope compensation circuitry.

PIN FUNCTIONS

LT1182

CCFL PGND: This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and allows for internal switch current sensing. Separate analog and power grounds have been provided for the CCFL and LCD regulators in order to minimize interaction.

ICCFL: This pin is the input to the CCFL bulb current programming circuit. This pin is internally regulated to 450mV and accepts an input current signal of 0µA to 100µA full scale which is converted to a 0µA to 500µA source current at the CCFL VC pin. By regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control.

DIO: This pin is the common connection between the cathode and anode of two internal diodes. DIO is used in a grounded-bulb configuration and connects directly to the low voltage side of the bulb. Bi-directional bulb current flows in the DIO pin and thus, the diodes conduct alternately on half cycles. Bulb current is controlled by monitoring one-half of the bulb current. The diode conducting on negative half cycles has one-tenth of its current di-

PIN FUNCTIONS

verted to the CCFL VC pin and nulls against the source current provided by the bulb current programmer circuit. The compensation capacitor on the CCFL VC pin acts not only to provide loop compensation but also to provide an averaging function to the rectified sinusoidal bulb current. This scheme reduces the number of loop compensation components and allows for faster loop transient response in comparison to previously published circuits. If a floating bulb configuration is used, this pin should be tied to ground.

CCFL VC: This pin is the output of the bulb current programmer circuit and the input of the current comparator for the CCFL regulator. It is used for frequency compensation, bulb current averaging for grounded-bulb circuits and current limiting. The voltage on the CCFL VC pin determines the current trip level for switch turnoff. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). This pin has a high impedance output, so the voltage can be clamped externally for adjusting current limit. Loop frequency compensation is typically performed with a series R/C network to ground.

AGND: This is the low current analog ground for the chip. It also acts as the sense for the LCD dual input error amplifier. External feedback divider networks which terminate to ground and frequency compensation components on the VC pins which terminate to ground should connect directly to this pin for best performance.

$\overline{\text{Shutdown}}$: Pulling this pin low causes complete regulator shutdown with quiescent current reduced to about 40μA. The threshold voltage for this pin is about 0.85V. If this pin is not used, it can be left to float high or pulled to a logic high level (max. of 6V). Allowing the pin to float high to provide active operation should be carefully evaluated as capacitive coupling into the pin from switching transients could cause erratic operation.

LCD VC: This pin is the output of the LCD Contrast dual input error amplifier and the input of the current comparator for the LCD Contrast regulator. It is used for frequency compensation and current limiting. The voltage on the LCD VC pin determines the current trip level for switch turnoff. During normal operation, this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). The LCD VC pin is a high impedance current output (g_m) error amplifier, so the voltage can be clamped externally for adjusting current limit. Loop frequency compensation is typically performed with a series R/C network to ground.

LCD PGND: This pin is the emitter of an internal NPN power switch. LCD Contrast switch current flows through this pin and allows for internal switch current sensing. Separate analog and power grounds have been provided for the CCFL and LCD regulators in order to minimize interaction.

LCD V_{SW}: This pin is the collector of the internal NPN power switch for the LCD Contrast regulator. The power switch is guaranteed to provide a minimum of 625mA. Fast switching times and high efficiency are obtained by using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state. The ratio of switch current to driver current is about 40:1.

FBN: This pin is the noninverting terminal for the negative contrast control error amplifier. The inverting terminal is offset from ground by –10mV to define the error amplifier output state under start-up conditions. The FBN pin acts as a summing junction for a resistor divider network. Input bias current for this pin is typically –1μA.

FBP: This pin is the inverting terminal for the positive contrast control error amplifier. The noninverting terminal is tied to an internal 1.24V reference. Input bias current for this pin is typically 0.5μA.

V_{IN}: This is the supply pin for the LT1182/LT1183. The IC accepts an input voltage range of 3V minimum to 30V maximum with little change in quiescent operating current (zero switch current) as a low dropout internal regulator provides a 2.4V supply for the majority of the internal circuitry. Supply current increases as each PWM's switch current increases at a rate approximately 1/40 of each switch current. This corresponds to a forced Beta of 40 for each switch. Undervoltage lockout is incorporated by sensing the saturation of the lateral PNP pass transistor which drives the 2.4V regulator. Remote collectors on this

PIN FUNCTIONS

transistor conduct current and lock out the switch for input voltages below about 2.5V. No hysteresis is used to maximize the useful range of input voltage. The typical input voltage used is a 3.3V or 5V logic supply.

Royer: This pin connects to the center-tapped primary of the Royer converter and is used in conjunction with the BAT pin in a floating-bulb configuration where bulb current is controlled by directly sensing Royer primary-side supply current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 60μA into the pin. If the CCFL regulator is not being used in a floating bulb configuration, the Royer and BAT pins should be tied together.

BAT: This pin connects to the battery voltage from which the CCFL Royer converter and LCD Contrast flyback converter operate. This voltage is typically higher than the V_{IN} supply voltage but can be equal or less than V_{IN}. However, the BAT voltage must be at least 2V greater than the internal 2.4V regulator. This pin is used in conjunction with the Royer pin for floating bulb configurations. This pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 60μA into the pin. The BAT and Royer pins monitor the voltage across an internal 0.1Ω top-side current sense resistor. A 0A to 1A Royer supply current translates into an input signal range of 0mV to 100mV for the current sense amplifier. This 0mV to 100mV signal range is converted to a 0μA to 500μA sink current at the CCFL VC pin to null against the source current provided by the bulb current programmer circuit. The BAT pin also connects to the top side of an internal clamp between the BAT and Bulb pins.

Bulb: This pin connects to the low side of an internal 7V threshold voltage comparator between the BAT and Bulb pins. This pin can be used to set a maximum threshold voltage level across the primary side of the Royer converter. This reduces the maximum output under start-up conditions or open bulb conditions, thereby easing transformer voltage rating requirements. The Bulb pin is connected to the junction of an external resistor divider network. The divider network connects from the center tap of the Royer transformer to the top side of the Royer inductor. A capacitor across the top of the divider network serves to filter out switching ripple and allows a time constant to be set for determining how quickly the comparator activates. When the comparator is activated, this transfers the Royer converter from current mode operation into voltage mode operation.

CCFL V_{SW}: This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch is guaranteed to provide a minimum of 1.25A. Fast switching times and high efficiency are obtained by using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state. The ratio of switch current to driver current is about 40:1.

LT1183

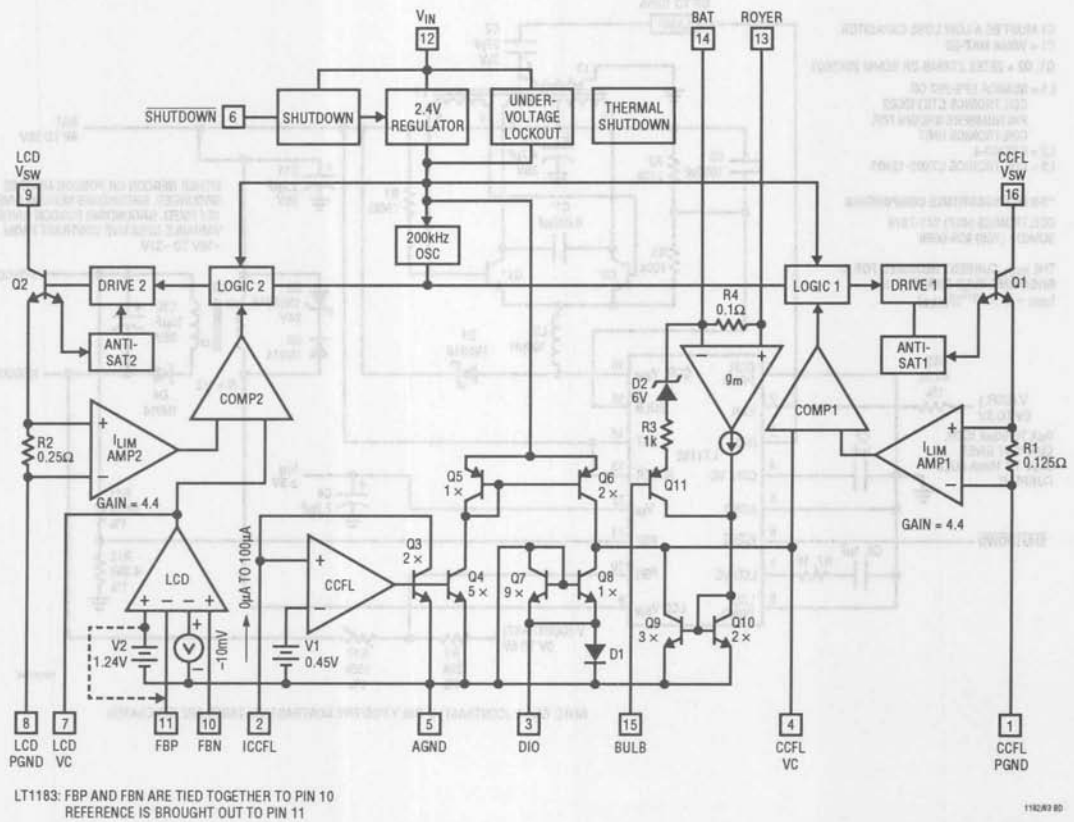
All functions and pins on the LT1183 are equivalent to the LT1182 with the exception of pins 10 and 11. On the LT1182, pin 10 is FBN and pin 11 is FBP. On the LT1183, pin 10 changes to FB and pin 11 changes to REF.

FB: This pin is the common connection between the noninverting terminal for the negative contrast control error amplifier and the inverting terminal for the positive contrast control error amplifier. In comparison to the LT1182, the FBN and the FBP pins have been internally tied together and brought out as one pin.

REF: This pin brings out the internal 1.24V reference and can be used for negative contrast control with an external resistor divider network. The REF pin has an output impedance of about 30Ω. The resistors in the divider network should be chosen to limit reference drive current to less than a few hundred microamps; otherwise reference regulation will be degraded. The REF pin may also be used to generate the maximum programming current for the ICCFL pin by placing a resistor between the pins. PWM or DAC control may then be used to subtract from the maximum programming current.

BLOCK DIAGRAM

LT1182/LT1183 CCFL/LCD Contrast Top Level Block Diagram



LT1183: FBP AND FBN ARE TIED TOGETHER TO PIN 10
REFERENCE IS BROUGHT OUT TO PIN 11

1182/83 BD

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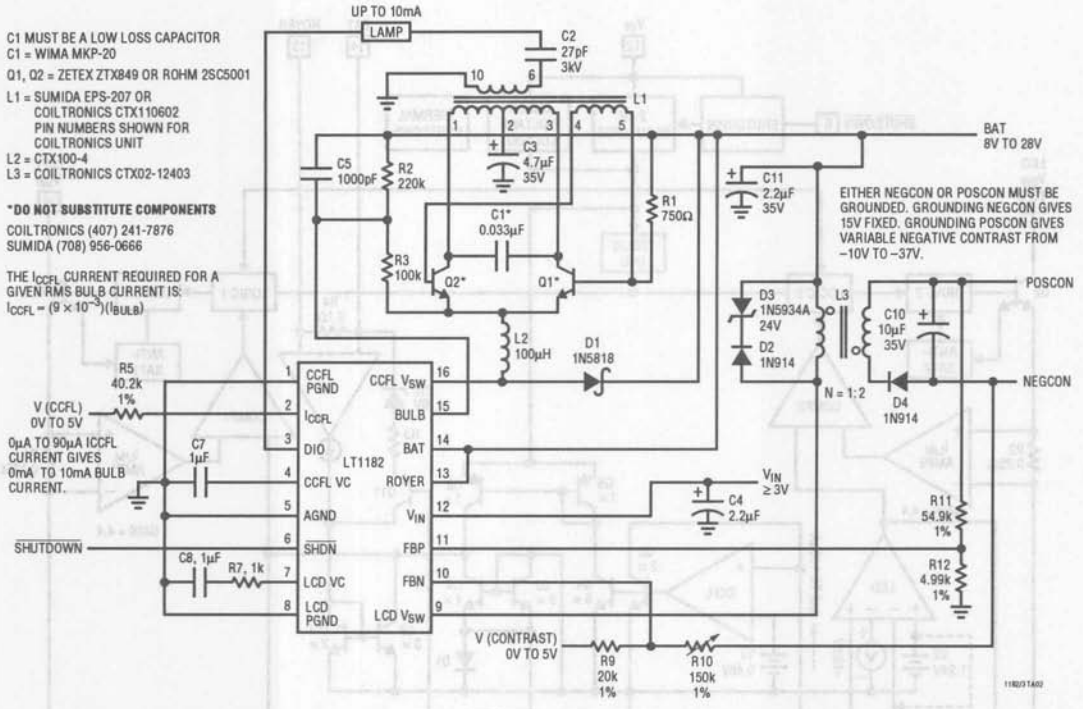
TYPICAL APPLICATION

90% Efficient Grounded CCFL configuration with Dual Polarity LCD Contrast



NOTE: GND V (CONTRAST) IF ONLY POSITIVE CONTRAST VOLTAGES ARE GENERATED.

12V, 30mA Flash Memory Programming Supply

April 1994

FEATURES

- Regulated 12V ±5% Output Voltage
- No Inductors
- Supply Voltage Range: 4.75V to 5.5V
- Guaranteed 30mA Output
- Low Power: I_{CC} = 500µA
- 0.5µA I_{CC} in Shutdown
- 8-Pin DIP or SO-8 Package
- Improved Second Source for the MAX662

APPLICATIONS

- 12V Flash Memory Programming Supplies
- Compact 12V Op Amp Supplies
- Battery-Powered Systems

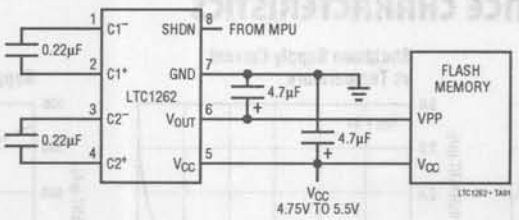
DESCRIPTION

The LTC1262 is a regulated 12V, 30mA output DC/DC converter. It is designed to provide the 12V ±5% output necessary to program byte-wide flash memories. The output will provide up to 30mA from input voltages as low as 4.75V without using any inductors. Only four external capacitors are required to complete an extremely small surface mountable circuit.

The TTL compatible shutdown pin can be directly connected to a microprocessor and reduces the supply current to less than 0.5µA. The LTC1262 is pin compatible with the MAX662 but requires fewer external capacitors and has 70 times lower power consumption in shutdown mode.

The LTC1262 is available in an 8-pin DIP or SO-8 package.

TYPICAL APPLICATION

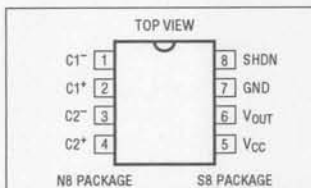


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{DD}) 6V
Input Voltage (SHDN) ..... −0.3V to V_{CC} + 0.3V
Output Current (I_{OUT}) 50mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC1262CN8 LTC1262CS8
S8 PART MARKING
1262

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.5V, T_A = 0°C to 70°C, (Notes 2, 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	0mA ≤ I_{OUT} ≤ 30mA, V_{SHDN} = 0V	●	11.4		12.6	V
I_{CC}	Supply Current	No Load, V_{SHDN} = 0V	●		0.5	1	mA
I_{SHDN}	Shutdown Supply Current	No Load, V_{SHDN} = V_{CC}	●		0.5	10	µA
f_{OSC}	Oscillator Frequency	V_{CC} = 5V, I_{OUT} = 30mA	●		300		kHz
	Power Efficiency	V_{CC} = 5V, I_{OUT} = 30mA	●		74		%
R_{SW}	V_{CC} to V_{OUT} Switch Impedance	V_{CC} = V_{SHDN} = 5V, I_{OUT} = 0mA	●		0.18	2	kΩ
V_{IH}	SHDN Input High Voltage		●	2.4			V
V_{IL}	SHDN Input Low Voltage		●			0.8	V
	SHDN Input Current	V_{CC} = 5V, V_{SHDN} = 0V V_{CC} = 5V, V_{SHDN} = 5V	● ●	−15	−10 0.06	−5 10	µA µA
t_{ON}	Turn On-Time	C1 = C2 = 0.22µF, C_{IN} = C_{OUT} = 4.7µF, (Figures 1, 2)				700	µs
t_{OFF}	Turn Off-Time	C1 = C2 = 0.22µF, C_{IN} = C_{OUT} = 4.7µF, (Figures 1, 2)				4	ms

The ● denotes specifications which apply over the full operating temperature range.

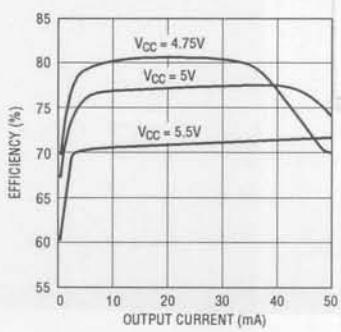
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

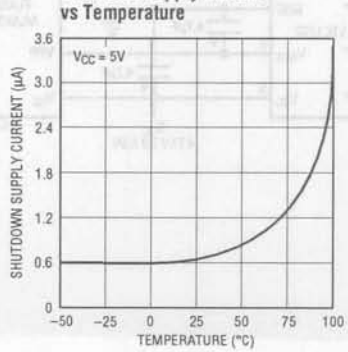
Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

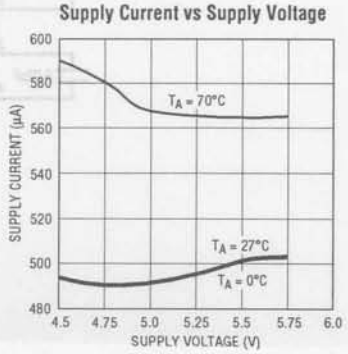
Efficiency vs Output Current



Shutdown Supply Current vs Temperature



Supply Current vs Supply Voltage



PIN FUNCTIONS

$C1^-$ (Pin 1): The First Commutating Capacitor Negative Input. Connect a 0.22µF capacitor (C1) between $C1^+$ and $C1^-$.

$C1^+$ (Pin 2): The First Commutating Capacitor Positive Input. Connect a 0.22µF capacitor (C1) between $C1^+$ and $C1^-$.

$C2^-$ (Pin 3): The Second Commutating Capacitor Negative Input. Connect a 0.22µF capacitor (C2) between $C2^+$ and $C2^-$.

$C2^+$ (Pin 4): The Second Commutating Capacitor Positive Input. Connect a 0.22µF capacitor (C2) between $C2^+$ and $C2^-$.

V_{CC} (Pin 5): The Positive Supply Input Where $4.75V \leq V_{CC} \leq 5.5V$. Connect a 4.7µF bypass capacitor to ground (C_{IN}).

V_{OUT} (Pin 6): The 12V Output. Connect a 4.7µF bypass capacitor to ground (C_{OUT}). When in the shutdown mode $V_{OUT} = V_{CC}$

GND (Pin 7): Ground.

SHDN (Pin 8): Active High TTL Logic Level Shutdown Pin. SHDN is internally pulled up to V_{CC}. Connect to GND for normal operation. In shutdown mode the charge pump is turned off and $V_{OUT} = V_{CC}$.

TIMING DIAGRAMS

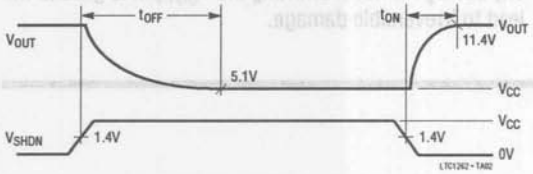


Figure 1. LTC1262 Timing Diagram

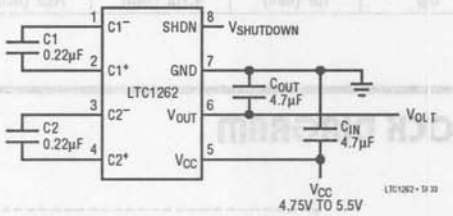


Figure 2. LTC1262 Timing Circuit

APPLICATIONS INFORMATION

Operation

The LTC1262 uses a tripler charge pump to generate 12V from a V_{CC} of 5V. The charge pump operates when clocked by a 300kHz oscillator. When the oscillator output is low, C1 and C2 are connected between V_{CC} and GND, charging them to V_{CC}. When the oscillator output goes high, C1 and C2 are stacked in series with the bottom plate of C1 pulled to V_{CC}. The top plate of C2 is switched to charge C_{OUT} and V_{OUT} rises. V_{OUT} is regulated to within 5% of 12V by an oscillator pulse gating scheme. A resistor divider senses V_{OUT}. When the output of the divider (V_{DIV}) is less than the output of a bandgap (V_{BGAP}) by the hysteresis voltage (V_{HYST}) of the comparator, oscillator pulses are applied to the charge pump to raise V_{OUT}. When V_{DIV} is above V_{BGAP} by V_{HYST}, the oscillator pulses are prevented from clocking the charge pump. V_{OUT} drops until V_{DIV} is below V_{BGAP} by V_{HYST} again. The gates of all internal switches are driven between V_{OUT} and GND. An internal diode ensures that the LTC1262 will start up under load by charging C_{OUT} to one diode drop below V_{CC}.

To reduce supply current the LTC1262 may be put into shutdown mode by floating the SHDN pin or taking it to V_{CC}. In this mode the bandgap, comparator, oscillator and resistor divider are switched off to reduce supply current to 0.5µA (Typ). At the same time an internal switch shorts V_{OUT} to V_{CC}, V_{OUT} takes about 4ms (Typ) to reach 5.1V

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APPLICATIONS INFORMATION

(see t_{OFF} in Figure 1). When the SHDN pin is grounded, the LTC1262 exits shutdown and the charge pump operates to raise V_{OUT} to 12V. V_{OUT} takes 650µs (Typ) to reach the lower regulation limit of 11.4V (see t_{ON} in Figure 1).

Choice of Capacitors

The LTC1262 is tested with the capacitors shown in Figure 2. C1 and C2 are 0.22µF ceramic capacitors and C_{IN} and C_{OUT} are 4.7µF tantalum capacitors. Refer to Table 1 if other choices are desired.

Table 1. Recommended Capacitor Types and Values

CAPACITOR	CERAMIC	TANTALUM	ALUMINUM
C1, C2	0.22µF to 1µF	Not Recommended	Not Recommended
C_{OUT}	2µF (Min)	4.7µF (Min)	10µF (Min)
C_{IN}	1µF (Min)	4.7µF (Min)	10µF (Min)

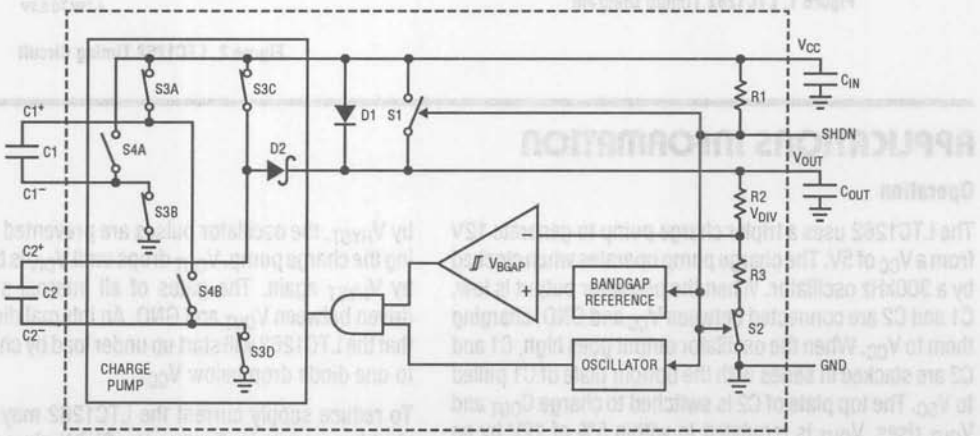
C1 and C2 should be ceramic capacitors with values in the range of 0.22µF to 1µF. Higher values provide better load regulation. Tantalum capacitors are not recommended as the higher ESR of these capacitors degrades performance at V_{CC} = 4.75V and load current above 25mA.

C_{IN} and C_{OUT} can be ceramic, tantalum or electrolytic capacitors. The ESR of C_{OUT} introduces steps in the V_{OUT} waveform whenever the charge pump charges C_{OUT}. This tends to increase V_{OUT} ripple. Ceramic or tantalum capacitors are recommended for C_{OUT} if minimum ripple is desired. The LTC1262 does not require a 0.1µF capacitor between V_{CC} and V_{OUT} for stability.

Maximum Load Current

The LTC1262 will source up to 50mA continuously without any damage to itself. Shorting the V_{OUT} pin to ground will lead to irreversible damage.

BLOCK DIAGRAM



S1 AND S2 SHOWN WITH SHDN PIN LOW.
S3A, S3B, S3C, S3D, S4A AND S4B SHOWN WITH OSCILLATOR OUTPUT LOW AND $V_{DIV} < V_{BGAP} - V_{HYST}$.
COMPARATOR HYSTERISIS IS $\pm V_{HYST}$.

LTC1285/LTC1288

3V Micropower 12-Bit A/D Converters in SO-8 Packages

April 1994

FEATURES

- 12-Bit Resolution
- 8-Pin SOIC Plastic Package
- Low Cost
- Low Supply Current: 160µA Typical
- Guaranteed ±3/4LSB Max DNL
- Auto-Shutdown to 1nA Typ
- Single Supply 3V to 6V Operation
- On-Chip Sample-and-Hold
- 100µs Conversion Time
- Sampling Rates: 7.5ksps (LTC1285)
  6.6ksps (LTC1288)
- I/O Compatible with SPI, Microwire, etc.
- Differential Inputs (LTC1285)
- 2-Channel MUX (LTC1288)

APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Pen Screen Digitizers
- Temperature Measurement
- Isolated Data Acquisition

DESCRIPTION

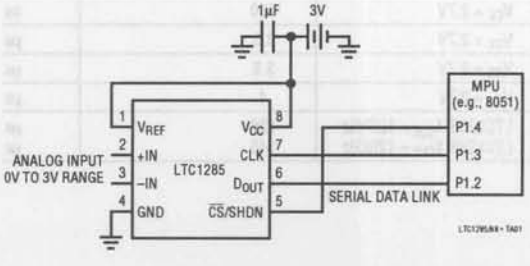
The LTC1285/LTC1288 are 3V micropower, 12-bit, sampling A/D converters. They typically draw only 160µA of supply current when converting and automatically power down to a typical supply current of 1nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on a 3V supply. These 12-bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1285 has a single differential analog input. The LTC1288 offers a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

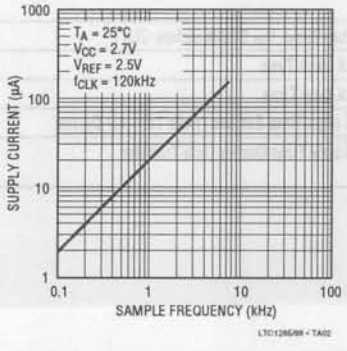
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATION

12µW, SO-8 Package, 12-Bit ADC
Samples at 200Hz and Runs Off a 3V Battery



Supply Current vs Sample Rate



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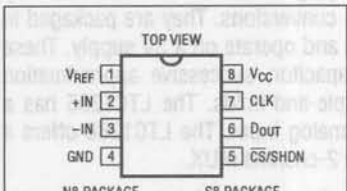
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
- Analog Reference ..... −0.3V to V_{CC} + 0.3V
- Digital Inputs ..... −0.3V to 12V
- Digital Output ..... −0.3V to V_{CC} + 0.3V

Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

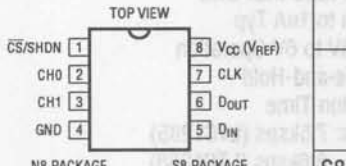
PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S)

ORDER PART NUMBER
LTC1285CN8 LTC1285CS8
S8 PART MARKING
1285



N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S)

ORDER PART NUMBER
LTC1288CN8 LTC1288CS8
S8 PART MARKING
1288

Consult factory for Industrial and Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	LTC1285 LTC1288	2.7 2.7		6 6	V V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	(Note 3)		120	kHz
t_{CYC}	Total Cycle Time	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	133.3 150.0			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	LTC1285, V_{CC} = 2.7V LTC1288, V_{CC} = 2.7V	5 5			µs µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	3.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	3.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 2.7V	4			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	128 145			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS		LTC1285 MIN	LTC1285 TYP	LTC1285 MAX	LTC1288 MIN	LTC1288 TYP	LTC1288 MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 5)	●			±2			±2	LSB
Differential Linearity Error		●			±3/4			±3/4	LSB
Offset Error		●			±3			±3	LSB
Gain Error		●			±8			±8	LSB
REF Input Range (LTC1285)	(Notes 6, 7)			1.5V to V_{CC} + 0.05V					V
Analog Input Range	(Note 6)			−0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 8)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA	●	2.4	2.64		V
		V_{CC} = 2.7V, I_O = 360µA	●	2.1	2.30		V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			15		mA
R_{REF}	Reference Input Resistance (LTC1285)	$\overline{CS}$ = V_{IH}			2700		MΩ
		$\overline{CS}$ = V_{IL}			54		kΩ
I_{REF}	Reference Current (LTC1285)	$\overline{CS}$ = V_{CC}	●		0.001	2.5	µA
		t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz			50		µA
		t_{CYC} = 134µs, f_{CLK} = 120kHz	●		50	70	µA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}	●		0.001	±3	µA
		LTC1285, t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz			150		µA
		LTC1285, t_{CYC} = 134µs, f_{CLK} = 120kHz	●		160	320	µA
		LTC1288, t_{CYC} ≥ 720µs, f_{CLK} ≤ 25kHz			200		µA
		LTC1288, t_{CYC} = 150µs, f_{CLK} = 120kHz	●		210	390	µA

DYNAMIC ACCURACY f_{SMPL} = 7.5kHz (LTC1285), f_{SMPL} = 6.6kHz (LTC1288) (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N +D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		72		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−80		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		80		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−80		dB

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AC CHARACTERISTICS (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	660	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
C_{IN}	Input Capacitance	Analog Inputs, On Channel			20		pF
		Analog Inputs, Off Channel			5		pF
		Digital Input			5		pF

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 75kHz$ at 70°C and $f_{CLK} \geq 1kHz$ at 25°C.

Note 4: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 120kHz unless otherwise specified.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This specification allows 50mV forward bias of either diode for $2.7V \leq V_{CC} \leq 6V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 3V input voltage range will therefore require a minimum supply voltage of 2.950V over initial tolerance, temperature variations and loading.

Note 7: Recommended operating condition.

Note 8: Channel leakage current is measured after the channel selection.

PIN FUNCTIONS

LTC1285

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN^+ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN^- (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$/SHDN (Pin 5): Chip Select Input. A logic low on this input enables the LTC1285. A logic high on this input disables the LTC1285 and disconnects the power to LTC1285.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

PIN FUNCTIONS

LTC1288

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1288. A logic high on this input disables the LTC1288 and disconnects the power to LTC1288.

CH0 (Pin 2): Analog Input. This input must be free of noise with respect to GND.

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

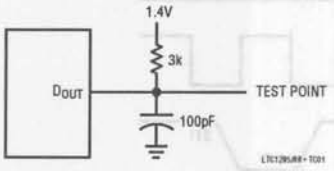
D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

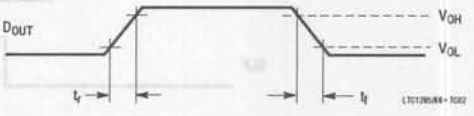
V_{CC}(V_{REF})(Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

TEST CIRCUITS

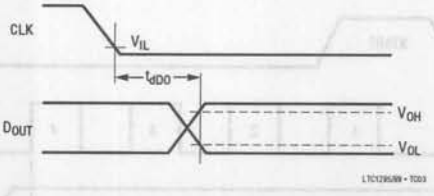
Load Circuit for t_{dDO}, t_r and t_f



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



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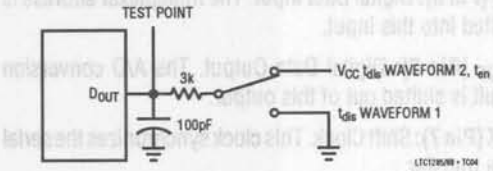
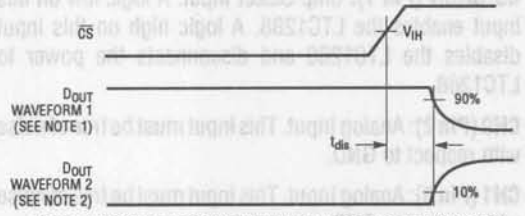
TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



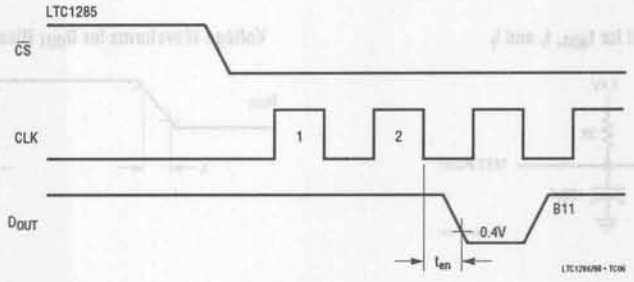
Voltage Waveforms for t_{dis}

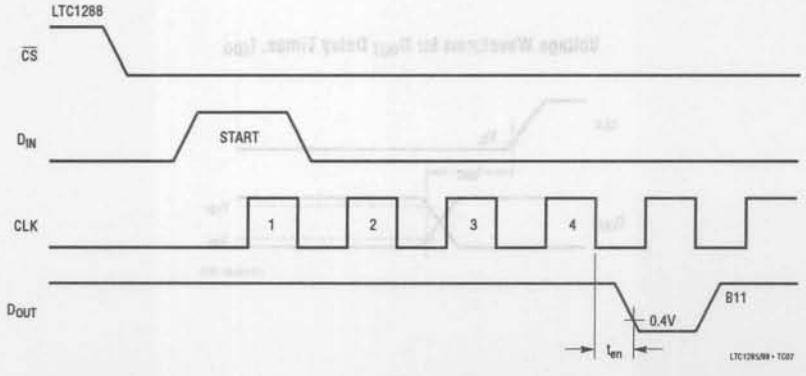


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

Voltage Waveforms for t_{en}

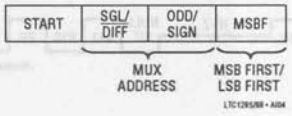




APPLICATIONS INFORMATION

INPUT DATA WORD (LTC1288 ONLY)

The LTC1288 four-bit data word is clocked into the D_{IN} input on the rising edge of the clock after $\overline{CS}$ goes low and the Start bit has been recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the Start bit. The Start bit initiates the data transfer and all leading zeros which precede this logical one will be ignored. After the Start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

MUX Address

The bits of the input word following the Start bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND. Only the "+" inputs have sample-and-hold. Signals applied at the "–" inputs must not change more than the required accuracy during the conversion.

Multiplexer Channel Selection

MUX ADDRESS		CHANNEL #		
SGL/$\overline{DIFF}$	ODD/SIGN	CH0	CH1	GND
1	0	+		–
1	1		+	–
0	0	+	–	
0	1	–	+	

MSB-FIRST/LSB-FIRST (MSBF)

The output data of the LTC1288 is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB-first data on the D_{OUT} line (see Operating Sequence).

ANALOG CONSIDERATIONS

Grounding

The LTC1285/LTC1288 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a printed circuit board. The ground pin (pin 4) should be tied directly to the ground plane with minimum lead length.

Bypassing

For good performance the LTC1285 V_{CC} and V_{REF} pins or the LTC1288 V_{CC} pin must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC}/V_{REF} pin directly to the analog ground plane with a minimum of 0.1µF capacitor and with leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1285/LTC1288 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. But if large source resistances are used, or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

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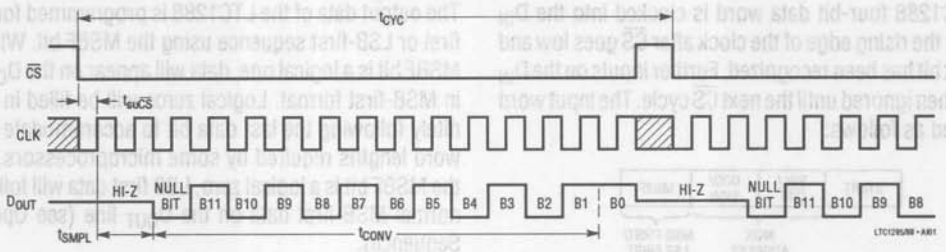
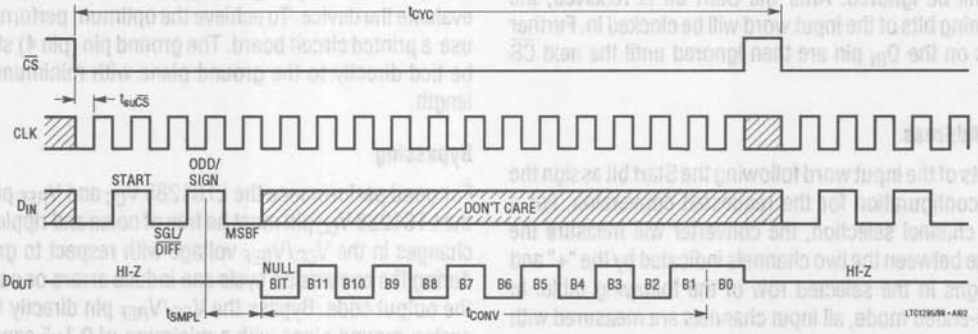
APPLICATIONS INFORMATION

LTC1285 Operating Sequence

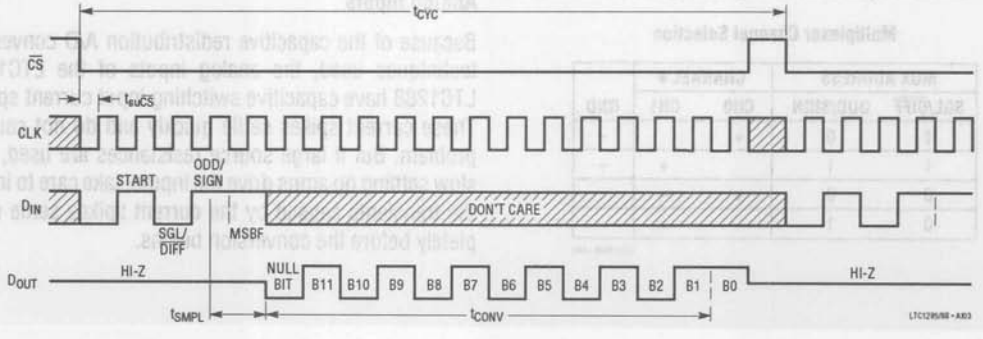


LTC1288 Operating Sequence
Example: Differential Inputs (CH^+, CH^-)

MSB-First Data (MSBF = 0)



MSB-First Data (MSBF = 1)



Micropower High Output Current Step-Up Adjustable and Fixed 5V DC/DC Converter

May 1994

FEATURES

- **5V at 600mA or 12V at 120mA from 2-Cell Supply**
- **200μA Quiescent Current**
- Logic Controlled Shutdown to 15μA
- Low V_{CESAT} Switch: 310mV at 2A Typical
- Burst Mode™ Operation at Light Load
- Current Mode Operation for Excellent Line and Load Transient Response
- Available in 8-Lead SO or DIP
- **Operates with Supply Voltage as Low as 2V**

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Personal Digital Assistants
- Cellular Telephones
- Flash Memory

DESCRIPTION

The LT1302/LT1302-5 are micropower step-up DC/DC converters that maintain high efficiency over a wide range of output current. They operate from a supply voltage as low as 2V and feature automatic shifting between Burst Mode operation at light load, and current mode operation at heavy load.

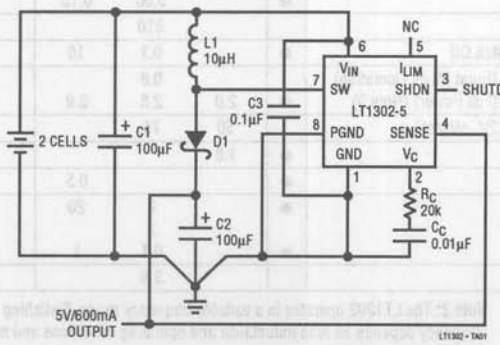
The internal low-loss NPN power switch can handle current in excess of 2A and switch at frequencies up to 400kHz. Quiescent current is just 200μA and can be further reduced to 15μA in shutdown.

Available in 8-pin DIP or 8-pin SOIC packaging, the LT1302/LT1302-5 have the highest switch current rating of any similarly packaged switching regulators presently on the market.

Burst Mode is a trademark of Linear Technology Corporation

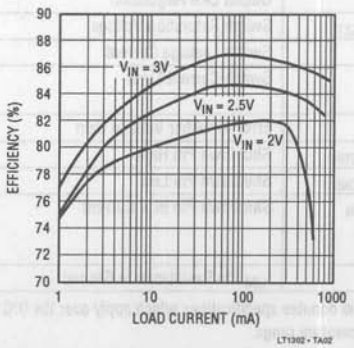
TYPICAL APPLICATION

2-Cell to 5V/600mA DC/DC Converter



C1 = C2 = SANYO OS-CON D1 = MOTOROLA MBRS130LT3
L1 = COILTRONICS CTX10-3
COILCRAFT DO3316-103

2-Cell to 5V Converter Efficiency

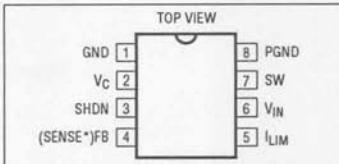


13

ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 25V
FB Voltage 10V
Shutdown Voltage 10V
V_C Voltage 4V
I_{LIM} Voltage 0.5V
Maximum Power Dissipation 700mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

*FIXED VERSION

PINS 1 AND 8 ARE INTERNALLY CONNECTED IN SOIC PACKAGE

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 60°C/W (S)

ORDER PART NUMBER
LT1302CN8
LT1302CS8
LT1302CN8-5
LT1302CS8-5

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{FB} = 1.3V	●		200	300	µA
		V_{SHDN} = 1.8V	●		15	25	µA
V_{IN}	Input Voltage Range			2.0			V
			●	2.2		8	V
V_{FB}	Feedback Voltage (LT1302)	V_C = 0.4V	●	1.22	1.24	1.26	V
	Feedback Pin Bias Current (LT1302)	V_{FB} = 1V			100		nA
	Output Sense Voltage (LT1302-5)	V_C = 0.4V	●	4.85	5.05	5.25	V
	Output Ripple Voltage (LT1302-5)				20		mV
	Sense Pin Resistance to Ground (LT1302-5)				420		kΩ
V_{OS}	Offset Voltage	See Block Diagram			15		mV
	Comparator Hysteresis	(Note 1)			5		mV
	Oscillator Frequency	Current Limit Not Asserted (Note 2)		175	220	265	kHz
	Oscillator TC				0.1		%/°C
DC	Maximum Duty Cycle			75	86	95	%
t_{ON}	Switch-On Time	Current Limit Not Asserted			3.9		µs
	Output Line Regulation	2 < V_{IN} < 8V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 2A			310		mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Switch Current Limit	V_{COMP} = 0.4V (Burst Mode Operation)			0.8		A
		V_{COMP} = 1.5V (Full Power) (Note 3)	●	2.0	2.8	3.9	A
	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.2V, $\Delta V_C/\Delta V_{FB}$		50	75		V/V
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low		●			0.5	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8	20	µA
		V_{SHDN} = 2V			3		µA
		V_{SHDN} = 0V	●		0.1	1	µA
	I_{LIM} Pin Resistance to Ground				3.9		kΩ

The ● denotes specifications which apply over the 0°C to 70°C temperature range.

Note 1: Hysteresis is specified at DC. Output ripple depends on capacitor size and ESR.

Note 2: The LT1302 operates in a variable frequency mode. Switching frequency depends on load inductance and operating conditions and may be above specified limits.

Note 3: Minimum switch current 100% tested. Maximum switch current guaranteed by design.

PIN FUNCTIONS

GND (Pin 1): Signal Ground. Feedback resistor and 0.1µF ceramic bypass capacitor from V_{IN} should be connected directly to this pin.

V_C (Pin 2): Frequency Compensation Pin. Connect series RC to GND.

SHDN (Pin 3): Shutdown. Pull high to effect shutdown; tie to ground for normal operation.

FB/Sense (Pin 4): Feedback/Sense. On LT1302 the pin connects to C1 input. On LT1302-5 the pin connects to the resistor string that sets output voltage to 5V.

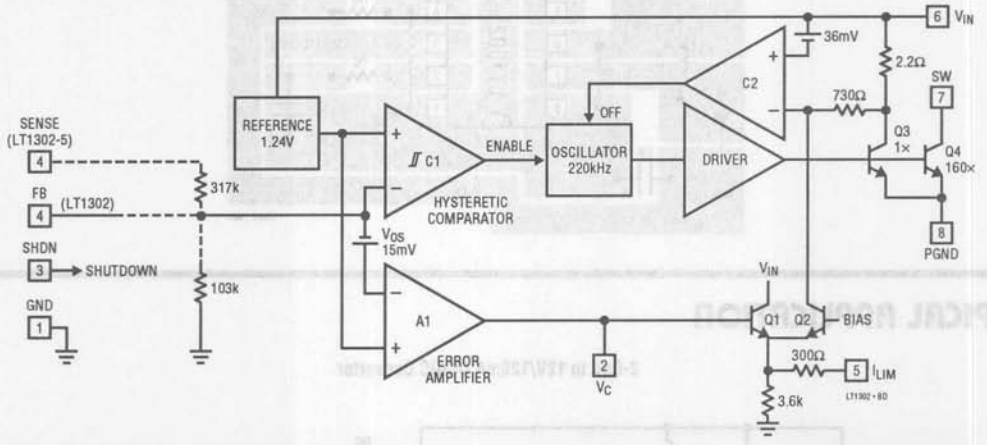
I_{LIM} (Pin 5): Normally left floating.

V_{IN} (Pin 6): Supply Pin. Must be bypassed with: 1) a 0.1µF ceramic to GND, and 2) a large value electrolytic to PGND.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct.

PGND (Pin 8): Power Ground. Pins 8 and 1 should be connected under the package. In the SOIC package, pins 1 and 8 are thermally connected to the die. One square inch of PCB copper provides an adequate heat sink for the device.

BLOCK DIAGRAM



OPERATION (Please refer to the Block Diagram)

The LT1302/LT1302-5 have two modes of operation. At light load the devices use Burst Mode operation to keep efficiency high. Hysteretic comparator C1 periodically enables the oscillator to regulate the output voltage. The switch current in this mode is limited to approximately 800mA. As the load is increased, a point is reached where output voltage cannot be maintained with Burst Mode operation. At this point, C1 switches on steady-state and output control is passed to the error amplifier A1. The peak switch current in Q4 is then regulated by the voltage on the V_C pin (A1's output). This current mode control results in good stability and immunity to input voltage variations. Current comparator C2 controls the oscillator on time. Off-time is affected but to a smaller degree. Switching frequency changes with input voltage, output voltage, inductance, and load variations and may be higher than data sheet limits.

Layout

High speed, high current switching mandate careful layout to achieve proper operation. Poor layout can result in unstable operation, particularly at higher switch

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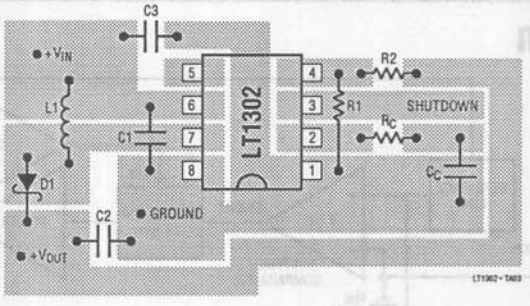
OPERATION (Please refer to the Block Diagram)

current levels. The LT1302/LT1302-5 pinout is arranged such that the high current functions are on one side of the package with sensitive control functions on the other.

Layout should follow the placement shown below. Be sure to bypass the LT1302/LT1302-5 with a 0.1µF ceramic capacitor right at the package. The input must also be bypassed with a large (100µF or more) electrolytic capacitor. Keep feedback resistors close to the FB pin. In some cases bypassing the FB pin with a 100pF capacitor to ground will aid stability.

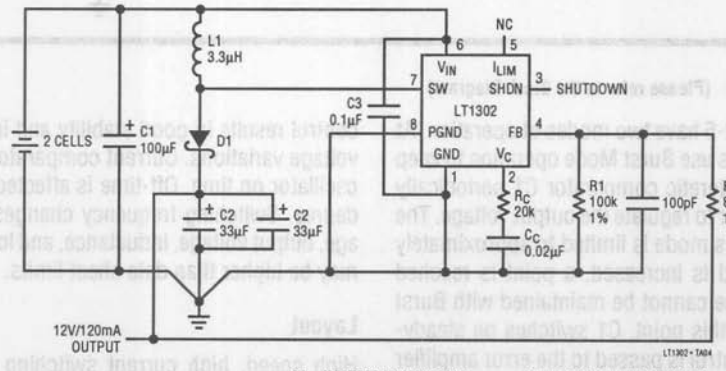
The output capacitor must have low enough ESR to prevent mode hopping. With a high ESR capacitor output voltage ripple can trip comparator C1 while in current mode, causing the device to jump between Burst Mode operation and current mode operation. ESR of 0.05Ω or less is recommended.

Recommended PC Component Placement



TYPICAL APPLICATION

2-Cell to 12V/120mA DC/DC Converter



C1 = AVX TPSD107M010R0100
C2 = AVX TPSD336M025R0200
D1 = MOTOROLA MBRS130LT3
L1 = COILCRAFT DO3316-332

Micropower High Efficiency DC/DC Converter with Low-Battery Detector Adjustable and Fixed 5V

April 1994

FEATURES

- 5V at 200mA from a 2V Input
- Supply Voltage As Low As 1.8V
- Up to 88% Efficiency
- 120μA Quiescent Current
- Low-Battery Detector
- Low V_{CESAT} Switch: 170mV at 1A Typ
- Uses Inexpensive Surface Mount Inductors
- 8-Lead DIP or SOIC Package

APPLICATIONS

- 2-Cell and 3-Cell to 5V Conversion
- Palmtop Computers
- Portable Instruments
- Bar-Code Scanners
- PDAs
- Wireless Systems

DESCRIPTION

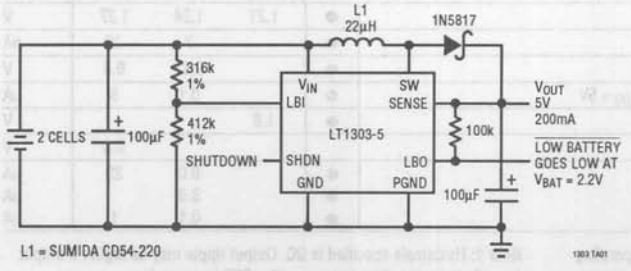
The LT1303/LT1303-5 are micropower step-up high efficiency DC/DC converters using Burst Mode™ operation. They are ideal for use in small, low-voltage battery-operated systems. The LT1303-5 accepts an input voltage between 1.8V and 5V and converts it to a regulated 5V. The LT1303 is an adjustable version that can supply an output voltage up to 25V. Quiescent current is only 120μA from the battery and the shutdown pin further reduces current to 10μA. The low-battery detector provides an open-collector output that goes low when the input voltage drops below a preset level. The on-chip NPN power switch has a low 170mV saturation voltage at a switch current of 1A. The LT1303/LT1303-5 are available in 8-lead DIP or SOIC packages, easing board space requirements.

For higher output current, please see the LT1302.

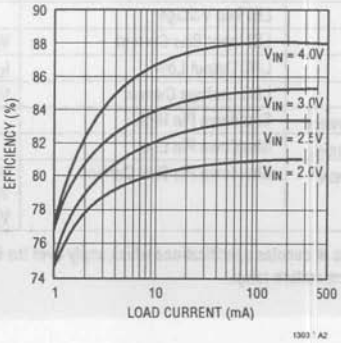
Burst Mode is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

2-Cell to 5V DC/DC Converter with Low-Battery Detect



5V Output Efficiency

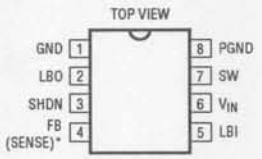


13

ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 25V
Sense Voltage (LT1303-5) 20V
FB Voltage (LT1303) 10V
Shutdown Voltage 10V
LBO Voltage 10V
LBI Voltage 10V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

*FIXED VERSION

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 100°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1303CN8 LT1303CS8 LT1303CN8-5 LT1303CS8-5
S8 PART MARKING
1303 13035

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{SEL} = 5V, V_{SENSE} = 5.5V	●		120	200	µA
		V_{SHDN} = 1.8V	●		7	15	µA
V_{IN}	Input Voltage Range			1.8	1.55		V
			●	2.0			V
	Feedback Voltage	LT1303	●	1.22	1.24	1.26	V
	Output Sense Voltage	LT1303-5	●	4.8	5.0	5.2	V
	Comparator Hysteresis	LT1303 (Note 1)	●		6	12.5	mV
	Output Hysteresis	LT1303-5 (Note 1)	●		22	50	mV
	Feedback Pin Bias Current	LT1303, V_{FB} = 1V	●		7	20	nA
	Oscillator Frequency	Current Limit Not Asserted		120	155	185	kHz
	Oscillator TC				0.2		%/°C
DC	Maximum Duty Cycle		●	75	86	95	%
t_{ON}	Switch On Time	Current Limit Not Asserted			5.6		µs
	Output Line Regulation	1.8V < V_{IN} < 6V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 700mA	●		130	200	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Peak Switch Current		●	0.75	1.0	1.25	A
	LBI Trip Voltage		●	1.21	1.24	1.27	V
	LBI Input Bias Current	V_{LBI} = 1.3V	●		7	20	nA
	LBO Output Low	I_{LOAD} = 100µA	●		0.11	0.4	V
	LBO Leakage Current	V_{LBI} = 1.3V, V_{LBO} = 5V	●		0.1	5	µA
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low					0.5	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8.0	20	µA
		V_{SHDN} = 2V	●		3.0		µA
		V_{SHDN} = 0V	●		0.1	1	µA

The ● denotes specifications which apply over the 0°C to 70°C operating temperature range.

Note 1: Hysteresis specified is DC. Output ripple may be higher if output capacitance is insufficient or capacitor ESR is excessive.

PIN FUNCTIONS

GND (Pin 1): Signal Ground. Tie to PGND under the package.

LBO (Pin 2): Open-Collector Output of Comparator C3. Can sink 100µA.

SHDN (Pin 3): Shutdown. Pull high to shut down the LT1303. Ground for normal operation.

FB/Sense (Pin 4): On 1303 (adjustable) this pin converts to main comparator C1 input. On 1303-5 this pin connects to the resistor string that sets output voltage at 5V.

LBI (Pin 5): Low-Battery Comparator Input. When voltage on this pin is below 1.24V, LBO is low.

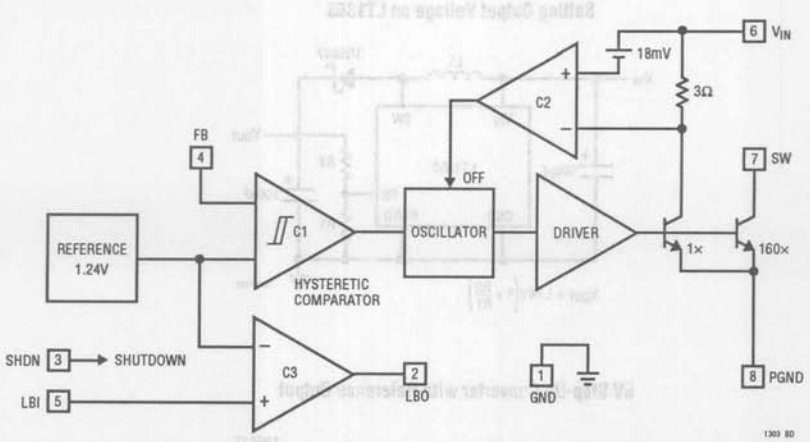
V_{IN} (PIN 6): Supply Pin. Must be bypassed with a large value electrolytic to gound. Keep bypass within 0.2" of the device.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct to minimize radio frequency interference.

PGND (Pin 8): Power Ground. Tie to signal ground (pin 1) under the package. Bypass capacitor from V_{IN} should be tied directly to PGND within 0.2" of the device.

BLOCK DIAGRAMS

LT1303 Block Diagram



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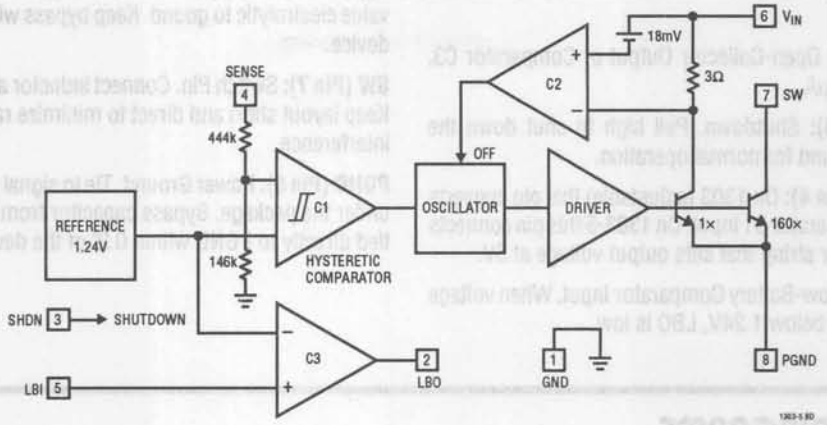
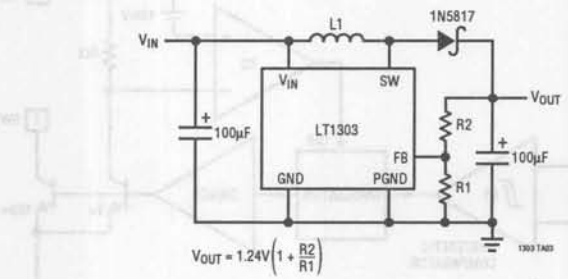
BLOCK DIAGRAMS

LT1303-5 Block Diagram

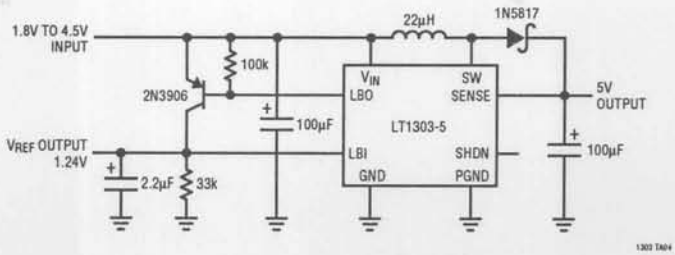


TYPICAL APPLICATIONS

Setting Output Voltage on LT1303



5V Step-Up Converter with Reference Output



500kHz Micropower DC/DC Converter for Flash Memory

April 1994

FEATURES

- **60mA Output Current at 12V from 3V or 5V Supply**
- **Shutdown to 6µA**
- $\overline{\text{VPP VALID}}$ Comparator
- **Up to 85% Efficiency**
- 500µA Quiescent Current
- V_{CESAT} Switch: 300mV at 0.5A Typical
- Soft Start Reduces Supply Current Transients
- Uses Low Value, Small Size, Surface Mount Inductors
- Available in 8-Lead SOIC Package

APPLICATIONS

- Flash Memory VPP Generator
- Type II and III PCMCIA Card DC/DC Converters
- 3V to 12V, 5V to 12V Converters
- Portable Computers and Instruments
- Cellular Telephones
- DC/DC Converter Module Replacements

DESCRIPTION

The LT1309 is a 500kHz micropower DC/DC converter for Flash Memory. The regulator features Burst Mode™ operation with a 0.5A, 300mV switch, enabling 85% efficiency at the fixed 12V output. High frequency operation permits the use of small value, and therefore small size, surface mount inductors and capacitors. The LT1309 comes in an 8-lead SOIC package allowing extremely compact PC board layouts. These features make the device attractive for PCMCIA cards, cellular phones, and other applications where board area is limited.

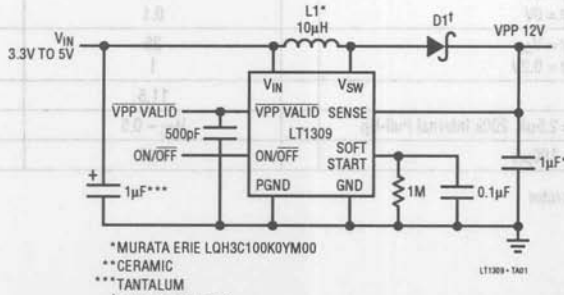
Quiescent current is 500µA that drops to 6µA when the part shuts down. The part includes a soft start feature which limits supply current transients during turn-on.

The LT1309 contains a $\overline{\text{VPP VALID}}$ comparator with a logic output that goes low when the output voltage is ready to program 12V Flash Memory. This comparator simplifies the interface to external control logic.

Burst Mode is a trademark of Linear Technology Corporation

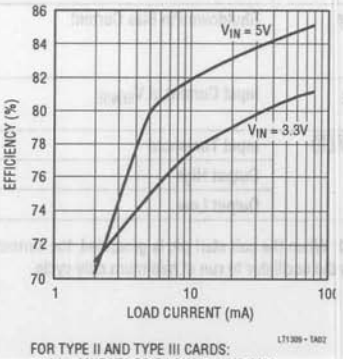
TYPICAL APPLICATION

12V, 60mA Flash Memory Programming Supply



*MURATA ERIE LQH3C100K0YM00
**CERAMIC
***TANTALUM
†PHILIPS PRLL5818

12V Output Efficiency



FOR TYPE II AND TYPE III CARDS:
L1 = MURATA ERIE LQH3C100K04M00
D1 = PHILIPS PRLL5818, 2.1mm MAXIMUM HEIGHT

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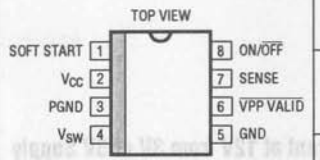
ABSOLUTE MAXIMUM RATINGS

V_{CC} Voltage 7V
V_{SW} Voltage 20V
V_{SENSE} Voltage 20V
$V_{ON/\overline{OFF}}$ Voltage 7V
V_{SEL} Voltage 7V
I_{LIM} Voltage 7V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1309CS8
S8 PART MARKING
1309

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	$V_{ON/\overline{OFF}}$ = 3V, V_{SEL} = 0.2V, Switch Off		500		µA
I_{SD}	Shutdown Mode Current	$V_{ON/\overline{OFF}}$ = 0.2V		6		µA
V_{CC}	Input Voltage Range		2		6	V
V_{SENSE}	Output Sense Voltage		11.5	12	12.5	V
	Output Referred Comparator Hysteresis	V_{SENSE} = 12V		35		mV
	Oscillator Frequency	Current Limit Not Asserted		500		kHz
DC	Maximum Duty Cycle			85		%
t_{ON}	Switch-On Time	Current Limit Not Asserted		1.7		µs
	Reference Line Regulation	2V < V_{IN} < 6V		0.06		%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 0.5A		300		mV
	Switch Leakage Current	V_{SW} = 12V, Switch Off		1		µA
	Peak Switch Current	Soft Start Floating Soft Start Grounded		0.5 0		A A
I_{START}	Soft Start Current	Soft Start Grounded		50		µA
$V_{ON/\overline{OFF}}$	Shutdown Pin Threshold			1.5		V
$I_{ON/\overline{OFF}}$	Shutdown Pin Bias Current	$V_{ON/\overline{OFF}}$ = 5V $V_{ON/\overline{OFF}}$ = 3V $V_{ON/\overline{OFF}}$ = 0V		20 9 0.1		µA µA µA
I_{SENSE}	Input Current at V_{SENSE}	$V_{ON/\overline{OFF}}$ = V_{CC} $V_{ON/\overline{OFF}}$ = 0.2V		25 1		µA µA
$\overline{VPPVALID}$	Input Threshold			11.5		V
	Output High	I_{LOAD} = 2.5µA, 200k Internal Pull-Up		V_{CC} – 0.5		V
	Output Low	I_{LOAD} = 100µA		0.13		V

Note 1: When the soft start pin is grounded, the current limit comparator forces the oscillator to run at minimum duty cycle.

PIN FUNCTIONS

Soft Start (Pin 1): Sets Peak Switch Current. Float this pin for normal 0.5A peak switch current. Tie this pin to GND through a resistor greater than 1k to limit the switch current from 0.125A to 0.5A. Connecting a capacitor from soft start to GND reduces switch current during start-up. The current limit with the soft start pin at 0V is about 0A which increases as the external capacitor charges from 0V to 1V. Select the capacitance for a given soft start duration. About 50μA flows from the soft start pin to ground.

V_{CC} (Pin 2): Input Supply. This pin should be decoupled close to the package with at least 1μF of low ESR input capacitance connected to GND (pin 5).

PGND (Pin 3): Power Ground. Large currents flow in this pin so it is highly recommended to make the PC board traces to the common ground plane as wide as possible.

V_{SW} (Pin 4): Collector of the Internal Power Switch. Large currents with fast edges flow through this pin. To reduce radiated noise, minimize the PCB trace area connected to this pin. Also minimize the distance to the inductor to decrease ohmic losses which degrade efficiency.

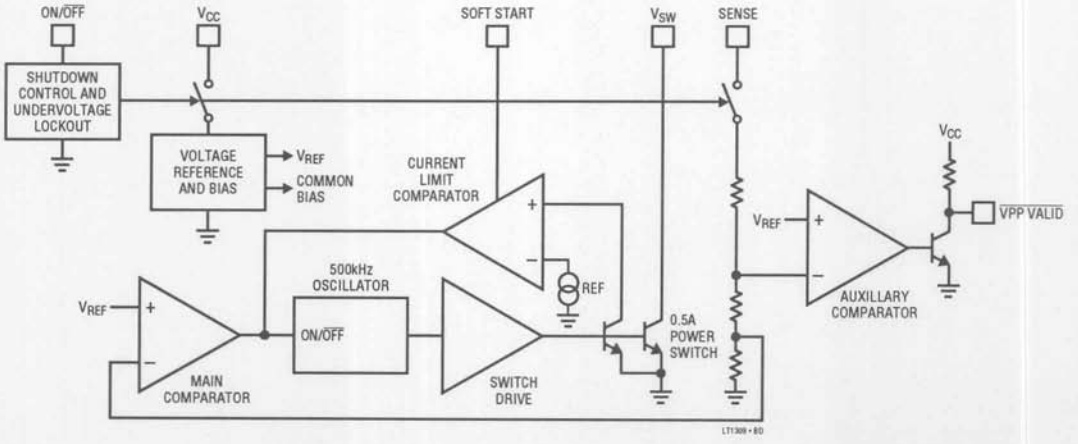
GND (Pin 5): Clean Analog Ground. V_{CC} should be decoupled to this point.

$\overline{\text{VPP VALID}}$ (Pin 6): $\overline{\text{VPP VALID}}$ Comparator Output. This output signals a logic low when the voltage at the sense pin is greater than 11.5V. In shutdown mode this pin is pulled up to the supply through a 200k resistor.

Sense (Pin 7): Output Feedback Sense Pin. This pin connects to an internal resistive divider that sets the output voltage.

ON/$\overline{\text{OFF}}$ (Pin 8): Shutdown Control. When pulled below 1.5V, this pin disables the LT1309-12 to a micropower off state (6μA). The part is fully operational when ON/$\overline{\text{OFF}}$ is greater than 1.5V.

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The LT1309 is a micropower, step-up, Burst Mode DC/DC converter. The device is intended for applications that demand the highest efficiency in the smallest amount of circuit board area. The device's 500kHz oscillator enables the use of small value and therefore small size inductors and capacitors.

In Burst Mode operation, a current limit comparator monitors switch current and establishes an upper limit by controlling the switch-on time. Current limit can be adjusted from 0% to 100% of its rated value by loading the soft start pin with a resistor. Connecting a 0.1µF capacitor to this pin momentarily forces the current limit to zero at device turn-on which reduces supply current transients.

The LT1309's shutdown control can be used to disable the device. When turned off, supply current drops to 6µA and the input current into the sense pin drops to zero.

Single PCMCIA VPP Driver/Regulator

May 1994

FEATURES

- **Digital Selection of 0V, V_{CC}, 12V or Hi-Z**
- Automatic Switching from 3.3V to 5V
- **120mA Output Current Capability**
- **Internal Current Limiting and Thermal Shutdown**
- Powered from Unregulated 13V to 20V Supply
- Logic Compatible with Standard PCMCIA Controllers
- 1µF Output Capacitor
- 30µA Quiescent Current in Hi-Z or 0V Mode
- VPP Valid Status Feedback Signal
- No VPP Overshoot

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers
- Flash Memory Programming

DESCRIPTION

The LT1312 provides 0V, 3.3V, 5V, 12V and Hi-Z regulated power to the VPP pin of a PCMCIA card slot from a single unregulated 13V to 20V supply. When used in conjunction with a PC card interface controller, the LT1312 forms a complete minimum component-count interface for palmtop, pen-based and notebook computers. The VPP output voltage is selected by two logic compatible digital inputs which interface directly with industry standard PC card interface controllers.

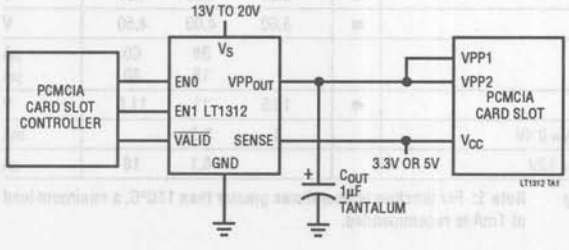
Automatic 3.3V to 5V switching is provided by an internal comparator which continuously monitors the PC card V_{CC} supply and automatically adjusts the regulated VPP output to match V_{CC} when the VPP = V_{CC} mode is selected.

An open-collector VPP $\overline{\text{VALID}}$ output is driven low when VPP is in regulation at 12V.

The LT1312 is available in both 8-pin DIP and 8-pin SOIC packaging.

TYPICAL APPLICATION

Typical PCMCIA Single Slot VPP Driver



LT1312 Truth Table

EN0	EN1	SENSE	VPP_{OUT}	$\overline{\text{VALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V to 3.6V	3.3V	1
0	1	4.5V to 5.5V	5V	1
1	1	X	HI-Z	1

X = Don't care

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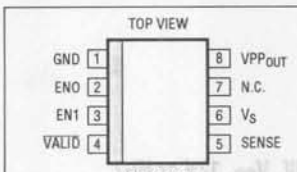
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Digital Input Voltage ..... 7V to (GND – 0.3V)
Sense Input Voltage ..... 7V to (GND – 0.3V)
Valid Output Voltage ..... 15V to (GND – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Operating Temperature ..... 0°C to 70°C
Junction Temperature ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1312CS8
S8 PART MARKING
1312

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 13V to 20V, T_A = 25°C, unless otherwise noted.

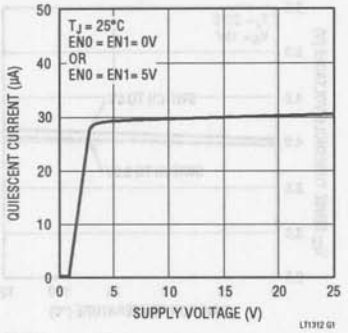
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VPP_{OUT}	Output Voltage	Program to 12V, $I_{OUT} \le 120mA$ (Note 1)	●	11.52	12.00	12.48	V
		Program to 5V, $I_{OUT} \le 30mA$ (Note 1)	●	4.75	5.00	5.25	V
		Program to 3.3V, $I_{OUT} \le 30mA$ (Note 1)	●	3.135	3.30	3.465	V
		Program to 0V, $I_{OUT} = -300\mu A$			0.42	0.60	V
I_{LKG}	Output Leakage	Program to Hi-Z, $0V \le VPP_{OUT} \le 12V$	●	-10		10	µA
I_S	Supply Current	Program to 0V	●		30	50	µA
		Program to Hi-Z	●		30	50	µA
		Program to 12V, No Load	●		230	360	µA
		Program to 5V, No Load	●		75	120	µA
		Program to 3.3V, No Load	●		55	90	µA
		Program to 12V, I_{OUT} = 120mA	●		126	132	mA
		Program to 5V, I_{OUT} = 30mA	●		31	33	mA
		Program to 3.3V, I_{OUT} = 30mA	●		31	33	mA
I_{LIM}	Current Limit	Program to 3.3V, 5V or 12V			330	500	mA
V_{ENH}	Enable Input High Voltage		●	2.4			V
V_{ENL}	Enable Input Low Voltage		●			0.4	V
I_{ENH}	Enable Input High Current	$2.4V \le V_{IN} \le 5.5V$			20	50	µA
I_{ENL}	Enable Input Low Current	$0V \le V_{IN} \le 0.4V$			0.01	1	µA
V_{SEN5}	V_{CC} Sense Threshold	VPP_{OUT} = 3.3V to 5V	●	3.60	4.05	4.50	V
V_{SEN3}	V_{CC} Sense Threshold	VPP_{OUT} = 5V to 3.3V	●	3.60	4.00	4.50	V
I_{SEN}	V_{CC} Sense Input Current	V_{SENSE} = 5V			38	60	µA
		V_{SENSE} = 3.3V			18	30	µA
$V_{\overline{VALID}\ TH}$	$VPP_{\overline{VALID}}$ Threshold Voltage	Program to 12V	●	10.5	11	11.5	V
$I_{\overline{VALID}}$	$VPP_{\overline{VALID}}$ Output Drive Current	Program to 12V, $V_{\overline{VALID}}$ = 0.4V		1	3.3		mA
	$VPP_{\overline{VALID}}$ Output Leakage Current	Program to 0V, $V_{\overline{VALID}}$ = 12V			0.1	10	µA

The ● denotes the specifications which apply over the full operating temperature range.

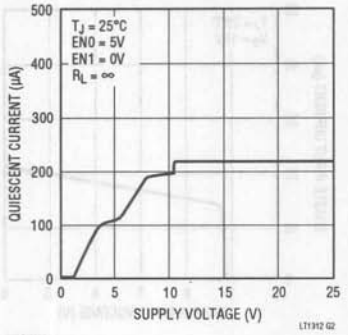
Note 1: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

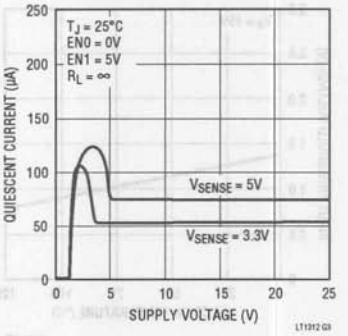
Quiescent Current (0V or Hi-Z Mode)



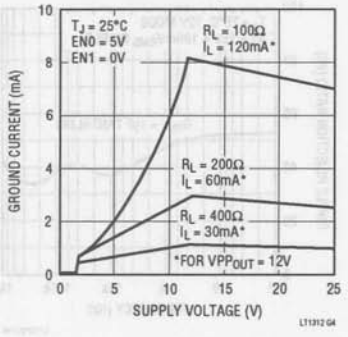
Quiescent Current (12V Mode)



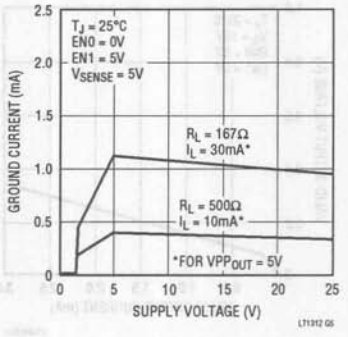
Quiescent Current (3.3V/5V Mode)



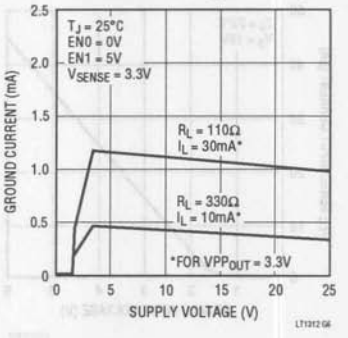
Ground Pin Current (12V Mode)



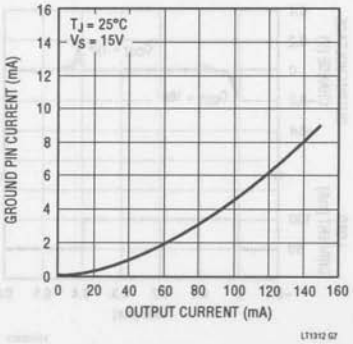
Ground Pin Current (5V Mode)



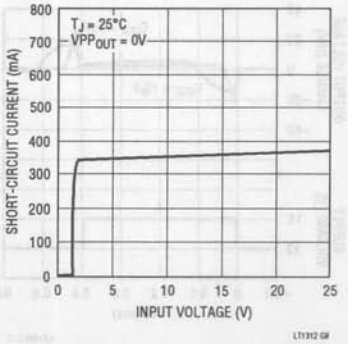
Ground Pin Current (3.3V Mode)



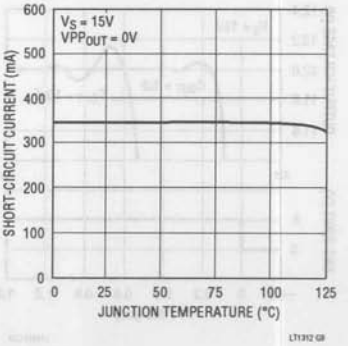
Ground Pin Current



Current Limit



Current Limit



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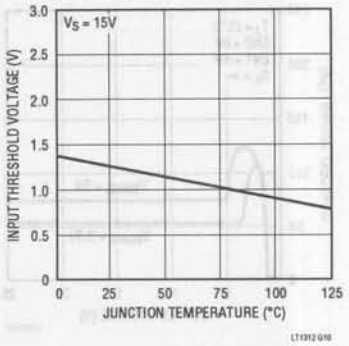
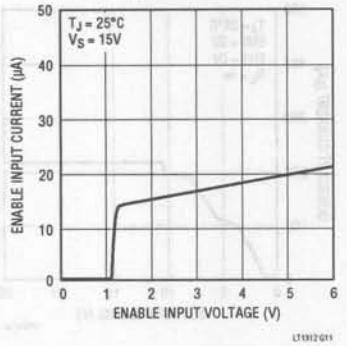
TYPICAL PERFORMANCE CHARACTERISTICS

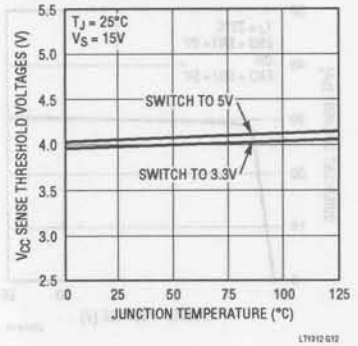
Enable Input Threshold Voltage



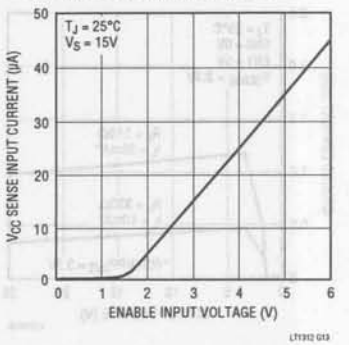
Enable Input Current



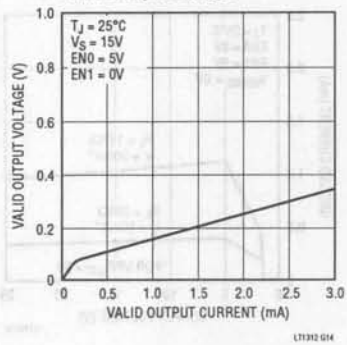
V_{CC} Sense Threshold Voltage



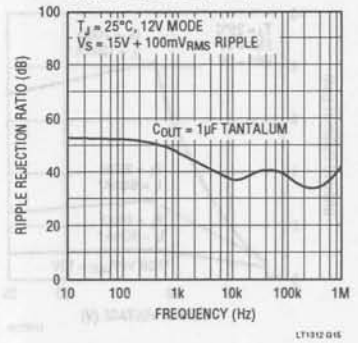
V_{CC} Sense Input Current



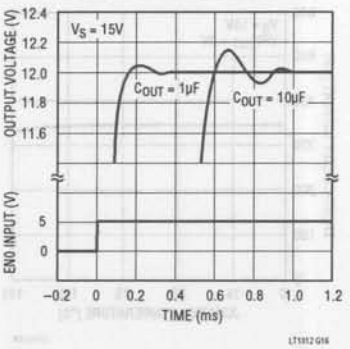
$\overline{VALID}$ Output Voltage



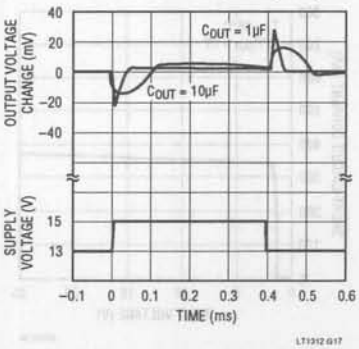
Ripple Rejection (12V)



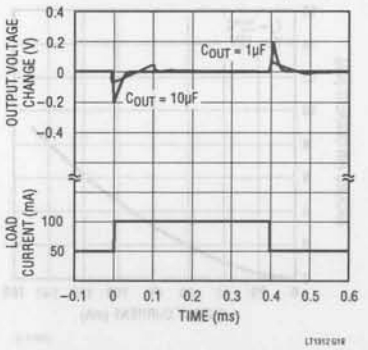
12V Turn-On Waveform



Line Transient Response (12V)



Load Transient Response (12V)



PIN FUNCTIONS

Supply Pin: Power is supplied to the device through the supply pin. The supply pin should be bypassed to ground if the device is more than 6 inches away from the main supply capacitor. A bypass capacitor in the range of 0.1µF to 1µF is sufficient. The supply voltage to the LT1312 can be loosely regulated between 13V and 20V. See Applications Information section for more detail.

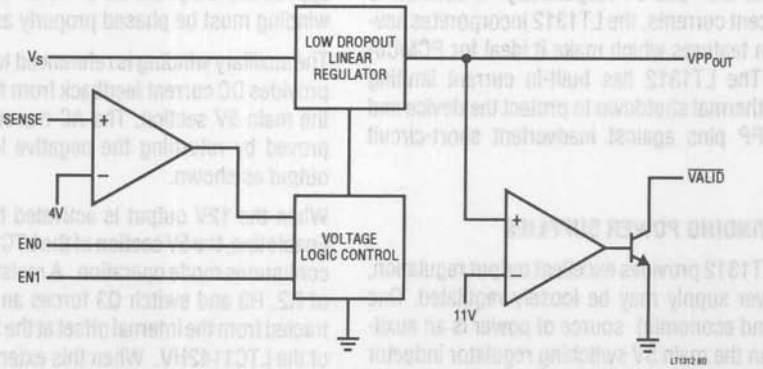
VPP_{OUT} Pin: This regulated output supplies power to the PCMCIA card VPP pins which are typically tied together at the card socket. The VPP_{OUT} output is current limited to approximately 330mA. Thermal shutdown provides a second level of protection. A 1µF to 10µF tantalum output capacitor is recommended. See Applications Information section for more detail on output capacitor considerations.

Input Enable Pins: The two digital input pins are high impedance inputs with approximately 20µA input current at 2.4V. The input thresholds are compatible with CMOS controllers and can be driven from either 5V or 3.3V CMOS logic. ESD protection diodes limit input excursions to 0.6V below ground.

$\overline{VALID}$ Output Pin: This pin is an open-collector NPN output which is driven low when the VPP_{OUT} pin is in regulation, i.e., when it is above 11V. An external 51k pull-up resistor is connected between this output and the same 5V or 3.3V logic supply powering the PCMCIA compatible control logic.

V_{CC} Sense Pin: A built-in comparator and 4V reference automatically switches the VPP_{OUT} from 5V to 3.3V depending upon the voltage sensed at the PCMCIA card socket V_{CC} pin. The input current for this pin is approximately 30µA. For 5V only operation, connect the Sense pin directly to ground. An ESD protection diode limits the input voltage to 0.6V below ground.

BLOCK DIAGRAM



OPERATION

The LT1312 is a programmable output voltage, low-dropout linear regulator designed specifically for PCMCIA VPP drive applications. Input power is typically obtained from a loosely regulated input supply between 13V and 20V (see Applications Information section for more detail on the input power supply). The LT1312 consists of the following blocks:

Low Dropout Voltage Linear Regulator: The heart of the LT1312 is a PNP-based low-dropout voltage regulator which drops the unregulated supply voltage from 13V to 20V down to 12V, 5V, 3.3V, 0V or Hi-Z depending upon the state of the two Enable inputs and the V_{CC} Sense input. The regulator has built-in current limiting and thermal shutdown to protect the device, the load, and the socket against inadvertent short circuiting to ground.

Voltage Control Logic: The LT1312 has five possible output modes: 0V, 3.3V, 5V, 12V and Hi-Z. These five modes are selected by the two Enable inputs and the V_{CC} Sense input as described by the Truth Table.

V_{CC} Sense Comparator: When the V_{CC} mode is selected, the LT1312 automatically adjusts the regulated VPP output voltage to 3.3V or 5V depending upon the voltage present at the PC card V_{CC} supply pin. The threshold voltage for the comparator is set at 4V and there is approximately 50mV of hysteresis provided to ensure clean switching between 3.3V and 5V.

VPP $\overline{\text{VALID}}$ Comparator: A voltage comparator monitors the output voltage when the 12V mode is selected and is driven low when the output is in regulation above 11V.

APPLICATIONS INFORMATION

The LT1312 is a voltage programmable linear regulator designed specifically for PCMCIA VPP driver applications. The device operates with very low quiescent current (30μA) in the 0V and Hi-Z modes of operation. In the Hi-Z mode, the output leakage current falls to 1μA. Unloaded quiescent current rises to only 55μA and 75μA when programmed to 3.3V and 5V respectively. In addition to the low quiescent currents, the LT1312 incorporates several protection features which make it ideal for PCMCIA applications. The LT1312 has built-in current limiting (330mA) and thermal shutdown to protect the device and the socket VPP pins against inadvertent short-circuit conditions.

AUXILIARY WINDING POWER SUPPLIES

Because the LT1312 provides excellent output regulation, the input power supply may be loosely regulated. One convenient (and economic) source of power is an auxiliary winding on the main 5V switching regulator inductor in the main system power supply.

LTC1142HV Auxiliary Winding Power Supply

Figure 1 is a schematic diagram which describes how a loosely regulated 14V power supply is created by adding an auxiliary winding to the 5V inductor in a split 3.3V/5V LTC1142HV power supply system. A turns ratio of 1:1.8 is used for transformer T1 to ensure that the input voltage to the LT1312 falls between 13V and 20V under all load conditions. The 9V output from this additional winding is rectified by diode D2, added to the main 5V output and applied to the input of the LT1312. (Note that the auxiliary winding must be phased properly as shown in Figure 1.)

The auxiliary winding is referenced to the 5V output which provides DC current feedback from the auxiliary supply to the main 5V section. The AC transient response is improved by returning the negative lead of C5 to the 5V output as shown.

When the 12V output is activated by a TTL high on the Enable line, the 5V section of the LTC1142HV is forced into continuous mode operation. A resistor divider composed of R2, R3 and switch Q3 forces an offset which is subtracted from the internal offset at the Sense– input (pin 14) of the LTC1142HV. When this external offset cancels the built-in 25mV offset, Burst Mode™ operation is inhibited and the LTC1142HV is forced into continuous mode operation. (See the LTC1142HV data sheet for further detail). In this mode, the 14V auxiliary supply can be

Burst Mode™ is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

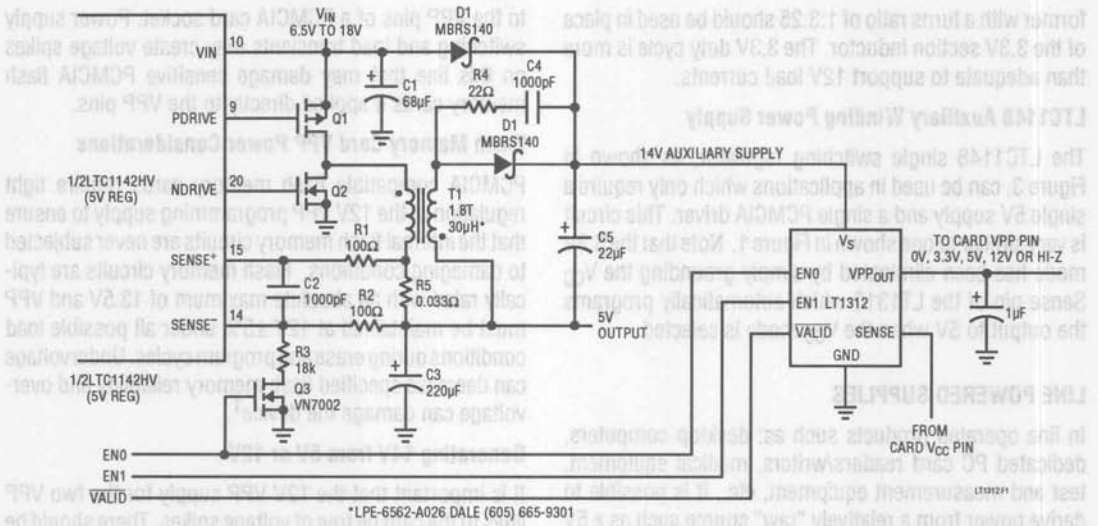


Figure 1. Deriving 14V Power from an Auxiliary Winding on the LTC1142HV 5V Regulator

loaded without regard to the loading on the 5V output of the LTC1142HV.

Continuous mode operation is only invoked when the LT1312 is programmed to 12V. If the LT1312 is programmed to 0V, 3.3V or 5V, power is obtained directly from the main power source (battery pack) through diode D1. Again, the LT1312 output can be loaded without regard to the loading of the main 5V output.

R4 and C4 absorb transient voltage spikes associated with the leakage inductance inherent in T1's secondary winding and ensure that the auxiliary supply does not exceed 20V.

Figure 2 is a graph of output voltage versus output current for the auxiliary 14V supply shown in Figure 1. Note that the auxiliary supply voltage is slightly higher when the 5V output is heavily loaded. This is due to the increased energy flowing through the main 5V inductor.

LTC1142HV Auxiliary Power from the 3.3V Output

The circuit of Figure 1 can be modified for operation with low-battery count applications (6 cell). As the input voltage falls, the 5V duty cycle increases to the point where there is simply not enough time to transfer energy from the 5V primary to the auxiliary winding secondary winding. For applications where heavy 12V load currents exist in conjunction with low input voltages (<6.5V), the auxiliary winding can be derived from the 3.3V section instead of the 5V section of the LTC1142HV. In this case, a trans-

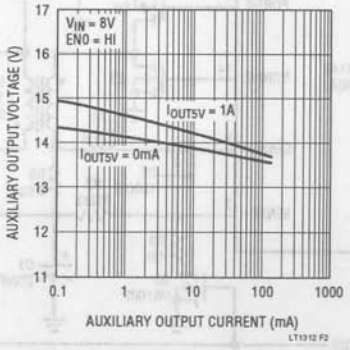


Figure 2. LTC1142 Auxiliary Supply Voltage

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APPLICATIONS INFORMATION

former with a turns ratio of 1:3.25 should be used in place of the 3.3V section inductor. The 3.3V duty cycle is more than adequate to support 12V load currents.

LTC1148 Auxiliary Winding Power Supply

The LTC1148 single switching regulator, as shown in Figure 3, can be used in applications which only require a single 5V supply and a single PCMCIA driver. This circuit is very similar to one shown in Figure 1. Note that the 3.3V mode has been eliminated by simply grounding the V_{CC} Sense pin of the LT1312 which automatically programs the output to 5V when the V_{CC} mode is selected.

LINE POWERED SUPPLIES

In line operated products such as: desktop computers, dedicated PC card readers/writers, medical equipment, test and measurement equipment, etc., it is possible to derive power from a relatively "raw" source such as a 5V or 12V power supply. The 12V supply line in a desktop computer however, is usually too "dirty" to apply directly to the VPP pins of a PCMCIA card socket. Power supply switching and load transients may create voltage spikes on this line that may damage sensitive PCMCIA flash memory cards if applied directly to the VPP pins.

Flash Memory Card VPP Power Considerations

PCMCIA compatible flash memory cards require tight regulation of the 12V VPP programming supply to ensure that the internal flash memory circuits are never subjected to damaging conditions. Flash memory circuits are typically rated with an absolute maximum of 13.5V and VPP must be maintained at 12V ±5% under all possible load conditions during erase and program cycles. Undervoltage can decrease specified flash memory reliability and overvoltage can damage the device[1].

Generating 14V from 5V or 12V

It is important that the 12V VPP supply for the two VPP lines to the card be free of voltage spikes. There should be little or no overshoot during transitions to and from the 12V level.

[1]See Application Note AP-357, "Power Supply Solutions for Flash Memory", Intel Corporation, 1992.

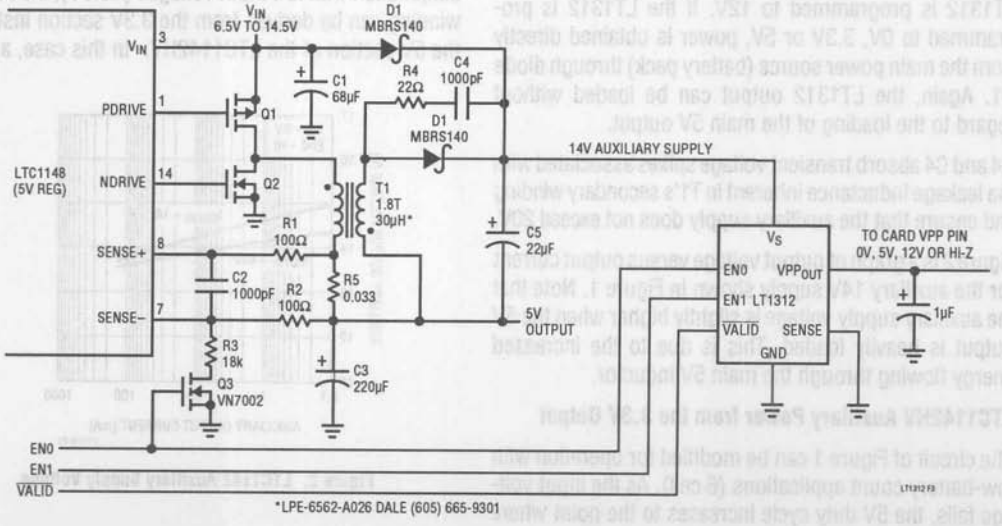

Figure 3. Deriving Auxiliary 14V Power from an LTC1148 5V Regulator

APPLICATIONS INFORMATION

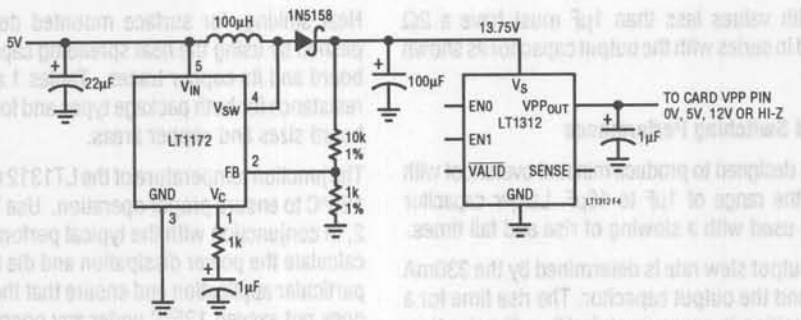

Figure 4. Local 5V to 15V Boost Regulator for Line Operated Applications

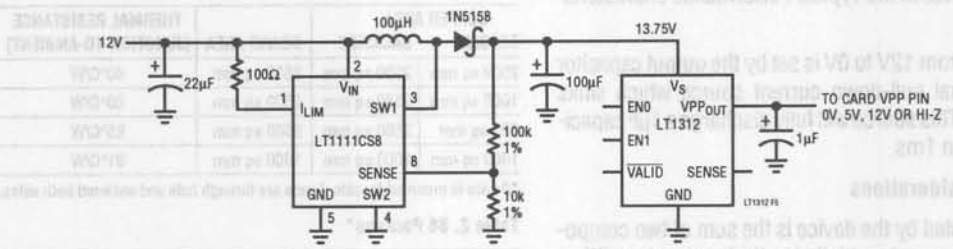

Figure 5. Local 12V to 15V Boost Regulator for Line Operated Applications

This is easily accomplished by generating a local 14V supply from a relatively "dirty" 5V or 12V supply as shown in Figures 4 and 5. Precise voltage control (and further filtering) is provided by the LT1312 driver/regulator. A further advantage to this scheme is that it adds current limit in series with the VPP pins to eliminate possible damage to the card socket, the PC card, or the switching power supply in the event of an accidental short circuit.

Output Capacitance

The LT1312 is designed to be stable with a wide range of output capacitors. The minimum recommended value is a 1µF with an ESR of 3Ω or less. The capacitor is connected directly between the output pin and ground as shown in Figure 6.

For applications where space is very limited, capacitors as low as 0.33µF can be used. Extremely low ESR ceramic

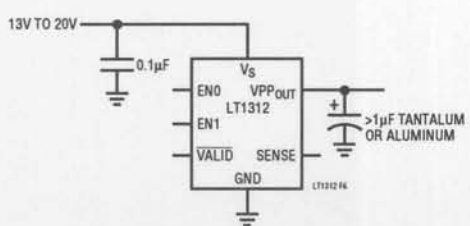

Figure 6. Recommended >1µF Tantalum Output Capacitor

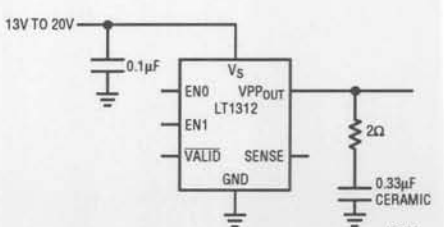

Figure 7. Using a 0.33µF to 1µF Output Capacitor

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APPLICATIONS INFORMATION

capacitors with values less than 1µF must have a 2Ω resistor added in series with the output capacitor as shown in Figure 7.

Transient and Switching Performance

The LT1312 is designed to produce minimal overshoot with capacitors in the range of 1µF to 10µF. Larger capacitor values can be used with a slowing of rise and fall times.

The positive output slew rate is determined by the 330mA current limit and the output capacitor. The rise time for a 0V to 12V transition is approximately 40µs, the rise time for a 10µF capacitor is roughly 400µs (see the Transient Response curves in the Typical Performance Characteristics section).

The fall time from 12V to 0V is set by the output capacitor and an internal pull-down current source which sinks about 30mA. This source will fully discharge a 1µF capacitor in less than 1ms.

Thermal Considerations

Power dissipated by the device is the sum of two components: output current multiplied by the input-output differential voltage $I_{OUT} \times (V_{IN} - V_{OUT})$, and ground pin current multiplied by supply voltage $I_{GND} \times V_{IN}$.

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics section.

Heat sinking, for surface mounted devices, is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Tables 1 and 2 list thermal resistance for both package types and for several different board sizes and copper areas.

The junction temperature of the LT1312 must be limited to 125°C to ensure proper operation. Use Table 1 and Table 2, in conjunction with the typical performance graphs, to calculate the power dissipation and die temperature for a particular application and ensure that the die temperature does not exceed 125°C under any operating conditions.

Table 1. N8 Package*

COPPER AREA TOPSIDE	COPPER AREA BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	80°C/W
1000 sq mm	2500 sq mm	2500 sq mm	80°C/W
225 sq mm	2500 sq mm	2500 sq mm	85°C/W
1000 sq mm	1000 sq mm	1000 sq mm	91°C/W

*Device is mounted topside. Leads are through hole and soldered both sides.

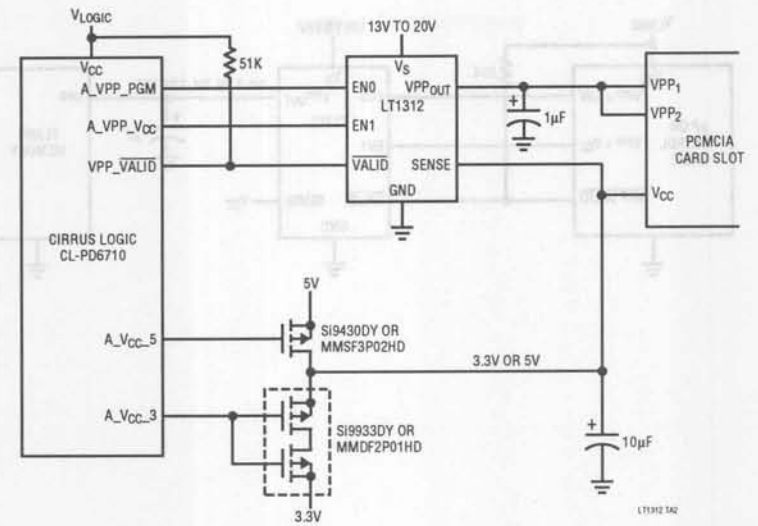
Table 2. S8 Package*

COPPER AREA TOPSIDE	COPPER AREA BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	120°C/W
1000 sq mm	2500 sq mm	2500 sq mm	120°C/W
225 sq mm	2500 sq mm	2500 sq mm	125°C/W
1000 sq mm	1000 sq mm	1000 sq mm	131°C/W

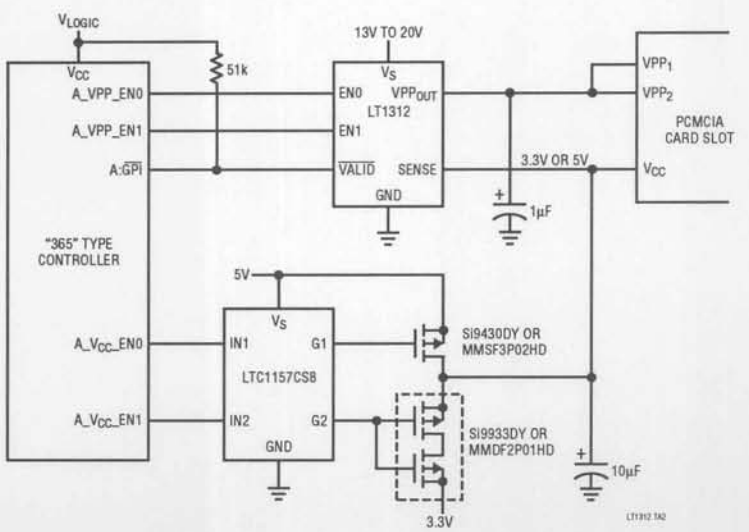
*Device is mounted topside.

TYPICAL APPLICATIONS

Single Slot Interface to CL-PD6710



Single Slot Interface to "365" Type Controller



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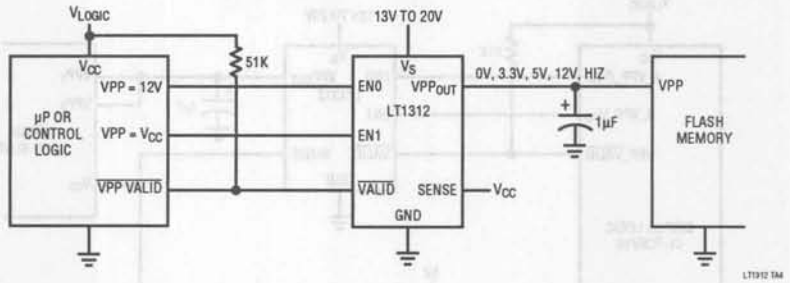
TYPICAL APPLICATIONS

Flash Memory Programmer



Dual PCMCIA VPP Driver/Regulator

May 1994

FEATURES

- **Digital Selection of 0V, V_{CC}, 12V or Hi-Z**
- Automatic Switching from 3.3V to 5V
- **120mA Output Current Capability**
- **Internal Current Limiting and Thermal Shutdown**
- Powered from Unregulated 13V to 20V Supply
- Logic Compatible with Standard PCMCIA Controllers
- 1µF Output Capacitors
- 60µA Quiescent Current in Hi-Z or 0V mode
- Independent VPP Valid Status Feedback Signals
- No VPP Overshoot

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers
- Flash Memory Programming

DESCRIPTION

The LT1313 provides 0V, 3.3V, 5V, 12V and Hi-Z regulated power to the VPP pins of two PCMCIA card slots from a single unregulated 13V to 20V supply. When used in conjunction with a PC Card Interface Controller, the LT1313 forms a complete minimum component-count interface for palmtop, pen-based and notebook computers. The two VPP output voltages are independently selected by four logic compatible digital inputs which interface directly with industry standard PC Card Interface Controllers.

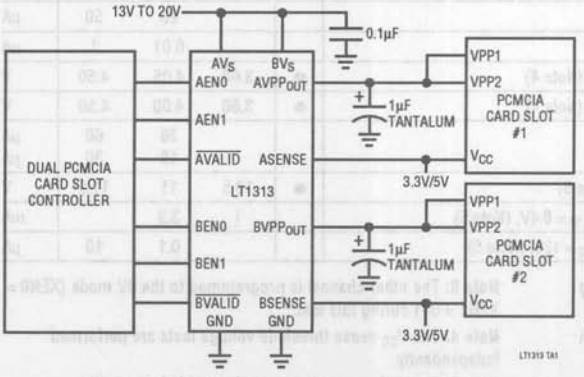
Automatic 3.3V to 5V switching is provided by two independent comparators which continuously monitor each PC card V_{CC} supply voltage and automatically adjust the VPP output to match the associated V_{CC} pin voltage when the VPP = V_{CC} mode is selected.

Two open-collector VPP $\overline{\text{VALID}}$ outputs are provided to indicate when the VPP outputs are in regulation at 12V.

The LT1313 is available in 16-pin SOIC packaging.

TYPICAL APPLICATION

Typical PCMCIA Dual Slot VPP Driver



LT1313 Truth Table

AEN0	AEN1	ASENSE	$AVPP_{OUT}$	$\overline{\text{AVALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V to 3.6V	3.3V	1
0	1	4.5V to 5.5V	5V	1
1	1	X	Hi-Z	1

X = Don't care

BEN0	BEN1	BSENSE	$BVPP_{OUT}$	$\overline{\text{BVALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V to 3.6V	3.3V	1
0	1	4.5V to 5.5V	5V	1
1	1	X	Hi-Z	1

Note: Each channel is independently controlled.

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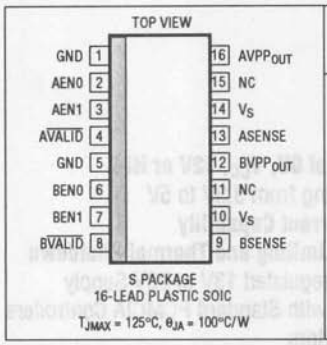
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Digital Input Voltage ..... 7V to (GND – 0.3V)
Sense Input Voltage ..... 7V to (GND – 0.3V)
$\overline{VALID}$ Output Voltage ..... 15V to (GND – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Operating Temperature ..... 0°C to 70°C
Junction Temperature ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1313CS

ELECTRICAL CHARACTERISTICS

V_S = 13V to 20V, T_A = 25°C (Note 1), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VPP_{OUT}	Output Voltage	Program to 12V, $I_{OUT} \le 120mA$ (Note 2)	●	11.52	12.00	12.48	V
		Program to 5V, $I_{OUT} \le 30mA$ (Note 2)	●	4.75	5.00	5.25	V
		Program to 3.3V, $I_{OUT} \le 30mA$ (Note 2)	●	3.135	3.30	3.465	V
		Program to 0V, $I_{OUT} = -300\mu A$			0.42	0.60	V
I_{LKG}	Output Leakage	Program to Hi-Z, $0V \le VPP_{OUT} \le 12V$	●	–10		10	µA
I_S	Supply Current	Both Channels Programmed to 0V	●		60	100	µA
		Both Channels Programmed to Hi-Z	●		60	100	µA
		One Channel Programmed to 12V, No Load (Note 3)	●		260	400	µA
		One Channel Programmed to 5V, No Load (Note 3)	●		105	150	µA
		One Channel Programmed to 3.3V, No Load (Note 3)	●		85	120	µA
		One Channel Programmed to 12V, I_{OUT} = 120mA (Note 3)	●		126	132	mA
		One Channel Programmed to 5V, I_{OUT} = 30mA (Note 3)	●		31	33	mA
		One Channel Programmed to 3.3V, I_{OUT} = 30mA (Note 3)	●		31	33	mA
I_{LIM}	Current Limit	Program to 3.3V, 5V or 12V (Note 3)			330	500	mA
V_{ENH}	Enable Input High Voltage		●	2.4			V
V_{ENL}	Enable Input Low Voltage		●			0.4	V
I_{ENH}	Enable Input High Current	$2.4V \le V_{IN} \le 5.5V$			20	50	µA
I_{ENL}	Enable Input Low Current	$0V \le V_{IN} \le 0.4V$			0.01	1	µA
V_{SEN5}	V_{CC} Sense Threshold	VPP_{OUT} = 3.3V to 5V (Note 4)	●	3.60	4.05	4.50	V
V_{SEN3}	V_{CC} Sense Threshold	VPP_{OUT} = 5V to 3.3V (Note 4)	●	3.60	4.00	4.50	V
I_{SEN}	V_{CC} Sense Input Current	V_{SENSE} = 5V			38	60	µA
		V_{SENSE} = 3.3V			18	30	µA
$V_{VALID\ TH}$	VPP_{VALID} Threshold Voltage	Program to 12V, (Note 5)	●	10.5	11	11.5	V
$I_{\overline{VALID}}$	VPP_{VALID} Output Drive Current	Program to 12V, V_{VALID} = 0.4V, (Note 5)		1	3.3		mA
	VPP_{VALID} Output Leakage Current	Program to 0V, V_{VALID} = 12V, (Note 5)			0.1	10	µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Both V_S pins (10, 14) must be connected together, and both ground pins (1, 5) must be connected together.

Note 2: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended.

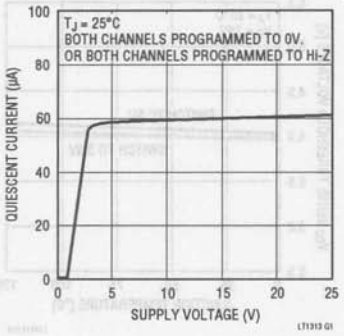
Note 3: The other channel is programmed to the 0V mode (XEN0 = XEN1 = 0V) during this test.

Note 4: The V_{CC} sense threshold voltage tests are performed independently.

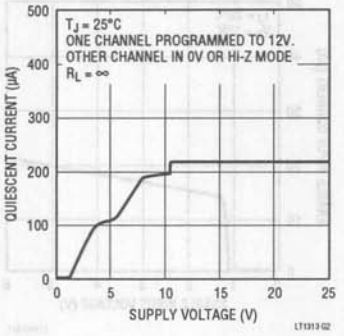
Note 5: The VPP_{VALID} tests are performed independently.

TYPICAL PERFORMANCE CHARACTERISTICS

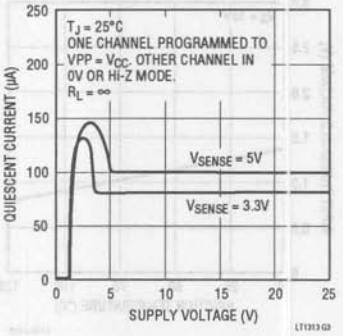
Quiescent Current (0V or Hi-Z Mode)



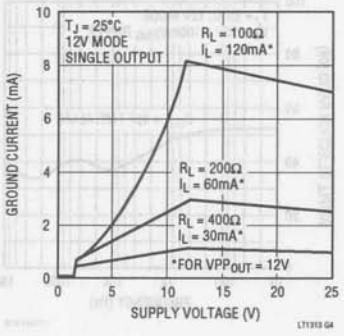
Quiescent Current (12V Mode)



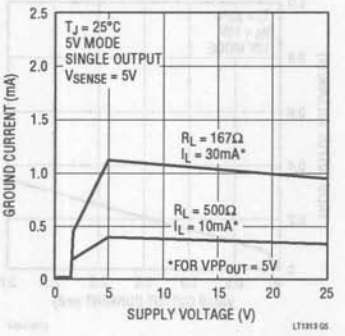
Quiescent Current (3.3V/5V Mode)



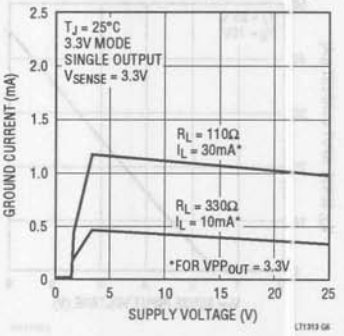
Ground Pin Current (12V Mode)



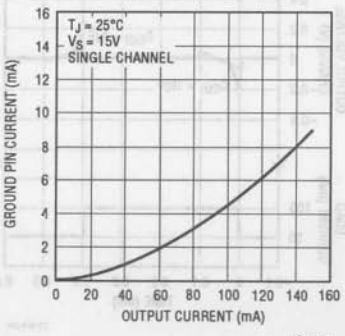
Ground Pin Current (5V Mode)



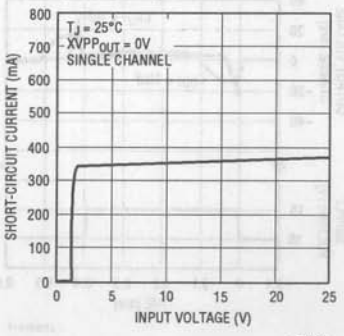
Ground Pin Current (3.3V Mode)



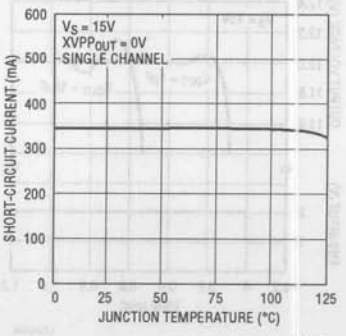
Ground Pin Current



Current Limit



Current Limit



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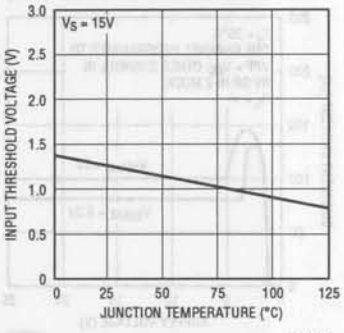
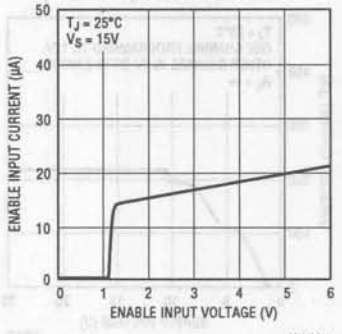
TYPICAL PERFORMANCE CHARACTERISTICS

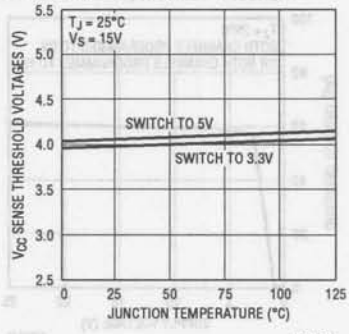
Enable Input Threshold Voltage



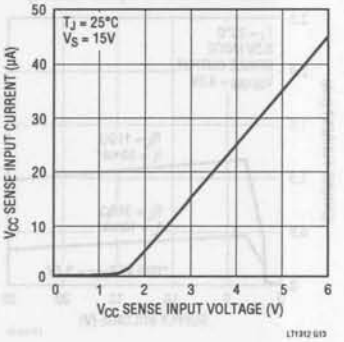
Enable Input Current



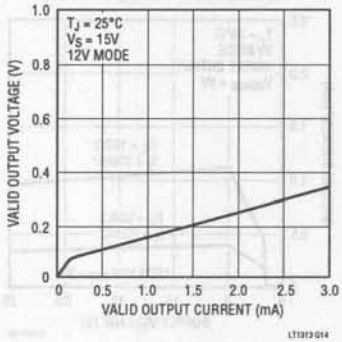
V_{CC} Sense Threshold Voltage



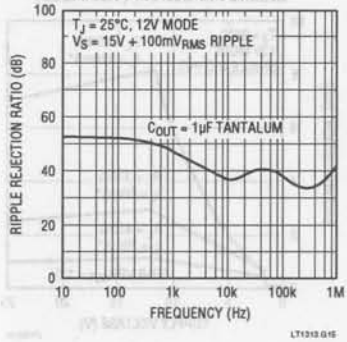
V_{CC} Sense Input Current



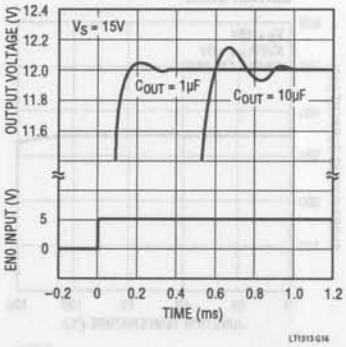
$\overline{VALID}$ Output Voltage



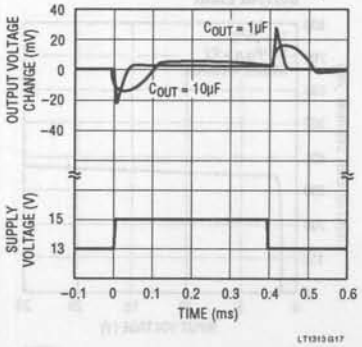
Ripple Rejection (12V)



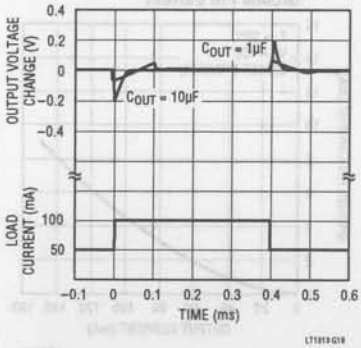
12V Turn-On Waveform



Line Transient Response (12V)



Load Transient Response (12V)



PIN FUNCTIONS

Supply Pins: Power is supplied to the device through the two supply pins *which must be connected together at all times* . The supply pins should be bypassed to ground if the device is more than six inches away from the main supply capacitor. A bypass capacitor in the range of 0.1µF to 1µF is sufficient. The supply voltage to the LT1313 can be loosely regulated between 13V and 20V.

VPP_{OUT} Pins: Each regulated output supplies power to the two PCMCIA card VPP pins which are typically tied together at the socket. Each VPP_{OUT} output is current limited to approximately 330mA. Thermal shutdown provides a second level of protection. A 1µF to 10µF tantalum output capacitor is recommended.

Input Enable Pins: The four digital input pins are high impedance inputs with approximately 20µA input current at 2.4V. The input thresholds are compatible with CMOS controllers and can be driven from either 5V or 3.3V CMOS logic. ESD protection diodes limit input excursions to 0.6V below ground.

$\overline{VALID}$ Output Pins: These pins are open-collector NPN outputs which are driven low when the corresponding VPP_{OUT} pin is in regulation, i.e., when it is above 11V. Two external 51k pull-up resistors are connected between these outputs and the same 5V or 3.3V logic supply powering the PCMCIA compatible control logic.

V_{CC} Sense Pins: Two independent comparators and 4V references automatically switch the VPP_{OUT} outputs from 5V to 3.3V depending upon the voltage sensed at the corresponding PCMCIA card socket V_{CC} pin. The input current for these pins is approximately 30µA. For 5V only operation, connect the Sense pins directly to ground. An ESD protection diode limits the input voltage to 0.6V below ground.

Ground Pins: *The two ground pins must be connected together at all times.*

OPERATION

The LT1313 is two programmable output voltage, low-dropout linear regulators designed specifically for PCMCIA VPP drive applications. Input power is typically obtained from a loosely regulated input supply between 13V and 20V. The LT1313 consists of the following blocks:

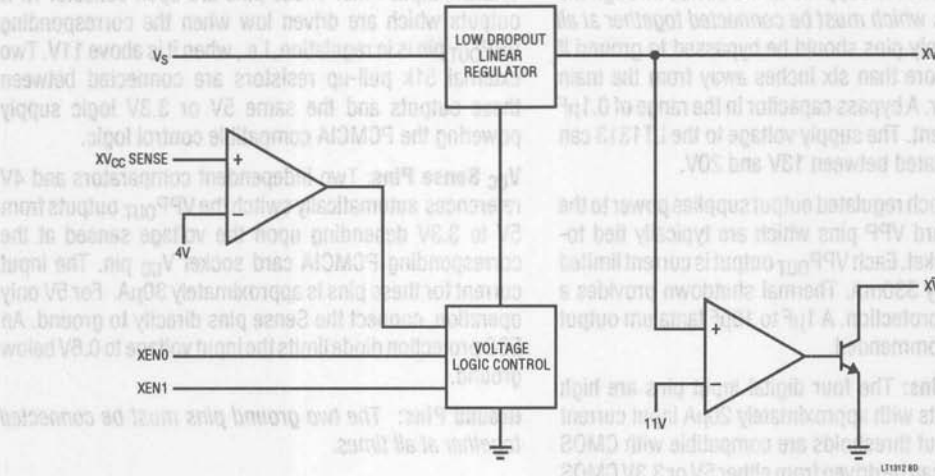
Two Low Dropout Voltage Linear Regulators: The heart of the LT1313 is two PNP-based low-dropout voltage regulators which drop the unregulated supply voltage from 13V to 20V down to 12V, 5V, 3.3V, 0V or Hi-Z depending upon the state of the four Enable inputs and the two V_{CC} Sense inputs. The regulators have built-in current limiting and thermal shutdown to protect the device, the loads, and the sockets against inadvertent short circuiting to ground.

Voltage Control Logic: The two VPP_{OUT} outputs have five possible output modes: 0V, 3.3V, 5V, 12V and Hi-Z. These five modes are selected by the four Enable inputs and the two V_{CC} Sense inputs as described by the Truth Table.

V_{CC} Sense Comparators: When the V_{CC} mode is selected, the LT1313 automatically adjusts each regulated VPP output voltage to 3.3V or 5V depending upon the voltage present at the corresponding PC card V_{CC} supply pin. The threshold voltage for these comparators is set at 4V and there is approximately 50mV of hysteresis provided to ensure clean switching between 3.3V and 5V.

VPP $\overline{VALID}$ Comparator: Two voltage comparators monitor each output voltage when the 12V mode is selected and are driven low when the output is in regulation above 11V. These two outputs function separately.

BLOCK DIAGRAM (One Channel)



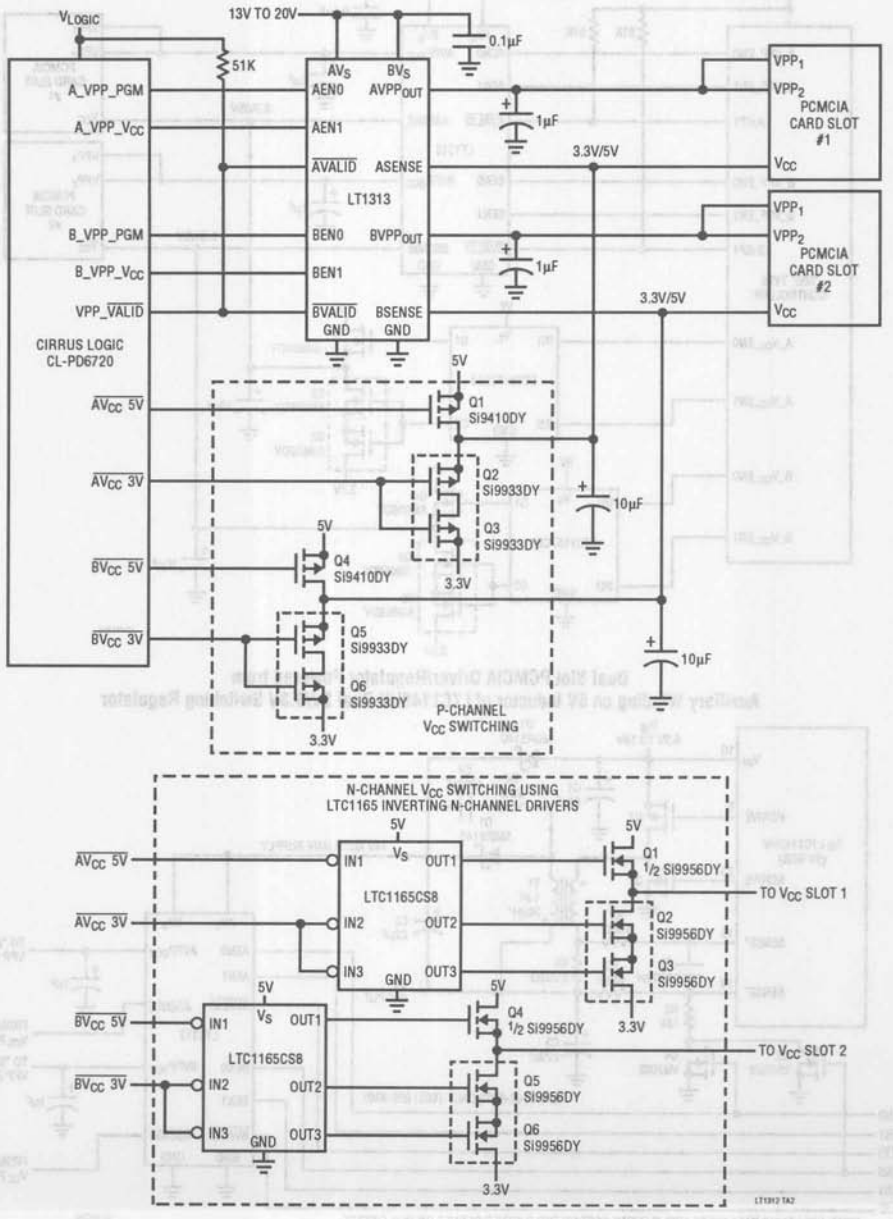
APPLICATIONS INFORMATION

The LT1313 is two voltage programmable linear regulators designed specifically for PCMCIA VPP driver applications. The device operates with very low quiescent current (60µA) in the 0V and Hi-Z modes of operation. In the Hi-Z mode, the output leakage current falls to 1µA. In addition to the low quiescent currents, the LT1313 incorporates several protection features which make it ideal for PCMCIA applications. The LT1313 has built-in current limiting (330mA) and thermal shutdown to protect the device and the socket VPP pins against inadvertent short-circuit conditions.

For more detailed applications information, see the LT1312 Single PCMCIA VPP Driver/Regulator data sheet.

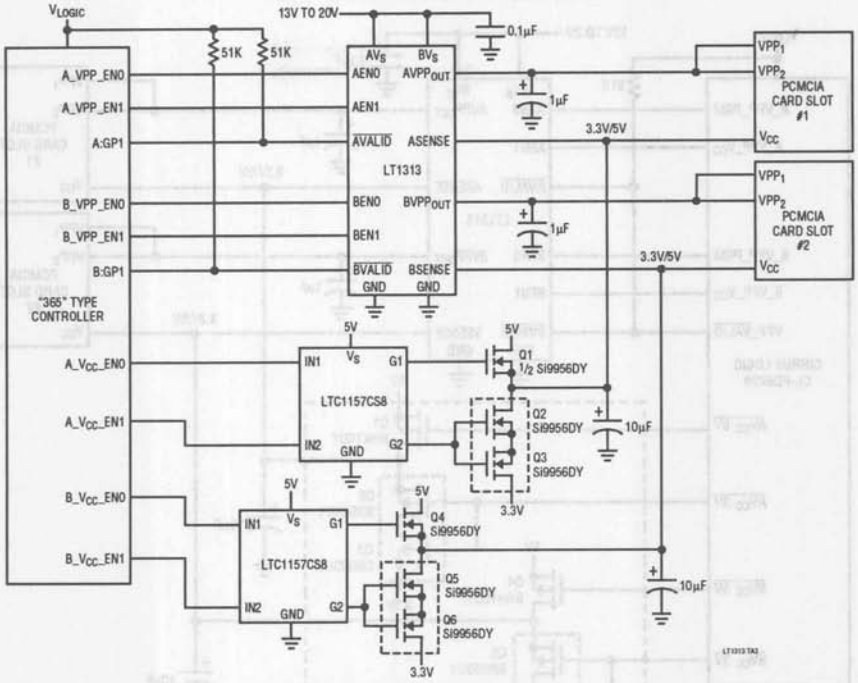
TYPICAL APPLICATIONS

Dual Slot PCMCIA Interface to CL-PD6720

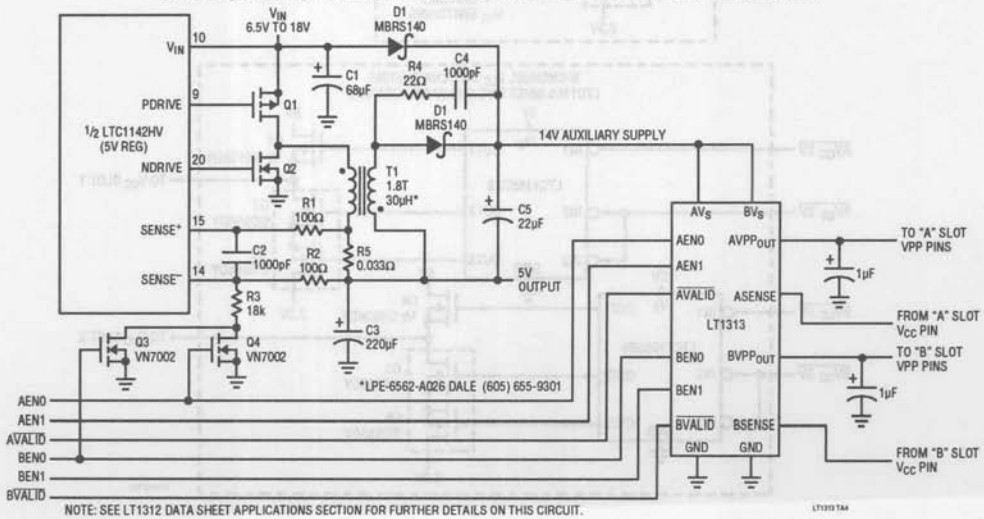


TYPICAL APPLICATIONS

Dual Slot PCMCIA Interface to "365" Type Controller



Dual Slot PCMCIA Driver/Regulator Powered from Auxiliary Winding on 5V Inductor of LTC1142HV Dual 5V/3.3V Switching Regulator



NOTE: SEE LT1312 DATA SHEET APPLICATIONS SECTION FOR FURTHER DETAILS ON THIS CIRCUIT.

LTC1318

Single 5V RS232/RS422/AppleTalk® Transceiver

May 1994

FEATURES

- Single Chip Provides Standard RS232 or RS422/AppleTalk Port
- Operates From a Single 5V Supply
- Charge Pump Uses 0.1µF Capacitors
- Output Common-Mode Voltage Range Exceeds Power Supply Rails for All Drivers
- Driver Outputs are High Impedance With Power Off
- Pin Selectable RS232/RS422 Receiver
- Thermal Shutdown Protection
- Drivers are Short-Circuit Protected

APPLICATIONS

- Dual-Mode RS232/RS422 Peripherals
- AppleTalk Peripherals
- Single 5V Systems

DESCRIPTION

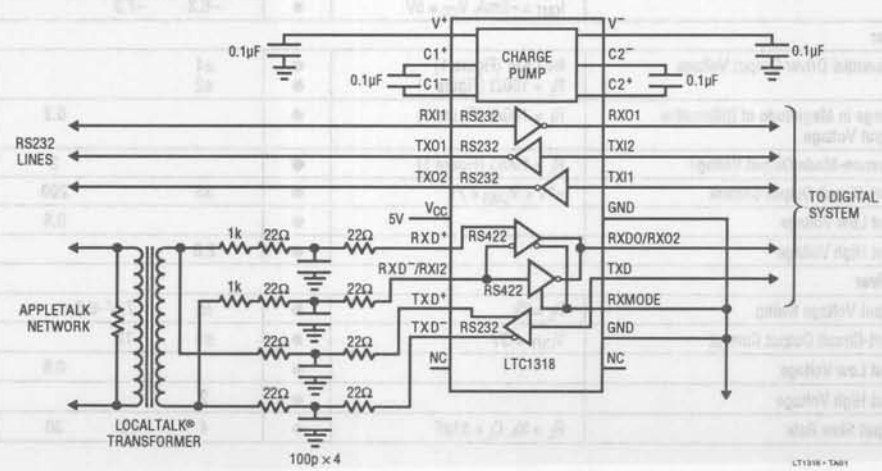
The LTC1318 is an RS232/RS422 transceiver that operates from a single 5V supply. It includes an on-board charge pump to generate a ±8V supply which allows true RS232 output swings. The charge pump requires only four external 0.1µF capacitors. The LTC1318 includes two RS232 drivers, a differential RS422 driver, a dedicated RS232 receiver, and a pin selectable RS232/RS422 receiver which can receive either single-ended or differential signals.

The LTC1318 features driver outputs which can be taken to common-mode voltages outside the power supply rails without damage. Additionally, the driver outputs assume a high impedance state when the power is shut off, preventing externally applied signals from feeding back into the power supplies. The RS232 devices will operate at speeds up to 100k baud. The RS422 devices will operate up to 2M baud.

The LTC1318 is available in a 24-lead SOL package.

AppleTalk and LocalTalk are registered trademarks of Apple Computer, Inc.

TYPICAL APPLICATION



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage:
- V_{CC} 7V
- V^+ 13.2V
- V^- ..... –13.2V

Input Voltage:
- All Drivers ..... –0.3 to (V_{CC} + 0.3V)
- All Receivers ..... –25V to 25V
- RXMODE Pin ..... –0.3V to (V_{CC} + 0.3V)

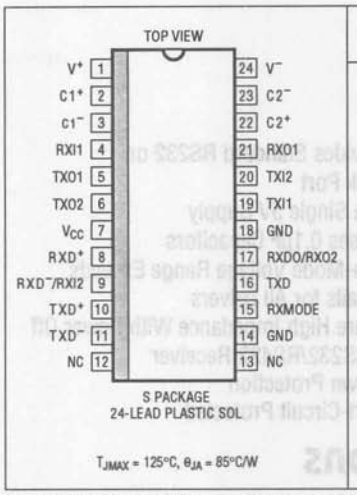
Output Voltage:
- RS232 Drivers ..... (V^+ – 30V) to (V^- + 30V)
- RS422 Drivers ..... ±15V
- All Receivers ..... –0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration:
- V^+ or V^- to GND ..... 30 sec
- Driver or Receiver Outputs ..... Indefinite

Operating Temperature Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1318CS

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

V_S = 5V ±5%, C1 = C2 = 0.1µF, T_A = 0°C to 70°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Supply Current	No Load	●		18	30	mA
V^+	Positive Charge Pump Output Voltage	I_{OUT} = 0mA I_{OUT} = 10mA, V_{CC} = 5V	● ●	7.8 6.8	8.8 7.4		V V
V^-	Negative Charge Pump Output Voltage	I_{OUT} = 0mA I_{OUT} = –5mA, V_{CC} = 5V	● ●	–7.3 –6.3	–8.6 –7.3		V V
Differential Driver							
V_{OD}	Differential Driver Output Voltage	No Load (Figure 1) R_L = 100Ω (Figure 1)	● ●	±4 ±2			V V
DV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 100Ω (Figure 1)	●			0.2	V
V_{OC}	Common-Mode Output Voltage	R_L = 100Ω (Figure 1)	●			3	V
I_{DSS}	Short-Circuit Output Current	–1V < V_{CMR} < 7V	●	35		200	mA
V_L	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	2.0			V
Single-Ended Driver							
V_O	Output Voltage Swing	R_L = 3k	●	±5	7.3/–6.5		V
I_{OSS}	Short-Circuit Output Current	V_{OUT} = 0V	●	±5	12		mA
V_{IL}	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	2			V
SR	Output Slew Rate	R_L = 3k, C_L = 51pF	●	4	15	30	V/µs

ELECTRICAL CHARACTERISTICS

V_S = 5V ±5%, C1 = C2 = 0.1µF, T_A = 0°C to 70°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Receiver							
V_{TH}	Differential Receiver Threshold		●	–0.2		0.2	V
CMR	Common-Mode Input Range		●	–7		7	V
	Hysteresis	V_{CM} = OV	●		70		mV
R_{IN}	Input Resistance	TA = 25°C		3	5	7	kΩ
V_{OL}	Output Low Voltage	I_{OUT} = –1.6mA				0.4	V
V_{OH}	Output High Voltage	I_{OUT} = 160µA, V_{CC} = 5V	●	3.5			V
I_{OSS}	Short-Circuit Output Current	V_O = GND or V_{CC}	●	±7		±85	mA
Single-Ended Receiver							
V_L	Input Voltage Low Threshold		●	0.8	1.3		V
V_{IH}	Input Voltage High Threshold		●		1.7	2.4	V
	Hysteresis		●	0.1	0.4	1.0	V
R_{IN}	Input Resistance	TA = 25°C		3	5	7	kΩ
V_{OL}	Output Low Voltage	I_{OUT} = –4mA	●		0.2	0.4	V
V_{OH}	Output High Voltage	I_{OUT} = 4mA, V_{CC} = 5V	●	3.5	4.8		–V
I_{OSS}	Short-Circuit Output Current	V_O = GND or V_{CC}	●	±7		±85	mA
V_{ILRXM}	RXMODE Input Low Voltage		●	0.8	1.6		V
V_{IHRXM}	RXMODE Input High Voltage		●		1.6	2.0	V
I_{INRXM}	RXMODE Input Current	V_{IN} = OV or V_{CC}	●			±2	mA
Switching Characteristics							
$t_{PLH,HL}$	Differential Driver Propagation Delay	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		35	100	ns
t_{SKEW}	Differential Driver Output to Output	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		5	35	ns
$t_{R,F}$	Differential Driver Rise, Fall Time	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		15	50	ns
$t_{PLH,HL}$	Differential Receiver Propagation Delay	C_L = 15pF, (Figures 4)	●		110	200	ns
t_{SEL}	Receiver Mode Switching Time		●		25	100	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are negative, all currents out of device pins are positive. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

TEST CIRCUITS

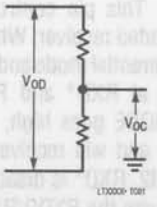


Figure 1.

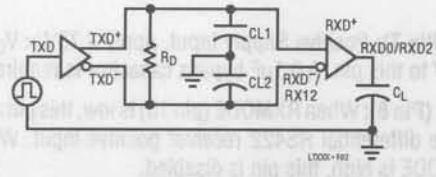


Figure 2.

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SWITCHING WAVEFORMS

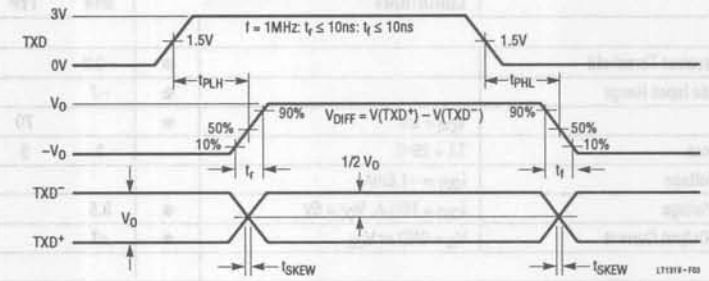

Figure 3. Differential Driver

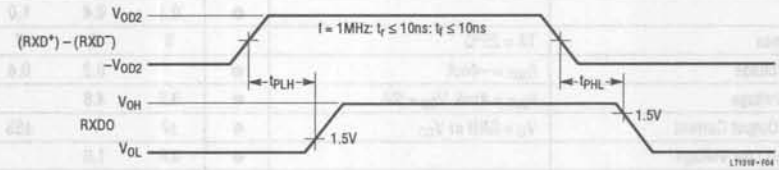

Figure 4. Differential Receiver

PIN FUNCTIONS

V^+ (Pin 1): Charge Pump Positive Output. This pin requires a 0.1µF capacitor to ground. Under normal operation this pin maintains a voltage of about 8.8V above ground. An external load can be connected between this pin and ground or V^-.

$C1^+$, $C1^-$ (Pins 2, 3): C1 Inputs. Connect a 0.1µF capacitor between $C1^+$ and $C1^-$.

RXI1 (Pin 4): First RS232 Single-Ended Receiver Input. This is an inverting receiver.

TXO1, TXO2 (Pins 5,6): RS232 Single-Ended Driver Outputs.

V_{CC} (Pin 7): Positive Supply Input. Apply 4.75V × V_{CC} × 5.25V to this pin. A 0.1µF bypass capacitor is required.

RXD^+ (Pin 8): When RXMODE (pin 15) is low, this pin acts as the differential RS422 receiver positive input. When RXMODE is high, this pin is disabled.

RXD^-/RXI2 (Pin 9): When RXMODE is low, this pin acts as the differential RS422 receiver negative input. When RXMODE (pin 15) is high, this pin acts as the second RS232 receiver input. The receiver is inverting in RS232 mode.

TXD^+ (Pin 10): Differential RS422 Driver Noninverting Output.

TXD^- (Pin 11): Differential RS422 Driver Inverting Output.

NC (Pin 12,13): No Internal Connection.

GND (Pins 14, 18): Power Supply Ground. Connect both pins to each other and to the ground.

RXMODE (Pin 15): This pin controls the state of the differential/single-ended receiver. When RXMODE is low, the receiver is in differential mode and will receive RS422-compatible signals at RXD^+ and RXD^-/RXI2 (pins 8 and 9). When RXMODE goes high, the receiver enters single-ended mode and will receive RS232-compatible signals at RXD^-/RXI2. RXD^+ is disabled in single-ended mode. Both modes use the RXDO/RXO2 pin (Pin 17) as their output.

PIN FUNCTIONS

TXD (Pin 16): Differential RS422 Driver Input (TTL Compatible).

RXD0/RX02 (Pin 17): This is the output of the configurable differential/single-ended receiver.

TXI1, TXI2 (Pins 20,19): RS232 Driver Inputs (TTL Compatible). Both are inverting inputs.

RX01 (Pin 21): First RS232 Receiver Outputs (TTL compatible).

$C2^+$, $C2^-$ (Pins 22, 23): C2 inputs. Connect a 0.1µF capacitor between $C2^+$ and $C2^-$.

V^- (Pin 24): Charge Pump Negative Output. This pin requires a 0.1µF capacitor to ground. Under normal operation, this pin maintains a voltage of about 8.6V below ground. An external load can be connected between this pin and ground or V^+.

APPLICATION INFORMATION

Interface Standards

The LTC1318 provides compatibility with both RS232 and RS422/AppleTalk/LocalTalk standards in a single chip, enabling a system to communicate using either protocol as necessary. The LTC1318 provides two RS232 single-ended drivers and one RS422 differential driver and two receivers. One of the receivers is a dedicated RS232 single-ended receiver, while the other can be configured for RS232 (single-ended) or RS422 (differential) operation by controlling the logic state of the select pin. All single-ended drivers and receivers meet the RS232C specification for output swing, load driving capacity and input range, and can additionally transmit and receive signals as high as 100kbaud. The differential driver and receiver can interface to both RS422 and AppleTalk networks, and can transmit and receive signals at rates exceeding 2Mbaud.

Fault Protection

The LTC1318 incorporates many protection features to make it as "bustproof" as possible. All driver outputs and receiver inputs are protected against ESD strikes to 6kV, eliminating the need for external protection devices in most applications. All driver outputs can be taken outside the power supply rails without damage and will not allow current to be forced back into the supplies, preventing the output fault from affecting other logic circuits using the same power supply. Additionally, the driver outputs enter a high-impedance state when the power is removed, preventing the system from loading the data lines when it is shut off. All driver and receiver outputs are protected against short circuits to ground or to the supply rails.

Charge Pump Power Supply

The LTC1318 includes an on-board charge pump to generate the voltages necessary for true RS232 compatible output swing. This charge pump requires just four external 0.1µF capacitors to operate; two flying caps connected to the $C1^+/C1^-$ and $C2^+/C2^-$ pins, and two hold caps, one from V^+ to ground and one from V^- to ground. The charge pump has enough extra capacity to drive light external loads and still meet RS232 specifications; it will support a 10mA load from V^+ to ground or a 5mA from V^+ to V^- (Figure 5).

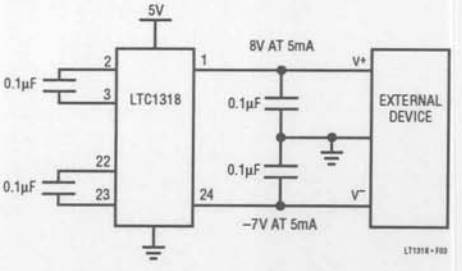

Figure 5.

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APPLICATION INFORMATION

Configurable RS422/RS232 Receiver

There are two line receivers in the LTC1318. One is a dedicated RS232 receiver; the other can receive both single-ended RS232 signals and differential RS422 signals. This second receiver has two inputs; RXD^+ (pin 8) and RXD^- (pin 9) to accept differential signals; The RXD^+ input is disabled in single-ended mode. The receiver mode is set by the RXMODE (pin 15). A low level on RXMODE configures the receiver in differential mode; it accepts input at RXD^+ and RXD^-, and outputs the data at RXDO (pin 17). A high level at RXMODE forces the receiver into single-ended mode; RXD^+ is disabled, pin 9 switches identity from RXD^- to RXI2, and pin 17 switches from RXDO to RXO2, the single-ended data output. In this mode the receiver accepts RS232 signals at RXI2 and outputs the data through RXO2. The receiver becomes inverting in single-ended mode. This receiver can switch between its two modes within 100ns allowing the system to sense the input signal and configure itself accordingly.

INITIAL RELEASE
Final Electrical Specifications

LTC1323

Single 5V AppleTalk® Transceiver

January 1994

FEATURES

- Single Chip Provides Complete LocalTalk®/AppleTalk Port
- Operates From a Single 5V Supply
- ESD Protection to 10kV on Receiver Inputs and Driver Outputs
- Low Power: I_{CC} = 2.4mA Typ
- Shutdown Pin Reduces I_{CC} to 0.5µA Typ
- Receiver Keep-Alive Function: I_{CC} = 65µA Typ
- Differential Driver Drives Either Differential AppleTalk or Single-Ended EIA562 Loads
- Drivers Maintain High Impedance in Three-State or with Power Off
- Thermal Shutdown Protection
- Drivers are Short-Circuit Protected

APPLICATIONS

- LocalTalk Peripherals
- Notebook/Palmtop Computers
- Battery-Powered Systems

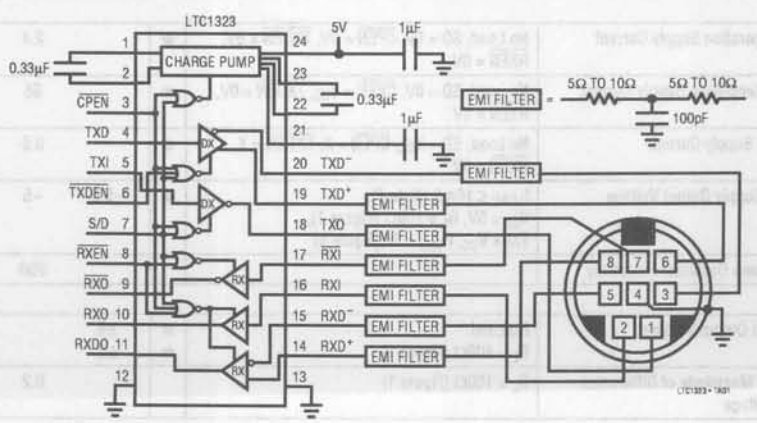
DESCRIPTION

The LTC1323 is a single 5V line transceiver designed to operate on Appletalk or EIA562 networks. The LTC1323 is available in 16-pin or 24-pin versions, each includes a differential RS422 compatible transceiver. A charge pump generates the chip's –5V supply which may also be used to power an external device. The 24-pin LTC1323 includes an additional dedicated EIA562 driver and two EIA562 receivers, one of which features a micropower keep-alive mode which can be used for monitoring external wake-up signals. The LTC1323 draws only 2.4mA quiescent current when active, 65µA in receiver keep-alive mode, and 0.5µA in shutdown making it ideal for use in battery-powered systems.

The differential driver will drive either differential AppleTalk loads or EIA562 single-ended loads. The driver outputs three-state when disabled, during shutdown, in receiver keep-alive mode, or when the power is off. The driver outputs will maintain high impedance even with output common-mode voltages beyond the power supply rails. Both the driver outputs and receiver inputs are protected against ESD damage to 10kV.

AppleTalk and LocalTalk are registered trademarks of Apple Computer, Inc.

TYPICAL APPLICATION



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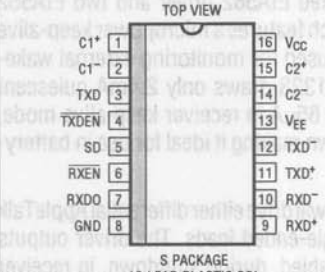
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 7V
Input Voltage
  Logic Inputs ..... −0.3V to V_{CC} + 0.3V
  Receiver Inputs ..... ±15V
Driver Output Voltage (Forced) ..... ±15V
Driver Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

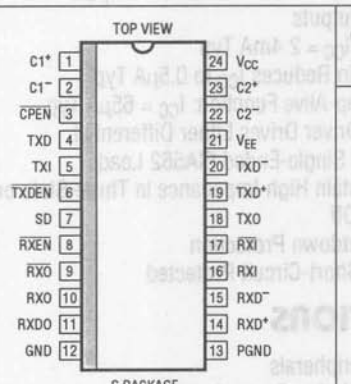


S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1323CS-16



S PACKAGE
24-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1323CS

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Normal Operation Supply Current	No Load, SD = 0V, $\overline{CPEN}$ = 0V, $\overline{TXDEN}$ = 0V, $\overline{RXEN}$ = 0V	●		2.4	4	mA
	Receiver Keep-Alive Supply Current	No Load, SD = 0V, $\overline{CPEN}$ = V_{CC}, $\overline{TXDEN}$ = 0V, $\overline{RXEN}$ = 0V	●		65	100	µA
	Shutdown Supply Current	No Load, SD = V_{CC}, $\overline{CPEN}$ = X, $\overline{TXDEN}$ = X, $\overline{RXEN}$ = 0V	●		0.5	10	µA
V_{EE}	Negative Supply Output Voltage	$I_{LOAD} \leq$ 10mA (Note 4), V_{CC} = 5V, R_L = 100Ω (Figure 1), TXI = V_{CC}, R_{TXO} = 3k (Figure 5)	●	−5.5	−5	−4.5	V
f_{OSC}	Charge Pump Oscillator Frequency				200		kHz
Differential Driver							
V_{OD}	Differential Output Voltage	No Load R_L = 100Ω (Figure 1)	● ●	±8 ±2			V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 100Ω (Figure 1)			0.2		V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver							
V_{OC}	Differential Common-Mode Output Voltage	R_L = 100Ω			3		V
V_{OS}	Single-Ended Output Voltage	No Load	●	±4.5			V
		R_L = 3k to GND	●	±3.7			V
V_{CMR}	Common-Mode Range	SD = V_{CC} or $\overline{CPEN}$ = V_{CC} or Power Off	●			±10	V
I_{SS}	Short-Circuit Current	$-5V \le V_O \le 5V$	●	35	120	250	mA
I_{OZ}	Three-State Output Current	SD = V_{CC} or $\overline{CPEN}$ = V_{CC} or Power Off, $-10V \le V_O \le 10V$	●		±2	±200	µA
Single-Ended Driver (Note 5)							
V_{OS}	Single-Ended Output Voltage	No Load	●	±4.5			V
		R_L = 3k to GND	●	±3.7			V
V_{CMR}	Common-Mode Range	SD = V_{CC} or $\overline{CPEN}$ = V_{CC} or $\overline{TXDEN}$ = V_{CC} or Power Off	●			±10	V
I_{SS}	Short-Circuit Current	$-5V \le V_O \le 5V$	●	35	220	500	mA
I_{OZ}	Three-State Output Current	SD = V_{CC} or $\overline{CPEN}$ = V_{CC} or $\overline{TXDEN}$ = V_{CC} or Power Off, $-10V \le V_O \le 10V$	●		±2	±200	µA
Receivers							
R_{IN}	Input Resistance	$-7V \le V_{IN} \le 7V$	●	12			kΩ
	Differential Receiver Threshold Voltage	$-7V \le V_{CM} \le 7V$	●	−200		200	mV
	Differential Receiver Input Hysteresis	$-7V \le V_{CM} \le 7V$	●		70		mV
	Single-Ended Input, Low Voltage	(Note 5)	●			0.8	V
	Single-Ended Input, High Voltage	(Note 5)	●	2			V
V_{OH}	Output High Voltage	I_O = −4mA	●	3.5			V
V_{OL}	Output Low Voltage	I_O = 4mA	●			0.4	V
I_{SS}	Output Short-Circuit Current	$-5V \le V_O \le 5V$	●	7		85	mA
I_{OZ}	Output Three-State Current	$-5V \le V_O \le 5V$, $\overline{RXEN}$ = V_{CC}	●		±2	±100	µA
Logic Inputs							
VIH	Input High Voltage	All Logic Input Pins	●	2.0			V
VIL	Input Low Voltage	All Logic Input Pins	●			0.8	V
IC	Input Current	All Logic Input Pins	●		±1.0	±20	µA
Switching Characteristics							
t_{PLH}, t_{PHL}	Differential Driver Propagation Delay	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		40	120	ns
	Differential Driver Propagation Delay with Single-Ended Load	R_L = 3k, C_L = 100pF (Figures 3, 9)	●		120	180	ns
	Single-Ended Driver Propagation Delay	R_L = 3k, C_L = 100pF, (Figures 5, 10) (Note 5)	●		40	120	ns
	Differential Receiver Propagation Delay	C_L = 15pF (Figures 2, 11)	●		70	160	ns
	Single-Ended Receiver Propagation Delay	C_L = 15pF (Figures 6, 12) (Note 5)	●		70	160	ns
	Inverting Receiver Propagation Delay in Keep-Alive Mode, SD = 0V, $\overline{CPEN}$ = V_{CC}	C_L = 15pF (Figures 6, 12) (Note 5)	●		150	400	ns
t_{SKEW}	Differential Driver Output to Output	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		10	50	ns

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ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Characteristics							
t_r, t_f	Differential Driver Rise/Fall Time	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		50	150	ns
	Differential Driver Rise/Fall Time with Single-Ended Load	R_L = 3k, C_L = 100pF (Figures 3, 9)	●		50	150	ns
	Single-Ended Driver Rise/Fall Time	R_L = 3k, C_L = 100pF (Figures 5, 10) (Note 5)	●		15	80	ns
t_{HDIS}, t_{LDIS}	Differential Driver Output Active to Disable	C_L = 15pF (Figures 4, 8)	●		50	150	ns
	Any Receiver Output Active to Disable	C_L = 15pF (Figures 4, 13)	●		30	100	ns
t_{ENH}, t_{ENL}	Differential Driver Enable to Output Active	C_L = 15pF (Figures 4, 8)	●		50	150	ns
	Any Receiver, Enable to Output Active	C_L = 15pF (Figures 4, 13)	●		30	100	ns
V_{EER}	Supply Rise Time From Shutdown or Receiver Keep-Alive	C1 = C2 = 0.33µF, C_{VEE} = 1µF	●		0.2		ms

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

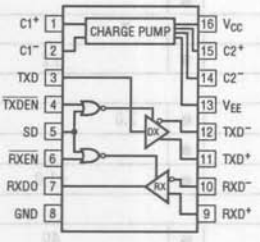
Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

Note 4: I_{LOAD} is an external current being sunk into the V_{EE} pin.

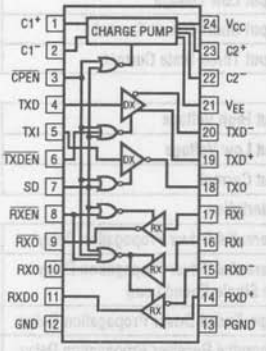
Note 5: These specifications apply to the 24-pin package only.

PIN FUNCTIONS

LTC1323CS-16



LTC1323CS



(16-Pin/24-Pin)

C1+ (Pin 1/Pin 1): C1 Positive Input. Connect a 0.33µF capacitor between C1+ and C1−.

C1− (Pin 2/Pin 2): C1 Negative Input. Connect a 0.33µF capacitor between C1+ and C1−.

$\overline{\text{CPEN}}$ (NA/Pin 3): TTL Level Charge Pump Enable Input. With $\overline{\text{CPEN}}$ held low, the charge pump is enabled and the chip operates normally. When $\overline{\text{CPEN}}$ is pulled high, the charge pump is disabled as well as both drivers, the noninverting single-ended receiver, and the differential receiver. The inverting single-ended receiver ($\overline{\text{RXI}}$) is kept alive to monitor the control line and I_{CC} drops to 65µA. To turn off the receiver and drop I_{CC} to 0.5µA, pull the S/D pin high.

PIN FUNCTIONS

TXD (Pin 3/Pin 4): Differential Driver Input (TTL compatible).

TXI (NA/Pin 5): Single-Ended Driver Input (TTL compatible).

$\overline{\text{TXDEN}}$ (Pin 4/Pin 6): Differential Driver Output Enable (TTL compatible). A high level on this pin forces the differential driver into three-state; a low level enables the driver. This input does not affect the single-ended driver.

S/D (Pin 5/Pin 7): Shutdown Input (TTL compatible). When this pin is high, the chip is shut down. All driver and receiver outputs are three-state, the charge pump turns off, and the supply current drops to 0.5µA. A low level on this pin allows normal operation.

$\overline{\text{RXEN}}$ (Pin 6/Pin 8): Receiver Enable (TTL compatible). A high level on this pin disables the receivers and three-states the logic outputs; a low level allows normal operation.

$\overline{\text{RXO}}$ (NA/Pin 9): Inverting Single-Ended Receiver Output. Remains active in the receiver keep-alive mode.

RXO (NA/Pin 10): Noninverting Single-Ended Receiver Output.

RXDO (Pin 7/Pin 11): Differential Receiver Output.

GND (Pin 8/Pin 12): Signal Ground. Connect to PGND with 24-pin package.

PGND (NA/Pin 13): Power ground is connected internally to the charge pump and differential driver. Connect to the GND pin.

RXD$^+$ (Pin 9/Pin 14): Differential Receiver Noninverting Input. When this pin is ≥200mV above RXD$^-$, RXDO will be high; when this pin is ≥200mV below RXD$^-$, RXDO will be low.

RXD$^-$ (Pin 10/Pin 15): Differential Receiver Inverting Input.

RXI (NA/Pin 16): Noninverting Receiver Input. This input controls the RXO output.

$\overline{\text{RXI}}$ (NA/Pin 17): Inverting Receiver Input. This input controls the $\overline{\text{RXO}}$ output. In receiver keep-alive mode ($\overline{\text{CPEN}}$ high, S/D low), this receiver can be used to monitor a wake-up control signal.

TXO (NA/Pin 18): Single-Ended Driver Output.

TXD$^+$ (Pin 11/Pin 19): Differential Driver Noninverting Output.

TXD$^-$ (Pin 12/Pin 20): Differential Driver Inverting Output.

V_{EE} (Pin 13/Pin 21): The Negative Supply Charge Pump Output. Requires a 1µF bypass capacitor to ground. If an external load is connected to the V_{EE} pin, the bypass capacitor value should be increased to 4.7µF.

C2$^-$ (Pin 14/Pin 22): C2 Negative Input. Connect a 0.33µF capacitor between C2$^+$ and C2$^-$.

C2$^+$ (Pin 15/Pin 23): C2 Positive Input. Connect a 0.33µF capacitor between C2$^+$ and C2$^-$.

V_{CC} (Pin 16/Pin 24): The Positive Supply Input. 4.5V ≤ V_{CC} ≤ 5.5V. Requires a 1µF bypass capacitor to ground.

TEST CIRCUITS

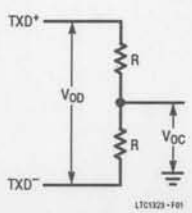


Figure 1

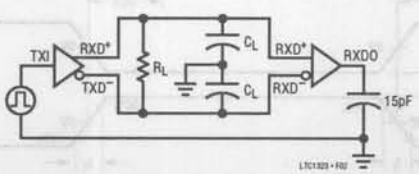


Figure 2

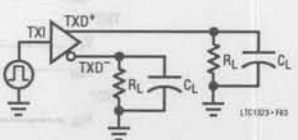


Figure 3

TEST CIRCUITS

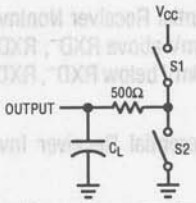


Figure 4

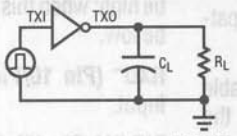


Figure 5

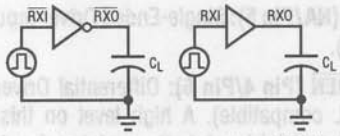


Figure 6

SWITCHING WAVEFORMS

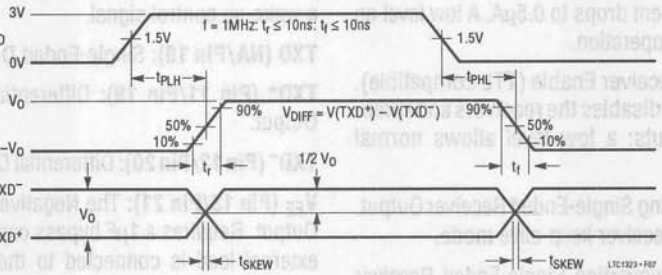


Figure 7. Differential Driver

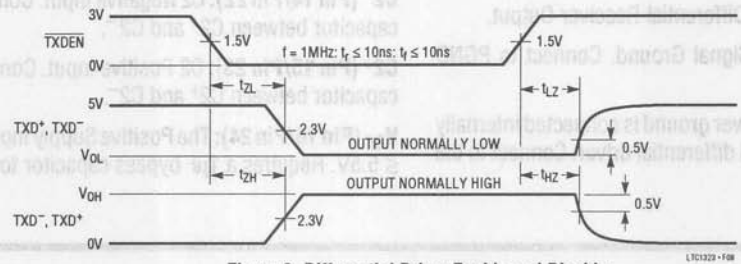


Figure 8. Differential Driver Enable and Disable

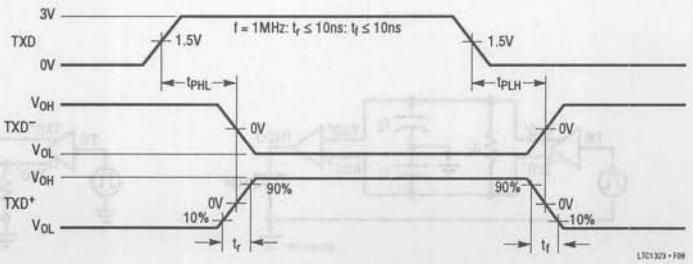


Figure 9. Differential Driver With Single-Ended Load

SWITCHING WAVEFORMS

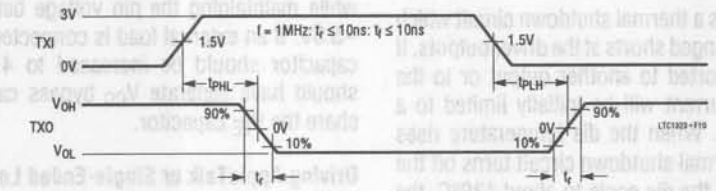


Figure 10. Single-Ended Driver

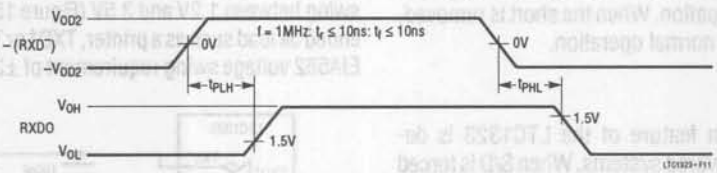


Figure 11. Differential Receiver

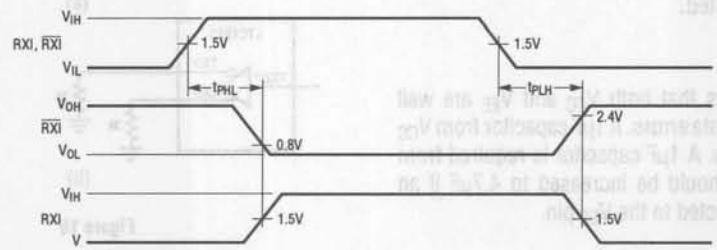


Figure 12. Single-Ended Receiver

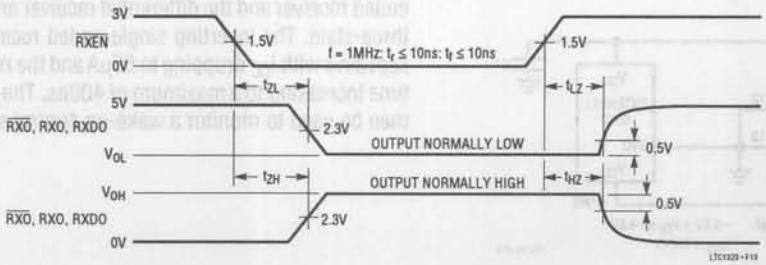


Figure 13. Receiver Enable and Disable

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APPLICATIONS INFORMATION

Thermal Shutdown Protection

The LTC1323 includes a thermal shutdown circuit which protects against prolonged shorts at the driver outputs. If a driver output is shorted to another output or to the power supply, the current will be initially limited to a maximum of 250mA. When the die temperature rises above 150°C, the thermal shutdown circuit turns off the driver outputs. When the die cools to about 130°C, the outputs re-enable. If the short still exists, the part will heat again and the cycle will repeat. This oscillation occurs at about 10Hz and prevents the part from being damaged by excessive power dissipation. When the short is removed, the part will return to normal operation.

Power Shutdown

The power shutdown feature of the LTC1323 is designed for battery-powered systems. When S/D is forced high the part enters shutdown mode. In shutdown the supply current typically drops from 2.4mA to 0.5µA, the charge pump turns off, and the driver and receiver outputs are three-stated.

Supply Bypassing

The LTC1323 requires that both V_{CC} and V_{EE} are well bypassed to prevent data errors. A 1µF capacitor from V_{CC} to ground is adequate. A 1µF capacitor is required from V_{EE} to ground and should be increased to 4.7µF if an external load is connected to the V_{EE} pin.

Driving an External Load from V_{EE}

An external load may be connected between ground and the V_{EE} pin as shown in Figure 14.

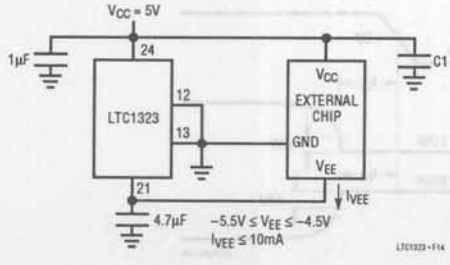


Figure 14

The LTC1323 V_{EE} pin will sink up to a maximum of 10mA while maintaining the pin voltage between –4.5V and –5.5V. If an external load is connected, the V_{EE} bypass capacitor should be increased to 4.7µF. Both chips should have separate V_{CC} bypass capacitors but can share the V_{EE} capacitor.

Driving AppleTalk or Single-Ended Loads

The differential driver is able to drive either an AppleTalk load or a single-ended load such as a printer. With a differential AppleTalk load, TXD⁺ and TXD⁻ will typically swing between 1.2V and 3.5V (Figure 15a). With a single-ended 3k load such as a printer, TXD⁺ or TXD⁻ will meet the EIA562 voltage swing requirement of ±3.7V (Figure 15b).

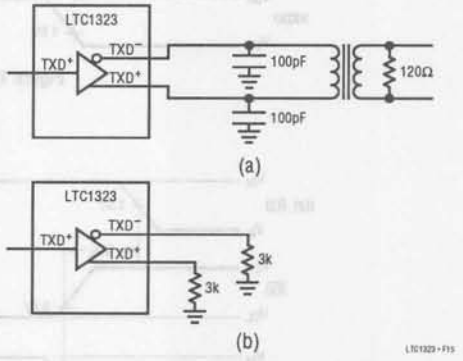


Figure 15

Receiver Keep-Alive Mode (24-Pin Package Only)

When $\overline{CPEN}$ is pulled high the charge pump is turned off and the outputs of both drivers, the noninverting single-ended receiver and the differential receiver are forced into three-state. The inverting single-ended receiver ($\overline{RXI}$) is kept alive with I_{CC} dropping to 65µA and the receiver delay time increasing to a maximum of 400ns. The receiver can then be used to monitor a wake-up control signal.

APPLICATIONS INFORMATION

EMI Filter

Most LocalTalk applications use an electromagnetic interference (EMI) filter consisting of a resistor-capacitor T network between each driver and receiver and the connector. Unfortunately, the resistors significantly attenuate the driver's signal applied to the cable. Because the LTC1323 uses a single supply driver, the resistor values should be reduced to 5Ω to 10Ω to insure enough voltage swing on the cable (Figure 16). In most applications, removing the resistors completely does not cause an increase in EMI as long as a shielded connector and cable are used. With the resistors removed the only DC load becomes the primary

Figure 16. EMI Filters

of the LocalTalk transformer. This will increase the DC standby current when the drivers are active, but does not adversely affect the drivers because they can handle a direct short circuit indefinitely. For maximum swing and EMI immunity, a ferrite bead and capacitor could be used.

INITIAL RELEASE
Final Electrical Specifications

LTC1325

Microprocessor-Controlled Battery Management System

June 1994

FEATURES

- Fast Charge Nickel Cadmium, Nickel Hydride or Lead Acid Batteries under µP Control
- Flexible Current Regulation:
  - Programmable 111kHz PWM Current Regulator with Built-In PFET Driver
  - PFET Current Gating for Use with External Current Regulator or Current Limited Transformer
- Discharge Mode
- Measures Battery Voltage, Battery Temperature and Ambient Temperature with Internal 10-Bit ADC
- Battery Voltage, Temperature and Charge Time Fault Protection
- Built-In Voltage Regulator and Programmable Battery Attenuator
- Easy to Use 3- or 4-Wire Serial µP Interface
- Accurate Gas Gauge Function
- Wide Supply Range: V_{DD} = 4.5V to 16V
- Can Charge Batteries Greater Than V_{DD}
- Can Charge Batteries from Charging Supplies Greater Than V_{DD}
- Digital Input Pins Are High Impedance in Shutdown Mode

APPLICATIONS

- System Integrated Battery Charger

DESCRIPTION

The LTC1325 provides the core of a flexible, cost-effective solution for a system integrated battery mangement system. The monolithic CMOS chip controls the fast charging of nickel cadmium, nickel hydride, or lead acid batteries under microprocessor control. The device features a programmable 111kHz PWM constant current source controller with built-in FET driver, 10-bit ADC, internal voltage regulator, discharge-before-charge controller, programmable battery voltage attenuator, and an easy to use serial interface.

The chip may operate in one of five modes: power shutdown, idle, discharge, charge, or gas gauge. In power shutdown the supply current drops to 30µA and in the idle mode, an ADC reading may be made without any switching noise affecting the accuracy of the measurement. In the discharge mode, the battery is discharged by an external transistor while the battery is being monitored by the LTC1325 for fault conditions. The charge mode is terminated by the µP while monitoring any combination of battery voltage and temperature, ambient temperature and charge time. The LTC1325 also monitors the battery for fault conditions before and during charging. In the gas gauge mode the LTC1325 allows the total charge leaving the battery to be calculated.

TYPICAL APPLICATION

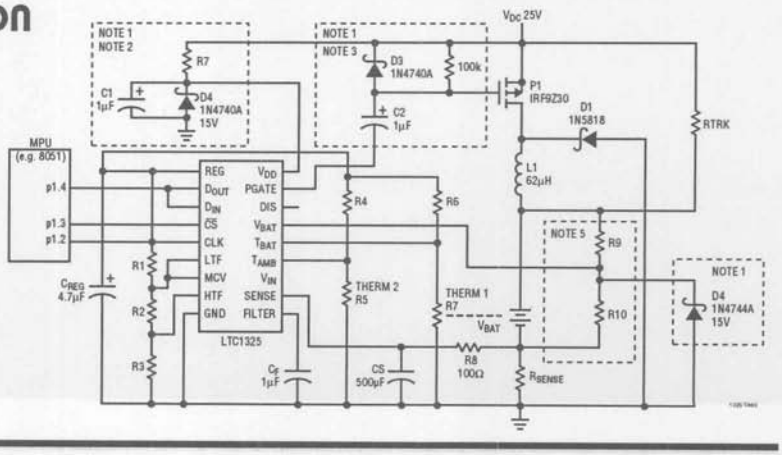
NOTE 1: NEEDED WHEN V_{DC} > 16V OR MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.

NOTE 2: REGULATOR. OMIT THIS BLOCK AND SHORT V_{DD} TO V_{DC} WHEN V_{DC} < 16V.

NOTE 3: LEVEL SHIFTER. OMIT THIS BLOCK AND SHORT PGATE TO P1 GATE WHEN V_{DC} < 16V.

NOTE 4: ZENER TO CLAMP V_{BAT} TO BELOW V_{DD}. OMIT WHEN V_{DC} > 16V.

NOTE 5: EXTERNAL BATTERY DIVIDER. NEEDED WHEN MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.

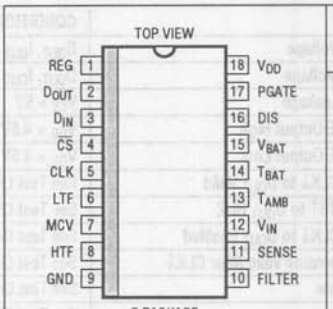


ABSOLUTE MAXIMUM RATINGS

(Note 1, 2)

V_{DD} to GND ..... −0.3V to 17V
All Other Pins ..... −0.3V to V_{DD} + 0.3V
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
18-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1325CN
LTC1325CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	V_{DD} Supply Voltage		4.5		16	V
I_{DD}	V_{DD} Supply Current	All TTL Inputs = 0V or 5V, No Load on REG		1200	2000	µA
I_{PD}	V_{DD} Supply Current	Power-Down Mode, All TTL Inputs = 0V or 5V		30	50	µA
V_{REG}	Regulator Output Voltage	No Load	3.037	3.072	3.107	V
LD_{REG}	Regulator Load Regulation	Sourcing Only, I_{REG} = 0mA to 2mA		−1	−5	mV/mA
LI_{REG}	Regulator Line Regulation	No Load, V_{DD} = 4.5V to 16V		−60	−100	µV/V
TC_{REG}	Regulator Output Tempco	No Load, 0°C < T_A < 70°C		50		ppm/°C
$V_{ERR(CHRG)}$	PWM Sense Voltage Error	V_{DAC} = 150mV		±3		%
		V_{DAC} = 150mV		±4		mV
		V_{DAC} = 50mV		±3		mV
		V_{DAC} = 30mV or 15mV		±2		mV
V_{HYST}	Fault Comparator Hysterisis	V_{HTF} = 1V, V_{EDV} = 0.9V, BATR		±20		mV
		V_{MCV} = V_{LTF} = 2V		±10		mV
V_{OS}	Fault Comparator Offset	V_{HTF} = 1V, V_{EDV} = 0.9V, BATR V_{MCV} = V_{LTF} = 2V		±50		mV
V_{BATR}	V_{BAT} for BATR = 1			100		mV
V_{BATP}	V_{BAT} for BATP = 1		V_{DD} − 1.8			V
V_{EDV}	Internal EDV Voltage		860	900	940	mV
V_{LTF}, V_{LTF}	LTF, MCV Voltage Range		1.6		2.8	V
V_{HTF}	HTF Voltage Range		0.5		1.3	V
$A_{(GG)}$	Gas Gauge Gain	−0.4V < V_{SENSE} < 0V		−4		
$V_{OS(GG)}$	Gas Gauge Offset	−0.4V < V_{SENSE} < 0V (Note 6)		±1		LSB
R_F	Internal Filter Resistor			1000		Ω
TOL_{BATD}	Battery Divider Tolerance	All Division Ratios		±2		%
V_{IL}	Input Low Voltage	CLK, $\overline{CS}$, D_{IN}	0.8	1.3		V
V_{IH}	Input High Voltage	CLK, $\overline{CS}$, D_{IN}		1.7	2.4	V
I_{IL}	Low Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 0V	−2.5		2.5	µA
I_{IH}	High Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 5V	−2.5		2.5	µA

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ELECTRICAL CHARACTERISTICS

V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	D_{OUT}, I_{OUT} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	D_{OUT}, I_{OUT} = –1.6mA	2.4			V
I_{OZ}	Hi-Z Output Leakage	$V_{\overline{CS}}$ = 5V			±10	µA
V_{OHFET}	DIS or PGATE Output High	V_{DD} = 4.5V to 16V	V_{DD} – 0.05			V
V_{OLFET}	DIS or PGATE Output Low	V_{DD} = 4.5V to 16V			0.05	V
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Valid	See Test Circuits			600	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits			450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits			400	ns
t_{hDO}	Time D_{OUT} Remains Valid After CLK↓	See Test Circuits		30		ns
t_{rDOUT}	D_{OUT} Rise Time	See Test Circuits			250	ns
t_{fDOUT}	D_{OUT} Fall Time	See Test Circuits			100	ns
f_{CLK}	Serial I/O Clock Frequency	CLK Pin	25		500	kHz
t_{rPGATE}	PGATE Rise Time	C_{LOAD} = 1500pF			120	ns
t_{fPGATE}	PGATE Fall Time	C_{LOAD} = 1500pF			120	ns
f_{OSC}	Internal Oscillator Frequency	Charge Mode, Fail-Safes Disabled	95	112	130	kHz
A/D Converter						
	Offset Error	V_{IN} Channel (Note 3)			±2	LSB
	Linearity Error	V_{IN} Channel (Notes 3, 4)		±0.5		LSB
	Full-Scale Error	V_{IN} Channel (Note 3)		±1		LSB
	On-Channel Leakage	V_{IN} Channel ON Only (Notes 3, 5)			±10	µA
	Off-Channel Leakage	V_{IN} Channel OFF (Notes 3, 5)			±10	µA

RECOMMENDED CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{hDI}	Hold Time, D_{IN} After CLK↑		150			ns
$t_{dsu\overline{CS}}$	Setup Time, $\overline{CS}$ Before First CLK↑		1			µs
t_{dsuDI}	Setup Time, D_{IN} Stable Before First CLK↑		400			ns
t_{WHCLK}	CLK High Time		0.8			µs
t_{WLCLK}	CLK Low Time		1			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfers		1			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transefer	MSBF = 1 MSBF = 0	43 52			CLK Cycles CLK Cycles

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to the GND pin.

Note 3: V_{REG} = 3.072mV ±20mV, CLK = 500kHz, unless otherwise stated.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 5: Channel leakage is measured after channel selection.

Note 6: Gas gauge offset excludes A/D offset error.

PIN FUNCTIONS

REG (Pin 1): Internal Regulator Output. The regulator provides a steady 3.072V to the internal analog circuitry and provides a temperature stable reference voltage for generating MCV, HTF, LTF and thermistor bias voltages with external resistors. Requires a 4.7µF or greater bypass capacitor to ground.

D_{OUT} (Pin 2): TTL Data Output Signal for the Serial Interface. D_{OUT} and D_{IN} may be tied together to form a 3-wire interface, or remain separated to form a 4-wire interface. Data is transmitted on the falling edge of CLK (pin 5).

D_{IN} (Pin 3): TTL Data Input Signal for the Serial Interface. The data is latched into the chip on the rising edge of the CLK (pin 5).

$\overline{CS}$ (Pin 4): TTL Chip Select Signal for the Serial Interface.

CLK (Pin 5): TTL Clock for the Serial Interface.

LTF (Pin 6): Minimum Allowable Battery Temperature Analog Input. LTF may be generated by a resistive divider between REG (pin 1) and ground.

MCV (Pin 7): Maximum Allowable Cell Voltage Analog Input. MCV may be generated by a resistive divider between REG (pin 1) and ground.

HTF (Pin 8): Maximum Allowable Battery Temperature Analog Input. HTF may be generated by a resistive divider between REG (pin 1) and ground.

GND (Pin 9): Ground

FILTER (Pin 10): The external filter capacitor C_F is connected to this pin. The filter capacitor is connected to the output of the internal resistive divider across the battery to reduce the switching noise while charging. In the gas gauge mode, C_F along with an internal R_F = 1k form a lowpass filter to average the voltage across the sense resistor.

SENSE (Pin 11): The Sense pin controls the switching of the 111kHz PWM constant current source in the charging mode. The Sense pin is connected to an external sense resistor R_{SENSE} and the negative side of the battery. The charging loop forces the average voltage at the Sense pin to equal a programmable internal reference voltage V_{DAC}. The battery charging current is equal to V_{DAC}/R_{SENSE}.

In the gas gauge mode the voltage across the Sense pin is filtered by an RC network (R_F and C_F), amplified by an inverting gain of 4, then multiplexed to the ADC so the average discharge current through the battery may be measured, and the total charge leaving the battery calculated.

V_{IN} (Pin 12): General Purpose ADC Input.

T_{AMB} (Pin 13): Ambient Temperature Input. Connect to an external thermistor network. Tie to REG if not used. May be used as another general purpose ADC input.

T_{BAT} (Pin 14): Battery Temperature Input. Connect to an external NTC thermistor network. Tie to REG if not used.

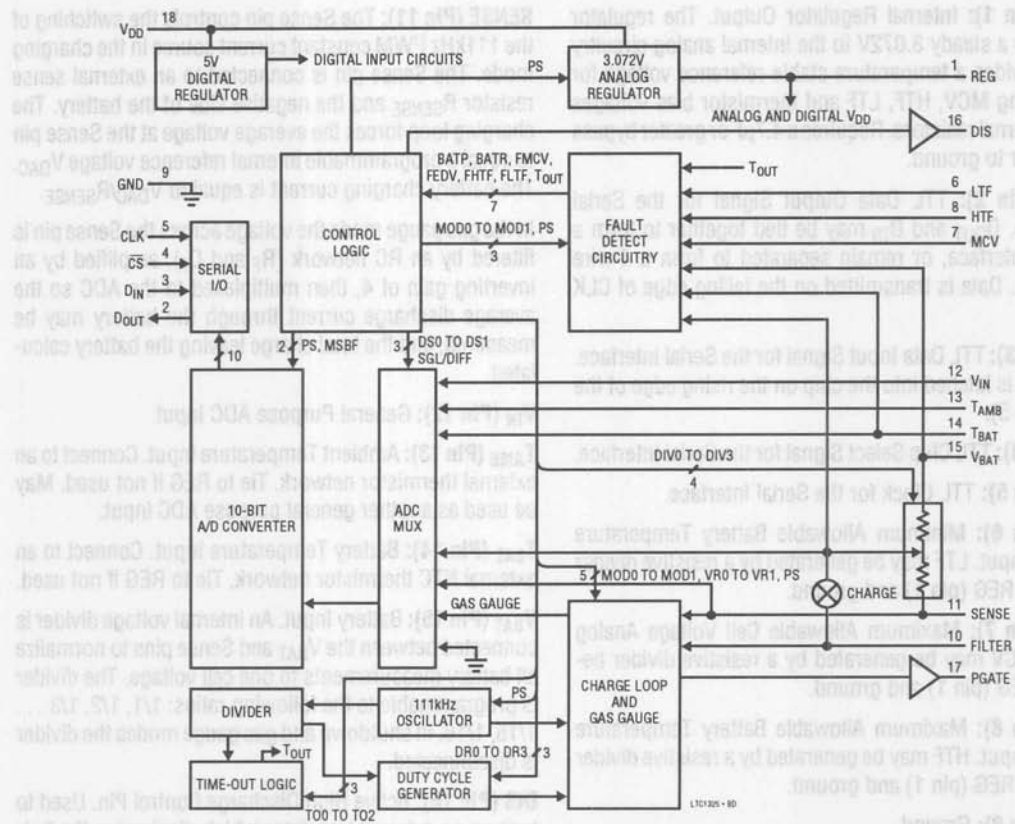
V_{BAT} (Pin 15): Battery Input. An internal voltage divider is connected between the V_{BAT} and Sense pins to normalize all battery measurements to one cell voltage. The divider is programmable to the following ratios: 1/1, 1/2, 1/3 . . . 1/15, 1/16. In shutdown and gas gauge modes the divider is disconnected.

DIS (Pin 16): Active High Discharge Control Pin. Used to turn on an external transistor which discharges the battery.

PGATE (Pin 17): FET Driver Output. Swings from GND to V_{DD}.

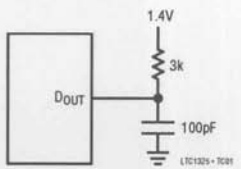
V_{DD} (Pin 18): Positive Supply Voltage. 4.5V < V_{DD} < 16V.

BLOCK DIAGRAM

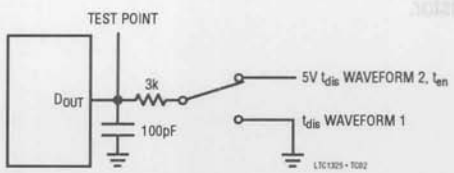


TEST CIRCUITS

Load Circuit for t_{dDO}, t_r and t_f

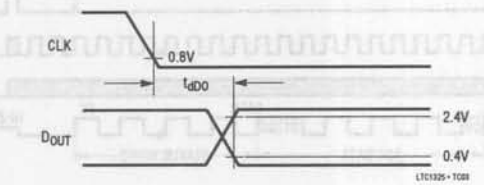


Load Circuit for t_{dis} and t_{en}

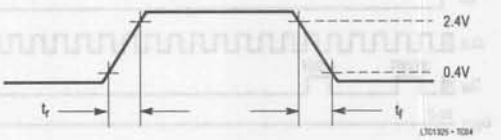


TEST CIRCUITS

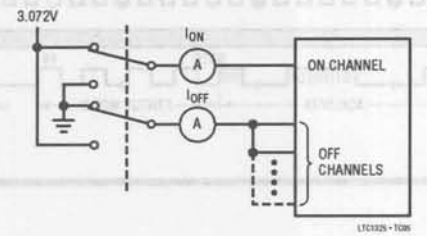
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



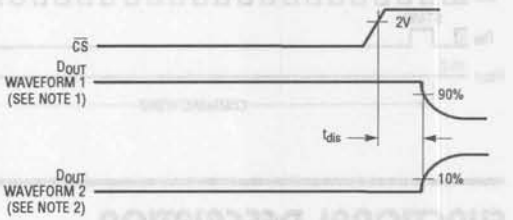
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



On and Off Channel Leakage



Voltage Waveforms for t_{dis}

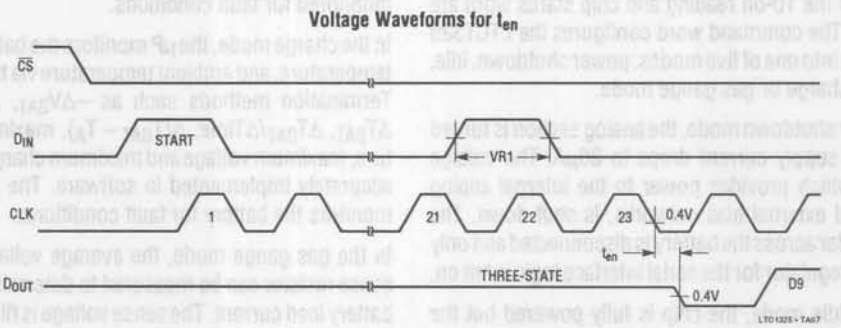


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$.

LTC1325 • TC06

Voltage Waveforms for t_{en}



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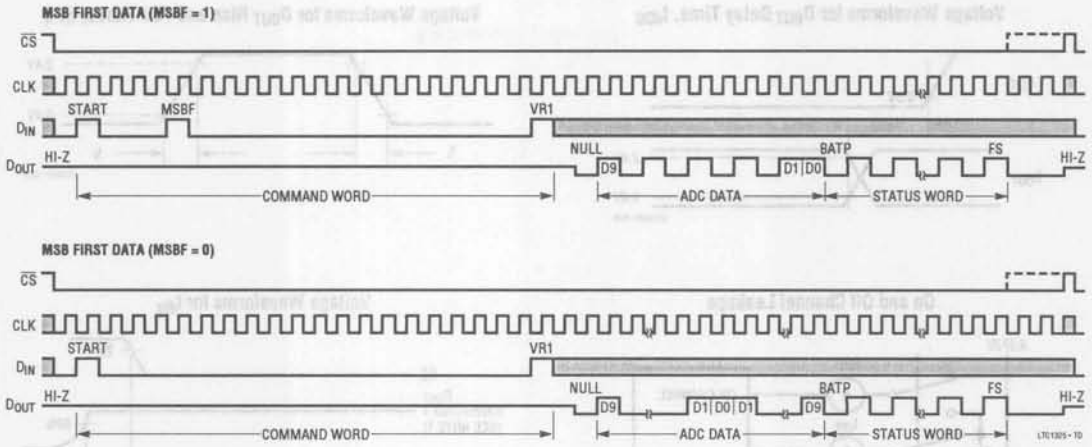
TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

During normal operation, a command word is shifted into the chip via the serial interface, then an ADC measurement is made and the 10-bit reading and chip status word are shifted out. The command word configures the LTC1325 and forces it into one of five modes: power shutdown, idle, discharge, charge or gas gauge mode.

In the power shutdown mode, the analog section is turned off and the supply current drops to 30μA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and only the voltage regulator for the serial interface logic is left on.

During the idle mode, the chip is fully powered but the discharge, charge, and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, allowing the charging loop to turn off and settle while the remainder of the command word is being shifted in.

During the discharge mode, the battery is discharged by an external transistor and series resistor. The battery is monitored for fault conditions.

In the charge mode, the μP monitors the battery's voltage, temperature, and ambient temperature via the 10-bit ADC. Termination methods such as $-\Delta V_{BAT}$, $\Delta V_{BAT}/\Delta Time$, ΔT_{BAT}, $\Delta T_{BAT}/\Delta Time$, $\Delta(T_{BAT} - T_A)$, maximum temperature, maximum voltage and maximum charge time may be accurately implemented in software. The LTC1325 also monitors the battery for fault conditions.

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The sense voltage is filtered by an RC circuit, multiplied by an inverting gain of four, then converted by the ADC. The μP can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The RC circuit consists of an internal 1k resistor R_F and an external capacitor C_F connected to the Filter pin.

FUNCTIONAL DESCRIPTION

COMMAND WORD

The command word is 22 bits long and contains all the information needed to configure and control the chip. On power-up all bits are cleared to logical "0."

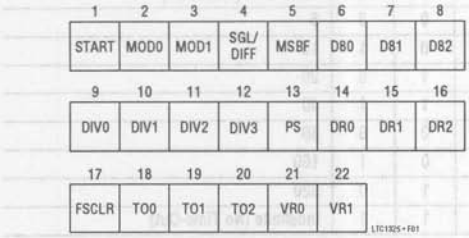


Figure 1. Command Word

Bit 1: Start Bit (Start)

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeros which precede this logical one will be ignored. After the start bit is received, the remaining bits of the command word will be clocked in.

START	DESCRIPTION
0	Wait
1	Start Reading Bits

Bits 2 and 3: Mode Select (MOD0 and MOD1)

The two mode bits determine which of four modes the chip will be in: idle, discharge, charge, or gas gauge.

MOD1	MOD0	DESCRIPTION
0	0	Idle
0	1	Discharge
1	0	Charge
1	1	Gas Gauge

Bit 4: Single-Ended Differential Conversion (SGL/DIFF)

SGL/DIFF determines whether the ADC makes a single-ended measurement with respect to ground or a differential measurement with respect to the Sense pin.

SGL/DIFF	DESCRIPTION
0	Single-Ended ADC Conversion
1	Differential ADC Conversion (with respect to Sense)

Bit 5: MSB-First/LSB-First (MSBF)

The ADC data is programmed for MSB-first or LSB-first sequence using the MSBF bit. See Serial I/O description for details.

MSBF	DESCRIPTION
0	LSB-First Data Follows MSB-First Data
1	MSB-First Data Only

Bits 6 to 8: ADC Data Input Select (DS0 to DS2)

DS0, DS1 and DS2 select which circuit is connected to the ADC input. Do not use unlisted combinations.

DS2	DS1	DS0	DESCRIPTION
0	0	0	Gas Gauge Output
0	0	1	T_{BAT} Pin
0	1	0	T_{AMB} Pin
0	1	1	Battery Cell Voltage, V_{CELL}
1	0	0	V_{IN} Pin

Bits 9 to 12: Battery Divider Ratio Select (DIV0 to DIV3)

DIV3, DIV2, DIV1 and DIV0 select the division ratio for the voltage divider across the battery.

DIV3	DIV0	DIV1	DIV0	DESCRIPTION
0	0	0	0	$(V_{BAT} - V_{SENSE})/1$
0	0	0	1	$(V_{BAT} - V_{SENSE})/2$
0	0	1	0	$(V_{BAT} - V_{SENSE})/3$
0	0	1	1	$(V_{BAT} - V_{SENSE})/4$
0	1	0	0	$(V_{BAT} - V_{SENSE})/5$
0	1	0	1	$(V_{BAT} - V_{SENSE})/6$
0	1	1	0	$(V_{BAT} - V_{SENSE})/7$
0	1	1	1	$(V_{BAT} - V_{SENSE})/8$
1	0	0	0	$(V_{BAT} - V_{SENSE})/9$
1	0	0	1	$(V_{BAT} - V_{SENSE})/10$
1	0	1	0	$(V_{BAT} - V_{SENSE})/11$
1	0	1	1	$(V_{BAT} - V_{SENSE})/12$
1	1	0	0	$(V_{BAT} - V_{SENSE})/13$
1	1	0	1	$(V_{BAT} - V_{SENSE})/14$
1	1	1	0	$(V_{BAT} - V_{SENSE})/15$
1	1	1	1	$(V_{BAT} - V_{SENSE})/16$

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FUNCTIONAL DESCRIPTION

Bit 13: Power Shutdown (PS)

PS selects between the normal operating mode, or the shutdown mode.

PS	DESCRIPTION
0	Normal Operation
1	Shutdown All Circuits Except Digital Inputs

Bits 14 to 16: Duty Ratio Select (DR0 to DR2)

DR2, DR1 and DR0 select the duty cycle of the charging loop. The last three selections place the chip into a test mode and should not be used.

DR2	DR1	DR0	DESCRIPTION
0	0	0	1/16
0	0	1	1/8
0	1	0	1/4
0	1	1	1/2
1	0	0	1
1	0	1	Test Mode 1
1	1	0	Test Mode 2
1	1	1	Test Mode 3

Bit 17: Fail-Safe Latch Clear (FSCLR)

When FSCLR bit is set to one, the internal fail-safe timer is reset to 0, and the fail-safe latches are reset. FSCLR is automatically reset to 0 when $\overline{CS}$ goes high.

FSCLR	DESCRIPTION
0	No Action
1	Reset Fail-Safe Timer and Latches

Bits 18 to 20: Time-Out Period Select (TO0 to TO2)

TO2, TO1 and TO0 select the desired fail-safe time-out period. On power-up, the default time-out is 5 minutes.

TO2	TO1	TO0	TIME-OUT (MINUTES)
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	40
1	0	0	80
1	0	1	160
1	1	0	320
1	1	1	Indefinite (No Time-Out)

Bits 21 and 22: Charging Loop Reference Voltage Select (VR0 and VR1)

VR1 and VR0 select the desired reference voltage V_{CHRG} for the charging loop. The charging loop will force the average voltage at the Sense pin to be equal to V_{DAC}. The average charging current is V_{DAC}/R_{SENSE}.

VR1	VR0	V_{DAC} (mV)
0	0	15
0	1	30
1	0	50
1	1	150

STATUS WORD

The status word is 8 bits long and contains the status of the internal fail-safe circuits.

1	2	3	4	5	6	7	8
BATP	BATR	FMCV	FEDV	FHTF	FLTF	T_{OUT}	FS

LTC1325 • F02

Figure 2. Status Word

FUNCTIONAL DESCRIPTION

Bit 1: Battery Present (BATP)

The BATP bit indicates the presence of a battery. The bit is set to 1 when the voltage at the V_{BAT} pin falls 1.6V below V_{DD}.

BATP	CONDITIONS
0	$(V_{DD} - 1.8) < V_{BAT} < V_{DD}$
1	$V_{BAT} < (V_{DD} - 1.8)$

Bit 2: Battery Reversed (BATR) or Shorted

The BATR bit indicates when the battery is connected backwards or shorted. The bit is set when the battery cell voltage at the output of the battery divider V_{CELL} is below 100mV.

BATR	CONDITIONS
0	$V_{CELL} > 100mV$
1	$V_{CELL} < 100mV$

Bit 3: Maximum Cell Voltage (FMCV)

The MCV bit indicates when the battery cell voltage has exceeded the preset limit. The bit is set when V_{CELL} is greater than the voltage at the MCV pin.

FMCV	CONDITIONS
0	$V_{CELL} < V(MCV)$
1	$V_{CELL} > V(MCV)$

Bit 4: End Discharge Voltage (FEDV)

The EDV bit indicates when the battery cell voltage has dropped below an internally preset limit. The bit is set when the battery cell voltage at the output of the voltage divider V_{CELL} is less than 900mV.

FEDV	CONDITIONS
0	$V_{CELL} > 900mV$
1	$V_{CELL} < 900mV$

Bit 5: High Temperature Fault (FHTF)

The HTF bit indicates when the battery temperature is too high. Using a negative TC thermistor, the bit is set when the voltage at the T_{BAT} pin is less than the voltage at the HTF pin.

FHTF	CONDITIONS
0	$T_{BAT} > V(HTF)$
1	$T_{BAT} < V(HTF)$

Bit 6: Low Temperature Fault (FLTF)

The LTF bit indicates when the battery temperature is too low. Using a negative TC thermistor, the bit is set when the voltage at the TBAT pin is greater than the voltage at the LTF pin

FLTF	CONDITIONS
0	$T_{BAT} < V(LTF)$
1	$T_{BAT} > V(LTF)$

Bit 7: Time-Out (T_{OUT})

The T_{OUT} bit indicates that the battery charging time has exceeded the preset limit. The bit is set when the internal timer exceeds the limit set by the command bits TO0, TO1 and TO2.

T_{OUT}	CONDITIONS
0	No Time-Out Has Occurred
1	Time-Out Has Occurred

Bit 8: Fail-Safe Occurred (FS)

The FS bit indicates that one of the fault detection circuits halted the discharging or charging cycle. The bit is set when an EDV, LTF, HTF, or T_{OUT} fault occurs during discharge. During charging, the bit is set when a MCV, LTF, HTF, or T_{OUT} fault occurs. The bit is reset by the command word bit FSCLR.

FS	CONDITIONS
0	No Fail-Safe Has Occurred
1	Fail-Safe Has Occurred

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FUNCTIONAL DESCRIPTION

DETAILED DESCRIPTION

Fault Conditions

The LTC1325 monitors the battery for fault conditions before and during discharge and charge (See Figure 3). They include: battery removed/present (BATP), battery reversed/shorted (BATR), maximum cell voltage exceeded (MCV), minimum cell voltage exceeded (EDV), high temperature limit exceeded (HTF), low temperature limit exceeded (LTF), and time limit exceeded (T_{OUT}). When a fault condition occurs, the discharge and charge loops are disabled or prevented from turning on and the fail-safe bit (FS) is set. The chip is reset by shifting in a new command word with the fail-safe clear FSCLR bit set. The 8-bit status word contains the state of each fault condition.

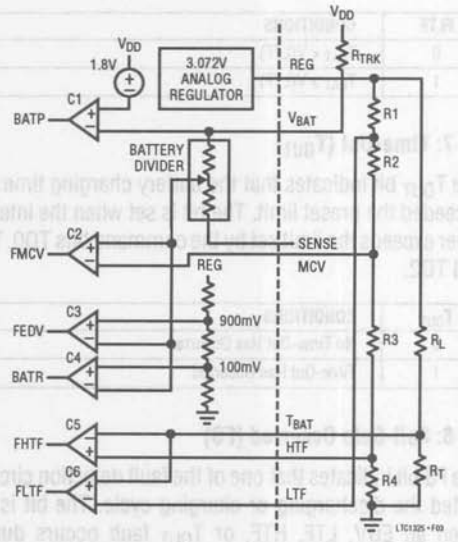


Figure 3. Fail-Safe or Fault Detection circuitry

Power Shutdown Mode

Command: MOD1 = X, MOD0 = X, PS = 1

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

In the power shutdown mode, the analog section is turned off and the supply current drops to 30µA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and the only circuit left on is the voltage regulator for the serial interface logic.

Idle Mode

Command: MOD1 = 0, MOD0 = 0, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

The chip enters the idle mode when the proper mode command bits are set and the power shutdown command bit is cleared. During the idle mode, the chip is fully powered, but the discharge, charge, and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, so that while the rest of the command word is being shifted in, the charging loop has time to settle before an ADC measurement is made.

FUNCTIONAL DESCRIPTION

Discharge Mode

Command: MOD1 = 0, MOD0 = 1, PS = 0

Status: BATP = 1, BATR = 0, FMCV = X, FEDV = 0, FHTF = 0, FLTF = 0, TOUT = 0

The chip enters the discharge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist, then the DIS pin is pulled up to V_{DD} by the internal driver. The DIS voltage is used to turn on an external transistor which discharges the battery through an external series resistor R_{DIS}.

Discharging will continue until a new command word is input to change the mode or a fault condition occurs.

Charge Mode

Command: MOD1 = 1, MOD0 = 0, PS = 0

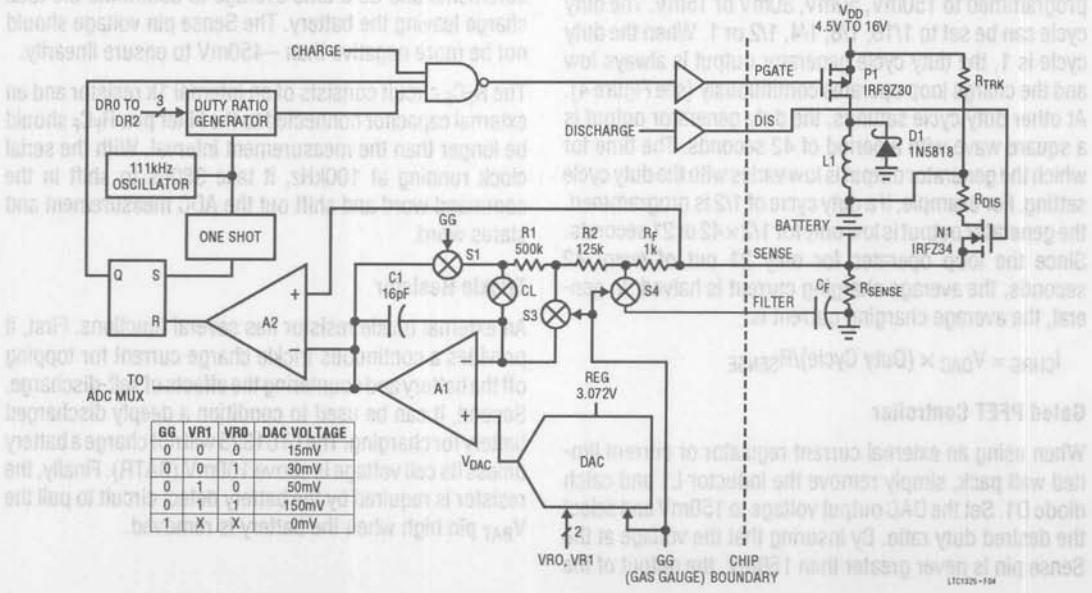
Status: BATP = 1, BATR = 0, FMCV = 0, FEDV = X, FHTF = 0, FLTF = 0, TOUT = 0

The chip enters the charge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist then charging can begin. Charging will continue until a new command word is input to change the mode or a fault condition occurs.

The charge current may be regulated by a programmable 111kHz PWM buck current regulator, or by using the PFET to gate an external current regulator or current limited transformer.

111kHz PWM Controller

The block diagram of the charging loop connected as a PWM buck current regulator is shown in Figure 4. The PWM may operate in either continuous or discontinuous mode. The loop forces the average voltage across the sense resistor to be equal to the voltage at the output of the DAC, so that the charging current becomes V_{DAC}/R_{SENSE}.



GG	VR1	VR0	DAC VOLTAGE
0	0	0	15mV
0	0	1	30mV
0	1	0	50mV
0	1	1	150mV
1	X	X	0mV

Figure 4. Charging Loop Block Diagram

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FUNCTIONAL DESCRIPTION

With switch S2 on and the others off, amplifier A1 along with C1, R1 and R2 are configured as an integrator with 16kHz bandwidth. The output of the integrator is the average difference between the voltage across the sense resistor and the DAC output voltage.

The rising edge of the oscillator waveform triggers the one shot which sets the flip-flop output high. This turns on the external PFET P1 by pulling its gate low via the FET driver. With P1 on, the current through the inductor L1 starts to rise as does the voltage across the sense resistor. When the voltage across the sense resistor is greater than the output of the integrator, comparator A2 changes state. This resets the flip-flop and P1 is turned off. Catch diode D1 clamps the drain of P1 one diode drop below ground when the inductor flies back and the current through the inductor starts to drop. The voltage across the sense resistor also drops and may reach zero and stay there until the next clock cycle begins.

The average charging current is set by the output of the DAC (V_{DAC}) and the duty cycle generator. V_{DAC} can be programmed to 150mV, 50mV, 30mV or 15mV. The duty cycle can be set to 1/16, 1/8, 1/4, 1/2 or 1. When the duty cycle is 1, the duty cycle generator output is always low and the charge loop operates continuously (see Figure 4). At other duty cycle settings, the duty generator output is a square wave with a period of 42 seconds. The time for which the generator output is low varies with the duty cycle setting. For example, if a duty cycle of 1/2 is programmed, the generator output is low only for 1/2×42 or 21 seconds. Since the loop operates for only 21 out of every 42 seconds, the average charging current is halved. In general, the average charging current is:

$$I_{CHRG} = V_{DAC} \times (\text{Duty Cycle})/R_{SENSE}$$

Gated PFET Controller

When using an external current regulator or current limited wall pack, simply remove the inductor L1 and catch diode D1. Set the DAC output voltage to 150mV and select the desired duty ratio. By insuring that the voltage at the Sense pin is never greater than 150mV, the output of the integrator A1 will saturate high, and the comparator A2 will never trip and turn the loop off. This can be achieved by removing the sense resistor and grounding the Sense pin or if the gas gauge is to be used, selecting R_{SENSE} so that $R_{SENSE}/I_{CHRG} < 150mV$.

Gas Gauge Mode

Command: MOD1 = 1, MOD0 = 1, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The output of the DAC is set to ground and switches S1, S3 and S4 are closed. A1 is configured as an inverting amplifier with R1 and R2 setting the gain to –4. The voltage across the sense resistor is filtered by an RC circuit (R_F, C_F) amplified by A1, then converted by the ADC.

The microprocessor can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The Sense pin voltage should not be more negative than –450mV to ensure linearity.

The R_FC_F circuit consists of an internal 1k resistor and an external capacitor connected to the Filter pin. R_FC_F should be longer than the measurement interval. With the serial clock running at 100kHz, it take 380µs to shift in the command word and shift out the ADC measurement and status word.

Trickle Resistor

An external trickle resistor has several functions. First, it provides a continuous trickle charge current for topping off the battery and countering the effects of self-discharge. Second, it can be used to condition a deeply discharged battery for charging. The LTC1325 will not charge a battery unless its cell voltage is above 100mV (BATR). Finally, the resistor is required by the battery detect circuit to pull the V_{BAT} pin high when the battery is removed.

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The LTC1325 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The clock CLK synchronizes the data transfer with each bit being transmitted on the falling edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1325 first receives input data and then transmits back the A/D conversion result and status word (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer if initiated by a falling chip select $\overline{CS}$ signal. After $\overline{CS}$ falls, the LTC1325 looks for a start bit on D_{IN}. The start bit is the first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low. The LTC1325 will ignore all leading zeros which precede this logical one. After the start bit is received, a 22-bit input word is shifted into the D_{IN} input which configures the LTC1325 and starts a conversion. After one null bit, the result of the conversion is output on the D_{OUT} pin followed by 8 status bits. At the end of the data exchange, $\overline{CS}$ should be brought high.

MSB-First/LSB-First (MSBF Control Bit)

The output data of the LTC1325 is programmed for MSB-first or LSB-first sequence using the MSFB control bit. When MSBF = 1, data will appear on D_{OUT} in MSB-first format. This is followed by the 8 status bits. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When MSBF = 0, LSB-first data will follow the MSB-first data. Regardless of the state of MSBF, the status bits are always shifted out in the same order (see Figure 2).

Accommodating Microprocessors with Different Word Lengths

The LTC1325 will fill zeros indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time D_{OUT} is disabled (three-stated). This makes for easy interfacing to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS). Any word length can be accommodated by the correct positioning of the start bit in the input word.

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1325 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate with the microprocessor. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1325 will take control of the dataline and drive it low after the 23rd falling CLK edge after the start bit is received. Therefore the processor port must be switched to an input before this happens to avoid a conflict.

Power-Up After Shutdown

When a control word with the PS bit set to one is written to the LTC1325, it enters shutdown mode in which the V_{DD} supply current is reduced to 30μA. In this mode the on-chip 3V regulator and all circuits powered off it are shut down. The only circuits that remain alive are D_{IN}, $\overline{CS}$ and CLK input buffers. To take the LTC1325 out from shutdown mode, a high to low edge must be applied to the $\overline{CS}$ pin. Either D_{IN} or CLK must be low when $\overline{CS}$ is low to prevent a false control word from being transmitted to the LTC1325. The 3V output decays with a time constant of 300ms with C_{REG} = 4.7μF. The microprocessor should wait three seconds before applying a wake-up edge to the $\overline{CS}$ pin to ensure proper power-up.

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APPLICATIONS INFORMATION

TEMPERATURE SENSING

NTC (Negative Temperature Coefficient) Thermistors

The simplest method to sense temperature (battery or ambient) with an NTC thermistor is to use a voltage divider powered by the REG pin. This divider consists of a load resistor R_L in series with a thermistor R_T as shown in Figure 3. For a given thermistor, there is a value of R_L which makes V_{DIV} (T) linear over a narrow but adequate temperature range. The easiest method (Inflection Point Method) to calculate R_L is to set the second temperature derivative of the divider output to 0. The equations relevant to this method are:

$$\frac{V_{DIV}(T)}{V_{REG}} = \frac{1}{\left(\frac{1+R_L}{R_T}\right)} = f(T) \quad (1)$$

$$\frac{R_T}{R_{TO}} = \exp\left[\beta \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \quad (2)$$

$$R_L = R_{TO} \times \frac{\beta - 2T_0}{\beta + 2T_0} \quad (3)$$

$$\beta = \left[T \times \frac{T_0}{T_0 - T}\right] \times \ln\left(\frac{R_T}{R_{TO}}\right) \quad (4)$$

$$\alpha = \frac{1}{R_T} \times \frac{dR_T}{dT} \quad (5)$$

$$\alpha = \frac{-\beta}{T^2} \quad (6)$$

$$\frac{dV_{DIV}}{dT} = V_{DIV}(T_0) \times \left(-\frac{-\beta}{2T_0{}^2} + \frac{1}{T_0}\right) \quad (7)$$

where,

V_{DIV} (T) is the output of the divider,

V_{REG} is the voltage at the REG pin (3.072V nominal),

R_T is the thermistor resistance at some temperature T,

R_{TO} is the thermistor resistance at some reference temperature T_0,

β is a constant dependent on thermistor material,

α is the temperature coefficient (in %/°C) of R_T at T_0, and

all temperatures are in °K (i.e., T°C + 273)

There are two assumptions in the derivation of the above equations. β is assumed to be constant and the temperature coefficient of R_L is small compared to that of the thermistor.

Most thermistor data sheets specify R_{TO}, β, R_T/R_{TO} ratios for two temperatures, α, and tolerances for β and R_{TO}. Given β, and R_{TO}, it is easy to calculate R_L from equation (3). Alternatively, β may be calculated from the R_T/R_{TO} ratio using equation (4) or from α, using equation (6).

As a numerical example, consider the Panasonic ERT-D2FHL103S thermistor which has the following characteristics:

1. R_T (25°C) = R_{TO} = 10k
2. $\alpha = -4.6\%/°C$ at $T_0 = 25°C$
3. Ratio $R_{25}/R_{50} = 2.9$

Using equation (4), and $R_{25}/R_{50} = 2.9$, $\beta = (323 \times 298) \times \ln(2.9)/(298-323) = 4099K$. Alternatively, using equation (6) and $\alpha = -4.6\%/°C$, $\beta = -(-0.046) \times (298)^2 = 4085K$.

Both values of β are close to each other. Substituting β = 4085K into equation (3) gives $R_L = 10k \times [4085 - (2 \times 298)]/[4085 + (2 \times 298)] = 7.45k$. The nearest 1% resistor value is 7.5k. Figure 5 shows a plot of $V_{DIV}(T)$ measured at various temperatures for this thermistor with a 7.5k R_L.

APPLICATIONS INFORMATION

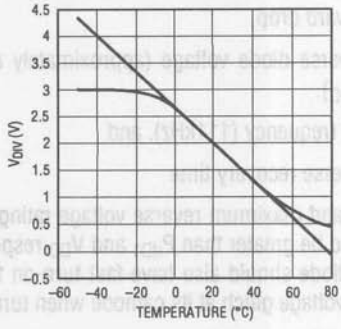

Figure 5. ERT-D2FHL103S Divider

There are two methods of calculating battery or ambient temperature from ADC readings of the T_{BAT} or T_{AMB} channels. The first method is to store the $V_{DIV}(T)$ vs T curve as a lookup table. The second method is to use a straight line approximation. The equation of this line may be calculated from the slope dV_{DIV}/dT at T_O [see equation (7)] and assuming that the line passes through the point $[T_O, V_{DIV}(T_O)]$ on the curve. For the ERT-D2FHL103S, the slope is minus 34mV/°C and the equation of the line is $T = [2.605 - V_{DIV}(T)]/0.034$. The straight line approximation is accurate to within 2°C over a temperature range of 5°C to 45°C, assuming a 3% β and 10% R_{TO} tolerances.

PTC (Positive Temperature Coefficient) Thermistors

Positive Temperature Coefficient (PTC) thermistors may be used in battery chargers that do not require accurate temperature measurements. The resistance vs temperature characteristics of PTC exhibits a sharp increase at a selectable switch temperature T_S. This sharp change is exploited in chargers which use TCO (Temperature Cutoff) or ΔTCO (Difference between battery and ambient temperature). With TCO termination, a voltage divider consisting of a PTC and a low temperature coefficient load resistor is connected between REG and GND with the top end of the PTC at REG. The PTC is mounted on the battery to sense its temperature. The divider output is tied to T_{BAT}. When the switch temperature is reached, the PTC resistance increases sharply causing T_{BAT} to fall below HTF. This causes an HTF fault and charging is terminated. To implement ΔTCO termination the load resistor can be replaced by a matching PTC and the divider now responds to differences between battery and ambient temperature. With both TCO and ΔTCO terminations, the position of the battery temperature PTC can be swapped with the load resistor or ambient temperature PTC. In both cases, an LTF fault terminates charge when the trip point is reached.

HARDWARE DESIGN PROCEDURE

This section discusses the considerations in selecting each component of a simple battery charger (see Figures 3 and 4).

1. R_{SENSE}

There are three factors in selecting R_{SENSE}:

a. LTC1325 V_{REF} and Duty Ratio Settings

b. Sense Resistor Dissipation

c. $I_{LOAD} \times R_{SENSE} < -450mV$ for Gas Gauge Linearity

The LTC1325 has five duty ratio and four V_{REF} settings giving 20 possible charge rates (for a given value of R_{SENSE}) as shown in the following table. For any combination of V_{DAC} and duty ratio, the average charging current is given by:

$$AVG\ I_{CHRG} = V_{DAC} \times (Duty\ Ratio)/R_{SENSE}$$

	DUTY RATIO				
V_{REF}	1	1/2	1/4	1/8	1/16
150mV (1)	1	1/2	1/4	1/8	1/16
50mV (1/3)	1/3	1/6	1/12	1/24	1/48
30mV (1/5)	1/5	1/10	1/20	1/40	1/80
15mV (1/10)	1/10	1/20	1/40	1/80	1/160

Note that in the table, the 150mV, 100% duty ratio entry is given a weighting of 1. For a battery charged at 1C rate with V_{REF} of 150mV and 100% duty ratio, the charge rate (in C-units) for other V_{REF} and duty ratio combinations can be read straight off the table. For a battery charged at 4C rate at 150mV, 100% duty ratio, all entries should be multiplied by 4 and so on. In general, V_{REF} and duty ratio settings are changed by the microprocessor to charge batteries of different capacities or to alter charge rates when charging the same battery in several stages. For best accuracy, V_{REF} should be set to 150mV where possible.

APPLICATIONS INFORMATION

The power dissipation of the sense resistor varies between charge, discharge and gas gauge modes and should be calculated for all three modes. Typically, dissipation is higher in discharge and gas gauge modes since batteries can deliver higher currents than they can be charged with.

In gas gauge mode, the load current supplied by the battery should not exceed $450mV/R_{SENSE}$ for the gas gauge to remain linear in response. R_{SENSE} should be low enough to ensure that $I_{LOAD} \times R_{SENSE}$ does not fall below ground by 1 diode drop.

2. V_{DD} Supply

The minimum V_{DD} supply must be greater than the end-of-charge voltage V_{EC} times the number of cells (n) in the battery plus drops across the on-resistance of the PFET, inductor (V_L), battery internal resistance R_{INT} and sense resistor R_{SENSE}.

$$\text{Min } V_{DD} = I_{CHRG} \times [R_{DS(ON)}(P1) + R_{SENSE} + n \times R_{INT}] + n \times V_{EC} + V_L$$

Assuming $V_{EC} = 2V$, the LTC1325 will charge up to 8 cells with a 16V supply. For a higher number of cells, an external level shifter and regulator are needed.

3. Inductor L

To minimize losses, the inductor should have low winding resistance. It should be able to handle expected peak charging currents without saturation. If the inductor saturates, the charging current is limited only by the total PFET $R_{DS(ON)}$, inductor winding resistance, R_{SENSE} and V_{DD} source resistance. This fault current may be high enough to damage the battery or cause the maximum power ratings of the PFET, inductor or R_{SENSE} to be exceeded.

4. Catch Diode D1

The catch diode should have a low forward drop and fast reverse recovery time to minimize power dissipation. Total power loss is given by:

$$P_{dD1} = V_F \times I_F + V_R \times f \times t_{RR} \times I_F'$$

where

I_F = forward diode current,

I_F' = forward diode current just prior to turn-off,

V_F = forward drop,

V_R = reverse diode voltage (approximately equal to V_{DD}),

f = PWM frequency (111kHz), and

t_{RR} = reverse recovery time

The power and maximum reverse voltage ratings of the diode should be greater than P_{dD1} and V_{DD} respectively. The catch diode should also have fast turn-on times to reduce the voltage glitch at its cathode when turning on.

Schottky diodes have fast switching times and low forward drops and are recommended for D1.

5. Trickle Resistor R_{TRK}

R_{TRK} sets the desired trickle current in the battery to compensate for self-discharge which is in the order 1% and 2% of capacity per day for NiCd and NiMH batteries respectively. Trickle charge rates are typically in the C/30 to C/50 range, where C is battery capacity.

$$I_{TRK} = (V_{DD} - V_{BAT})/R_{TRK}$$

where V_{BAT} is the voltage of a full charged battery. Note that I_{TRK} varies as the battery is being charged.

6. Thermistor R_{THERM} and Load R_L

The total resistance of the thermistor network should be greater than 30k at the high temperature extreme to minimize effects of load regulation (see REG pin loading).

7. Fault Setting Resistors R1, R2, R3 and R4

The voltage levels at the LTF, HTF and MCV pins are tapped from a resistor divider powered by the REG pin. The voltage levels are selected taking into account:

a. Manufacturer Recommended Temperature and Voltage limits,

b. Loading on the REG Pin (< 2mA)

c. Input Voltage Ranges of the LTF, HTF and MCV Comparators:

$1.6V < V_{LTF}, V_{MCV} < 2.8V$ and
$0.5V < V_{HTF} < 1.3V$

d. Thermistor Divider Temperature Curve

APPLICATIONS INFORMATION

Typical temperature limits for both NiCd and NiMH batteries are shown below.

BATTERY TYPE	DISCHARGE TEMP RANGE (°C)		DISCHARGE TEMP RANGE (°C)	
	MIN	MAX	MIN	MAX
Standard	–20	45/50	0	45/50
Quick	–20	45/50	10	45/50
Fast or Rapid	–20	45/50	15	45/50
Trickle	–20	45/50	0	45/50

Note that the discharge limits are wider than the charge limits. To prolong battery life, manufacturers generally recommend discharge temperatures that are similar to the charge limits. For this reason, the LTC1325 recognizes the same LTF and HTF limits in both charge and discharge modes. MCV should be set just above the charging voltage per cell given in battery specifications. The voltage at the LTF and HTF pins should be set to correspond to narrowest temperature range. These are typically 15°C and 45°C. The corresponding voltages may be read from the thermistor divider temperature curve such as that shown in Figure 5. For this thermistor, it works out to be about for 2.12V for LTF and for 1.13V for HTF. The MCV may be conveniently tied to LTF since MCV is typically 2V. If desired, external analog switches under microprocessor control may be used to vary the LTF, HTF and MCV voltages between modes or for different charge rates. The values of R1, R2, R3 and R4 in Figure 3 can be calculated from the following equations:

$$R4 = V(HTF) \times RE/V_{REG}$$

$$R3 = V(MCV) \times RE - R4$$

$$R2 = V(LTF) \times RE - (R3 + R4)$$

$$R1 = RE - (R2 + R3 + R4)$$

where RE = R1 + R2 + R3 + R4 is chosen to minimize loading on the REG pin. A minimum value of 30k is recommended. Note that V(LTF) is assumed to be greater than V(MCV). If this is not the case, V(LTF) and V(MCV) in the above equations should be swapped. If the MCV and LTF pins are shorted to the same point, R2 should be set to 0.

8. REG Pin Loading

The 3.072V regulator has a load regulation specification of –5mV/mA. Since the ADC uses the same regulator as reference, it is desirable to reduce loading effects on the REG pin especially over temperature. Thermistors with R_{TO} values of at least 10k at 25°C are recommended. At 50°C, the thermistor resistance could drop by a factor of 3 from its value at 25°C. R_L is chosen as explained in the section on Temperature Sensing. The temperature coefficient of R_L is not critical since the thermistor tempco dominates the sensing circuit.

9. R_{DIS}

R_{DIS} is selected to limit the discharge current to a value within the battery discharge specifications and must have a power rating above $I_{DIS}^2 \times R_{DIS}$ where:

$$I_{DIS} = V_{BAT}/[R_{DIS} + R_{DS(ON)}(N1)]$$

10. PFET(P1) and NFET(N1)

For operation of the charge and discharge loops, $|V_{GS}| < V_{DD}$ since the PGATE and DIS pins swing between 0 and V_{DD}. $|V_{GS}| \ll V_{DD}$ to minimize power dissipation. The power ratings of P1 and N1 should be above $I_{CHRG}^2 \times R_{DS(ON)}$(P1)and $I_{DIS}^2 \times R_{DS(ON)}$(N1) respectively. $V_{DS(MAX)}$ should be above V_{DD}.

Charging From Supplies Above 16V

In many applications, the charging supply is greater than the 16V maximum V_{DD} rating of the LTC1325. The LTC1325 can easily be adapted to charge the batteries from a charging supply (V_{DC}) above 16V by adding 3 external sub-circuits:

1) A regulator to drop V_{DC} down to within the supply range of the LTC1325.
2) A level shifter between the PGATE and the gate of the PFET, P1, to ensure that P1 can be completely turned offwhen PGATE rises to V_{DD}.
3) A voltage clamp on the V_{BAT} pin to prevent R_{TRK} from pulling V_{BAT} above V_{DD}.

The Typical Application circuit on page 1 shows low cost implementations of all 3 sub-circuits. C1, R7 and D4 generate a 15V V_{DD} for the LTC1325. D3 and C2 form a level shifter. The zener D3 is chosen to clamp the source-gate voltage of the PFET to within the maximum gate-source voltage rating of the latter. Finally, D5 clamps V_{BAT} to 15V.

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APPLICATIONS INFORMATION

Charging Batteries With Voltages above 16V

To charge a battery with a maximum (fully charged) voltage of above 16V, the charging supply V_{DC} must be above 16V. Thus the charger will need the regulator, level shifter and clamp mentioned in the previous section. In addition, an external battery divider must be added to limit the voltage at the V_{BAT} pin to less than V_{DD}. This is shown in the Typical Application circuit on page 1. The resistors R9 and R10 are selected to divide the battery voltage by the number of cells in the battery and the battery divider internal to the LTC1325 is set to divide-by-1. The external divider prevents V_{BAT} from ever rising to V_{DD} and this causes the B_{ATP} (Battery Present Flag) to be high regardless of whether the battery is physically present or not. This does not affect the other operations of the LTC1325.

SOFTWARE DESIGN

A general charging algorithm consists of the following stages:

Discharge Before Charge

Fast Charge

Top Off Charge

Trickle Charge

Under some operating conditions, NiCd and NiMH batteries may not provide full capacity. Examples are repeated shallow charge and discharge cycles which causes the "memory effect" in NiCd batteries and long term storage at high temperatures. In order to restore full capacity (battery conditioning), these batteries have to be subjected to several deep discharge/charge cycles which will be provided by repetitions of the above algorithm.

Figure 6 shows a simplified flowchart of a charging algorithm. In practice, this flowchart has to be augmented to take into account the occurrence of fail-safes at any point in the algorithm. For example, the battery temperature could rise above HTF during discharging or charging. Table 1 shows the corresponding command word the microprocessor sends to the LTC1325 in each step of the flowchart. General programming notes are as follows:

1. The start bit is always high.
2. The SGL/DIFF bit is generally set to low so that the ADC makes conversions with respect to ground.
3. The MSBF bit is set depending on whether the microprocessor clocks in serial data with MSB- or LSB-first.
4. The DS0 to DS2 bits can be anything except when entering idle mode or when requesting for ADC readings. In these cases, DS0 to DS2 are set to select the desired reading: T_{BAT}, V_{CELL} or T_{AMB}.
5. The PS bit should always be 0 so that the LTC1325 does not go into shutdown mode.
6. The DR0 to DR2 should not select any of the test modes. It may assume different settings between Fast charge and Top Off charge in order to alter the charging current.
7. The FSCLR bit should be set to 1 to clear any faults and reset the timer when starting Discharge, Fast charge or Top Off. The status bits that the LTC1325 returns during the same I/O operation (that FSCLR is set to 1) should be checked to determine if faults were indeed cleared, i.e., discharging or charging has begun. This is not shown in the simplified flowchart of Figure 6. For commands other than the START commands, FSCLR should be set to 0 so as not to reset the timer.
8. The TO0 to TO2 bits should all be set to 1 in discharge mode to ensure discharge does not end prematurely due to a time-out fault. During Fast charge or Top Off charge, these bits are set to a value suitable for the charge rate used. For example, if the charge rate is 1C, the time-out period should be set to 80 minutes.
9. In charge mode, the C_F capacitor filters the V_{CELL} node and sees a small ripple due to ripple at the Sense pin. Prior to taking an ADC reading, the LTC1325 is put in idle mode to minimize noise. The microprocessor should either disregard readings or wait for a second or so before taking a reading. This is to allow V_{CELL} to decay to the correct cell voltage. The worst case time constant is $150k\Omega \times C_F$.
10. Prior to the first START command, the battery divider setting may be incorrect so that C_F may charge to a voltage that causes EDV, BATR or MCV faults. The worst case time constant is as in (9). The microprocessor should check faults during the transmission of a START command and resend the START command again when C_F has been given enough time to charge up to the correct value.

APPLICATIONS INFORMATION

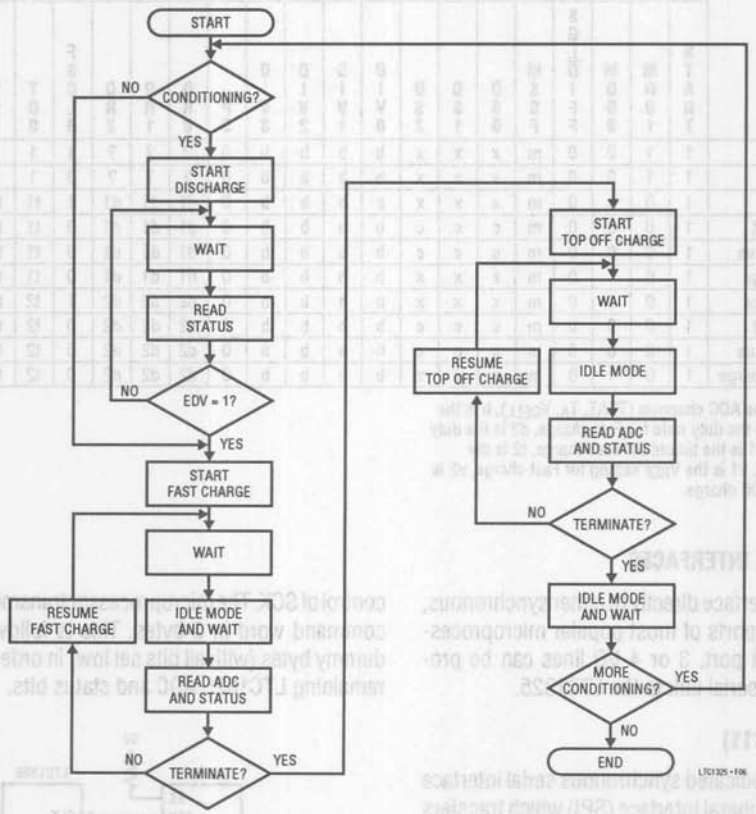

Figure 6. Simple Charging Algorithm

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APPLICATIONS INFORMATION

Table 1. Commands for Flowchart in Figure 6

		COMMAND WORD																				
NO	STEP	START	MOD1	MOD0	SGL/DIFF	MSBF	DS0	DS1	DS2	DIV0	DIV1	DIV2	DIV3	PS	DR0	DR1	DR2	FSCLR	TO0	TO1	TO2	VR0	VR1
1	Start Discharge	1	1	0	0	m	x	x	x	b	b	b	b	0	?	?	?	1	1	1	1	x	x
2	Read Status	1	1	0	0	m	x	x	x	b	b	b	b	0	?	?	?	0	1	1	1	x	x
3	Start Fast Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d1	d1	d1	1	t1	t1	t1	v1	v1
4	Idle Mode and Wait	1	0	0	0	m	c	c	c	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
5	Read ADC and Status	1	0	0	0	m	c	c	c	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
6	Resume Fast Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
7	Start Top Off Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d2	d2	d2	1	t2	t2	t2	v2	v2
8	Idle Mode and Wait	1	0	0	0	m	c	c	c	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2
9	Read ADC and Status	1	0	0	0	m	c	c	c	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2
10	Resume Top Off Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2

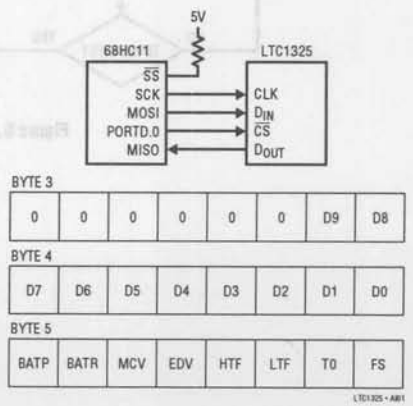
Note: c refers to one of the ADC channels (TBAT, T_A, V_{CELL}), b is the battery divider ratio, d1 is the duty ratio for Fast charge, d2 is the duty ratio for Top Off charge, t1 is the timout for Fast charge, t2 is the timout for Top Off charge, v1 is the V_{REF} setting for Fast charge, v2 is the V_{REF} setting for Top Off charge.

MICROPROCESSOR INTERFACES

The LTC1325 can interface directly to either synchronous, serial or parallel I/O ports of most popular microprocessors. With a parallel port, 3 or 4 I/O lines can be programmed to form a serial link to the LTC1325.

Motorola SPI (68HC11)

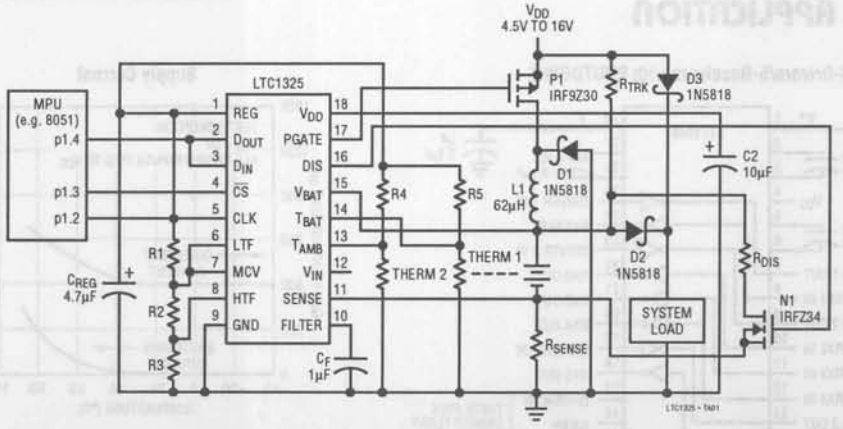
The 68HC11 has a dedicated synchronous serial interface called the Serial Peripheral Interface (SPI) which transfers data with MSB-first and in 8-bit increments. To communicate with this microprocessor, the LTC1325 MSBF control bit should be set to 1. The SPI has 4 lines: Master In Slave Out (MISO), Master Out Slave In (MOSI), Serial Clock (SCK) and Slave Select ($\overline{SS}$). The 68HC11 is configured as a Master by tying the $\overline{SS}$ line high. A control byte is written to the Serial Peripheral Control Register to select master mode, set baud rate and clock timing relationship. Another byte is written to the Port D Direction Register to set MOSI, SCK and bit 0 ($\overline{CS}$ of LTC1325) as outputs. The 68HC11 clocks in data from the LTC1325 simultaneously under the control of SCK. The microprocessor transmits the LTC1325 command word in 3 bytes. This is followed by 2 more dummy bytes (with all bits set low) in order to clock in the remaining LTC1325 ADC and status bits.



APPLICATIONS INFORMATION

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#01010101B	Write control byte to the SPCR
	STAA	$1028	
	LDAA	#00100001B	Setup Port D
	STAA	$1009	
	LDX	#$1000	Base adress of SPI registers
MSBF1	BCLR	$08,#0	Take $\overline{CS}$ low
	LDAA	#$00	Send Byte 1 (MSB)
	STAA	$102A	
LOOP1	TST	$1029	
	BPL	LOOP1	
	LDAA	#$FF	Send Byte 2
	STAA	$102A	
LOOP2	TST	$1029	
	BPL	LOOP2	
	LDAA	#$00	Send Byte 3
	STAA	$102A	
LOOP3	TST	$1029	
	BPL	LOOP3	
	LDAA	#$FF	Send Byte 4 (dummy)
	STAA	$102A	
LOOP4	TST	$1029	
	BPL	LOOP4	
	LDAA	#$FF	Send Byte 5 (dummy)
	STAA	$102A	
LOOP5	TST	$1029	
	BPL	LOOP5	
	BSET	$08,X,#01	Take $\overline{CS}$ high
	END	MSBF1	End of MSBF = 1 code

TYPICAL APPLICATION



PRELIMINARY

LTC1348

3.3V Low Power RS232 3-Driver/5-Receiver Transceiver

December 1993

FEATURES

- **True RS232 from a Single 3.3V Supply**
- **Low Supply Current: 500μA**
- **0.2μA Supply Current in SHUTDOWN**
- 10μA Supply Current in RECEIVER ALIVE Mode
- ESD Protection Over ±10kV
- Available in SSOP Package
- Uses Small Capacitors: 0.1μF
- Operates to 120k Baud
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers

DESCRIPTION

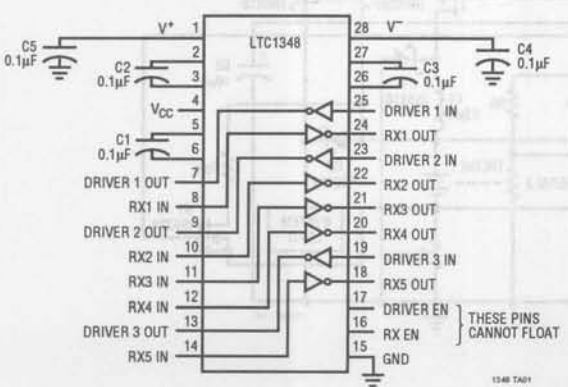
The LTC1348 is a 3-driver/5-receiver RS232 transceiver with very low supply current. The charge pump only requires five 0.1μF capacitors.

The transceiver operates in one of the four modes: NORMAL, RECEIVER DISABLE, RECEIVER ALIVE or SHUTDOWN. In NORMAL or RECEIVER DISABLE mode, I_{CC} is only 500μA with the RS232 outputs unloaded condition. In SHUTDOWN mode, the supply current is further reduced to 0.2μA. In RECEIVER ALIVE mode, all five receivers are kept alive and the supply current is 10μA. All RS232 outputs assume a high impedance state in SHUTDOWN or RECEIVER ALIVE mode or with the power off. The receiver outputs assume a high impedance state in RECEIVER DISABLE.

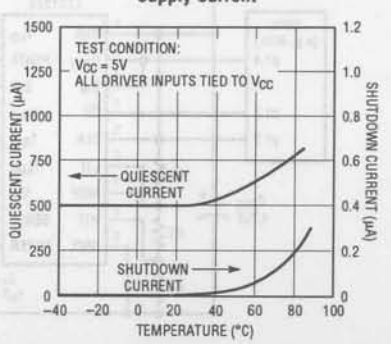
The LTC1348 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver can operate up to 120k baud with a 2500pF, 3kΩ load. Both driver outputs and receiver inputs can be forced to ±25V without damage, and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with SHUTDOWN



Supply Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 4V
Input Voltage
- Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
- Receiver ..... $-25V$ to $25V$
- Driver/Receiver Enable Pin ..... $-0.3V$ to $V_{CC} + 0.3V$

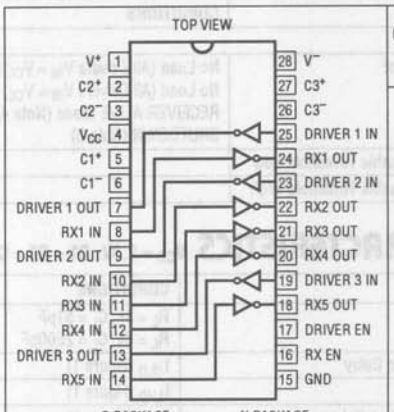
Output Voltage
- Driver ..... $-25V$ to $25V$
- Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$

Short-Circuit Duration
- V^+ ..... 30 sec
- V^- ..... 30 sec
- Driver Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range
- Commercial (LTC1348C) ..... 0°C to 70°C
- Industrial (LTC1348I) ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD SSOP

N PACKAGE
28-LEAD PLASTIC DIP

S PACKAGE
28-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 56°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1348CG
LTC1348CN
LTC1348CS
LTC1348IG
LTC1348IN
LTC1348IS

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	7.0		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●		−20	−40	µA
Output Short-Circuit Current	V_{OUT} = 0V				±12		mA
Output Leakage Current	SHUTDOWN (Note 3) or RECEIVER ALIVE Mode (Note 4), V_{OUT} = ±20V		●		±10	±500	µA
Any Receiver							
Input Voltage Thresholds	Input Low Threshold		●	0.8	1.3		V
	Input High Threshold		●		1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA (V_{CC} = 3.3V)		●		0.2	0.4	V
	Output High, I_{OUT} = 160µA (V_{CC} = 3.3V)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−3	−20		mA
Output Leakage Current	SHUTDOWN (Note 3), $0 \le V_{OUT} \le V_{CC}$		●		1	10	µA
Power Supply Generator							
V^+ Output Voltage	I_{OUT} = 0mA				8.0		V
	I_{OUT} = 12mA				7.5		V
V^- Output Voltage	I_{OUT} = 0mA				−8.0		V
	I_{OUT} = −12mA				−7.0		V
Supply Rise Time	SHUTDOWN to Turn-On				0.2		ms

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
V_{CC} Supply Current	No Load (All Drivers $V_{IN} = V_{CC}$)(Note 2), 0°C ≤ T_A ≤ 70°C	●		0.5	1.0	mA
	No Load (All Drivers $V_{IN} = V_{CC}$) (Note 2), –40°C ≤ T_A ≤ 85°C	●		0.5	1.5	mA
	RECEIVER ALIVE Mode (Note 4)	●		10	20	µA
	SHUTDOWN (Note 3)	●		0.2	10	µA
Driver/Receiver Enable Threshold Low		●		1.4	0.8	V
Driver/Receiver Enable Threshold High		●	2.0	1.4		V

AC CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF		3	5		V/µs
Driver Propagation Delay	t_{HLD} (Figure 1)	●		2	3.5	µs
(TTL to RS232)	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay	t_{HLR} (Figure 2)	●		0.3	0.8	µs
(RS232 to TTL)	t_{LHR} (Figure 2)	●		0.2	0.8	µs

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade, –40°C ≤ T_A ≤ 85°C for industrial grade).

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded. The $V_{DRIVER\ EN}$ and $V_{RX\ EN}$ = V_{CC}.

Note 3: Supply current measurement in SHUTDOWN is performed with $V_{DRIVER\ EN}$ and $V_{RX\ EN}$ = 0V.

Note 4: Supply current measurement in RECEIVER ALIVE mode is performed with $V_{DRIVER\ EN}$ = 0V and $V_{RX\ EN}$ = V_{CC}.

PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current is less than 0.2µA in the SHUTDOWN mode. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

RX EN: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its functional description.

DRIVER EN: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its function description.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \cong 3V_{CC} - 2V$. This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \cong -(3V_{CC} - 2V)$. This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$: Commutating Capacitor Inputs. These pins require three external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$, and another from $C2^+$ to $C2^-$ and another from $C3^+$ to $C3^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 20Ω.

DRIVER IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip. To minimize power consumption, the internal driver pull-up resistors are disconnected from V_{CC} in SHUTDOWN or RECEIVER ALIVE mode.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in SHUTDOWN, RECEIVER ALIVE mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

PIN FUNCTIONS

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in high impedance state when in SHUTDOWN or RECEIVER DISABLE mode to allow data line sharing.

Table 1. Function Description

MODE	RX EN	DR EN	DRIVERS	RECEIVERS	ICC(μA) (TYP)
SHUTDOWN	0	0	All Drivers SHUTDOWN All Driver Outputs Assume High Impedance	All Receivers SHUTDOWN All Receivers Outputs Assume High Impedance	0.2
RECEIVER DISABLE	0	1	All Drivers Alive	All Receiver Outputs in Three-State	500
RECEIVER ALIVE	1	0	All Drivers SHUTDOWN All Driver Outputs in Three-State	All Receivers Alive	10
NORMAL	1	1	All Drivers Alive	All Receivers Alive	500

SWITCHING TIME WAVEFORMS

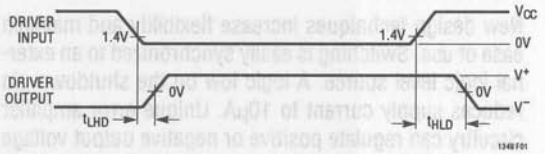


Figure 1. Driver Propagation Delay Timing

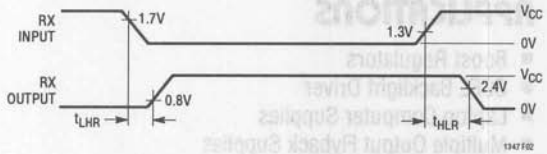


Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

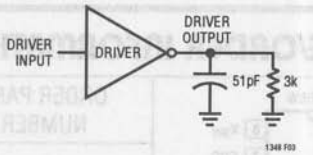


Figure 3. Driver Timing Test Load

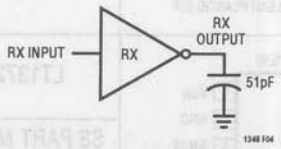
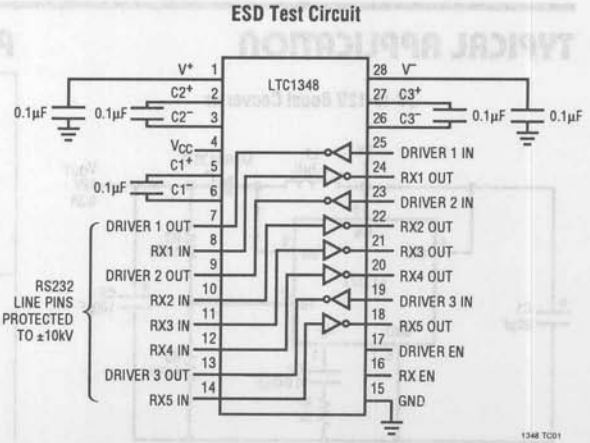


Figure 4. Receiver Timing Test Load

ESD Test Circuit



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PRELIMINARY

LT1372

500kHz High Efficiency 1.5A Switching Regulator

May 1994

FEATURES

- Uses Small Inductors: 4.7µH
- All Surface Mount Components
- Only 0.5 Square Inch of Board Space
- Minimum Supply Voltage: 2.7V
- Quiescent Current: 3mA
- Current Limited Power Switch: 1.5A
- High Efficiency Plus Increased Speed
- Regulates Positive or Negative Outputs
- Shutdown Supply Current: 10µA
- Easy External Synchronization
- Small 8-Pin SO or MiniDIP Packages

APPLICATIONS

- Boost Regulators
- CCFL Backlight Driver
- Laptop Computer Supplies
- Multiple Output Flyback Supplies
- Inverting Supplies

DESCRIPTION

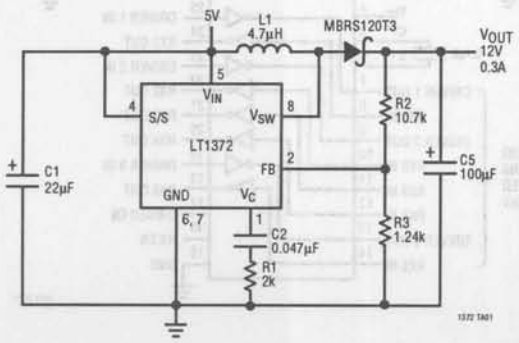
The LT1372 is a monolithic high frequency switching regulator. It can be operated in all standard switching configurations including boost, buck, flyback, forward, inverting and "Cuk." A 1.5A high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1372 to be built in 8-pin SO or miniDIP packages.

The LT1372 consumes only 3mA quiescent current and has higher efficiency than previous parts. High frequency switching allows for very small inductors to be used. All surface mount components consume less than 0.5 square inch of board space.

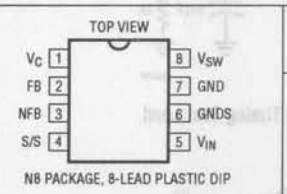
New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic level source. A logic low on the shutdown pin reduces supply current to 10µA. Unique error amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency compensation techniques. Nonlinear error amplifier transconductance reduces output overshoot on start-up or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

TYPICAL APPLICATION

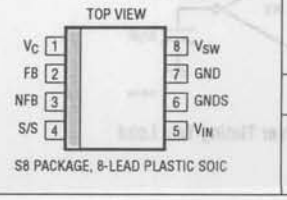
5V-to-12V Boost Converter



PACKAGE/ORDER INFORMATION



N8 PACKAGE, 8-LEAD PLASTIC DIP



S8 PACKAGE, 8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LT1372CN8
LT1372CS8
S8 PART MARKING
1372

PRELIMINARY

LT1376

1.5A, 500kHz Step-Down Switching Regulator

May 1994

FEATURES

- Fixed 500kHz Switching Frequency
- Uses All Surface Mount Components
- Inductor Size Reduced to 5µH
- Saturating Switch Design: 0.4Ω
- Effective Supply Current: 2mA
- Shutdown Current: 20µA
- Cycle-by-Cycle Current Limiting
- Easily Synchronizable to 1MHz

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Battery Charger
- Distributed Power
- 5V to 3.3V Regulator

DESCRIPTION

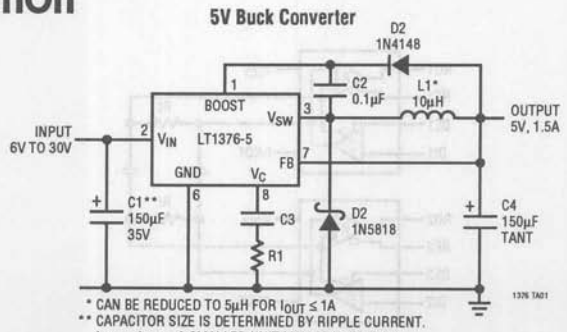
The LT1376 is a 500kHz monolithic buck mode switching regulator. A 1.5A switch is included on the die along with all the necessary oscillator, control, and logic circuitry. High switching frequency allows a considerable reduction in the size of external components. The topology is current mode for fast transient response and good loop stability. Both fixed output voltage and adjustable parts are available.

A special high speed bipolar process and new design techniques allow the LT1376 to achieve high conversion efficiency at high switching rates. High efficiency is maintained over a wide output current range by keeping quiescent supply current to 4mA and by utilizing a boost capacitor to allow the NPN power switch to saturate. A special biasing pin can reduce effective supply current to 2mA for even higher efficiency at light loads. A shutdown signal will reduce supply current to 20µA. Synchronizing the switching frequency to an external signal requires no extra parts.

The LT1376 is available in 8-pin DIP and SO packages. Temperature rise is kept to a minimum by the high efficiency design. Full cycle-by-cycle short-circuit protection and thermal shutdown are provided. Standard surface mount external parts are used, including the inductor and capacitors.

TYPICAL APPLICATION

5V Buck Converter



* CAN BE REDUCED TO 5µH FOR $I_{OUT} \leq 1A$

** CAPACITOR SIZE IS DETERMINED BY RIPPLE CURRENT. $I_{RMS} = I_{OUT}/2$. A SMALLER UNIT MAY BE USED FOR LOWER OUTPUT CURRENTS.

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INITIAL RELEASE
Final Electrical Specifications

LTC1481

Ultra-Low Power RS485 Transceiver with Shutdown

May 1994

FEATURES

- **Low Power: I_{CC} = 120µA Max with Driver Disabled**
- I_{CC} = 500µA Max with Driver Enabled, No Load
- **1µA Quiescent Current in Shutdown Mode**
- **High Speed: Up to 2.5Mbits/s Data Rate**
- Single 5V Supply
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- 30ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

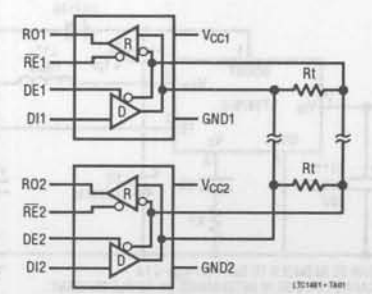
DESCRIPTION

The LTC1481 is an ultra-low power differential line transceiver designed for data transmission standard RS485 applications. It will also meet the requirements of RS422. The CMOS design offers significant power savings over its bipolar counterparts without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80µA while operating and less than 1µA in shutdown.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The LTC1481 is fully specified over the commercial and extended industrial temperature range and is available in 8-pin DIP and SO packages.

TYPICAL APPLICATION

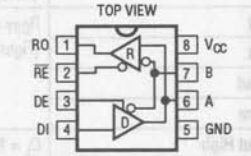


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1481C ..... $0°C \le T_A \le 70°C$
LTC1481I ..... $-40°C \le T_A \le 85°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S)

ORDER PART NUMBER
LTC1481CN8
LTC1481IN8
LTC1481CS8
LTC1481IS8
S8 PART MARKING
1481
1481I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V \pm 5\%$, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	$R = 50\Omega$ (RS422)	●	2.0			V
		$R = 27\Omega$ (RS485), Figure 1	●	1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V	●			1.0	mA
		DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	●			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Output Enabled	●		300	500	µA
		No Load, Output Disabled	●		80	120	µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

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SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5%, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 5)	●	10	30	60	ns
t_{PHL}	Driver Input to Output		●	10	30	60	ns
t_{SKEW}	Driver Output to Output		●		5	10	ns
t_r, t_f	Driver Rise or Fall Time		●	3	15	40	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●			2.5	Mbits/s
t_{SHDN}	Time to Shutdown		●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	100	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	100	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power (1μA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

FUNCTION TABLES

LTC1481 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1481

LTC1481 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1481

TEST CIRCUITS

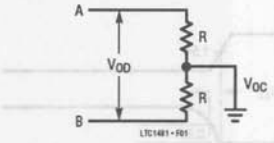

Figure 1. Driver DC Test Load

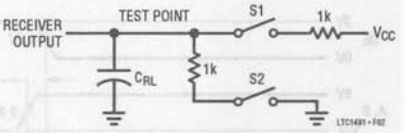

Figure 2. Receiver Timing Test Load

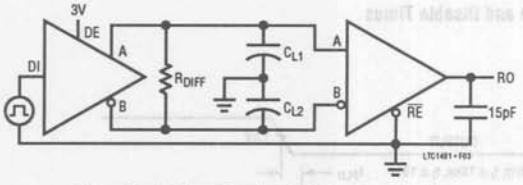

Figure 3. Driver/Receiver Timing Test Circuit

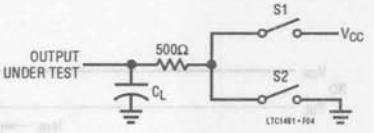

Figure 4. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

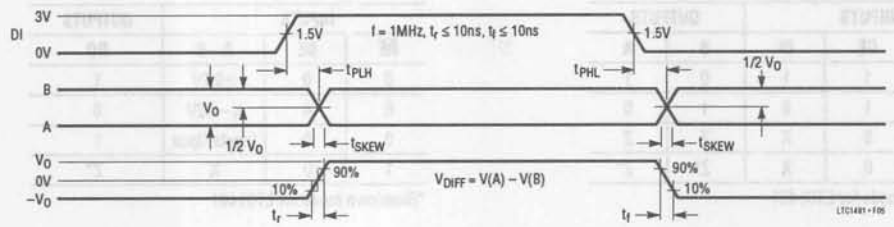

Figure 5. Driver Propagation Delays

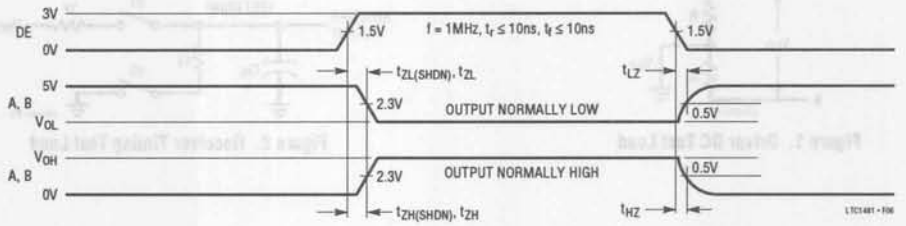

Figure 6. Driver Enable and Disable Times

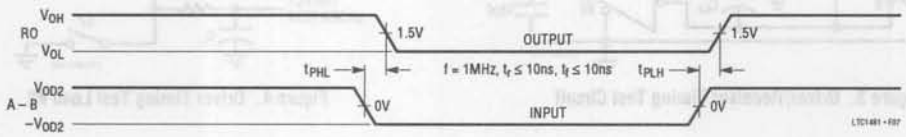

Figure 7. Receiver Propagation Delays

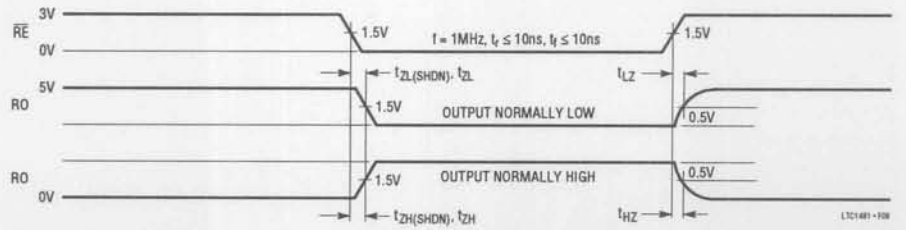

Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Basic Theory of Operation

Traditionally RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1481 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1481 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1481 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

The LTC1481 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

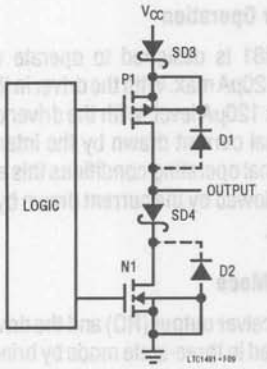

Figure 9. LTC1481 Output Stage

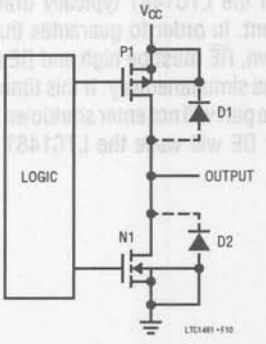

Figure 10. Conventional CMOS Output Stage

The LTC1481 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. This clamp protects the MOS gates from ESD voltages well over 2kV. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques.

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APPLICATIONS INFORMATION

Low Power Operation

The LTC1481 is designed to operate with a quiescent current of 120µA max. With the driver in three-state I_{CC} will drop to this 120µA level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ high and DE low respectively. In addition, the LTC1481 will enter shutdown mode when $\overline{RE}$ is high and DE is low.

In shutdown the LTC1481 typically draws only 1µA of supply current. In order to guarantee that the part goes into shutdown, $\overline{RE}$ must be high and DE must be low for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1481 back up within 3.5µs.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1481 propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 5V

The drivers skew times are:

Skew = 5ns Typ, V_{CC} = 5V

10ns Max, V_{CC} = 5V, T_A = −40°C to 85°C

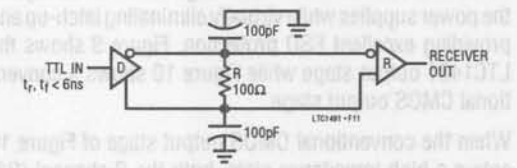


Figure 11. Receiver Propagation Delay Test Circuit

Ultra-Low Power RS485 Low EMI Transceiver with Shutdown

May 1994

FEATURES

- **Low Power: I_{CC} = 120µA Max with Driver Disabled**
- I_{CC} = 500µA Max with Driver Enabled, No Load
- **1µA Quiescent Current in Shutdown Mode**
- Controlled Slew Rate Driver for Reduced EMI
- Single 5V Supply
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

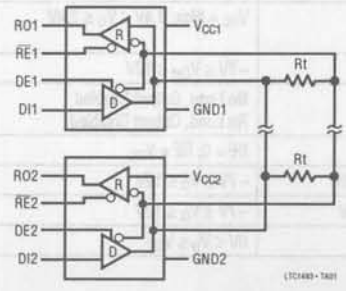
DESCRIPTION

The LTC1483 is an ultra-low power differential line transceiver designed for data transmission standard RS485 applications. It will also meet the requirements of RS422. The LTC1483 features output drivers with controlled slew rate, decreasing the EMI radiated from the RS485 lines, and improving signal fidelity with misterminated lines. The CMOS design offers significant power savings over its bipolar counterparts without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80µA while operating and less than 1µA in shutdown.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The LTC1483 is fully specified over the commercial and extended industrial temperature range and is available in 8-pin DIP and SO packages.

TYPICAL APPLICATION



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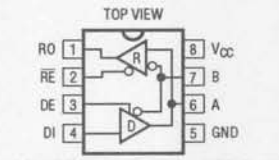
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1483C ..... $0°C \le T_A \le 70°C$
LTC1483I ..... $-40°C \le T_A \le 85°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S)

ORDER PART NUMBER
LTC1483CN8 LTC1483IN8 LTC1483CS8 LTC1483IS8
S8 PART MARKING
1483 1483I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422)	●	2			V
		R = 27Ω (RS485), Figure 1	●	1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V	●			1.0	mA
		DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	●			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Output Enabled	●		300	500	µA
		No Load, Output Disabled	●		80	120	µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

SWITCHING CHARACTERISTICS

LTC1483, V_{CC} = 5V ±5%, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1483 MIN	LTC1483 TYP	LTC1483 MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 5)	●	150		2000	ns
t_{PHL}	Driver Input to Output		●	150		2000	ns
t_{SKEW}	Driver Output to Output		●		100	800	ns
t_r, t_f	Driver Rise or Fall Time		●	150		2000	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●	100		2000	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●	100		2000	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4, 6), S1 Closed	●	150		2000	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4, 6), S2 Closed	●	150		2000	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●	150			kbits/s
t_{SHDN}	Time to Shutdown		●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●			2000	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●			2000	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power (1µA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

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FUNCTION TABLES

LTC1483 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1483

LTC1483 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1483

TEST CIRCUITS

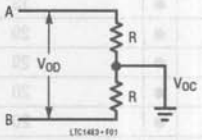

Figure 1. Driver DC Test Load

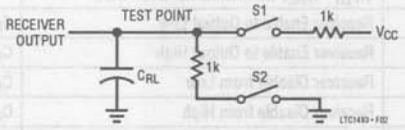

Figure 2. Receiver Timing Test Load

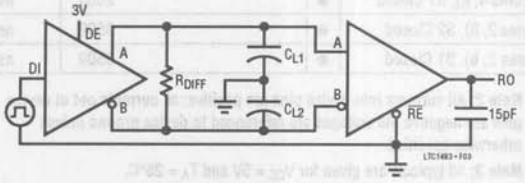

Figure 3. Driver/Receiver Timing Test Circuit

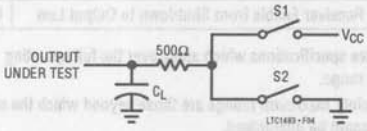

Figure 4. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

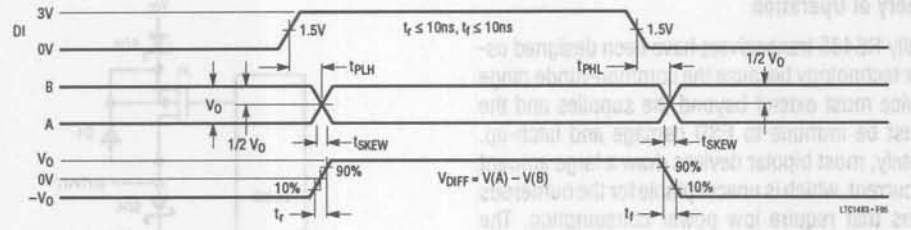

Figure 5. Driver Propagation Delays

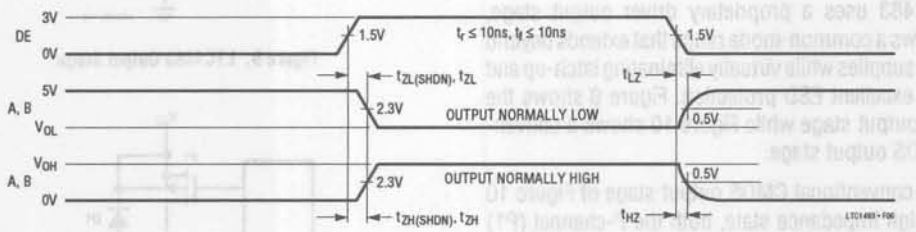

Figure 6. Driver Enable and Disable Times

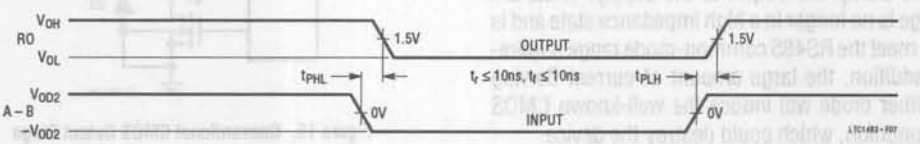

Figure 7. Receiver Propagation Delays

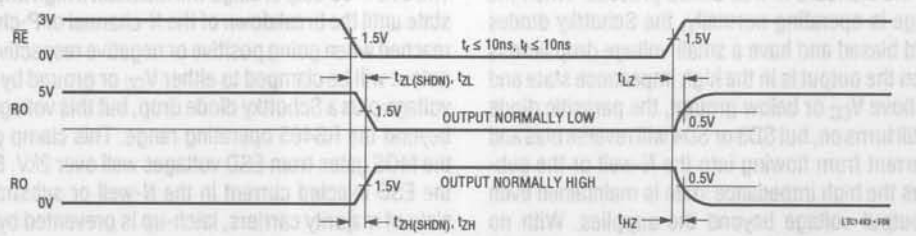

Figure 8. Receiver Enable and Disable Times

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APPLICATIONS INFORMATION

Basic Theory of Operation

Traditionally RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1483 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1483 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1483 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

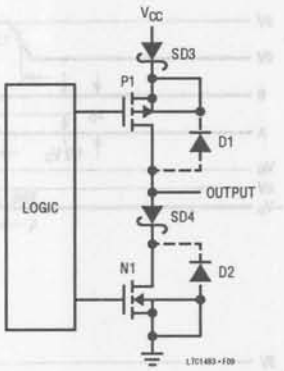


Figure 9. LTC1483 Output Stage

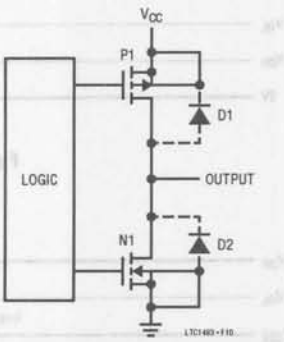


Figure 10. Conventional CMOS Output Stage

The LTC1483 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

The LTC1483 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. This clamp protects the MOS gates from ESD voltages well over 2kV. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques.

APPLICATIONS INFORMATION

Low Power Operation

The LTC1483 is designed to operate with a quiescent current of 120µA max. With the driver in three-state I_{CC} will drop to this 120µA level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ high and DE low respectively. In addition, the LTC1483 will enter shutdown mode when $\overline{RE}$ is high and DE is low.

In shutdown the LTC1483 typically draws only 1µA of supply current. In order to guarantee that the part goes into shutdown, $\overline{RE}$ must be high and DE must be low for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1483 back up within 3.5µs.

If the slow slew rate driver was active immediately prior to shutdown, the supply current will not drop to 1µA until the driver outputs have reached a steady state; this can take as long as 2.6µs under worst case conditions. If the driver was disabled prior to shutdown the supply current will drop to 1µA immediately.

Slew Rate and Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1483 propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 5V

The LTC1483 driver's feature controlled slew rate to reduce system EMI and improve signal fidelity by reducing reflections due to misterminated cables.

The drivers skew times are:

Skew = 100ns Typ, V_{CC} = 5V

800ns Max, V_{CC} = 5V, T_A = –40°C to 85°C

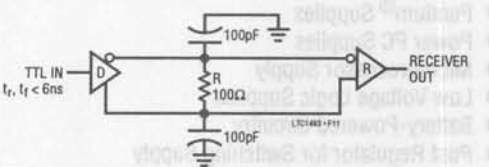


Figure 11. Receiver Propagation Delay Test Circuit

INITIAL RELEASE
Final Electrical Specifications

LT1585

4A Low Dropout Fast Response Positive Regulator Adjustable and Fixed

June 1994

FEATURES

- Output Voltage Trimmed to ±1%
- **Fast Transient Response**
- **Guaranteed Dropout Voltage at Multiple Currents**
- Load Regulation: 0.1% Typ
- Trimmed Current Limit
- On-Chip Thermal Limiting
- Standard 3-Pin Power Package

APPLICATIONS

- Pentium® Supplies
- Power PC Supplies
- Microprocessor Supply
- Low Voltage Logic Supplies
- Battery-Powered Circuitry
- Post Regulator for Switching Supply

LT1585CM, LT1585CT	Adjustable
LT1585CM-3.3, LT1585CT-3.3	3.3V Fixed
LT1585CM-3.38, LT1585CT-3.38	3.38V Fixed
LT1585CM-3.45, LT1585CT-3.45	3.45V Fixed
LT1585CM-3.6, LT1585CT-3.6	3.6V Fixed

DESCRIPTION

The LT1585 is a low dropout three-terminal regulator with up to 4A output current capability. The design has been optimized for low voltage applications where transient response and minimum input voltage are critical. Similar to the LT1085, it has lower dropout voltage and faster transient response. These improvements make it ideal for low voltage microprocessor applications requiring a regulated 2.5V to 3.6V output with a 5V to 7V input supply.

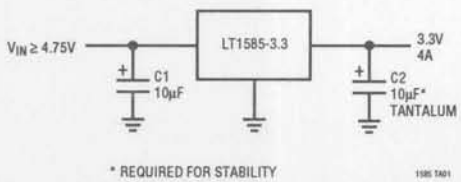
Current limit is trimmed to about 4.5A to ensure adequate output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload that would create excessive junction temperatures.

The LT1585 is available in both the through-hole and surface amount versions of the industry standard 3-pin TO-220 power package.

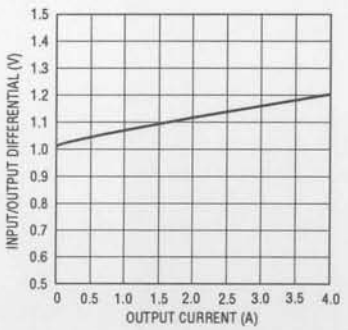
Pentium is a registered trademark of Intel Corp.

TYPICAL APPLICATION

3.3V, 4A Regulator



Dropout Voltage vs Output Current

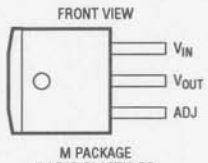
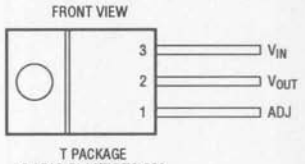
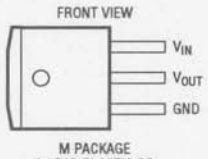
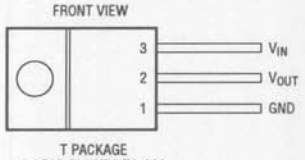


ABSOLUTE MAXIMUM RATINGS

V_{IN} (No Short Circuit) 7V
V_{IN} (Short Circuit) 5.5V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Junction Temperature Range
Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 M PACKAGE 3-LEAD PLASTIC DD	LT1585CM	 T PACKAGE 3-LEAD PLASTIC TO-220	LT1585CT
 M PACKAGE 3-LEAD PLASTIC DD	LT1585CM-3.3 LT1585CM-3.38 LT1585CM-3.45 LT1585CM-3.6	 T PACKAGE 3-LEAD PLASTIC TO-220	LT1585CT-3.3 LT1585CT-3.38 LT1585CT-3.45 LT1585CT-3.6

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	LT1585	$V_{IN} - V_{OUT} = 3V$, $I_{OUT} = 10mA$, $T_J = 25°C$, $10mA \le I_{OUT} \le 4A$, $1.5V \le V_{IN} - V_{OUT} \le 5.75V$	 ●	1.238 1.225	1.250 1.250	1.262 1.275	V V
Output Voltage	LT1585-3.3	$V_{IN} = 5V$, $I_{OUT} = 0mA$, $T_J = 25°C$, $5V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	 ●	3.270 3.235	3.300 3.300	3.330 3.365	V V
	LT1585-3.38	$V_{IN} = 5V$, $I_{OUT} = 0mA$, $T_J = 25°C$, $5V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	 ●	3.347 3.313	3.380 3.380	3.413 3.447	V V
	LT1585-3.45	$V_{IN} = 5V$, $I_{OUT} = 0mA$, $T_J = 25°C$, $5V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	 ●	3.416 3.381	3.450 3.450	3.484 3.519	V V
	LT1585-3.6	$V_{IN} = 5V$, $I_{OUT} = 0mA$, $T_J = 25°C$, $5V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	 ●	3.564 3.528	3.600 3.600	3.636 3.672	V V
Line Regulation		$4.75V \le V_{IN} \le 7V$, $I_{OUT} = 0mA$, $T_J = 25°C$ $2.75V \le V_{IN} \le 7V$ (LT1585), $I_{OUT} = 10mA$, $T_J = 25°C$	 ●		0.005 0.005	0.2 0.2	% %
Load Regulation		$V_{IN} = 5V$, $T_J = 25°C$, $0mA \le I_{OUT} \le 4A$, $V_{IN} = 5.25V$, $T_J = 25°C$, $0mA \le I_{OUT} \le 4A$ (LT1585-3.6) $V_{IN} - V_{OUT} = 3V$, $T_J = 25°C$, $10mA \le I_{OUT} \le 4A$ (LT1585)	 ●		0.05 0.05	0.3 0.5	% %
Dropout Voltage		$\Delta V_{REF} = 1\%$, $I_{OUT} = 3A$ $\Delta V_{REF} = 1\%$, $I_{OUT} = 4A$	 ●		1.150 1.200	1.300 1.400	V V
Current Limit		$V_{IN} = 5.5V$	●	4.100	4.750		A

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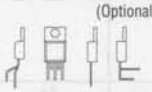
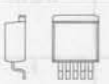
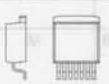
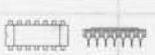
NOTES

SECTION 14—PACKAGE DIMENSIONS

SECTION 14 - PACKAGE DIMENSIONS

INDEX 14-2
PACKAGE CROSS REFERENCE 14-3
PACKAGE DIMENSIONS 14-5

PACKAGE CROSS REFERENCE

	LTC	NSC	ADI	MOT	TI	SG	RAYTH	PMI	MAXIM
Plastic DIP 8 Lead	N8	N N8	N	P1	P	M	P, NB	P	PA
Plastic DIP 14, 16, 18, 20, 24, and 28 Lead	N	N N14	N	P2	N NE NG	N	P, N	P	PD, PE, PN, PP, PG, PI
TO-220 3 Lead	T	T	—	T	KC	P	—	—	AR
(Optional)  TO-220 5 Lead	T	T	—	—	KV	P	—	—	—
TO-220 7 Lead	Y	—	—	—	—	—	—	—	—
Plastic DD 3 Lead	M	—	—	—	—	—	—	—	—
 Plastic DD 5 Lead	Q	—	—	—	—	—	—	—	—
 Plastic DD 7 Lead	R	—	—	—	—	—	—	—	—
Side Brazed Hermetic DIP 8 Lead	D8	D	D	L	—	—	—	—	DA
 Side Brazed Hermetic DIP 14, 16, 18 and 20 Lead	D	D	D	L	—	—	—	YB QB XB	DD, DE, DN, DP
TO-92 3 Lead	Z	Z	—	P	LP	—	—	—	ZR
TO-5, TO-39, TO-46, TO-99, TO-100 and TO-101	H	H	H	G H	—	T	T H	H J K	VR, TA, TB
Ceramic DIP 8 Lead	J8	J J8	D	U	JG	Y	DE	Z	JA
Ceramic DIP 14, 16, 18, 20, 24, and 28 Lead	J	J J14	D	L	J	J	DB DC J	Y Q X	JD, JE, JN, JP, JG, JI

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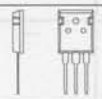
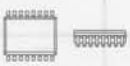
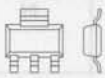
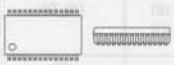
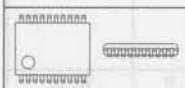
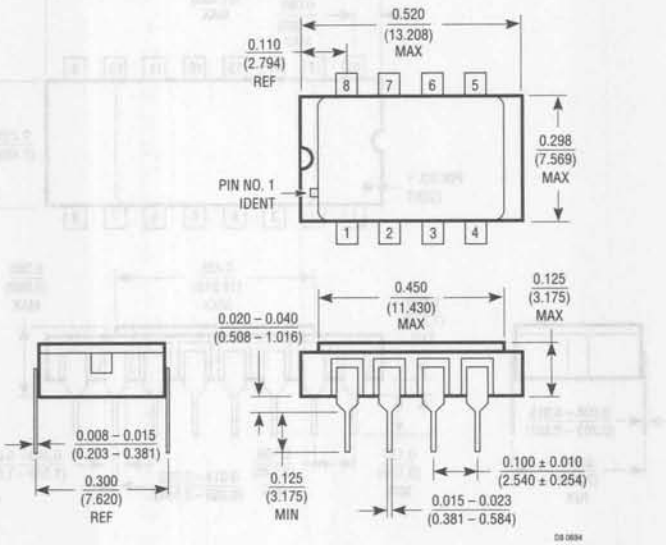
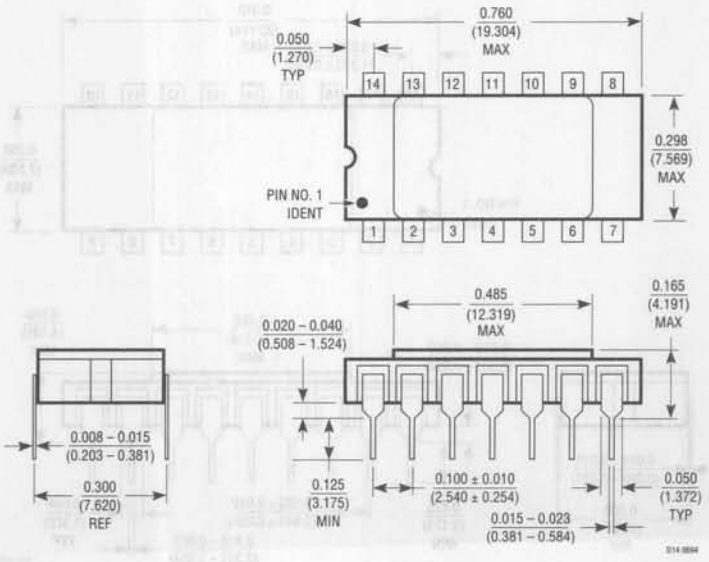
PACKAGE CROSS REFERENCE

		LTC	NSC	ADI	MOT	TI	SG	RAYTH	PMI	MAXIM
	TO-3 (Steel) 2 Lead	K	K Steel	—	K	—	K	—	—	KR
	TO-3 4 Lead	K	K	—	—	KJ	K	—	—	—
	TO-46 2, 3, 4 Lead	H	H	H	—	—	T	—		—
	TO -52 3 Lead									SR
	TO-3P 3 Lead	P	—	—	—	—	—	—	—	—
	Plastic SO 8 Lead	S8	M	R	D	D	—	—	—	SA
	Plastic SO 14, 16 Lead	S	M	R	D	D	—	—	—	SD SE
	Plastic SOL 16, 18, 20, 24, 28 Lead	S	M	R	D	D	—	—	—	WE, WN, WP, WF, WG, WI
	10 Lead Cerpac	W	W	F	F	U010	F	—	RC	F
	10, 14 Lead Flatpack (Bottom-Brazed)		F	AH-14B	—	W010 W014	—		OH-14B	M
	SOT-223 3 Lead	ST	—	—	—	—	—	—	—	—
	Plastic SSOP 20, 24, 28 Lead	G								AI
	Plastic TSSOP 20, 24, 28 Lead	F				DL				
	20-Pin Lead-less Chip Carrier	L	E	E	FN	FN	L		F	L
Proprietary Device Prefixes		LT LTC	LF LP LH MF LM	AD	MC	TL	SG	RM RC	OP REF CMP	MAX

D Package
8-Lead Sidebrazed

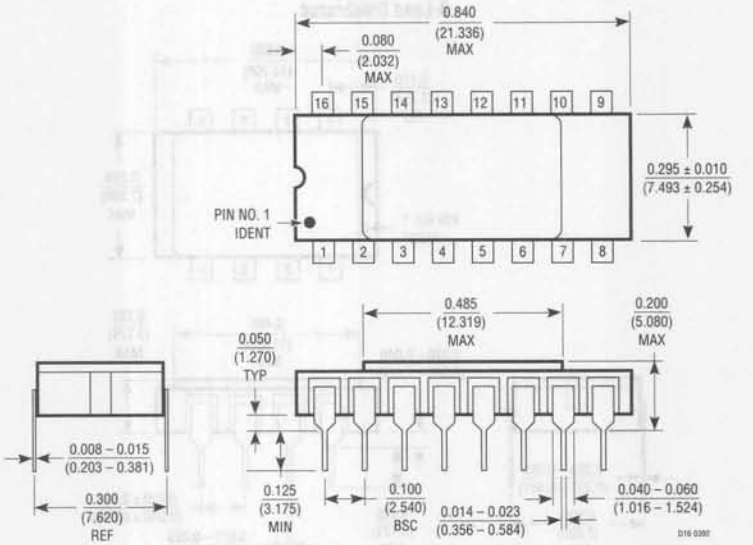


D Package
14-Lead Sidebrazed

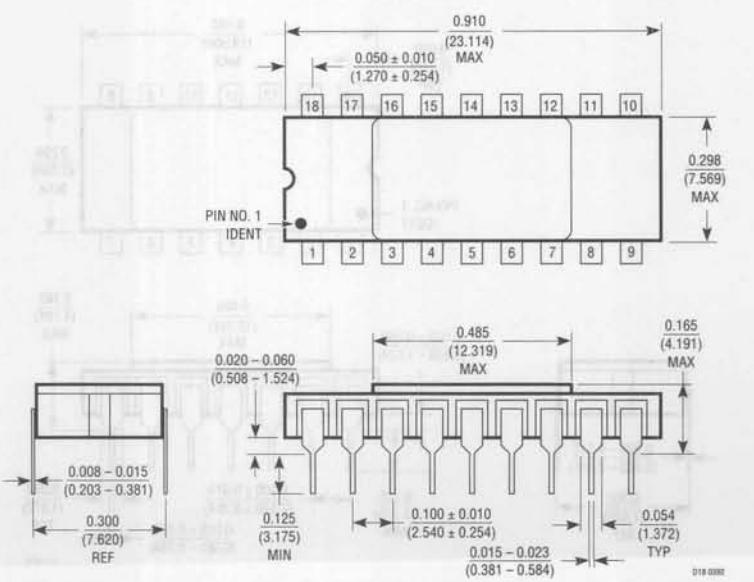


14

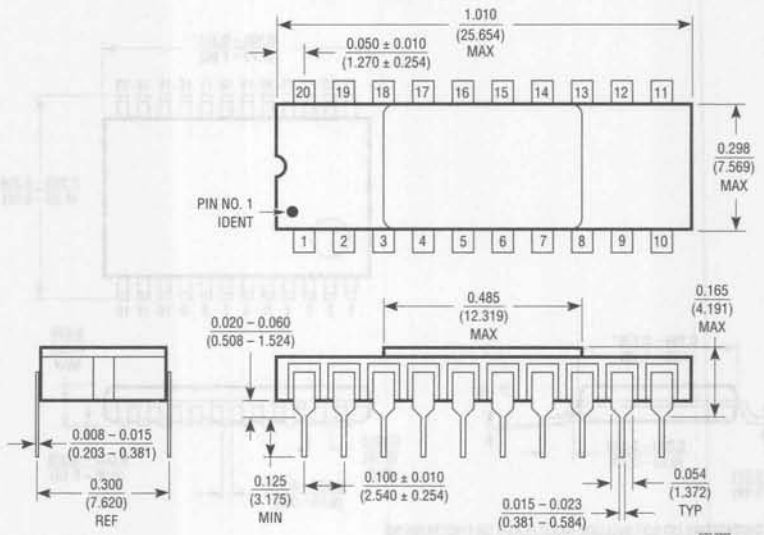
D Package
16-Lead Sidebrazed



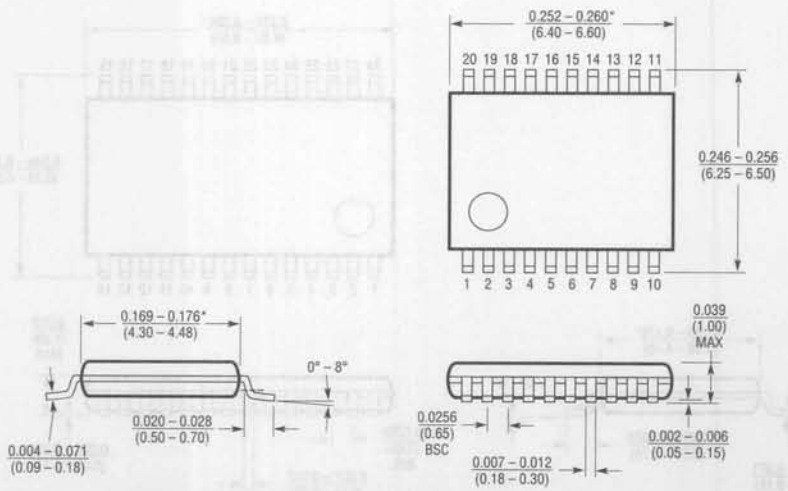
D Package
18-Lead Sidebrazed



D Package
20-Lead Sidebrazed



F Package
20-Lead TSSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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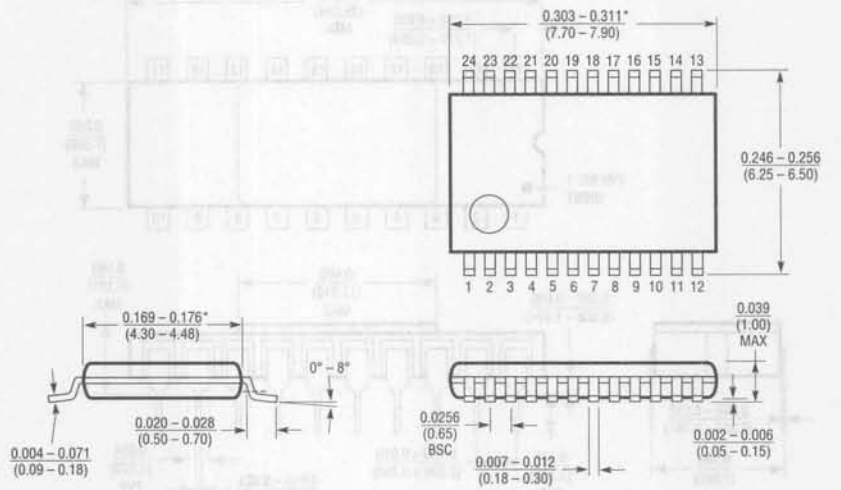
PACKAGE DIMENSIONS

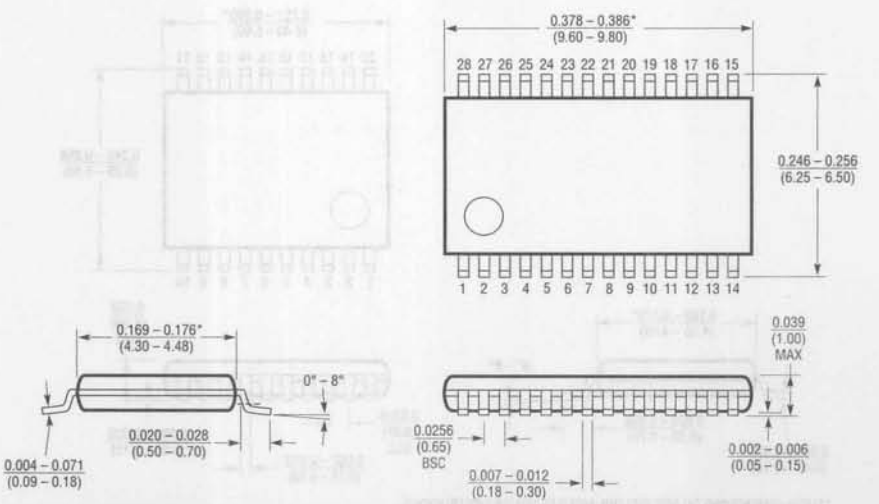
F Package
24-Lead TSSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

F24 TSSOP 0694

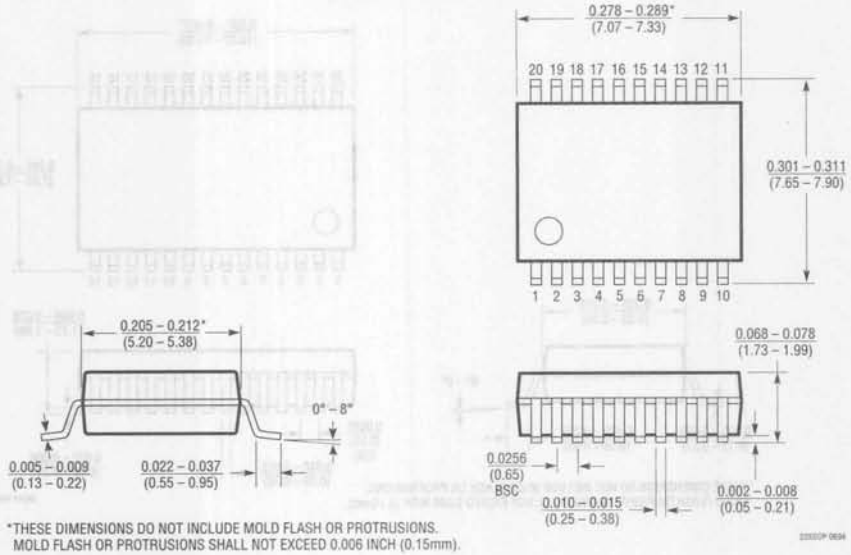
F Package
28-Lead TSSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

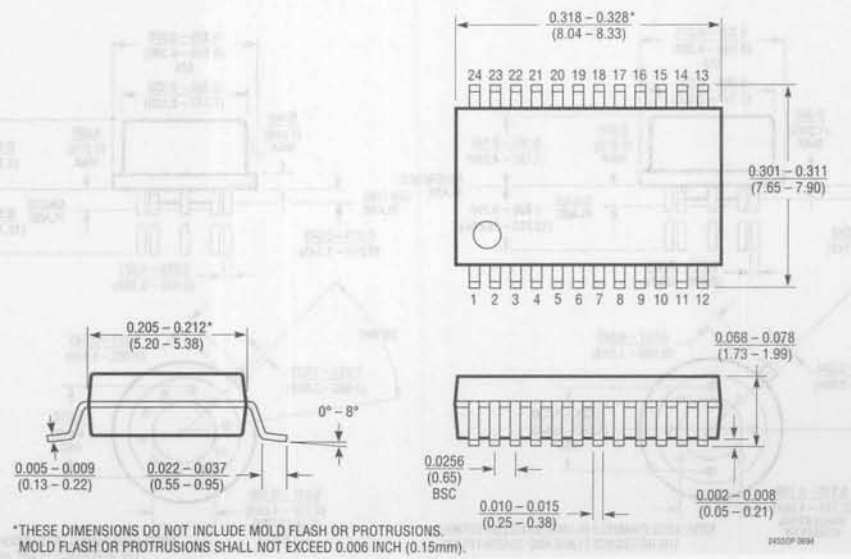
F28 TSSOP 0694

G Package
20-Lead SSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

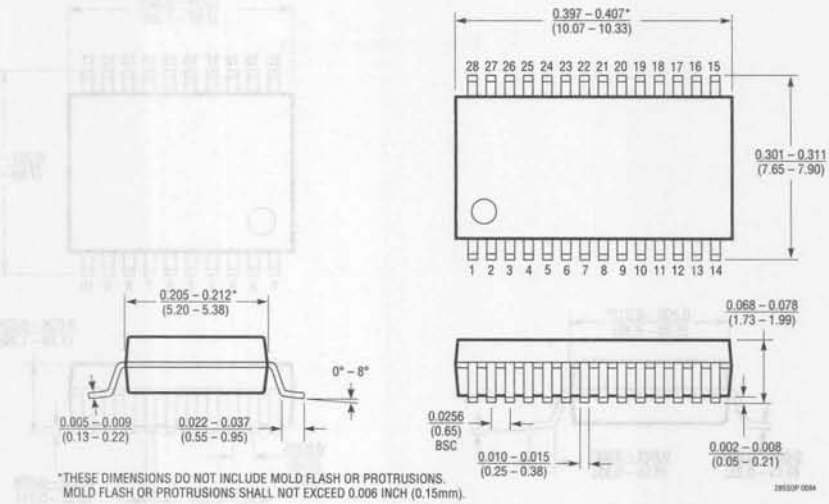
G Package
24-Lead TSSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

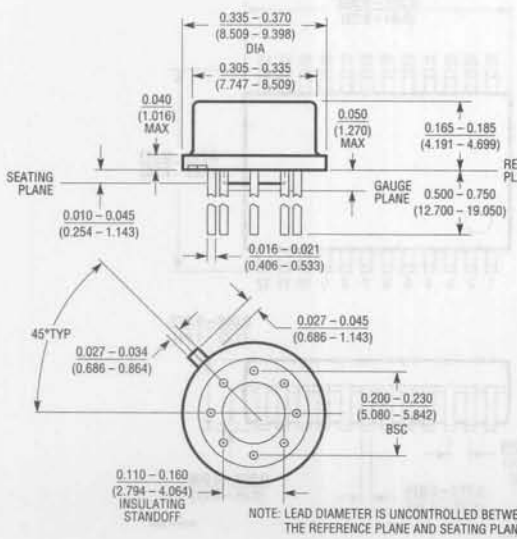
14

G Package
28-Lead SSOP



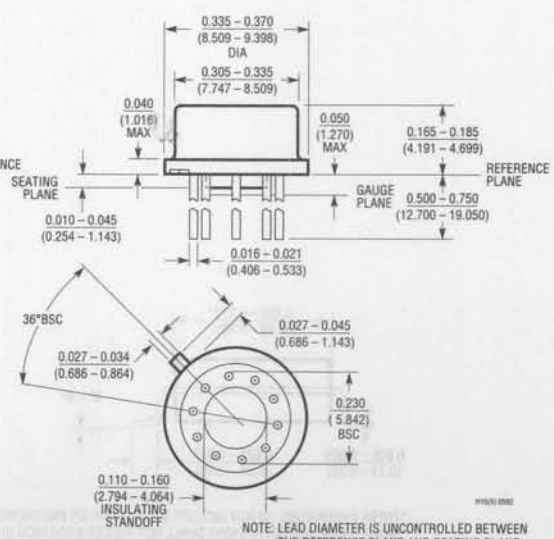
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

H Package
8-Lead TO-5 Metal Can



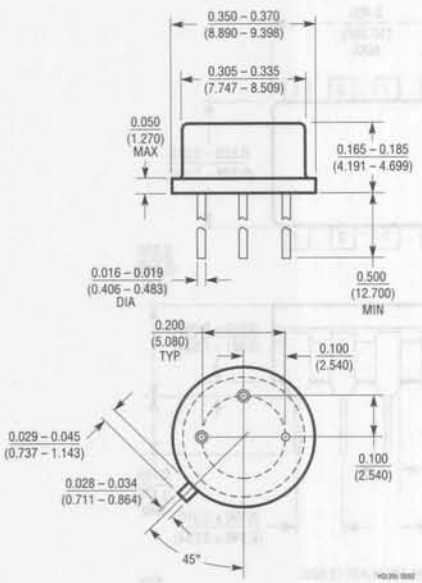
NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

H Package
10-Lead TO-5 Metal Can

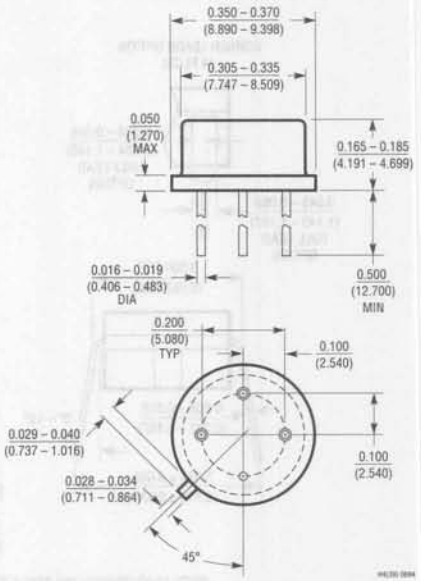


NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

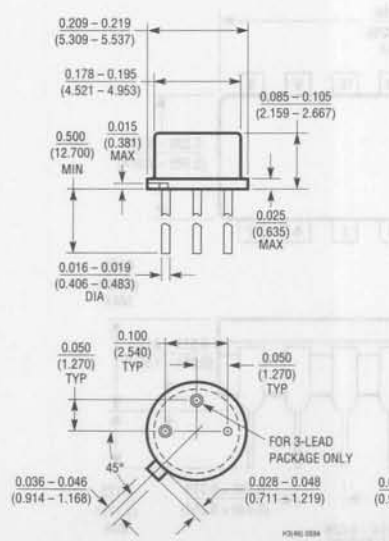
H Package
3-Lead TO-39 Metal Can



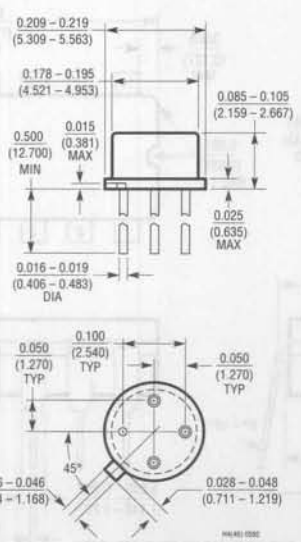
H Package
4-Lead TO-39 Metal Can



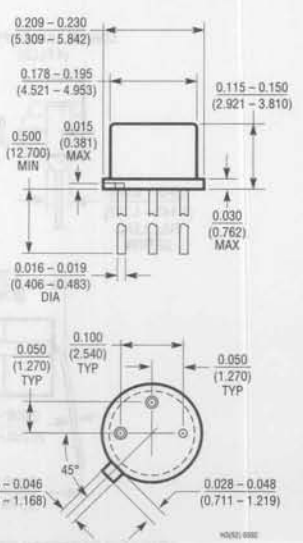
H Package
2-Lead and 3-Lead TO-46 Metal Can



H Package
4-Lead TO-46 Metal Can



H Package
3-Lead TO-52 Metal Can

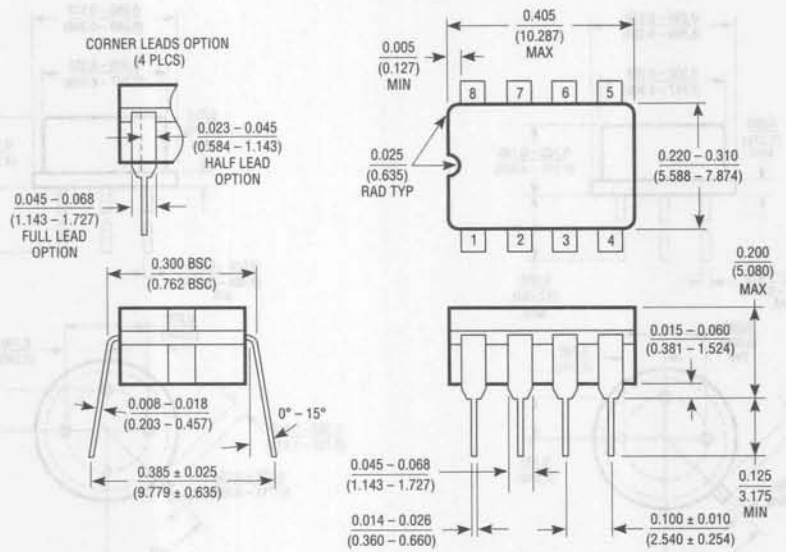


* FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

14

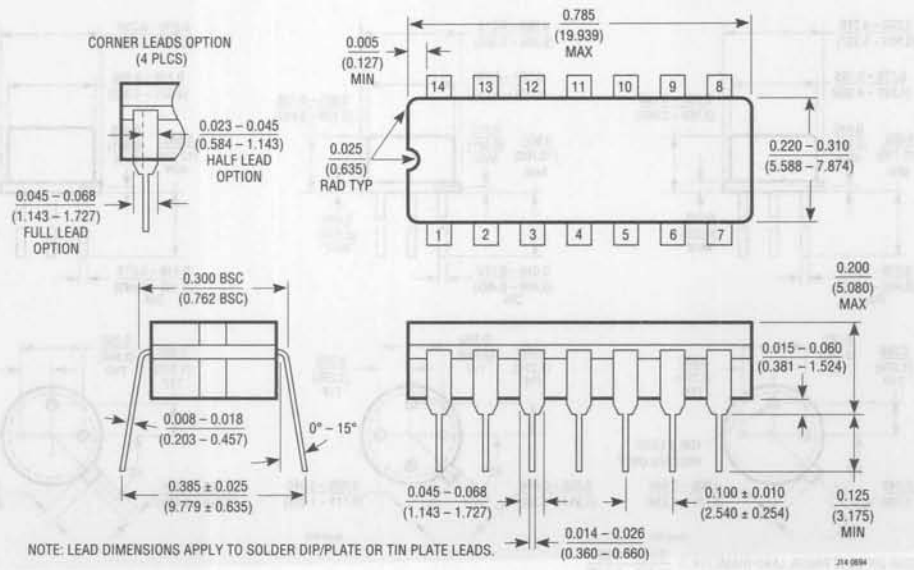
PACKAGE DIMENSIONS

J Package
8-Lead Cerdip



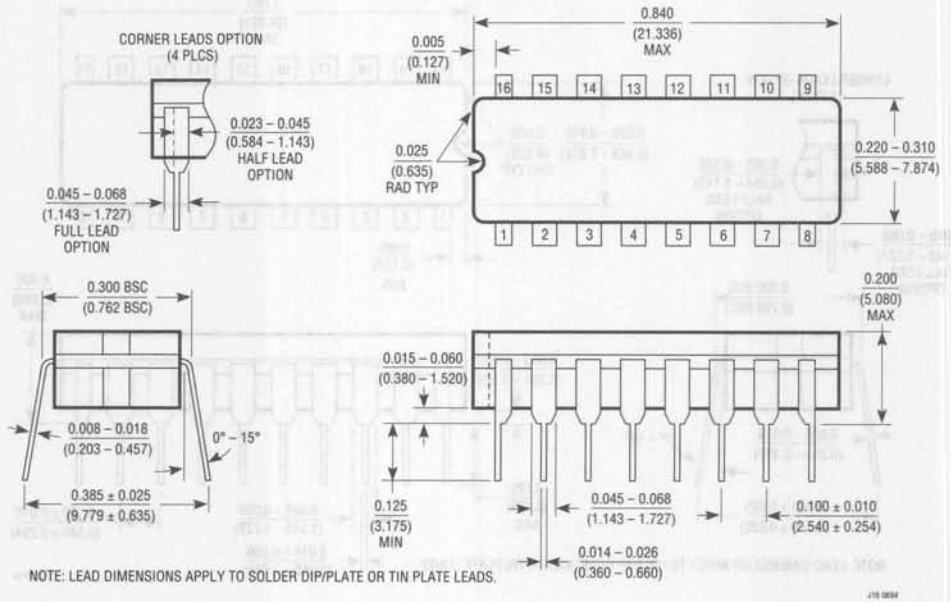
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J Package
14-Lead Cerdip



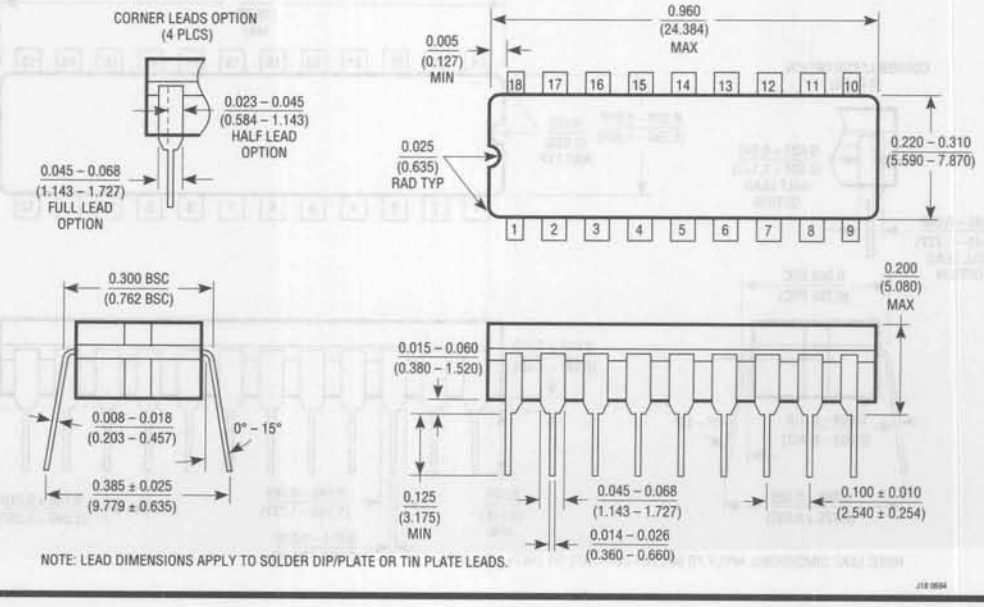
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J Package
16-Lead Cerdip



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

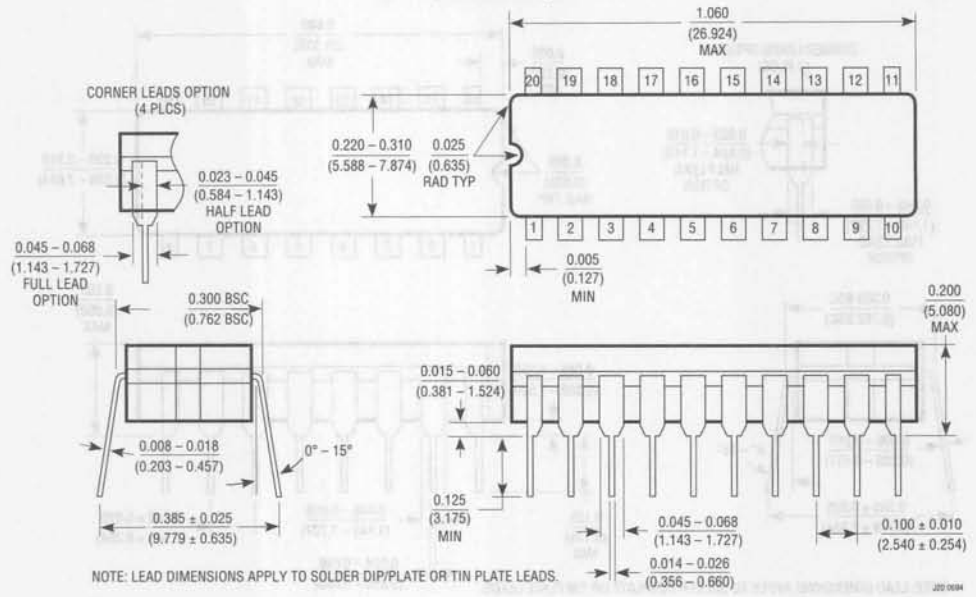
J Package
18-Lead Cerdip



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

PACKAGE DIMENSIONS

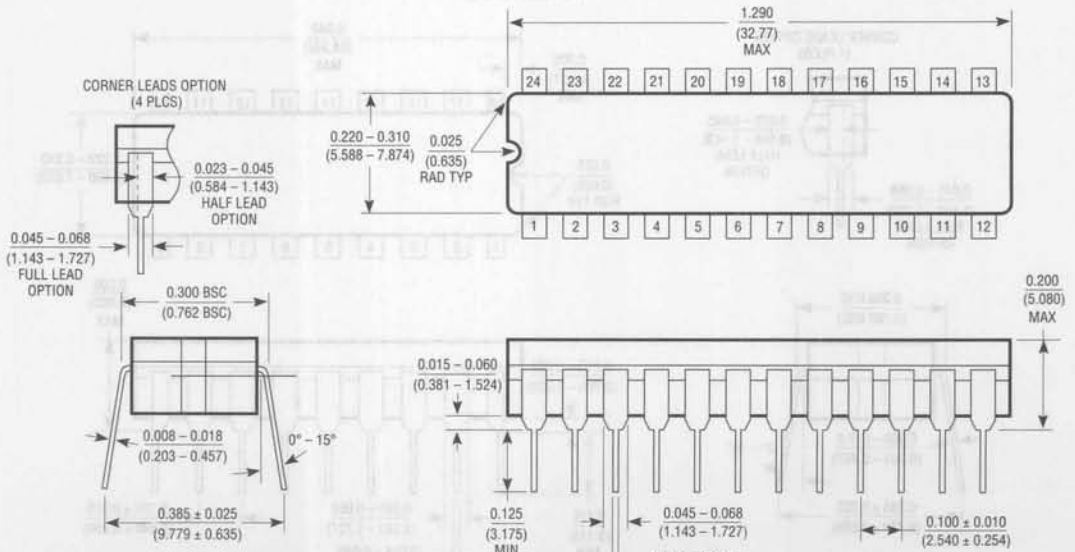
J Package
20-Lead Cerdip



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J20 0694

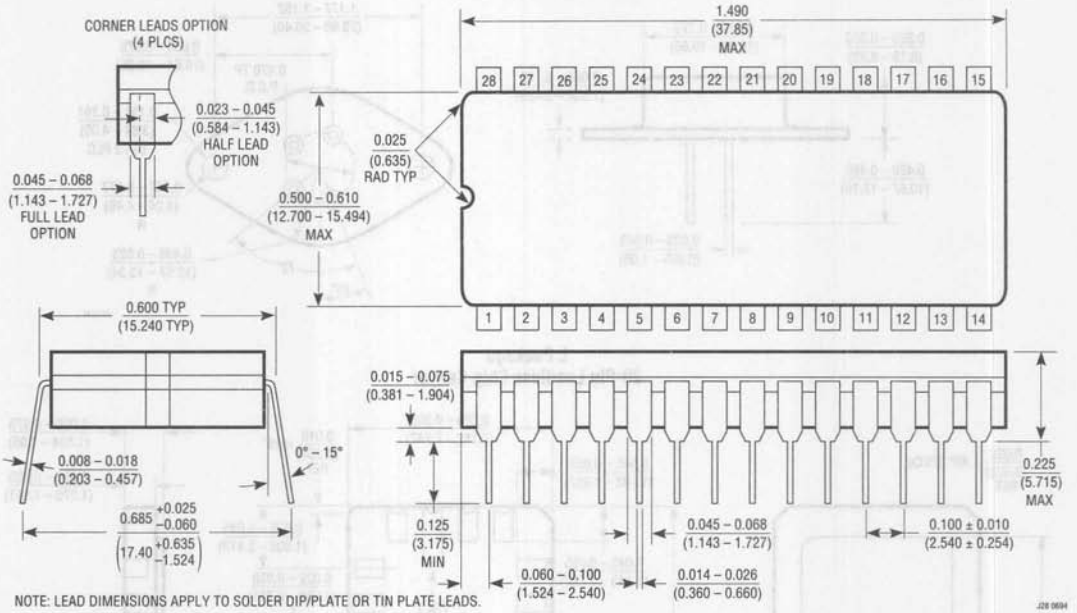
J Package
24-Lead Cerdip



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J24 0694

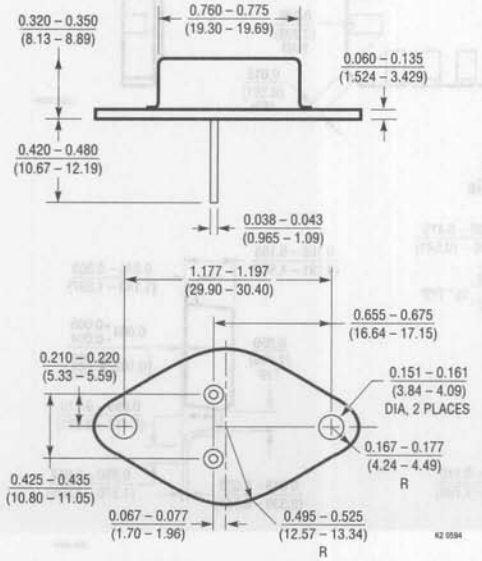
J Package
28-Lead Cerdip



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

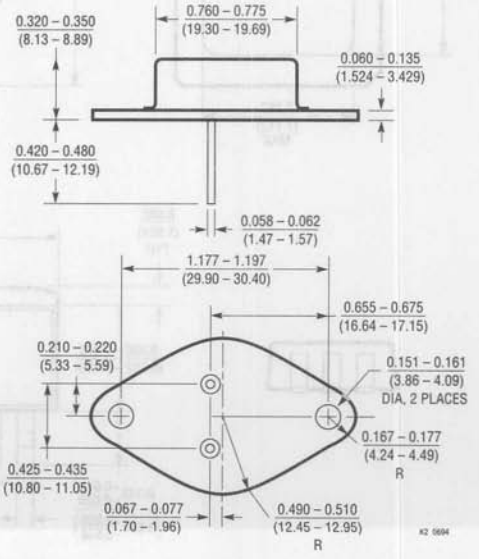
J28 0694

K Package
2-Lead TO-3 Metal Can



K2 0694

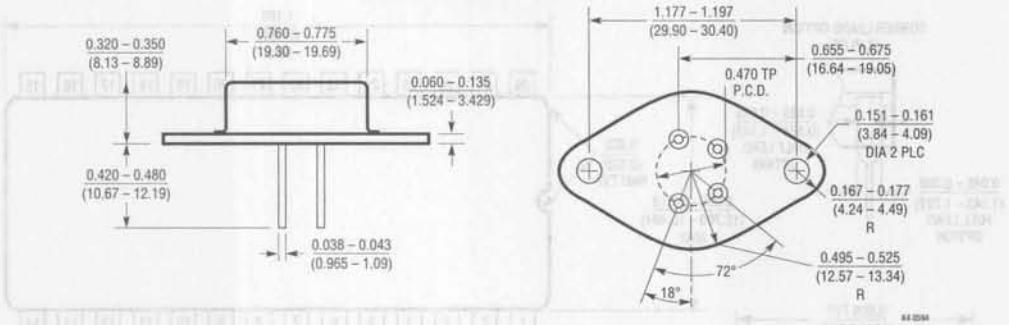
K Package
2-Lead TO-3 Metal Can
(60mil Diameter Leads)



K2 0694

14

K Package
4-Lead TO-3 Metal Can



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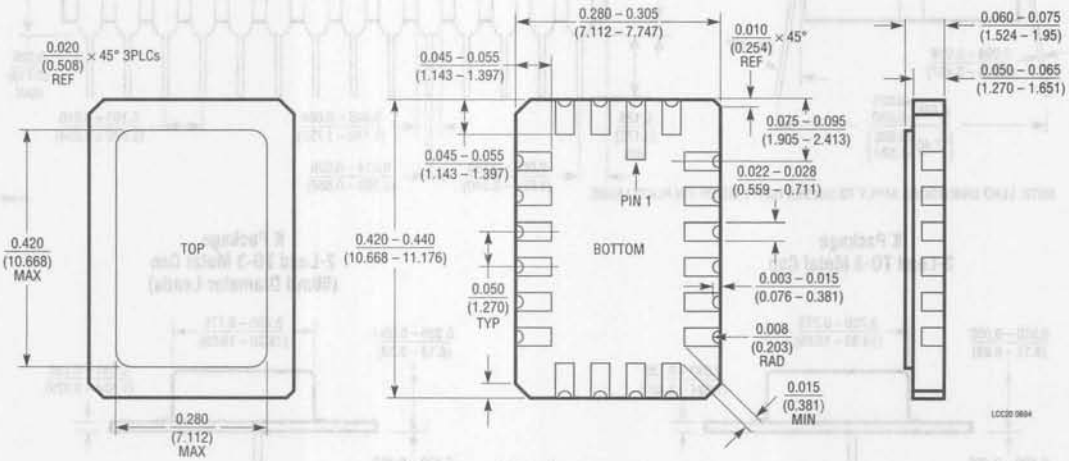
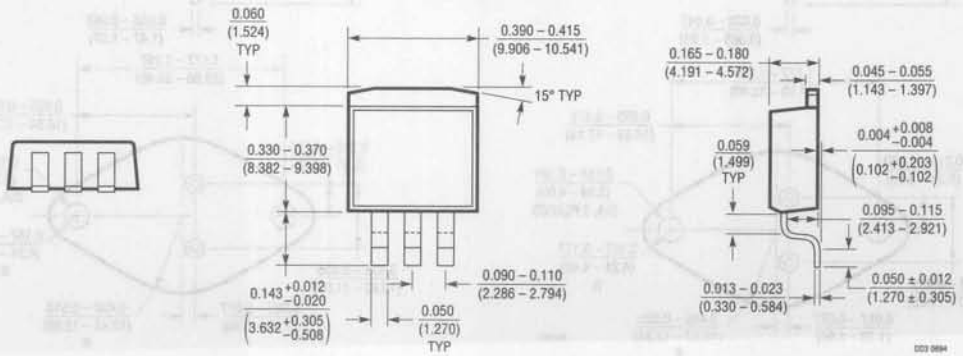
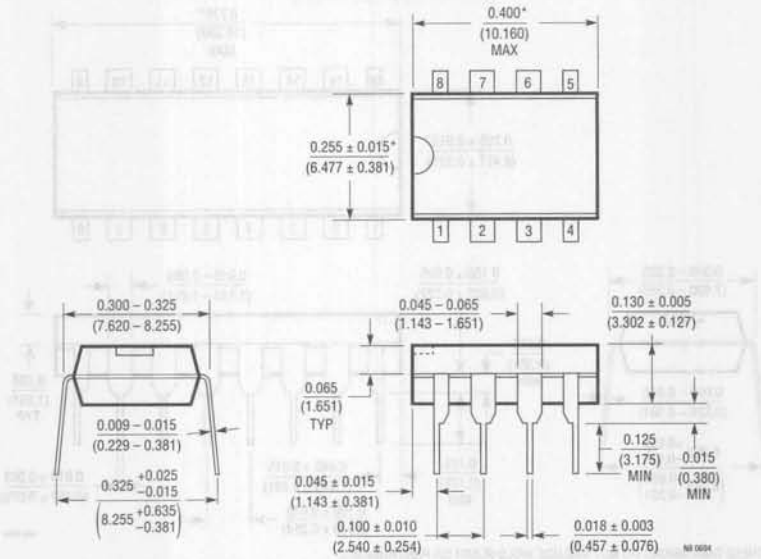
20-Pin Leadless Chip Carrier



M Package
3-Lead Plastic

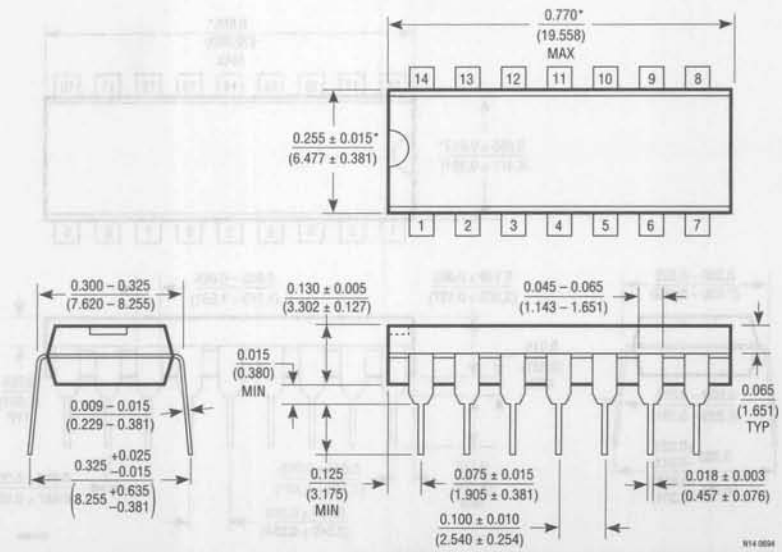


N Package
8-Lead Molded DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

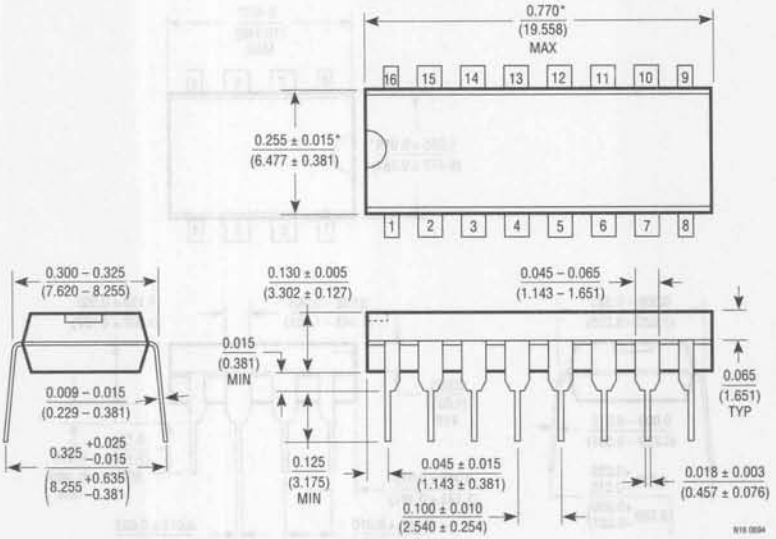
N Package
14-Lead Molded DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

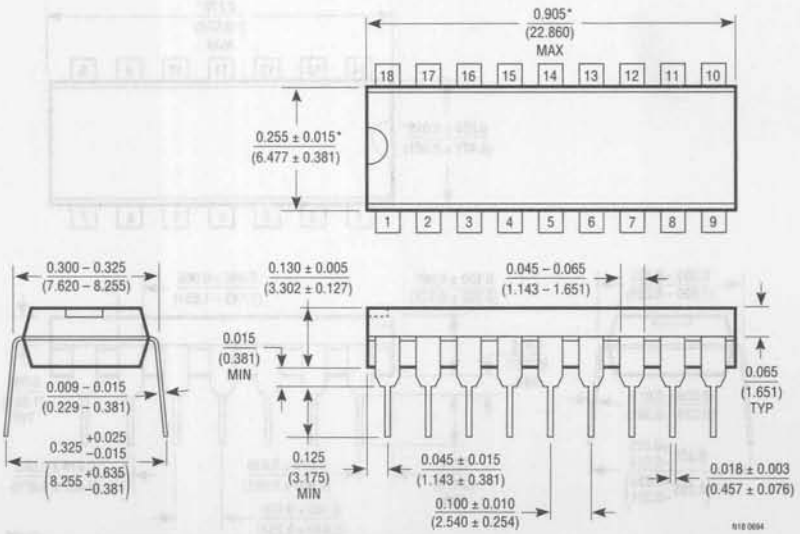
14

N Package
16-Lead Molded DIP



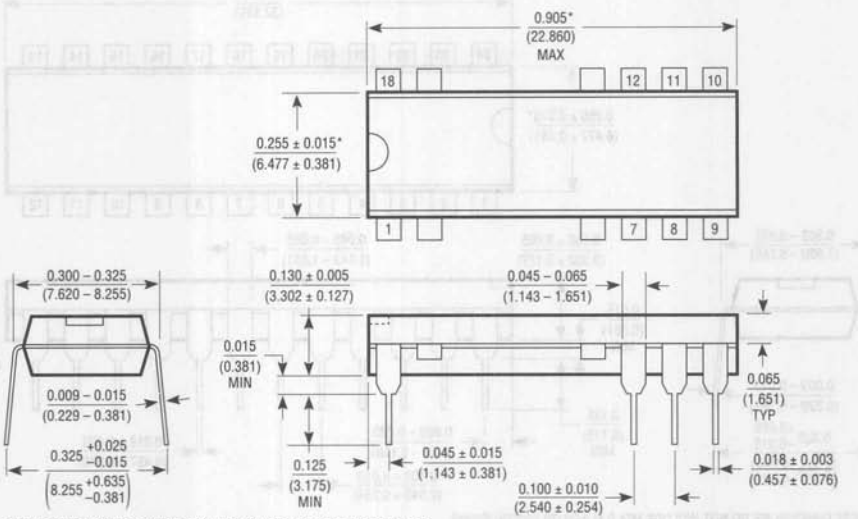
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

N Package
18-Lead Molded DIP



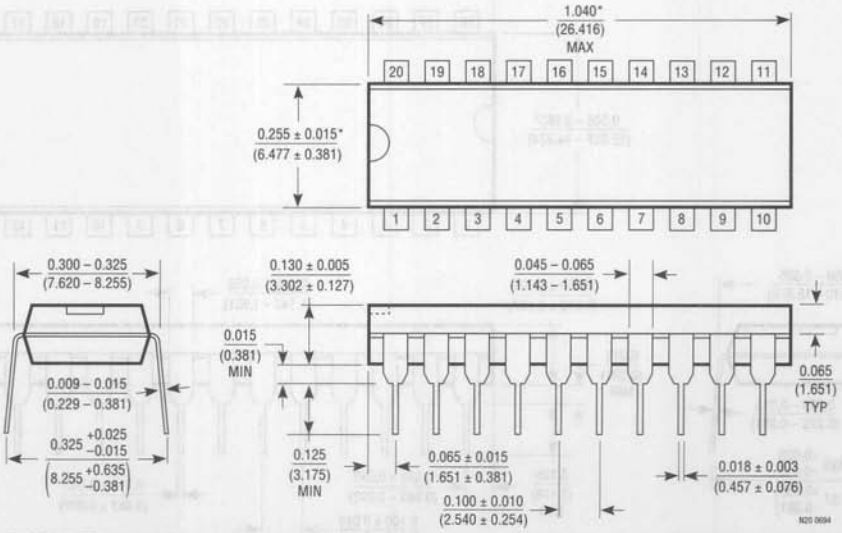
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

N Package
18-Lead Outline ISO Barrier



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

N Package
20-Lead Molded DIP

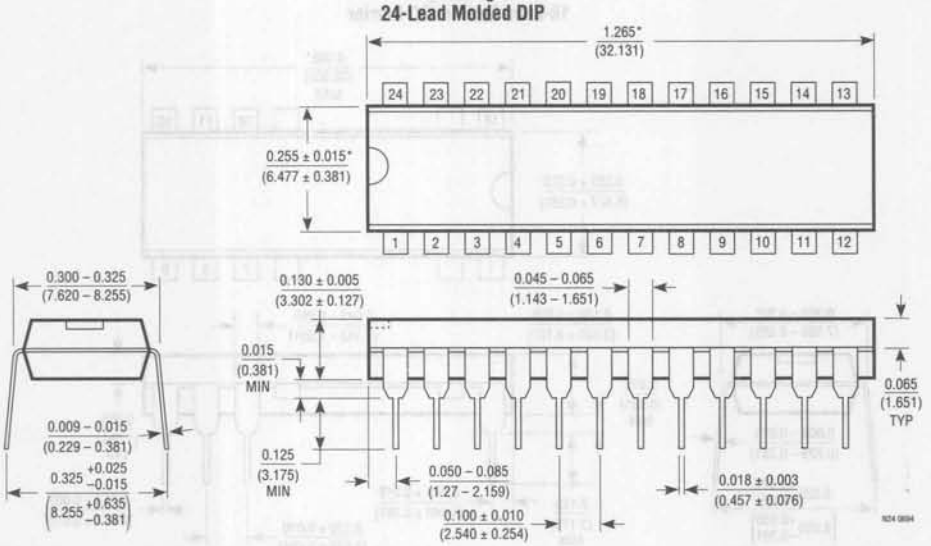


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

14

PACKAGE DIMENSIONS

N Package
24-Lead Molded DIP



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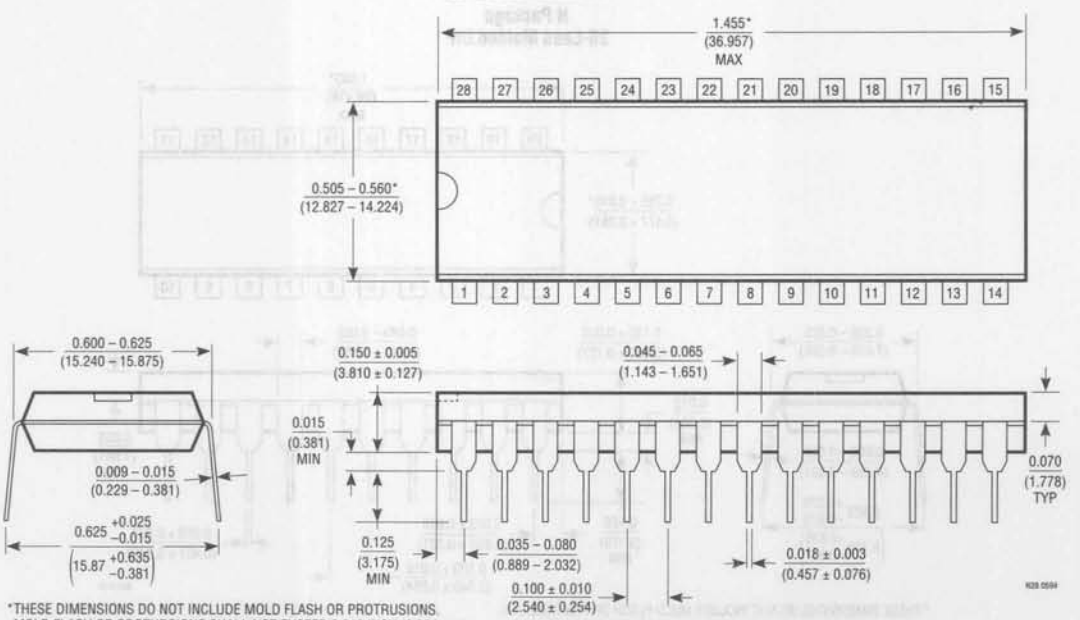
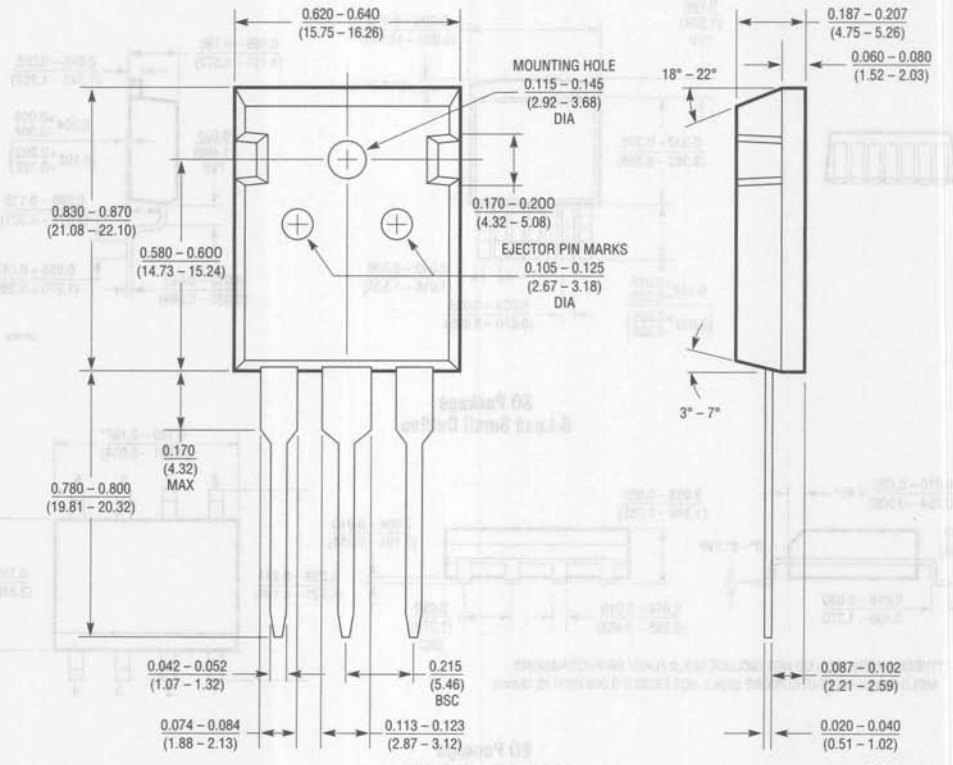
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

N Package
28-Lead Molded DIP

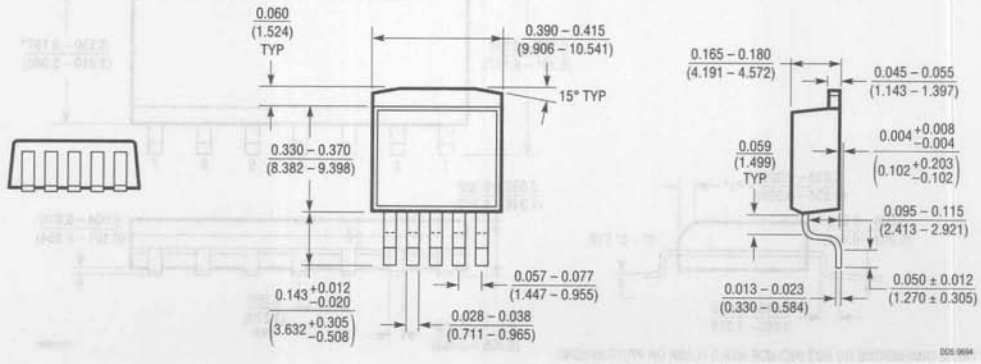


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

P Package
3-Lead TO-247



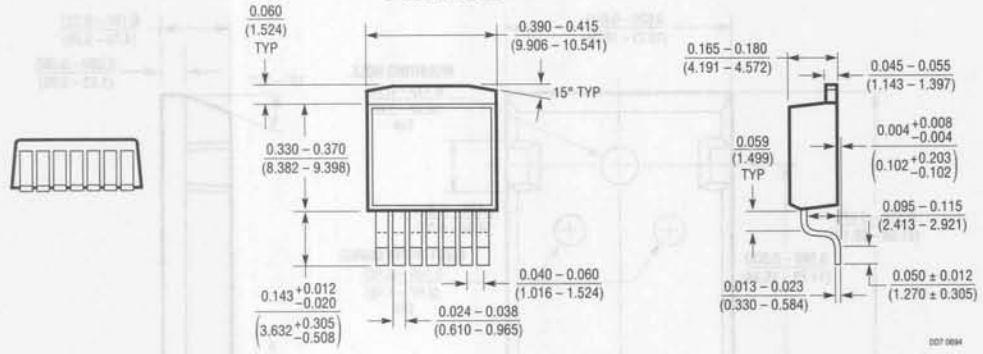
Q Package
5-Lead Plastic



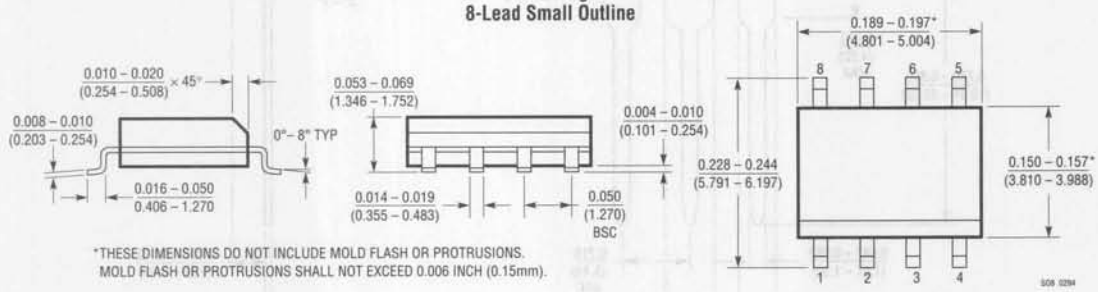
14

PACKAGE DIMENSIONS

R Package
7-Lead Plastic

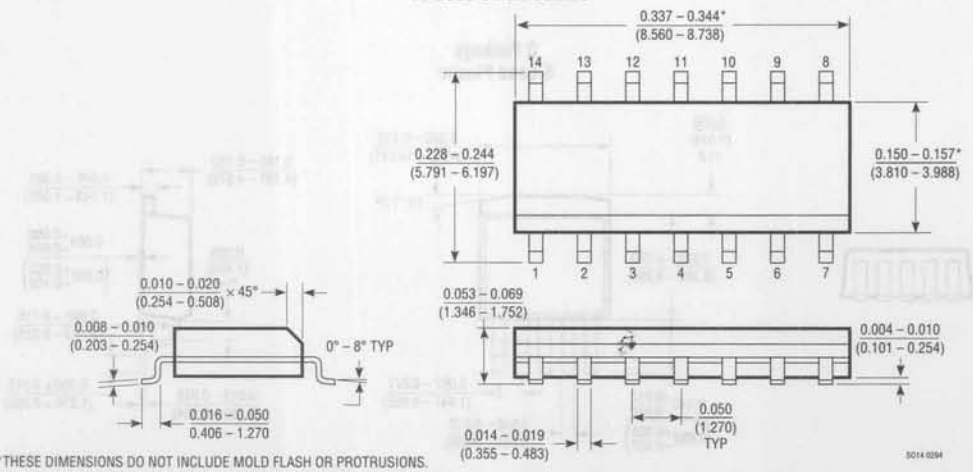


SO Package
8-Lead Small Outline



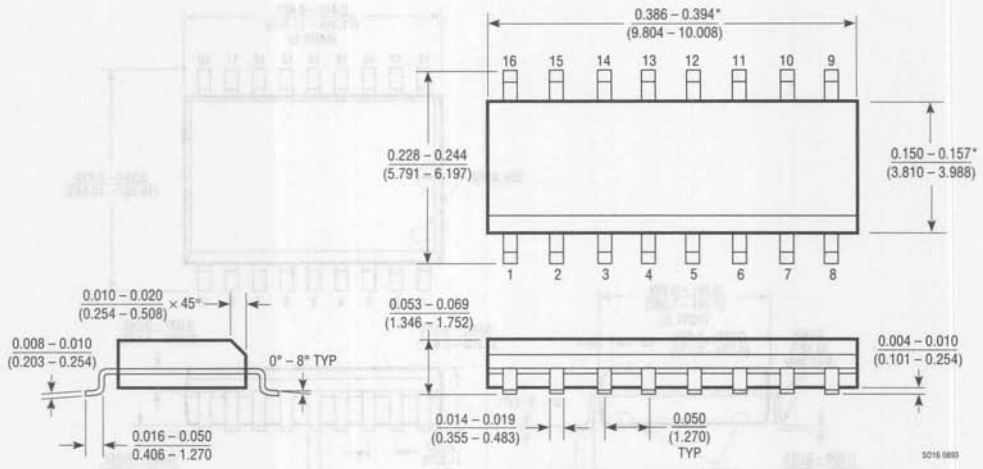
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

SO Package
14-Lead Small Outline



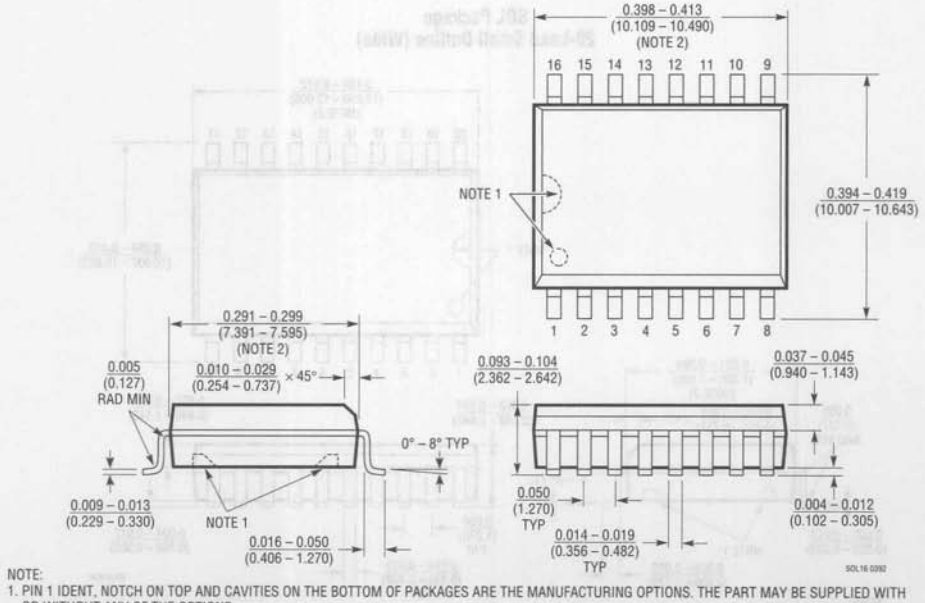
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

SO Package
16-Lead Small Outline (Narrow)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

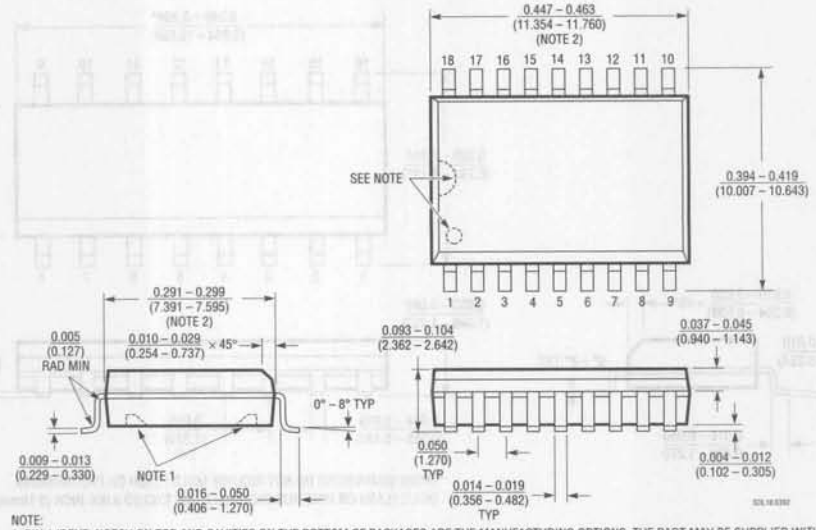
SOL Package
16-Lead Small Outline (Wide)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

14

SOL Package
18-Lead Small Outline (Wide)



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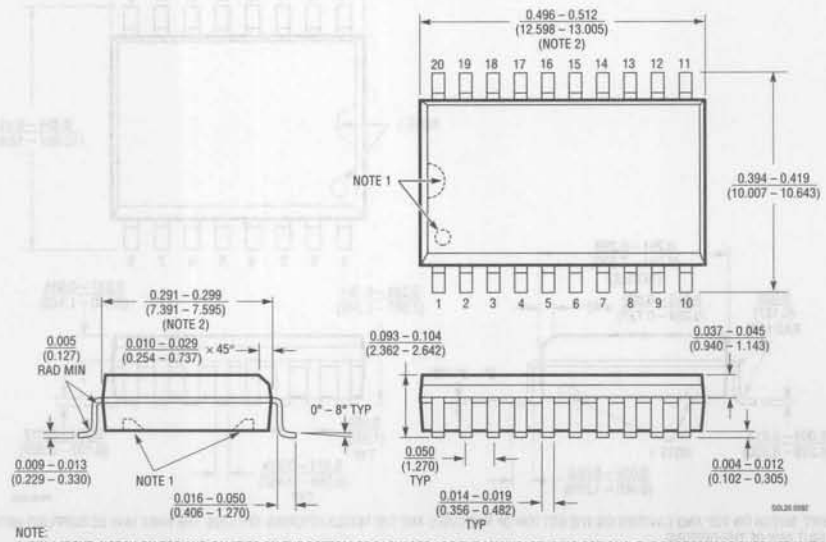
SOL Package
20-Lead Small Outline (Wide)



NOTE:
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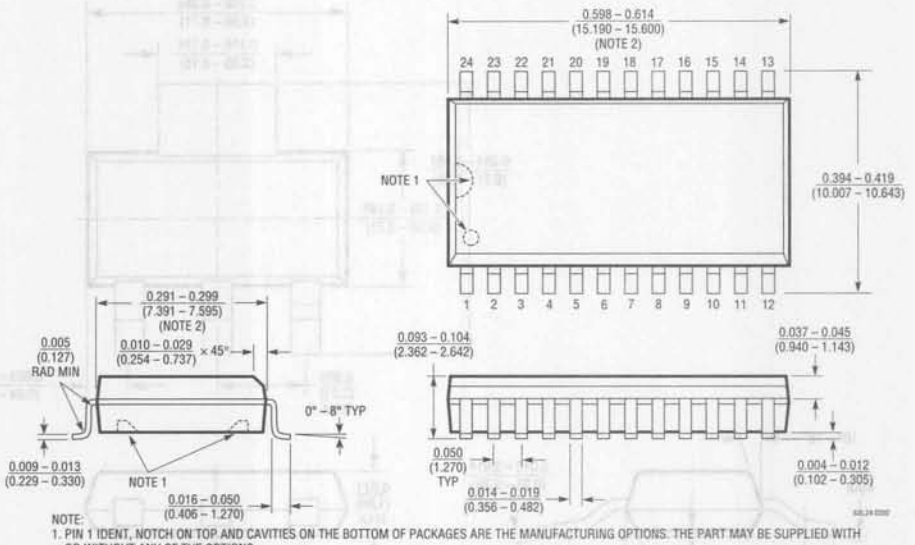
SOL Package
24-Lead Small Outline (Wide)



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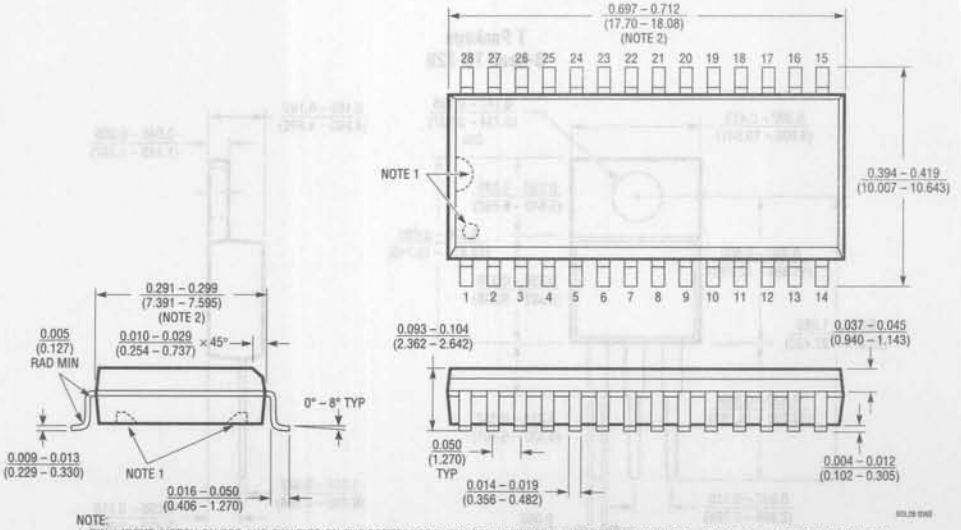
SOL Package
28-Lead Small Outline (Wide)



NOTE:
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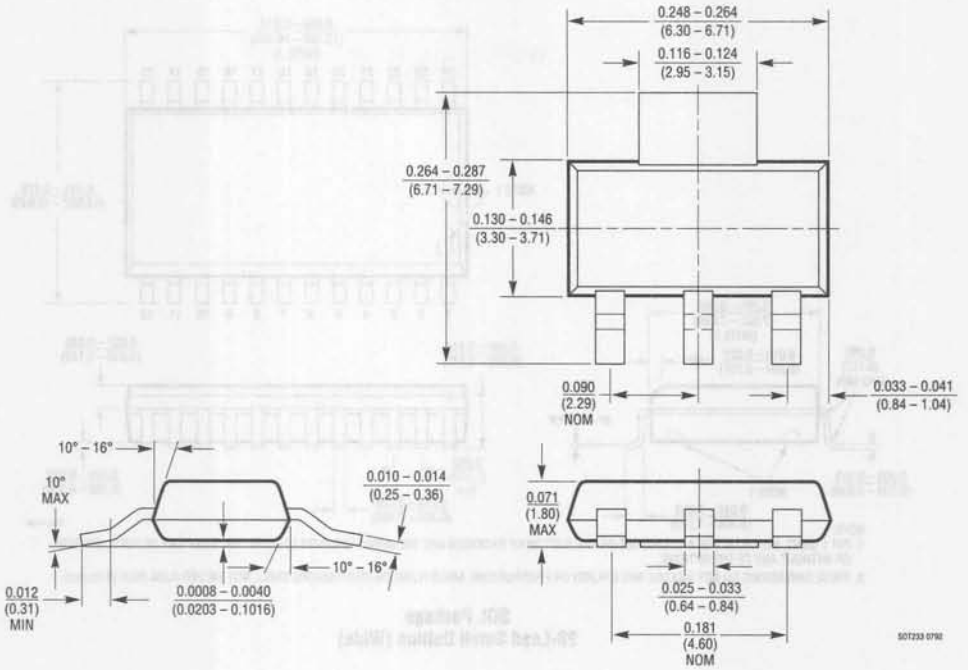
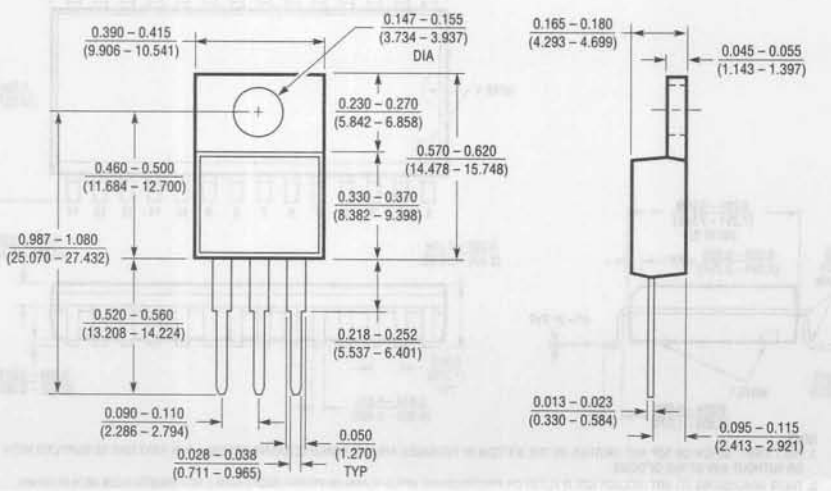
PACKAGE DIMENSIONS

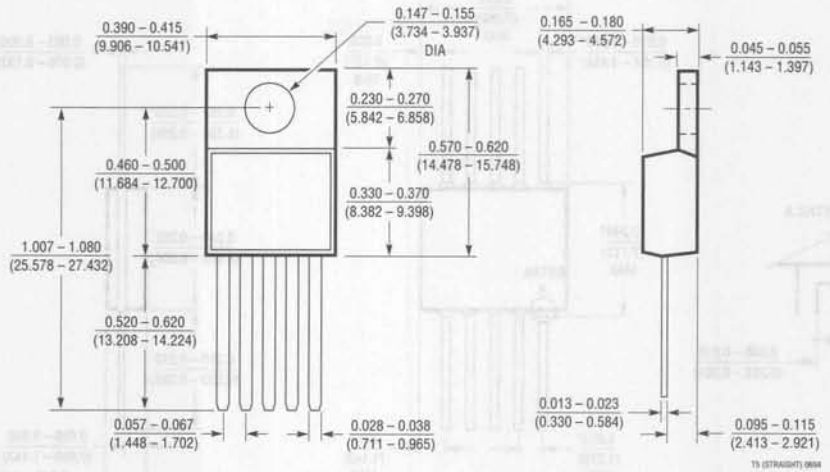
ST Package
3-Lead Plastic SOT-223



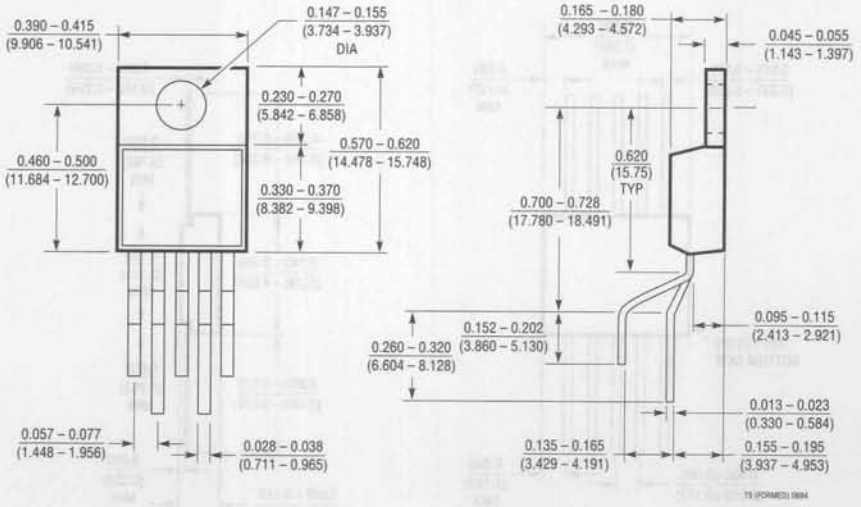
T Package
3-Lead TO-220



T Package
5-Lead TO-220 (Straight Lead)

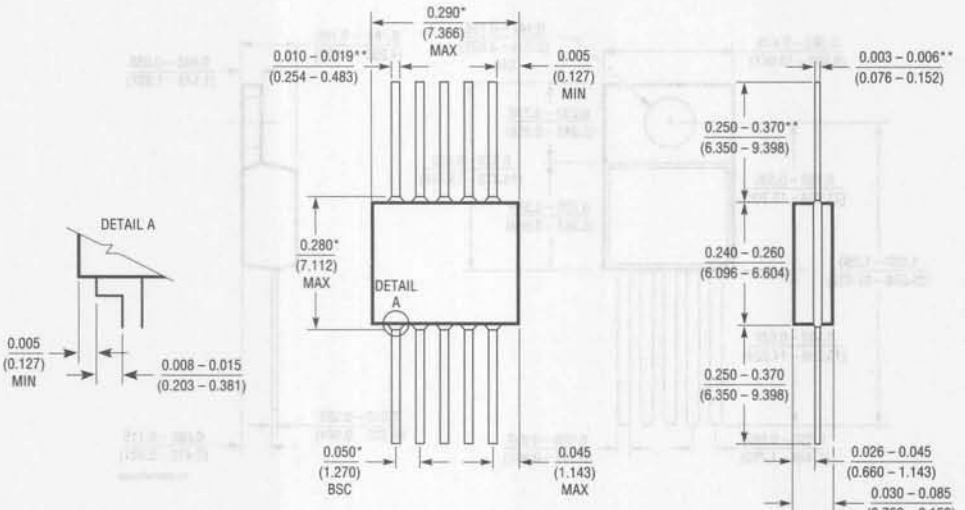


T Package
5-Lead TO-220



14

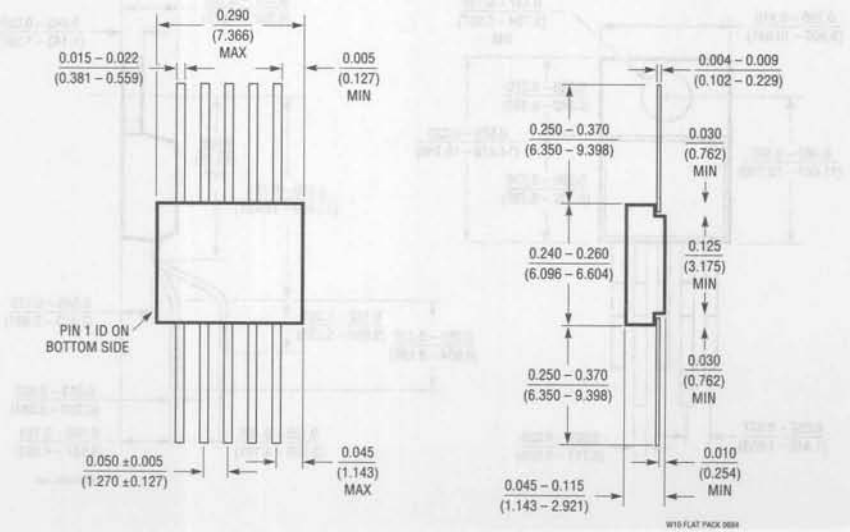
W Package
10-Lead Flatpack (Cerpak)



NOTES:
*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND CLASS OVERRUN.
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED).

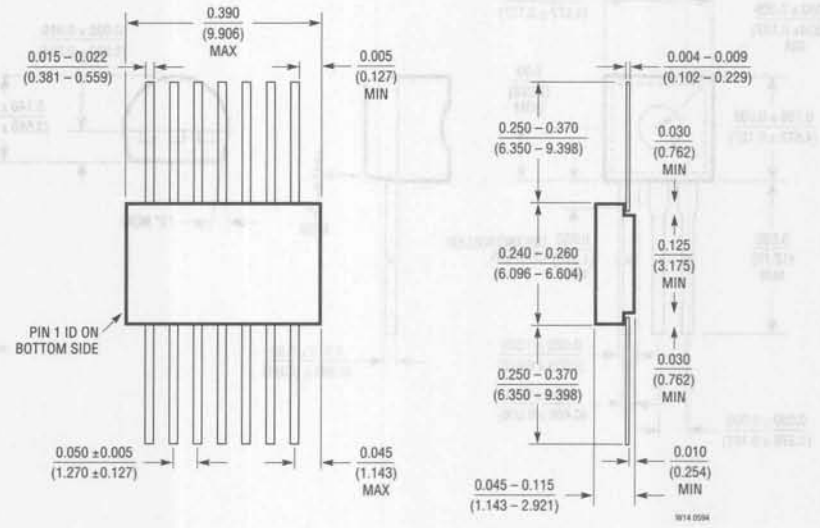
W10 0594

W Package
10-Lead Flatpack (Bottom Brazed)

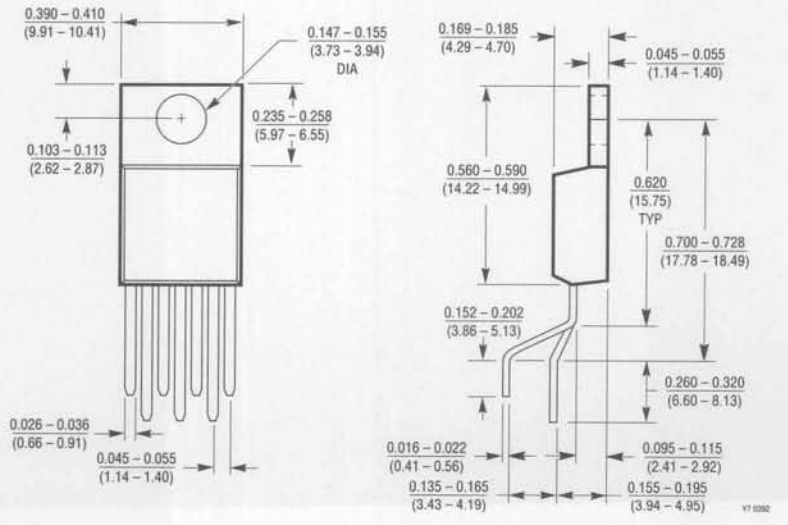


W10 FLAT PACK 0694

W Package
14-Lead Flatpack (Bottom Brazed)



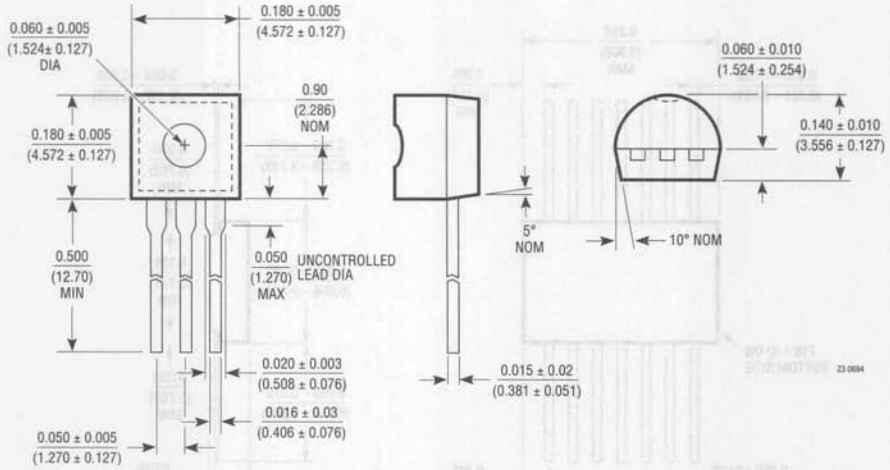
Y Package
7-Lead TO-220



14

PACKAGE DIMENSIONS

Z Package
3-Lead TO-92



SECTION 15—APPENDICES

SECTION 15—APPENDICES

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Quality and Reliability Assurance Programs

Linear Technology Corporation has a wide ranging program integrating vendor participation, design engineering, and manufacturing to produce the most reliable and highest quality linear integrated circuits available on the market. Our modern manufacturing facility in Milpitas, California is DESC Class S and Class B line certified. We have successfully completed over 90 major OEM quality system surveys to MIL-Q-9858 and MIL-I-45208 including achieving several major customer quality awards. Our Quality and Reliability Assurance Programs are summarized below:

- **Wafer Fabrication** — A modern class 100 area modular clean room construction with full environmental monitors. Emphasis is placed on statistical quality control, CV plots, SEM monitors and on our proprietary dual layer passivation system.
- **SPC (Statistical Process Control)** — LTC is committed to SPC as the cornerstone of our continuous quality improvement and Total Quality Management System (TQMS) programs. SPC is fully implemented in all manufacturing areas.
- **Assembly and End of Line** — Incoming inspection of all materials and piece-parts, line surveillance and process control monitors.
- **Testing** — Incoming inspection and acceptance of all offshore lots prior to release to test. LTX testers, multipass testing with closed loop binning to reduce outgoing electrical defective levels. Many "beyond data sheet" tests and full temperature QA lot buy-offs are performed as standard processing.
- **Traceability** — A backside or side mark is placed on all units, where space permits, to give information on each unit to identify the wafer fab lot, assembly, end of line (e.o.l.) and test lots. The information provided exceeds the seal week traceability control required by MIL-STD-883.
- **ESD (Electro Static Discharge)** — A full program is in place from design through manufacturing. Products are fully characterized to MIL-STD-883 (Method 3015) and strict controls on handling and packaging are observed.
- **Training and Certification** — Operator training has been established for all operations and recertification is performed every 6 months.
- **Major Change Control** — Major change controls are in place to notify our customers in accordance with MIL-M-38510, LTC internal specifications, or specific customer specifications as required.
- **Quality Assurance** — Full monitoring and reporting of quality data with emphasis on statistical process control charts and continuous quality improvement. Refer to our section on Quality Assurance Program.
- **Failure Analysis and Reporting** — A full analytical lab and formal program exists to record, analyze and take appropriate corrective action on all returns. A report is generated and sent to the customer stating our findings and action.
- **Reliability Flows** — Linear Technology reliability flows include Class S and Class B JAN-38510, Standard Military Drawings (SMD), DESC Drawings, 883, R-Flow, and Hi-Rel (Source Controlled Drawings). In addition, specialized processing such as SEM, PIND and other tests can be performed as required.
- **Reliability Monitor** — LTC has a unique reliability structure built into each wafer that is used to obtain rapid feedback on reliability. This data is obtained in less than 1 week, versus 40 weeks for a typical reliability audit. See the LTC Reliability Program for more details. LTC has a comprehensive reliability monitor program for plastic packaged devices. A variety of tests are performed on every 1 week date code, for every package type and lead count and real time feedback to the assembly facilities.
- **Reliability Reporting** — Data is gathered on a monthly basis for selected package/product combinations. This data is summarized each quarter and published in a Reliability Data Pack showing Operating Life, 85/85, HAST, Autoclave, Temperature Cycle, Thermal Shock, 883 Group C, and 883 Group D summary data. Copies of Reliability Data Pack summaries are available by writing or calling Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035, (800) 637-5545.

INTRODUCTION

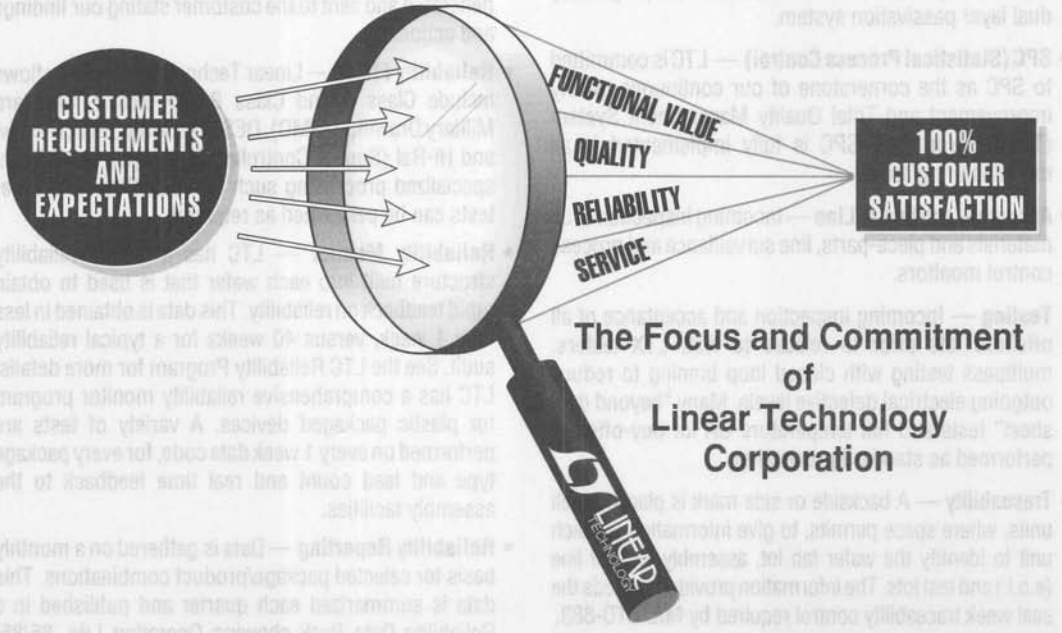
In 1981, Linear Technology Corporation was founded with the intention of becoming a world leader in high performance analog semiconductors. To achieve this goal Linear Technology Corporation committed itself to consistently meet its customers' needs in four areas:

- ❒ Functional Value
- ❒ Quality
- ❒ Reliability
- ❒ Service

Linear Technology Corporation has achieved its primary goal and is now focused to achieve 100% customer satisfaction.

This brochure defines the key elements of Linear Technology Corporation's Reliability Assurance Program which is divided into three groups:

- ❒ Reliability Planning
- ❒ Manufacturing for Reliability
- ❒ Reliability Assessment and Improvement



RELIABILITY PLANNING

Reliability planning takes three forms at Linear Technology Corporation (LTC). The first is the establishment of the reliability requirements for a product to be released to manufacturing. The second is the definition and implementation of a predictive reliability system. The third is designing for reliability, which includes new product development, materials selection, and construction techniques.

We fully realize that the cost of failure in the field is many orders of magnitude more than the initial component cost. Therefore, the goal of the reliability planning process is to provide reliable product to reduce the cost of ownership to our customers.

Reliability Criteria

A key element of reliability planning is LTC's internal specification entitled "Quality Assurance/Reliability Assurance Qualification Requirement". It contains a complete description of the interrelationships of the various groups involved in meeting LTC's reliability objectives and defines the guidelines for release decisions which affect quality and reliability of the device.

Predictive Reliability System

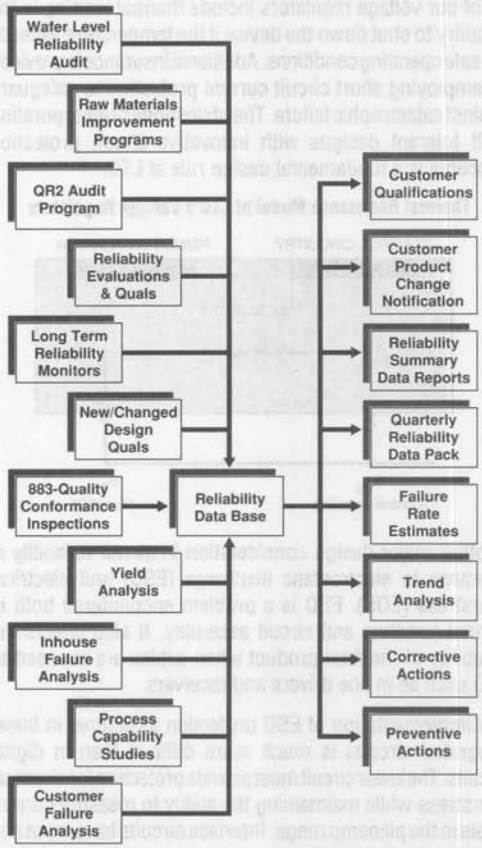
LTC has developed a predictive reliability system which combines quality and reliability information in a database to provide reliability summaries and trend analysis. A block diagram of the system is shown on this page.

Designing for Reliability

Considerable planning goes into the design of LTC's products. This planning includes device layout considerations, selection of input and output protection schemes, selection of fab processing technology, and specification of materials and manufacturing techniques.

A stringent set of bipolar and CMOS design rules have been established to enhance reliability and optimize manufacturability through robust design. At the design stage, the reliability of the circuit is heavily dependent on layout considerations. The rules for thickness and width of metallization have been defined to minimize the current density and prevent electromigration. Current density calculations are required to be performed on all products to ensure that the designs are conservative. The routing of the metal pattern is designed to eliminate potential inversion or leakage failures and guard ring structures are used where appropriate. The positions of bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires.

The Predictive Reliability System

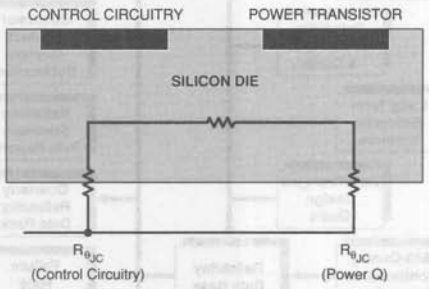


The thermal layout of our circuits also receives considerable attention to minimize parametric drift and optimize performance. In the case of voltage regulators, for any given power dissipation there will be some temperature difference between the power transistor and the control circuitry, due to their separation on the die. This temperature difference is a desirable situation which is used to reduce the power transistor's temperature affect on the control circuitry. Additionally, the power transistor has a higher maximum

junction temperature rating than that of the control circuitry and may be allowed to run warmer without degradation. Such LTC products are also designed for maximum efficiency to reduce power dissipation and thereby improve reliability and reduce the cost of heat sinking in the customer's product.

All of our voltage regulators include thermal limiting in the circuitry to shut down the device if the temperature exceeds the safe operating conditions. Additional insurance is provided by employing short circuit current protection to safeguard against catastrophic failure. The philosophy of incorporating fault tolerant designs with innovative circuit protection concepts is a fundamental design rule at LTC.

Thermal Resistance Model of LTC's Voltage Regulators



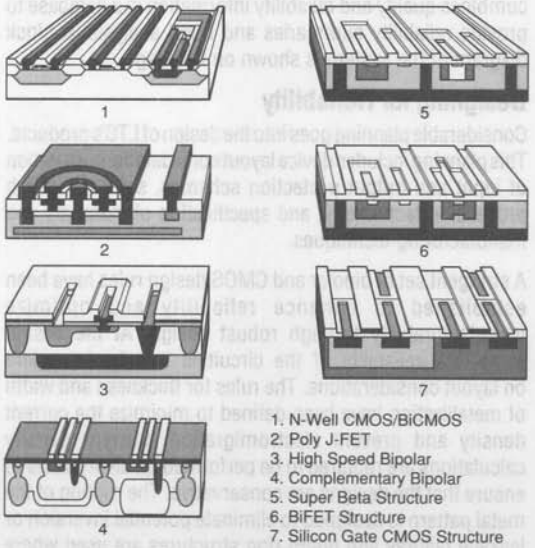
Another major design consideration in circuit reliability is tolerance to electrostatic discharge (ESD) and electrical overstress (EOS). ESD is a problem encountered both in normal handling and circuit assembly. It also affects the reliability of the final product when cables are exposed to ESD such as in line drivers and receivers.

The implementation of ESD protection structures in linear integrated circuits is much more difficult than in digital circuits. The linear circuit must provide protection for electrical overstress while maintaining the ability to measure current levels in the picoamp range. Interface circuits have input and output connections that normally operate at voltages in excess of the power supply, thereby precluding the use of clamp structures to the power supply for ESD protection. LTC, using a combination of circuit design and proprietary structures, provides high levels of overstress immunity to its devices which enhances their reliability. As a goal, all devices are designed for a minimum of 2,000 volts ESD protection with some devices achieving 5,000 volts to 10,000 volts ESD protection.

Linear circuits with total supply currents in the microamp range cannot tolerate leakages induced by contamination. Whether the circuit is Bipolar, CMOS or Complementary Bipolar, the circuit must withstand high operating voltage and high temperature for thousands of hours without leakage currents degrading device performance. LTC uses advanced process techniques to shield the die from sodium contamination while preventing electron accumulation causing surface inversions. This, combined with continuous monitoring of the assembly process, ensures high reliability devices.

LTC utilizes state-of-the-art processes in manufacturing its products. Our high voltage Bipolar process provides high gain, low noise general purpose devices as well as high power integrated circuits. CMOS can provide high complexity ICs with a large digital content. Complementary Bipolar, a new process developed in-house by LTC, provides high speed NPNs and PNPs on the same monolithic die. Complementary Bipolar enables an expanded product range for linear circuits and is suitable for very high speed amplifiers, general purpose linear signal processing or even high speed D/A converters. All of these products are characterized by high reliability, low power consumption and the ability to operate from a wide range of power supplies and over a wide range of ambient temperatures.

LTC's Process Structures



1. N-Well CMOS/BiCMOS
2. Poly J-FET
3. High Speed Bipolar
4. Complementary Bipolar
5. Super Beta Structure
6. BiFET Structure
7. Silicon Gate CMOS Structure

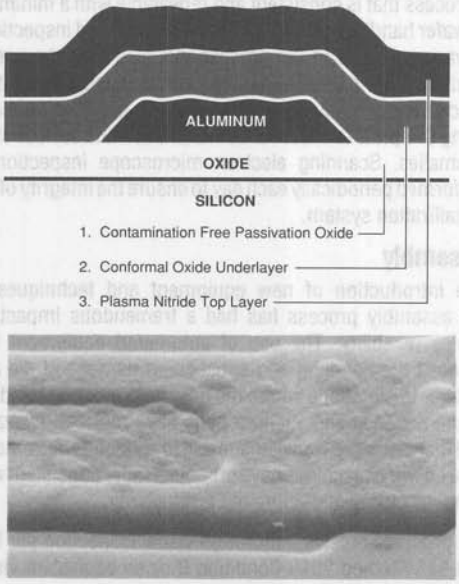
In order to ensure that device performance and reliability goals are achieved on new products, design review meetings are held regularly during the design and development phase.

Material Selection

LTC has selected assembly processes and materials that are closely matched to achieve the highest reliability level in both ultra precision and high power devices. Compatibility between the different package elements, such as the molding compound and lead frame, are carefully researched and qualified. The choice of materials and assembly processes are especially critical in surface mount devices, which must maintain reliability after being subjected to harsh board soldering environments. At LTC we are using the latest state-of-the-art assembly equipment and materials to guarantee reliability. Our low stress epoxy molding compound is extremely low in ionic impurities.

Similar improvements have been made in hermetic packages in the modern low temperature glass ceramic seals and improved die attach materials.

LTC's Dual Layer Passivation System



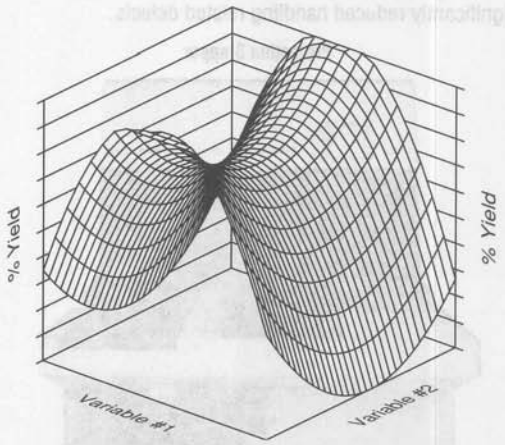
To protect the die from degradation before assembly, and from the long term effects of the package environment, LTC has developed a proprietary dual layer passivation. This dual layer passivation system is free from cracks and pinhole defects and offers an outstanding moisture barrier without detrimental side affects to device performance.

Design of Experiments

LTC is committed to the use of design of experiments (DOE) when developing new products and processes. We firmly believe that design of experiments will be the new industry standard for product and process development.

DOE has been successfully utilized on numerous products and processes at LTC. DOE, coupled with response surface methodology, has provided LTC the ability to solve complex problems that were previously unsolvable. We have used DOE to characterize wafer fab processes and provided this information to our IC designers which enabled them to produce devices that were less sensitive to manufacturing variations.

Response Surface Model of PIND Yield after Welding Operation



MANUFACTURING FOR RELIABILITY

LTC is keenly aware of the influence which the manufacturing process has on the quality and reliability of the finished product. For this reason, LTC has placed critical emphasis on the manufacturing facility and associated process controls. LTC's claims of outstanding manufacturing capability and controls are validated by the fact that we achieved Class S Certification by DESC in November of 1987.

LTC's strategy in manufacturing for reliability includes the use of automated state-of-the-art equipment, protection of the product as it moves through manufacturing, effective inspection and screening, device traceability and statistical process control. These and other similar tight controls are applied from wafer fabrication through product shipment.

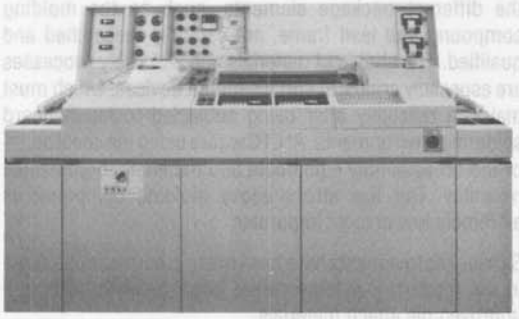
Wafer Fab

In wafer fabrication, the key to a reliable process is process control. Two major thrusts of process control in the wafer fab are the application of statistical process control (SPC) and the use of automated processing equipment. Automated equipment employing cassette-to-cassette wafer transfer, proximity mode aligners and projection steppers have significantly reduced handling related defects.

Projection Stepper

Microprocessor controlled furnaces are used to eliminate the effects of process variations and human errors. Thin film processing employs fully automated sputtering and metal etch systems.

Automated Metal Etch System



All of these equipment enhancements work together to yield a process that is consistent and repeatable with a minimum of wafer handling. Quality control monitors and inspections at various points in the process, coupled with the use of control charting throughout the fab area, ensure consistent processing. The quality of the oxide is checked regularly using C-V plots to check for contamination and surface state anomalies. Scanning electron microscope inspection is performed periodically each day to ensure the integrity of the metallization system.

Assembly

The introduction of new equipment and techniques in the assembly process has had a tremendous impact on device reliability. The use of automated equipment has reduced the handling and subsequent damage of die and wafers. In situations where die or wafers must be handled, vacuum wands and vacuum pens have replaced tweezers and thereby decreased damage due to scratches. Automated wire bonding machines have produced more consistent wire bonding quality and improved productivity.

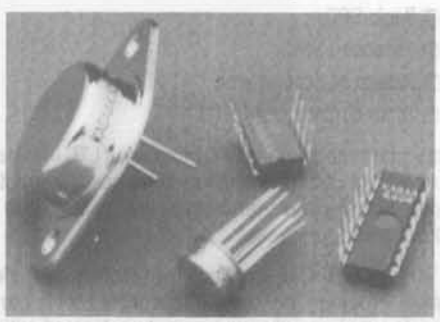
All products receive a thorough visual inspection per Mil-Std-883 Method 2010 Condition B or an equivalent visual criteria prior to encapsulation.

High Speed Automatic Bonder

Traceability

LTC has an outstanding traceability control system. A backside mark or a side mark is used to code information including the country of assembly, assembly facility, exact assembly lot seal date, wafer fab lot, die type and revision. Additionally, this backside mark will identify any non-standard processing which may have been required using a custom flow. At the wafer level, each wafer is laser scribed to include the fab run number and wafer serial number. This traceability benefit is offered as a standard feature on all packages where space allows and is part of the "added value" of LTC products.

Traceability Control Using Backside Mark or Side Mark Coding



To enhance traceability, LTC is using the latest state-of-the-art document archival system. This computerized system incorporates a document scanner which digitizes and compresses documents to be stored on optical disks. As the documents are stored, their ID number, date, and classification are recorded in the system's database to facilitate retrieval. This system allows fab travelers, test travelers and other critical documents to be retrieved in minutes as opposed to hours or days.

Optical Disk Archive System

Reliability Screening

Although our standard product families are recognized for their very low infant mortality, customer requested additional reliability screening can be provided by LTC. This added reliability screening for commercial or industrial level products is offered for both hermetic and plastic devices and is designated as our "R" flow process signified by a /R symbol as a suffix to the part number.

The "R" flow includes temperature cycle, burn-in and QA testing at 0°C, +25°C, and +70°C. A simplified flowchart of the "R" flow is shown in Table 1 at the end of this brochure. The hermetic devices are also offered as JAN Class S or Class B, Standardized Military Drawings (SMDs) and also as Mil-Std-883 devices.

LTC offers a cost effective reliability screen for hermetic product using the Mil-Std-883 screening and quality conformance inspection. This flow is defined in our "Mil-Std-883" brochure and depicted in a brief flow diagram shown in Table 2 at the end of this brochure.

The Mil-Std-883 burn-in at 125°C for 160 hours is roughly equivalent to 80,000 hours or approximately 9 years of continuous operation at a normal operating temperature of around 55°C (Assuming an activation energy of 1.0 electron volts).

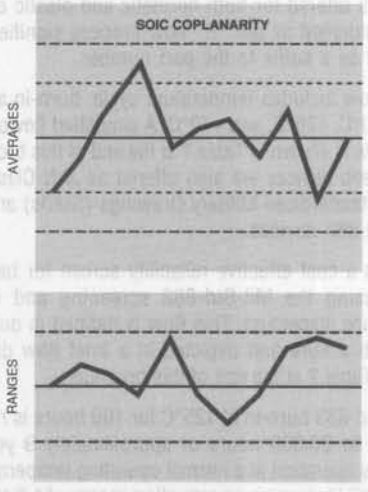
Whether testing plastic or hermetic devices, the engineers at LTC routinely add tests in addition to the standard data sheet tests. These added tests are used to detect potential flaws that could impact reliability and provide additional device compatibility with subtle application related performance characteristics. Examples of such additional tests are the exercising of thermal shutdown mode of regulators prior to burn-in or the stressing of on-chip capacitors with voltages in excess of the device maximum rating to induce failure in substandard lots.

Data sheet electrical parameters are measured before and after the specified stress testing to ensure the electrical integrity of the devices.

Statistical Process Control

At LTC we believe that quality and reliability should be built into a product as opposed to simply screening out bad devices. Statistical Process Control (SPC) is ideally suited to our manufacturing goals. SPC has enabled us to run processes with uniform and centered distributions which have not only optimized yields, but have also produced a finished product that is rugged and reliable.

Example of Control Chart for SOIC Coplanarity



Control charting at all critical processes is used to identify the need for corrective action before an out of control situation occurs, thus reducing the overall process variation. LTC has an active SPC program. The generic process from wafer fabrication through shipping has been flow charted with critical nodes defined. The Control Plan Detail outlines the various attributes of the activities surrounding that particular activity. Organization for SPC is comprised of the:

- ❒ Steering Committee
- ❒ SPC Quality Control Teams (QCTs)
- ❒ Process/Preventive Action Teams (PATs)

The Steering Committee provides the leadership for the SPC process, while the QCTs are responsible for the implementation and maintenance of SPC within their respective operational groups. PATs are formed by the QCTs to implement certain initial or corrective measures with specific stated goals, using SPC tools. There are four QCTs in place:

- ❒ Wafer Fab
- ❒ Quality and Reliability
- ❒ Local Assembly
- ❒ End-of-Line (which includes Test, Mark, Pack, Product and Test Engineering)

Since by definition, a PAT functions until its stated goal is attained, their number and tasks are constantly changing. We have had as many as 23 active PATs which include operators and maintenance personnel.

Training is provided in-house for a majority of the Company's employees, who receive test materials and 135 to 279 hours of instruction in one or more of the following courses:

- ❒ Basic SPC
- ❒ Advanced SPC
- ❒ Design of Experiments
- ❒ Team Organization

An important aspect of the SPC program at LTC involves the use of Design of Experiments to solve specific problems, develop new products/processes, and characterize new products and/or processes.

LTC is driving SPC beyond our own factory. A Preferred Supplier Program has been implemented with our raw materials suppliers, wherein parameters deemed critical to the manufacturing process at LTC are controlled statistically by the raw material supplier. Evidence of this control is supplied to LTC on a regular basis. This system of customer-supplier cooperation ensures the integrity of the materials and maintains a mutual focus on improvement.

RELIABILITY ASSESSMENT AND IMPROVEMENT

LTC combines a traditional approach to reliability which incorporates product qualification and long term reliability assessment with a "leading edge" approach, which incorporates wafer level reliability testing and in line assembly reliability monitoring.

Qualification Testing

Before a new product can be released to production, strict qualification testing requirements must be met. These same qualification requirements apply to new processes, new materials, new designs and major changes in any of these areas. The guidelines for qualification of process or product changes are detailed in Mil-M-38510. At LTC we adhere to those guidelines and in many cases impose additional testing per our own requirements. Examples of some of the qualification tests which are used by LTC are shown in Table 3 at the end of this brochure.

As part of new product qualification, LTC performs ESD sensitivity classification testing of devices to Method 3015 of Mil-Std-883. This ESD sensitivity testing uses both the human body model and the machine model. During this rigorous testing, every pin combination on at least 3 devices is subjected to 3 positive pulses followed by 3 negative pulses at the specified voltage increment with a 1 second cool down period between pulses. Following this ESD testing, the device is tested for opens or shorts on a curve tracer and then must pass the full data sheet limits on the automatic test equipment.

Additionally, for CMOS circuits, latch-up testing is performed on every pin to determine the device's ability to source or sink current without destructive latch-up. We require new LTC products to handle increasingly high currents without latch-up and subsequently meet all data sheet parameters.

Reliable radiation hardened devices are produced by LTC using a proprietary process technology designed to meet or exceed 100k RADS total dose. Qualification testing of these devices using a Cobalt 60 source has demonstrated excellent results on a number of products. Data sheets for our RAD hard product line are available from your local sales representative.

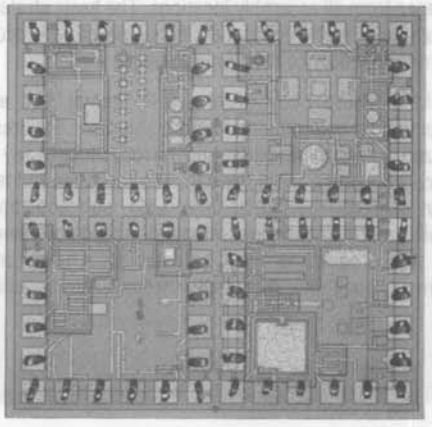
Wafer Level Reliability Assessment

As an additional reliability control, LTC has innovated a strategy for auditing the wafer fab process. Diagnostic structures, in addition to the device structures, are specifically designed as either Bipolar or CMOS reliability test patterns and are stepped into all wafers. These structures are tested during fabrication using a parametric analyzer. Then these test vehicles are used to investigate and detect potential yield and reliability hazards after assembly.

The Bipolar Process version of this structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits, namely mobile positive ions and surface charge-induced inversions. This three terminal structure is scribed from a wafer and assembled in an either hermetic or plastic package. These devices are burned-in for a predetermined temperature and time. The same structures becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a wafer fab problem which will be addressed by the process engineering group.

The CMOS Process version allows measurements of thresholds of various sizes and kinds of N-Channel and P-Channel MOSFETs. Body effects, L effective, sheet resistance, zener breakdown voltage, contact metal resistance and impact ionization current are measurable with this chip which is assembled in a twenty lead DIP.

Bipolar Test Pattern



Electrical testing is performed on the structure before and after burn-in. After evaluating any sample population shifts or failures, process engineering is appraised of the results of this process monitor.

The use of test patterns allow any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week, giving immediate feedback to the production line.

LTC utilizes this new reliability control technique in addition to the conventional reliability audit on randomly pulled finished product. Operating Life tests are performed and the distributions of key parameters before and after testing are evaluated for stability and control.

Quick Reaction Reliability Monitor

As a complement to the wafer level reliability program, a monitor program focused on assembly related issues has been fully implemented. This reliability monitor program, known as the QUICK REACTION RELIABILITY (QR^2) monitor, has been specifically tailored to provide quick feedback of reliability assessment of the assembly operation. The tests in the QR^2 program are designed to identify reliability weaknesses associated with wire bonding, die attach, package encapsulation and contamination related failures. The actual tests performed in the QR^2 Monitor Program are shown in Table 4 at the end of this brochure.

In order to ensure that representative reliability assessment is made, the QR^2 sampling matrix requires QR^2 testing of every date code from each assembly location on each package type and lead count from that assembly location. This provides a weekly snapshot of the reliability of all packages from all assembly locations. The basic strategy is to evaluate as many production lots as possible to provide maximum confidence to our customers.

Should a failure occur during QR^2 testing, the entire production lot is impounded before shipment. Failures are analyzed to determine validity and the root cause of any valid failure. Quite often, additional samples are pulled and tested for an extended period of time. Lots with substandard reliability performance are scrapped. The data generated from this program is used to establish a program for continuous quality improvement with our assembly facilities.

Long Term Reliability Monitor

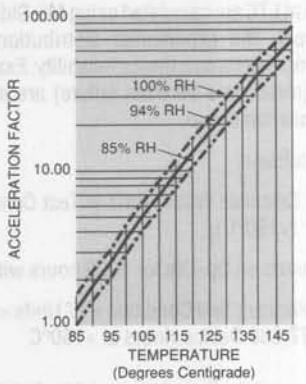
LTC also conducts a traditional long term reliability monitor program on devices pulled from Boxstock. This long term reliability monitor is used for extended life and end of life approximations such as FIT (failure in time) calculations. The long term reliability monitor also serves as a check against our short term reliability estimates.

The long term reliability tests are designed to evaluate design, wafer fab and assembly related weaknesses. Industry standard reliability tests and the relatively new HAST (highly accelerated stress test) have been incorporated into this program. The long term reliability monitor tests are shown in Table 5 at the end of this brochure.

The most severe tests for plastic package devices are the temperature and humidity tests, particularly HAST testing. We have included HAST testing in the long term reliability monitor program due to the highly accelerated nature of the this test. This test accelerates the penetration of moisture through the external protective encapsulant or along the interface between the encapsulant and the metallic lead frame. Additionally, the HAST test is conducted with the device under bias. The HAST test places the plastic devices in a humid environment of 85% relative humidity under 45psi of pressure at 130°C to 140°C. Under these conditions, 24 hours of HAST testing at 140°C is roughly equivalent to 1,000 hours of 85°C/85% RH testing. The employment of HAST testing has dramatically reduced the length of time required for qualification.

Qual Samples Being Loaded into the HAST System

Acceleration Factor Using HAST Compared to 85/85



Group C and D Testing

Since LTC is a certified producer of JAN 38510 and 883 product, we perform Group C and D testing regularly on our devices. This data is also incorporated into the reliability datapack in the back of this brochure. The Group C and D test lists are shown in Tables 6 and 7 at the end of this brochure.

Failure Analysis and Corrective Action

LTC is extremely concerned with all failures whether they occur in-house or at a customer location. We have focused significant resources in the area of failure verification and analysis.

LTC offers failure analysis services to its customers, free of charge. In an emergency situation a preliminary failure analysis report can be issued within 24 hours. Our failure analysis database revealed that the vast majority of all devices returned for failure analysis are invalid due to improper application, gross misuse or they are fully functional and meet all data sheet parameters. LTC also offers outstanding applications assistance to help the customer achieve the full value of our products.

Scanning Electron Microscope with X-RAY Dispersive Analysis

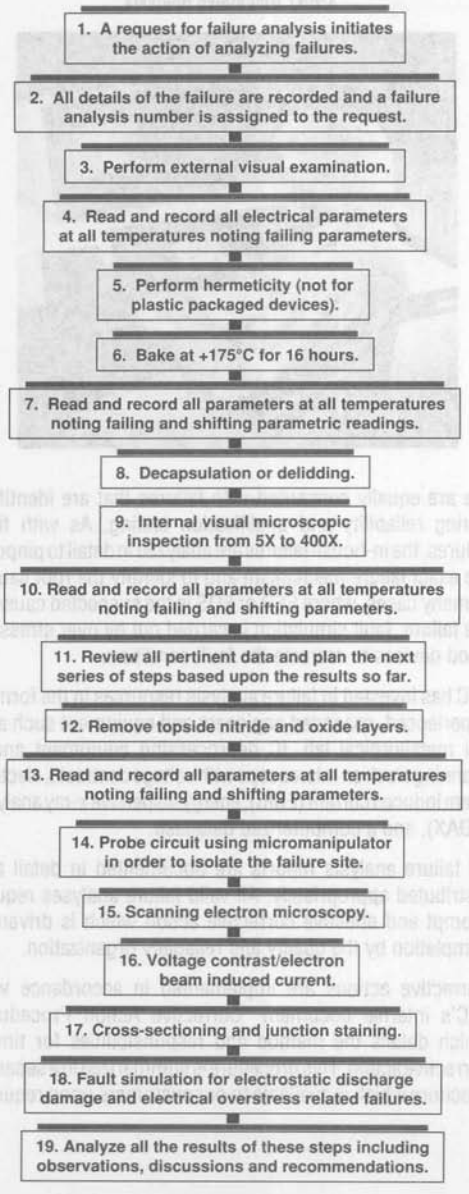
We are equally concerned with failures that are identified during reliability and qualification testing. As with field failures, the in-house failures are analyzed in detail to pinpoint the exact failure mechanism and to identify the root cause. In many cases, where ESD or EOS is the suspected cause of the failure, fault simulation is carried out by over stressing good devices to recreate the fault condition.

LTC has invested in failure analysis resources in the form of experienced, seasoned engineers and equipment such as a full metallurgical lab, IC deprocessing equipment and a scanning electron microscope with voltage contrasts, electron beam induced current (EBIC), energy dispersive x-ray analysis (EDAX), and a computerized database.

All failure analysis reports are documented in detail and distributed appropriately. All valid failure analyses require prompt and effective corrective action which is driven to completion by the quality and reliability organization.

Corrective actions are implemented in accordance with LTC's internal document "Corrective Action Procedure" which details the method and responsibilities for timely corrective action. This procedure is summarized in a separate brochure which is available to our customers upon request.

Typical Failure Analysis Flow



Failure Rate Calculations

Failure rates at LTC are calculated using Mil-Std-690B which is based upon the exponential distribution model for predicting microelectronic device reliability. Examples of FIT and MTBF (mean time between failure) are shown in the sample calculation below.

Sample Calculation:

Step 1. Calculate Failure Rate at Test Condition (+150°C).

Assume 77 units on Op-Life for 1000 hours with Ø failures:

Device Hours at Test Condition = 77 Units × 1000 Hours equals 77,000 Device Hours at +150°C

$$\text{Fail Rate} = \frac{\text{Value from Table A-1 (Mil-Std-690B)}}{\text{Device Hours}}$$

$$= \frac{91.641}{77{,}000} = 1.19\%\ 1\text{K Hours (11,900 FITS)}$$

The Arrhenius model is used to extrapolate a failure rate from an accelerated test condition to a use temperature condition.

Step 2. Calculate Acceleration Factor and Extrapolate Equivalent Failure Rate to +55°C.

Af = Acceleration Factor

$$Af = e^{\frac{E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$Af = e^{\left(\frac{1.0}{0.0000863}\right)\left(\frac{1}{328} - \frac{1}{423}\right)}$$

$$Af = 2791$$

Where:

E_a = Activation Energy (Assume 1.0 eV)
K = Boltzmann's Constant = 8.63×10^{-5} eV/°Kelvin
T_2 = Test Condition Temperature in °Kelvin
T_1 = Use Condition Temperature in °Kelvin
e = 2.71828 (Natural Antilog)

Now the equivalent failure rate is calculated:

$$\text{Failure Rate } (+55°C) = \frac{\text{Failure Rate at Test Condition}}{\text{Acceleration Factor}}$$

$$= \frac{11{,}900 \text{ FITS}}{2791}$$

$$= 4.2637 \text{ FITS}$$

Finally MTBF is calculated:

$$\text{MTBF} = \frac{100000}{0.000426} = \frac{234{,}700{,}000 \text{ Hours}}{\text{or } 26{,}778 \text{ Years.}}$$

Reliability Datapack

On a quarterly basis, the reliability department compiles and publishes a report which summarizes all the reliability testing results. This report is intended to provide our customers with a means of determining system reliability. The data is presented at +150°C and at +125°C for those customers who wish to perform their own failure rate calculations. This report can be found in the pocket in the back of this brochure.

In addition, up to the minute reliability summary data reports on particular devices can be generated from the computerized reliability database. ESD simulation testing reports and current density calculations of individual device types are also available upon request.

Should you desire additional information, please contact your local LTC representative.

Table 1. "R" Flow for Plastic Dual-In-Line Packages

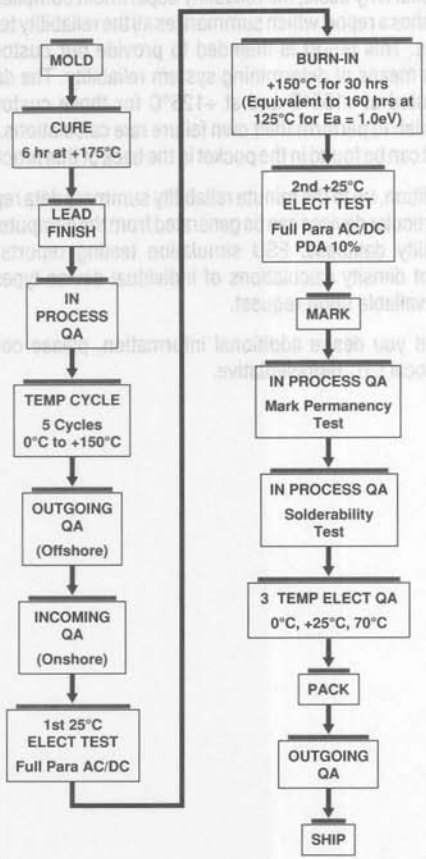


Table 2. Screening Flow per Mil-Std-883, Method 5004

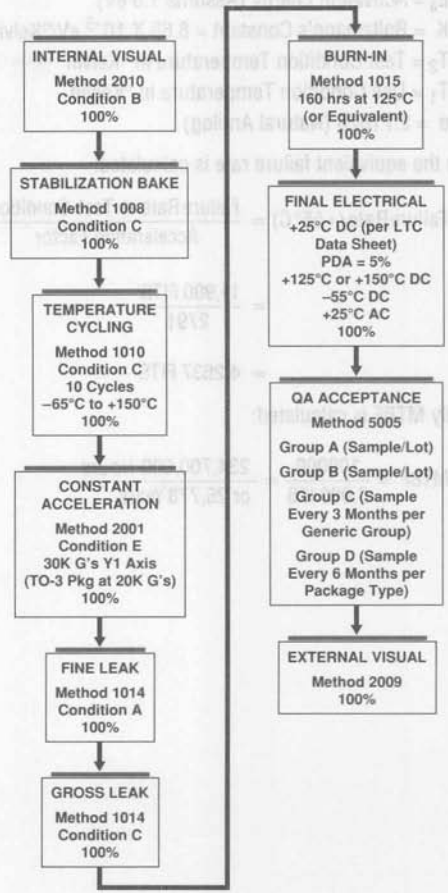


Table 3. Reliability Qualification Test Guidelines for Plastic Packages

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	CONTINGENT RELEASE DURATION	FULL AND CONTINGENT RELEASE LTPD
High Temperature Bias Operating Life (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage T_A = +125°C or T_A = +150°C	 1000 Hours 500 Hours	 500 Hours 168 Hours	 5%, Acc = 0 5%, Acc = 0
Temperature Humidity Bias Life (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = +85°C, 85% RH	1000 Hours	500 Hours	5%, Acc = 0
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = +140°C, 85% RH, 3 Atmospheres	Equivalent to 1000 Hours 85/85	Equivalent to 500 Hours 85/85	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, –65°C to +150°C, >10 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition C	Liquid-to-Liquid, –65°C to +125°C, > 5 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, Acc = 0
Autoclave (Pressure Pot with Bias) (BPPT)	JEDEC Spec 22	Continuous Storage at T_A = +105°C, 100% RH, 1.67 Atmospheres, Max Rated Supply Voltage for the Last 3 Hours	350 Hours	350 Hours	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = +121°C, 100% RH, 2 Atmospheres	350 Hours	350 Hours	5%, Acc = 0
Power Cycle (PW) Regulators Only	Mil-Std-883 Method 1006	Power Cycled "ON" and "OFF" as Required to Cycle Case Temperature Between +60°C and +120°C	50,000 Cycles	10,000 Cycles	15%, Acc = 0
Thermal Resistance (TMLR)	Mil-Std-883 Method 1012 Condition C	Junction to Case or Junction to Ambient as Appropriate	N/A	N/A	15%, Acc = 0
Dye Penetrant (DY)	Mil-Std-883 Method 1014	Immersion in Dye Penetrant at 60 PSIG for 2 Hours Minimum	N/A	N/A	15%, Acc = 0
X-Ray Inspection Radiography (XRAY)	Mil-Std-883 Method 2012	Top View Only	N/A	N/A	15%, Acc = 0

Table 4. Quick Reaction Reliability (QR^2) Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = +125°C or T_A = +150°C	168 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +85°C, 85% RH	168 Hours	45	5%, Acc = 0
— or —					
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, −65°C to +150°C, >10 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition B	Liquid-to-Liquid, −65°C to +150°C, >5 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = +121°C, 100% RH, 2 Atmospheres	48 Hours	45	5%, Acc = 0
X-Ray Inspection Radiography (XRAY)	Mil-Std-883 Method 2012	Top View Only	N/A	45	5%, Acc = 0
Package Separation Visual Inspection	N/A	30X Magnification	N/A	45	5%, Acc = 0
Unmolded Strip Evaluation	N/A	30X Magnification	N/A	1 Strip	N/A
Hot Intermittent Opens Test at Subcontractor	N/A	Automated Electrical Test at +125°C	N/A	250	N/A

Table 5. Long Term Reliability Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = +125°C or T_A = +150°C	1000 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +85°C, 85% RH	1000 Hours	45	5%, Acc = 0
— or —					
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, −65°C to +150°C, >10 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition B	Liquid-to-Liquid, −65°C to +150°C, >5 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = +121°C, 100% RH, 2 Atmospheres	1000 Hours	45	5%, Acc = 0

Table 6. Group C per Mil-Std-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group C-1 Operating Life Test (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage T_A = +125°C or T_A = +150°C	 1000 Hours 500 Hours	45	5%, Acc = 0

Table 7. Group D per Mil-Std-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group D-1 Physical Dimensions	Mil-Std-883 Method 2016	N/A	N/A	15	15%, Acc = 0
Group D-2 Lead Integrity	Mil-Std-883 Method 2004	Condition B2 (Lead Fatigue)	N/A	15	15%, Acc = 0
Group D-3 Thermal Shock Temperature Cycle Moisture Resistance Hermeticity Visual Exam End Point Electricals	Mil-Std-883 Method 1011 Method 1010 Method 1004 Method 1014 Method 1004/10	 Condition B Condition C	 15 Cycles 100 Cycles	15	15%, Acc = 0
Group D-4 Mechanical Shock Vib. Variable Frequency Constant Acceleration Hermeticity Visual Exam End Point Electricals	Mil-Std-883 Method 2002 Method 2007 Method 2001 Method 1014 Method 1010/11	 Condition B Condition A Condition E (Y1 Only)	N/A	15	15%, Acc = 0
Group D-5 Salt Atmosphere Hermeticity Visual Exam	Mil-Std-883 Method 1009 Method 1014 Method 1009	Condition A	24 Hours	15	15%, Acc = 0
Group D-6 Internal Water Vapor	Mil-Std-883 Method 1018	<5000ppm	N/A	3	0
Group D-7 Adhesion of Lead Finish	Mil-Std-883 Method 2025	N/A	N/A	15	15%, Acc = 0
Group D-8 Lid Torque	Mil-Std-883 Method 2024	(Glass Frit Seal Only)	N/A	5	15%, Acc = 0

LINEAR TECHNOLOGY

QUALITY ASSURANCE PROGRAM

At Linear Technology Corporation our overriding commitment is to achieve Excellence in Quality, Reliability and Service (QRS) and total customer satisfaction. We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the President to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, Linear Technology has established a comprehensive program called "Quality for the Nineties."

This program is divided into four separate, but highly interrelated programs, namely Quality Environment, Total Quality Management System (TQMS), Vendor Participation, and Focus for the Nineties.

Quality Environment

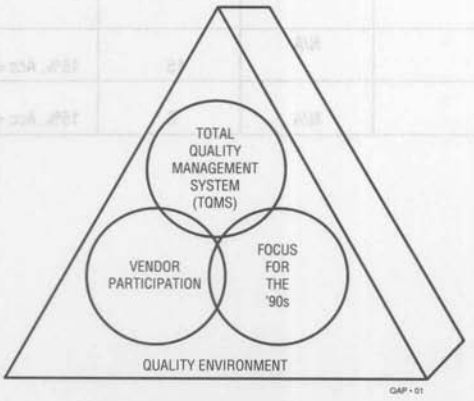
This first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conductive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

A comprehensive operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

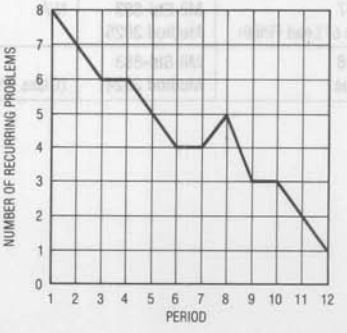
To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas and suppliers at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate Quality Assurance Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

Quality for the '90s



Systems Quality Audit-Tracking Recurring Problems

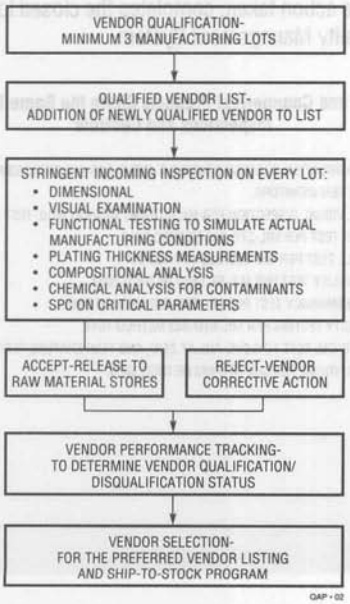


Total Quality Management System (TQMS)

The second program starts with the incorporation of innovative, but conservative, design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, Design, Product, Package, Manufacturing, Quality and Reliability Engineering groups participate in design reviews to ensure that all program aspects are covered; ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature operational life and high temperature humidity bias 85°C/85% RH and HAST (Highly Accelerated Stress Testing) for plastic packages, and MIL-STD-883 method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified.

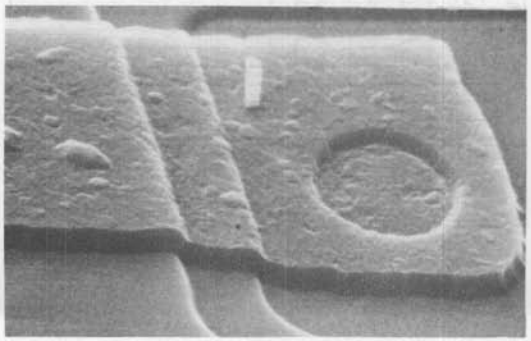
Raw Material Controls



In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

Stringent process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly, package finishing, mark and pack and shipping as depicted in the Wafer Fabrication, Assembly and Test/End of Line flowcharts.

SEM Monitor of Metallization Quality



QUALITY ASSURANCE PROGRAM

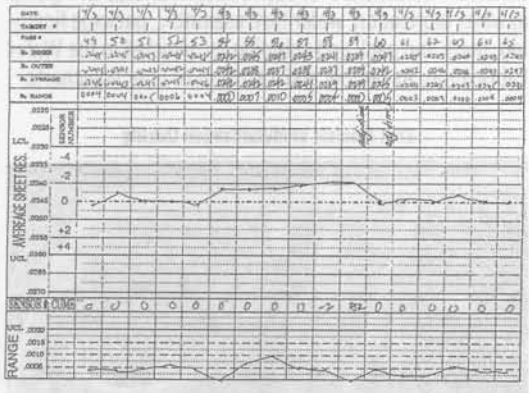
The process controls include monitors of critical assembly processes and lot acceptance inspection for operations requiring 100% production inspection. Preseal visual inspection is performed per MIL-STD-883 Method 2010 Test Condition B. Statistical process control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end of line operations. Lead finish processes have been selected that minimize solderability problems and all lots are subjected to a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Through the use of automated equipment, strict process controls (utilizing proven statistical process control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, Linear Technology is able to ensure quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Management System.

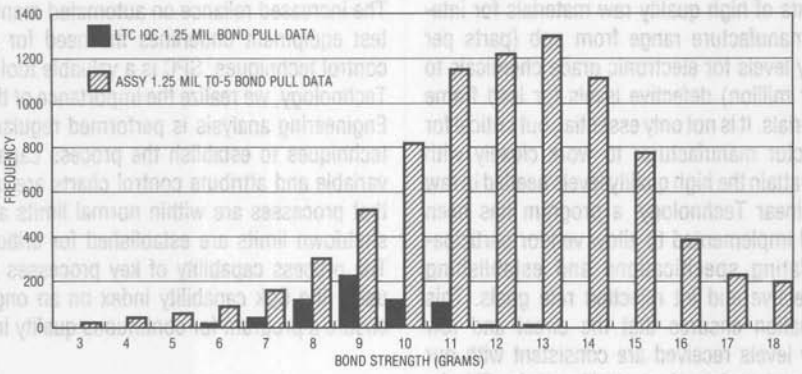
Actual $\bar{X}$ and R Chart of Aluminum Sputter Deposition Using Sensor Number Control



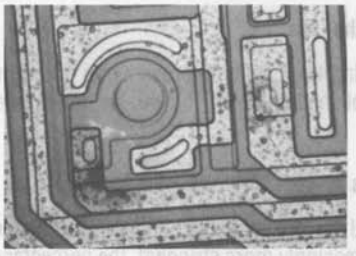
Military and Commerical Products Share the Same Stringent Inspections and Controls

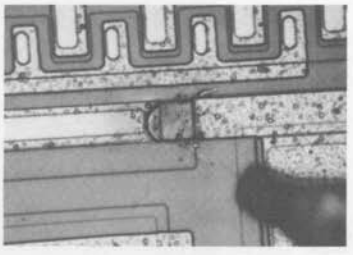
- WAFER FABRICATION PROCESS CONTROLS AND CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883 METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883 METHOD 2019.
- BOND PULL TEST PER MIL-STD-883 METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883 METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883 METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883 METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883 METHOD 2009.

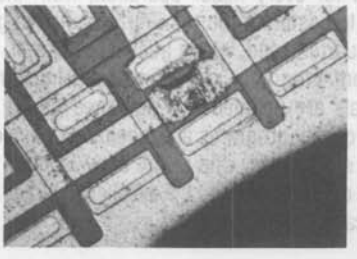
Bond Strength Histogram



Failure Analysis Photomicrographs







Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with their vendors to attain the high quality levels needed in raw materials. At Linear Technology, a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area. A Preferred Vendor Program helps to drive vendors to manufacturing excellence.

Focus for the '90s

The following key quality improvements programs have been established to meet the quality requirements of the '90s.

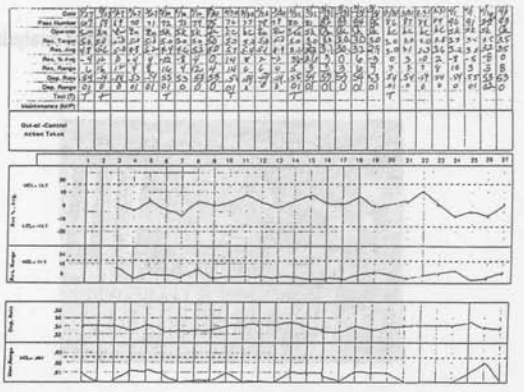
PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970s have given way to ppm goals in the '80s and '90s. At Linear Technology, ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

Statistical Process Control (SPC)

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. SPC is a valuable tool and, at Linear Technology, we realize the importance of these methods. Engineering analysis is performed regularly, using SPC techniques to establish the process capability. Various variable and attribute control charts are used to ensure that processes are within normal limits and action and shutdown limits are established for critical operations. The process capability of key processes are calculated using the Cpk capability index on an ongoing basis to ensure a program for continuous quality improvement.

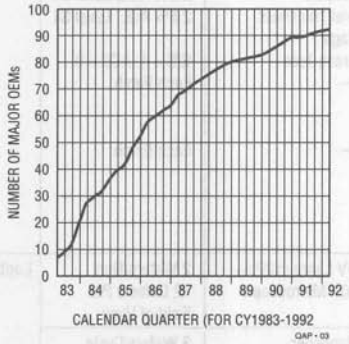
Actual Normalized X and Moving R Chart of Epitaxial Growth Reactor Controlling Resistivity and Deposition Rate



ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage, and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval

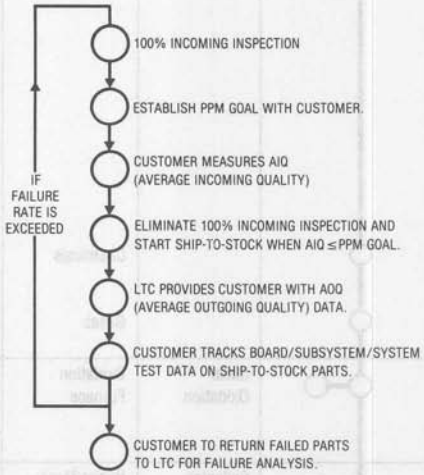


Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve our product quality and exceed the demands of our customer in the '90s and beyond.

Customer Ship-To-Stock Program

Linear Technology is working hand-in-hand with customers to consistently supply high quality products to achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and re-work costs because of higher component quality.

Ship-To-Stock Program Flow



WAFER FABRICATION FLOWCHART
Generic Bipolar Process

Vendor: Linear Technology Corporation
Package: Plastic DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Offshore
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore

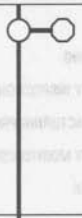
▽ INCOMING
◻ QUALITY INSPECTION AND GATE
◯ MANUFACTURING PROCESS
◯ QUALITY MONITOR/SURVEILLANCE
□ REWORK

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Incoming Raw Material Inspection	Wafers	Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination,	1X Inspection	1.0% AQL to 2.5% AQL Level 1.	% LAR Trend Chart and % Defective Trend Chart
			Oxygen/Carbon Measurement	Infrared Spectrometer	S/S = 2, ACC = 0	
			Resistivity/ Conductivity	Magnetron V/I Meter	S/S = 2, ACC = 0	
			Dimensional	Calipers	2.5% AQL, Level S1	
			Thickness and Taper/Bow	Dial Thickness Gage	2.5% AQL, Level S1	
			Orientation	Break Test	S/S = 1, ACC = 0	
			C of C Verification Against "MPS" Requirements	—	Each Batch	
		Chemicals	C of C Verification Against "MPS" Requirements	—	Each Batch	
		Gases	Plus Yearly Gas Analysis			
	Initial Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run <2 Defects Per Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
	Collector Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	Collector Implant	Implant				Logbook
	Collector Diffusion	Oxidation and Diffusion	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run <2 Defects Per Field	Logbook
		Furnace	Oxide Thickness	Nanospec	2 Wafers/Run	
			R	4 Point Probe	1 Test Wafer/Run	
			XJ	Philtec Groove	1 Test Wafer/ Cycle	

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	EPI	Deposit EPI Gemini Reactor	Visual	UV Lamp	100% for EPI Spike More Than 5/WFR is Reject	Trend Chart
				Interference Contrast Microscope	More Than 1 Slip and Stacking Fault is Reject	
			R	4 Point Probe	2 Reading/Pass	$X + R_M$
			EPI Thickness	Nicolet	2 Reading/Pass	Trend Chart
	EPI Re-Ox	Oxidation Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	2 Wafers/Run <2 Defects Per Field of View	
			Oxide Thickness	Nanospec	2 Wafers/Run	
	Isolation Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Isolation Predeposition	Boron Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
	Isolation Diffusion	Diffusion Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Logbook
				20X Microscope	2 Wafers/Run <2 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			XJ	Philtec Groove	1 Test Chip/Run	Production Logbook
			TOX	Nanospec	2 Product Wafers/ Run	
	Sinker Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	
	Sinker Predeposition	Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
			R	4 Point Probe	2 Test Wafers/Run	
	Sinker Diffusion	Diffusion Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	<3 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Test Wafers/Run	
	Base Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	ISO Diode Check	Curve Tracer BVCSO	BVCSO	Curve Tracer	4 Wafers/Run >1 Per 12 Readings is Fail	Logbook

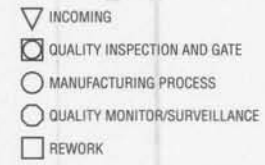
QUALITY ASSURANCE PROGRAM

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Base Predeposition	Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	$\bar{X} + R$
	Base Diffusion	Diffusion Furnace	Visual	UV Lamp	100% <10 Defects Per Wafer	Trend Chart
				20X Microscope	2 Wafers Per Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Product Wafers Per Run	
	Emitter Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	CB Diode Check	Curve Tracer	BVCBO	Curve Tracer	<1 Out of 16 Readings is Fail	Logbook
	Emitter Diffusion	Deposition Furnace	R	4 Point Probe	2 Test Chip/Cycle	Logbook
			Beta/LV	Curve Tracer	3 Sites Per Wafer Every Fourth Wafer >2 Readings Out of Spec	
	Contact Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers Per Run Lot, Accept on 0 Failures	Trend Chart
	Metal Deposition	Deposition Sputter Machine	Visual	UV Lamp	<5 Defects/Wafer 100%	Logbook
			R /Thickness	4 Point Probe	2 Readings/Pass	$X + R_M$
	Metal Mask	Resist Mask Etchant Bath	Final Inspection	Optical Microscope 200X	"Z" Pattern Scan. 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers Per Run Lot, Accept on 0 Failures	CD Logbook
	Alloy	Anneal Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Logbook
	Electrical Test	To Evaluate Electrical Parameters LOMAC			2 Wafers/Run	Logbook

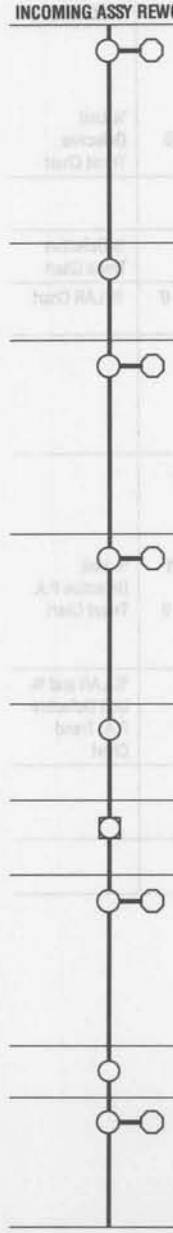
FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	LPOM	Passivation LPCVD Furnace	Visual	UV Lamp	100%, >2 Color Changes is Fail	Trend Chart
				10X Microscope	3 Wafers/Cycle <3 Defects Per Field of View	
			TOX	Nanospec	3 Wafers/Cycle	$\bar{X}$ + R
			Phosphorous Concentration	10:1 HP Etch Rate	3 Wafers/Cycle	Trend Chart
	PEN	PECVD Nitride Deposition	Visual	UV Lamp	100%, >2 Color Changes is Fail	Trend Chart
				10X Microscope	2 Wafers/Run, <5 Defects Per Field of View	
			Thickness	Nanospec	3 Wafers/Cycle	
			Index of Refraction	Ellipsometer	3 Wafers/Cycle	
	Pad Mask	Resist Mask RF Plasma Etch and Oxide Wet Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Electrical Test	Evaluate Electrical Parameters			100%	Logbook
	Backlap	Disco.	N/A	N/A	N/A	Logbook
	Backside Metal	Backside Metallization	Visual	Un-Aided Eye	100%	Logbook

ASSEMBLY FLOWCHART
Plastic DIP

Vendor: Linear Technology Corporation
Package: Plastic DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Offshore
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore



FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Wafer Sort	Electrical Test Rejects are Red Inked		Wafer Prober		% Defective Trend Chart
	Wafer Sort Monitor	Monitor Probing and 2nd Optical Quality	Probe Defects 2nd Optical Defects	3X to 75X Microscope	Minimum of 3 Times Per Shift. S/S = 1, ACC = 0	
	Kit for Overseas Assembly	Wafers are Kitted with LTC Bonding Diagram and LTC Assembly Traveler				
	Incoming Piece Parts Inspection	Lead Frame	Visual	10X to 30X Microscope	1% AQL, Level 2	% LAR Trend Chart
			Mechanical	Optical Comparator, Calipers, X-Ray Fluorescence		
			Functional (Assembly Process Simulation): Bond Pull Test Die Shear Test			
	Incoming Piece/Parts Inspection (Continued)	Molding Compound	Spiral Flow Moldability	Spiral Mold Press	1% AQL, Level 2 8 Drums for Every Transfer	% LAR Trend Chart
		Bonding Wire	Tensile Strength	Tensile Strength Tester	S/S = 1 to 5 Spools Depending on Lot Size, ACC = 0	% LAR Trend Chart X and R Bond STR Chart
		Wire	Elongation	Bonder, Bond Pull Tester		
		Epoxy Die Attach	Bondability	Die Attacher, Die Shear Tester	S/S = 20, ACC = 0	% LAR Trend Chart

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Wafer Saw	Die Separation	Alignment Accuracy	TV Alignment Micro Automation on Disco Saw 10X to 30X Microscope		% Defective Trend Chart
	Wafer Saw Monitor		Saw Quality Saw Accuracy	10X to 30X Microscope	Once Every 2 Hours, S/S = 1 Wafer, ACC = 0 S/S = 25 Die, ACC = 0	
	2nd Optical Inspection	Die Quality	Die Visual Quality	75X Microscope	Every Lot 100% Basis	% LAR and % Unit Defective Trend Chart Yield Analysis
	Die Attach	Die Bonded to Lead Frame with Epoxy		Auto Die Bonder		
	Die Attach Monitor		Visual Quality Die Shear Test	10X to 30X Microscope Die Shear Tester	4 Times Per Shift S/S = 20, ACC = 0 Per Bonder	% Defective Trend Chart. X and R Die Shear Strength Chart
	Wire Bond	Ball Bonds		Auto Thermosonic Ball Bonder		—
	Wire Bond Monitor		Wire Dress Bond Pull Strength	10X to 30X Microscope Bond Pull Tester	4 Times Per Shift S/S = 25, ACC = 0	% Defective Trend Chart. X and R Die Shear Strength Trend Chart
	100% 3rd Optical Inspection	Check for Workmanship Quality Prior to Molding	Die, Die Bond, Wire Bond Visual Quality	30X to 60X Microscope	Every Lot 100% Basis	Yield Chart
	QA 3rd Optical Inspection		Assembly Visual Quality	30X to 60X Microscope	Every Lot LTPD = 5% S/S = 45, ACC = 0	% LAR and % Unit Defective Trend Chart
	Mold	Encapsulation with Epoxy Novalac B Composition		Transfer Mold	2 Times Per Shift Per Mold 1 Shot, ACC = 0	
	Mold Monitor	Molding Quality	Visual: Chip, Void and Cracks, Misalignment, etc.	30X to 60X Microscope		% LAR Trend Chart
	Top Mark	Traceability Mark	Visual Quality	Un-Aided Eye	S/S = 15, ACC = 0	Logbook
	Post Mold Bake	Cure Molding Compound		Bake in +175°C Oven for 6 Hours		
	Mold Bake Monitor	Process Monitor	Check Oven Temperature	Mold Cure in Oven	Each Oven at Start and 1 Time Per Shift	% Failed Monitor Trend Chart

QUALITY ASSURANCE PROGRAM

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Deflash	Remove Mold Flash from Package	L/F and Heatsink Must be Free from Mold Flash			
	Deflash Monitor	Process Monitor	Visual: Incomplete Deflash, Package Damage	7X to 30X Microscope	2 Strips Every 2 Hours, ACC = 0	% Unit Defective Trend Chart
	Solder Plate	Lead Finish				
	Solder Plate Inspection	Solder Plate Quality	Coverage, Thickness, Quality	Un-Aided Eye	100%	% Defective Trend Chart
	Solderability Test	Solder Plate Quality	Minimum 95% Coverage	3X to 10X Microscope	S/S = 11, ACC = 0	% LAR Chart
	Trim and Form Singulation	Singulate Unit and Place in Black Conductive Tube				
	Mark	Date Code and Device Marking		Offset Marking with Markem 7226 or Laser Mark	Every Half Hour, S/S = 15 Units, ACC = 0 Per Machine	
	Mark Monitor	Check Marking Quality	Visual: Illegible Mark, Correct Mark, Marking Permanency Test (If Ink Marked)	Un-Aided Eye, 6 Inches Under Normal Room Lighting Method 2015 Mil-Std-883	2 Times Per Shift Per Machine S/S = 20, ACC = 0	% Unit Defective P.A. Trend Chart
	Final Visual Inspection	100% Inspect	Visual: Bent Leads, Mold Flash, Solder Quality, etc.	Un-Aided Eye to 10X Microscope	Every Lot 100% Basis	% LAR and % Unit Defective P.A. Trend Chart
	Pack	Packing and Preparation for Delivery		Antistatic Shipping Tube		
	Ship to LTC					

EOL FLOWCHART
(End of Line)

Vendor: Linear Technology Corporation
Package: Plastic DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Offshore
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore

FLOWCHART	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	LTC Incoming Inspection	Check Quality of Incoming Assembled Material	Package Dimension	Optical Comparator and Calipers	S/S = 2, ACC = 0	% LAR Trend Chart
			External Visual	3X to 30X Microscope	S/S = 76, ACC = 0	
			Mark Permanency (If Ink Mark)	Mil-Std-883 Method 2015	S/S = 4, ACC = 0	
			Solderability	Mil-Std-883 Method 2003	S/S = 3, ACC = 0	
			Die Attach Quality	Pliers	S/S = 5, ACC = 0	
			Lead Fatigue Test	Lead Fatigue Tester	S/S = 10, ACC = 0	
	100% Class Test	Electrical Test	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System		
	QA Electrical Test at +25°C	Electrical Quality	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, ACC = 0	PPM Chart
	QA Electrical Test at +70°C and at 0°C	Electrical Quality	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, ACC = 3 Skip Lot	PPM Chart
	100% External Visual Inspection	Check for Package Quality	Visual: Bent Leads, Lead Form Criteria, Mold Voids/Cracks, etc.	3X Eyepiece		Yield Chart
	QA Post Pack Inspection	Package/ Pack Quality Inspection	Verify Correct Top Mark, Correct Pack Method, Correct Labeling, External Visual Inspection	3X to 10X Microscope Inspection	S/S = 125, ACC = 0	% LAR and PPM P.A. Chart
	QA Shipbench Inspection	Plant Clearance Inspection	Paperwork Check, Verify Correct Part Number and Correct PAR Count	Un-Aided Eye Inspection	LTPD = 2% S/S = 116, ACC = 0	% LAR Trend Chart
	Ship to Customer					

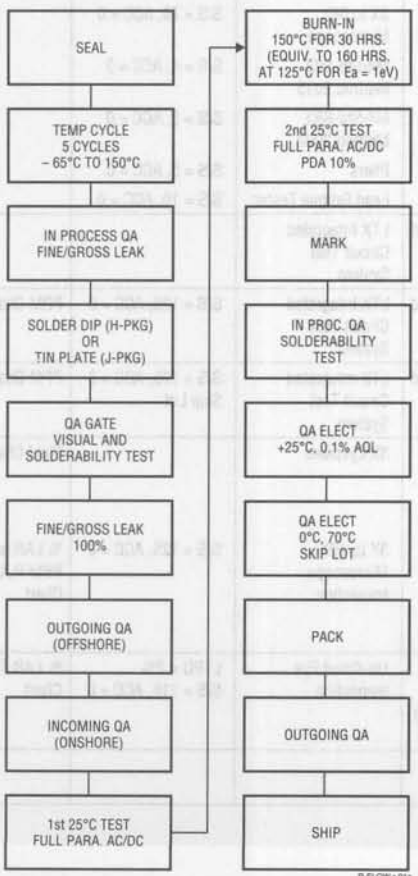
Linear Technology R-Flow

Reliability has been a key focal point at Linear Technology Corporation since our inception in 1981. Our standard product reliability is monitored closely and we have generated an extensive reliability data base for both hermetic and plastic devices. This data is published on a quarterly basis and we are seeing very low reliability failure rates in the under 1 FIT range at 55°C.*

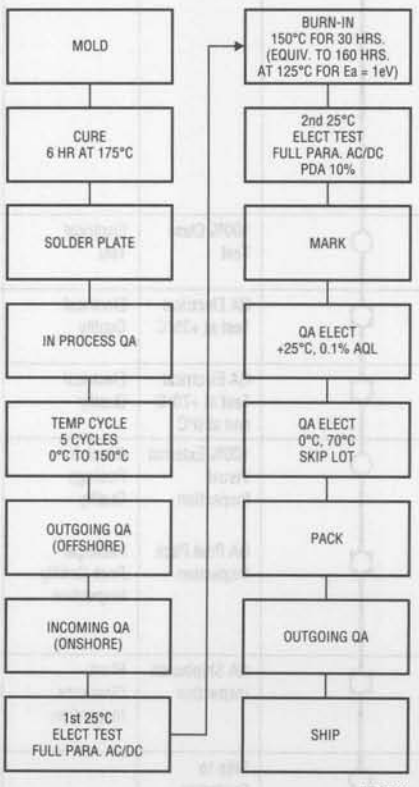
In response to customer requests, we have added an even higher level of reliability screening for commercial hermetic and plastic components. LTC's R-Flow adds an equivalent 160 hours 125°C burn-in to the standard commercial process flow. Following burn-in, a 100% room temperature test is performed and a 10% PDA (Percent Defective Allowed) is applied. This PDA limit affords an additional level of insurance on a lot-by-lot basis and prevents the occasional disparate lot from being shipped for critical applications. The additional room temperature insertion also decreases the probability of any electrical defectives in the R-Flow lot.

*1 FIT = 1 failure in 10^9 device hours.

R-Flow for TO-5 and CERDIP Packages



R-Flow for Plastic Dual-In-Line Packages



ESD PROTECTION PROGRAM

Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a trend toward greater ESD (Electrostatic Discharge Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has now become increasingly more important for all semiconductor manufacturers and users of semiconductor and other electronic components to fully understand the nature of ESD, the sources of ESD, and its impact on quality and reliability, to effectively deal with this *silent chip killer.*

Linear Technology Corporation has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability. Described in this section are the keypoints of this program.

The objective is to provide increased ESD awareness by showing the sources of ESD in the work environment, and to recommend keypoints for the successful implementation of an ESD program on a company-wide basis.

The end result of a successful ESD program would be the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We hope that this will help to convince the reader that an ESD Protection Program must be an integral part of every electronic company's product quality and reliability program.

Key Elements of a Successful ESD Protection Program

Recent improvements in failure analysis techniques to correctly identify ESD failures together with an increase in ESD related information from technical publications, EOS/ESD symposiums and vendors have significantly helped to increase ESD awareness.

The ESD Protection Program at Linear Technology Corporation was successfully launched in 1983 when production of ICs was first started. A constant upgrading of the program is still underway. During the ongoing efforts to improve product quality and reliability, previously unrecognized ESD related problems have been brought to light and corrected.

An effective ESD Protection Program must start at product design, and encompass all manufacturing and handling steps up to and including field service and repair. Our design goal is to achieve an ESD susceptibility level of 2,000V or greater.

Since the sources of static in any work environment are similar, key elements of the program successfully implemented at Linear Technology Corporation can also be applied to all users of electronic components. Where these key elements apply, static controls generic to an electronic systems manufacturer are included.

The key elements of a successful ESD Protection Program include:

1. Understanding static electricity.
2. Understanding ESD related failure mechanisms.
3. ESD sensitivity (ESD) testing.
4. Establishing an ESD task force to outline the requirements of the program, sell the program to management, implement the program, review progress against milestones, and follow-up to ensure the program is continuously improved and upgraded. Selecting an ESD coordinator to interface with all departments affected.
5. Conducting a facility evaluation to help identify the sources of ESD and establish static control measures.
6. Setting up an audit program.
7. Selection of ESD protective materials and equipment.
8. Establish a training and ESD awareness program.

What is Static Electricity?

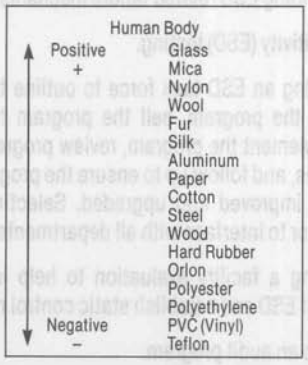
Lightning and sparks from a metallic doorknob during a dry month are examples of static electricity. The magnitude of a static charge is dependent on many variables, among them the size, shape, material composition, surface characteristics and humidity. There are basically three primary static generators, namely triboelectric, inductive and capacitive charging.

Triboelectric Charging

The most common static generator is triboelectic charging. It is caused when two materials (one or both of which are insulators) come in contact and are suddenly separated or rubbed together, creating an imbalance of electrons on the materials and thus static charge.

Some materials readily give up electrons whereas others tend to accumulate excess electrons. The Triboelectric Series lists materials in descending order from positive to negative charging due to this triboelectric effect. A sample triboelectric series is shown here. A material that is higher on the list, e.g., a human body, will become positively charged when rubbed with a material, e.g., polyester, that is lower on the list, due to the transfer of electrons from the human body to the polyester material.

Triboelectric Series



Inductive Charging

Static can also be caused by induction, where a charged surface induces polarization on a nearby material. If there is a path to ground for the induced charge, an ESD event may take place immediately. An example of an induced charge is when the plastic portion of a molded IC package acquires a charge either through triboelectric charging or other means, produces an electrostatic field and induces a charge on the conductive leads of the device. When the device leads are grounded, a short duration damaging static pulse can take place.

Capacitive Charging

The capacitance of a charged body relative in position to another body also has an effect on the static field. To see that this is true, one need only look at the equation $Q = CV$ (charge equals capacitance times voltage). If the charge is constant, voltage increases as capacitance decreases to maintain equilibrium. As capacitance decreases the voltage will increase until discharge occurs via an arc. A low voltage on a body with a high capacitance to ground can become a damaging voltage when the body moves away from the ground plane. For example a 100V charge on a common plastic bag lying on a bench may increase to a few thousand volts when picked up by an operator, due to a decrease in capacitance.

These sources of static can be found almost anywhere in an unprotected work environment, on personnel wearing synthetic clothing and smocks, on equipment with painted or anodized surfaces, and on materials such as carpets, waxed vinyl floors, and ungrounded work surfaces.

Understanding the Failure Mechanisms

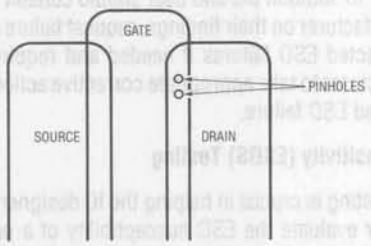
In the past, analysis of electrical failures to pinpoint ESD as a cause was often difficult. But with a better understanding of failure mechanisms and their causes, and the use of more sophisticated techniques like scanning electron microscopy (SEM), pinpointing ESD failures can now be part of a routine failure analysis.

Parametric or functional failure of bipolar and MOS ICs can occur as a result of ESD.

The primary ESD failure mechanisms include:

1. **Dielectric Breakdown:** This is a predominant failure mechanism on MOS devices when the voltage across the oxide exceeds the dielectric breakdown strength. This failure mechanism is basically voltage dependent where the voltage must be high enough to cause dielectric breakdown. As such, the thinner the oxide, the higher the susceptibility to ESD. MOS device failures are characterized by resistive shorts from the input to V_{DD} or V_{SS}.

MOS Transistor Structure
Showing ESD Included Pinholes at Gate Oxide



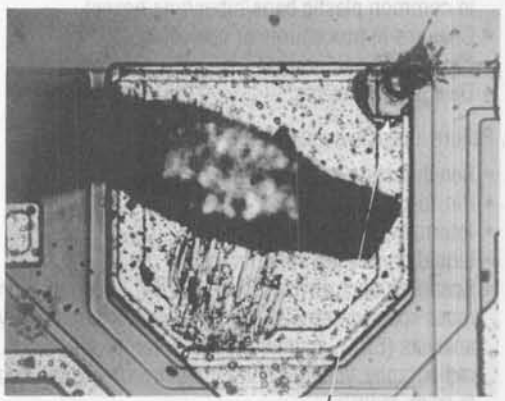
This failure mechanism can also be found on bipolar ICs which have metallization runs over active semiconductor regions separated by a thin oxide. Device failures are characterized by resistive or high leakage paths.

2. **Thermal Runaway (Second Breakdown):** This failure mechanism results in junction melting when the melting temperature of silicon (1415°C) is reached. This is basically a power dependent failure mechanism, namely the ESD pulse shape, duration and energy can produce power levels resulting in localized heating and eventually junction melting, even though the voltage level is below that required to cause dielectric breakdown. Breakdown of the emitter-base junction of a NPN transistor is a common ESD related failure mode on bipolar ICs, since the highest current density occurs on the smallest current carrying area which is typically the emitter-base junction. Low current gain (h_{FE}) is a very sensitive indicator of emitter-base junction damage on bipolar linear ICs.

3. **Parametric Degradation:** On precision, high speed ICs (e.g., bipolar operational amplifiers with a typical input bias current of 10pA and low input offset voltage of typically 50μV) ESD can cause device degradation, besides functional failures. This can impact electrical performance and adversely affect device reliability.

   This degradation in device parametric performance is far more difficult to pinpoint as an ESD related failure mode. It is also the least understood among the failure modes. The extent of this degradation is dependent on the number of ESD pulses and the level of damage sustained. The first ESD pulse may not cause an IC to fail the electrical data sheet limits, but with each subsequent ESD pulse, the parametric performance can degrade to the point where the device no longer meets the data sheet limits.

   There is a great deal of current research focused on ESD induced latent failures, and there now appears to be more evidence of this type of failure mechanism.



RESISTIVE SHORT ON A METALLIZATION STRIP OVER A THIN OXIDE N + REGION ON A BIPOLAR IC

ESD Failure Analysis Program

ESD defect identification must be an integral part of a failure analysis program. The key objectives are to help identify the ESD failure mechanism, isolate the cause for

failure, and implement corrective action to prevent recurrence. All devices suspected of being damaged by ESD after initial electrical verification, should be failure analyzed.

An ESD failure analysis program is outlined below.

1. Initial electrical test verification.
2. Review device history to determine if there are any similar failures in the past. Review ESD sensitivity data if available.
3. Investigate conditions in any area that can potentially cause ESD damage. Common potential problem areas include:
   - Proper grounding procedures not being followed (e.g., conductive table/floor mats not grounded, personnel not wearing wrist strap, etc.)
   - Improper handling (e.g., handling devices at a non-ESD protected station)
   - Transporting devices in unapproved containers (e.g., in common plastic bags/tubes/tote boxes)
   - Changes in procedures or operation
   - Changes in equipment
   - Design deficiencies
4. Failure analysis sequence:
   - Bench testing and curve tracer analysis
   - Pin-to-pin analysis
   - Internal visual (10 x to 1000 x)
   - Liquid crystal hot spot detection
   - Scanning electron microscopy (SEM), secondary ion mass spectrometry (SIMS), energy dispersive X-ray analysis (EDX), scanning auger microprobe (SAM), radiography, voltage contrast, electron beam induced current (EBIC)
   - Plasma/chemical etching
   - Special fault decoration
   - Micro-sectioning
   - Documentation

   An excellent failure analysis manual is published by the Rome Air Development Center titled "Failure Analysis Techniques—A Procedural Guide."
5. Duplication of failure by stressing identical devices. The same or similar electrical failure mode is a good indicator of an ESD induced failure mode.
6. Implement corrective action to prevent recurrence. Corrective action may include:
   - Component, board, sub-system or system level redesign
   - Improve ESD controls
   - Improve part handling
   - Improve ESD awareness
   - Improve compliance with ESD protection procedures
   - Increase audit frequencies
   - Improve packaging materials and procedures

Corrective action taken by the end user should include a thorough review of electrical and mechanical packaging designs. In addition the end user should consult with the IC manufacturer on their findings, request failure analysis of suspected ESD failures if needed and require the IC manufacturer to take appropriate corrective action on any confirmed ESD failure.

ESD Sensitivity (ESDS) Testing

ESDS testing is crucial in helping the IC designer and the end user evaluate the ESD susceptibility of a particular device. At Linear Technology Corporation ESDS testing is incorporated into the failure analysis program and is performed on each device as part of the product characterization program. The ESDS testing is also part of new product qualification. Linear Technology performs this ESDS testing according to MIL-STD-883 Method 3015.

The ESDS testing provides immediate feedback to the IC designer on any weakness found in the design and permits design correction before product release. The ESDS data collected is also used as baseline data to evaluate the effect of any future design changes on the ESDS testing performance, and to help ensure that the final packaging methods meet MIL-M-38510 requirements. Devices are categorized as either Class One, Class Two or Class Three, each with a susceptibility range from 0 to 2000 volts, above 2000 but below 4000 volts, and above 4000 volts respectively. Topside marking with equilateral triangles is specified by MIL-M-38510.

Since people are considered to be a prime source of ESD, the ESDS test circuit is based on a human ESD model. A 1500Ω resistor and a 100pF capacitor are used in the test circuit. Human capacitance is typically 50pF to 250pF, with the majority of people at 100pF or less, and human resistance ranges from 1000Ω to 5000Ω. An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical data sheet limits.

After initial ESDS testing, it is important that ESDS test monitoring be performed periodically on devices from various lots to determine lot-to-lot variation. The VZAP-2 report titled "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" published by the Reliability Analysis Center, Rome Air Development Center, contains a wealth of information on ESDS testing data on devices of different process technologies from many manufacturers. The data in this report clearly indicates a large lot-to-lot variation relating to ESD susceptibility on the same device.

Design for ESD Protection

ESD protection designs employed on Linear Technology Corporation devices include:

1. Input clamp diodes
2. Input series resistors to limit ESD current in conjunction with clamp diodes
3. New ESD Structures
4. Eliminating metallization runs over thin oxide regions when they are tied directly to external pins

ESD Task Force

An ESD task force should consist of members from each affected department to do the foundation work, sell the program to management, and implement the program with the following objectives:

1. Develop, approve and implement an ESD control specification covering all aspects of design, ESD protected materials and equipment, and manufacturing
2. Raise the level of ESD awareness
3. Develop a training and certification program
4. Work with all departments on any ESD questions or problems
5. Develop a program to educate and assist sales offices, distributors and customers to minimize ESD
6. Review and qualify new ESD protective materials and equipment, and keep specifications and training program upgraded
7. Measure the cost-to-benefit ratio of the program

Facilities Evaluation

The ESD task force should be responsible for facility evaluation. This evaluation should be guided by the ESD coordinator. The ESD coordinator should be chosen for strong knowledge of ESD controls, and for the ability to effectively interface with all affected departments. The primary objective of the task force is to pinpoint areas that represent sources of static electricity and potential yield losses due to ESD.

A representative, preferably the engineering or production manager, from each of the key manufacturing areas should be represented on this task force. At Linear Technology Corporation this effort is headed by the Quality Assurance Manager and the Package Engineering Manager. The balance of the ESD task force members are the Test Engineering, Product Engineering, and Production Managers.

The only equipment needed for this survey is a field static meter which measures static up to a level of 50kV. Both nuclear and electronic type static meters are available from manufacturers like 3M, Simco, Wescorp, Scientific Enterprises, Voyager Technologies and ACL.

Regardless of area classification, all manufacturing areas can be broken down into the following categories for evaluation purposes.

1. Personnel

Personnel represents one of the largest sources of static, from the type of clothing, smocks and shoes that they wear (for example, polyester or nylon smocks).

2. The Environment

The environment includes the room humidity and floors. Relative humidity plays a major part in determining the level of static generated. For example, at 10-20% RH a person walking across a carpeted floor can develop 35kV versus 1.5kV when the relative humidity is increased to 70%-80%. Therefore the humidity level must be controlled and should not be allowed to fluctuate over a broad range.

Floors also represent one of the greatest contributors of static generation on personnel, moving carts or equipment because of movement across its surface. Carpeted and waxed vinyl floors are prime static generators.

3. Work Surfaces

Painted or vinyl covered table tops, vinyl covered chairs, conveyor belts, racks, carts and shelving are also static generators.

4. Equipment

Anodized surfaces, plexiglass covers, ungrounded solder guns, plastic solder suckers, heat guns and blowers are also static generators.

5. Materials

Look out for common plastic work holders, foam, common plastic tote boxes and packaging containers.

Examples of typical static levels are shown in the table below.

	RELATIVE HUMIDITY	
	10%-20%	70%-80%
Walking across a carpeted floor	35kV	1.5kV
Walking across a vinyl floor	12kV	0.3kV
Picking up a common plastic bag	15kV	0.5kV
Sliding plastic box over bench/conveyor	15kV	2.0kV
Ungrounded solder sucker	8kV	1.0kV
Plastic cabinets	8kV	1.0kV

This ESD survey should include all direct and support manufacturing areas where semiconductor and other electronic components are handled, and should be extended to cover distribution and field sales offices, and field service centers. Once the facility evaluation is completed, the results are reviewed by the ESD task force, and controls are selected to combat each potential ESD problem area.

The ESD Protection Program

The degree of static control should be determined by the most static sensitive device or assembly in the operation. Top management support and implementing the same basic controls in all areas with no double standards will help to ensure success.

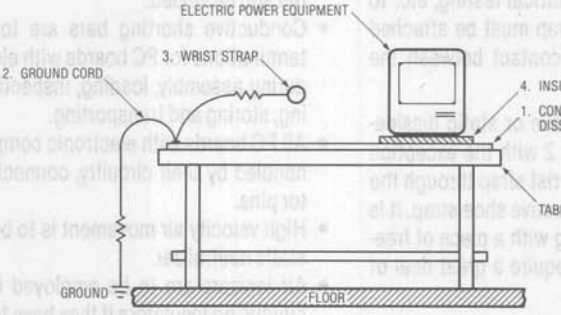
The basic concept of complete static protection is the prevention of static buildup, the removal of any already existing charges, and the protection of electronic components from induced fields. The first and foremost line of defense is the personnel wrist strap together with grounded conductive or static dissipative table tops, and conductive heel straps and grounded conductive or static dissipative floor mats.

To increase ESD awareness at Linear Technology Corporation, all ESD Protection Areas are marked by an identifying label (for example, label shown below). This label alerts all personnel that ESD protection procedures are enforced in the area.

ESD Protected Workstation

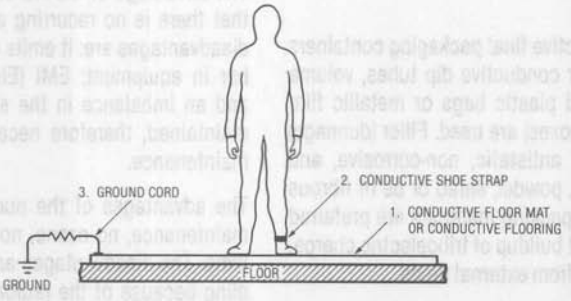
Examples of ESD Protected Workstations are shown in Figures 1 and 2.

Option 1 (Figure 1): All electronic components, sub-assemblies and assemblies must be handled at an ESD Protected Workstation only. The figure illustrates an ESD Protected Workstation consisting of a static dissipative table mat grounded to earth or electrical ground through a 1MΩ series resistor, with the requirement that the operator wears a grounded insulated conductive wrist strap with a 1MΩ series resistor. This 1MΩ series resistor protects the operator from electrical shock, should the operator come in contact with a potentially lethal voltage. Option 1 should be used where the operator does not require a large degree of freedom, e.g., during product inspection, component soldering, board repair, etc.



MATERIALS:
1. 1/16″ THICK CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT WITH SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
2. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.
3. INSULATED CONDUCTIVE WRIST STRAP WITH 1/4W MINIMUM, 1MΩ ± 10%, AND 20AWG OR LARGER INSULATED WIRE. THE CURRENT LIMITING 1MΩ RESISTOR MUST BE LOCATED RIGHT NEXT TO THE WRIST TO PREVENT THE POSSIBILITY OF SHUNTING THE RESISTOR.
4. POWER TEST EQUIPMENT MUST BE CHASSIS GROUNDED VIA A THREE-PRONG PLUG, AND PLACED ON AN INSULATION PAD MADE OF FORMICA, FIBERGLASS OR EQUIVALENT MATERIAL.

Figure 1



MATERIALS:
1. OPTIONAL 1/8″ THICK CONDUCTIVE OR STATIC DISSIPATIVE MAT OR CONDUCTIVE FLOORING (e.g., CONDUCTIVE FLOOR TILES) WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
2. CONDUCTIVE SHOE STRAP WITH A SURFACE RESISTIVITY OF $< 10^5\Omega$ PER SQUARE.
3. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.

Figure 2

Option 2 (Figure 2): Shows an alternate installation method for an ESD Protected Workstation. It consists of a conductive or static dissipative floor mat grounded to earth or electrical ground through a 1MΩ series resistor with the operator wearing a conductive shoe strap. This installation is typically used where the operator needs freedom of movement over a large area, e.g., environmental chamber loading and unloading, electrical testing, etc. To be effective the conductive shoe strap must be attached to the wearer's shoe to maximize contact between the strap and the conductive floor.

Option 3: Utilizes the same conductive or static dissipative floor mat installation as Option 2 with the exception that the operator is grounded via a wrist strap through the equipment ground instead of a conductive shoe strap. It is utilized where an operator is working with a piece of freestanding equipment and does not require a great deal of freedom of movement.

Handling

At Linear Technology Corporation all products are handled, transported and staged in volume conductive tote boxes. This offers maximum protection to the components from triboelectrically generated and inductive static charges. The rule is under no circumstances should components be removed from their approved containers except at an ESD protected workstation.

Final Packaging

Only antistatic and conductive final packaging containers (for example, antistatic or conductive dip tubes, volume conductive carbon loaded plastic bags or metallic film laminate bags, foil lined boxes) are used. Filler (dunnage) material used should be antistatic, non-corrosive, and should not crumble, flake, powder, shred or be of fibrous construction. Conductive packing materials are preferred since they not only prevent buildup of triboelectric charge, but also provide shielding from external fields.

Other ESD Preventative Measures

- Where possible, ban all static bearing materials, e.g., common plastics, styrofoam from the work environment.
- Use only synthetic material smocks with 1% to 2% interwoven steel.
- Ensure all electronic and electro-mechanical equipment is chassis grounded, including conveyor belts, vapor degreasers and baskets, solder pots, etc.
- Tips of hand soldering irons are to be grounded.
- All parts of hand tools (e.g., solder suckers, pliers, etc.) which can be expected to come in contact with electronic components are to be made of conductive material and grounded.
- Conductive shorting bars are to be installed on all terminations for PC boards with electronic components during assembly, loading, inspecting, repairing, soldering, storing and transporting.
- All PC boards with electronic components are not to be handled by their circuitry, connector points or connector pins.
- High velocity air movement is to be delivered through a static neutralizer.
- Air ionizers are to be employed in neutralizing static buildup on insulators if they have to be used or as an extra precautionary measure for extremely sensitive assemblies.
- Do not slide electronic components over a surface.

Air ionizers come in three basic types: nuclear, AC and pulsed DC. These ionizers can neutralize static charges on non-conductive materials by supplying the materials with a stream of both positive and negative ions.

The advantage of the AC or pulsed DC type air ionizer is that there is no recurring annual replacement cost. The disadvantages are: it emits ozone which can damage rubber in equipment; EMI (Electro Magnetic Interference); and an imbalance in the stream of ions if not properly maintained, therefore necessitating frequent preventive maintenance.

The advantages of the nuclear type air ionizer are low maintenance, no ozone, no EMI and no imbalance problems. The disadvantages are that it requires careful handling because of the radioactive source, and the annual recurring cost to replace the radioactive source.

The selection of air ionizers must be done with care with awareness of the above limitations. The squirrel cage ionized air blower has been proven to produce a significantly more even distribution of ion patterns than does a conventional fan blower design.

Maintenance

ESD protective floor and table coverings must be properly maintained. Do not wax over them. Cleaners must not degrade their electrical properties. Vacuum to remove loose particles, followed by a wet mop with a solution of mild detergent and hot water.

Periodic Audits

At Linear Technology Corporation periodic audits are conducted to check on the following at least once a month, unless otherwise noted.

- Compliance with ESD control procedures.
- Ensure that the conductive ground cord connection is intact by measuring the series resistance to ground with an ohmmeter.
- Ensure that wrist straps are still functional by measuring the resistance from the person to ground. The ground lead of the ohmmeter is connected to the ground connection of the wrist strap, and the positive lead is connected to a stainless steel electrode (one inch in diameter, and three inches long #304 stainless steel) which is held by the person. This test method not only checks the resistance of the series resistor, but also resistance through the ground cord and also any contact resistance between the wrist strap and the person's skin. This test procedure is required when wrist straps with an elastic nylon band with interwoven metallic strands are used, since the metallic strands breakdown with prolonged use. This monitor frequency may be shortened depending on audit results.
- Measure the surface resistivity of conductive or static dissipative table tops once every 6 months using ASTM-F-150-72, ASTM-D-257 or ASTM-D-991 test methods as appropriate.

Materials Selection and Specification

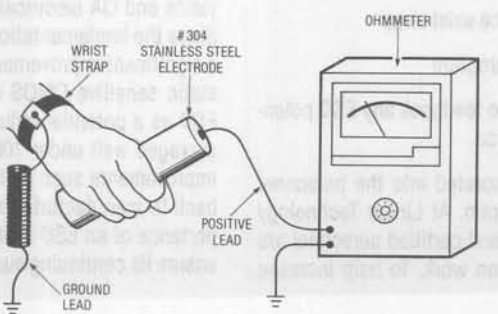
Based on the tremendous amount of ESD protective materials available, it is important that materials are selected based on a stringent qualification. Once the materials have been selected and specifications defined, a material procurement specification needs to be initiated that defines the materials and quality requirements to the vendor. One of the major pitfalls is to procure material in haste, e.g., a wrist strap, only to find out it does not perform reliably.

The SOAR-1 report titled "ESD Protective Material and Equipment: A Critical Review" published by the Rome Air Development Center is an excellent reference on the various types of ESD protective materials available.

At Linear Technology Corporation a minimum of three manufacturing lots from a potential vendor are subjected to qualification testing per the requirements of the material procurement specification for ESD protective materials. The vendor is considered qualified only when all three lots are found to be acceptable. Once vendors have been qualified, all incoming ESD protective materials are subjected to a stringent incoming inspection.

The following table summarizes a sample material and test specification for ESD protective materials.

Wrist Strap Resistance Test Set-Up



MATERIAL	PROPERTIES/DESCRIPTION	TEST METHODS
Wrist Strap	• Insulated coil cord with a 1MΩ ± 10%, ¼W minimum series resistor molded into snap fastener (at wrist end), and an elastic wrist band with inner metallic filaments and insulative exterior.	Measure series resistance with ohmmeter. Apply normal tug to both ends of strap and remeasure series resistance. Resistance must be between 0.8 to 1.2MΩ.
Conductive or Static Dissipative Table and Floor Coverings, Conductive Tote Boxes, Conductive Shoe Straps	• Must not shed particles • Must not support bacterial or fungal growth • Conductive: surface resistivity $<10^5$Ω/square. Static Dissipative: surface resistivity $>10^5$ and $<10^9$Ω/square.	Test per ASTM-F-150-72, ASTM-D-257, ASTM-D-991 (for surface resistivity $<10^6$Ω/square).
Conductive Foam	• Shall not contain more than 30ppm Cl, K, Na when a quantitative chemical analysis is performed • Must not support bacterial or fungal growth	With devices inserted into the foam, the foam must not cause lead corrosion after a 24 hour 85°C/85% RH temperature/humidity storage.
Antistatic and Conductive Dip Tubes	• Must not exhibit an oily-like film	Must meet an Electrostatic Decay test per Federal Test Method Standard 101 Test Method 4046. Material charged to 5000V must be discharged to 1% of its initial value (50V) in 2 seconds after a 24 hour conditioning at 15% relative humidity.
Antistatic and Conductive Bags	• Antistatic bags must meet MIL-B-81705 type 2 • Conductive bags must meet MIL-B-117 and sealing requirements of MIL-B-81705 • Must not support bacterial or fungal growth	Test method for antistatic bags same as for antistatic/conductive dip tubes. Test method for conductive bags same as for conductive table/floor coverings.
Static Eliminators/Ionized Air Blowers	• Ozone level: 0.1ppm maximum for 8 hour exposure • Noise: 60dB maximum • EMI: non-detectable when measured 6 inches away	Voltage Decay test: A non-conductive sheet of material charged to 5kV must be discharged to 1% of its initial value (50V) in 2 seconds at a distance of 2 feet from the ionizer or larger distance if application calls for a larger distance.

Training and Certification Program

The training program should be developed to increase ESD awareness and to assist all personnel in complying with the ESD control specification. The program should include:

1. A discussion on "What is Static Electricity?"
2. How ESD affects ICs
3. Estimated cost of ESD related losses
4. Materials and equipment for controlling static
5. The importance of wearing the wrist strap
6. The importance of an audit program
7. Encourage floor personnel to feedback any ESD potential areas to the ESD task force

ESD training should be incorporated into the personnel training and certification program. At Linear Technology Corporation only fully trained and certified personnel are allowed to do actual production work. To help increase ESD awareness, it is often a good idea to show ESD awareness films and video tapes which are available from a variety of sources (Reference 3 provides a list of films and video tapes). Personnel are retrained and recertified at a minimum frequency of once per year.

Measuring the Benefits

Where possible, the benefits of an ESD Protection Program should be tracked and quantified. The two yardsticks used at Linear Technology Corporation are final test yields and QA electrical average outgoing quality (AOQ). Since the implementation of this program, there has been a significant improvement in final test yields especially on static sensitive CMOS devices. With the elimination of ESD as a potential failure cause, the electrical AOQ has averaged well under 100ppm for all products combined. Improvements such as this help to provide positive feedback to manufacturing and support personnel on the importance of an ESD Protection Program, and also help to ensure its continuing success.

References

1. DOD-STD-1686 — Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment.
2. DOD-HDBK-263 — Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment.
3. SOAR-1 — State-of-the-Art Report ESD Protective Materials and Equipment: A Critical Review, published by the Rome Air Development Center.
4. VZAP-2 — Electrostatic Discharge (ESD) Susceptibility Data published by the Rome Air Development Center.
5. EOS-1, EOS-2, etc. — Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1979 to current year.
6. MIL-STD-883 — Test Methods and Procedures For Microelectronics
7. MIL-M-38510 — Microcircuits, General Specification for
8. MIL-M-55565 — Microcircuits, Packaging of
9. MIL-M-81705 — Barrier Materials, Flexible, Electrostatic—Free, Heat Sealable
10. FED-STD-101 — Preservation, Packaging and Packing Materials Test Procedures; Test Methods. 4046: Electrostatic Properties of

Linear Technology has an active Statistical Process Control (SPC) System. It operates via the interrelated mechanisms of: a structure, control charts with built-in contingency action plans, operational area documentation (flowcharts and control plan details), an SPC training program, each of which is defined in the Company's officially controlled SPC specification.

STRUCTURE

At the core of the SPC system are the Process (or Preventive) Action Teams (PATs). These cross-functional teams are comprised of individuals directly involved with a process element or problem. In a production operation, they typically involve production operators, lead operators, maintenance, engineering, and/or supervision. In a non-production operation, the PATs are comprised of operating employees and representatives of related functions.

Each operating group (e.g., Wafer Fab) has a formal SPC presence in the form of a SPC Quality Control Team (QCT). These SPC QCTs are comprised mostly of the manager and staff of that particular operating unit bearing the responsibility to implement and maintain SPC within their respective areas.

This QCT structure is the leadership of that operating unit, and as such, sanctions the various PATs within its jurisdiction as they implement and maintain SPC and/or solve specific problems in their respective areas. In addition, the QCT conducts monthly reviews of SPC charts, action items, and new programs.

The QCTs, in turn, report to the SPC Steering Committee. This body consists of the President, Chief Operating Officer, Vice President of Operations, Vice President of Quality & Reliability, and the SPC Manager. Thus, it has the corporate leadership responsibility for SPC at Linear Technology.

Figure 1. Linear Technology Corporation SPC Quality Control Teams

CONTROL CHARTS

The control charts at Linear Technology are manually charted by the operators to insure they are the custodians of the process, its trends, and defined corrective measures (as opposed to computerized SPC charting).

The contingency action plan, known as the Out-of-Control Action Plan (OCAP), defines the specific corrective actions when the process experiences out-of-control situations. No control chart is put in place without an OCAP. This strategy has in effect empowered the work force, while freeing the Engineering staff for systematic and continuous improvement.

FLOW CHARTS AND CONTROL PLAN DETAILS

The flow charts serve to graphically display the flow of products in each operational area, as well as define and communicate the critical nodes of that operation. The

details of each critical node are defined in the Control Plan Detail, which serves as a planning, reporting, and communication tool.

An example of a flow chart and the related Control Plan Detail for one operational area (e.g., The Wafer Fabrication Area) Figure 2, and Table 1 follows:

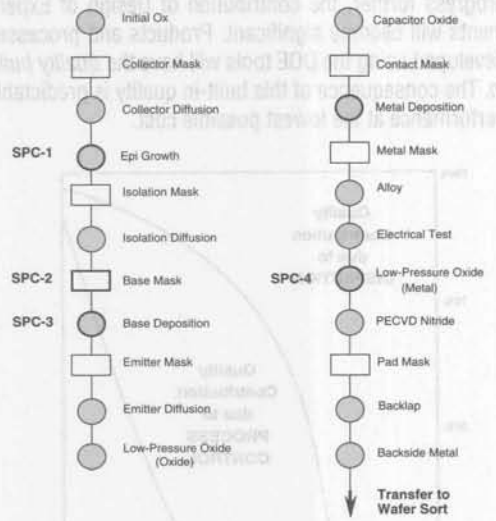


Figure 2. General Bipolar Wafer Fabrication Flow Chart

TRAINING PROGRAM

In order to pursue and continue the smooth operation of the SPC System within LTC, an all-encompassing instructional program for employees was initiated according to the following plan.

Each employee designated for SPC training is classified into one of three groups, and attends the specific classroom instruction for that classification. The courses and length of training (hours) for each group are designated in Table 2.

The content of the Training Courses is as follows:

BASIC SPC: Philosophy of SPC, concepts of variation, control, capability; tools and techniques for control and capability, including histograms, capability studies, control charting; 8D problem solving, including normality, brainstorming, cause and effect diagramming, Pareto analysis, capability index/ratio.

ADVANCED SPC: Review of basic concepts, fundamentals of Measurement System Evaluation (Gage R&R), process capability studies, determination and use of control charts, i.e., Xbar & R, Median & R, X & Moving R, p, np, u, and c chart techniques. Chart interpretation and the basics of attributes sampling system.

Table 1. Linear Technology Corporation Process Control Plan Detail for Bipolar Wafer Fab

SPC Node and Process	Critical Features	Measurement Method	Sample Size	Sample Frequency	SPC Control System	MSE (Gage R and R)	Process Capability Cp	Process Capability Cpk	Status
(SPC-1) Epi Growth	Resistivity	4-Point Probe	2	Batch	X and Moving R Chart with Adaptive Control	Acceptable	1.59-1.89	1.12-1.41	On Line
(SPC-2) Base Mask	CDs	OSI-VLS1	1 Site/ 3 Wafers	Batch	Xbar and R Chart with Adaptive Control	Acceptable	1.54	1.54	Out of Control
(SPC-3) Base Deposition	Sheet Resistance	4-Point Probe	3 Sites/ 3 Wafers	Batch	Xbar and R Chart	Acceptable	1.64-1.70	1.59-1.63	On Line
(SPC-4) LPOM	Thickness	Nanospec	5 Sites/ 3 Wafers	Batch	Xbar and R Chart	Acceptable	1.82-2.31	1.74-1.94	On Line

Table 2.

Group #	Trainee Audience	Basic SPC	Advanced SPC	D.O.E.	TEAM ORG.	TOTAL
1	Engineering (Technical)	15	20	24	4	63
2	Management/Supervision Technicians	15	20	—	4	39
3	Operators	15	—	—	—	15

DESIGN OF EXPERIMENTS: Philosophy and need of experimental design, experimental methodologies utilizing Fisher & Taguchi concepts. Response Surface Methodology for parameters and tolerance designs, including ANOVA, and analysis of co-variance.

TEAM ORGANIZATION: An outline of the SPC organization within Linear Technology, the concepts of the SPC Quality Control Teams (SPC QCTs) and Preventive/Process Action Teams (PATs). Strategies for Detailed Control Plans and Out-of-Control Action Plans (OCAPs). Concepts of team effectiveness.

Manufacturing Excellence

One of the Linear Technology goals is *manufacturing excellence*. The traditional SPC techniques seek to produce processes that are capable and in control. To improve those processes and to determine rational parameters and specification tolerance of new products and processes requires the *Design of Experiments* (DOEs) methodology.

Linear Technology actively pursues the screening techniques described by Fisher as well as the optimization techniques of Box and Taguchi. These latter techniques, known as *Response Surface Methodology* and *Taguchi Methods*, are particularly useful in developing robust products and processes, with a minimum of sensitivity to process variation.

Contribution to Quality

Contribution to quality improvement has evolved from one dominated by ATTRIBUTE INSPECTION (pass/fail) to one involving a mixture of SPC and attribute inspection. As we progress further, the contribution of Design of Experiments will become significant. Products and processes developed using the DOE tools will have the *quality built-in*. The consequence of this built-in quality is predictable performance at the lowest possible cost.

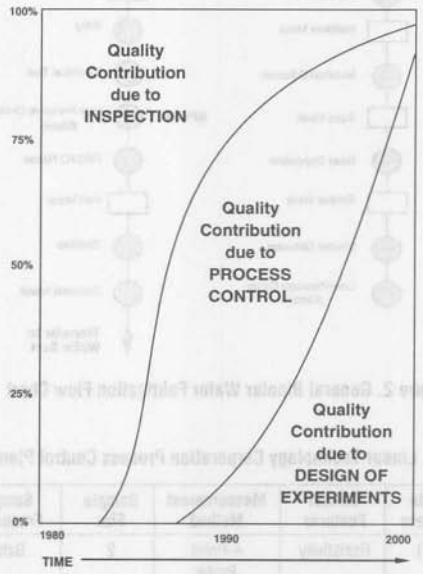


Figure 3. The Semiconductor Quality Evolution

The concepts of SPC and DOE have already been institutionalized within Linear Technology and will provide the methodology to ensure a process of continuing improvement.

Introduction

Linear Technology Corporation was founded in 1981 to address the growing demand for high performance and superior quality linear integrated circuits.

Today, Linear Technology has successfully established a leadership position by introducing and supplying leading edge products in each of the industry's basic functional groups — op amps, comparators, voltage regulators, references, switched-capacitor filters, interface, data conversion, and a variety of special function CMOS devices, in all major package styles.

Early on, Linear Technology made the commitment to provide advanced technology, *surface mount packaging.* This made Linear Technology the first company to offer true precision and high performance linear devices across the full range of functional categories, plus many of the popular second-source devices in JEDEC Standard SO-8, 14, 16 and SOL-16, 18, 20 and 28 pin packages.

The continuing demand for more complete surface mount designs has spurred the introduction of two power surface mount packages by LTC — the 3 lead SOT-223 and the DD package available in 3, 5, and 7 lead versions. Many LTC power products are now being introduced in these packages which, for the first time, enables high power designs to be realized using 100% surface mount devices. Support for Linear Technology's surface mount devices includes service for tape and reel, antistatic rails, quality and reliability data, and data sheets on each product.

Linear Technology intends to address customer demand for surface mount devices where technology and die sizes permit, making the combination of small package size and high performance linear devices readily available to our users.

This section contains information summarizing Linear Technology's capabilities and services for surface mount packaged products, as well as specific device data sheets.

Package Descriptions

Linear Technology's SO packages conform to Standard JEDEC SOIC outlines.

In some instances, an LTC product available in an 8-pin standard DIP package is offered in a 16-pin SOL package. This covers the situation where the die is too large to be accommodated by the smaller SO-8 package. Although it is preferable for an SO-8 device to have the same pinout as the standard 8-pin dual-in-line version, some devices necessitate a rotation of the die to fit in the SO-8 package. Please refer to the applicable SO device data sheet, or consult with the factory to verify exact pinouts for each device.

Electrical Specifications

Wherever possible, electrical specifications for a surface mount technology (SMT) device are the same as the plastic molded equivalent. Exceptions to this are identified by the omission of the standard product electrical grade designator from the part number.

For example:

- LT1013DS8 has the same electrical specifications as LT1013DN8, since the "D" is common to both product numbers.
- LT1012S8 has one or more different electrical specifications than LT1012CN8, as the "C" is missing from this product designator suffix.

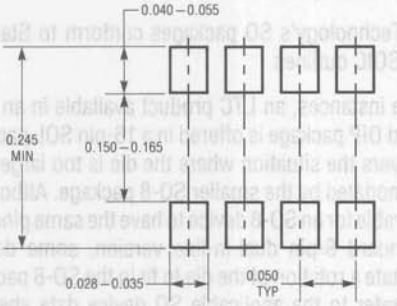
Please consult the appropriate SMT package data sheet for complete electrical specifications.

Marking

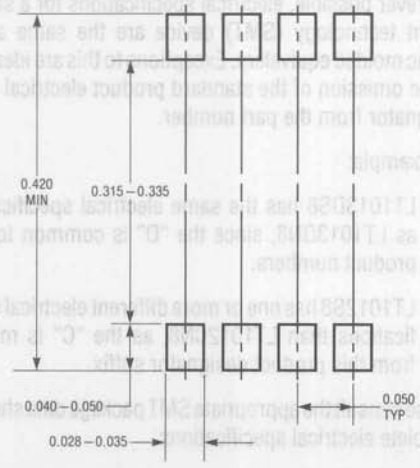
Because of the limited space available for part marking on some SMT packages, abbreviated marking codes are used to identify the device. These codes, if used, are identified in the individual SMT package data sheets.

Recommended Solder Pads

SO-8, SO-14, SO-16



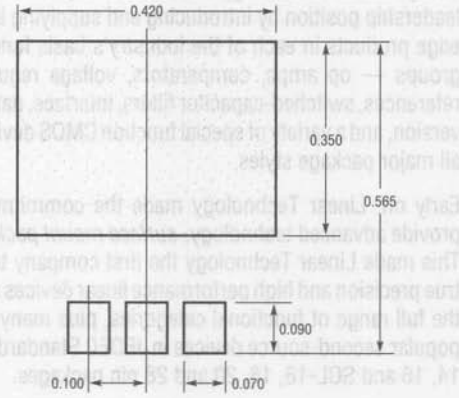
SOL-16, SOL-18, SOL-20, SOL-24, SOL-28



Lead Finish and Solderability

Lead finish is electroplated, lead-tin, with a low carbon content. Solderability meets the requirements of MIL-STD-883C, Method 2003. Recommended solder pads are given in Figure 1.

3-Lead DD



5-Lead DD

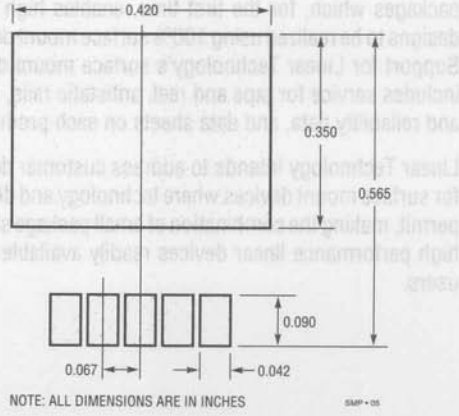
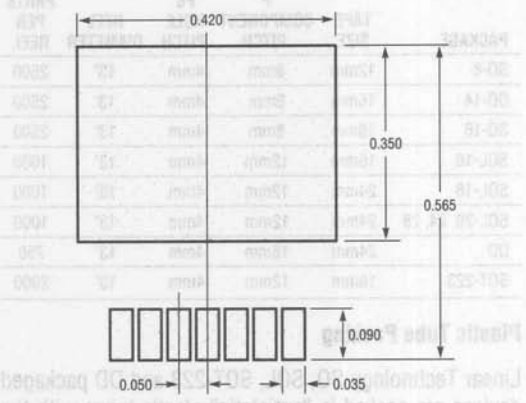


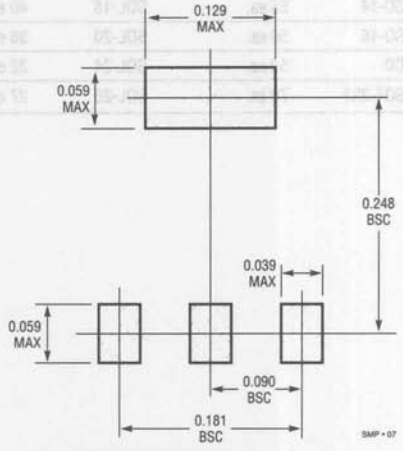
Figure 1. Recommended Solder Pads

7-Lead DD



NOTE: ALL DIMENSIONS ARE IN INCHES

3-Lead SOT-223



NOTE: ALL DIMENSIONS ARE IN INCHES

Figure 1. Recommended Solder Pads (Continued)

Wave and Reflow Soldering

Following are the recommended procedures for soldering surface mount packages to PC boards.

1. Wave Soldering

- Use solder plating boards.
- Dispense adhesive to hold components on board.
- Place components on board.
- Cure adhesive per adhesive manufacturer's specification.
- Foam flux using RMA (Rosin Mildly Activating) flux.
- Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
- Clean board.

2. Reflow Soldering

- Use solder plating boards.
- Screen solder paste on board.
- Mount components on board.
- Bake for 15-20 minutes at 65°C to 90°C.
- Preheat to within 65°C of the solder temperature.
- Reflow solder paste. The solder paste temperature must be 200°C for at least 30 seconds. LTC recommends vapor phase or infrared reflow systems for best performance.
- Clean boards.
- Hand soldering of DD and SOT-223 packages is not recommended.

Thermal Information

Table 1 shows the range of junction-to-ambient thermal resistance of SO and SOL devices mounted on a PCB of FR4 material with copper traces, in still air at 25°C. θ_{JA} with a ceramic substrate is about 70% of the FR4 value. Maximum power dissipation may be calculated by the following formula:

$$P_{D\,MAX}[TA] = \frac{T_{J\,MAX} - T_A}{\theta_{JA}}$$

where $T_{j\,MAX}$ = Maximum operating junction temperature.

T_A = Desired ambient operating temperature.

θ_{JA} = Junction-to-ambient thermal resistance.

Table 1. Typical Thermal Resistance Values

SO-8	150° to 200°C/W	SOL-18	70° to 100°C/W
SO-14	100° to 140°C/W	SOL-20	70° to 90°C/W
SO-16	90° to 130°C/W	SOL-24	60° to 80°C/W
SOL-16	85° to 100°C/W	SOL-28	55° to 75°C/W

Conditions: PCB mount on FR4 material, still air at 25°C, copper trace.

Thermal resistance for power packages (DD and SOT-223) depends greatly on the individual device type. Please consult the device data sheets for thermal information.

More current data, by device type, may be obtained by contacting Linear Technology Corporation, Marketing Department.

Tape and Reel Packing

Tape and reel packing is available for all SO, SOL, SOT-223 and DD packages in accordance with EIA Specification 481-A. Table 2 lists the applicable tape widths, dimensions, and quantities for all LTC small-outline products. Consult factory for tape and reel pricing and minimum order requirements.

Table 2. Tape and Reel Packing Specifications

PACKAGE	TAPE SIZE	P COMPONENT PITCH	Po HOLE PITCH	REEL DIAMETER	PARTS PER REEL
SO-8	12mm	8mm	4mm	13"	2500
SO-14	16mm	8mm	4mm	13"	2500
SO-16	16mm	8mm	4mm	13"	2500
SOL-16	16mm	12mm	4mm	13"	1000
SOL-18	24mm	12mm	4mm	13"	1000
SOL-20, 24, 28	24mm	12mm	4mm	13"	1000
DD	24mm	16mm	4mm	13"	750
SOT-223	16mm	12mm	4mm	13"	2000

Plastic Tube Packing

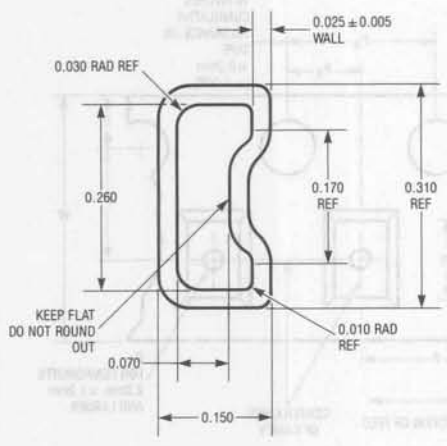
Linear Technology SO, SOL, SOT-223 and DD packaged devices are packed in "antistatic" plastic tubes with the dimensions indicated in Figure 2. Unit quantities per tube are as listed in Table 3.

Table 3. Devices Per Tube

SO-8	100 ea.	SOL-16	47 ea.
SO-14	55 ea.	SOL-18	40 ea.
SO-16	50 ea.	SOL-20	38 ea.
DD	50 ea.	SOL-24	32 ea.
SOT-223	78 ea.	SOL-28	27 ea.

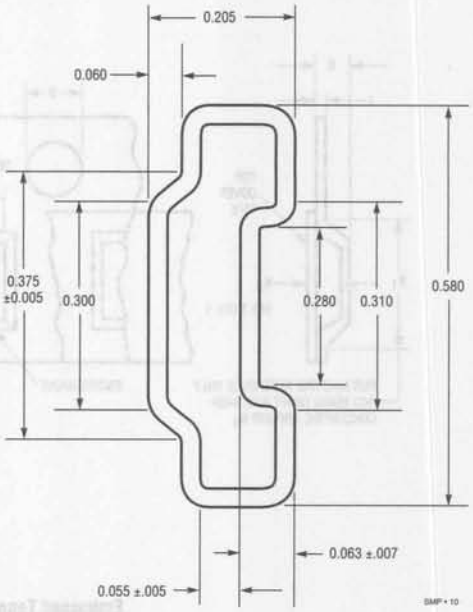
PLASTIC TUBE SPECIFICATIONS

SO Package Shipping Tube



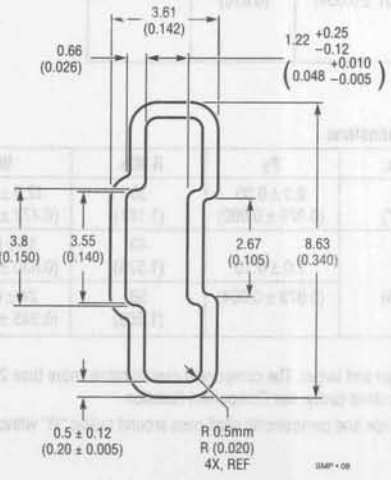
Length: 20.50 $^{+1/16}_{-1/32}$ inches

SOL Package Shipping Tube



Length: 20.75 $^{+1/32}_{-1/16}$ inches

SOT-223 Package Shipping Tube



Note 1: Tolerances: ± 0.010 unless otherwise specified.

Note 2: Material: anti-static treated rigid transparent PVC or rigid black conductive.

Note 3: Printing: "LTC logo, Linear Technology Corp., Antistatic" on top side of tube.

Figure 2

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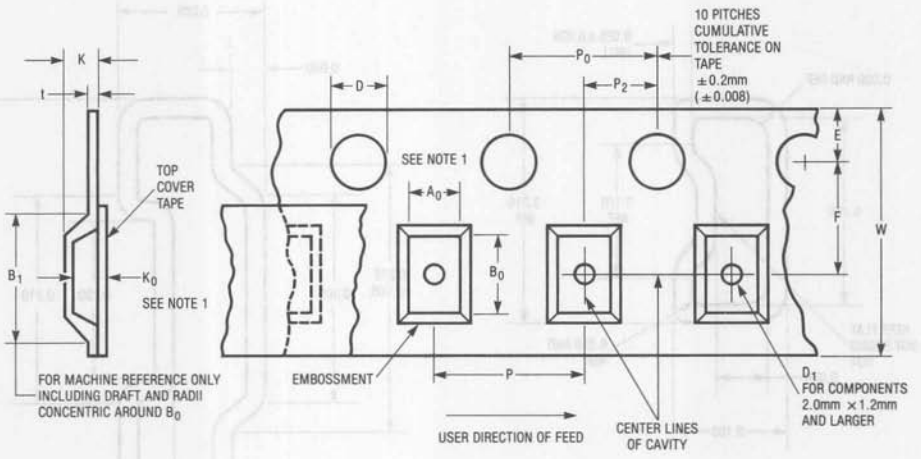
TAPE AND REEL SPECIFICATIONS

Embossed Carrier Dimensions (12mm, 16mm, 24mm Tape Only)



Embossed Tape — Constant Dimensions

Tape Size	D	E	P_0	t(Max.)	A_0 B_0 K_0
12mm, 16mm, 24mm	1.5 +0.10 −0.0 0.059 +0.004 −0.0	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	0.400 (0.016)	See Note1

Embossed Tape Variable Dimensions

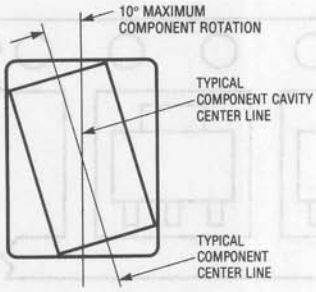
Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W
12mm	8.2 (0.323)	1.5 (0.059)	5.5 ± 0.05 (0.217 ± 0.002)	6.5 (0.177)	2.0 ± 0.05 (0.079 ± 0.002)	30 (1.181)	12.0 ± 0.30 (0.472 ± 0.012)
16mm	12.1 (0.476)		7.5 ± 0.10 (0.295 ± 0.004)	6.5 (0.256)	2.0 ± 0.10 (0.079 ± 0.004)	40 (1.575)	16 ± 0.30 (0.630 ± 0.012)
24mm	20.1 (0.791)		11.5 ± 0.10 (0.453 ± 0.004)			50 (1.969)	24 ± 0.30 (0.945 ± 0.012)

Note 1: A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape and 0.050 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation.

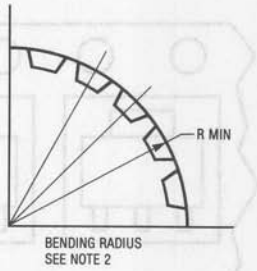
Note 2: Tape and components shall pass around radius "R" without damage.

TAPE AND REEL SPECIFICATIONS

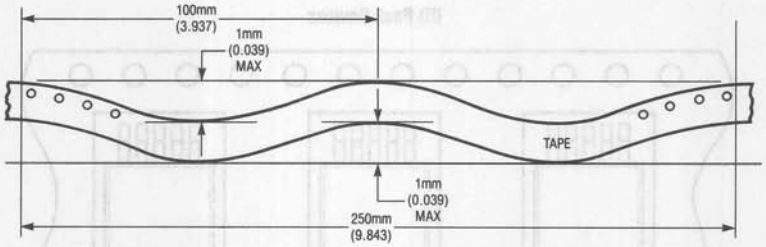
Component Rotation



Bending Radius

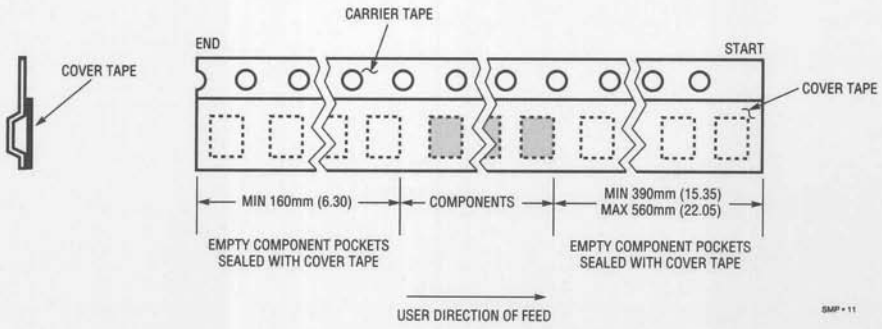


Tape Camber (Top View)



Allowable camber to be 1mm/100mm nonaccumulative over 250mm

Tape Leader (Start/End) Specification (SO Packages)



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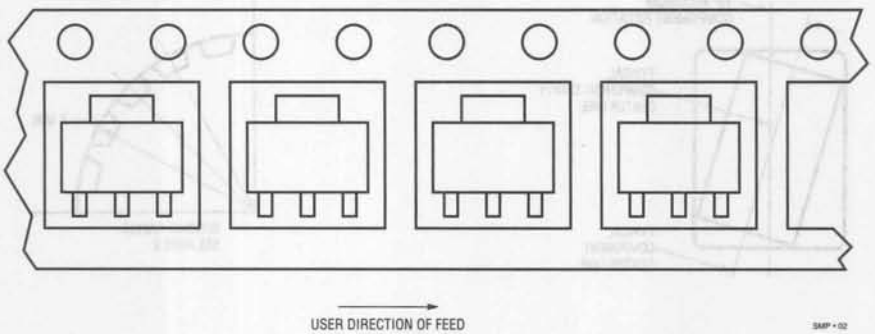
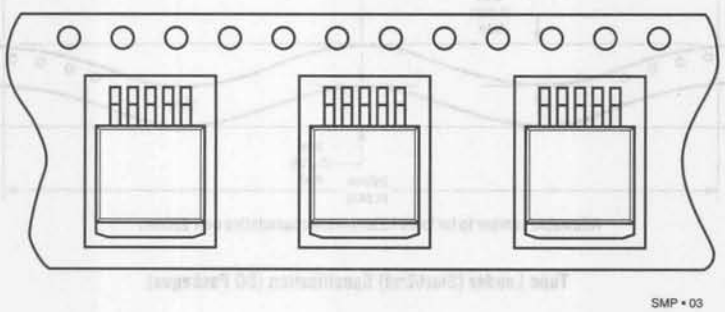
TAPE AND REEL SPECIFICATIONS

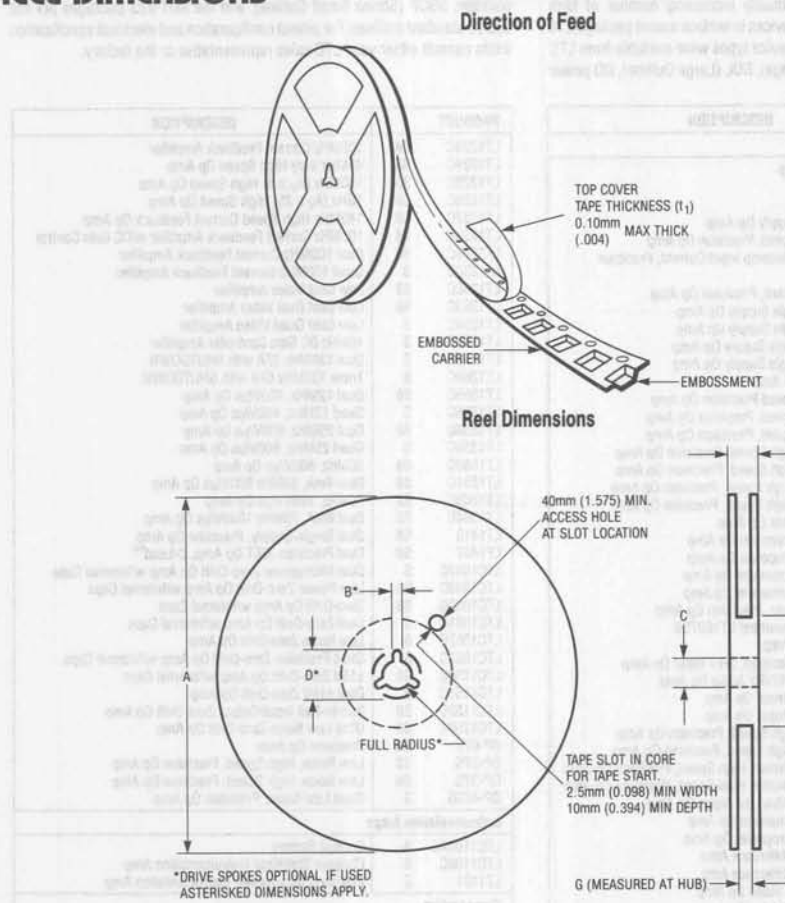
SOT-223 Devices



DD Pack Devices



REEL DIMENSIONS



Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
12mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$12.4\ ^{+2.0}_{-0.0}$ $\left(0.488\ ^{+0.078}_{-0.0}\right)$	18.4 (0.724)
16mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$16.4\ ^{+2.0}_{-0.00}$ $\left(0.646\ ^{+0.078}_{-0.00}\right)$	22.4 (0.882)
24mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$24.4\ ^{+2.0}_{-0.00}$ $\left(0.961\ ^{+0.078}_{-0.00}\right)$	30.4 (1.197)

*Metric dimensions will govern.
English measurements rounded and for reference only.

Surface Mount Small Outline (SO), DD and SOT Device Packaging

Linear Technology now offers a continually increasing number of high performance CMOS and bipolar linear devices in surface mount packages. At the time of this printing, the following device types were available from LTC packaged in the SO (Small Outline Package), SOL (Large Outline), DD power package, SSOP (Shrink Small Outline), and the SOT-223 packages per the JEDEC standard outlines. For pinout configuration and electrical specification limits consult either your LTC sales representative or the factory.

PRODUCT		DESCRIPTION
Operational Amplifiers		
LF398	S8	Sample & Hold Amp
LM318	S8	Fast Op Amp
LT1001C	S8	Precision Op Amp
LT1006	S8	Precision Single Supply Op Amp
LT1007C	S8	Low Noise, High Speed, Precision Op Amp
LT1008	S8	Uncompensated, Picoamp Input Current, Precision Op Amp
LT1012	S8	Picoamp Input Current, Precision Op Amp
LT1013D	S8	Dual Precision Single Supply Op Amp
LT1013I	S8	Dual Precision Single Supply Op Amp
LT1014D	S	Quad Precision Single Supply Op Amp
LT1014I	S	Quad Precision Single Supply Op Amp
LT1028C	S8	Ultra Low Noise Op Amp
LT1037C	S8	Low Noise, High Speed Precision Op Amp
LT1055	S8	JFET Input, High Speed, Precision Op Amp
LT1056	S8	JFET Input, High Speed, Precision Op Amp
LT1057	S8	Dual JFET Input, High Speed, Precision Op Amp
LT1057I	S8	Dual JFET Input, High Speed, Precision Op Amp
LT1058	S	Quad JFET Input, High Speed, Precision Op Amp
LT1058I	S	Quad JFET Input, High Speed, Precision Op Amp
LT1077	S8	Precision Micropower Op Amp
LT1078	S8	Dual Precision Micropower Op Amp
LT1078I	S8	Dual Precision Micropower Op Amp
LT1079	S	Quad Precision Micropower Op Amp
LT1079I	S	Quad Precision Micropower Op Amp
LT1097	S8	Low Cost, Low Power, Precision Op Amp
OP97F	S	Order Pin/Pin Replacement LT1097S8
LT1112	S8	Dual Precision Op Amp
LT1113C	S8	Dual Low Noise, Precision, JFET Input Op Amp
LT1115C	S	50MHz, 11V/µs, 1nV/√Hz Audio Op Amp
LT1122C	S8	Fast Settling, JFET Input Op Amp
LT1122D	S8	Fast Settling, JFET Input Op Amp
LT1124C	S8	Dual Low Noise, High Speed, Precision Op Amp
LT1125C	S	Quad Low Noise, High Speed, Precision Op Amp
LT1126C	S8	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1127C	S	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1128C	S8	Unity-Gain Stable Ultra Low Noise Op Amp
LT1178	S8	Dual Precision Micropower Op Amp
LT1179	S	Quad Precision Micropower Op Amp
LT1187C	S8	Low Power Video Difference Amp
LT1189C	S8	Low Power Video Difference Amp
LT1190C	S8	50MHz High Speed Video Op Amp
LT1191C	S8	90MHz High Speed Video Op Amp
LT1192C	S8	350MHz ($A_V \geq 25$)High Speed Video Op Amp
LT1193C	S8	80MHz (Adj Gain) High Speed Video Op Amp
LT1194C	S8	35MHz ($A_V = 10$) Fixed Differential Video Op Amp
LT1195C	S8	Low Power, High Speed Op Amp
LT1200C	S8	Low Power, High Speed Op Amp
LT1201C	S8	Dual Low Power, High Speed Op Amp
LT1202C	S	Quad Low Power, High Speed Op Amp
LT1206C	S8	250mA, 60MHz Current Feedback Amplifier
LT1206C	R	250mA, 60MHz Current Feedback Amplifier
LT1208C	S8	Dual Very High Speed Op Amp
LT1209C	S	Quad Very High Speed Op Amp
LT1211C	S8	14MHz Dual Precision Op Amp
LT1212C	S	14MHz Quad Precision Op Amp
LT1213C	S8	28MHz Dual Precision Op Amp
LT1214C	S	28MHz Quad Precision Op Amp
LT1215C	S8	23MHz Dual Precision Op Amp
LT1216C	S	23MHz Quad Precision Op Amp
LT1217C	S8	Low Power, 10MHz Current Feedback Amplifier
LT1220C	S8	Very High Speed Op Amp
LT1221C	S8	Very High Speed Op Amp ($A_V \geq 4$)
LT1222C	S8	Very High Speed Op Amp ($A_V \geq 10$,Ext Comp)
LT1223C	S8	100MHz Current Feedback Amplifier
LT1224C	S8	45MHz Very High Speed Op Amp
LT1225C	S8	150MHz ($A_V \geq 5$) High Speed Op Amp
LT1226C	S8	1GHz ($A_V \geq 25$) High Speed Op Amp
LT1227C	S8	140MHz High Speed Current Feedback Op Amp
LT1228C	S8	100MHz Current Feedback Amplifier w/DC Gain Control
LT1229C	S8	Dual 100MHz Current Feedback Amplifier
LT1230C	S	Quad 100MHz Current Feedback Amplifier
LT1252C	S8	Low Cost Video Amplifier
LT1253C	S8	Low Cost Dual Video Amplifier
LT1254C	S	Low Cost Quad Video Amplifier
LT1256C	S	40MHz DC Gain Controller Amplifier
LT1259C	S	Dual 130MHz CFA with SHUTDOWN
LT1260C	S	Triple 130MHz CFA with SHUTDOWN
LT1355C	S8	Dual 12MHz, 400V/µs Op Amp
LT1356C	S	Quad 12MHz, 400V/µs Op Amp
LT1358C	S8	Dual 25MHz, 600V/µs Op Amp
LT1359C	S	Quad 25MHz, 600V/µs Op Amp
LT1360C	S8	50MHz, 800V/µs Op Amp
LT1361C	S8	Dual 4mA, 50MHz 800V/µs Op Amp
LT1363C	S8	70MHz, 1000V/µs Op Amp
LT1364C	S8	Dual 6mA, 70MHz 1000V/µs Op Amp
LT1413	S8	Dual Single-Supply, Precision Op Amp
LT1457	S8	Dual Precision JFET Op Amp, C-Load™
LTC1047C	S	Dual Micropower Zero-Drift Op Amp w/Internal Caps
LTC1049C	S8	Low Power Zero-Drift Op Amp w/Internal Caps
LTC1050C	S8	Zero-Drift Op Amp w/Internal Caps
LTC1051C	S	Dual Zero-Drift Op Amp w/Internal Caps
LTC1052C	S	Low Noise Zero-Drift Op Amp
LTC1053C	S	Quad Precision Zero-Drift Op Amp w/Internal Caps
LTC1150C	S8	±15V Zero-Drift Op Amp w/Internal Caps
LTC1151C	S	Dual ±15V Zero-Drift Op Amp
LTC1152C	S8	Rail-to-Rail Input/Output Zero-Drift Op Amp
LTC1250C	S8	Ultra Low Noise Zero-Drift Op Amp
OP-07C	S8	Precision Op Amp
OP-27G	S8	Low Noise, High Speed, Precision Op Amp
OP-37G	S8	Low Noise, High Speed, Precision Op Amp
OP-470G	S	Quad Low Noise, Precision Op Amp
Instrumentation Amps		
LTC1100AC	S	Consult Factory
LTC1100C	S	Chopper Stabilized Instrumentation Amp
LT1101	S	Precision Micropower Instrumentation Amp
Comparators		
LT1011C	S8	Precision Volt Comparator
LT1016C	S8	High Speed Comparator
LT1016I	S8	High Speed Comparator
LT1017C	S	Micropower Dual Comparator
LT1017I	S8	Micropower Dual Comparator
LT1018C	S8	Micropower Dual Comparator
LTC1040C	S	Micropower Dual Sampling Comparator
LT1116C	S8	High Speed, Ground-Sensing Comparator
Data Acquisition		
LTC1090C	S	10-Bit A/D with 8 Ch MUX & S/H
LTC1093C	S	10-Bit A/D with 6 Ch MUX & S/H
LTC1096AC	S8	8-Bit Micropower A/D with S/H
LTC1096C	S8	8-Bit Micropower A/D with S/H
LTC1098AC	S8	8-Bit Micropower A/D with S/H
LTC1098C	S8	8-Bit Micropower A/D with S/H
LTC1099C	S	8-Bit High Speed ADC with S/H
LTC1196-1AC	S8	8-Bit, 600ns, 1MHz Sampling ADC
LTC1196-1BC	S8	8-Bit, 600ns, 1MHz Sampling ADC
LTC1196-2AC	S8	8-Bit, 710ns, 800kHz Sampling ADC
LTC1196-2BC	S8	8-Bit, 710ns, 800kHz Sampling ADC

C-Load is a trademark of Linear Technology Corporation

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT	DESCRIPTION
LTC1198-1AC S8	2-Channel, 8-Bit, 600ns, 750kHz, Sampling ADC
LTC1198-1BC S8	2-Channel, 8-Bit, 600ns, 750kHz, Sampling ADC
LTC1198-2AC S8	2-Channel, 8-Bit, 710ns, 750kHz, Sampling ADC
LTC1198-2BC S8	2-Channel, 8-Bit, 710ns, 750kHz, Sampling ADC
LTC1257C S8	12-Bit Complete V_{OUT} DAC
LTC1257I S8	12-Bit Complete V_{OUT} DAC
LTC1272-3AC S	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-3BC S	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-3CC S	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-5AC S	12-Bit 5µs Parallel I/O A/D with S/H
LTC1272-5BC S	12-Bit 5µs Parallel I/O A/D with S/H
LTC1272-5CC S	12-Bit 5µs Parallel I/O A/D with S/H
LTC1272-8AC S	12-Bit 8µs Parallel I/O A/D with S/H
LTC1272-8BC S	12-Bit 5µs Parallel I/O A/D with S/H
LTC1272-8CC S	12-Bit 8µs Parallel I/O A/D with S/H
LTC1273AC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1273BC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1275AC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1275BC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1276AC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1276BC S	12-Bit 3µs Parallel I/O with S/H & Ref.
LTC1278-4C S	12-Bit 2.5µs High Speed Sampling A/D
LTC1278-4I S	12-Bit 2.5µs High Speed Sampling A/D
LTC1282AC S	12-Bit 6µs Parallel I/O with S/H & Ref.
LTC1282BC S	12-Bit 6µs Parallel I/O with S/H & Ref.
LTC1285C S8	12-Bit 3V ADC
LTC1286C S8	12-Bit Micropower A/D with S/H
LTC1286I S8	12-Bit Micropower A/D with S/H
LTC1288C S8	12-Bit 3V ADC
LTC1289BC S	12-Bit 3V 8-Ch MUX, S/H Full Duplex I/O
LTC1289CC S	12-Bit 3V 8-Ch MUX, S/H Full Duplex I/O
LTC1290BC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1290BI S	12-Bit A/D with 8-Ch MUX & S/H
LTC1290CC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1290CI S	12-Bit A/D with 8-Ch MUX & S/H
LTC1290DC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1290DI S	12-Bit A/D with 8-Ch MUX & S/H
LTC1293BC S	12-Bit A/D with 6-Ch MUX & S/H
LTC1293CC S	12-Bit A/D with 6-Ch MUX & S/H
LTC1293DC S	12-Bit A/D with 6-Ch MUX & S/H
LTC1294BC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1294CC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1294DC S	12-Bit A/D with 8-Ch MUX & S/H
LTC1296BC S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1296BI S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1296CC S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1296CI S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1296DC S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1296DI S	12-Bit A/D with 8-Ch MUX & S/H, Single Supply
LTC1298C S8	12-Bit Micropower A/D with S/H
LTC1298I S8	12-Bit Micropower A/D with S/H
Regulators, PWMs, DC/DC Converters	
LT1020C S	µPower Low Dropout Regulator with Comparator
LT1020I S	µPower Low Dropout Regulator with Comparator
LT1072C S8	40kHz 1.25A Switching Regulator
LT1073C S8	µPower Switching Regulator Works Down to 1V Input,
S8-5, 12	Adjustable & Fixed 5V, 12V Outputs
LT1076C Q	2A Step-Down Switching Regulator
LT1076C Q-5	2A Step-Down Switching Regulator
LT1076C R	2A Step-Down Switching Regulator with Shutdown,
	5-Lead DD Pkg, Adjustable Output
LT1076C R-5	2A Step-Down Switching Regulator with Shutdown,
	7-Lead DD Pkg, 5V
LT1076HVC R	2A Step-Down Switching Regulator, 7-Lead DD Pkg
LT1085C M	Adjustable Low Dropout Pos Voltage Regulator, 3A
LT1085C M-3.3	3.3V Low Dropout Voltage Regulator, 3A
LT1085C M-3.6	3.6V Low Dropout Voltage Regulator, 3A
LT1086C M	1.5A Low Dropout Regulator, 3-Lead DD Pkg
LT1086C M-3.3	3.3V Low Dropout Pos Voltage Regulator, 1.5A
LT1086C M-3.6	3.6V Low Dropout Pos Voltage Regulator, 1.5A

PRODUCT	DESCRIPTION
LT1107C S8	µPower DC/DC Converter Works Down to 2V Input,
S8-5, 12	Adjustable & Fixed 5V, 12V Outputs
LT1108C S8	µPower DC/DC Converter Works Down to 2V Input,
S8-5, 12	Adjustable & Fixed 5V, 12V Outputs
LT1109AC S8	µPower DC/DC Converter with Shutdown & 100kHz
	Swtiching Frequency, Adjustable & Fixed 5V, 12V Outputs
LT1109AC S8-5	µPower Switching Regulator, 5V Output
LT1109AC S8-12	µPower Switching Regulator, 12V Output
LT1109C S8	µPower DC/DC Converter with Shutdown & 100kHz
S8-5, 12	Switching Frequency, Adjustable & Fixed 5V, 12V Outputs
LT1110C S8	µPower DC/DC Converter Works Down to 1V Input,
S8-5, 12	Adjustable & Fixed 5V, 12V Outputs
LT1111C S8	µPower Switching Regulator Works Down to 2V Input,
S8-5, 12	Adjustable & Fixed 5V, 12V Outputs
LT1111I S8	µPower Adjustable Switching Regulator
LT1117C M	Adjustable Low Dropout Regulator
LT1117C M-3.3	3.3V Low Dropout Regulator
LT1117C M-5	5V Low Dropout Regulator
LT1117C ST	Low Dropout 800mA Adjustable Regulator
LT1117C ST-5	Low Dropout 800mA Regulator, 5V
LT1117C ST-2.85	Active SCSI-2 Terminator, 2.85V
LT1117C ST-3.3	Low Dropout 800mA Fixed 3.3V Regulator
LT1120AC S8	µPower Voltage Regulator and Comparator with Shutdown
LT1120C S8	µPower Low Dropout Regulator with Shutdown
LT1121AC S8	µPower Low Dropout Regulator with Shutdown,
S8-3.3, 5	Adjustable & Fixed 3.3V, 5V Outputs
LT1121AI S8	Adjustable Low Dropout µP Regulator
LT1121AI S8-3.3	3.3V Low Dropout µPower Regulator
LT1121AI S8-5	5V Low Dropout µPower Regulator
LT1121C S8	µPower Low Dropout Regulator with Shutdown,
S8-3.3, 5	Adjustable & Fixed 3.3V, 5V Outputs
LT1121C ST-3.3, 5	µPower Low Dropout Regulator, Fixed 3.3V, 5V Output
LT1121I S8	Adjustable Low Dropout µPower Regulator
LT1121I S8-3.3	3.3V Low Dropout µPower Regulator
LT1121I S8-5	5V Low Dropout µPower Regulator
LT1121I ST-3.3	3.3V Low Dropout µPower Regulator
LT1121I ST-5	5V Low Dropout µPower Regulator
LT1123C ST	Low Dropout Regulator Driver
LT1129C Q	700mA µPower Low Dropout Voltage Regulator
LT1129C Q-3.3	700mA µPower Low Dropout Voltage Regulator
LT1129C Q-5	µPower Low Dropout Regulator, Fixed 5V Output
LT1129C S8	Adjustable 700mA µPower Low Dropout Regulator
LT1129C S8-3.3	3.3V 700mA µPower Low Dropout Regulator
LT1129C S8-5	5V 700mA µPower Low Dropout Regulator
LT1129C ST-3.3	700mA µPower Low Dropout Regulator
LT1129C ST-5	µPower Low Dropout Regulator, Fixed 5V Output
LT1129I Q	700mA µPower Low Dropout Voltage Regulator
LT1129I Q-3.3	700mA µPower Low Dropout Voltage Regulator
LT1129I Q-5	700mA µPower Low Dropout Voltage Regulator
LT1129I S8	Adjustable 700mA µPower Low Dropout Regulator
LT1129I S8-3.3	3.3V 700mA µPower Low Dropout Regulator
LT1129I S8-5	5V 700mA µPower Low Dropout Regulator
LT1129I ST-3.3	700mA µPower Low Dropout Regulator
LT1129I ST-5	700mA µPower Low Dropout Regulator
LT1170C Q	100kHz 5A Switching Regulator, 5-Lead DD Pkg
LT1171C Q	100kHz 2.5A Switching Regulator, 5-Lead DD Pkg
LT1172C S8	100kHz 1.25A Switching Regulator
LT1172C S8	1.25A High Efficiency 100kHz Switching Regulator
LT1172C Q	100kHz 1.25A Switching Regulator, 5-Lead DD Pkg
LT1172I S8	100kHz 1.25A Power Switching Regulator
LT1173C S8	µPower Switching Regulator for Inputs Greater than
S8-5, 12	Greater than 2V. Adjustable & Fixed 5V, 12V Versions
LT1176C S	100kHz 1A Step-Down Switching Regulator with Shutdown
LT1176C S-5	5V 1A Step-Down Switching Regulator
LT1241C S8	Current Mode PWM Controller
LT1241I S8	Current Mode PWM Controller
LT1242C S8	Current Mode PWM Controller
LT1242I S8	Current Mode PWM Controller
LT1243C S8	Current Mode PWM Controller
LT12431 S8	Current Mode PWM Controller
LT1244C S8	Current Mode PWM Controller

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
LT1244I	S8	Current Mode PWM Controller
LT1245C	S8	Current Mode PWM Controller
LT1245I	S8	Current Mode PWM Controller
LT1246C	S8	1MHz Current PWM Controller
LT1248C	S	Power Factor Correction Contoller
LT1248I	S	Power Factor Correction Contoller
LT1249C	S8	8-Pin Power Factor Correction Controller
LT1249I	S8	8-Pin Power Factor Correction Controller
LT1251C	S	40MHz Video Fader
LT1268BC	Q	7.5A, 150kHz Switching Regulator
LT1268C	Q	7.5A, 150kHz Switching Regulator
LT1269C	Q	4A, Power Switching Regulator, 5-Lead DD Pkg
LT1269C	S	100kHz 4A Switching Regulator, 20-Lead SOIC
LT1271C	Q	60kHz 4A Switching Regulator, 5-Lead DD Pkg
LT1300C	S8	µPower Step-Up DC/DC Converter, 1.8V Input
LT1301C	S8	µPower Step-Up DC/DC Converter, 1.8V Input
LT1301I	S8	5V/12V µPower DC/DC Boost Converter
LT1302C	S8	µPower High Current Step-Up DC/DC Converter
LT1303C	S8	5V/12V µPower DC/DC Boost Converter with LBD
LT1303C	S8-5	5V µPower DC/DC Boost Converter with LBD
LT1312C	S8	VPP Regulator
LT1313C	S	Dual VPP Regulator
LT1432C	S8	High Efficiency Switching Regulator Controller
LT1432C	S8-3.3	High Efficiency 3.3V Controller
LTC1142C	G	Dual High Efficiency Switching Regulator Controller
LTC1142HVC	G	HV Dual High Efficiency Switching Regulator Controller
LTC1142HVC	G-Adj	Adjustable HV Dual High Efficiency Sw. Reg. Controller
LTC1143C	S	Dual High Efficiency Switching Regulator Controller
LTC1144C	S8	20V Switched Capacitor Voltage Converter
LTC1144I	S8	20V Switched Capacitor Voltage Converter
LTC1147C	S8-3.3, 5	High Efficiency Step-Down Switching Regulator Controller
LTC1148C	S S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1148HVC	S S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1149C	S S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller, 48V Inputs
LTC1174C	S8 S8-3.3, 5	High Efficiency, 400mA Step-Down Switching Regulator
LTC1174HVC	S8	HV Adjustable µPower Step-Down DC/DC Converter
LTC1174HVC	S8-3.3	HV 3.3V µPower Step-Down DC/DC Converter
LTC1174HVC	S8-5	HV 5V µPower Step-Down DC/DC Converter
LTC1174I	S8	Adjustable µPower Step-Down DC/DC Converter
LTC1262C	S8	12V, 30mA VPP Generator
SG3524	S	Pulse Width Modulator
Switched-Capacitor Converters		
LT1054C	S	100mA Switched Capacitor Voltage Converter
LT1054C	S8	100mA Switched Capacitor Voltage Converter
LT1054I	S	100mA Switched Capacitor Voltage Converter
LTC1043C	S	Dual Precision Instrumentation Switched Capacitor Building Block
LTC1044AC	S8	Switched Capacitor Voltage Converter, 13V
LTC1044C	S8	Switched Capacitor Voltage Converter
LTC1044AI	S8	Switched Capacitor Voltage Converter, 13V
LTC1046C	S8	50mA Switched Capacitor Voltage Converter
LTC1046I	S8	50mA Switched Capacitor Voltage Converter
Switched-Capacitor Filters		
LTC1059C	S	2nd Order Universal Filter
LTC1060C	S	Dual 2nd Order Universal Filter
LTC1061C	S	Triple 2nd Order Universal Filter
LTC1062C	S	5th Order Lowpass Filter (Patented)
LTC1063C	S	Low Offset Clock-Tunable Lowpass Filter
LTC1064C	S	100kHz Quad 2nd Order Universal Filter
LTC1064-1C	S	8th Order Cauer Lowpass Filter
LTC1064-2C	S	8th Order Butterworth Lowpass Filter
LTC1064-3C	S	8th Order Bessel (Linear Phase) Lowpass Filter
LTC1064-4C	S	8th Order Cauer/Transitional Lowpass Filter
LTC1064-7C	S	100kHz Phase Corrected Lowpass Filter
LTC1064-XXC	S	High Speed, Low Noise Quad Semi-Custom Filter

PRODUCT		DESCRIPTION
LTC1065C	S	Low Offset Clock-Tunable Lowpass Filter
LTC1065I	S	Low Offset Clock Sweep. Bessel Filter
LTC1066-1C	S	14-Bit Accurate, 8th Order, LP Filter
LTC1164C	S	Low Power Quad 2nd Order Universal Filter
LTC1164AC	S	Quad 20kHz Low Power
LTC1164-5C	S	Low Power, 8th Order, Butterworth Filter
LTC1164-6C	S	Low Power, 8th Order, Cauer Filter
LTC1164-7C	S	Low Power, 8th Order, Linear Phase Filter
LTC1164-XXC	S	Low Power, Low Noise Quad Semi-Custom Filter
LTC1264C	S	High Speed, Quad 2nd Order Universal Filter
LTC1264-7C	S	High Speed, 8th Order, Linear Phase Filter
References		
LM334	S8	Constant Current Source & Temp. Sensor Reference
LM385	S8-1.2	1.2V Bandgap Voltage Reference
LM385	S8-2.5	2.5V Bandgap Voltage Reference
LM385B	S8-1.2	1.2V Bandgap Voltage Reference
LM385B	S8-2.5	2.5V Bandgap Voltage Reference
LT1004C	S8-1.2	1.2V Bandgap Voltage Reference
LT1004C	S8-2.5	2.5V Bandgap Voltage Reference
LT1004I	S8-1.2	1.2V Bandgap Voltage Reference
LT1004I	S8-2.5	2.5V Bandgap Voltage Reference
LT1009	S8	2.5V Reference
LT1009I	S8	2.5V Reference
LT1019C	S8-2.5	2.5V Buried Zener Precision Reference
LT1019C	S8-4.5	4.5V Buried Zener Precision Reference
LT1019C	S8-5	5V Buried Zener Precision Reference
LT1019C	S8-10	10V Buried Zener Precision Reference
LT1021DC	S8-5	5V Buried Zener Precision Reference
LT1021DC	S8-7	7V Buried Zener Precision Reference
LT1021DC	S8-10	10V Buried Zener Precision Reference
LT1027DC	S8-5	5V 5.0ppm Buried Zener Precision Reference
LT1027EC	S8-5	5V 7.5ppm Buried Zener Precision Reference
LT1034C	S8-1.2	Micropower Dual Reference: 1.2V, 7V
LT1034C	S8-2.5	Micropower Dual Reference: 2.5V, 7V
LT1034I	S8-2.5	2.5V Reference, 40ppm/°C Max TC
LT1431C	S8	Programmable Reference
LT1431I	S8	Programmable Reference
Interface Circuits		
LT1030C	S	Quad Low Power Line Driver
LT1032C	S	Quad Low Power Line Driver with Response Time Control
LT1039C	S	3 TX/3 RX RS232 XCVR with Shutdown
LT1039I	S	3 TX/3 RX RS232 XCVR with Shutdown
LT1039C	S16	3 TX/3 RX RS232 XCVR
LT1080C	S	Dual RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1080I	S	Dual RS232 XCVR with 5V to ±9V Pump
LT1081C	S	Dual RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1081I	S	Dual RS232 XCVR with 5V to ±9V Pump
LT1130AC	S	5 TX/5 RX RS232 XCVR with 5V to ±9V Pump
LT1130C	S	5 TX/5 RX RS232 XCVR with 5V to ±9V Pump
LT1131AC	S	5 TX/4 RX RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1132AC	S	5 TX/3 RX RS232 XCVR with 5V to ±9V Pump
LT1133AC	S	3 TX/5 RX RS232 XCVR with 5V to ±9V Pump
LT1134AC	S	4 TX/4 RX RS232 XCVR with 5V to ±9V Pump
LT1134AI	S	4 TX/4 RX 5V RS232 XCVR
LT1135AC	S	5 TX/3 RX RS232 XCVR
LT1136AC	S	4 TX/5 RX RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1137AC	G	3 TX/5 RX RS232 XCVR with 5V and Shutdown
LT1137AC	S	3 TX/5 RX RS232 XCVR with 5V to ±9V Pump & Shutdown & ±10kV ESD
LT1137AI	S	3 TX/5 RX RS232 XCVR with 5V and Shutdown
LT1138AC	S	5 TX/3 RX RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1139AC	S	4 TX/4 RX RS232 XCVR, 5V/12V Powered with Shutdown
LT1140AC	S	5 TX/3 RX RS232 XCVR with Shutdown
LT1141AC	S	3 TX/5 RX RS232 XCVR with Shutdown
LT1180AC	S	±10kV, 5V RS232 TX/RX with Shutdown, 0.1µF
LT1180AI	S	Dual RS232 XCVR with 5V to ±9V Pump & Shutdown

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
LT1181AC	S	Dual RS232 XCVR with 5V to ±9V Pump
LT1181AI	S	±10kV, 5V RS232 TX/RX, 0.1µF
LT1237C	G	5V RS232 Transceiver with 1 RX Active in Shutdown
LT1237C	S	3 TX/5 RX RS232 XCVR with 5V to ±9V Pump, Single RX Keep-Alive & Shutdown
LT1280AC	S	Dual RS232 XCVR with 5V to ±9V Pump & Shutdown
LT1281AC	S	Dual RS232 XCVR with 5V to ±9V Pump
LT1281I	S	Low Power Dual RS232 XCVR with 5V to ±9V Pump
LTC1318C	S	Single 5V AppleTalk® DCE XCVR
LTC1320C	S	AppleTalk XCVR
LTC1321C	S	Programmable EIA/TIA562/RS232 and RS485 XCVR
LTC1321I	S	Programmable EIA/TIA562/RS232 and RS485 XCVR
LTC1322C	S	Programmable EIA/TIA562/RS232 and RS485 XCVR
LTC1322I	S	Programmable EIA/TIA562/RS232 and RS485 XCVR
LTC1323C	S	Single 5V AppleTalk XCVR
LTC1327C	G	3V Low Power EIA562 3 TX/5 RX Transceiver
LTC1327C	S	3V Low Power EIA562 3 TX/5 RX Transceiver
LT1330C	G, S	5V RS232 XCVR with 3V Logic Interface and 1 RX Active in SHUTDOWN
LT1331C	S	3 TX/5 RX RS232 XCVR with 3V only Supply
LT1331C	G	3 TX/5 RX RS232 XCVR with 3V only Supply
LT1332C	S	3 TX/5 RX RS232 XCVR with Low Power
LT1332C	G	3 TX/5 RX RS232 XCVR with Low Power
LTC1335C	S	Programmable EIA/TIA562 and RS485 XCVR
LTC1335I	S	Programmable EIA/TIA562 and RS485 XCVR
LTC1337C	S	3 TX/5 RX RS232 XCVR with µPower
LTC1337C	G	3 TX/5 RX RS232 XCVR with µPower
LTC1337C	S	3 TX/5 RX RS232 XCVR with µPower
LTC1338C	G, S	5V Low Power RS232 5 DX/3 RX XCVR
LTC1338I	G, S	5V Low Power RS232 5 DX/3 RX XCVR
LT1341C	S	3 TX/5 RX RS232 XCVR with Shutdown and DX Disable
LT1341C	G	3 TX/5 RX RS232 XCVR with Shutdown and DX Disable
LT1342C	S	3 TX/5 RX RS232 XCVR with 3V & 5V Logic Supplies
LT1342C	G	3 TX/5 RX RS232 XCVR with 3V & 5V Logic Supplies
LTC1347C	G	5V Low Power RS232 3 DX/5 RX XCVR with 5 RX Active in SHUTDOWN
LTC1347C	S	5V Low Power RS232 3 DX/5 RX XCVR with 5 RX Active in SHUTDOWN
LTC1348C	S	3.3V Low Power RS232 3 DX/5 RX XCVR
LTC1349C	G, S	5V Low Power RS232 3 DX/5 RX XCVR with 2 RX Active in SHUTDOWN
LTC1349I	G, S	5V Low Power RS232 3 DX/5 RX XCVR with 2 RX Active in SHUTDOWN
LTC1350C	G, S	3.3V Low Power EIA/TIA562 3 RX/5 RX XCVR
LTC1350I	G, S	3.3V Low Power EIA/TIA562 3 RX/5 RX XCVR
LT1381C	S16	Dual RS232 XCVR with Narrow 16-Lead SOIC
LT1381I	S16	Dual RS232 XCVR with Narrow 16-Lead SOIC
LTC1382C	S	5V Low Power RS232 XCVR
LTC1383C	S	5V Low Power RS232 XCVR
LTC1384C	S	5V Low Power RS232 XCVR with 3 RX Active in SHUTDOWN
LTC1385C	S	3V Low Power EIA/TIA562 XCVR with 2 RX Active in SHUTDOWN
LTC1386C	S	RS232 2 TX/2 RX in Narrow SOIC
LTC1485I	S8	High Speed RS485 TX/RX
LTC485C	S8	Ultra Low Power RS485
LTC485I	S8	Interface
LTC486C	S	Ultra Low Power RS485 Interface Device
LTC486I	S	Ultra Low Power RS485 Interface Device
LTC487C	S	Ultra Low Power RS485 Interface Device
LTC487I	S	Ultra Low Power RS485 Interface Device
LTC488C	S	Ultra Low Power RS485 Quad Receiver
LTC488I	S	Ultra Low Power RS485 Quad Receiver
LTC489C	S	Ultra Low Power RS485 Quad Receiver
LTC489I	S	Ultra Low Power RS485 Quad Receiver
LTC490C	S8	Ultra Low Power RS485 Full-Duplex XCVR
LTC490I	S8	Ultra Low Power RS485 Full-Duplex XCVR
LTC491C	S	Ultra Low Power RS485 Full-Duplex XCVR
LTC491I	S	Ultra Low Power RS485 Full-Duplex XCVR
LTC1041C	S8	Bang-Bang Controller
LTC1485C	S8	10Mbit/s Low Power RS485 Half-Duplex XCVR
Analog Switches		
LTC201AC	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC202C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC203C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC221C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
LTC222C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
High-Side Switch Drivers		
LT1158C	S	Half-Bridge N-Channel Power MOSFET Driver
LTC1153C	S8	Electronic Circuit Breaker
LTC1154C	S8	Single High-Side MOSFET Switch Driver
LTC1155C	S8	Dual High-Side MOSFET Switch Driver
LTC1155I	S8	Dual High-Side MOSFET Switch Driver
LTC1156C	S	Quad High-Side MOSFET Switch Driver
LTC1157C	S8	Dual 3.3V Supply High-Side MOSFET Switch Driver
LT1158I	S	Half Bridge N-Channel Power MOSFET Driver
LT1161C	S	Quad High-Side MOSFET Driver
LT1161I	S	Quad High Voltage, High Side N-Channel MOSFET DRIVER
LTC1163C	S8	Triple 1.8V Supply High-Side MOSFET Switch
LTC1165C	S	Triple 1.8V Supply High-Side MOSFET Switch
LTC1255C	S8	Dual 24V High-Side Switch Driver
LTC1255I	S8	Dual 24V High-Side Switch Driver
Watchdog Timer/Microprocessor Supervisory		
LTC690C	S8	Microprocessor Supervisory Circuit
LTC690I	S8	Microprocessor Supervisory Circuit
LTC691C	S	Microprocessor Supervisory Circuit
LTC691I	S	Microprocessor Supervisory Circuit
LTC692C	S8	Microprocessor Supervisory Circuit
LTC693C	S	Microprocessor Supervisory Circuit
LTC694C	S8	Microprocessor Supervisory Circuit
LTC694C	S8-3.3	3.3V Microprocessor Supervisory Circuit
LTC694I	S8	Microprocessor Supervisory Circuit
LTC694I	S8-3.3	3.3V Microprocessor Supervisory Circuit
LTC695C	S	Microprocessor Supervisory Circuit
LTC695C	S-3.3	3.3V Microprocessor Supervisory Circuit
LTC695I	S	Microprocessor Supervisory Circuit
LTC695I	S-3.3	3.3V Microprocessor Supervisory Circuit
LTC699C	S8	Microprocessor Supervisory Circuit
LTC699I	S8	Microprocessor Supervisory Circuit
LTC1232C	S8	Microprocessor Supervisory Circuit
LTC1232I	S8	Microprocessor Supervisory Circuit
LTC1235C	S	Microprocessor Supervisory Circuit
Video Mulitplexers		
LT1203	S8	150MHz, 2:1 Video Multiplexer
LT1204	S	4-Input Video Multiplexer with 75MHz CFA
LT1205	S	Dual 150MHz, 2:1 or 4:1 Video Multiplexer

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INTRODUCTION

Linear Technology Corporation offers a wide variety of precision linear IC's in die form. It is our intent to offer dice electrically tested to levels which can be expected to yield the best possible performance in hybrid circuits. Complicating this task is the fact that many specifications given for our standard packaged products cannot be tested at the wafer level. Further, parameters which are 100% tested at wafer probe testing may shift during the die attach/assembly process.

There is a Dice Products Catalog available that contains ordering information and datasheets for obtaining dice products. Catalogs are available from your local LTC Sales Rep, or from LTC Communications at (800) 637-5545.

GENERAL INFORMATION

Electrical Testing

Dice are 100% tested in wafer form at 25°C to the DC limits shown on the dice data sheet for a given device type. Many LTC packaged products have multiple electrical grades associated with a basic die type. A cross reference appears on each dice data sheet indicating which die product grade should be ordered to optimize candidates to meet the specifications of the desired finished product grade. This information should be used as a guideline only since LTC does not guarantee electrical specifications after assembly. Since electrical testing is done only at 25°C, no absolute guarantee can be made regarding performance at other temperatures. Some LTC products require post-package trimming to overcome certain assembly related parameter shifts. Details on this trimming may be obtained by contacting the factory.

Visual Inspection

Dice are 100% visually inspected in accordance with MIL-STD-883, Method 2010 Condition B.

Chip Dimensions

Chip dimensions are as indicated on individual dice data sheets. Tolerance is ±1 mil. Chip thickness ranges from 12 mils to 20 mils, depending on product type. Bond pad dimensions are 4.5 x 4.5 mils. minimum.

Topside Passivation

Linear Technology products are passivated with a two layer system: A proprietary deposited oxide gives a crack-free conformal coverage of metal and oxide steps. A plasma nitride overcoat protects the die from ionic contamination and scratches during handling, testing and assembly. Note that LTC uses fuse link and zener zap trimming techniques which require windows in the passivation over the trim points. This passivation system is a major contributor to the extremely high reliability demonstrated throughout millions of device-hours of accelerated testing of LTC devices in plastic and hermetic packages.

Topside Metallization

The metallization is a minimum of 11,000 Å thick unless otherwise specified. The quality of the metallization step coverage is monitored via a weekly SEM inspection per MIL-STD-883, Method 2018.

Backside Metal

Contact LTC for details about availability of LTC products with a particular backside metallization.

Backside Potential

Linear Technology products are junction isolated. For proper operation the backside must be electrically connected to the most negative potential seen by the IC (for bipolar products) or the most positive potential (for CMOS products). This information is also given in the individual dice data sheets.

Packaging

Dice are packaged in compartmentalized waffle packs for ease of handling and storage. Each waffle pack contains 100 dice. Special packaging methods are also available by contacting the factory.

Quality Levels of Dice Shipped

Each dice lot is guaranteed to meet the following requirements:

- Internal visual per MIL-STD-883, Method 2010 Condition B: 1.0% AQL Level II.
- Electrical: Due to variations in assembly methods and packaging techniques LTC does not guarantee electrical specifications after assembly. When a determination as to the finished product assembly yield is needed, the lot acceptance testing available at extra cost should be pursued.

Reliability Assurance

In addition to the more conventional reliability audits performed on finished products, LTC has innovated a unique periodic wafer fab reliability audit using a specially designed reliability structure that is stepped into all wafers. The test structure is optimized to accelerate the two primary failure mechanisms in linear circuits, namely mobile positive ions and surface charge-induced inversions. This provides a continuous monitor on the reliability performance of LTC's wafer fab processes and provides immediate feedback to wafer fab typically within one week.

Electrostatic Discharge (ESD) Precautions

Precision linear devices, especially those with very low (pA) input bias current levels and low (<50 microvolts) input offset voltages are susceptible to shifts in electrical performance and ESD damage as a result of improper handling. LTC recommends that ESD precautions, such as grounded conductive work stations, grounded conductive wrist straps and grounded equipment, be taken to prevent ESD damage.

ORDERING INFORMATION

Dice may be ordered by the part number defined in the dice data sheet. Minimum direct dice order, per delivery, is 1000 pieces or $5,000, whichever is greater. In some cases, tighter parameter selections than indicated on the dice data sheets can be obtained by special order. Please contact the factory for details.

Lot Acceptance Testing

Lot acceptance testing (L.A.T.) based on sample assembly and testing is available at extra cost. Sample sizes and acceptable electrical test limits vary from device to device and must be negotiated at the time of quoting. Contact the factory for details.

Application Notes

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**
This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**
This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**
This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F/V and V/F converters, 12-bit A/D converter and more.

AN4 **Application for a New Power Buffer**
The LT1010 150mA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wide-band DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**
6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, and anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**
Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**
Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**
A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**
A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN10 **Methods for Measuring Op Amp Settling Time**
The AN10 begins with a survey of methods for measuring op amp settling time. This commentary develops into circuits for measuring settling time to 0.0005%. Construction details and results are presented. Appended sections cover oscilloscope overload limitations and amplifier frequency compensation.

AN11 **Designing Linear Circuits for 5V Operation**
This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**
Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**
The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz to 30MHz V/F converter, a 200ns 0.01% sample-hold and a 10MHz fiber-optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-to-Frequency Converters**
A variety of high performance V/F circuits is presented. Included are a 1Hz to 100MHz design, a quartz-stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output an nonlinear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V/F conversion.

AN15 **Circuitry for Single Cell Operation**
1.5V powered circuits for complex linear functions are detailed. Designs include a V/F converter, a 10-bit A/D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section of component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**
This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Consideration for Successive Approximation A/D Converters**
A tutorial on SAR type A/D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and preamplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8μs. Appended sections explain the basic SAR technique and explore D/A considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**
This note presents output state circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**
This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk." The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Lowpass Switched-Capacitor Filter**
Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062s and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**
Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS/DC Conversion**
AN22 details the theoretical and application aspects of the LT1088 thermal RMS/DC converter. The basic theory behind thermal RMS/DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS/DC converters, wide-band input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**
Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**
Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**
Subtitled "A Gentle Guide for the Trepidatious," this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26 A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
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AN26J	LTC1091	TMS7742
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AN26L	LTC1091	HD63705VO
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A **A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections**
Presents two methods of designing high quality switched-capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumed no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched-Capacitor filter family: LTC1060, LTC1061, and LTC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 **Thermocouple Measurement**
Considerations for thermocouple-based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor-based linearization is also presented with the necessary software detailed.

AN29 **Some Thoughts on DC/DC Converters**
This note examines a wide range of DC/DC converter applications. Single inductor, transformer, and switched-capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 **Switching Regulator Circuit Collection**
Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 **Linear Circuits for Digital Systems**
Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. V_{PP} generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 **High Efficiency Linear Regulators**
Presents circuit techniques permitting high efficiency to be ob-

tained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 **Converting Light to Digits: LTC1099 Half-Flash 8-Bit A/D Converter Digitizes Photodiode Array**
This application note describes a Linear Technology "Half-Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand-held (i.e., low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 **LTC1099 Enables PC-Based Data Acquisition Board to Operate DC-20kHz**
A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speed of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on a 4.77MHz clock speed.

AN35 **Step-Down Switching Regulators**
Discusses the LT1074, an easily applied step-down regulator IC. Basic concepts and circuits are described along with more sophisticated applications. Six appended sections cover LT1074 circuitry detail, inductor and discrete component selection, current measuring techniques, efficiency considerations and other topics.

AN36 A collection of interface applications between various microprocessors/controllers and the LTC1290 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN36A	LTC1290	8051
AN36B	LTC1290	MC68HC05
AN36C	LTC1290/LTC1090	TMS370
AN36D	LTC1290	COP820C
AN36E	LTC1290	TMS7742
AN36F	LTC1290	COP402N
AN36O	LTC1290	Z-80
AN36P	LTC1290	HD64180

These interface notes demonstrate the ease with which the LTC1290 can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN37 **Fast Charge Circuits for NiCad Batteries**
Safe, fast charging of NiCad batteries is attractive in many applications. This note details simple, thermally-based fast charge circuitry for NiCads. Performance data is summarized and compared to other charging methods.

AN38 **FilterCAD User's Manual, Version 1.00**
This note is the manual for FCAD, a computer-aided design program for designing filters with LTC's switched-capacitor filter family. FCAD helps users design good filters with a minimum amount of effort. The experienced filter designer can use the program to achieve better results by providing the ability to play "what if" with the values and configuration of various components.

AN39 **Parasitic Capacitance Effects in Step-Up Transformer Design**
This note explores the causes of the large resonating current spikes on the leading edge of the switch current waveform. These anomalies are exacerbated in very high voltage designs.

AN40 **Take the Mystery Out of the Switched-Capacitor Filter: The System Designer's Filter Compendium**
This note presents guidelines for circuits utilizing LTC's switched-capacitor filters. The discussion focuses on how to optimize filter performance by optimizing the printed wiring board, the power supply, and the output buffering of the filter. Many additional topics are discussed such as how to select the proper filter response for the application and how to characterize a filter's THD for DSP applications.

AN41 **Questions and Answers on the SPICE Macromodel Library**
This note provides answers to some of the more common questions concerning LTC's Macromodel Library. Topics include hardware and software requirements, model characteristics, and limitations and interpretation of results.

AN42 **Voltage Reference Circuit Collection**
A wide variety of voltage reference circuits are detailed in this extensive guidebook of circuits. The detailed schematics cover simple and precision approaches at a variety of power levels. Included are 2 and 3 terminal devices in series and shunt modes for positive and negative polarities. Appended sections cover resistor and capacitor selection and trimming techniques.

AN43 **Bridge Circuits**
Subtitled "Marrying Gain and Balance," this note covers signal conditioning circuits for various types of bridges. Included are transducer bridges, AC bridges, Wien bridge oscillators, Schottky bridges, and others. Special attention is given to amplifier selection criteria. Appended sections cover strain gauge transducers, understanding distortion measurements, and historical perspectives on bridge readout mechanisms and Wein bridge oscillators.

AN44 **LT1074/LT1076 Design Manual**
This note discusses the use of the LT1074 and LT1076 high efficiency switching regulators. These regulators are specifically designed for ease of use. This application note is intended to eliminate the most common errors that customers make when using switching regulators as well as offering insight into the inner workings of switching designs. There is an entirely new treatment of inductor design based upon simple mathematical formulas that yield direct results. There are extensive tutorial sections devoted to the care and feeding of the Positive Step-Down (Buck) Converter, the Tapped Inductor Buck Converter, the Positive-to-Negative Converter and the Negative Boost Converter. Additionally, many trouble-shooting hints are included as well as oscilloscope techniques, soft-start architectures, and micropower shutdown and EMI suppression methods.

AN45 **Measurement and Control Circuit Collection**
A variety of measurement and control circuits are included in this application note. Eighteen circuits, including ultra low noise amplifiers, current sources, transducer signal conditioners, oscillators, data converters and power supplies are presented. The circuits emphasize precision specifications with relatively simple configurations.

AN46 **Efficiency Characteristics of Switching Regulator Circuits**
Efficiency varies for different DC/DC converters. This application note compares the efficiency characteristics of some of the more popular types. Step-up, step-down, flyback, negative-to- positive, and positive-to-negative are shown. Appended sections discuss how to select the proper aluminum electrolytic capacitor and explain power switch and output diode loss calculations.

AN47 **High Speed Amplifier Techniques**
This application note, subtitled "A Designer's Companion for Wideband Circuitry," is intended as a reference source for designing with fast amplifiers. Approximately 150 pages and 300 figures cover frequently encountered problems and their possible causes. Circuits include a wide range of amplifiers, filters, oscillators, data converters and signal conditioners. Eleven appended sections discuss related topics including oscilloscopes, probe selection, measurement and equipment considerations, and breadboarding techniques.

AN48 **Using the LTC Op Amp Macromodels**
LTC's op amp macromodels are described in detail, along with the theory behind each model and complete schematics of each topology. Extended modeling topics are discussed, such as phase/frequency response modifications and asymmetric slew rate for JFET op amp models. LTC's macromodels are optimized for accuracy and fast simulation times. Simulation times can be further reduced by using streamlining techniques found throughout AN48.

AN49 **Illumination Circuitry for Liquid Crystal Displays**
Current generation portable computers and instruments utilize back-lit liquid crystal displays. The back light requires a highly efficient, high voltage AC source as well as other supply circuitry. AN49 details these circuits and also includes sections on efficiency measurements and instrumentation considerations. A separate section discusses physical and layout considerations for the display.

AN50 **Interfacing to Microprocessor Based 5V Systems**
This application note discusses a variety of approaches for interfacing analog signals to 5V powered systems. Synthesizing a "rail-to-rail" op amp and scaling techniques for A/D converters are covered. A voltage-to-frequency converter, applicable where high resolution is required, is also presented.

AN51 **Power Conditioning for Notebook and Palmtop Systems**
Notebook and palmtop systems need a number of voltages developed from a battery. Competitive solutions require small size, high efficiency and light weight. This publication includes circuits for high efficiency 5V and 3.3V switching and linear regulators, back light display drivers and battery chargers. All the circuits are specifically tailored for the requirements outlined above.

AN52 **Linear Technology Magazine Circuit Collection, Vol 1**
This application note consolidates the circuits from the first few years of Linear Technology Magazine into one publication. Presented in the note are a variety of circuits ranging from a 50W high efficiency (>90%) switching regulator to steep roll-off filter circuits with low distortion to 12-bit differential temperature measurement systems.

AN53 **Micropower High-Side MOSFET Drivers**
This application note describes the operation of high-side N-channel MOSFET switch drivers designed specifically for operation in battery-powered equipment, such as notebook and palmtop computers and portable medical instruments. A selection guide simplifies the proper choice of MOSFET and driver for a particular high-side switch application. Circuits to drive and protect load impedances ranging from large inductors to large capacitors are described and a section on surface mount and copper clad shunts is included.

AN54 **Power Conversion from Milliamps to Amps at Ultra High Efficiency (Up to 95%)**
This application note discusses the use of the LTC1147, LTC1148, and LTC1149 ultra high efficiency switching regulators in a wide variety of applications. These controllers feature a current-mode architecture which includes an automatic low current operating mode called Burst Mode™ operation, making greater than 90% efficiencies possible at output currents as low as 10mA. This feature maximizes battery life while a product is in sleep or standby modes. In addition, the LTC1148 and LTC1149 are synchronous switching regulators which achieve high efficiency conversion from 10mA to 10A.

AN55 **Techniques for 92% Efficient LCD Illuminatio**
This publication details several LCD backlight circuits which feature 92% efficiency. Other benefits include low voltage operation, synchronizing capability, higher output power for color displays, and extended dimming range. Extensive coverage of practical issues includes lay out problems, multi-lamp displays, safety and reliability concerns and efficiency and photometric measurements. Also included is a review of circuits which did not work along with appropriate commentary.

AN56 **"Better Than Bessel" Linear Phase Filters for Data Communications**
The pace of the world of digital communications is increasing at a tremendous rate. Each day the engineer is requested to compact more data in the same channel bandwidth with closer channel spacing. This application note discusses some of the requirements and techniques for using the new LTC1064/1164 and LTC1264-7 filters which were designed specifically for digital communications. The terms "channel bandwidth," "eye diagrams" and "linear phase" filtering are discussed without the need for the "engineering speak" which permeates many textbook explanations of the same subjects.

AN57 **Video Circuit Collection**
AN57, the Video Circuit Collection, features a variety of video circuits designed at LTC. The LT1204 70MHz multiplexer is featured in a number of circuits which require excellent video isolation from channel to channel. High speed voltage and current feedback amplifiers are highlighted throughout the section on video processing circuits. There is a section on applying Current Feedback Amplifiers (CFAs) and a number of articles taken from the Linear Technology Magazine.

AN58 **5V to 3.3V Converters for Microprocessor Systems**
Many popular microprocessors operate from 3.3V supplies, yet they are used in systems where the predominate source of power is 5V. AN58 presents a collection of both linear and switching regulator solutions for conversion of 5V to 3.3V at currents ranging from 100mA to 20A. Applications information and a comparison of various bypass capacitor types is included. Most of the designs can be easily modified for other intermediate voltages such as 3.45V, 3.7V, and 4.1V.

AN59 **Applications of the LT1300 and LT1301 Micropower DC/DC Converters**
This note covers operation and applications of the LT1300 and LT1301 high efficiency micropower step-up DC/DC converter ICs. Internal operation of the ICs is described in detail. A variety of applications are presented, ranging from straightforward 2-cell to 5V converters and 5V to 12V converters to exotic transducer-based circuits such as flame detectors and CCFL drivers. Converters from both 2-cell and 4-cell inputs are included. Operating hours at various load currents are presented and relative merits of different battery types are discussed.

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Applications on Disk

NOISE DISK
This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim.

FILTERCAD DISK
FilterCAD is a menu-driven filter design aid program which runs on IBM-PCs (or compatibles). This collection of design tools will assist in the selection, design, and implementation of the right switched capacitor filter circuit for the application at hand. Standard classical filter responses (Butterworth, Cauer, Chebyshev, etc.) are available, along with a CUSTOM mode for more esoteric filter responses. SAVE and LOAD utilities are used to allow quick performance comparisons of competing design solutions. GRAPH mode, with a ZOOM function, shows overall or fine detail filter response. Optimization routines adapt filter designs for best noise performance or lowest distortion. A design time clock even helps keep track of on-line hours.

SWITCHERCAD DISK
SwitcherCAD is a powerful design tool that significantly eases the task of selecting topologies, calculating operating points, and specifying component values and part numbers for DC/DC converters. It can cut days off of the design cycle by eliminating the process of wading through multiple data sheets, application notes, and magazine "cookbook" articles searching for answers in a field where the user may have little familiarity. SwitcherCad runs on IBM-PCs and compatibles. Please see the next page for ordering information.

Technical Publications

$10.00

1990 Linear Databook — This 1,440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

$10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. $10.00

$20.00

1990 Linear Applications Handbook Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

$20.00

1993 Linear Applications Handbook Volume II — Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00

$40.00

Monolithic Filter Handbook — This 234 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes. $40.00

$20.00

SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD – a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. $20.00

Interface Product Handbook — This 312 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages.

AppleTalk is a registered trademark of Apple Computer, Inc.

Power Solutions Brochure — A 52 page collection of circuits containing real-life solutions for common power supply design problems. There are over 45 circuits, including descriptions, graphs and performance specifications. Topics covered include micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators, switched capacitor conversion and power management.

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