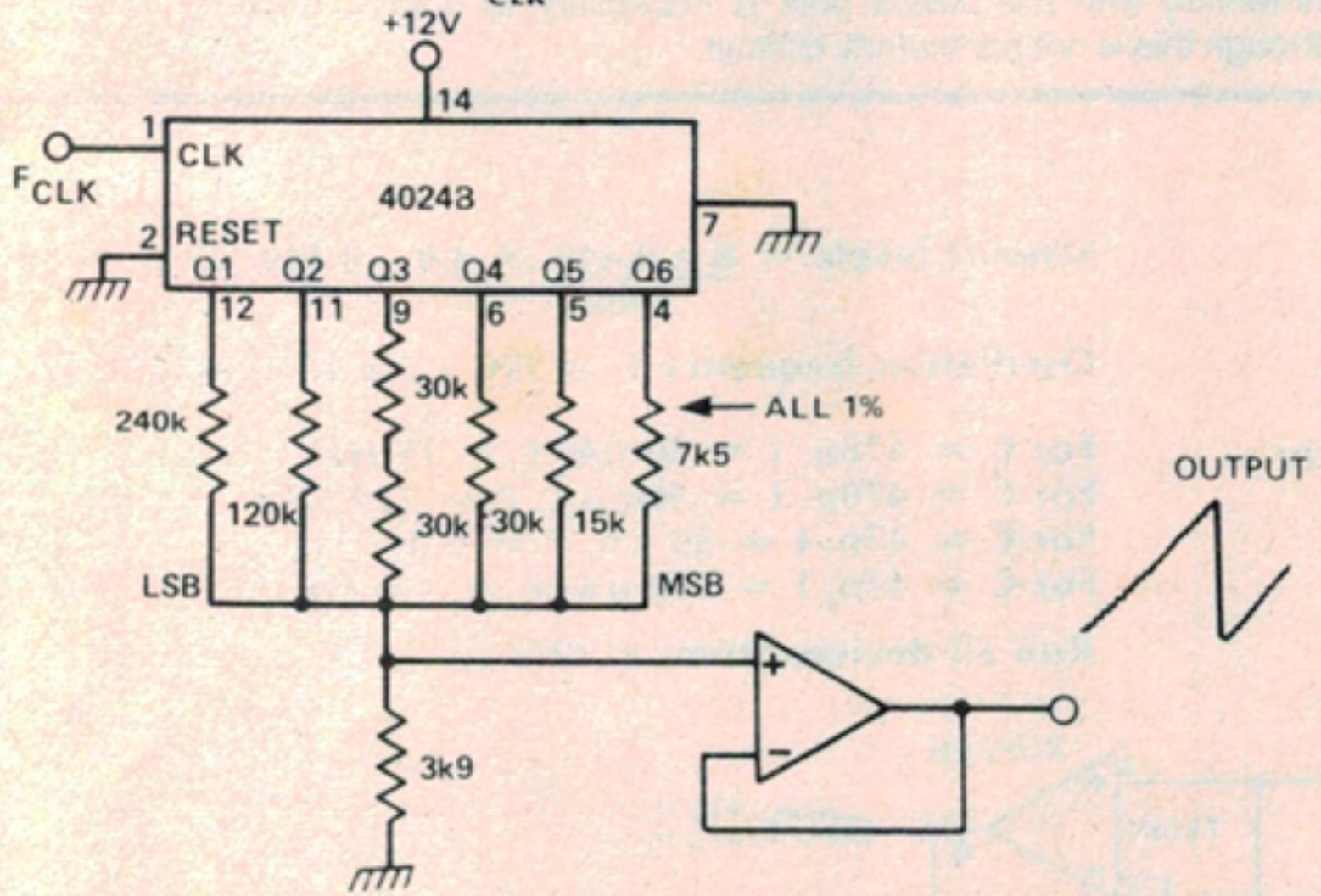
Staircase Generator

Output frequency $F = F_{CLK}/64$ Staircase is made up of 64 steps



The 4024B is a CMOS seven-stage binary ripple counter. Upon receipt of a clock pulse the counter selects a combination of the resistors and increases the voltage at the output of the op-amp buffer. As with all edge-triggered devices the clock should be conditioned to have a single clean edge with a rise and fall time faster than 5 uS. The device clocks on the falling edge of the clock waveform.