Dual flip-flop forms simple delayed-pulse generator

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Some applications require clock-timing adjustments, such as generating precision clocks for time-interleaved ADCs, or delay adjustments in a variety of precision-timing and pulse-delay applications. This Design Idea describes a delayed-pulse generator using a dual-CMOS D-type flip-flop (**Figure 1**). The circuit provides precision time delays of a trigger-input pulse. A dc-control voltage selects a time delay within the full-scale range. When the rising edge of a pulse triggers the input, the circuit's output generates a pulse with its rising edge delayed by an amount equal to the selected time delay, T_D, plus a fixed inherent propagation delay T_{PD}. Also, a time constant, R_4C_2, determines the output pulse's width.

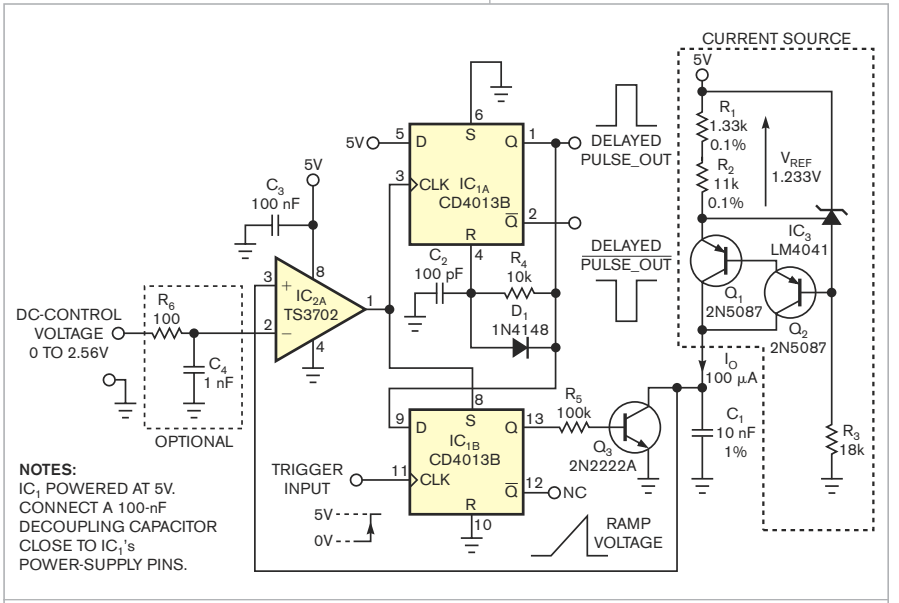

Figure 1 The rising edge of a trigger input starts a precision ramp voltage that compares with a control voltage, generating a precise delay.

A precision dc source, I_O, and capacitor C_1 set the full-scale delay range. When Q_3 is off, the current source charges capacitor C_1, generating a linear-ramp voltage with slope equal to I_O/C_1. The delay is the time it takes for the ramp to rise from its initial voltage to the control-voltage value.

In this application, the ramp slope is 10 mV/1 µsec, so that the full-scale delay range is 256 µsec for a control voltage of 0 to 2.56V. You can set the full-scale delay by changing I_O through either R_1+R_2 or capacitor C_1. For best accuracy, the current source can range from 10 µA to 1 mA, the capacitor's value can range from 1 nF to 1 µF, and the corresponding full-scale delay can range from 2.56 µsec to 256 msec. Use a precision film capacitor for C_1.

The basis of the current source is a shunt precision-micropower-voltage-reference, IC_3, producing a reference voltage of 1.233V with an initial ac-

curacy of 0.2%. A Texas Instruments (www.ti.com) LM4041, through precision resistors R_1 and R_2, biases the Darlington-coupled transistors Q_1 and Q_2 with a reference current $I_O=V_{REF}/(R_1+R_2)=100\ \mu A$. The Darlington configuration ensures that base current is negligible and that the output collector current can achieve a worst-case accuracy of 0.3%. You can use any small-signal transistor, but, for best accuracy, use high-gain, low-level, low-noise BJTs, (bipolar-junction transistors) such as a 2N5087 or a BC557C.

IC_{1A} is a one-shot circuit (**Reference 1**). The output pulse's width, T_W, is $R_4C_2\times\ln(V_{DD}/V_{TH})$, where V_{TH} is the threshold voltage of the digital CMOS. Because $V_{TH}\approx V_{DD}/2$, then $T_W\approx R_4C_2\times 0.69$. Diode D_1 reduces recovery time. After power-up, Q_3 is in saturation, absorbing the current source's output, and, as soon as an input pulse triggers the circuit, IC_{1B}'s Q output goes low, switching off Q_3, starting a ramp. When the ramp exceeds the control voltage, then the IC_{2A} comparator's output goes high, and the rising edge triggers one-shot IC_{1A} and switches on Q_3 through IC_{1B}, allowing the discharge of the capacitor C_1. When an input pulse triggers the circuit, any other trigger pulse that occurs before the falling edge of the delayed output pulse does not produce an output pulse; in other words, the circuit is not retriggerable. This feature permits you, at the same time, to divide and delay an input-trigger clock.

Although IC_1 and IC_2 can operate from a 3 to 16V supply, the minimum supply voltage of the circuit is 5V; otherwise, Q_1 and Q_2 approach saturation, generating to a less linear ramp voltage. Voltage comparator IC_{2A}, an STMicroelectronics (www.st.com) TS3702, has an input-common-mode-voltage range that includes ground, permitting you to monitor input voltages as low as 0V.

However, for correct operation of the circuit, the minimum control voltage must be greater than the saturation voltage of Q_3. For the components in **Figure 1**, the measured value is 12 mV. If you want to reduce this voltage, you can use a digital N-channel MOSFET with low on-resistance. The optional input lowpass filter, comprising R_6 and C_4, helps to clean noise from the dc-control voltage.

If a DAC drives the control input, you can build a digitally programmable delay generator. A suitable low-cost, 8-bit DAC is the AD558 from Analog Devices (www.analog.com), which features an internal precision bandgap reference to provide an output voltage of 0 to 2.56V, making 1 LSB equal to 1 μsec. It operates from 5 to 16V, with a 1-μsec settling time. The circuit's quiescent current, I_{DD}, is less than 300 μA because all ICs are micropower. EDN

REFERENCE

1 Bhandarkar, Santosh, "Single-IC-based electronic circuit replaces mechanical switch" *EDN*, March 15, 2007, pg 76, www.edn.com/article/CA6421439.