Lab Notes

A look at the versatile 4046B

The 4046B CMOS chip is probably one of the most versatile and least-used of all the ICs in the CMOS range. The device glories in (or suffers from) the descriptive title of 'micropower phase-locked loop' and there is a widespread misconception amongst many electronics amateurs and professionals that the device can only be used in PLL-type applications. In fact nothing could be further from the truth.

Ray Marston

THE 4046B CONTAINS a pair of phase-comparators, a zener diode and one VCO or voltage-controlled oscillator. All of these sections are independently accessible via the IC pin-outs. The VCO section of the device is probably the most versatile and cost-effective voltage-controlled oscillator on the market. It produces a well-shaped symmetrical square wave output, has a top-end frequency limit in excess of 1 MHz, can be voltage-scanned through a 1 000 000:1 range (1 Hz to 1 MHz) when used with a single timing resistor or through any range from 1:1 to infinity (0 Hz to 1 MHz) when used with a pair of timing resistors.

If that were not enough, the voltage-controlled oscillator can also be independently gated on and off via an INHIBIT terminal, can be operated from any supply in the range 3-18 V and can, when used in conjunction with one of the 4046B's phase comparators, produce a two-phase output. The linearity of the VCO is typically a healthy 1% or so.

4046B VCO circuits

Figure 1 shows the internal block diagram and the pinouts of the 4046B phase-locked loop IC. The device contains two types of phase comparator, a VCO and a zener diode. In practical PLL applications, the VCO and one or other of the comparators are interconnected to form a 'loop', which causes the VCO to lock to the mean frequency of an input signal connected to pin 14.

For our present purposes the most important element of the IC is the VCO, ▶

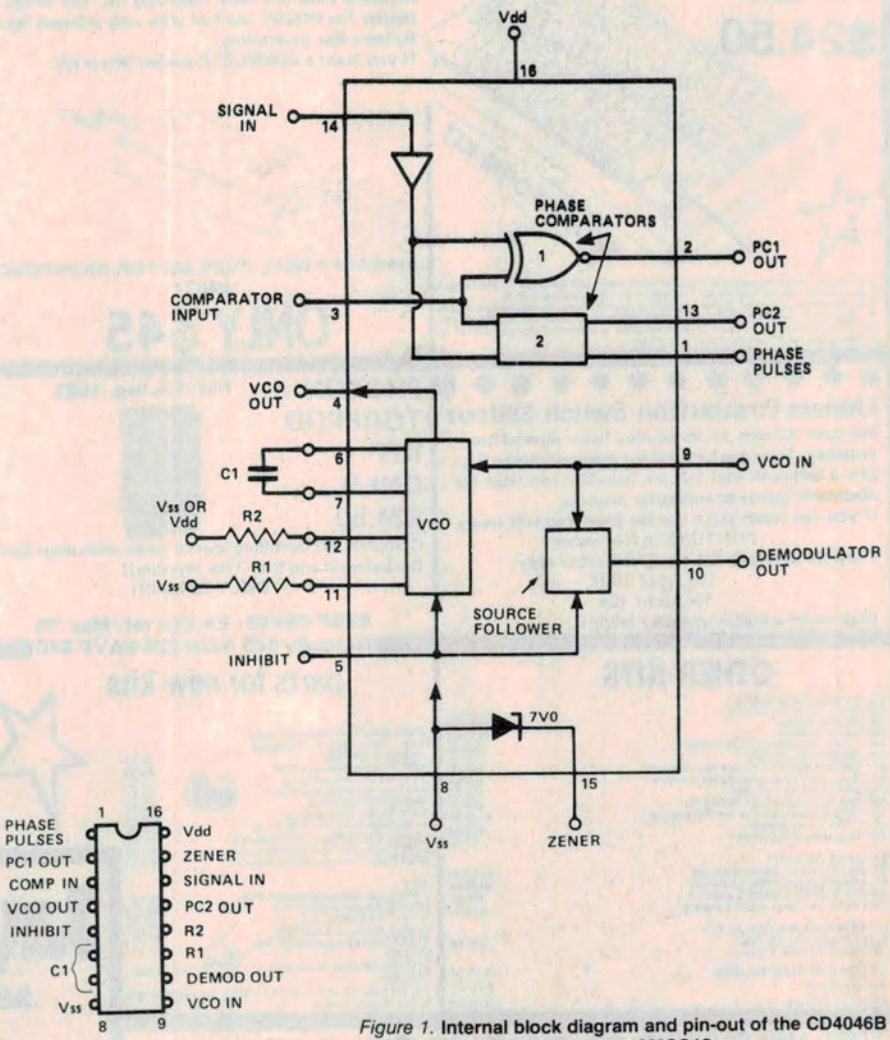

Figure 1. **Internal block diagram and pin-out of the CD4046B micropower phase-locked loop CMOS IC.**

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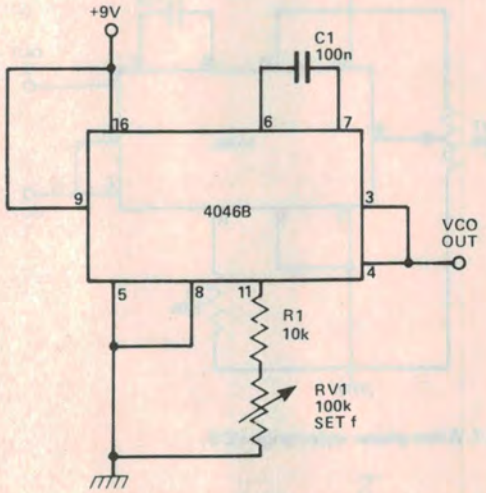

Figure 2. **Simple variable-frequency (200 Hz to 2 kHz) square wave generator.**

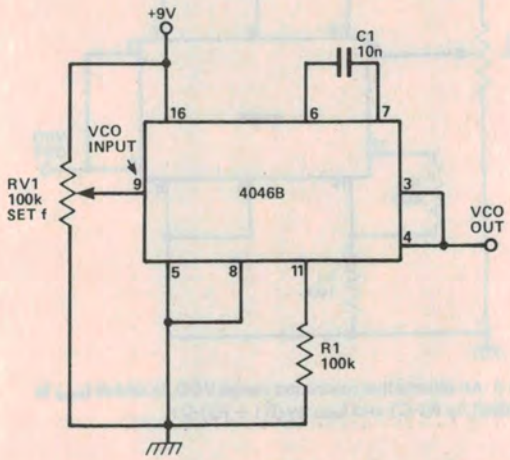

Figure 3. **Wide range VCO with frequency variable from near zero to 1.4 kHz via the pin 9 voltage.**

or voltage-controlled oscillator. The operating frequency of the oscillator is governed by the value of a capacitor connected between pins 6 and 7 (minimum value 50 pF), by the value of a resistor wired between pin 11 and ground (minimum value 10k) and by the voltage applied to VCO-input pin 9 (any value up to the supply voltage in use).

Figure 2 shows the simplest possible way of using the VCO section. Here, the pin 9 'voltage control' input is tied permanently high and the circuit acts as a basic square wave oscillator, with its frequency variable over a 10:1 range by RV1. Note at this point that the VCO output (pin 4) is tied directly to the pin 3 phase comparator input. If pin 3 is allowed to float, the comparators tend to self-oscillate at about 20 MHz and superimpose an HF signal on the top part of the VCO output waveform.

Ranging far and wide

Figure 3 shows how to connect the 4046B as a wide-range VCO. Here, R1-C1 determine the top (maximum) frequency that can be obtained and RV1 controls the actual frequency via the pin 9 voltage. The frequency falls to near zero (a few cycles per minute) with pin 9 at 0 V. The effective control range of pin 9 varies from roughly 1 V below the supply value to 1 V above zero, i.e: RV1 has a 'dead' control area of several hundred millivolts at either end of its range.

Figure 4 shows how these 'dead' areas can be eliminated by wiring a silicon diode in series with each end of RV1. The circuit also shows how the minimum operating frequency can be reduced to absolute zero by wiring a high value resistor (R2) between pins 12 and 16. Note here that, when the frequency is reduced to zero, the VCO output randomly settles in either the logic 0 or logic 1 state.

Figure 5 shows how the pin 12 resistor can alternatively be used to determine the minimum operating frequency of a restricted-range VCO. Here, f_{min} is determined by R2-C1 and f_{max} is determined by C1 and the parallel resistance of R1-R2.

Figure 6 shows an alternative version of the restricted-range VCO, in which f_{max} is controlled by R1-C1 and f_{min} is determined by C1 and the series com- ▶

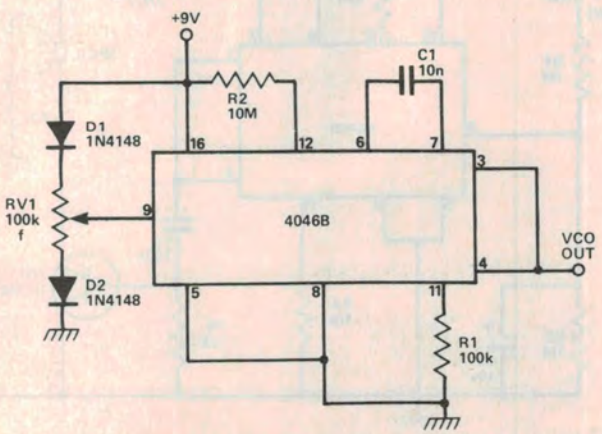

Figure 4. **Wide range VCO with frequency variable down to absolute zero.**

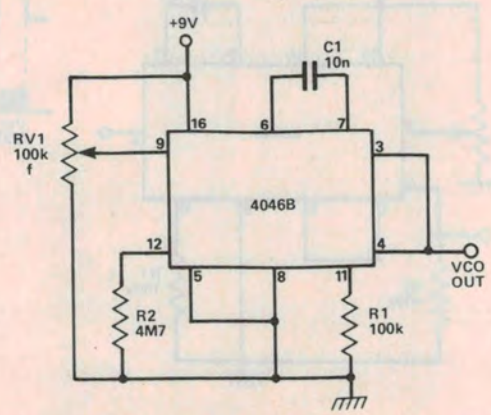

Figure 5. **Restricted range VCO with frequency variable from 60 Hz to 1.4 kHz by RV1. R2 acts as an offset resistor.**

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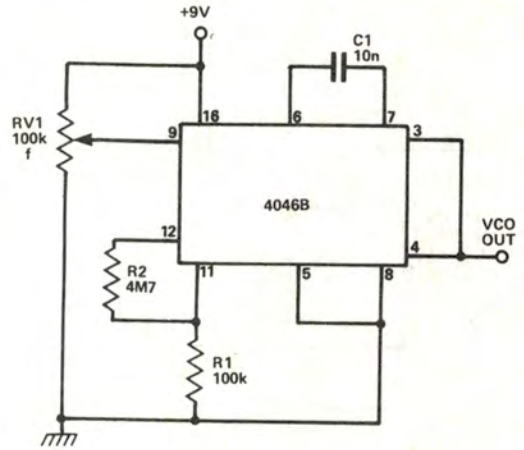

Figure 6. **An alternative restricted range VCO, in which f_{max} is controlled by R1-C1 and f_{min} by (R1 + R2)-C1.**

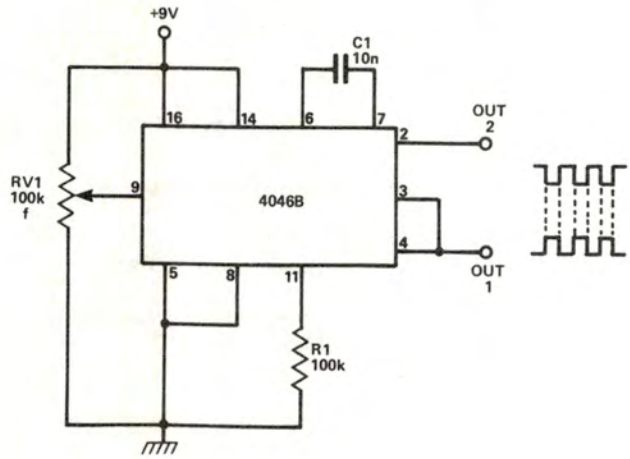

Figure 7. **A two-phase wide-range VCO.**

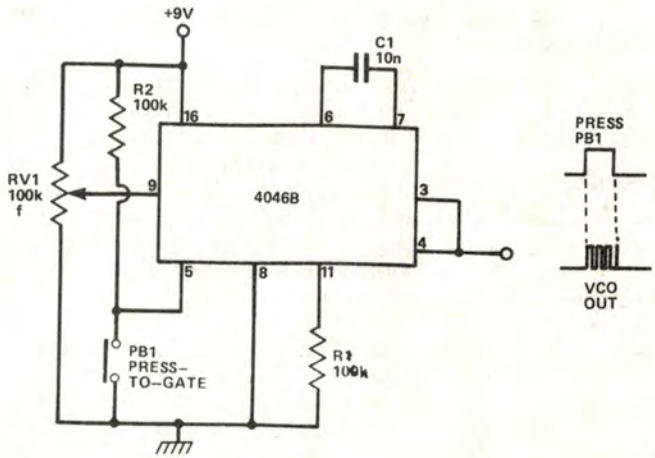

Figure 8. **A manually gated wide-range VCO.**

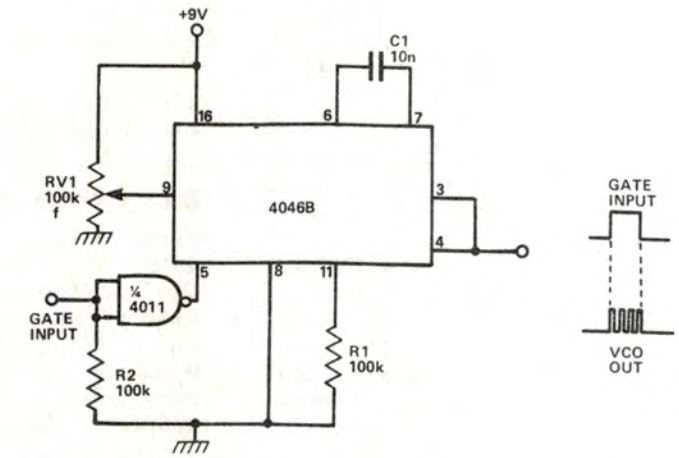

Figure 9. **An electronically gated wide-range VCO, using an external gate inverter.**

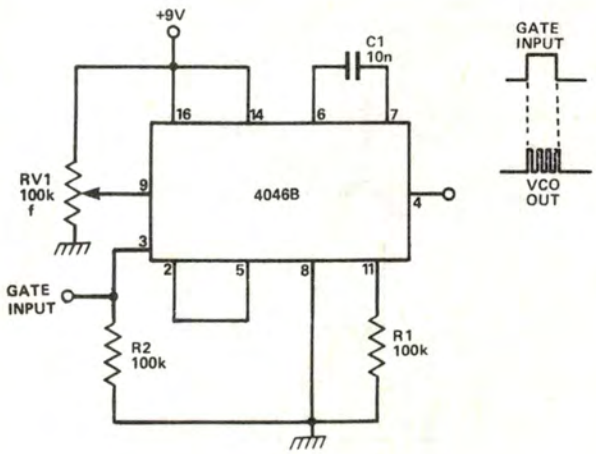

Figure 10. **An electronically gated wide-range VCO using the internal EX-OR phase detector for gate inversion.**

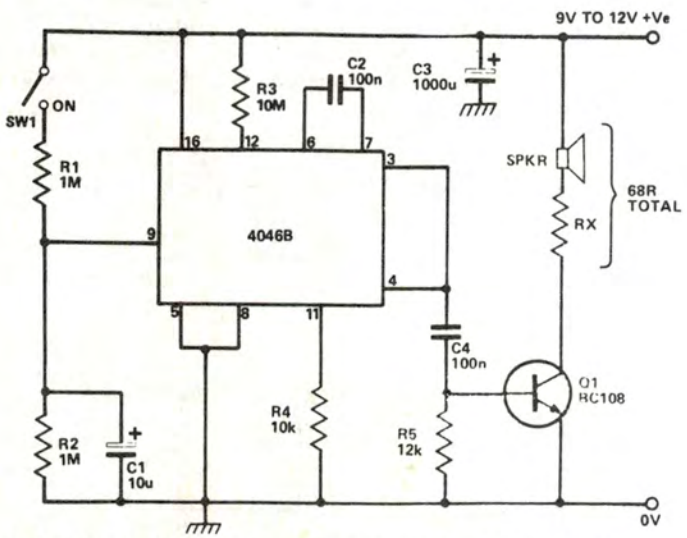

Figure 11. **An electronic siren giving slow rise and fall of its operating frequency.**

bination of R1 and R2. Note that, by suitable choice of the R1 and R2 values, the restricted-range VCO can be made to span any range from 1:1 to near infinity.

Square pair

The VCO can be made to generate a pair of anti-phase square wave outputs by connecting its output to the phase-comparator input, taking the signal input (pin 14) high and taking the anti-phase output from pin 2. Figure 7 shows the connections. Note that this circuit makes use of the IC's built-in EX-OR gate (phase comparator 1).

The VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic level 1). This feature enables the VCO to be gated on and off by external signals. Figure 8 shows how the VCO can be manually gated via a pushbutton connected directly to pin 5, while Figure 9 shows how the circuit can be gated electronically by an external gate inverter. Alternatively, if the two-phase output facility is not required, the internal EX-OR phase detector can be used to provide gate inversion, as shown in Figure 10. Note in this latter case that pin 4 is not connected to pin 3.

Sirens and sound effects

Figures 11 to 14 show some practical siren and sound effects generator VCO circuits. Figure 11 is a conventional siren circuit. When SW1 is closed, C1 charges exponentially via R1 and the VCO frequency rises slowly from zero to a maximum value. When SW1 is opened, C1 discharges via R2 and the operating frequency slowly decays to zero. The VCO output is ac-coupled to the speaker via C4 and Q1.

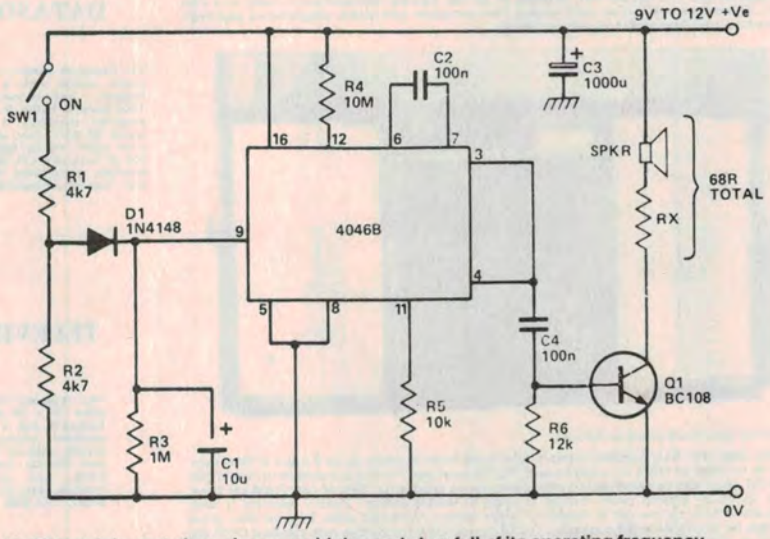

Figure 12. **This quick-start siren gives a rapid rise and slow fall of its operating frequency.**

The Figure 12 quick-start siren is similar to the above, except that C1 charges rapidly to half supply volts via R1, R2 and D1 when SW1 is closed and discharges slowly via R3 when SW1 is opened.

The Figure 13 circuit produces a 'phaser' sound when PB1 is closed. The 4011 astable is gated by PB1 and produces a chain of 4 ms pulses at intervals of 70 ms. Each pulse rapidly charges C2 via R3 and D2, to produce a high tone that then decays rapidly as C2 discharges via R5, only to be repeated again on the arrival of the next pulse.

The Figure 14 circuit generates either a pulsed tone or a warble tone signal (depending on the setting of SW1) when PB1 is closed. PB1 is used both to enable pin 5 of the 4046B and to gate on the 4001 astable, which then applies a rectangular (alternatively fully high and fully low) waveform to pin 9. In the pulsed mode the VCO generates zero frequency when pin 9 is low. In the warble mode it generates a tone that is 20% down on the high tone when pin 9 is low.

Miscellaneous VCO circuits

Figures 15 to 17 show a miscellany of 4046B VCO circuits. The Figure 15 circuit is that of an FSK generator which produces a 2.4 kHz tone when a logic 1 signal is applied to pin 9 and a 1.2 kHz tone when a logic 0 signal is ▶

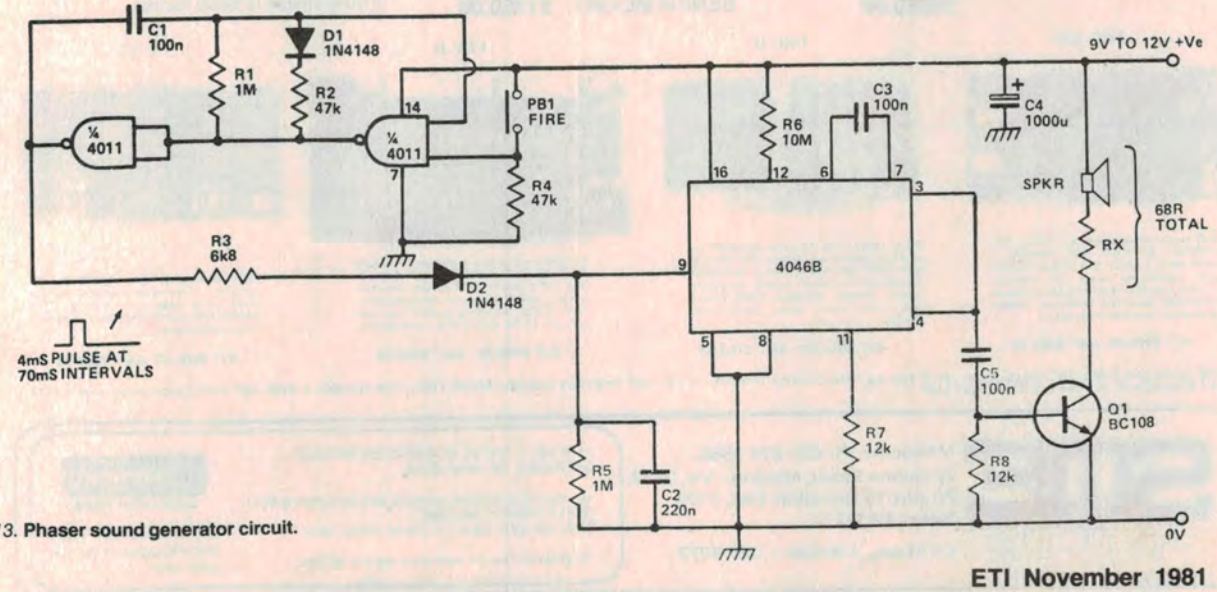

Figure 13. **Phaser sound generator circuit.**

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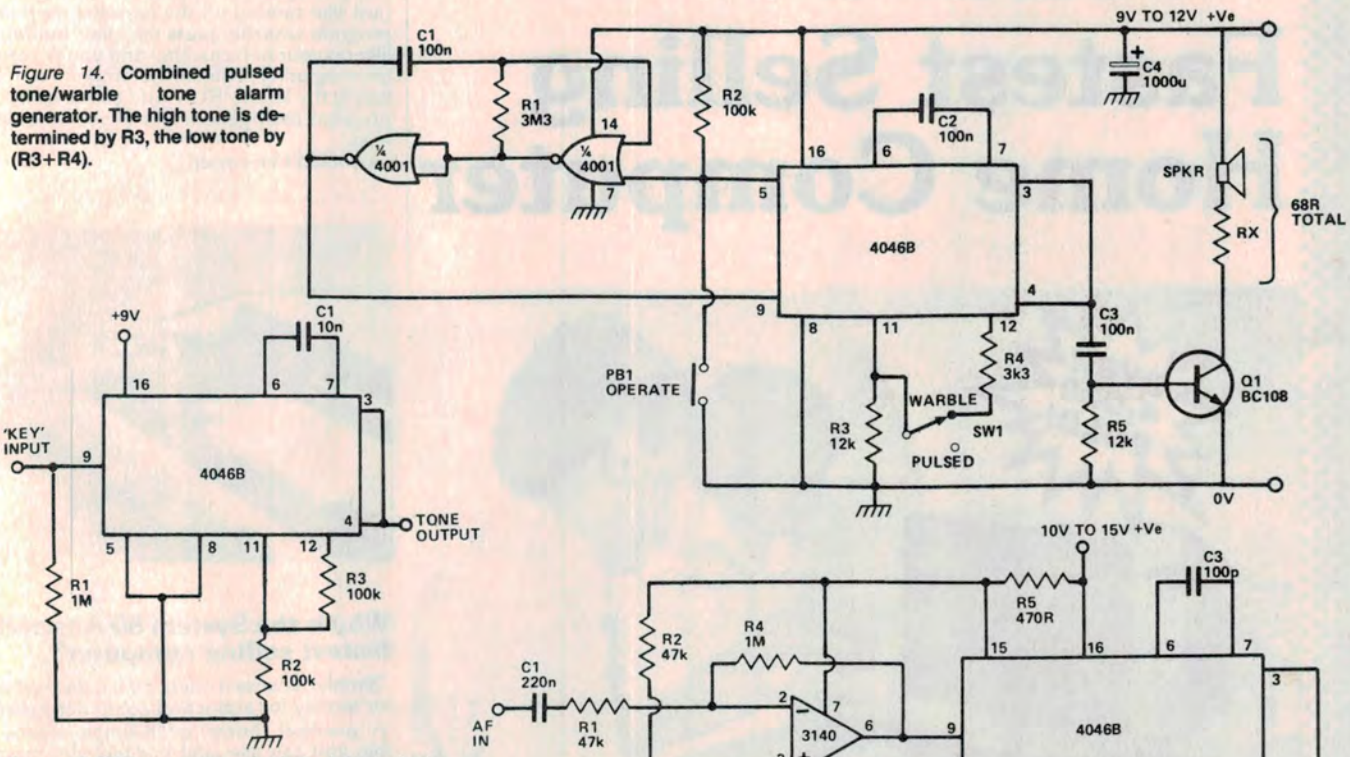

Figure 14. **Combined pulsed tone/warble tone alarm generator. The high tone is determined by R3, the low tone by (R3+R4).**

Figure 15. **FSK generator — logic 0=1.2 kHz, logic 1=2.4 kHz.**

applied. The high tone is controlled by R2 and the low tone by R2 and R3.

Figure 16 is a 220 kHz FM generator. The internal zener of the 4046B (pin 15) is used to provide a stable 7 V supply to the x20 3140 inverting amplifier, which is quiescently biased at 3.5 V by the R2-R3 potential divider. The pin 9 VCO signal is thus a mean 3.5 V potential amplitude modulated by an amplified version of the AF input signal, which thus frequency-modulates the output of the VCO.

Figure 16. **220 kHz FM generator.**

Running down

The Figure 17 circuit is that of a run-down clock generator of the type used in dice and roulette games. When PB1 is pressed, C1 charges to a high voltage via D2. Simultaneously, Q1 is biased on via D3-D4 and effectively connects R6 between pin 11 and ground. Under this condition, the VCO operates a high frequency (tens of kHz) and effectively generates a random number of clock pulses. When PB is released, Q1 turns off and the VCO timing is governed by R8. Simultaneously, C1 rapidly discharges to half supply volts via R1-R2-D1, so the VCO operates at only 100 Hz or so. C1 then slowly discharges via R3 and the VCO frequency slowly decays to zero over a period of about 15 seconds. ●

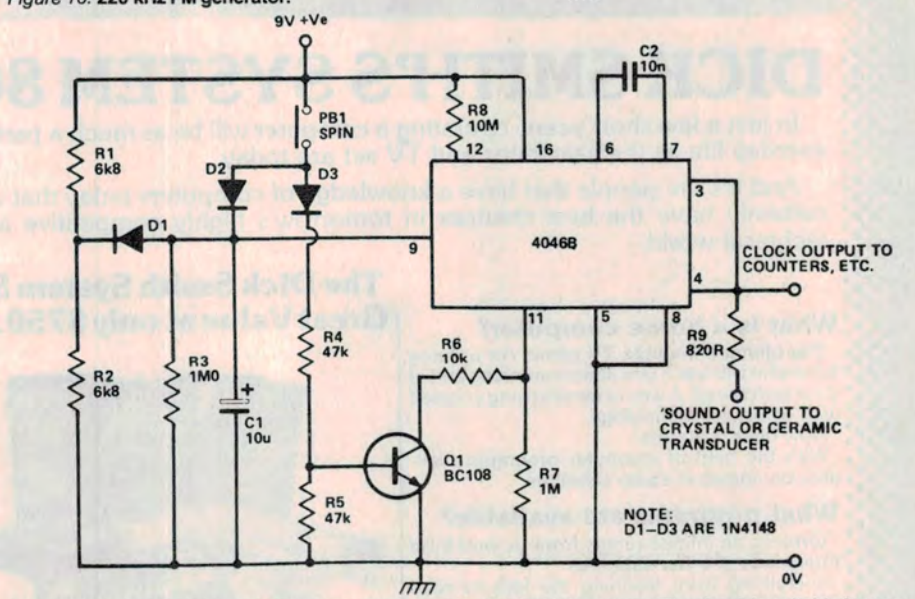

Figure 17. **Run-down clock/sound generator for use in dice/roulette games. The circuit is suitable for use with edge-sensitive clock circuits only. The output can be used to directly clock most types of counter and can be fed, via R9, to crystal or ceramic transducers to directly produce 'run down' sounds. When the run-down is complete this circuit may settle in either logic 0 or 1, so it cannot safely be used to clock level-sensitive circuitry.**