Staggered-finger heat sink design is more efficient, saves space and weight

Unique design is causing circuit designers to re-think their thermal theory.

Design engineers are learning daily that power ratings of power transistors are often not at all what they appear to be at first glance. For example, the data sheet on a transistor may state, "maximum power dissipation — 50 watts." But the fine print — if there is any — says, *"at 25°C case temperature."* Actually, the transistor alone will dissipate only 3 to 4 watts before the maximum allowable junction temperature is reached!

Obviously, something must be done to maintain the specified case temperature when more than 3-4 watts are to be dissipated. This is normally accomplished by mounting the transistor case to a dissipator or heat sink, but dissipator state-of-the-art has been such that these devices are too bulky, too heavy — just plain inefficient. Now you needn't tolerate these size and weight penalties in your design because IERC has achieved a major breakthrough in heat sink design: The IERC Staggered Finger Dissipator.

International Electronic Research Corporation has developed a broad line of these smaller, lighter, much more efficient heat dissipators based on the unique, multiple staggered finger design which has proven to be 30% more efficient overall, and in some cases up to 500% more effective than many conventional designs now in wide use. An example of the staggered finger design is shown in Figure 1. This is an IERC HP3 Heat Dissipator. To show how efficient this device is, it is shown compared to a common finned extrusion. The HP3 and the extrusion are virtually equivalent in their heat dissipating ability; however, the HP3 is only ⅓rd the weight and ⅔rd the volume of the extrusion.

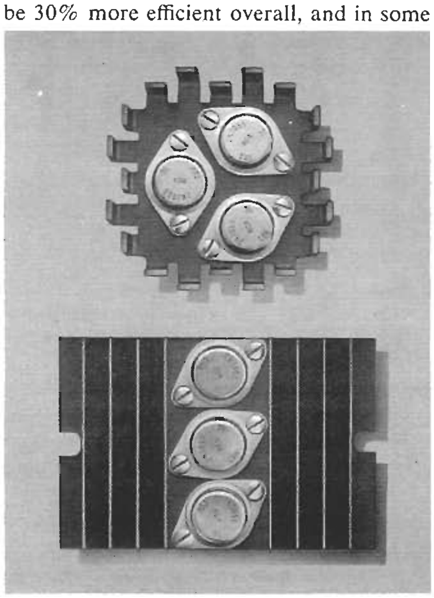


FIGURE 1

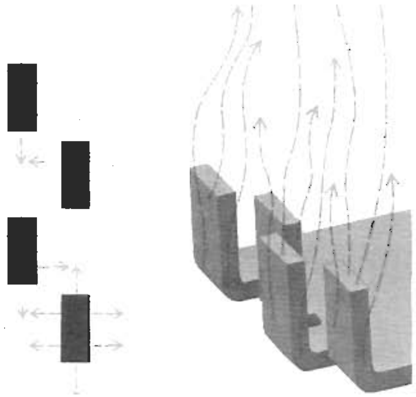


FIGURE 2

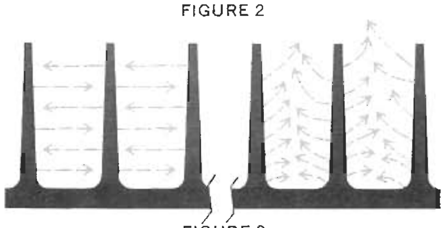


FIGURE 3

The secret to the efficiency of the new dissipators is the staggered fingers. (Figure 2) Note how the fingers are positioned so they do not radiate to each other and the configuration is so arranged that natural convection takes place very readily.

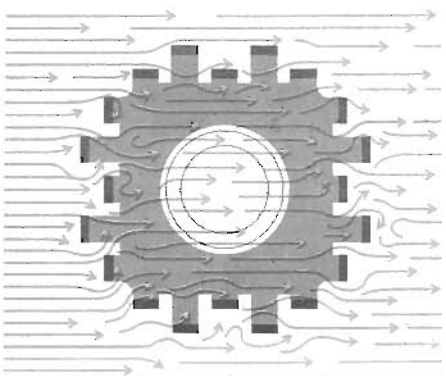


FIGURE 4

In a finned extrusion the fins radiate to each other and it is difficult for natural convection to take place in the confined area between the fins. (Figure 3)

In a forced air environment the staggered finger configuration is even more effective. The air can be from any direction. (Figure 4) As it hits the fingers, turbulence causes it to move around each of the fingers, striking many surfaces in its flow past the part. The turbulent air against these surfaces disturbs their surface barrier and is the principal reason for the significant improvement in the forced air heat dissipating properties of these parts.

Compare this turbulent air flow over the staggered fingers of the IERC part with the air flow conditions when directed at a finned extrusion. Here laminar air flow, rather than turbulent air flow, takes place. The air must be directed in one direction only, (Figure 5) parallel to the fins. The air enters the space between the fins; but because of this restricted space, it immediately tries to leave. Shortly after entering, it is not flowing against the bottom of the fin surfaces. Since the air flow is laminar, not turbulent, and it is not disturbing the surface barrier at the bottom of the fins shortly after entering, the surface areas of the fins are only partially effective.

The old rule-of-thumb which considers only the surface area relative to heat dissipation is not valid. The effectiveness of the area must also be considered. The staggered finger concept is a significant breakthrough in heat dissipating devices and is the first improvement in heat dissipator design since the flat fin or extrusion design.

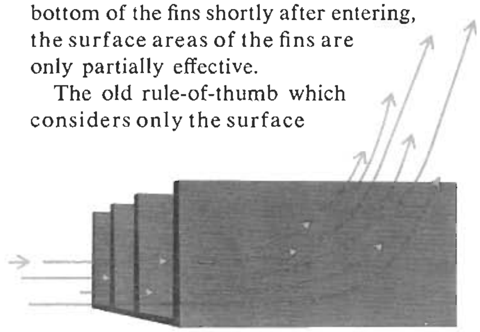


FIGURE 5

Broad line accommodates all lead and case mounted semiconductors.

During the past several years, IERC has developed numerous heat dissipating devices using the staggered finger configuration.

The UP style (Figure 6) is just 1.78 inches square and is available in various heights up to one inch. It was designed particularly to accommodate a single power transistor such as a TO36, TO3, TO15, etc. However, it will also accommodate more than one smaller semiconductor, including the newer plastic case power transistors.

To really appreciate the efficiency of the UP, refer to the temperature vs. power

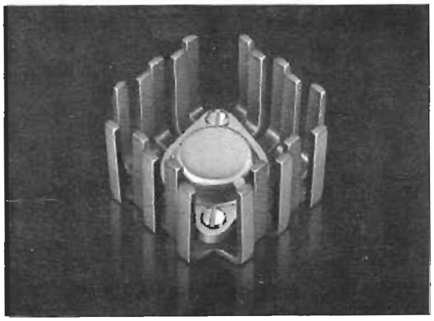


FIGURE 6

curve (Figure 7) showing a 2N1208 power transistor mounted in a UP-TO15-B dissipator. Remember, now, that this UP part weighs *less than one ounce*. Considering a maximum case rise of 100°C, the 2N1208 by itself will dissipate only 3 watts. When mounted in the UP dissipator in natural convection, it will dissipate 14 watts, or

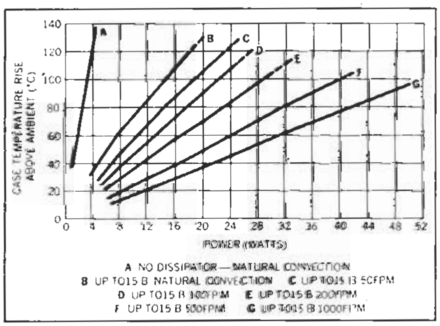


FIGURE 7

more than four times more power at the same case temperature. In a forced air environment of only 200 FPM, 28 watts can be dissipated — more than nine times the power at the same case temperature. With 1000 FPM, the remarkable light weight UP will allow 50 watts of dissipation from the transistor — *seventeen times more power at the same case temperature.*

Think now. You must limit the case temperature rise of a power transistor to 100°C. You need to dissipate 14, 28 or 50 watts. You have three cubic inches of space and are limited to adding one ounce of weight. And you can't spend more than 40 cents for a dissipator or sink in medium quantities. What would your present thinking lead you to do?

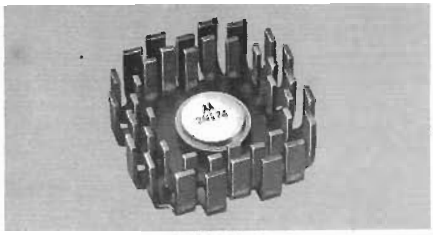


FIGURE 8

Another IERC dissipator, the HP1, is a companion to the HP3 shown in Figure 1. The HP1 is 2½ inches square, slightly larger than the UP. At the same case temperature rise of 100°C, it will dissipate 23 watts in natural convection; in a forced air flow of 200 FPM, it will dissipate 33 watts; and 65 watts with 1000 FPM. The HP3, which is 3⅛ inches square, will dissipate 28 watts in natural convection, 42 watts with 200 FPM, and 74 watts with 1000 FPM. When the HP1 and HP3 are nested, Figure 8, more than 100 watts can be dissipated at the same 100°C case temperature rise with 1000 FPM.

Stop and contemplate the sizes of heat dissipating devices which would have been required to dissipate these powers before the advent of the staggered finger design, and you will appreciate the savings of space and weight which the UP and HP make possible.

The staggered finger design has also been used in heat dissipators for TO5 and TO18 metal case transistors. Models in the LP Series, Figure 9, are available in three lengths and two heights and to accommodate one or two transistors. These parts are so efficient that when a TO5 transistor is mounted in the largest model

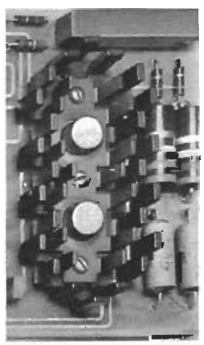


FIGURE 9

LP dissipator (only 2.31 x 1.12 x ½), the dissipator is virtually an infinite heat sink. The case temperature rises only 65°C when 5 watts are being dissipated. When 1000 FPM of air is used at 5 watts dissipation, the case temperature rise is phenomenally low — less than 15°C.

In addition to their thermal efficiency, LP parts are extremely versatile. Almost any application problem where a conduction plane is not available can be solved with these simple, low cost devices.

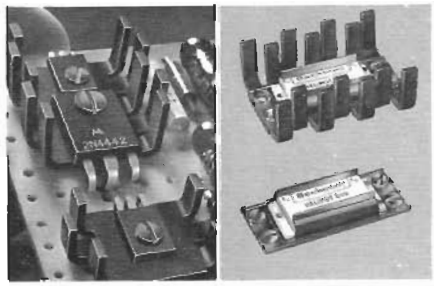


FIGURE 10

The staggered finger concept is also available in dissipators for plastic case power transistors and integrated circuits and microcircuit packages as shown in Figure 10.

The staggered finger concept of heat dissipation is the most significant breakthrough in heat sink technology since the advent of the power transistor. Get specific technical and pricing information on those IERC heat dissipators most applicable to your needs. Write on your company letterhead for Technical Bulletin 149 for more detailed information on the PA and PB series and Technical Bulletin 151 for the LB series. Technical Bulletin 134 and Test Report 172A detail the UP series; Technical Bulletin 139 and Test Report 198 cover the HP series; and for the LP series, ask for Technical Bulletin 135 and Test Report 182. You'll be surprised how substantially these advanced new heat sinks will contribute to the efficiency of your design and your equipment.

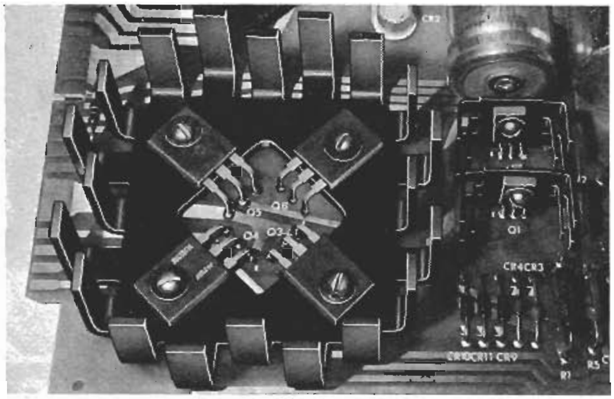
International Electronic Research Corporation, a corporate division of Dynamics Corporation of America, 135 West Magnolia Boulevard, Burbank, California 91502.

IERC | DCA

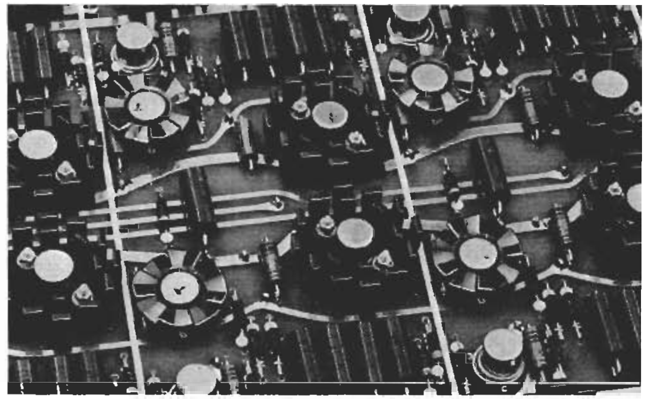
HEAT SINKS/DISSIPATORS

These ideas for cooling board-mounted semis could improve your circuit's performance

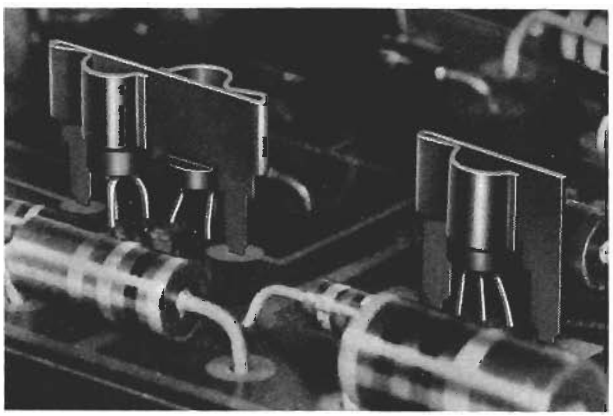
Thermal management is a highly versatile and valuable circuit design tool that can be used to increase semiconductor power, increase circuit density (or reduce the number of semiconductors), improve switching and temperature-related rise and fall characteristics, increase small signal gain and DC beta, match operating characteristics of two or more devices, improve reliability and cut costs. Here are some ways circuit designers have used IERC heat sinks/dissipators to beat printed circuit board-mounted semiconductor heat problems in order to improve their circuits, ideas that may be of help to you.



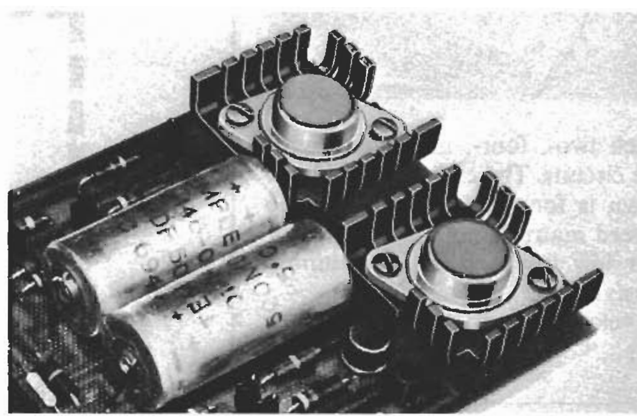
Four times the power from four power plastics took just one IERC dissipator. Bare transistors were capable of only 2 watts with 102°C substrate rise above ambient so designer used modified HP3 dissipator and got 8 watts from each at the same temperature rise. Or you could improve transistor life — roughly 7 times — by operating the devices at 2 watts and letting the same dissipator keep the substrate temperature rise to 32°.



Temperature matching at varying power levels is easy with the wide variety of IERC dissipators. On this board problem was to keep TO-5s at approximately equal case temperatures although some were operated at 2.2 watts and others at 1 watt. Press-on Fan Tops costing pennies kept 1 watters at 55°C case rise above ambient while LP dissipators held 2.2-watt devices at nearly identical case temperatures. IERC Insulube® coating permits mounting LPs directly on printed circuit lines.



Dissipators protect circuit — Designer of this TV circuit made sure dissipators would stay when D-case devices needed replacing. He designed dissipators as a part of the circuit, making it impossible to fire the circuit without them. In addition to this circuit protection the dual "Universals" gave him some other benefits: excellent retention in shock/vibration environments, good heat sinking during solder operations, and they cost just pennies.



Lower cost per unit was result of replacing four TO-3s used in this 10-watt power supply with two TO-3s in UP3 dissipators. Dissipators allow two TO-3s to operate at 5 watts each with same 65°C case rise above ambient as four devices operated at 2.5 watts each. Low profile dissipators plus TO-3s were assembled in less space allotted to four transistors. New design saved money, improved reliability.