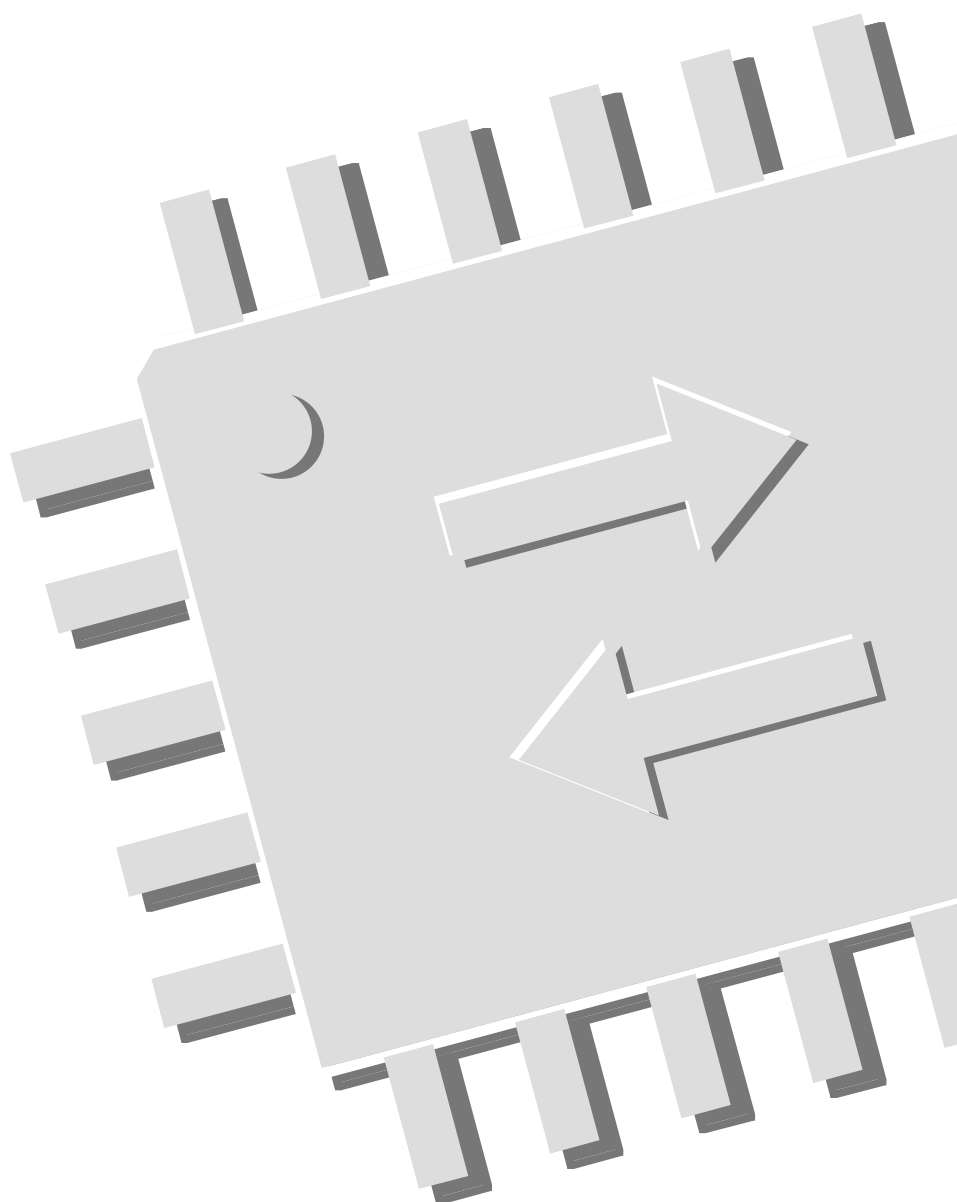


LINK (IEEE 1394)

MD8413

Users Manual

PRELIMINARY



MEMO

History

Rev.	Date	Comments
0.81	11/13/1996	Initialized Register s at LinkReset
0.90	12/25/1996	DC/AC timing and pinout
0.91	01/25/1997	Minor change

MEMO

Keys:

MSB, LSB of data : MSB on the right and LSB on the left

Negative logic signal description : Attached with # at the last end of signal name

Numeral description : Binary ****b or ****
 Decimal ****
 Hexadecimal ****h or 0x****

Table descriptions : The area hatched without names on the table of registers, etc., denotes an invalid area, and there is no change in operation.

Terminology : Byte Data in 8-bit width
 Word Data in 16-bit width
 Quadlet Data in 32-bit width
 Octlet Data in 64-bit width

Associated Materials

IEEE 1394 -1995 Standard for a High Performance Serial Bus

IEEE Std 1212-1991 Command and Status Register architecture

MEMO

Contents

1 Introduction	1
1-1 Features	1
1-2 Applications	1
1-3 Internal Block Diagram	2
1-4 Outline Functions	3
1-4-1 Host Interface	3
1-4-2 PHY Interface	3
1-4-3 Transmitter	3
1-4-4 Receiver	3
1-4-5 Built-in Buffer	3
1-4-6 Isochronous Transfer Function	4
2 Terminal Descriptions	5
2-1 Functional Descriptions of Terminals	5
3 Control Register	8
3-2 Register Contents	8
3-2-1-1 Version Register	8
3-2-1-2 Revision Register	8
3-2-2-1 Control Register-H	9
3-2-2-2 Control Register-L	11
3-2-3-1 Node Identification Register-H	13
3-2-3-2 Node Identification Register-H	13
3-2-4 Reset Register	15
3-2-5 Asynchronous Buffer Size Set Register	17
3-2-6 Packet Control Register	18
3-2-7-1 Diagnostic Status Register-H	20
3-2-7-2 Diagnostic Status Register-L	21
3-2-8 Phy Control Register	22
3-2-9-1 ATRetries Register	23
3-2-9-2 ATRetries Register	24
3-2-9-3 ATRetries Register	25
3-2-10-1 Cycle Timer Register-H	26
3-2-10-2 Cycle Timer Register-L	26
3-2-11-1 Bus Time Register-H	28
3-2-11-2 Bus Time Register-L	28
3-2-12-1 Isochronous Transmit Configuration Register	29
3-2-12-2 Isochronous Transmit Configuration Register	29
3-2-12-3 Isochronous Transmit Configuration Register	30
3-2-13-1 Isochronous Receive Configuration Register 1,2,3,4	32
3-2-13-2 Isochronous Receive Configuration Register 1,2,3,4	32
3-2-14-1 ATF Data Register -H	34
3-2-14-2 ATF Data Register -L	34
3-2-15-1 ARF Data Register -H	34

3-2-15-2 ARF Data Register -L	35
3-2-16-1 Buffer Status and Control Register	36
3-2-17-1 Interrupt Register -H	38
3-2-17-2 Interrupt Register -L	39
3-2-18-1 Interrupt Mask Register -1-H	40
3-2-18-2 Interrupt Mask Register -1-L	40
3-2-19-1 Interrupt Mask Register -2-H	40
3-2-19-2 Interrupt Mask Register -2-L	40
3-2-20 Split TimeOut Register	41
3-2-21 Split TimeOut Register	41
3-2-23 Split Timer Start Register	41
3-2-24-1 GPIO Register	42
3-2-24-2 GPIO Register	42
3-2-25 ATGo Register	44
3-3 List of Registers	45
4 Data Format	49
4-1 Asynchronous	49
4-1-1 Quadlet Transmit	49
4-1-2 Block Transmit	50
4-1-3 Quadlet Receive	51
4-1-4 Block Receive	52
4-2 Isochronous	55
4-2-1 For Normal Mode	55
4-2-1-1 Transmit	55
4-2-1-2 Receive	55
4-2-2 For Auto Mode	56
4-2-2-1 Transmit	56
4-2-2-2 Receive	57
4-3 Snoop	57
4-4 SelfID Packet	59
4-5 PHY Control Packet	62
4-6 Code	62
5 Functional Descriptions	64
5-1 Host Interface	64
5-1-1 Register Access Timing	64
5-1-2 Host Bus Width	65
5-1-3 DMA Transfer	65
5-1-4 Interrupt Processing	66
5-2 PHY Chip Interface	66
5-2-1 Connection Method	66
5-2-2 PHY Chip Control	67
5-2-3 Request	67
5-2-3-1 LREQ	68
5-2-4 Transfer	70
5-2-4-1 Status Request	70

5-2-4-2 Transmit	71
5-2-4-3 Receive	72
5-3 Buffer Access	73
5-3-1 Buffer Configuration	73
5-3-2 Size Setting for Each Sub-Buffer.....	73
5-3-3-1 Soft Access	74
5-3-3-2 DMA Access.....	74
5-3-4 Buffer Control	75
5-3-4-1 Asynchronous Buffer Control	75
5-3-4-1-1 Transmission Buffer	75
5-3-4-1-2 Reception Buffer	76
5-6 32-bit CRC	78
5-7 Control Flow	78
5-7-1 Asynchronous Transmission	79
5-7-2 Asynchronous Reception	81
6 Processing.....	84
7 Processing for BusReset.....	86
7-1 After Closure of POWER Switch	86
7-2	86
8 Exclusive Isochronous Bus	86
8-1 Isochronous Cycle Start Timing	86
8-2 Request-to-Send Processing	86
8-3 Processing for Multi-Channel Transmission.....	88
8-4 Processing for Reception	88
8-4-1 BE# Signal.....	89
8-4-2 CH Signal.....	89
8-4-3 SYNC Signal	89
8-5 Reception of CycleStartPacket	90
8-6 Packet Error Announcement for Reception.....	91
8-6-1 Error Announcement for Cycle Start Packet	91
8-6-2 Error Announcement for Isochronous Packet	91
8-7 Discrepancy in Timing between 100MHz and 200MHz	92
8-8 Example Isochronous Bus Timing.....	92
8-8-1 Example Receive Timing.....	92
8-8-2 Example Receive Timing.....	93
9 Electric Characteristics	96
9-1 Absolute Maximum Rating	96
9-2 Recommended Operating Condition	96
9-3 DC Characteristics	97
9-4 AC Characteristics	98
10 Terminal Arrays and Outline Drawings.....	106
10-1 Terminal Arrays.....	106
10-2 External Dimensions	107
Appendix 1 I/O Status	108

Appendix 2 Example circuit for AC connection.....	109
Notes	110

Contents of Figures and Tables

Figure 1-3-1	Block Diagram of MD8413.....	2
Figure 5-1-1	Host Access Timing.....	59
Figure 5-1-1	DMA Transfer Timing	60
Figure 5-1-2	DREQ Negate Timing.....	61
Figure 5-2-1	MD8413-PHY Chip Connection Diagram (DC Connection)	61
Figure 5-2-2	MD8413-MD8402 Connection Diagram (AC Connection).....	62
Figure 5-2-3	LREQ Stream.....	63
Figure 5-2-4	Status Request.....	65
Figure 5-2-5	Transmit.....	66
Figure 5-2-6	Receive.....	67
Figure 5-3-3	ARF/ATF Size Allocation.....	68
Figure 5-3-4	Register Operation during Soft Access (ATF)	69
Figure 5-3-5	Register Operation during Soft Access (ARF).....	69
Figure 5-3-6	Register Operation during DMA Access (ATF).....	69
Figure 5-3-7	Register Operation during DMA Access (ARF)	69
Figure 5-3-8	Concept of ATF Operation.....	71
Figure 5-3-9	Concept of ARF Operation	72
Figure 5-3-10	ARF Operation after BusReset (ARFBusReset="0").....	72
Figure 5-3-11	ARF Operation after BusReset (ARFBusReset="1").....	73
Figure 5-7-1	ATF Transmission Flow 1	74
Figure 5-7-2	ATF Transmission Flow 2	75
Figure 5-7-3	ARF Reception Flow 1.....	76
Figure 5-7-4	ARF Reception Flow 2.....	77
Figure 8-2	Isochronous Transmission Timing	82
Figure 8-3	Multi-Channel Isochronous Transmission Timing.....	83
Figure 8-4	Isochronous Reception Timing.....	84
Figure 8-5	Cycle_Time_Data Output Timing	85
Figure 8-6-1	Error Timing for Cycle Start Packet.....	86
Figure 8-6-2	Patterns of IRERR# Appearance	87
Figure 8-7	100/200Mbps Timing	87
Figure 8-8-1	Isochronous Bus Timing (1).....	89
Figure 8-8-2	Isochronous Bus Timing (2).....	90
Figure 9-4-1	Host Interface AC Characteristics (Read/Write).....	94
Figure 9-4-2	Host Interface AC Characteristics (Reset).....	94
Figure 9-4-3	Host Interface AC Characteristics (DMA)	95
Figure 9-4-4	Host Interface AC Characteristics (CYCLEIN/OUT)	96
Figure 9-4-5	PHY Interface AC Characteristics (SCLK).....	97
Figure 9-4-6	PHY Interface AC Characteristics (CTL,D).....	98
Figure 9-4-7	PHY Interface AC Characteristics (LREQ)	98

Figure 9-4-8	Isochronous Bus AC Characteristics (???).....	98
Table 2-1	MD8413 Terminals (1)	5
Table 2-2	MD8413 Terminals (2)	6
Table 2-3	MD8413 Terminals (3)	7
Table 4-1-1	Quadlet Transmit format (Asynchronous).....	49
Table 4-1-2	Block Transmit format (Asynchronous)	50
Table 4-1-3	Quadlet Receive format (Asynchronous).....	51
Table 4-1-4	Block Receive format (Asynchronous)	52
Table 4-3-1	Snoop Receive format	54
Table 4-4-1	SelfID Packet Receive format (first quadlet).....	55
Table 4-4-2	SelfID Packet Receive format (SelfID Packet #0)	55
Table 4-4-3	SelfID Packet Receive format (SelfID Packet #1, #2, & #3)	55
Table 4-4-4	SelfID Packet Receive format (last quadlet)	55
Table 4-4-5	SelfID Packet Receive format (pn)	55
Table 4-5-1	PHY control packet format (first quadlet).....	57
Table 4-6-1	List of Retry Codes	57
Table 4-6-2	List of Transaction Codes (tCode).....	57
Table 4-6-3	List of Bus Number / Node Numbers.....	57
Table 4-6-4	List of Data Length (dataLength).....	58
Table 4-6-5	List of Extension Transaction Codes (Extended tCode)	58
Table 4-6-6	List of Speed Codes (spd)	58
Table 4-6-7	List of Acknowledge Codes (Ack)	58
Table 5-1-3	Assert / Negate Condition of the DREQ Signal	60
Table 5-2-1	PHY Chip Control Mode 1	62
Table 5-2-2	PHY Chip Control Mode 2	62
Table 5-2-3	Request Format.....	63
Table 5-2-4	Speed Format.....	63
Table 5-2-5	Read Register Format	63
Table 5-2-5	Write Register Format	63
Table 5-2-6	Request Type	64
Table 5-2-7	Status Request Format.....	65
Table 5-2-8	Speed Codes (SP[0:7]).....	67
Table 5-7-1	Interrupt and FIFO Conditions for ARF Reception	78
Table 8-1	Contents of CTm	85
Table 8-2	Contents of CTI	85
Table 9-4-1	Host Interface AC Characteristics	93
Table 9-4-2	PHY Interface AC Characteristics	97
Table 9-4-3	Isochronous Bus AC Characteristics	99

MEMO

1 Introduction

The MD8413 is a controller for high-speed serial-bus link layers, arranged in accordance with IEEE P1394, Draft8.2. It has all necessary functions for the link layer as a matter of course, and it also offers maximum transfer performance with an isochronous packet, by gaining access to the outside through an exclusive bus.

1-1 Features

- ✦ Packing for transmission and unpacking for reception, according to IEEE 1394 - 1995
- ✦ Supporting the CycleMaster
- ✦ Parity generation and error detection by 32-bit CRC
- ✦ Detection of dropped cycle start messages
- ✦ Direct with PHY chip (MD8402) and interface by AC coupling
- ✦ Controlling the transfer number for each cycle during isochronous transfer
- ✦ Automatic insertion of a header during transmission and automatic separation of the header during reception for the isochronous packet
- ✦ Full support of the out-band retry sequence
- ✦ Data bus for exclusive isochronous send/receive
- ✦ Support of control signals toward LPS (Link Power Status) of PHY (MD8402)
- ✦ Supporting the bus time register

1-2 Applications

- | | | |
|----------------------------------|---------------|-----------------|
| ✦ Digital camera | ✦ Digital VTR | ✦ Digital audio |
| ✦ Electronic musical instruments | ✦ Scanner | ✦ Printer |
| ✦ Various storages | ✦ DVD | ✦ Set-top box |

1-3 Internal Block Diagram

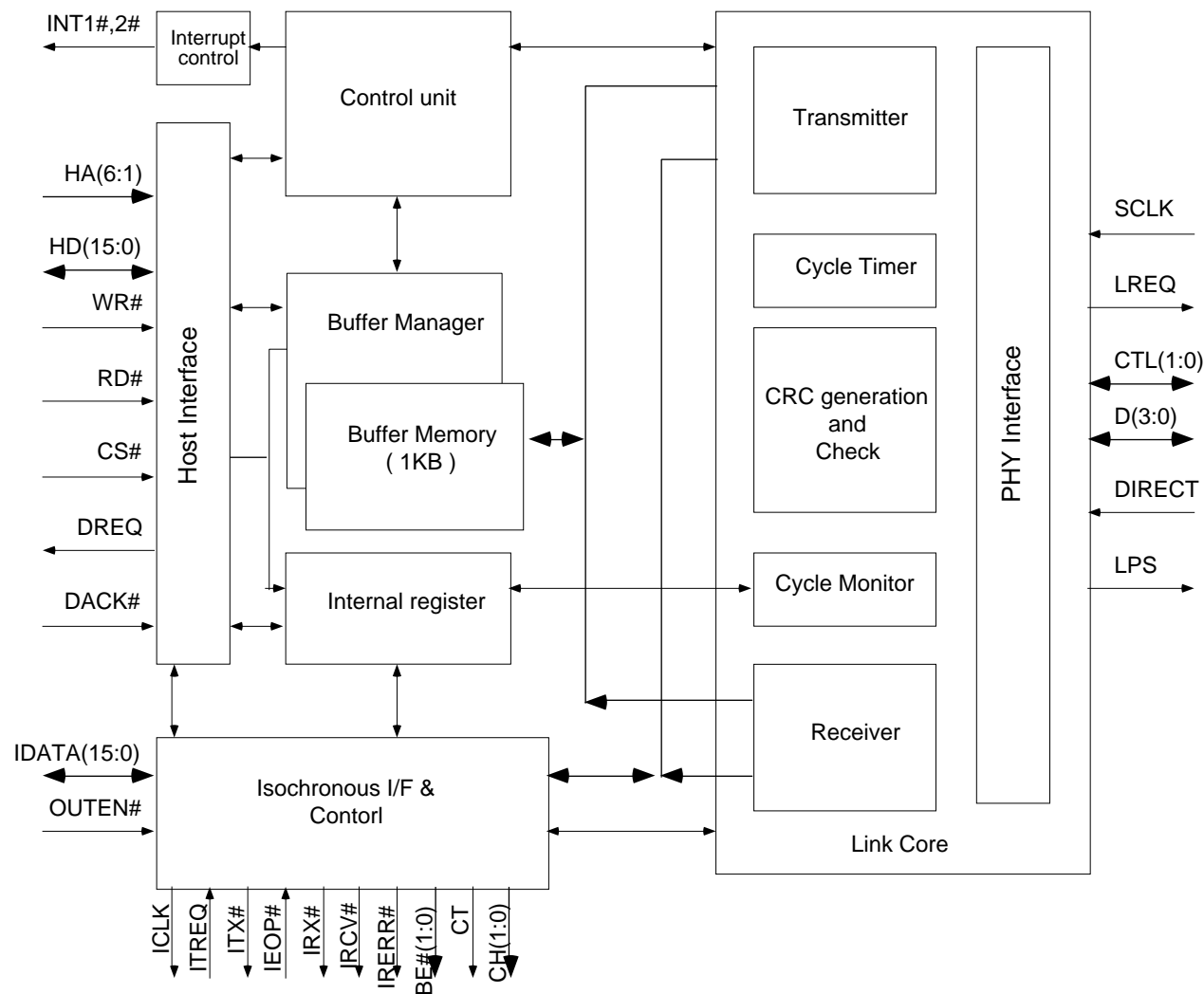


Figure 1-3-1 Block Diagram of MD8413

1-4 Outline Functions

1-4-1 Host Interface

The host interface consists of an asynchronous bus with a 16-bit width like the SRAM. Since DMA control functions are accommodated inside, the DREQ signal can be produced according to the status of buffer, in order to realize high-speed data transfer. Data access to the MD8413 is made in the Big Indian mode.

All registers can be directly accessed from the host. Inner buffer selection is performed by DMA transfer, and it is possible to gain access to the selected buffer.

1-4-2 PHY Interface

An interface is available, which enables direct connection with the PHY chip to process a physical layer according to IEEE 1394. Either 100Mbps or 200Mbps is acceptable for the PHY chip to be connected.

In the IEEE1394 Draft, the connection mode for the PHY and LINK chips is classified to the following two kinds:

- ☞ DC connection
- ☞ AC connection

This IC supports both kinds of connections.

1-4-3 Transmitter

The transmitter reads out data from the MD8413's internal asynchronous transmission buffer or the isochronous transmission data bus, and performs formatting into each packet format defined in IEEE 1394. The resultant packet is sent to the PHY interface. When the CycleMaster bit is "1" and the node employing the MD8413 is a root, a cycle start packet is also sent out to indicate the head of the isochronous cycle.

1-4-4 Receiver

The receiver receives a packet from the PHY interface and identifies if this packet is the one to be accepted by the MD8413 node. If it has been identified as an asynchronous packet, judgment is made with the node address of the MD8413. If it is an isochronous packet, judgment is made with the preset channel number. If it is a packet headed to this node, it is written in the asynchronous reception buffer and data output is transferred to the isochronous data bus. In the case of broadcast packet and snoop mode, no judgment is made and data are written in the respective buffers, transferring output to the data bus.

1-4-5 Built-in Buffer

The MD8413 has a built-in buffer with a capacity of 276 X 32 (bits) configuration for 1K-byte + 20 quadlets in total, to be used for asynchronous transmission and reception. This is a temporary buffer intended for the data-rate absorption between the transmitter and the host bus. The host performs data access to this buffer. The host splits this buffer in advance for asynchronous transmission and reception. Designation of each buffer size is set at the register. The status information concerned with the grade of vacancy and congestion in the buffer can be picked up by the host in the split unit.

1-4-6 Isochronous Transfer Function

The MD8413 has an isochronous function. Since a cycle timer is incorporated, a cycle start packet can be transmitted every 125μsec when the node employing the MD8413 is the CycleMaster. This cycle is produced from the 49.152MHz clock entered from the PHY chip and the trigger is an 8kHz signal entered from the CYCLEIN pin.

If the CycleMaster is not used, synchronism with the CycleMaster is established while making compensation for the cycle timer inside the MD8413 using the value in the packet, each time a cycle start packet is received from another CycleMaster node.

The MD8413 has two types of isochronous modes. HOST is a mode used to gain access to the host in a packet image, and the other is a mode for host access in an image of data stream. (Details to be related later)

The user determines the mode according to the nature of data source to be handled in isochronous transfer mode. For isochronous packet access with the outside, synchronous transfer is effected using an exclusive isochronous data bus. In this case, data control with the outside is effected by the MD8413 that functions as the master.

2 Terminal Descriptions

2-1 Functional Descriptions of Terminals

Signal	Type	Pin	No. of Pin	Contents															
PHY Interface																			
SCLK	I	69	1	Master clock: A 49.152MHz clock supplied from the PHY chip. The MD8413 uses this clock signal as a master clock. Usually connected to this signal pin of the PHY chip.															
LREQ	O	71	1	Link request : The MD8413 uses this signal when requesting register access in the PHY chip and the use of a serial bus. Usually connected to this signal pin of the PHY chip.															
CTL(0:1)	I/O	66,67	2	PHY-LINK control : An interface control signal exchanged with the PHY chip. Usually connected to this signal pin of the PHY chip.															
D(0:3)	I/O	61,62 64,65	4	PHY-LINK data bus : A data bus for data transmission / reception with the PHY chip. D (0:1) is used for packet reception at 100Mbps, and (0:3) is used for packet reception at 200Mbps.															
DIRECT	I	73	1	PHY I / F direct select signal : A changeover signal used to select direct or isolation connection of I / F with PHY. 0 : Isolation connection 1 : Direct connection															
LPS	O	72	1	Link status : An LPS signal to PHY. Output in the following combination available by register setting <table><tr><th>DIRECT input</th><th>LPS On bit</th><th>LPS output</th></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>Clock output of about 2MHz</td></tr></table>	DIRECT input	LPS On bit	LPS output	1	0	0	1	1	1	0	0	0	0	1	Clock output of about 2MHz
DIRECT input	LPS On bit	LPS output																	
1	0	0																	
1	1	1																	
0	0	0																	
0	1	Clock output of about 2MHz																	
Host Interface																			
HA(6:1)	I	10,11,12 13,14,15	6	Host address : Host address for register selection.															
HD(15:0)	I/O	82,83,84 85,87,88 89,90,92 93,94,95 97,98,99 100	16	Host data bus: Data bus for register and data access.															
WR#	I	7	1	Write enable : A write signal for the host data bus.															
RD#	I	8	1	Read enable : A read signal for the host data bus.															
CS#	I	6	1	Chip select : A chip select signal for the host data bus.															
DREQ	O	3	1	Data request : A request signal for DMA transfer. Valid only for asynchronous packet and data transfer.															
DACK#	I	5	1	Data acknowledge : An acknowledge signal for DMA transfer. only for asynchronous packet and data transfer.															
INT1#	O	1	1	Interrupt signal 1 : An interrupt signal to be sent to the host. This signal is asserted when a factor arises in the interrupt register. This factor is selected by register setting.															
INT2#	O	2	1	Interrupt signal 2 : An interrupt signal to be sent to the host. This signal is asserted when a factor arises in the interrupt register. This factor is selected by register setting.															

Table 2-1 MD8413 Terminals (1)

Signal	Type	Pin	No. of Pin	Contents
Isochronous Bus Interface				
ICLK	O	29	1	Isochronous bus master clock : A master clock for each signal of isochronous interface, to be output from the MD8413. This is a 24.576MHz output necessary for counting outside cycle timer.
ITREQ#	I	52	1	Isochronous send request : To be asserted when requesting isochronous packet transmission from the outside. This signal is kept asserted while multiple packets are transmitted for some isochronous cycle. Once deasserted, further packets are identified as those for another send request from the next cycle.
ITX#	O	50	1	Isochronous send data enable : when a send request arises, the MD8413 uses this signal for data request from the outside. The outside is required to be synchronized with this signal when handling data.
IEOP#	I	51	1	Isochronous send packet last data signal : With the last data (16-bit) of a packet during transmission, this signal is asserted from the outside synchronized with ITX#. The MD8413 knows the last data of each packet with this signal.
IRX#	O	27	1	Isochronous receive data enable : when a receive packet comes from PHY, the MD8413 sends out a packet data output to the outside, synchronized with this signal.
IRCV#	O	26	1	Isochronous packet receive enable : This signal shows that there is a receive packet output on the IDATA bus. In other words, the direction of IDATA bothway bus is indicated.
IRERR#	O	25	1	Isochronous packet error flag : To be asserted in the case of a CRC error in the received isochronous packet or data error.
IDATA(15:0)	I/O	31,32,33 34,35,37 38,39,40 42,43,44 45,47,48,49	16	Isochronous data bus : An exclusive bus for isochronous data access. The cycle timer value in the cycle start packet is also output from this bus.
CH(1:0)	O	17,18	2	Isochronous receive packet channel status : During presentation of an isochronous receive packet, a channel identification number or that packet is output.
CT	O	53	1	Cycle timer enable : When a cycle start packet is transmitted for root or received for non - root, this signal is used to indicate that cycle time data in the packet only are output on the IDATA bus.
BE#(1:0)	O	19,20	2	Byte enable : Indicates that an effective data output is available for isochronous reception of the respective upper / lower 8 - bit of the IDATA bus. BE# (1) denotes IDATA (15:8), and BE# (0) IDATA (7:0).
OUTEN#	I	28	1	ISO bus enable signal : During data reception, the IDATA bus assumes the output condition when this signal is enabled and IRCV# is asserted.
SYNC (1..0)	O	22,23	2	The following codes are output when there is coincidence with the sync bit preset value in the received isochronous packet Coincidence with StopSync : 10b Coincidence with StartSync : 01b Between Start and Stop: 11b Other cases : 00b
BUSRST	O	24	1	In case Bus Reset occurs, a one - pulse output of 24.576MHz is generated.
ICS	O	54	1	This is a timing output signal for isochronous CycleStart Packet transmission / reception.

Table 2-2 MD8413 terminals (2)

Signal	Type	Pin	No. of Pin	Contents
Others				
CYCLEIN	I	59	1	Isochronous cycle input : An external clock for counting the internal cycle timer in 8KHz unit. When CycleSource bit is " 1 " in the control register, this clock becomes valid.
CYCLEOUT	O	58	1	Isochronous cycle output : A cycle clock output generated by counting the internal cycle timer of the MD8413.
ITSYNC	I	74	1	Sync control signal : A sync field setting control signal in the header, used during auto - mode transmission.
ASYNCF LG	O	57	1	Asynchronous flag : This signal is asserted when an asynchronous packet is transmitted to PHY or received from it. It is valid as a trigger signal for packet exchange.
ISOCFLG	O	56	1	Isochronous flag : This signal is asserted when an isochronous packet is transmitted to PHY or received from it. It is valid as a trigger signal for packet exchange.
RESET#	I	75	1	Reset : A system reset signal of the MD8413.
GPIO(3:0)	I/O	77,78,79 80	4	General purpose application I/O
Test Terminals				
TEST	I	76	1	A signal for testing.
Power supply				
VDD	I	9,21,36 46,60,70 86,96	8	3.3V power supply.
VSS	I	4,16,30 41,55,63 68,81,91	9	GND

Table 2-3 MD8413 terminals (3)

3 Control Register

3-2 Register Contents

3-2-1-1 Version Register

Address 00h

Initial value 0002h

This register defines the version number of the MD8413. It is useful for future IEEE 1394-LINK chip control with software.

7	6	5	4	3	2	1	0
Version							
15	14	13	12	11	10	9	8
Version							

Bit 15~0 version : Version number of IC chip (R - initial value : 0002h)
The MD8413 version number is indicated. The MD8413 always reads out “0002h”.

3-2-1-2 Revision Register

Address 02h

Initial value 0000h

This register defines the revision number of the MD8413. The value starts with 0, and is increased each time revision is made. It is useful for future IEEE 1394-LINK chip control with software.

7	6	5	4	3	2	1	0
Revision							
15	14	13	12	11	10	9	8
Revision							

Bit 15~0 Revision : Revision number of IC chip (R - initial value : 0000h)
The MD8413 revision number is indicated. The value starts with 0, and is increased each time revision is made.

3-2-2-1 Control Register-H

Address 04h

Initial value 1803h

This register is used to set up configuration, enable, etc., of each operation for the MD8413. Generally, the MD8413 configuration is determined in advance by making this register's setting, after setting up the LinkOn bit shortly after the energization of the power supply.

7	6	5	4	3	2	1	0
ITZERO		IsoMode			CycleSource	CycleMaster	CycleTimerEn
15	14	13	12	11	10	9	8
DackHigh	DreqLow		ARFBusReset	CSEn	IACTIVE	AACTIVE	LPSON

Bit 0 **CycleTimerEn** : Cycle Timer Enable bit (RW - initial value : 1b)

- 0 = Cycle timer disabled
- 1 = Cycle timer enabled

Setting is made to determine whether the cycle timer in the MD8413 is enabled or not..

Bit 1 **CycleMaster** : Cycle Master bit (RW - initial value : 1b)

- 0 = The cycle timer is controlled by receiving a cycle start packet from a node of another root.
Setting is made at "0" or the node with which an ordinary root cannot be obtained.
- 1 = When this bit is "1", a cycle start packet is produced each time the MD8413 cycle timer is carried.

Even though this bit has been set, no cycle start packet will be generated if the root bit is "0".

Bit 2 **CycleSource** : Cycle Sourcer bit (RW - initial value : 0b)

- 0 = The master clock of 49.152MHz fed from the PHY chip is frequency-divided into 24.576MHz, at which the cycle timer is counted to control the isochronous cycle.
- 1 = With a rising signal entered from the CYCLEIN terminal, the cycle timer is updated to control the isochronous cycle.

The update origin is set up for the internal cycle timer where isochronous time control is effected.

Bit 5~4 **IsoMode** : Isochronous Mode bit (RW - initial value : 00b)

IsoMode

- 0 0 Iso exchange mode in normal mode. A maximum of 4 channels can be received.
- 0 1 Iso exchange mode in normal mode. For reception, Iso snoop reception is effected.
- 1 0 Iso exchange mode in auto mode. A maximum of 4 channels can be received.
- 1 1 Iso exchange mode in auto mode. For reception, Iso snoop reception is effected.

When LSB setting of IsoMode is "0" during reception, packet reception for a maximum of 4 channels is effected with the receive channel setting register, where coincidence is perceived with the setting value. When it is "1" similarly, all Iso packets carried on the bus are received, irrespective of the setting register value. They are then output to the IDATA bus. If channels more than 4 are received,

setting is made for these.

Bit 7 **ITZERO** :Isochronous ZeroLength Packet bit (RW - initial value : 0b)

- 0 = During isochronous transmission in auto mode, no transmission is effected for a cycle that has no send request.
- 1 = During isochronous transmission in auto mode, a packet of Length=0 is transmitted for a cycle that has no send request.

If there is no data to be sent for a cycle during isochronous transmission in the auto mode, this bit is used to decide whether packet transmission is effected for a cycle where no ITREQ# has been asserted, or whether auto-transmission of Length=0 packet is transmitted.

Bit 8 **LPSOn** : Ink power status on bit (RW - initial value : 0b)

This bit is used to control the LPS signal supplied to the PHY chip. According to the status of the DIRECT terminal, contents of output are different.

DIRECT terminal	LPSOn bit	LPS terminal output
High	0	Low
High	1	High
Low	0	Low
Low	1	Clock of about 1MHz

Bit 9 **AACTIVE** : ASYNCFLG terminal bit (RW - initial value : 0b)

- 0 = The assert condition for the ASYNCFLG terminal is made valid during transmission and at the time of reception of an Async packet at this node.
- 1 = The assert condition for the ASYNCFLG terminal is made valid during transmission and at the time of reception of all Async packets.

This bit is used to determine the assert condition for the ASYNCFLG terminal. It is effective as a trigger signal for asynchronous packet transmission/reception.

Bit 10 **IACTIVE** : ISOFLG terminal bit (RW - initial value : 0b)

- 0 = The assert condition for the ISOFLG terminal is made valid during transmission and at the time of reception of a channel set in the isochronous receive register.
- 1 = The assert condition for the ISOFLG terminal is made valid during transmission and at the time of reception of all isochronous packets.

This bit is used to determine the assert condition for the ISOFLG terminal. It is effective as a trigger signal for isochronous packet transmission/reception.

Bit 11 **CSEn** : Cycle Start Packet output enable bit (RW - initial value : 1b)

- 0 = Cycle time data in the cycle start packet are not output to the IDATA bus.
- 1 = Cycle time data in the cycle start packet are output to the IDATA bus.

When a cycle start packet is received from a serial bus, the MD8413 sends out only cycle time data of that packet to the IDATA bus. This bit is used to set up data output enable.

Bit 12 ARFBusReset : ARF BusReser mode bit (RW - initial value : 1b)

- 0 = Contents of the ARF buffer are retained after bus reset.
- 1 = Contents of the ARF buffer are abandoned after bus reset.

If the RxSelfID bit has been set after bus reset, the MD8413 saves the SelfID packet in the ARF buffer. If this bit is already set at that time, data having been saved shortly before bus reset are abandoned, in order to save the SelfID packet assuredly.

Bit 14 DreqLow : DREQ Low active bit (RW - initial value : 0b)

- 0 = The DREQ terminal is set at high active.
- 1 = The DREQ terminal is set at low active.

The MD8413 selects a logic of the DREQ terminal in active state.

Bit 15 DackHigh : DACK High active bit (RW - initial value : 0b)

- 0 = The DACK terminal is set at high active.
- 1 = The DACK terminal is set at low active.

The MD8413 selects a logic of the DACK terminal in active state.

3-2-2-2 Control Register-L

Address 06h

Initial value 0001h

This register is used to set up configuration, enable, etc., of each operation for the MD8413. Generally, the MD8413 configuration is determined in advance by making this register's setting, after setting up the LinkOn bit shortly after the energization of the power supply.

7	6	5	4	3	2	1	0
						ReceiveEn	TransmitEn
15	14	13	12	11	10	9	8

Bit 0 TransmitEn : Transmitter Enable bit (RW - initial value : 1b)

- 0 = Transmitter disabled
- 1 = Transmitter enabled

Setting is made to determine whether the transmitter in the MD8413 is enabled or not. When enabled, transmission is effected for the following:

- ☛ Asynchronous packet
- ☛ Cycle start packet when the CycleMaster bit is enabled

- ✎ Isochronous packet upon cycle start

When disabled, no transmission is effected.

Bit 1 **ReceiveEn** : Receiver Enable bit (RW - initial value : 0b)

0 = Receiver disabled

1 = Receiver enabled

Setting is made to determine whether the receiver in the MD8413 is enabled or not. When enabled, reception is effected for the following:

- ✎ Asynchronous packet addressed from another node to this node
- ✎ Isochronous packet of the designated channel
- ✎ Reception in snoop mode

When disabled, only reception is effected for the following:

- ✎ SelfID packet

3-2-3-1 Node Identification Register-H

Address 08h

Initial value 0000h

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
IDValid	root						

Bit 14 **root** : root bit (R - initial value : 00b)

0 = Connected Phy being not of root

1 = Connected Phy being of root

When bus reset occurs, setting is generally made by examining whether the automatically connected Rhy is of a root. At that time, accomplishment of setting can be known by the occurrence of PhyRegRcvd interruption. Shortly after the energization of the power supply, this root bit is set up because the host begins to read out Reg0 of Phy.

Bit 15 **IDValid** : ID Valid bit (RW - initial value : 00b)

0 = Only the packet is received, for which the BusNumber value is addressed at "3FFH" and the NodeNumber value is addressed at "3FH". All other packets are rejected.

1 = Only packet is received, which has been set in the above-mentioned register under the conditions shown below, and addressed in the IEEE1212 address space. A broadcast packet is also received.

☛ Coincidence with the register set value for both BusNumber and NodeNumber

☛ Coincidence of BusNumber with the register set value, and NodeNumber value being "3FH"

☛ BusNumber value being "3FH" and coincidence of NodeNumber with the register set value

☛ BusNumber value being "3FH" and NodeNumber value being "3FH"

When the bus reset state is assumed, this register is automatically cleared to "0".

3-2-3-2 Node Identification Register-H

Address 0Ah

Initial value FFFFh

7	6	5	4	3	2	1	0
BusNumber-L		NodeNumber					
15	14	13	12	11	10	9	8
BusNumber-H							

Bit 5~0 NodeNumber : Node Number bit (RW - initial value : 3Fh)

For this value, a 6-bit node number defined in the IEEE1212 space is set up. During transmission, this value is used in the header source area of the IEEE 1394 packet format. This value is received, provided that it coincides with the destination node number of the receiving packet. Otherwise, it is rejected.

Generally, the host sends out a NodeID read-out request to the Phy after completion of the self-identification phase preceded by bus reset. The obtained result must be set in this bit.

Bit 15 ~6 BusNumber : Bus Number bit (RW - initial value : 3FFh)

A 10-bit bus number defined in the IEEE 1212 space is set up for this value. During transmission, this value is used in the header source area of the IEEE 1394 packet format. This value is received, provided that it coincides with the destination bus number of the receiving packet. Otherwise, it is rejected.

3-2-4 Reset Register

Address 0Ch

Initial value 0000h

7	6	5	4	3	2	1	0
			ResetDMA	ResetLink	ResetTx	ResetARF	ResetATF
15	14	13	12	11	10	9	8

Bit 0 **ResetATF** : Reset ATF bit (RW - initial value : 0b)

0 = Normal status

1 = Initialization of buffer area for asynchronous transmission

Only the buffer area for asynchronous transmission is restored to its initial status. At that time, all data staying in this area are lost. All buffer status flags are also restored to their initial status.

When “1” is set, this bit is automatically set at “0” upon completion of initialize operation inside.

Bit 1 **ResetARF** : Reset ARF bit (RW - initial value : 0b)

0 = Normal status

1 = Initialization of buffer area for asynchronous reception

Only the buffer area for asynchronous reception is restored to its initial status. At that time, all data staying in this area are lost. All buffer status flags are also restored to their initial status.

When “1” is set, this bit is automatically set at “0” upon completion of initialize operation inside.

Bit 2 **ResetTx** : Reset Transmitter bit (RW - initial value : 0b)

0 = Normal status

1 = Transmitter reset

A transmission-enabled condition is set, by resetting the transmitter. If a packet is in the middle of transmission, such transmission operation is aborted. When “1” is set, this bit is automatically set at “0” upon completion of initial status inside.

Bit 3 **ResetLink** : Reset Link Core bit (RW - initial value : 0b)

0 = Normal status

1 = Link core reset

The link core is reset. All operation is aborted. When “1” is set, this bit is automatically set at “0” upon completion of initial status inside.

At that time, following registers are not initialized.

✎ CycleTimer Register

✎ BusTimer Register

Following bits of registers are initialized.

✎ RetryTimeMax

✎ RetryCount

✎ AckStatus

⚡ ATAck

Bit 4 **ResetDMA** : Reset DMA bit (RW - initial value : 0b)

- 0 = Normal status
- 1 = DMA control reset

DMA control is reset to set up the DMA-transfer-enabled condition. DMA is required to complete data transfer in the Quadlet unit. The DMA transfer pointer in this Quadlet unit is cleared with this bit, and a pointer is set in the front position in the Quadlet unit. When “1” is set, this bit is automatically set at “0” upon completion of initial status inside.

Address 0Eh

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-5 Asynchronous Buffer Size Set Register

Address 10h

Initial value 0007h

In this register, an allocation size is specified to allocate an asynchronous receive area in the buffer having a capacity of internal 1KB (for payload) + 80B (for header, etc.). Setting is made according to the size of the receiving-packet payload. The MD8413 secure a buffer size for the required size plus others (header, Speed, AckSent). For transmit buffer allocation, the capacity remaining after receive allocation is assigned.

7	6	5	4	3	2	1	0
					ARxBufferSize		
15	14	13	12	11	10	9	8

Bit 2~0 ARxBufferSize : Asynchronous Receive Buffer Size bit (RW - initial value : 0007h)

The buffer size for asynchronous reception is chosen from the following:

ARxBufferSize field	Receive packet size (byte)	Send packet size (byte)
000	44	1060
001	48	1056
010	56	1048
011	72	1032
100	104	1000
101	168	936
110	296	808
111	552	552

Address 12h

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-6 Packet Control Register

Address 14h

Initial value 0000h

7	6	5	4	3	2	1	0
		RxSelfID	EnSnoop				
15	14	13	12	11	10	9	8
			WritePending		BusyCtrl		

Bit 4 EnSnoop : EnableSnoop bit (RW - initial value : 0b)

- 0 = Generally, only packets mapped in this node address are received.
- 1 = Snoop mode is assumed.

This bit is used to set up the snoop mode for receiving all packets entered from Phy. The Ack code is not returned when an asynchronous packet is received. All packets received in this mode are output from the IDATA bus.

Bit 5 RxSelfID : Recive Self ID bit (RW - initial value : 1b)

- 0 = No SelfID packets are entered in the buffer.
- 1 = SelfID packets are entered in the buffer.

This bit is used to set up whether the Self ID packets, received during the Self ID phase after bus reset, should be inserted in the buffer area for receive Async.

Bit 10 ~8 BusyCtrl : Busy Control bit (RW - initial value : 000b)

- 000= Only if there is no vacant area for one packet to be received at the internal Async receive buffer, a busy acknowledge signal is returned according to the dual phase retry protocol.
- 001= Only if there is no vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyA status.
- 010= Only if there is no vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyB status.
- 011= Only if there is no vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyX status.
- 100= Regardless of whether there is a vacant area for one packet to be received at the internal Async receive buffer, a busy acknowledge signal is returned according to the dual phase retry protocol.
- 101= Regardless of whether there is a vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyA status for all packets received.
- 110= Regardless of whether there is a vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyB status for all packets received.
- 111= Regardless of whether there is a vacant area for one packet to be received at the internal Async receive buffer, an acknowledge signal is returned in the BusyX status for all packets received.

When the node for MD8413 is in-bound, and an acknowledge signal is returned in the busy status to

the packet that has been sent from the out-bound node of the MD8413, contents of that status are set in this register.

Bit 12 WritePending : Write Request Ack-Pending bit (RW - initial value : 1b)

- 0 = An Ack-Complete signal is returned when normal reception is accomplished with the Ack code for Write Request Packet.
- 1 = An Ack-Pending signal is returned when normal reception is accomplished with the Ack code for Write Request Packet.

Generally, when Write Request Packet is received and normal reception is accomplished, the Ack code functions to return ACK-Complete. In case of failure in normal reception due to lack of buffer capacity or the like, ACK-Busy is returned. When normal reception is effected by setting up "1" for this bit, the Ack code returns ACK-Pending. In other words, Split Transaction of Write Request is effected. Upon completion of Write Request processing, the host must send out a Write Response packet. The table below shows types of return Ack codes for the respective packets. Each return Ack packet is indicated by a circle (O).

Packet	WritePending = '0b'			WritePending = '1b'		
	ack_complete	ack_pending	ack_busy	ack_complete	ack_pending	ack_busy
Write Request	O	-	O	-	O	O
Read Request	-	O	O	-	O	O
Write Response	O	-	O	O	-	O
Read Response	O	-	O	O	-	O
Lock Request	-	O	O	-	O	O
Lock Response	O	-	O	O	-	O

Address 16h

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-7-1 Diagnostic Status Register-H

Address 18h

Initial value 0000h (Read only register)

Various status information can be picked up from this register.

7	6	5	4	3	2	1	0
					BusyState		
15	14	13	12	11	10	9	8
RetryTimeMax		AckStatus		ATAck			

Bit 2 BusyState : Busy State bit (R - initial value : 0b)

0 = Acknowledge is returned with BusyA.

1 = Acknowledge is returned with BusyB.

When this node issues Busy Acknowledge at the next opportunity, this bit is used to indicate the type of that Acknowledge.

Bit 11~8 ATAck : AT Ack bit (R - initial value : 0000b)

0000 = No Ack

0001 = ack_complete

0010 = ack_pending

0011 = reserve

0100 = ack_busy_X

0101 = ack_busy_A

0110 = ack_busy_B

0111

~1100= reserve

1101 = ack_data_error

1110 = ack_type_error

1111 = reservation

During transmission, contents of Acknowledge (Ack code), returned from the destination node to the packet that is sent from the transmitter, are reflected in this register. The reflection timing is defined when the busy flag is negated, showing that the sending packet in the Asynchronous buffer is being processed. This value is retained until this busy status is negated for the next packet transmission.

Bit 13~12 AckStatus : Ack Status bit (R - initial value : 00b)

00 = Normal reception

01 = Parity error

10 = Packet lost (No Ack packet sent within the specified time)

11 = reservation

These bits are used to indicate the status of Acknowledge Packet returned from the destination node for the transmitted asynchronous packet.

Bit 15 RetryTimeMax : Retry Time Max bit (R - initial value : 0b)

0 = Normal

1 = Max. number of retries

The condition is indicated when a certain retry phase is started and a setting retry is effected within the specified time, also showing the maximum number of retries counted within the ATRetry register. The ATAck bit is used to identify whether a retry phase has been finished or has resulted in a busy state.

This value is retained until the next packet transmission is effected.

3-2-7-2 Diagnostic Status Register-L

Address 1Ah

Initial value 0000h (Read only register)

Various status information can be picked up from this register.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
							ATBusy

Bit 8 ATBusy : AT Busy bit (R - initial value : 0b)

0 = ndicates that ATGo issue is enabled.

1 = Indicates that ATGo issue is disabled. Processing of a packet is indicated by ATGo issued shortly before the present time.

During asynchronous transmission, this bit is asserted with ATGo issued, and negated when its acknowledge return is set in the ATAck register. While this bit is being asserted, the host cannot issue the next ATG0. Even when it is issued, it is disregarded. When certain packet transmission is put into retry operation, this bit is not negated until completion of the said retry.

3-2-8 Phy Control Register

Address 1Ch

Initial value 0000h

This register is used to gain access to a register in the PHY chip. When reading a register, its register address is set in the RegAddr register and the RdReg bit is made active. With the RdReg bit being active, a read request for the register of that address is forwarded to PHY and the RdReg bit is cleared. Contents of the register for the address from PHY are entered in the RegData register. Also for the write request toward the PHY register, data in the Reg Data register are written with the WrReg bit used as a trigger according to the PHY address set in the RegAddr register.

7	6	5	4	3	2	1	0
RegData							
15	14	13	12	11	10	9	8
	RegRcvd	RdReg	WrReg	RegAddr			

Bit 7~0 RegData : Register Data bit (RW - initial value : 00h)

Data to be transferred to PHY are stored, with a write request. With a read request, data transferred from PHY are also stored. When reading out the contents of this register, contents of RegDta are read out, the data transferred from PHY according to the read request placed shortly before. In other words, it is impossible to read out the data, which have been written from the host, directly from this register. To realize reading out, it is necessary to send a read request to PHY .

Bit 11~8 RegAddr : Register Address bit (RW - initial value : 00h)

The address value of the accessing PHY register is set up.

Bit 12 WrReg : Write Register bit (RW - initial value : 0b)

0 = Normal status

1 = Write request issued

A write request toward the PHY register is issued. After execution of this write request, this bit is cleared.

Bit 13 RdReg : Read Register bit (RW - initial value : 0b)

0 = Normal status

1 = Read request issued

A read request toward the PHY register is issued. After execution of this read request, this bit is cleared.

Bit 14 RegRcvd : Register Data Received bit (R - initial value : 0b)

0 = Normal status

1 = Indicates that the data from PHY have been saved in RegData after the issuing of a read request.

After a read request toward the PHY register has been issued, "1" is set up upon storage of the data

from PHY in RegData. Once this register is read out thereafter, it is cleared to "0".

Address 1Eh

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-9-1 ATRetries Register

Address 20h

Initial value 0000h

There are provisions of functions to perform automatic retry when the MD8413 node performs asynchronous packet transmission and a busy acknowledge signal is returned from the related destination node. The number of retries and time are set in this register. Once entering the retry phase, a busy flag at the ATGo register is not negated and next packet transmission is impossible to carry out, until an acknowledge signal other than busy is returned from the destination node or the preset retry number and time have expired. It is, however, possible to perform forced ending of the retry phase using the RetryStop bit.

7	6	5	4	3	2	1	0
RetryCount				MaxRetryCountLimit			
15	14	13	12	11	10	9	8
							RetryStop

Bit 3~0 MaxRetryCountLimit : Maximum Retry Count Limit bit (RW - initial value : 0h)

This register is used to set up how many times retries should be repeated at the maximum, for Busy Acknowledge from the destination node. The retry phase for this count number is for the single phase. If the retry phase is not finished within this set value, a retry time-out status flag is stood in the ATAck register to complete the retry phase to be executed by the MD8413. Since then, packet data in the ATF buffer are flashed. The maximum setting value is 15 (times). When "0000" is set, the MD8413 automatically stops processing for the single retry phase. In such a case, packet data are flashed for Busy Acknowledge. If an error acknowledge signal is returned during the retry phase, this retry is interrupted on the way, the buffer is flashed, and a flag (AckErr) is provided to complete all processing.

Bit 7~4 RetryCount : Retry Count bit (R - initial value : 0h)

While the MD8413 is performing a single retry, the number of retries at present is indicated.

Bit 8 RetryStop : Retry Forced Ending bit (RW - initial value : 0b)

When the MD8413 automatically enters the retry phase, this bit may be used to perform forced ending of the retry before attaining the limit value yet. When “1” is set, this bit is automatically cleared upon completion of the retry phase.

0 : Normal status

1 : Forced ending

Address 22h

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-9-2 ATRetries Register

Address 24h

Initial value 00C8h

There are provisions of functions to perform automatic retry when the MD8413 node performs asynchronous packet transmission and a busy acknowledge signal is returned from the related destination node. The number of retries and time are set in this register. Once entering the retry phase, a busy flag at the ATGo register is not negated and next packet transmission is impossible to carry out, until an acknowledge signal other than busy is returned from the destination node or the preset retry number and time have expired. It is, however, possible to perform forced ending of the retry phase using the RetryStop bit.

This register is used to set up how long this retry should be performed at the maximum, for Busy Acknowledge from the destination node. The retry phase for this register value is for the dual phase. If the retry phase is not finished within this set time, a retry time-out status flag is stood in the ATAck register to complete the retry phase to be executed by the MD8413. Since then, packet data in the ATF buffer are flashed. The maximum setting value is 8 seconds. When “0” is set in this field, the MD8413 automatically stops processing for the dual retry phase. In such a case, packet data are flashed for Busy Acknowledge. If an error acknowledge code is returned during the retry phase, this retry is suspended at that time point, the buffer is flashed, and a flag (AckErr) is provided to complete all processing.

7	6	5	4	3	2	1	0
MaxRetryCycle Limit							
15	14	13	12	11	10	9	8
MaxRetrySecond Limit				MaxRetryCycle Limit			

Bit 12~0 MaxRetryCycleLimit : Maximum Retry Cycle Limit bit (RW - initial value : 00C8h)

This area is for the designated value in Cycle unit. It is valid within the range of 0~7999.

Bit 15~13 MaxRetrySecondLimit : Maximum Retry **Second** Limit bit (RW - initial value : 0000h)

This area is for the designated value in Second unit.

3-2-9-3 ATRetries Register

Address 26h

Initial value 0000h

7	6	5	4	3	2	1	0
RetryCycle Limit							
15	14	13	12	11	10	9	8
RetrySecond Limit				RetryCycle Limit			

Bit 12~0 RetryCycleLimit : Retry Cycle Limit bit (R - initial value : 0000h)

While the MD8413 is in the middle of a dual retry, the present retry lapse time is shown in **Cycle** unit.

Bit 15~13 RetrySecond/Limit : Retry Second Limit bit (R - initial value : 0000h)

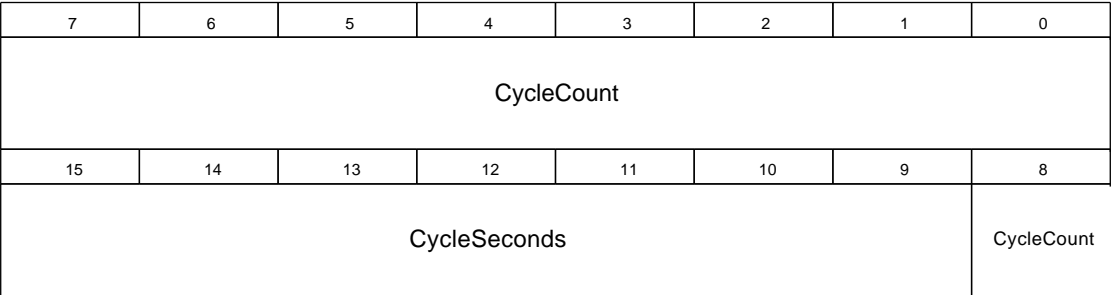
While the MD8413 is in the middle of a dual retry, the present retry lapse time is shown in **Second** unit.

3-2-10-1 Cycle Timer Register-H

Address 28h
Initial value 0000h

The present cycle timer value is indicated. This register is split into three regions as shown below. When the node employing the MD8413 is for the CycleMaster, this register value is inserted during cycle start packet transmission. Otherwise, the cycle timer value in the received cycle start packet is loaded in this register to update the cycle timer.

The host is allowed to load any cycle timer value in this register. The load timing is defined when Cycle Timer Register-L has been written.



Bit 8~0 CycleCount : Cycle Count bit (RW - initial value : 00h)

This area is counted up when the Cycle Field register is carried, in order to count isochronous cycles. Operation is maintained with Modulo8000.

Bit 15~9 CycleSeconds : Cycle Seconds bit (RW - initial value : 00h)

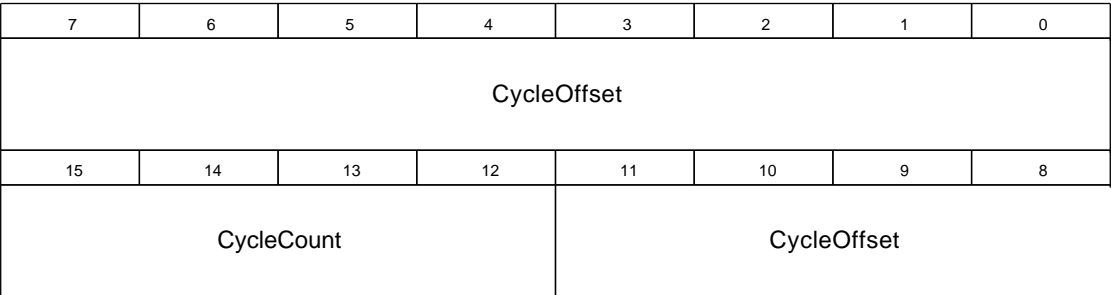
This area is counted up when the Cycle Count register is carried, in order to count seconds. Operation is maintained with Modulo128.

3-2-10-2 Cycle Timer Register-L

Address 2Ah
Initial value 0000h

The present cycle timer value is indicated. This register is split into three regions as shown below. When the node employing the MD8413 is for the CycleMaster, this register value is inserted during cycle start packet transmission. Otherwise, the cycle timer value in the received cycle start packet is loaded in this register to update the cycle timer.

The host is allowed to load any cycle timer value in this register. The load timing is defined when Cycle Timer Register-L has been written.



Bit 11~0 CycleOffset : Cycle Offset bit (RW : initial value : 00h)

This area is counted up with a 24.576MHz clock. Operation is maintained with Modulo3072.

Bit 15~24 CycleCount : Cycle Count bit (RW - initial value : 00h)

This area is counted up when the Cycle Field register is carried, in order to count isochronous cycles.
Operation is maintained with Modulo8000.

3-2-11-1 Bus Time Register-H

Address 2Ch
Initial value 0000h

This is a timer register used to count the bus time in 32-bit width. Each time the Cycle Count timer of the Cycle Time register is carried, counting is forwarded. This address is given by upper 16 bits on the Bus Time with a 32-bit width.

Used for the BUS_TIME register of the Serial-dependent registers specified by IEEE1212.

7	6	5	4	3	2	1	0
SecondCountHi							
15	14	13	12	11	10	9	8
SecondCountHi							

Bit 15~0 SecondCountHi : Bus Time H bit (RW - initial balue : 00h)

Upper 16 bits of the Bus Time register.

3-2-11-2 Bus Time Register-L

Address 2Eh
Initial value 0000h

This is a timer register used to count the bus time in 32-bit width. Each time the Cycle Count timer of the Cycle Time register is carried, counting is forwarded. This address is given by lower 16 bits on the Bus Time with a 32-bit width.

Used for the BUS_TIME register of the Serial-dependent registers specified by IEEE1212.

7	6	5	4	3	2	1	0
SecondCo untHi	SecondCountLo						
15	14	13	12	11	10	9	8
SecondCountHi							

Bit 6~0 SecondCountLo : Bus Time L bit (R - initial value : 00h)

Lower 7 bits of the Bus Time register. It coincides with the CycleTimeSecond value.

Bit 15~7 SecondCountHi : Bus Time H bit (RW - initial value : 00h)

Upper 9 bits of SecondCountHi.

3-2-12-1 Isochronous Transmit Configuration Register

Address 30h

Initial value 0000h

This register is used to set up how the MD8413 should handle a packet when the transmission mode is AUTO for IsoMode. The volume of data for one packet to be transferred with each isochronous cycle is defined with this register. In the iso-auto mode, it is only one channel that can be transmitted.

7	6	5	4	3	2	1	0
						Speed	
15	14	13	12	11	10	9	8
Tag		Channel					

Bit 1~0 **Speed** : Speed bit (RW - initial value : 0b)

0 = Transmission at 100Mbps

1 = Transmission at 200Mbps

In transmission mode, the transfer speed on the cable is set up.

Bit 13~8 **Channel** : Channel bit (RW - initial value : 00h)

A channel of a transmitting isochronous packet is designated. The channel number set up here is inserted in the packet header for transmission. The setting range is 0 to 63.

Bit 15~14 **Tag** : Tag bit (RW - initial value : 00h)

Tag of an isochronous packet is designated. The setting range is 0 to 3.

3-2-12-2 Isochronous Transmit Configuration Register

Address 32h

Initial value 0000h

This register is used to set up how the MD8413 should handle a packet when the transmission mode is AUTO for IsoMode. The volume of data for one packet to be transferred with each isochronous cycle is defined with this register. In the Iso-auto mode, it is only one channel that can be transmitted.

7	6	5	4	3	2	1	0
StopSync							SyncEn
15	14	13	12	11	10	9	8
Sync				StartSync			

Bit 0 SyncEn : Sync Enable bit (RW - initial value : 0b)

0 = Contents of the Sync register are reflected at any time in the Sync area of the packet header, regardless of the ITSYNC signal.

1 = Used to determine the Sync field value in the packet header transmitted according to the ITSYNC signal. Contents of StartSync are entered in the transmission packet shortly after ITSYNC active, and then those of StopSync are entered in the transmission packet shortly after ITSTART non-active. When ITSYNC is disabled, the following conditions are assumed according to the setting value of ITZERO:

 ITZERO=0 : No transmission is effected.

 ITZERO=1 : Sync field is entered at any time.

Bit 7~4 StopSync : Stop Sync bit (RW - initial value : 00h)

When the ITSTART terminal is made non-active with SyncEn="1b", this value is written in the Sync field of the packet shortly after that.

Bit 11~8 StartSync : Start Sync bit (RW - initial value : 00h)

When the ITSTART terminal is made active with SyncEn="1b", this value is written in the Sync field of the packet shortly after that.

Bit 15~12 Sync : Sync bit (RW - initial value : 00h)

With SyncEn="1b", this value is written in a packet other than the packets specified for the StartSync packet/StopSync packet at the ITSTART terminal.

3-2-12-3 Isochronous Transmit Configuration Register

Address 34h

Initial value 0000h

7	6	5	4	3	2	1	0
ITLength							
15	14	13	12	11	10	9	8
ITLength							

Bit15~0 ITLength : Isochronous Transmit Length bit (RW - initial value : 0h)

Length of the sending packet is set in this register. This value is used for the header block during transmission.

Address 36h

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-13-1 Isochronous Receive Configuration Register 1,2,3,4

Address 38h (1), 3Ch (2), 40h (3), 44h (4)
Initial value 0000h

In cases other than snoop reception of an isochronous packet, how the MD8413 should receive a packet of what kind is set in this register group. There are 4 channels that can receive this packet in a mode other than the snoop receive mode.
A maximum of 4 types of receive channel numbers preset here are output from the CH(1:0) terminal as the identification numbers specified below.

- Isochronous Receive Configuration 1 : CH(1:0) = "00"
- Isochronous Receive Configuration 2 : CH(1:0) = "01"
- Isochronous Receive Configuration 3 : CH(1:0) = "10"
- Isochronous Receive Configuration 4 : CH(1:0) = "11"

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
		Channel					

Bit 13~8 **Channel** : Channel bit (RW - initial value : 00h)
A receiving isochronous channel is set. The setting range is 0 to 63.

3-2-13-2 Isochronous Receive Configuration Register 1,2,3,4

Address 3Ah (1), 3Eh (2), 42h (3), 46h (4)
Initial value 0000h

In cases other than snoop reception of an isochronous packet, how the MD8413 should receive a packet of what kind is set in this register group. There are 4 channels that can receive this packet in a mode other than the snoop receive mode.

7	6	5	4	3	2	1	0
StopSync						IsoRxEn	SyncEn
15	14	13	12	11	10	9	8
				StartSync			

Bit 0 **SyncEn** : Sync Enable bit (RW - initial value : 0b)
0 = Packet reception is effected, irrespective of the contents of StartSync and StopSync.

1 = Packet reception is controlled, using the preset channel number, StartSync, and StopSync.

Bit 1 **IsoRxEn** : Isochronous Receive Enable bit (RW - initial value : 0b)

0 = Isochronous reception is disabled.

1 = Isochronous reception is enabled.

Setting is made to determine whether the Isochronous reception is effect or not.

Bit 7~4 **StopSync** : Stop Sync bit (RW - initial value : 00h)

When SyncEn=1, this bit and the Sync field value of the packet are used for receive control. Once packet reception is started with StartSync, and the Sync field of the packet with the preset channel number has received a packet coinciding with this register value, successive packet reception is stopped.

If receive operation is stopped with the IsoRxEn bit prior to receiving this value, further reception is not effected until another StartSync comes again.

Bit 11~8 **StartSync** : Start Sync bit (RW - initial value : 00h)

When SyncEn=1, this bit and the Sync field value of the packet are used for receive control. The Sync field of the packet with the preset channel number begins to perform reception, starting with the packet that has coincided with this register value.

3-2-14-1 ATF Data Register -H

Address 48h
Initial value 0000h

This is a register intended for asynchronous packet send data writing. Data of the upper 16 bits are written in the internal asynchronous transmit buffer. This writing must be done in the Quadlet unit, without fail.

7	6	5	4	3	2	1	0
ATFData-H							
15	14	13	12	11	10	9	8
ATFData-H							

3-2-14-2 ATF Data Register -L

Address 4Ah
Initial value 0000h

This is a register intended for asynchronous packet send data writing. Data of the lower 16 bits are written in the internal asynchronous transmit buffer. This writing must be done in the Quadlet unit, without fail. When these data are written here, they are joined with data of ATFData-H, and saved in the internal buffer as the Quadlet data.

7	6	5	4	3	2	1	0
ATFData-L							
15	14	13	12	11	10	9	8
ATFData-L							

3-2-15-1 ARF Data Register -H

Address 4Ch
Initial value 0000h

This is a register intended for asynchronous packet receive data reading. Data of the upper 16 bits are read from the internal asynchronous receive buffer. This reading must be done in the Quadlet unit, without fail. Since reading must be done in the Quadlet unit, it is necessary to read out data for the upper 16 bits first, then data for the lower 16 bits.

7	6	5	4	3	2	1	0
ARFData-H							
15	14	13	12	11	10	9	8
ARFData-H							

3-2-15-2 ARF Data Register -L

Address 4Eh
Initial value 0000h

This is a register intended for asynchronous packet receive data reading. Data of the lower 16 bits are read from the internal asynchronous receive buffer.

7	6	5	4	3	2	1	0
ARFData-L							
15	14	13	12	11	10	9	8
ARFData-L							

3-2-16-1 Buffer Status and Control Register

Address 50h

Initial value 0000h

This register is used for the status control for the asynchronous send/receive internal buffer and the flash control for the asynchronous receive buffer.

7	6	5	4	3	2	1	0
					ARFEmpty	ATFFull	ATFEmpty
15	14	13	12	11	10	9	8
DackEn	DreqEn		SelectDreq				

Bit 0 **ATFEmpty** : ATF Empty bit (R - initial value : 1b)

0 = Indicates that the buffer is not vacant.

1 = Indicates that the buffer is vacant.

This bit indicates that the asynchronous send buffer accessed from the ATF Data register is vacant.

Bit 1 **ATFFull** : ATF Full bit (R - initial value : 0b)

0 = Indicates that the buffer is not full.

1 = Indicates that the buffer is full.

This bit indicates that the asynchronous send buffer accessed from the ATF Data register is full.

Bit 2 **ARFEmpty** : ARF Empty bit (R - initial value : 1b)

0 = Indicates that the buffer is not vacant.

1 = Indicates that the buffer is vacant.

This bit indicates that the asynchronous receive buffer accessed from the ARF Data register is vacant.

Bit 12 **SelectDreq** : Select Dreq bit (RW - initial value : 0b)

0 = Reflected to the DREQ signal as the status, equivalent to the ATFFull bit of a buffer being accessed by the ATF Data register.

1 = Reflected to the DREQ signal as the status, equivalent to the ARFEmpty bit of a buffer being accessed by the ARF Data register.

Bit 14 **DreqEn** : Dreq Enable bit (RW - initial value : 0b)

0 = The DREQ signal is kept non-active at any time.

1 = The DREQ signal is made active as the status with the contents chosen by SelectDreq.

This is a bit to make the DREQ signal valid.

This register is to select the buffer status in the chip in order to reflect to DREQ signal.

Bit 15 **DackEn** : Dack Enable bit (RW - initial value : 0b)

- 0 = Even when the Dack# signal is active, the MD8413 disables this signal.
1 = The Dack# signal is made valid.

Address 52h

Initial value 0000h

This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-17-1 Interrupt Register -H

Address 54h

Initial value 0000h

When contents of this register are read by the host, it is possible to know a variety of interrupt factors for the MD8413. For all bits in this register, “1” indicates that an interrupt factor has arisen. The interrupt factor can be cleared by writing “1”.

7	6	5	4	3	2	1	0
ATxEnd			ARxEnd		ITFNoTx		
15	14	13	12	11	10	9	8
			ARFRej			STO	RetryLimit

Bit 2 ITNoTx : Isochronous No Transmit bit (RW - initial value : 0b)

When the MD8413 maintains isochronous transmission in AUTO mode, “1” is set under the following conditions:

- ✎ When ITZERO=0 and transmission is not effected after the exchange of the Cycle Start packet.
- ✎ When ITZERO=1 and a packet of Length=0 is sent after the exchange of the Cycle Start packet.

Bit 4 ARxEnd : Asynchronous Receive End bit (RW - initial value : 0b)

Setting is made at “1” when the MD8413 performs asynchronous reception, and data are saved in the ARF buffer.

Bit 7 ATxEnd : Asynchronous Transmitt End bit (RW - initial value : 0b)

Setting is made at “1” when the MD8413 performs asynchronous transmission, and the Ack code is returned from the destination upon completion of transmission. In the case of retry operation, setting is also made at “1” when AckErr is set upon completion of or in the middle of the retry phase.

Bit 8 RetryLimit : Retry Limit Detect bit (RW - initial value : 0b)

Setting is made at “1” when the MD8413 is operating in the retry phase and this retry phase cannot be finished even after exceeding the limit value.

Bit 9 STO : Split Time Out Detect bit (RW - initial value : 0b)

Setting is made at “1” when STStart is issued and a count value is delivered to the Split Time Out register.

Bit 12 ARFRej : ARF Reject bit (RW - initial value : 0b)

Setting is made at “1” when the MD8413 performs asynchronous reception, but data are not saved in the ARF buffer.

3-2-17-2 Interrupt Register -L

Address 56h

Initial value 0000 0000h

When contents of this register are read by the host, it is possible to know a variety of interrupt factors for the MD8413. For all bits in this register, "1" indicates that an interrupt factor has arisen. The interrupt factor can be cleared by writing "1".

7	6	5	4	3	2	1	0
CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset			
15	14	13	12	11	10	9	8
PhyInt	BusReset		PhyRegRcvd	AckErr	TCodeErr	HdrErr	SentRej

Bit 3 **CmdReset** : Command Reset bit (RW - initial value : 0b)

Setting is made at "1" when a packet has been received, addressed in the reset area of the CSR space.

Bit 4 **CycleLost** : Cycle Lost bit (RW - initial value : 0b)

Setting is made at "1" when the MD8413 node is not of the CycleMaster, and the next Cycle Start packet cannot be received for 250μsec of the cycle timer, after the renewal of this internal cycle timer upon reception of a certain Cycle Start packet.

Bit 5 **CycleDone** : Cycle Done bit (RW - initial value : 0b)

Setting is made at "1" when a certain isochronous cycle is over.

Bit 6 **CycleStart** : Cycle Start bit (RW - initial value : 0b)

Setting is made at "1" when a new isochronous cycle is started.

Bit 7 **CycleSeconds** : Cycle Seconds bit (RW - initial value : 0b)

Setting is made at "1" when the cycle timer possessed by the MD8413 has counted 1 second.

Bit 8 **SentRej** : Sent Reject bit (RW - initial value : 0b)

Setting is made at "1" when an asynchronous packet has been received, but it cannot have been received completely because of lack of vacancy in the receive buffer to cover the capacity of this packet, and a busy acknowledge packet is returned from the MD8413 to the source node.

Bit 9 **HdrErr** : Header Error bit (RW - initial value : 0b)

Setting is made at "1" when packet reception is effected and a packet with the header including an error has been received.

Bit 10 **TCodeErr** : TCode Error bit (RW - initial value : 0b)

Setting is made at "1" when packet transmission is effected and a code not supported by the MD8413 is set in the TCode area of the packet header.

Bit 11 AckErr : Acck Error bit (RW - initial value : 0b)

Setting is made at "1" when an acknowledge packet is not normally received, returned from the destination node for the transmitted asynchronous packet.

Bit 12 PhyRegRcvd : Phy Register Received bit (RW - initial value : 0b)

Setting is made at "1" when data from Phy have been saved in RegData, after read request issuing toward the PHY register.

Bit 14 BusReset : Bus Reset bit (RW - initial value : 0b)

Setting is made at "1" when PHY is set in the Bus Reset mode.

Bit 15 PhyInt : Phy Interrupt bit (RW - initial value : 0b)

Setting is made at "1" when an interrupt factor comes from PHY connected to the MD8413.

3-2-18-1 Interrupt Mask Register -1-H

Address 58h

Initial value 0000h

This register is used for masking when avoiding reflection on the INT-1# signal of each interrupt causing factor in the Interrupt register. Arrangement for this register is the same as that for the Interrupt register. For each bit, masking is effected with "1" setting. This register enables combination of interrupt factors with the INT-1# and INT-2# signals.

3-2-18-2 Interrupt Mask Register -1-L

Address 5Ah

Initial value 0000h

This register is used for masking when avoiding reflection on the INT-1# signal of each interrupt causing factor in the Interrupt register. Arrangement for this register is the same as that for the Interrupt register. For each bit, masking is effected with "1" setting. This register enables combination of interrupt factors with the INT-1# and INT-2# signals.

3-2-19-1 Interrupt Mask Register -2-H

Address 5Ch

Initial value 0000h

This register is used for masking when avoiding reflection on the INT-2# signal of each interrupt causing factor in the Interrupt register. Arrangement for this register is the same as that for the Interrupt register. For each bit, masking is effected with "1" setting. This register enables combination of interrupt factors with the INT-1# and INT-2# signals.

3-2-19-2 Interrupt Mask Register -2-L

Address 5Eh

Initial value 0000h

This register is used for masking when avoiding reflection on the INT-2# signal of each interrupt causing factor in the Interrupt register. Arrangement for this register is the same as that for the Interrupt register. For each bit, masking is effected with "1" setting. This register enables combination of interrupt factors with the INT-1# and INT-2# signals.

3-2-20 Split TimeOut Register

Address 60h

Initial value 0320h

When a certain transaction falls into a split transaction, this setting register is used to control its time-out condition. Counting is started with “1” for the STStart bit, and is stopped with “0”. When coincidence with the set value in this register is detected during counting, Split Time Out is sent to the host by STO Interrupt. This counter completes counting every 125μsec. Therefore, the maximum setting value is less than 8 seconds.

7	6	5	4	3	2	1	0
SplitTimeLimit							
15	14	13	12	11	10	9	8
SplitTimeLimit							

3-2-21 Split TimeOut Register

Address 62h

Initial value 0000h

When a certain transaction falls into a split transaction, this setting register is used to control its time-out condition. Counting is started with “1” for the STStart bit, and is stopped with “0”. The lapse time is output at that time.

7	6	5	4	3	2	1	0
SplitTime							
15	14	13	12	11	10	9	8
SplitTime							

3-2-23 Split Timer Start Register

Initial value 64h

Initial value 0000h

7	6	5	4	3	2	1	0
							STStart
15	14	13	12	11	10	9	8

Bit 0 **STStart** : Split Timer Start bit (RW - initial value : 0b)
STStart=0 : Clear condition of the Split timer is retained.
STStart=1 : The Split Timer counter is started. Initial state is recovered with “0”.

When STO interrupt arises, the STStart bit is automatically cleared.

Address 66h
Initial value 0000h
This address is reserved.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

3-2-24-1 GPIO Register

Address 68h
Initial value 0000h
It is possible to make setting for each pin, regarding whether the status of each GPIO pin should be input or output.

7	6	5	4	3	2	1	0
				GPIOCTL(3:0)			
15	14	13	12	11	10	9	8

Bit 3~0 **GPIOCTL(3:0)** : GPIO Control bit (RW - initial value : 0b)
GPIOCTL(3:0)=0 : Each GPIO pin is set for INPUT.
GPIOCTL(3:0)=1 : Each GPIO pin is set for OUTPUT.

3-2-24-2 GPIO Register

Address 6Ah
Initial value 0000h

7	6	5	4	3	2	1	0
				GPIO(3:0)			
15	14	13	12	11	10	9	8

Bit 3~0 GPIO(3:0) : GPIO Data bit (RW - initial value : 0b)

When setting is made for INPUT with GPIOCTL, reading out is valid and it is possible to read out information of each GPIO pin. If setting is made for OUTPUT, writing only is valid and “high” level for “1” and “low” level for “0” are output from the respective GPIO pins.

3-2-25 ATGo Register

Address 6Ch
Initial value 0000h

“1” is set in the ATGo register of this register in the case of asynchronous packet transmission, and the occurrence of this packet transmission is announced to the MD8413. When the required packet is sent to the internal buffer of the MD8413, the host sets up this ATGo register thereafter. The MD8413 starts packet transmission with “1” in the STGo register, using a packet that contains data having been accumulated in the buffer. Since a Go command is issued at that time, the host can identify the start of MD8413’s sending operation, with ATBusy that has been turned “1” or asynchronous transmission. Timing for the next ATGo command issuing is when ATBusy is turned “0” in asynchronous transmission. Even though an ATGo command is issued while ATBusy is “1”, the MD8413 will disregard it. Even though “0” is written in this register, such an attempt is also useless.

7	6	5	4	3	2	1	0
							ATGo
15	14	13	12	11	10	9	8

Bit 0 **ATGo** : AT Go bit (RW - initial value : 0b)

When “1” is written in this register, the MD8413 know the start of asynchronous packet transmission.

3-3 List of Registers

Register	Adrs	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version	00h	Version															
Revision	02h	Revision															
Control-H	04h	DackHigh	DreqLow		ARFBusReset	CSEn	IACTIVE	AACTIVE	LPSON	ITZERO		IsoMode			CycleSource	CycleMaster	CycleTimeEn
Control-L	06h															ReceiveEn	TransmitEn
Node Identification-H	08h	IDValid	root														
Node Identification-L	0Ah	BusNumber										NodeNumber					
Reset	0Ch												ResetDMA	ResetLink	ResetTx	ResetARF	ResetATF
Reserved	0Eh																
Asynchronous Buffer Size Set	10h														ARxBufSize		
Reserved	12h																
Packet Control	14h						BusyCtrl					RxSelfID	EnSnoop				
Reserved	16h																
Diagnostic Status-H	18h																
Diagnostic Status-L	1Ah	RetryTimeMax		Ack Status		ATAck									BusyState		

Table 3-4-1 List of registers 1

Register	Adrs	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phy Control	1Ch		RegRcvd	RdReg	WrReg	RegAddr				RegData							
Reserved	1Eh																
ATRetries	20h								RetryStop	RetryCount				MaxRetryCountLimit			
Reserved	22h																
ATRetries	24h	MaxRetrySecondLimit			MaxRetryCycleLimit												
ATRetries	26h	RetrySecond			RetryCycle												
Cycle Timer-H	28h	CycleSeconds							CycleCount								
Cycle Timer-L	2Ah	CycleCount				CycleOffset											
Bus Timer-H	2Ch	SecondCountHi															
Bus Timer-L	2Eh	SecondCountHi									SecondCountLo						
Isochronous Transmit Configuration Register	30h	Tag	Channel													Speed	
Isochronous Transmit Configuration Register	32h	Sync				StartSync				StopSync							SyncEn
Isochronous Transmit Configuration Register	34h	ITLength															
Reserved	36h																

Table 3-4-2 List of registers 2

Register	Adrs	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Isochronou Receive Configuration 1	38h			Channel													
Isochronou Receive Configuration 1	3Ah					StartSync				StopSync						IsoRxEn	SyncEn
Isochronou Receive Configuration 2	3Ch			Channel													
Isochronou Receive Configuration 2	3Eh					StartSync				StopSync						IsoRxEn	SyncEn
ReservedIsochronou Configuration 3	40h			Channel													
Isochronou Receive Configuration 3	42h					StartSync				StopSync						IsoRxEn	SyncEn
Isochronou Receive Configuration 4	44h			Channel													
Isochronou Receive Configuration 4	46h					StartSync				StopSync						IsoRxEn	SyncEn
ATF Data-H	48h	ATF Data-H															
ATF Data-L	4Ah	ATF Data-L															
ARF Data-H	4Ch	ARF Data-H															
ARF Data-L	4Eh	ARF Data-L															
Buffer Status and Control	50h	DackEn	DreqEn		SelectDreq											ARFEmpty	ATFFull
Reserved	52h																
Interrupt-H	54h				ARFRej			STO	RetryLimit	ATxEnd			ARxEnd		ITFNoTx		
Interrupt-L	56h	PhyInt	BusReset		PhyRegRcvd	AckErr	TcodeErr	HdrErr	SentRej	CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset			

Table 3-4-3 List of registers 3

Register	Adrs	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Mask-1-H	58h				ARFRrej			STO	RetryLimit	ATxEnd			ARxEnd		ITFNoTx		
Interrupt Mask-1-L	5Ah	PhyInt	BusReset		PhyRegRcvd	AckErr	TcodeErr	HdrErr	SentRej	CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset			
Interrupt Mask-2-H	5Ch				ARFRrej			STO	RetryLimit	ATxEnd			ARxEnd		ITFNoTx		
Interrupt Mask-2-L	5Eh	PhyInt	BusReset		PhyRegRcvd	AckErr	TcodeErr	HdrErr	SentRej	CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset			
Split TimeOut-H	60h	SplitTimeLimit															
Split TimeOut-L	62h	SplitTime															
Split TimeOut Start	64h																STStart
Reserved	66h																
GPIO Conrtol	68h													GPIOCTL(3:0)			
GPIO	6Ah													GPIO(3:0)			
ATGo	6Ch																ATGo

Table 3-4-4 List of registers 4

4 Data Format

4-1 Asynchronous

4-1-1 Quadlet Transmit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														spd		tLabel					rt		tCode					priority			
destinationID															destinationOffset-H																
destinationOffset-L																															
quadlet data (for write request and read response)																															

Table 4-1-1 Quadlet Transmit format (Asynchronous)

spd : speed field

This field is used to designate the transfer speed. Refer to Table 4-6-6 regarding setting values.

tLabel : Transaction label field

This field is used to define a unique tag for each transferred transaction. The tLabel sent for requesting is used as a transaction label for correct response. The values used are valid in the range of 0h~Fh.

rt : retry field

This field is used to define whether this packet is in the middle of making a retry. The retry protocol is followed by the destination node. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

This field is used to set up a transaction code. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

priority : priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to set up 0000b, without fail.

destinationID : destination ID field

This field is used to set up destination bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

destinationOffset : destination Offset Address field

This field is used to define the lower 48-bit address of the destination node for the requested packet. The setting value need be defined in the quadlet unit in the case of a read request for quadlet data and a write request for quadlet data.)

quadletData:quadlet data field

This field is used to set up actual transfer data (1 Quadlet).

4-1-2 Block Transmit

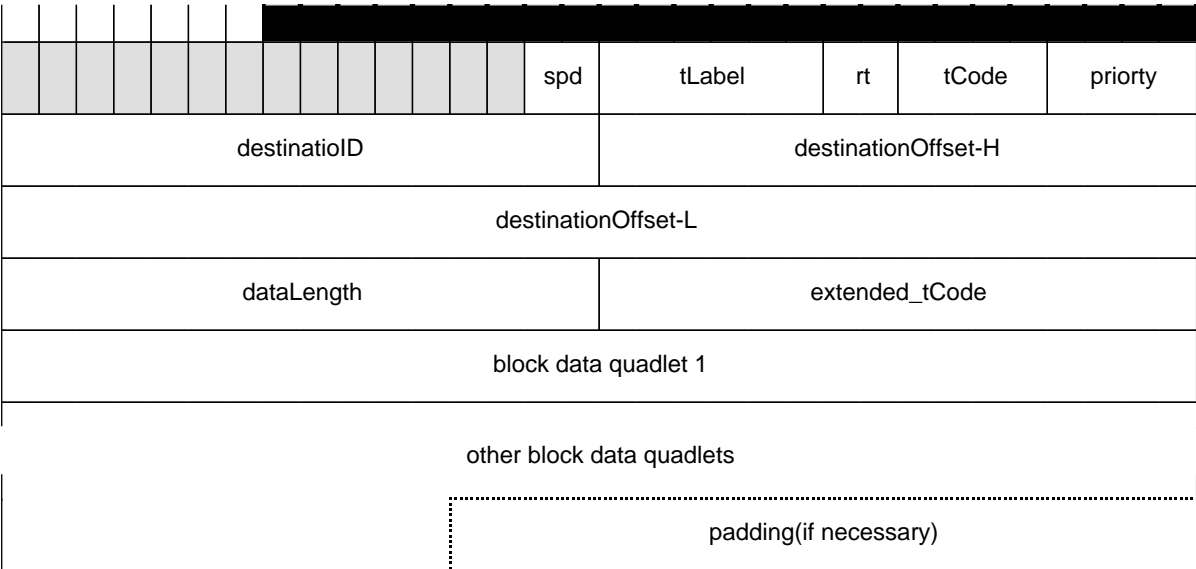


Table 4-1-2 Block Transmit format (Asynchronous)

spd : speed field

This field is used to designate the transfer speed. Refer to Table 4-6-6 regarding setting values.

tLabel :Transaction label field

This field is used to define a unique tag for each transferred transaction. The tLabel sent for requesting is used as a transaction label for correct response. The values used are valid in the range of 0h~FFf.

rt : retry field

This field is used to define whether this packet is in the middle of making a retry. The retry protocol is followed by the destination node. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

This field is used to set up a transaction code. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

priority : priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to set up 0000b, without fail.

destinationID : destination ID field

This field is used to set up destination bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3

regarding details.

destinationOffset : destination Offset Address Field

This field is used to define the lower 48-bit address of the destination node for the requested packet.

The setting value need be defined in the quadlet unit in the case of a read request for quadlet data and a write request for quadlet data.

dataLength : data length field

This field is used to set up data length for the blockData field. The maximum value of the setting value depends on that of the speed field. Refer to Table 4-6-4 regarding details.

extended_tCode : extended transaction code field

This field is used to define the extension tCode. This extended_tCode becomes valid only if tCode is "lock request" or "lock response". For other tCodes, 0000h must be set in this register. Refer to Table 4-6-5 regarding details.

blockData : block data field

This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.

4-1-3 Quadlet Receive

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
destinatioID																tLabel						rt		tCode				priority				
sourceID																destinationOffset-H																
destinationOffset-L																																
quadlet data (for write request and read response)																																
																spd																ackSent

Table 4-1-3 Quadlet Receive format (Asynchronous)

destinationID : destination ID field

The destination bus of this packet and the node ID are saved in this field. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

tLabel : Transaction label field

This field is used to define a unique tag for each transferred transaction.

rt : retry field

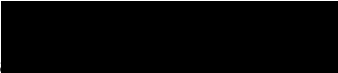
This field is used to define whether this packet having been sent is in the middle of making a retry. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

A transaction code is saved in this field. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

priority : priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to save 0000b, without fail.

sourceID :  **spd** **tLabel** **rt** **tCode**

This field is used to save the source bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

destinationOffset :destination Offset Address field

This field is used to save the lower 48-bit address of the destination node for the requested packet.

quadletData : quadlet data field

This field is used to save transferred data.

spd : speed field

This field is used to designate the received speed. Refer to Table 4-6-6 regarding setting values.

ackSent : ackSent field

This field saves the Ack code returned as an acknowledge signal after this packet has been received. Refer to Table 4-6-7 regarding details.

4-1-4 Block Receive

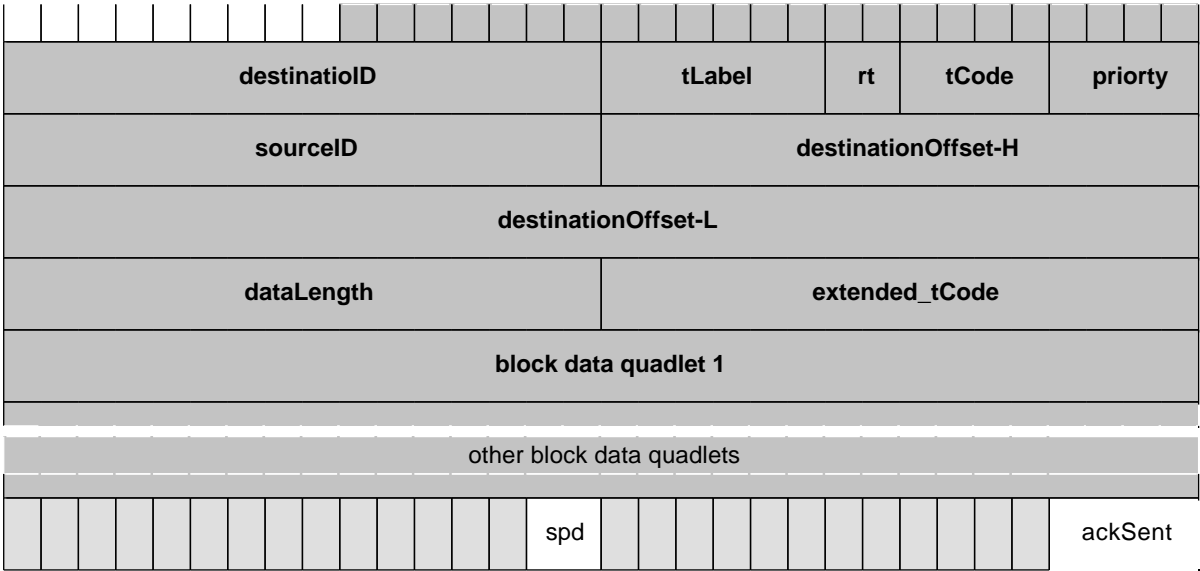


Table4-1-4 Block Receive format (Asynchronous)

destinationID : destination ID field

The destination bus of this packet and the node ID are saved in this field. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

tLabel : Transaction label field

This field is used to define a unique tag for each transferred transaction.

rt : retry field

This field is used to define whether this packet having been sent is in the middle of making a retry. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

A transaction code is saved in this field. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

priority : priority field

This field is valid in the back plane environment. Therefore, 0000b is always saved.

sourceID : source ID field

This field is used to save the source bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

destinationOffset : destination Offset Address field

This field is used to save the lower 48-bit address of the destination node for the requested packet.

dataLength : data length field

This field is used to set up data length for the blockData field.

extended_tCode : extended transaction code field

This extended_tCode becomes valid only if tCode is "lock request" or "lock response". For other tCodes, 0000h is saved in this register.

blockData : block data field

The transferred data are saved in this field.

spd : speed field

This field is used to designate the received speed. Refer to Table 4-6-6 regarding setting values.

ackSent : ackSent field

This field saves the Ack code returned as an acknowledge signal after this packet has been received.

Refer to Table 4-6-7 regarding details.

4-2 Isochronous

4-2-1 For Normal Mode

4-2-1-1 Transmit

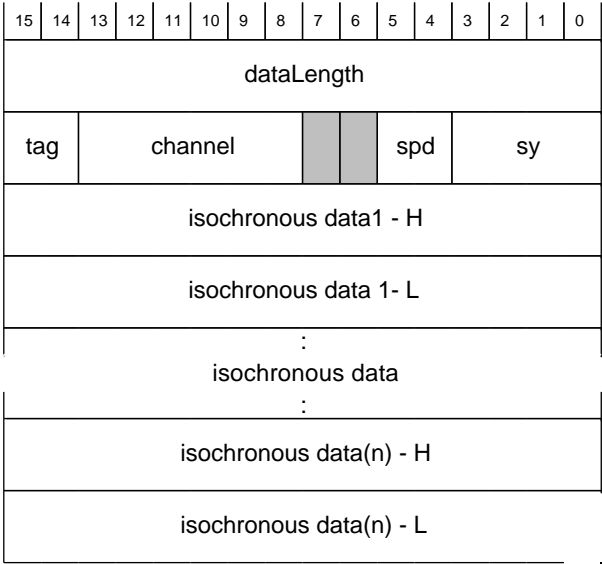


Table4-2-1 Block Transmit format (Isochronous:normal)

dataLength : data length field
This field is used to set up data length for the blockData field.

tag : tag field
This field is used to set up Tag for Isochronous transmit.

channel : channel field
This field is used to set up Channel number for Isochronous transmit.

spd : speed field
This field is used to designate the transfer speed.

sy : sync field
This field is used to set up Sync data for Isochronous transmit.

Isochronous Data : Isochronous data field
This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.

4-2-1-2 Receive

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dataLength															
tag		channel						tCode				sy			
isochronous data1 - H															
isochronous data1 - L															
:															
isochronous data															
:															
isochronous data(n) - H															
isochronous data(n) - L															

Table4-2-2 Block Receive format (Isochronous:normal)

- dataLength

: data length field

This field is used to designate the received data length for the blockData field.
- tag

: tag field

This field is used to designate the received Tag data.
- channel

: channel field

This field is used to designate the received Channel number.
- sy

: sync field

This field is used to designate the received Sync data.
- tCode

: Transaction code field

A transaction code is saved in this field. The transaction code values is 'Ah'.
- isochronous Data

: Isochronous data field

The transferred data are saved in this field.

4-2-2 For Auto Mode

4-2-2-1 Transmit

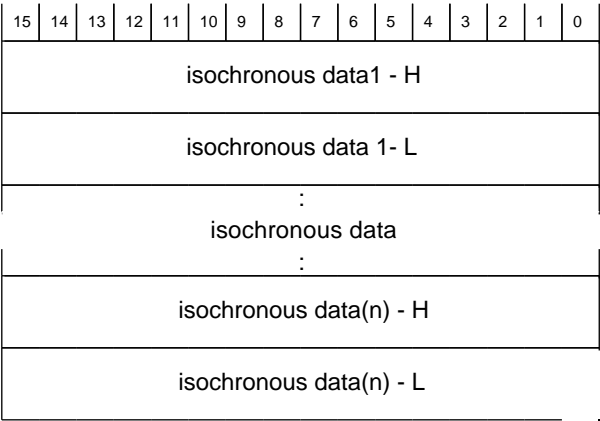


Table4-2-3 Block Transmit format (Isochronous:auto)

Isochronous Data : Isochronous data field

This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.

4-2-2-2 Receive

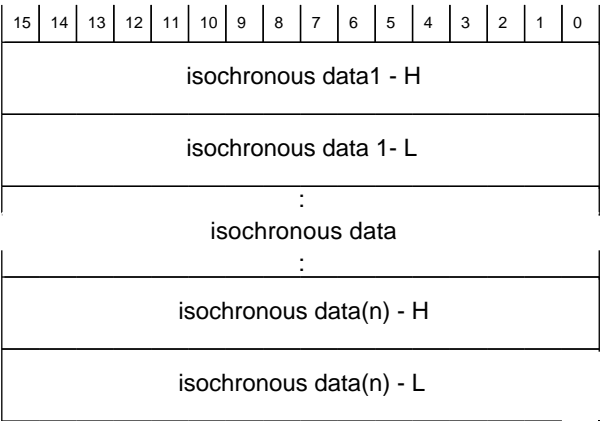


Table4-2-4 Block Receive format (Isochronous:auto)

isochronous Data : Isochronous data field

The transferred data are saved in this field.

4-3 Snoop

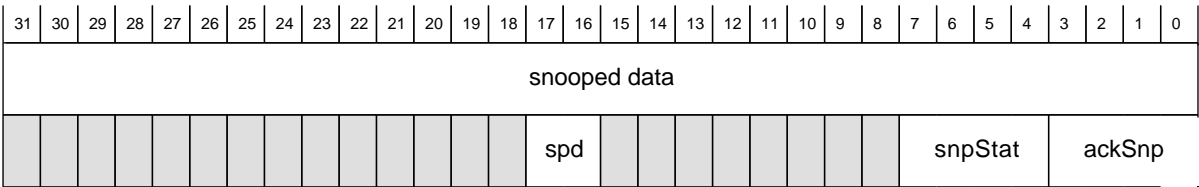


Table4-3-1 Snoop Receive format

snoopedData : snooped data field

Third field is used to save the snooped data.

spd : speed field

This field is used to save the received speed. Refer to Table 4-6-6 regarding setting values.

snpStat : snooped Status field

This field saves the Ack code to be returned as a status (acknowledge) signal after this packet has been received. Actually, however, the Ack code is not returned. Refer to Table 4-6-7 regarding details.

ackSnp : snooped ack-code field

This field saves the received Ack code. In other words, a node that has received this packet corresponds to the returned Ack code.

4-4 SelfID Packet

After the identification quadlet data shown in Table 4-4-1 have been saved, an actual SelfID packet is saved.
This operation is completed with the last quadlet ID data as shown in Table 4-4-4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table4-4-1 SelfID Packet Receive format(first quadlet)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID						0	L	gap_cnt						sp	del	C	pwr			p0	p1	p2	i	m					
logical inverse of first quadlet																															

Table4-4-2 SelfID Packet Receive format(SelfID Packet #0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID								1	n	rsv	pa	pb	pc	pd	pe	pf	pg	ph	r	m									
logical inverse of first quadlet																															

Table4-4-3 SelfID Packet Receive format(SelfID Packet #1, #2, & #3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ackSent																															

Table4-4-4 SelfID Packet Receive format(last quadlet)

	n	pa	pb	pc	pd	pe	pf	pg	ph
pkt #1	0	p3	p4	p5	p6	p7	p8	p9	p10
pkt #2	1	p11	p12	p13	p14	p15	p16	p17	p18
pkt #3	2	p19	p20	p21	p22	p23	p24	p25	p26

Table4-4-5 SelfID Packet Receive format(pn)

phy_ID : physical_ID field

A node ID of the PHY chip used to send this packet.

L : link_active field

0 = LINK is not active.

1 = Active link and transaction layer are present in this node.

gap_cnt : gap_count field

A present value of the PHY_CONFIGURATION.gap_count field for this node is saved.

sp : PHY_SPEED field

- 00 = 98.304Mbps
- 01 = 98.304 and 196.608Mbps
- 10 = 98.304 and 196.608 and 393.216Mbps
- 11 = Reserved

Available speeds are saved.

del : PHY_DELAY field

- 00 = 144ns or less (~14/BASE_RATE)
- 01~11= Reserved.

The delay time of the repeater in the worst case is saved.

C : CONTENDER field

When this field is set and the link_active field is also set, this node indicates that it can be a bus or isochronous resource manager.

pwr : POWER_CLASS field

- 000= The node does not require power supply.
- 001= The node does has its own power supply that can feed a minimum of 15W.
- 010= The node does has its own power supply that can feed a minimum of 30W.
- 011= The node does has its own power supply that can feed a minimum of 45W.
- 100= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the LINK and upper layers.
- 101= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the LINK and upper layers.
- 110= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 5W to enable the LINK and upper layers.
- 111= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 9W to enable the LINK and upper layers.

p0 ... p26 : NORT,child[NPORT],connected[NPORT]field

- 11 = Connected to the parent node.
- 10 = Connected to the parent node.
- 01 = Not connected to another PHY.
- 00 = This PHY is not offered.

The port status is shown.

i : initiated_reset field

If it is set, this node has issued present bus reset.

m : more_packets field

If it is set, this node indicates that another SelfID packet of this node is closely following.

n : Extended field

An extension SelfID packet sequence number (value from 0~2).

r,rsv : reserved field

Reserved.

4-5 PHY Control Packet

To send a PHY control packet, the first quadlet of data shown in Table 4-5-4 is saved in the ATF buffer, and the PHY Control Packet specified by 1394 is then saved. In this case, it is necessary to save the PHY Control Packet data together with the reversal data.

In actual transmission, the first quadlet is not sent and the PHY Control packet only is sent. Refer to the Draft regarding details.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																								1110b							

Table 4-5-1 PHY control packet format(first quadlet)

4-6 Code

The codes used for packet formatting specified by 1394 are shown. Refer to the 1394 Draft for details of each code.

Code	Name
00b	retry_1
01b	retry_X
10b	retry_A
11b	retry_B

Table 4-6-1 List of Retry code

Code	Name	Code	Name
0h	write request for data quadlet	8h	cycle start
1h	write request for data block	9h	lock request
2h	write response	Ah	isochronous data block
3h	reserved	Bh	lock response
4h	read request for data quadlet	Ch	reserved
5h	read request for data block	Dh	reserved
6h	read response for data quadlet	Eh	reserved
7h	read response for data block	Fh	reserved

Table 4-6-2 List of Transaction code (tCode)

destination bus_ID	destination node_ID	Contents
0Å`3FEh	0Å`3Eh	Transferred to the node defined by bus_ID and node_ID.
3FFh	0Å`3Eh	Transferred to the node defined by node_ID in local bus.
0Å`3FEh	3Fh	Broadcast transfer to the bus defined by bus_ID.
3FFh	3Fh	Broadcast transfer in local bus.

Table 4-6-3 List of Bus Number / Node Number

Data rate	Maximum payload size (byte)
100Mbps	512
200Mbps	1024
400Mbps	2048

Table 4-6-4 List of Data Length (Data Length)

Code	Name
0000h	reserved
0001h	mask_swap
0002h	compare_swap
0003h	fetch_add
0004h	little_add
0005h	bounded_add
0006h	wrap_add
0007h	vender-dependent
0008h - FFFh	reserved

Table 4-6-5 List of Extension Transaction Code(Extend tCode)

Code	Speed
00b	100Mbps
01b	200Mbps
10b	400Mbps
11b	reserved

Table 4-6-6 List of Speed Codes (spd)

Code	Name
0h	reserved
1h	ack_complete
2h	ack_pending
3h	reserved
4h	ack_busy_X
5h	ack_busy_A
6h	ack_busy_B
7h	reserved
8h	reserved
9h	reserved
Ah	reserved
Bh	reserved
Ch	reserved
Dh	ack_data_error
Eh	ack_type_error
Fh	reserved

Table 4-6-7 List of Acknowledge Codes (Ack)

5 Functional Descriptions

5-1 Host Interface

All MD8413 control and asynchronous exchange data transfer are effected through the host interface. Timing of the host interface signal is controlled with the respective signals of CS#, RD#, WR#, HA(6:1), and HD(15:0) by SRAM-like asynchronous transfer.

The internal registers and the 1394 packet formats basically have a width of 32 bits, but the MD8413 can be directly combined with the MPU that has a 16-bit data bus.

5-1-1 Register Access Timing

As shown in Fig. 5-1-1, the register is accessed by the SRAM-like asynchronous bus.

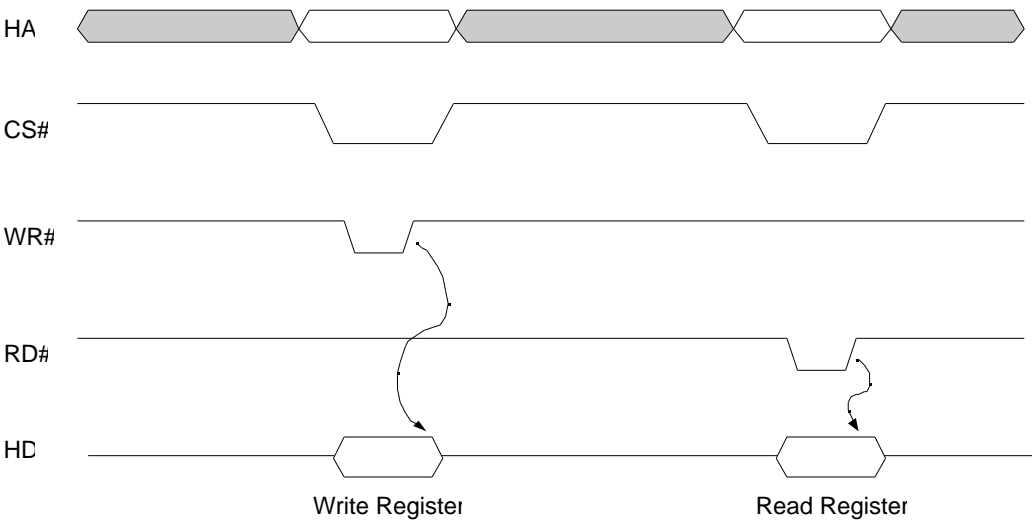


Figure 5-1-1 Host Access Timing

5-1-2 Host Bus Width

The effective bits for access from the host have the 16-bit width fixed.

5-1-3 DMA Transfer

The MD8413 supports the DMA transfer functions in terms of data transfer with exchange buffers. The supporting DMA mode is available only if the DMA service request signal (DREQ) is of the level sense. Only one objective buffer for DMA transfer can be chosen by the SelectDreq bit. Whether the DREQ signal is made valid or not is controlled by the DreqEn bit. When DreqEn="1" and the DREQ signal is valid, the assert/negate conditions for this DREQ signal are shown in Table 5-1-3. When DreqEn="0", the DREQ signal always stays in the negate state.

To transfer the send data, size of data being transferred to DMA is set up and executed. When DreqEn is set at "1" since then, a DREQ request is issued for the DMA and this enables execution of DMA transfer.

When transferring receive data to the host side, the data length is read out and the resultant value is set in DMAC, which is thereby actuated. When DreqEn is set at "1" since then, a DREQ request is issued for the DMA and this enables execution of DMA transfer.

SelectDreq bit	Destination buffer	DREQ assert condition	DREQ negate condition
0b	ATF	ATF buffer not full	ATF buffer full (ATFFull = "1")
1b	ARF	DATA remaining in ARF buffer	ARF buffer empty (ARF Empty = "1")

Table 5-1-3 Assert/Negate Conditions of the DREQ Signal

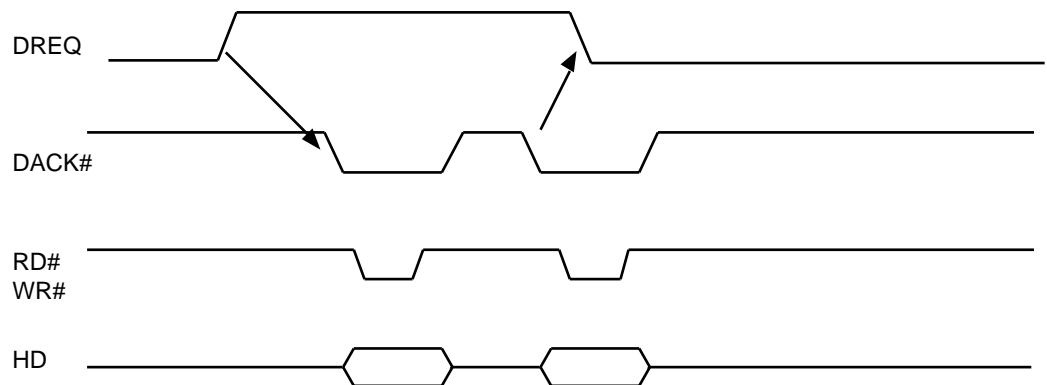


Figure 5-1-1 DMA Transfer Timing

Additional explanation is given below for the negate timing of the DMA service request signal (DREQ). As shown in Table 5-1-3, the negate condition appears when the internal buffer is full. When writing is done to attain a full condition (WR# entered), the DREQ signal is negated with a timing as shown in Table 5-1-2.

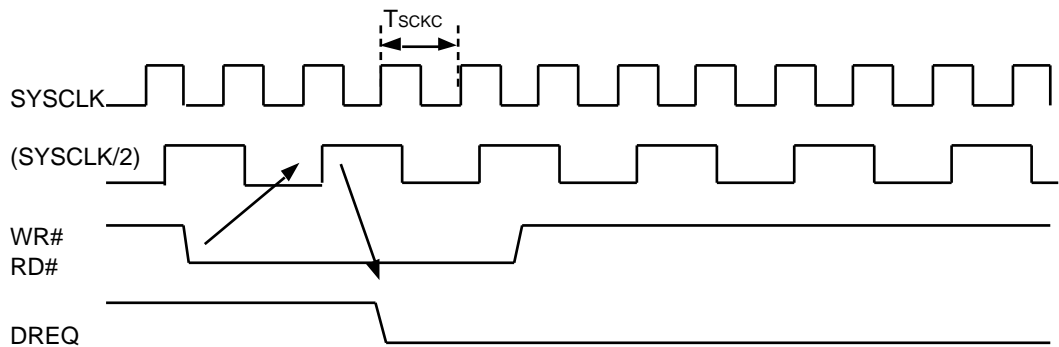


Figure 5-1-2 DREQ Negate Timing

5-1-4 Interrupt Processing

The MD8413 is provided with an INT# terminal to be used as a means of announcing the host about the interrupt factor defined by the Interrupt and Interrupt Mask registers. This INT# signal is active low, and is asserted in the form of an interrupt factor without OR, not masked by the Interrupt Mask register. When “1” is written in all bits of the Interrupt register, each bit is cleared and the INT# terminal is negated.

5-2 PHY Chip Interface

The interface toward the PHY chip is composed of the signals of SCLK, LREQ, D(0:3), and CTL(0:1). For connections with the PHY chips that have various maximum transfer speeds, a D (0:3) signal is used for selection from 100Mbps, 200Mbps, and 400Mbps. For connection with the PHY chip of 100Mbps, D(0:1) is used to enable communication. For connection with the PHY chip of 200Mbps, D(0:3) is used likewise to enable communication.

5-2-1 Connection Method

Regarding the method of connection with the PHY chips, the MD8413 supports both DC connection and AC connection systems. Regarding connection with the MD8402 which is the PHY chip of 200Mbps, the DC connection is shown in Fig. 5-2-1, and the AC connection is shown in Fig. 5-2-2. Details of the circuit for the AC connection are obtainable from Appendix.

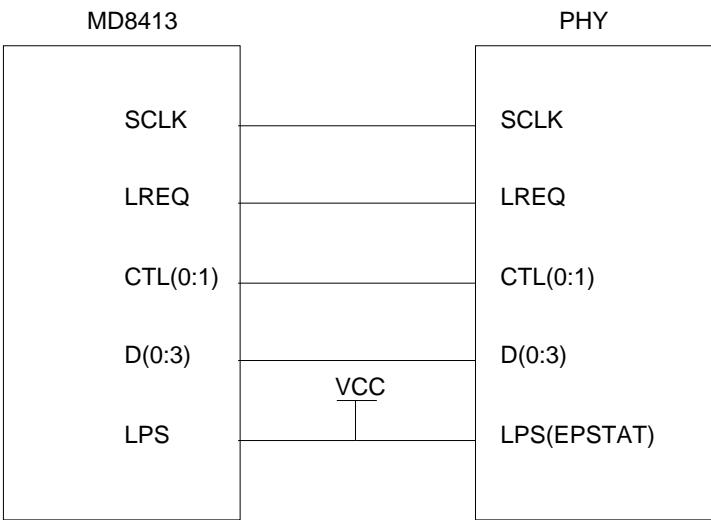


Figure 5-2-1 MD8413-PHY Chip Connection Diagram (DC Connection)

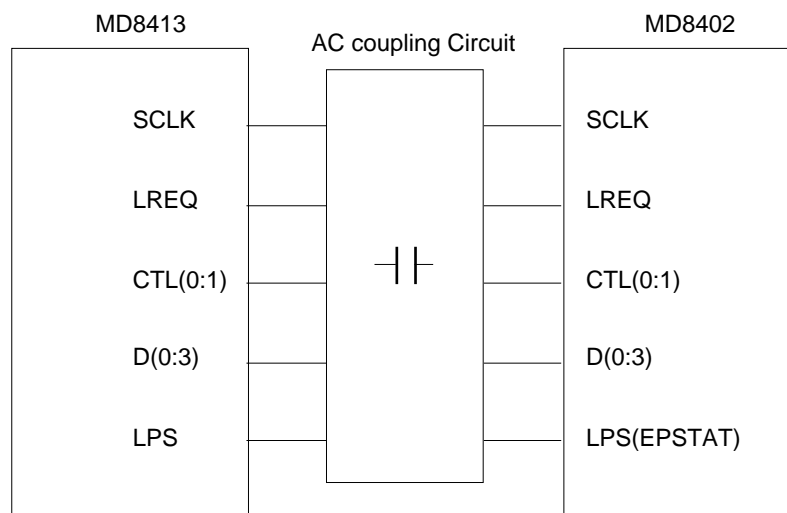


Figure 5-2-2 MD8413-MD8402 Connection Diagram (AC Connection)

5-2-2 PHY Chip Control

To control the PHY chip, the MD8413 employs a communication measure defined by 4 types of operation modes shown below. Each operation mode is defined by conditions of CTL(1:0) terminal.

CTL[0:1]	Operation	Contents
00b	Idle	Idle condition, with nothing in operation (default mode)
01b	Status	Status data transfer from the PHY chip
10b	Receive	Contents of receive packet transfer from the PHY chip
11b	Transmit	PHY - LINK bus controlled to transfer a send packet from LINK to the PHY chip

Table 5-2-1 PHY Chip Control Mode 1

After the PHY-LINK bus control is enabled in the above-mentioned Transmit mode, an operation mode is assumed as shown in Table 5-2-2.

CTL[0:1]	Operation	Contents
00b	Idle	PHY - LINK bus is released since LINK has completed data transfer
01b	Hold	<p>• The bus is held until data are fixed, since LINK is making data transfer</p> <p>• Link is calling for another packet transmission, without performing arbitration</p>
10b	Transmit	Transmit packet data are transferred to the PHY chip
11b	Reserved	Reserved

Table 5-2-2 PHY Chip Control Mode 2

5-2-3 Request

As a request to gain access to a register of the PHY chip or the PHY-LINK bus, the MD8413 sends out a short serial stream to the LREQ terminal. This stream contains the requested type, transferring packet speed, and reading or writing command.

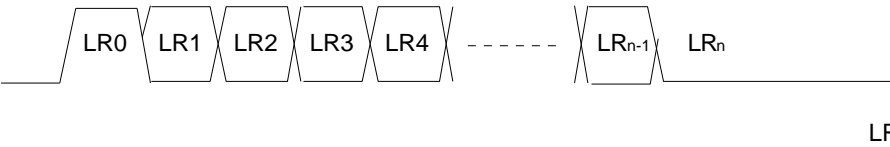


Figure 5-2-3 LREQ Stream

5-2-3-1 LREQ

The request for the PHY-LINK bus is effected with a 7-bit format indicated by LREQ shown in Table 5-2-3.

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. " 1 " is always transferred
1∧`3	Request Type	Indicates the request type shown in Table 5-2-6
4∧`5	Request Speed	Indicates the transfer speed of the request PHY chip
6	Stop Bit	Indicates the end of data transfer. " 0 " is always transferred

Table 5-2-3 Request Format

LREQ[4:5]	Data Rate
00	100Mbps
01	200Mbps
10	400Mbps
11	>400Mbps

Table 5-2-4 Speed Format

The request of register read-out for the PHY chip is effected with a 9-bit format indicated by LREQ shown in Table 5-2-5. The request of register write is effected with a 17-bit format indicated by LREQ shown in Table 5-2-6.

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. " 1 " is always transferred
1∧`3	Request Type	Indicates the request type shown in Table 5-2-6
4∧`7	Address	Indicates the register address of the reading PHY chip
8	Data	Indicates the end of data transfer. " 0 " is always transferred

Table 5-2-5 Read Register format

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. " 1 " is always transferred
1∧`3	Request Type	Indicates the request type shown in Table 5-2-6
4∧`7	Address	Indicates the register address of the writing PHY chip
8∧`15	Data	Indicates the register data of the writing PHY chip
16	Stop Bit	Indicates the end of data transfer. " 0 " is always transferrd

Table 5-2-5 Write Register Format

LREQ[1:3]	Operation	Contents
000	ImmReq	Immediate request
001	IsoReq	Isochronous request
010	PriReq	Priority request
011	FairReq	Fair request
100	RdReg	Contents of the set register being read out
101	WrReg	Writing in the set register
110, 111	Reserved	Reserved

Table 5-2-6 Request Type

5-2-4 Transfer

5-2-4-1 Status Request

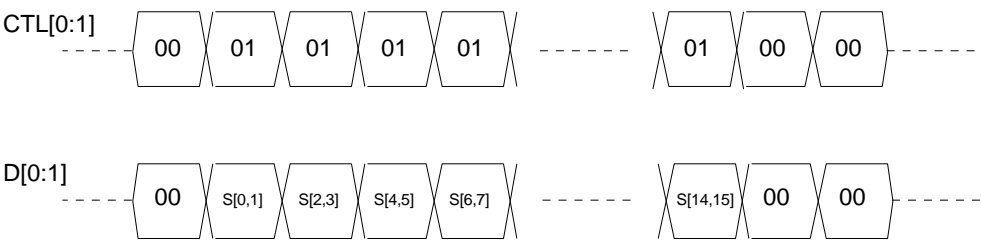


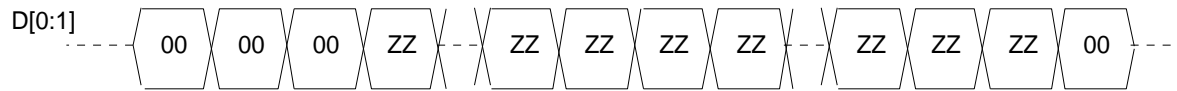
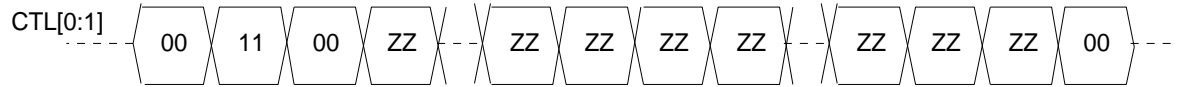
Figure 5-2-4 Status Request

Bit (Sn)	Operation	Contents
0	Arbitration Reset Gap	Arbitration Reset Gap is detected
1	Fair Gap	Fair Gap is detected
2	Bus Reset	Bus Reset is detected
3	Phy Interrup	Interrupt to the host is requested
4~7	Address	PHY register address returning the status
8~15	Data	Status data

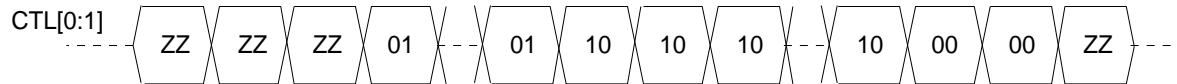
Table 5-2-7 Status Request Format

5-2-4-2 Transmit

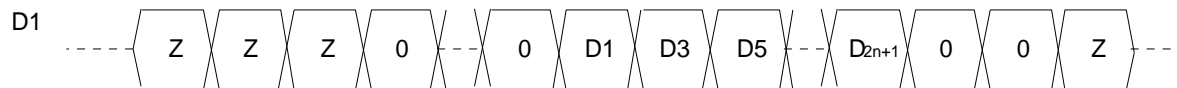
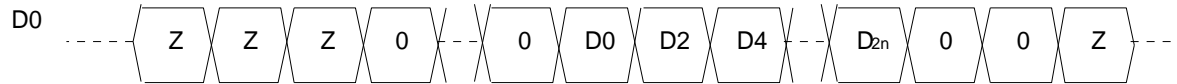
PHY Drive



LINK Drive



100Mbps



200Mbps

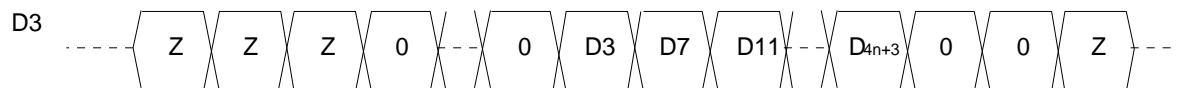
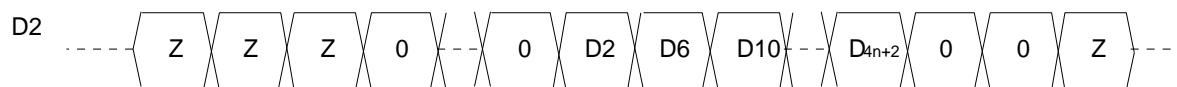
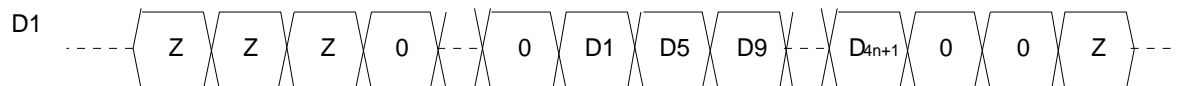
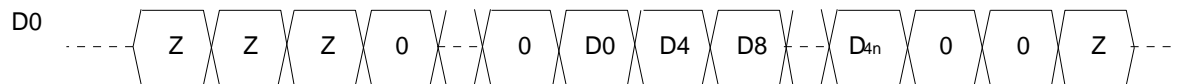


Figure 5-2-5 Transmit

5-2-4-3 Receive

PHY Drive



Figure 5-2-6 Receive

SP[0:7]	Data Rate
00xxxxxx	100Mbps
0100xxxx	200Mbps
01010000	400Mbps

Table 5-2-8 Speed Code (SP[0:7])

5-3 Buffer Access

5-3-1 Buffer Configuration

The MD8413 incorporates a memory buffer in 256X32+20X32 bit configuration, with a capacity of 1108 bytes in all. For rate absorption of host access rate and asynchronous transfer rate, the host and transmitter or receiver are temporarily used through an interface.

The MD8413 has an internal buffer control block that controls this buffer, split into two sections for transmission and reception of asynchronous data transfer. (The asynchronous transmission buffer and the asynchronous reception buffer are respectively referred to as ATF and ARF hereafter.)

To gain access to these buffers from the host, such actions are always taken through the ATF register and the ARF register.

5-3-2 Size Setting for Each Sub-Buffer

Buffer size is set with an initial value of 552 Bytes for ARF and 552 Bytes for ATF, respectively. Modification of the buffer size is possible by deciding the ARF size and using the remaining portion for the ATF. Prior to actual data exchange in applications, ARF size setting must be done by determining and designating the maximum receiving payload size. Generally, maximum receiving payload size is specified to the same value that is specified in the max_rec field of Bus_Info_Block in the Configuration ROM.

This size designation is effected according to the asynchronous receiving size (ARxBufferSize) of the Asynchronous Buffer Size Set register. By this setting, the transmission buffer size (ATxBufferSize) appears as shown below.

$$\text{ATxBufferSize} = 1104 - \text{ARxBufferSize}(\text{byte})$$

For block reception, the header generally requires 168 bytes and another 4 bytes is required for receive status and speed data. For receive size designation in the MD8413, the overall capacity is equal to a total of payload size and header-block size so that such a header block can be received. If an ARF size is specified for a size that is smaller than the receive packet size, the MD8413 returns a busy acknowledge signal to the source, and the related packet is not saved in ARF.

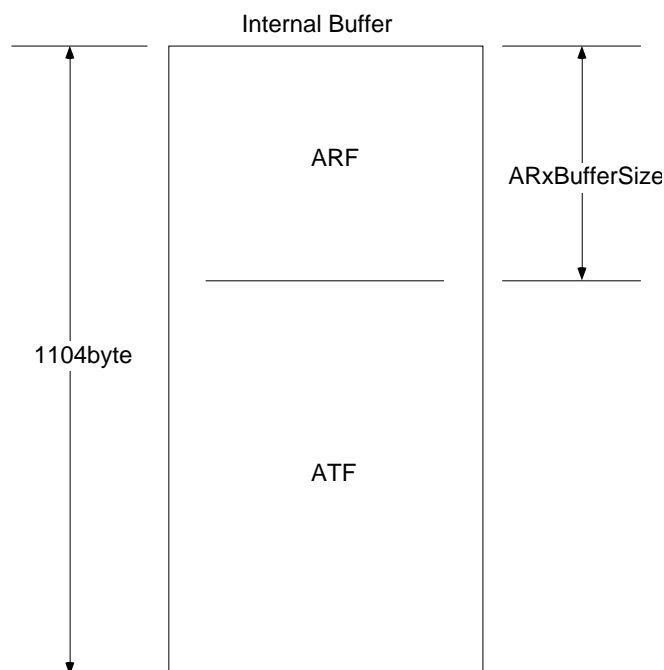


Figure 5-3-3 ARF/ATF Size Allocation

5-3-3-1 Soft Access

Since the IEEE 1394 stipulates that each packet is arranged in the Quadlet unit, the host bus has 16 bits. Therefore, it is necessary to perform data write/read operation for one Quadlet by dividing the process into two portions.

In the first place, data for 1 word are written in the 48h register. Then, writing is effected in the order of 4Ah. Upon completion of writing up to 4Ah, data for 1 Quadlet become valid. Therefore, writing order must be 48h and then 4Ah, without fail.

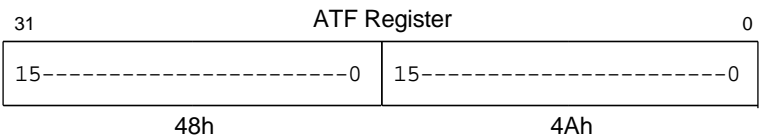


Figure 5-3-4 Register Operation during Soft Access(ATF)

For data reading from the ARF buffer, reading must be carried out in the order of 4Ch and then 4Eh.

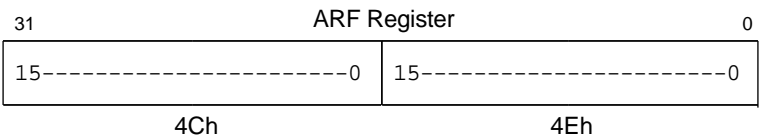


Figure 5-3-5 Register Operation during Soft Access(ARF)

5-3-3-2 DMA Access

In the case of DMA access, the objective buffer must be designated with the SelectDreq bit.

To set the ATF as a DMA transfer object, SelectDreq=0b is set up. DMAC is started and DreqEn is turned “1” thereafter. This causes a DREQ request to be issued toward DMAC, and DMA transfer is started. In this case, the first 1 word is saved in the 31~16 bits of the ATF buffer, and the second word is saved in the 15~bits. As a result, the saved data become valid as the 1 Quadlet data. For this reason, the number of DMA transfers is required to be a multiple of 2.

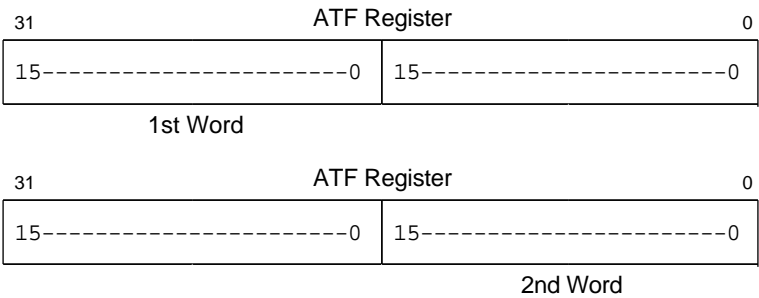


Figure 5-3-6 Register Operation during DMA Access (ATF)

Likewise, the same operation is performed for reading from the ARF buffer by DMA data transfer. The upper part of 32 bits is read out.

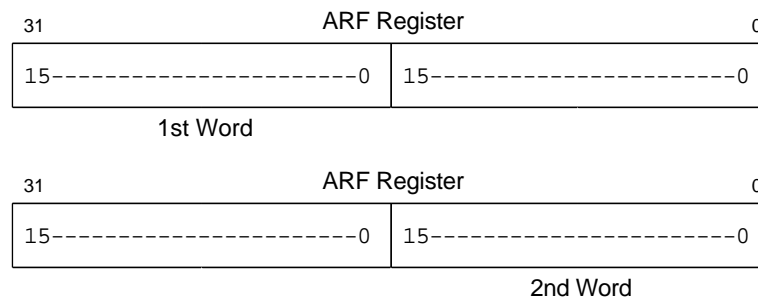


Figure 5-3-7 Register Operation during DMA Access (ARF)

5-3-4 Buffer Control

5-3-4-1 Asynchronous Buffer Control

For both asynchronous transmission and reception, the host gains access to a buffer in the packet unit. Therefore, as stated previously, designation of a send/receive packet size is always to a size that is larger than one packet. Otherwise, the MD8413 cannot send such a packet during transmission. In the case of reception, a busy acknowledge code is returned.

5-3-4-1-1 Transmission Buffer

When the host sends data to the buffer during transmission and ATGo is issued, such data contained in the ATF are regarded as one packet. If there is still some vacancy in the ATF buffer after the issuing of ATGo, the host can write data of the next requested packet in the ATF. In this manner, the MD8413 performs ping-pong-like control in the unit of one packet using the ATF on the host side and the transmitter side. If the buffer status is not of Empty, the quantity of data the host can write next may be on-line-controlled according to the ATF size set at the BufferSizeSet register and the transmitting ATGo packet size, or controlled with the ATFFull bit at the BufferStatus register.

The packet data presently being sent are kept buffered in the ATF until a complete or pending Ack code is returned from the destination node. Therefore, in the case of Ack code being busy, the buffered data are repeatedly transmitted until attaining the number of retries scheduled. If a complete, pending, or retry count value is exceeded in this time period, only the area in the ATF, where the packet is kept, is automatically flashed. If there is an error Ack code in the retry phase, this phase is suspended and flashing is performed at that time point, regardless of whether the maximum retry value is attained. In this case, even though the packet to be sent next has been written in a vacant area of the ATF, the saved data are never influenced by any other factors.

When ATF reset is effected with the Reset ATF in the Reset register, this ATF is restored to its initial state, all data therein are lost, and the Empty flag is turned active.

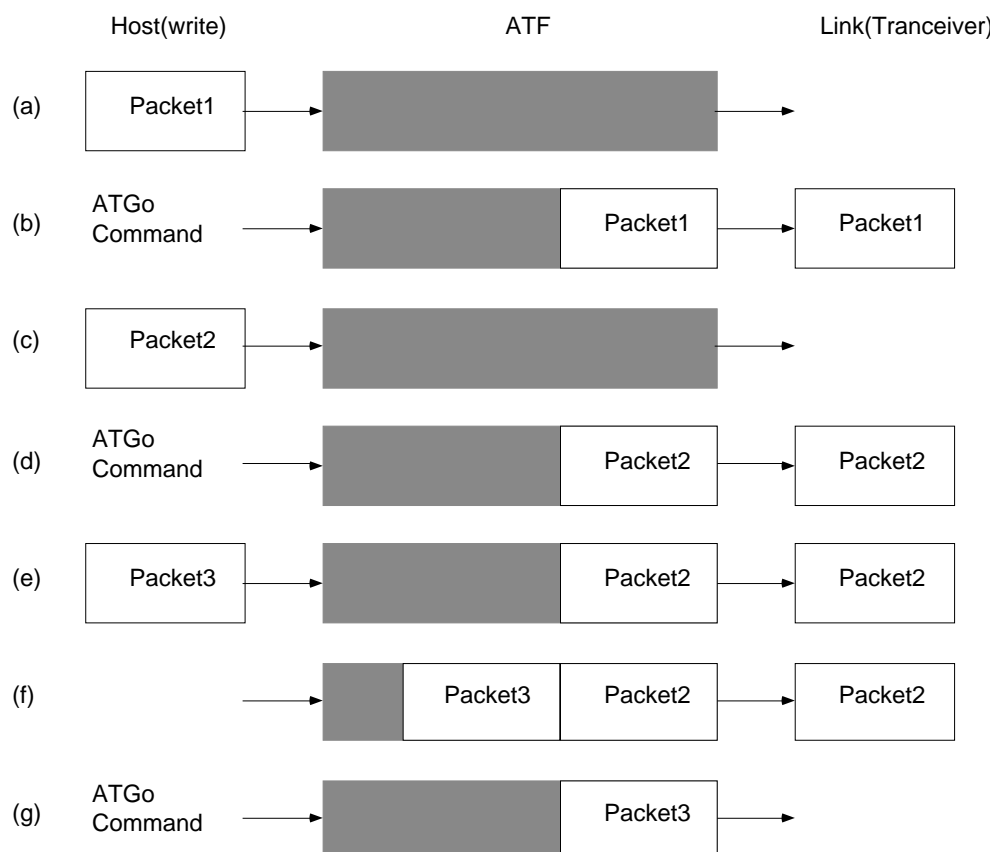


Figure 5-3-8 Concept of ATF Operation

5-3-4-1-2 Reception Buffer

The asynchronous receive buffer ARF performs FIFO operation of the primary dimension. At the time point when all of one packet received has been written in the ARF by the receiver, ARxEnd interrupt occurs and the host is then allowed to read out this packet. Even though the host does not read out this packet at that time, write-in operation of the next receive packet from the receiver to the ARF is effected insofar as there is some vacancy in the ARF buffer. While this vacancy is available in the ARF buffer, it is possible to receive more data. If there is only vacancy that is smaller than one packet in the ARF buffer, a newly received packet cannot be written in this ARF buffer and the busy Ack code is returned to the source node to call for a retry for that packet. If the received packet contains any CRC error, such a packet cannot be written in the ARF buffer. In short, the packet data are stored in the ARF buffer only if correct reception has been accomplished. (See Fig. 5-3-9.)

If ARF reset is performed for the ResetARF in the Reset register, the ARF is restored to its initial state and all data are lost. If the Full bit is active, a non-active mode is assumed.

When ARFBusReset of the control register is set at "1", the ARF buffer is flashed after the occurrence of BusReset. (See Fig. 5-3-10, 11.) If a read-out request is forwarded to the ARF buffer under the conditions that the ARF buffer is flashed and the first reception is attempted, "0x00E0" is read out.

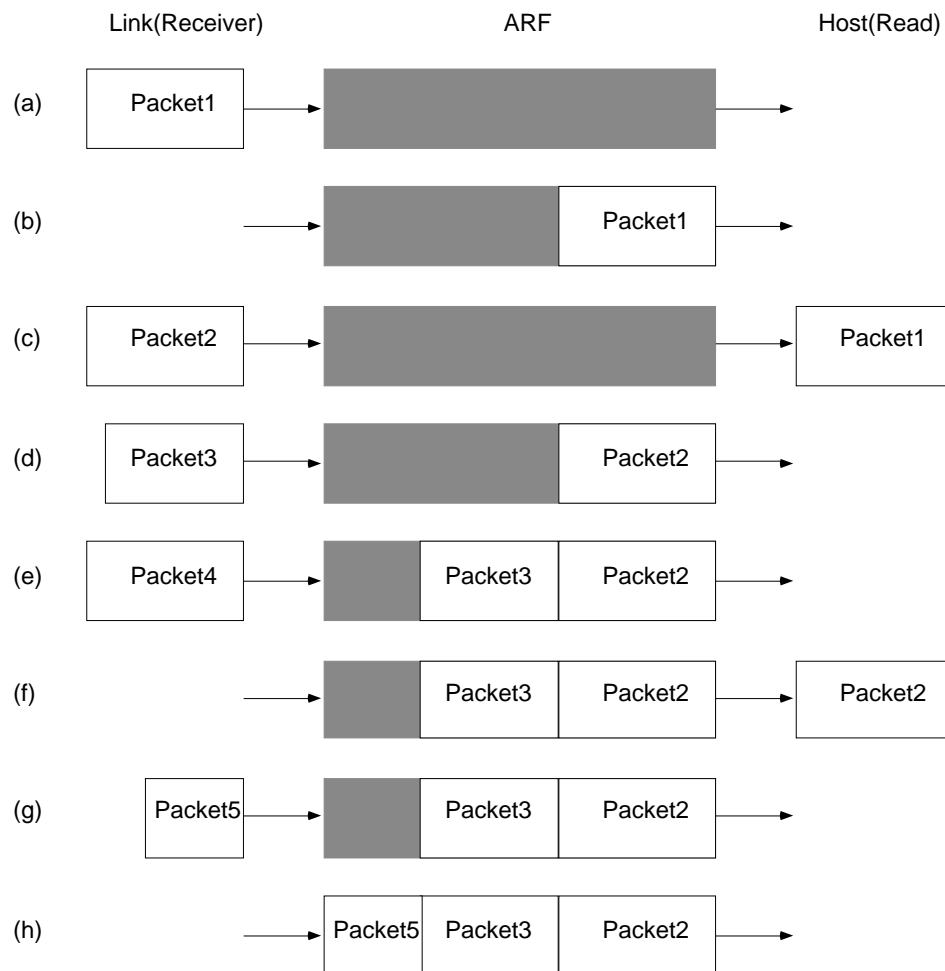


Figure 5-3-9 Concept of ARF Operation

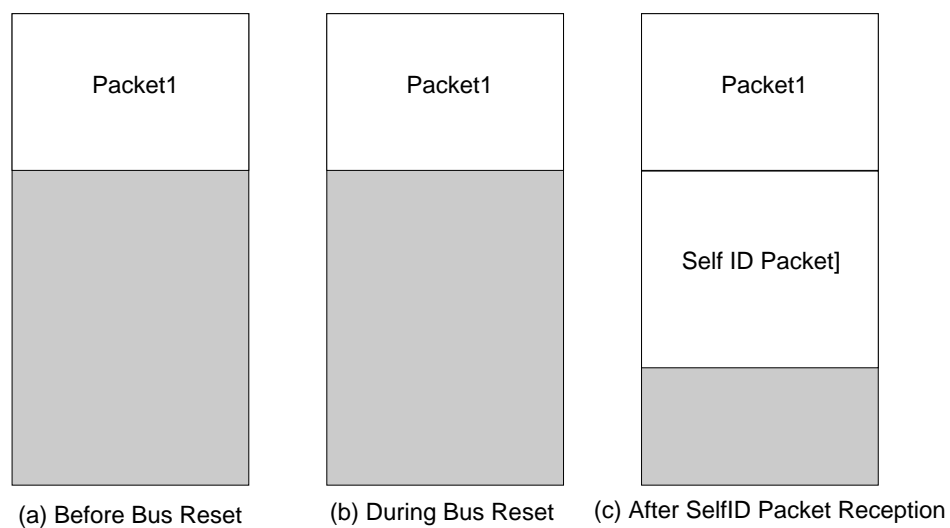


Figure 5-3-10 ARF Operation after BusReset (ARFBusReset="0")

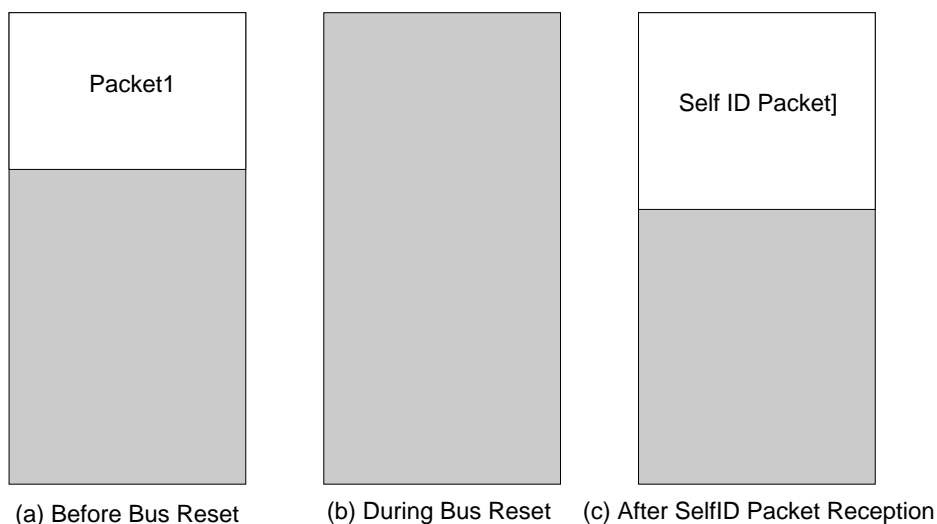


Figure 5-3-11 ARF Operation after BusReset (ARFBusReset="1")

5-6 32-bit CRC

As stipulated by IEEE 1394 Draft, the MD8413 sends out the packet data whose header block and data block are attached with CRC of 32 bits. During reception, CRC is calculated according to the received data at the header and data blocks. Comparison is made with the CRC data attached to the received packet. If there is any failure in coincidence, such announcement is sent to the HdrErr bit of the Interrupt register or the AckStatus bit of the Diagnostic Status register.

As a CRC polynomial, the following expression is employed:

$$X^{32} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} \\ + X^9 + X^6 + X^5 + X^4 + X^3 + X + 1$$

5-7 Control Flow

TBD

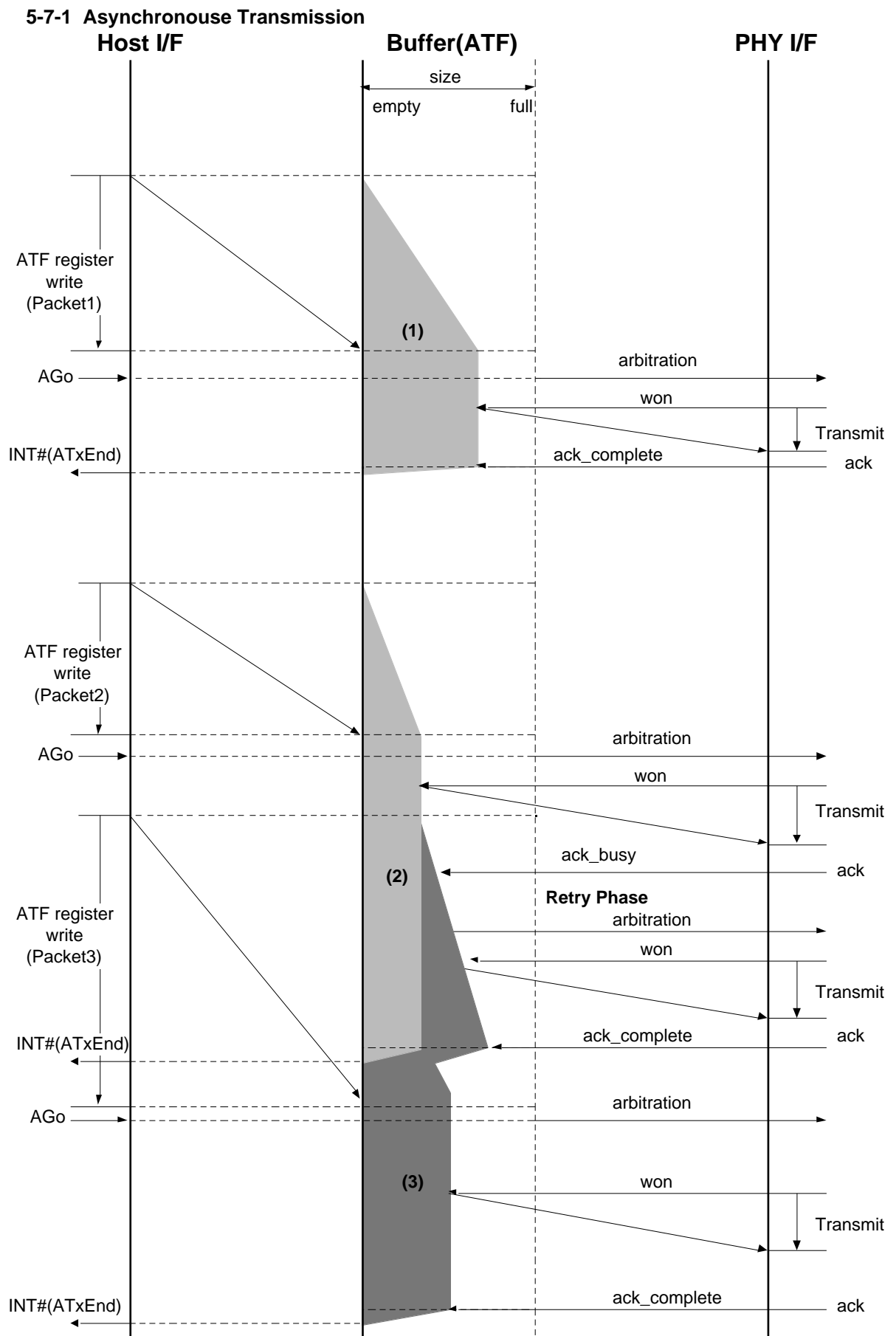


Figure 5-7-1 ATF Transmission Flow 1

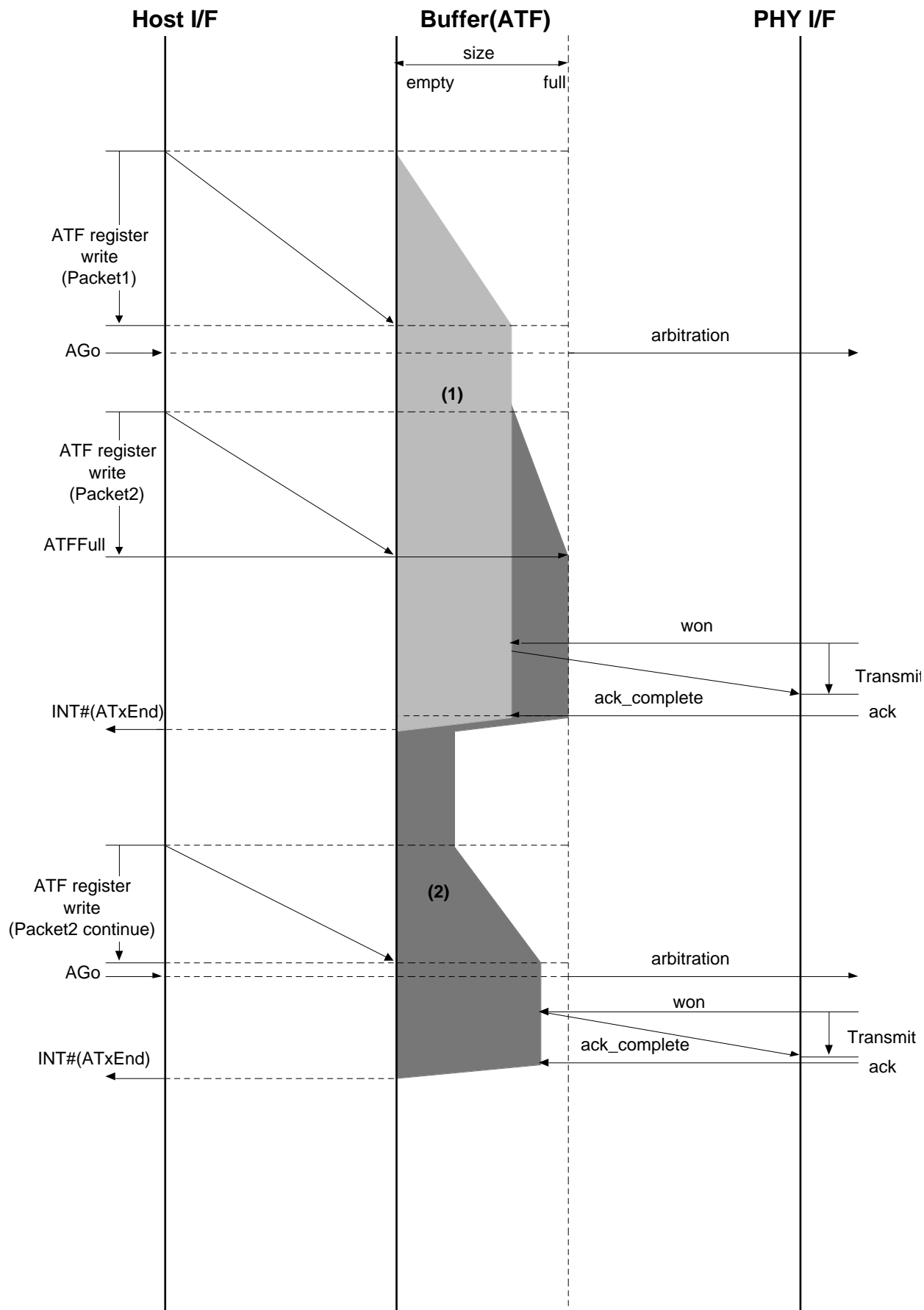


Figure 5-7-2 ATF Transmission Flow 2

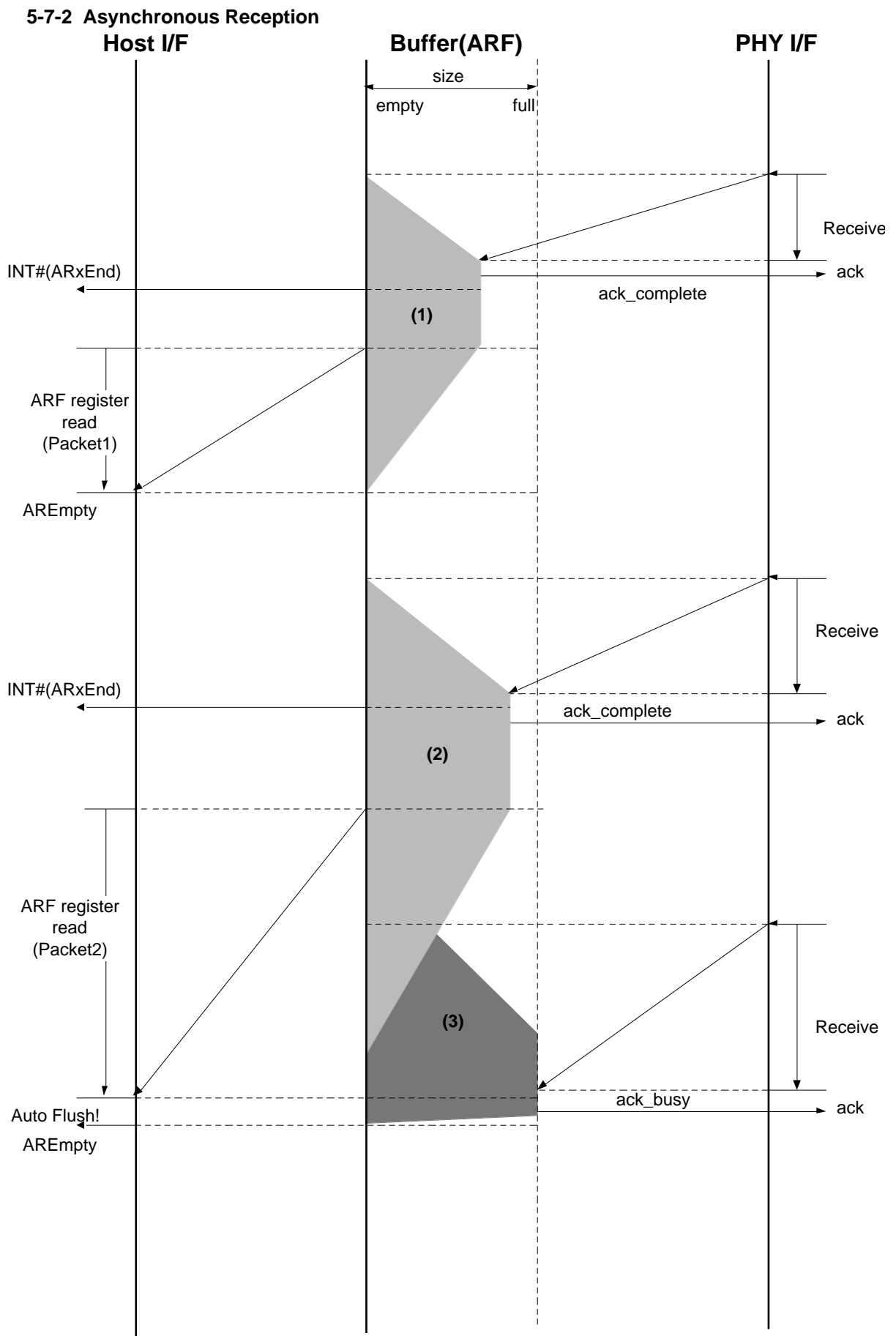


Figure 5-7-3 ARF Reception Flow 1

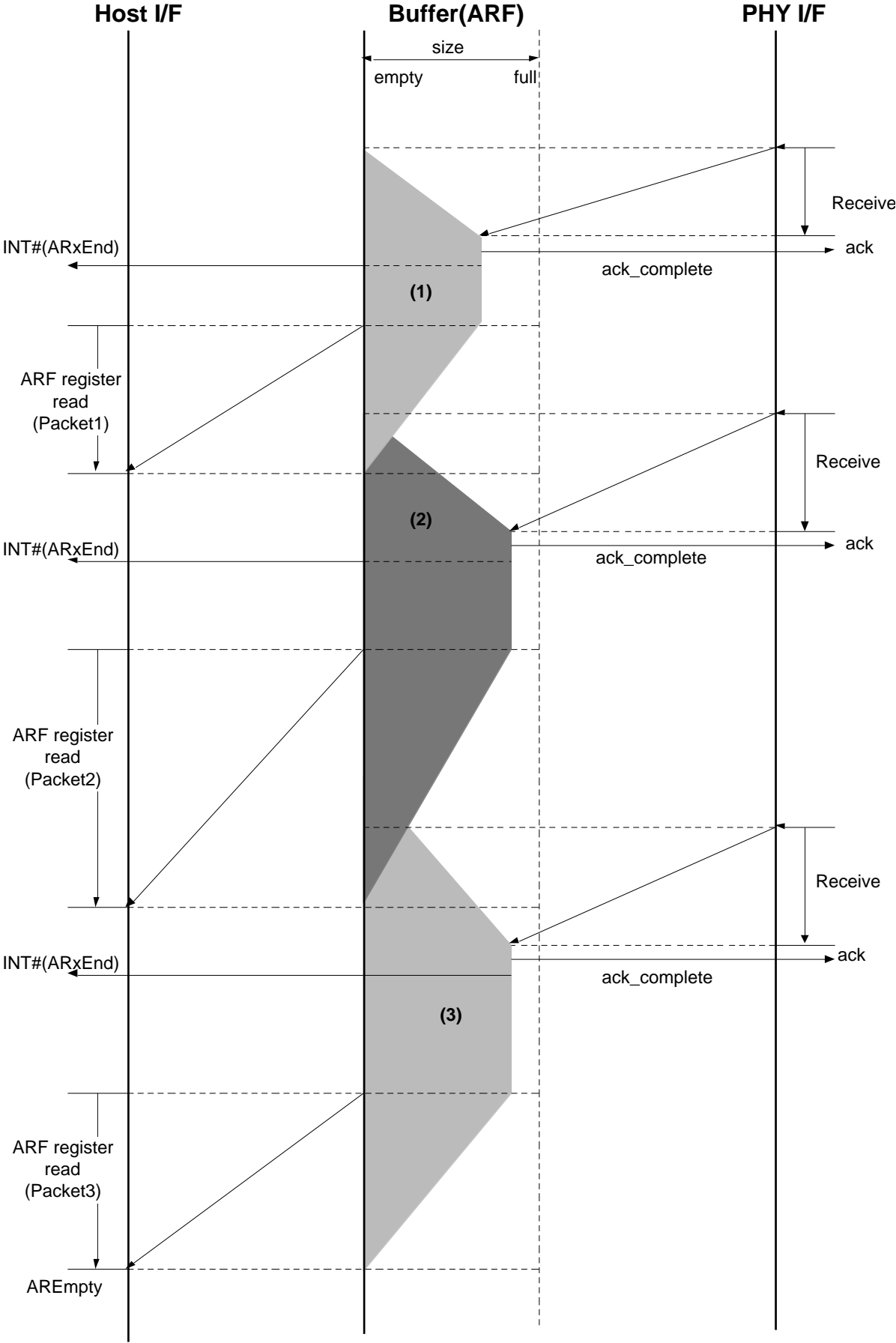


Figure 5-7-4 ARF Reception Flow 2

The table below shows the interrupt and status announcements regarding the receiving conditions achieved by the above flow.

Status	FIFO is full in the middle of reception and normal reception is impossible		Normal reception achieved
	ARF vacancy 4 Quadlet or below at the start of reception	ARF vacancy 5 Quadlet or below at the start of reception	
ARxEnd Interrupt	0	0	1
ARFRej Interrupt	1	1	0
ARF condition	Same status as that before reception; Nothing written	Same status as that before reception; Nothing written	All saved

Table 5-7-1 Interrupt and FIFO Conditions for ARF Reception

6 Processing
TBD

TBD

7 Processing for BusReset

The processing flow after bus reset is explained.

7-1 After Closure of POWER Switch

The following processing steps are followed:

1. LinkOn bit setting

TBD

7-2 Processing after Bus Reset

The TransmitterEn bit is retained.

When the root bit is set and the CycleMaster bit is also set, transmission of CycleStart Packet is immediately started.

Additional explanation of ATF, ARF processing

TBD

8 Exclusive Isochronous Bus

The MD8413 handles isochronous data in conjunction with the external system via the exclusive bus of IDATA(15:0).

The MD8413 is turned to be a master at any time, and it performs synchronous transmission using a variety of control signals, making a data input request from the outside for transmission and a data output request to the outside for reception.

Since the MD8413 does not have any internal buffer for isochronous packets, the external system is required to take action without fail according to each data input request from the MD8413 for transmission. Also in the case of reception, the external system is required to obtain data with an output timing from the MD8413. Transmission control in the packet unit is effected with the ITREQ# signal from the external system.

The data transfer rate of a packet, where isochronous data with the external system are located, is SCLK/8 for both transmission and reception if this packet is for 100Mbps. This rate is SCLK/4 if the packet is for 200Mbps. SCLK is a system clock of the MD8413 entered from PHY.

8-1 Isochronous Cycle Start Timing

The isochronous cycle is started at the intervals of 125μsec. Because of interrupt by asynchronous packets, however, actual cycle start has some jitter. As a signal of indicating the start of actual isochronous cycle, the MD8413 generates an output of ICS signal. The ICS signal is asserted for 4 clocks of ICLK.

A transmission request is made based on this ICS signal, and the successive isochronous cycle. Data output is also generated during reception if there is a receive packet preceded by ICS.

8-2 Request-to-Send Processing

When the isochronous source of the external system makes a request to send a packet to the MD8413, this request is raised toward the MD8413 using the ITREQ# signal in the first place. When ITREQ# is asserted, the MD8413 identifies the occurrence of a request from the outside to send a packet, and recognizes the end of this request in the cycle by examining the negate data.

This identification is effected under the condition that the ITREQ# signal is asserted in the enable period of the

ICS signal. As shown in Fig. 8-2, information of ITREQ# assert is picked up with any one of ICLK 1, 2, 3, and 4 while ICS is in the enable period. According to an example of Fig. 8-2, ITREQ# assert is identified with ICLK 2. Using the isochronous cycle started shortly after the presentation of the ICS signal, the MD8413 executes the packet transmit request by actuating the PHY device. At the time point when arbitration is prevalent on the bus, the MD8413 sends out a data request toward the external system using the ITX# signal. For actual data request at that time, the MD8413 sends out a request of data pre-read operation toward the external system for the amount of 4 words (2 Quadlets) after the lapse of 1 ICLK clock from the rising point of ICLK that has identified the ITREQ# being asserted. Therefore, regardless of whether the arbitration is acquired, the MD8413 always makes a request for data pre-read operation. Consequently, the external system is required to provide for at least 2 Quadlets (4 words) of data until ITREQ# is asserted and this is identified in the ICS period. Transmission packet data on the IDATA bus are picked up at the rising point of ICLK during the ITX# enabled period. According to the example in the figure, Iso-U(1) of the initial data is picked up at the rising point of ICLK 4.

To finish a packet, IEOP# from the external system is asserted in conjunction with the ITX# timing when the last data request is made for the packet. This IEOP# assert is identified with the rising point of ICLK in the ITX# enable period of the last data, similarly as for packet data pickup timing.

In the case of packet transmission only with an isochronous header and "0" for data payload, IEOP# is asserted at the second word out of one Quadlet (2 words) of the header, and presence of a vacant packet of data is shown to the MD8413. Thus, the MD8413 does not place a request for data pre-read operation of these two words, and packet transmission for the header only is effected.

Handling for transmission is the same as for isochronous normal mode and auto mode. Only difference is that contents of data for data pre-read operation in normal mode are given by the first Quadlet in the isochronous header and the payload area. They are given by the two Quadlets of the payload area in auto mode.

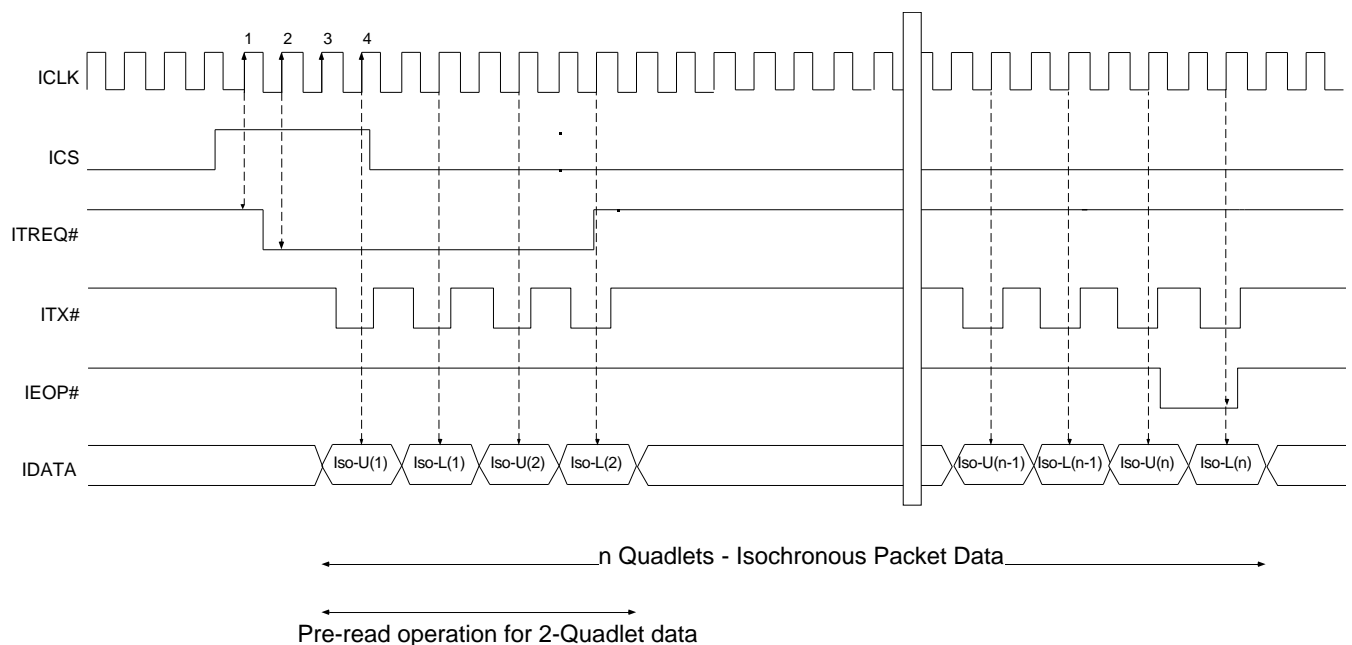


Figure 8-2 Isochronous Transmission Timing

8-3 Processing for Multi-Channel Transmission

Fig. 8-3 shows an example multi-channel (multiple packets) transmission using a certain isochronous cycle. As shown, ITREQ# is asserted in the enable period of the first (Isochronous Packet Data (1)) IEOP#, and the MD8413 identifies the presence of the next transmit packet according to this fact. When this has been identified, the MD8413 performs pre-read operation for the next packet data with the timing shown (period of pre-read for Isochronous Packet Data (2)). In the same manner as described in 8-2, a packet data request is successively forwarded to the external system at the time point when the arbitration is prevalent after pre-read operation. In the example of the figure, transmission of two packets is effected and then ITREQ# is negated with IEOP# of Isochronous Packet Data (2) to complete that cycle, because packet transmission is finished in the period of Isochronous Cycle (N).

For multiple packet transmission as described, ITREQ# is kept asserted and this action is finished by negating ITREQ# with IEOP# of the last packet.

When ITREQ# is once negated in the enable period of IEOP# in an isochronous cycle, the MD8413 identifies it as the end of transmission of this cycle at the negate time point and finishes this cycle, even though another assert is retired. When this assert condition is maintained until presentation of the next ICS, this is recognized as a request for transmission of the next isochronous cycle.

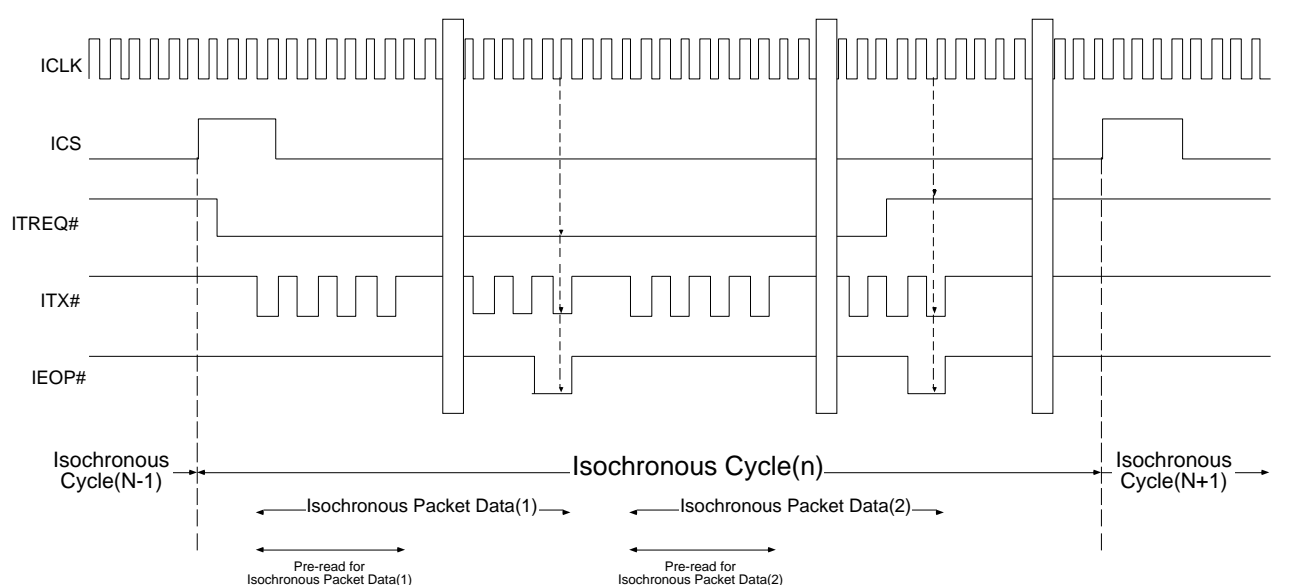


Figure 8-3 Multi-Channel Isochronous Transmission Timing

8-4 Processing for Reception

With IsoMode in the Control Register and the contents of Isochronous Receive Configuration Register, reception of an isochronous packet is successively started after the generation of a Cycle Start packet. The start of a receive packet is indicated at the external system by asserting IRCV#. Until reception of this packet is finished, IRCV# is kept asserted. In other words, IRCV# asserted shows that a packet is being output. In the assert period for IRCV#, the both way IDATA bus is in the output condition.

After IRCV# assert, isochronous receive packet data are output from the IDATA bus in synchronization with IRX# asserted.

When IRCV# is asserted, the MD8413 continues to output packet data. Therefore, the external system must be arranged so that these data can be picked up without fail.

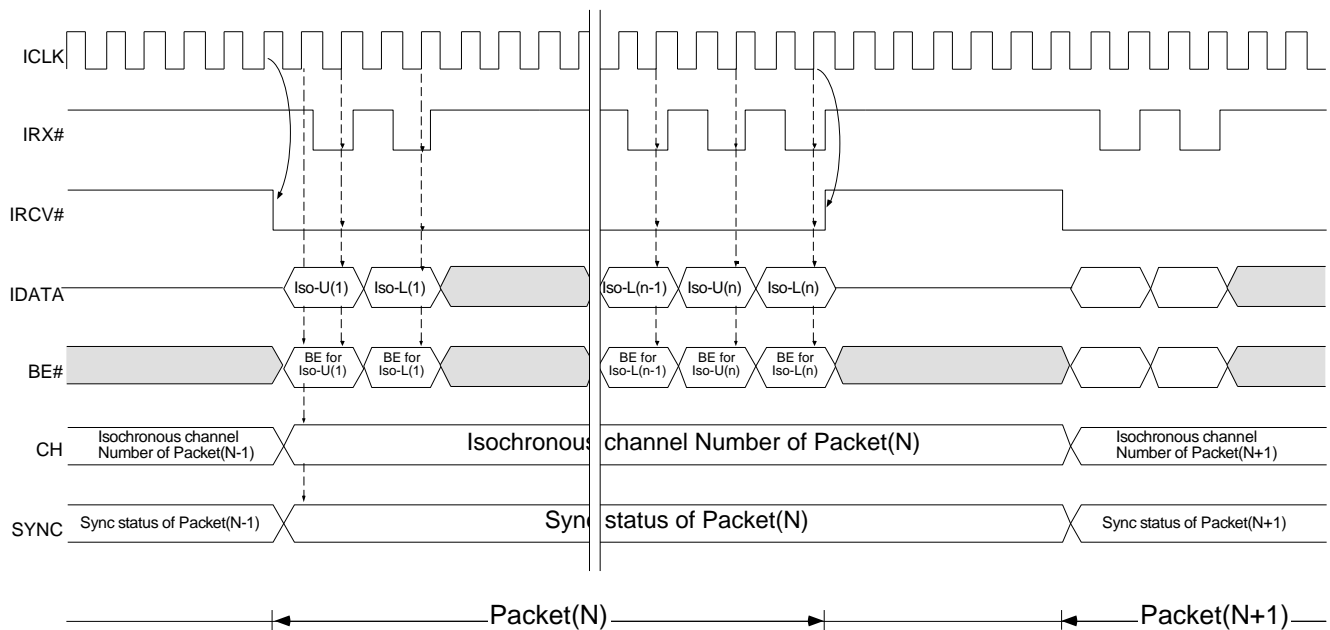


Figure 8-4 Isochronous Reception Timing

8-4-1 BE# Signal

It is possible to know the byte position of zero padding in the payload area of the received packet, using the BE# signal in the unit of upper 8-bit and lower 8-bit. BE# is output, synchronized with a data output on the IDATA bus. BE#(1) shows data of IDATA(15:8) and BE#(0) shows data of IDATA(7:0). BE#="0" indicates valid data and BE#="1" shows a padding byte. The MD8413 identifies zero padding according to the length value in the header (Length) and the Quadlet number of the packet payload (Quadlet), when the Length value is in the relationship of $(\text{Quadlet}-1) < \text{Length}/4 < \text{Quadlet}$.

8-4-2 CH Signal

The channel number of the received isochronous packet can be indirectly known from the CH signal. This value is valid only for reception setting for a maximum of 4 channels in IsoMode of the Control register. (When the lower bit of IsoMode is "0".) In other cases, an indefinite value is output. At the time point when IRCV# is asserted, the Isochronous Receive Configuration Register number is shown corresponding to that packet. This condition is maintained until the next IRCV# is asserted (next packet reception). CH="00" shows Isochronous Receive Configuration Register-1, CH="01" shows -2, CH="10" shows -3, and CH="11" shows -4. It is therefore possible to know the channel indirectly, set with the Isochronous Receive Configuration Register.

8-4-3 SYNC Signal

According to the respective data in the SYNC area in the Isochronous header of the received packet and those set with the Isochronous Receive Configuration Register, it is possible to know the status with the SYNC signal, meeting the requirements shown below.

SYNC Values

"01" : When the StartSync value set in the Register coincides with the SYNC value in the packet header.

"10" : When the StopSync value set in the Register coincides with the SYNC value in the packet header.

"11" : When the StartSync value set in the Register coincides with the SYNC value in the packet header, and further coincides with the StopSync value.

"00" : Conditions other than the above.

At the time point when IRCV# is asserted, the above conditional values are output according to that packet.

This condition is retained until the next IRCV# is asserted (next packet reception).

8-5 Reception of CycleStartPacket

When the node is of root and the MD8413 is sending a CycleStart packet, the MD8413 provides output to the IDATA bus only for the Cycle_Time_Data field in the packet. The same operation is performed when the MD8413 receives a Cycle Start packet in the non-root mode. As shown in Fig. 8-5, the external system identifies the condition with the CT signal enabled that Cycle_Time_Data is output on the IDATA bus. Each Cycle_Time_Data block of 32 bits is output twice to the IDATA bus by dividing it into two blocks, each in 16-bit bus width. Accuracy of each Cycle_Time_Data spacing of the first output data is relatively the same as the timing accuracy when the cycle timer in the MD8413 is updated with Cycle_Time_Data. Accordingly, the external system can construct a local cycle timer with the same accuracy as for the cycle timer in the MD8413, based on the output timing of the CT signal.

(As shown in Fig. 8-5, Delta t (=t2-t1) being a spacing from t2 to t1 offers the same accuracy as for the one in the MD8413.)

According to this function of the MD8413, the external system can use a cycle timer which provides a bus time for the 1394 bus. For example, time-stamp processing becomes possible.

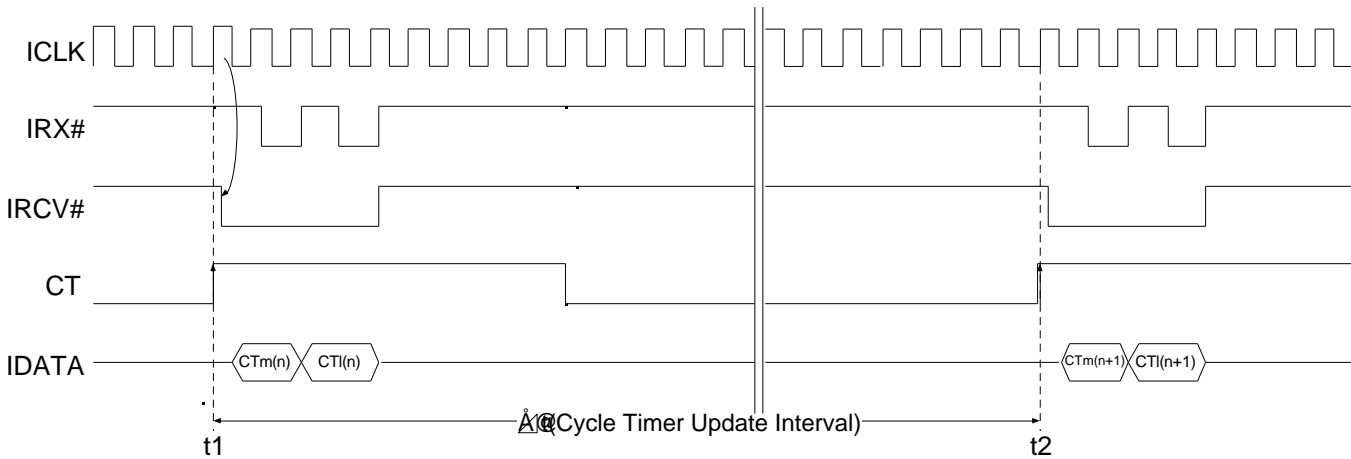


Figure 8-5 Cycle_Time_Data Output Timing

Cycle_Time_Data in the Cycle Start packet appearing on the IDATA bus in Fig. 8-5 corresponds to a format for CTm in Table 8-1 and one for CTI in Table 8-2.

IDATA(15:0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
second_count								cycle_count							

Table 8-1 Contents of CTm

IDATA(15:0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
cycle_count				cycle_offset											

Table 8-2 Contents of CTI

8-6 Packet Error Announcement for Reception

When an isochronous packet is received, and if this reception is unusual due to CRC error or any defect in the packet, the MD8413 sends out information of such a packet error to the external system, by asserting the IRERR# signal. With this IRERR# signal, the external system can abandon a packet that is suffering from an error.

8-6-1 Error Announcement for Cycle Start Packet

Regarding announcement of an error in the Cycle Start packet, an ordinary CRC error is indicated by the IRERR# signal after the lapse of 8 clocks of ICLK after the CT signal has been asserted as shown in Fig. 8-6-1. Even though there is no occurrence of a CRC error, the CT signal is asserted till the last timing for the occurrence of an error in the Cycle Start packet. (For 9 ICLK clocks) An error such as Cycle Start packet defect, etc., accompanies the appearance of IRERR# before this timing, but IRERR# occurring in the enable period of CT signal is always regarded as an error in the Cycle Start packet.

Therefore, when updating a local Cycle Timer counter using this Cycle Timer value from the external system, it is possible to avoid updating with a cycle timer value in the faulty Cycle Start packet, by loading the cycle timer value at the falling timing of the CT signal and updating the Cycle Timer counter under the condition that no IRERR# has occurred in the assert period of the CT signal.

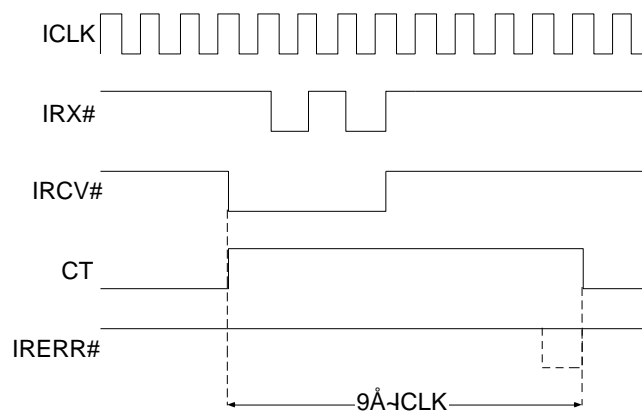


Figure 8-6-1 Error Timing for Cycle Start Packet

8-6-2 Error Announcement for Isochronous Packet

According to errors, such as CRC error of the header/payload, discrepancy between length value in the header and data number in actual packet payload, lack of data in the header, mid-lack of payload, etc., the appearance pattern of IRERR# can differ in many ways. Whether a packet being received during IRCV# assertion is encountering an error or not is known in the period after the assertion of IRCV# or the negation of IRCV# of the packet and before the assertion of IRCV# in the next packet received. The relationship among IRX#, IRCV#, and IRERR# is shown by the patterns in Fig. 8-6-2. In Pattern (1), IRCV# and IRERR# are simultaneously asserted and reception of this packet is finished when IRCV# is negated without the assertion of IRX#. In this case, the error pattern indicates that reception is finished only with the first Quadlet of the packet. Reception of isochronous packet header itself is also ended on the way, without attaining the specified number of quadlets. In Patterns (2) and (3), there is a header CRC check error, lack of a packet, etc. during reception. In Pattern (4), this is mainly a CRC check error in the payload area and IRERR# is asserted.

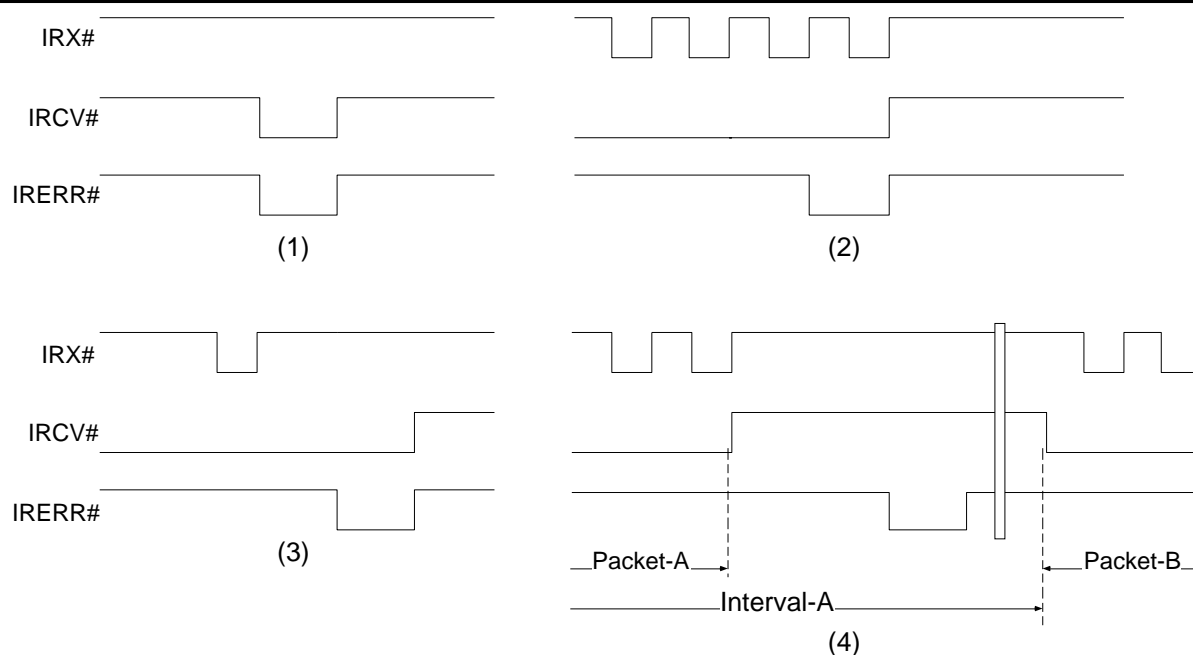


Figure 8-6-2 Patterns of IRERR# Appearance

8-7 Discrepancy in Timing between 100MHz and 200MHz

For packet reception at 100MHz and 200MHz, timing is different as shown in Fig. 8-7 as a matter of course. A packet received from the IDATA bus at a speed of 200MHz is generally output at the intervals of 2 clocks (12.5MHz) for ICLK, or at the intervals of 4 clocks (6.25MHz) when received at 100MHz. At 100Mbps in Fig. 8-7, a Quadlet of 2 words (16-bit) is output at the intervals of 2 clocks for ICLK.

Due to the overhead caused by calculation of header CRC, some timing may have more spacing.

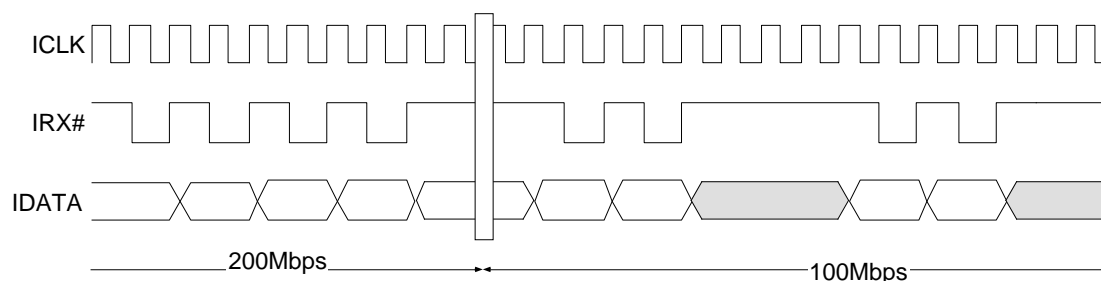





Figure 8-7 100/200Mbps Timing

8-8 Example Isochronous Bus Timing

Example bus timings are shown in Figs. 8-8-1 and 8-8-2. Each example will be explained below.

On the IDATA both way bus, Mark  shows a condition of input into the MD8413, Mark  shows a condition of output from the MD8413, and Mark  shows a condition of “don't care”.

Contents of the 1394 Bus Status are described for easy understanding of the figures, and timing with signals of ICLK or below are not very accurate.

8-8-1 Example Receive Timing

Fig. 8-8-1 shows an example timing for transmission. In this example, the starting ICS of an isochronous cycle is asserted and the system performs transmission, starting with this cycle. The MD8413 makes a pre-read request for 2 Quadlets of Packet-A data. Succeeding the ICS, only Cycle_Time_Data in the Cycle Start packet is output by the CT toward the outside. When the external system intends to use this value, no generation of

IRERR# until the negate timing of the CT signal is confirmed, and then the Cycle Time counter of the external system is updated. Since then, with permission of transmission from the PHY device, remaining transmit data are read from the external system and these data are transferred to the PHY. Information about the end of the packet is sent from the external system to the MD8413 with IEOP#, and transmission of Packet-A is finished. If further transmission of a packet is intended through a different channel in the isochronous cycle at that time, ITREQ# is kept asserted. As a result, the MD8413 continues to perform pre-read of Packet-B that is the next packet. Upon completion of data transmission for Packet-B, and if there is no transmit packet in that cycle, ITREQ# is negated before the timing of IEOP# for Packet-B and such a condition is sent to the MD8413.

8-8-2 Example Receive Timing

Fig. 8-8-2 shows an example timing for reception. In this example, the two packets of Channel-A and Channel-B are successively received in an isochronous cycle. At that time, valid or invalid of the upper/lower bytes of data on each IDATA bus is indicated by the BE# signal. Synchronized with the fall of IRCV#, information about the channel and SYNC in the header of the subsequently output receive-packet data is sent to the external system in the form of CH and SYNC signals. After the reception of Packet-B, the transmit packet of Packet-C (pre-read of packet data already finished for 2 Quadlets) is sent to the bus, according to the request previously provided by the external system. As the next packet is sent in the cycle by the external system, and since ITREQ# is also asserted on IEOP# of Packet-C, the MD8413 makes a pre-read request for the Packet-D. A receive packet of Packet-E is in higher preference than Packet-D on the bus. As such, the MD8413 performs the related processing for reception.

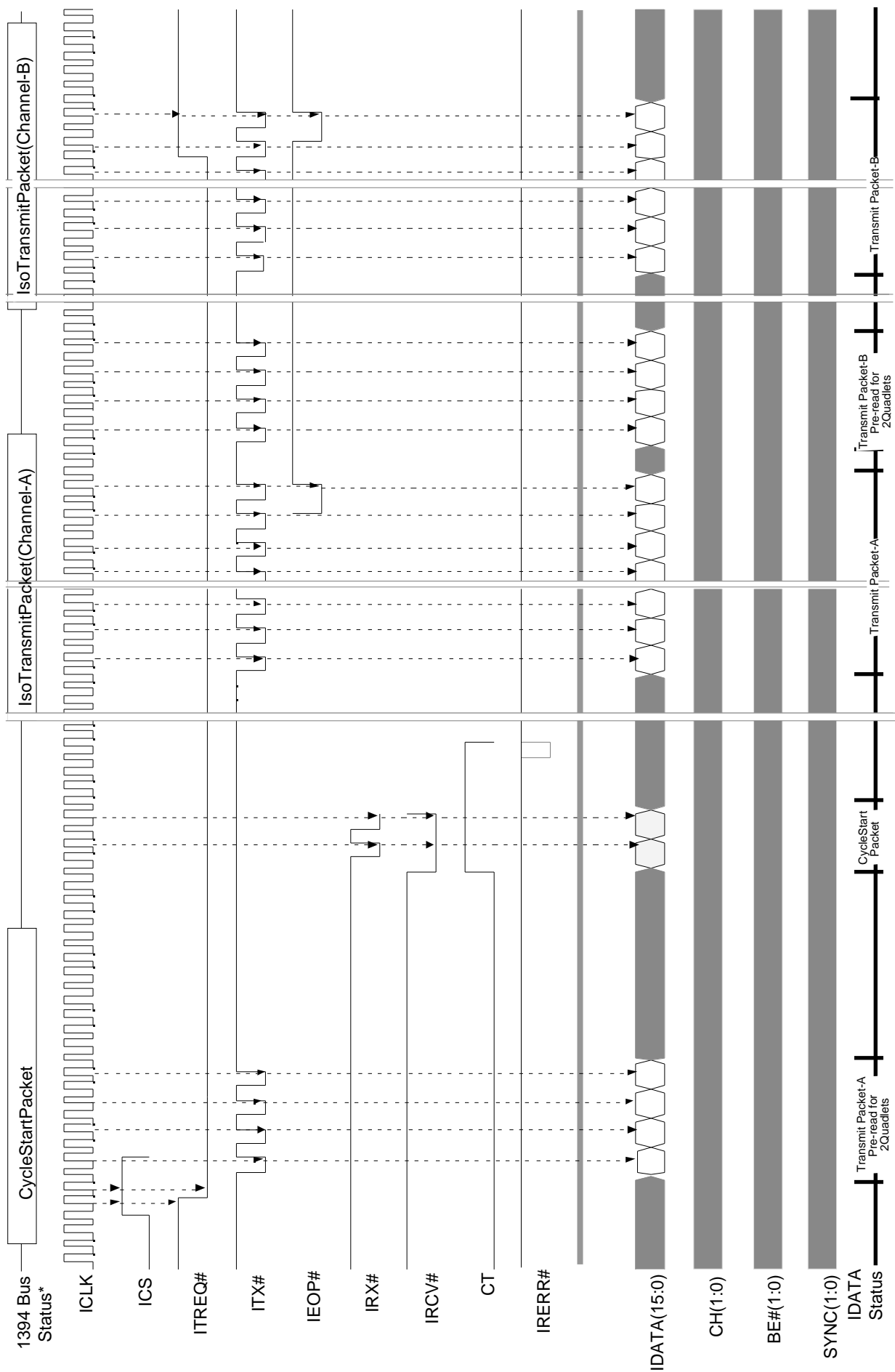


Figure8-8-1 Isochronous Bus Timing (1)

Figure 8-8-2 Isochronous Bus Timing (2)

9 Electric Characteristics

9-1 Absolute Maximum Rating

(VSS = 0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	-0.3~+7.0	V
VIN	Input voltage	-0.3~VDD+0.3	V
IIN	Input current	±10	mA
TSTG	Storage temp.	-40~+125	°C

9-2 Recommended Operating Condition

(Vss=0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	3.00~ 3.60	V
VIN	INput voltage	0 ~ VDD	V
TA	Ambient temp.	0 ~ + 70	°C

9-3 DC Characteristics

DC characteristics under the recommended conditions except special mention.

(VSS = 0V)

Symbol	Item	Terminal	Test condition	MIN	TYP	MAX	Unit
VIH	Input high voltage	SCLK,CTL,D		VDD-0.7			V
		Except above		2.0			
VIL	Input low voltage	SCLK,CTL,D				VSS+0.7	V
		Except above				0.8	
IIH	Input high current		VIN=VDD	-10		10	μA
IIL	Input low current		VIN=VSS	-10		10	μA
VOH	Output high voltage	LPS,LREQ,CTL,D	IOH= -12mA	2.4			V
		Except above	IOH=-8mA	2.4			
VOL	Output low voltage	LPS,LREQ,CTL,D	IOL= 12mA			0.5	V
		Except above	IOL= 8mA			0.5	
IOZ	Output diable current		VOUT = VDD or VSS	-10		10	μA
IDD	Dynamic power supply current	VDD	VDD=3.3V				mA

9-4 AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit
T _{CSS}	CS#,DACK# setup time	5			nS
T _{CSWH}	CS#,DACK# holding time(while WRITE)	0			nS
T _{CSRH}	CS#,DACK# holding time(while READ)	0			nS
T _{DREQWD}	DREQ output lagging time(while WRITE)	18		54	nS
T _{DREQRD}	DREQ output lagging time(while READ)	18		54	nS
T _{TRW}	Read,write pulse width	60			nS
T _{TRWC}	Read,write cycle time	60			nS
T _{DTD}	Read data output lagging time	7		20	nS
T _{DTH}	Read data output holding time	3		14	nS
T _{WRDS}	Write data setup time	12			nS
T _{WRDH}	Write data holding time	2			nS
T _{RSW}	Reset pulse width	160			nS
T _{CYCD}	CYCLEOUT signal output lagging time	7		18	nS
T _{CYCC}	CYCLEIN signal cycle time		125		É S
T _{CYCH}	CYCLEOUT signal high level time		62.5		É S
T _{CYCL}	CYCLEOUT signal low level time		62.5		É S

(Load capacitance 50pF)

Table 9-4-1 Host interface AC characteristics

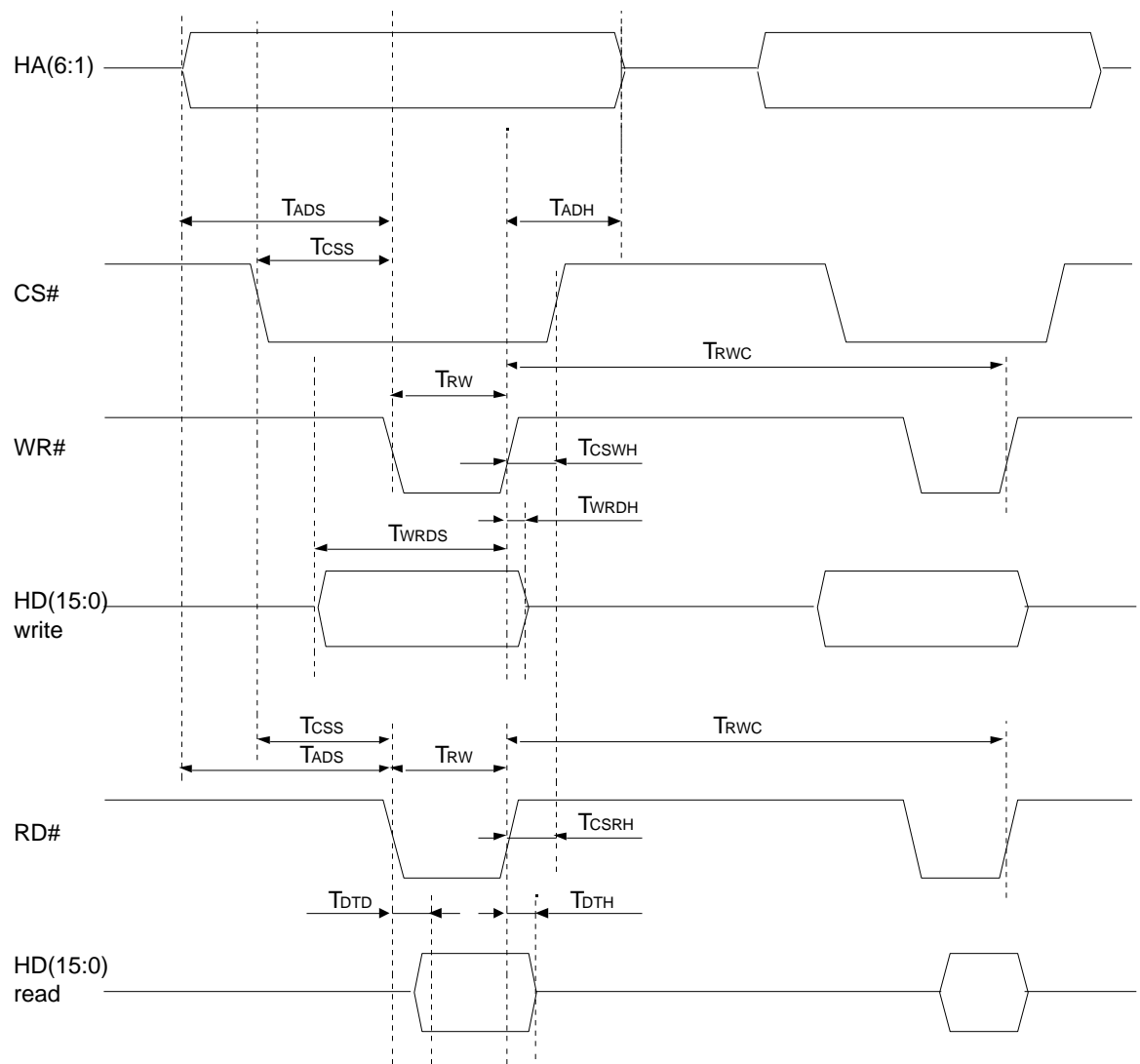


Figure 9-4-1 Host Interface AC Characteristics (Read / Write)

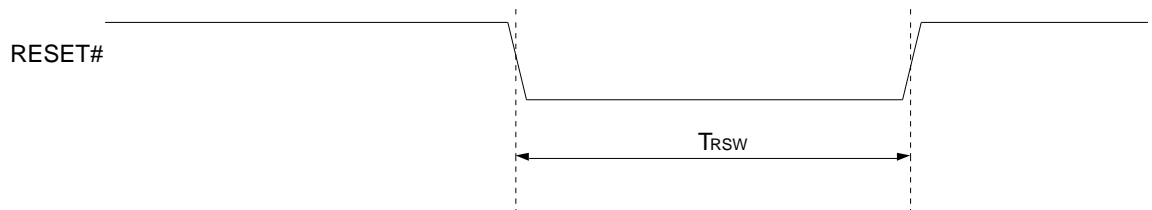


Figure 9-4-2 Host Interface AC Characteristics (Reset)

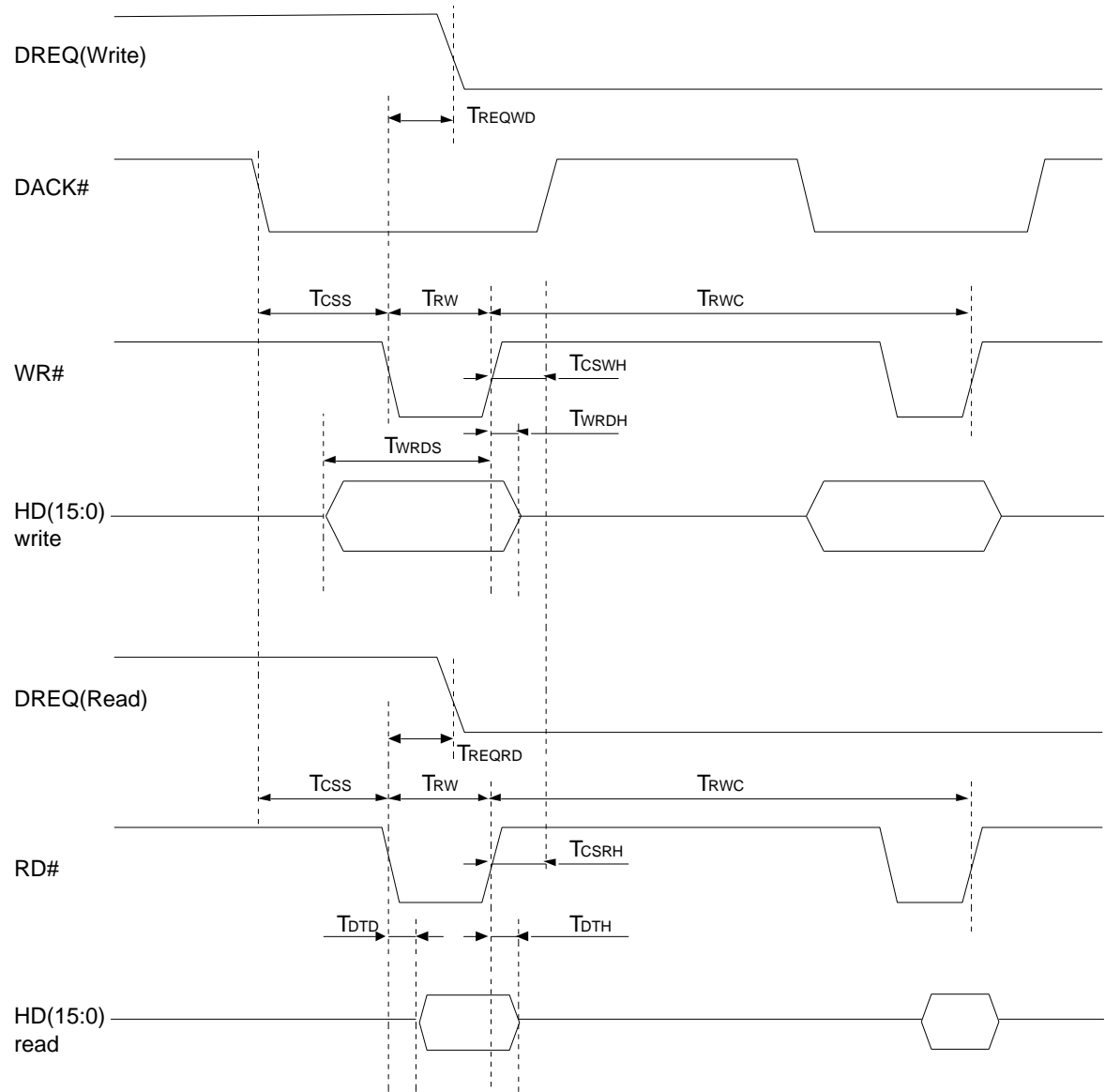


Figure 9-4-3 Host Interface AC Characteristics (DMA)

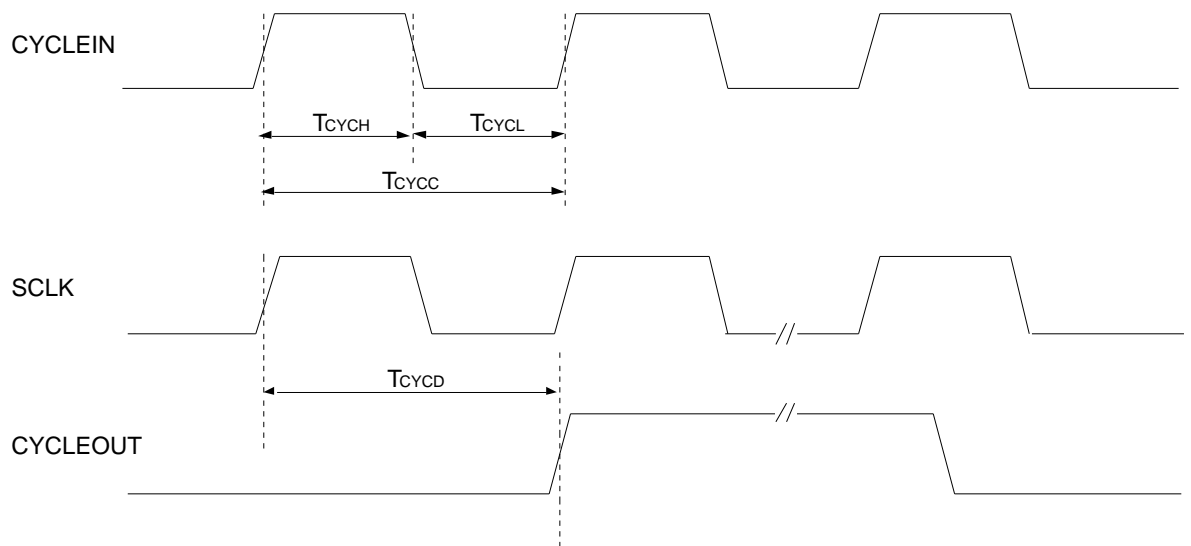


Figure 9-4-4 Host Interface AC Characteristics (CYCLEIN / OUT)

Symbol	Item	MIN	TYP	MAX	Unit
T_{CTD}	Control output lagging time	4		13	nS
T_{PDD}	PHY data Output lagging time	4		13	nS
T_{CTS}	Control Setup time	8			nS
T_{CTH}	Control Holding time	0			nS
T_{PDS}	PHY data setup time	8			nS
T_{PDH}	PHY data holding time	0			nS
T_{LRD}	LREQ data output lagging time	4		13	nS
T_{SCKC}	SCLK cycle time	20			nS
T_{SCKH}	SCLK high level time	8		12	nS
T_{SCKL}	SCLK low level time	8		12	nS
T_{LPSC}	LPS cycle time	360		570	nS
T_{LPSH}	LPS high level time	175		290	nS
T_{LPSL}	LPS low level time	175		290	nS

(Load capacitance 20pF)

Table 9-4-2 PHY Interface AC Characteristics

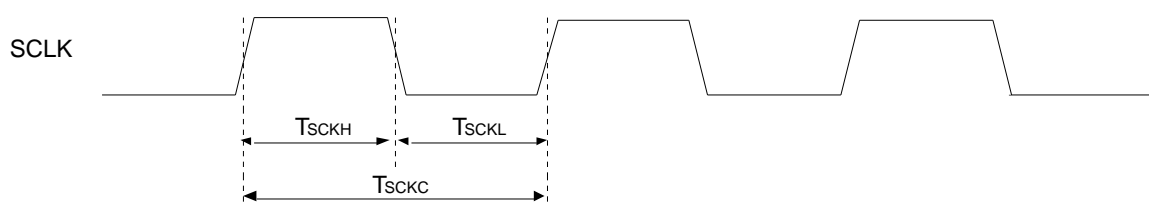


Figure 9-4-5 PHY Interface AC Characteristics (SCLK)

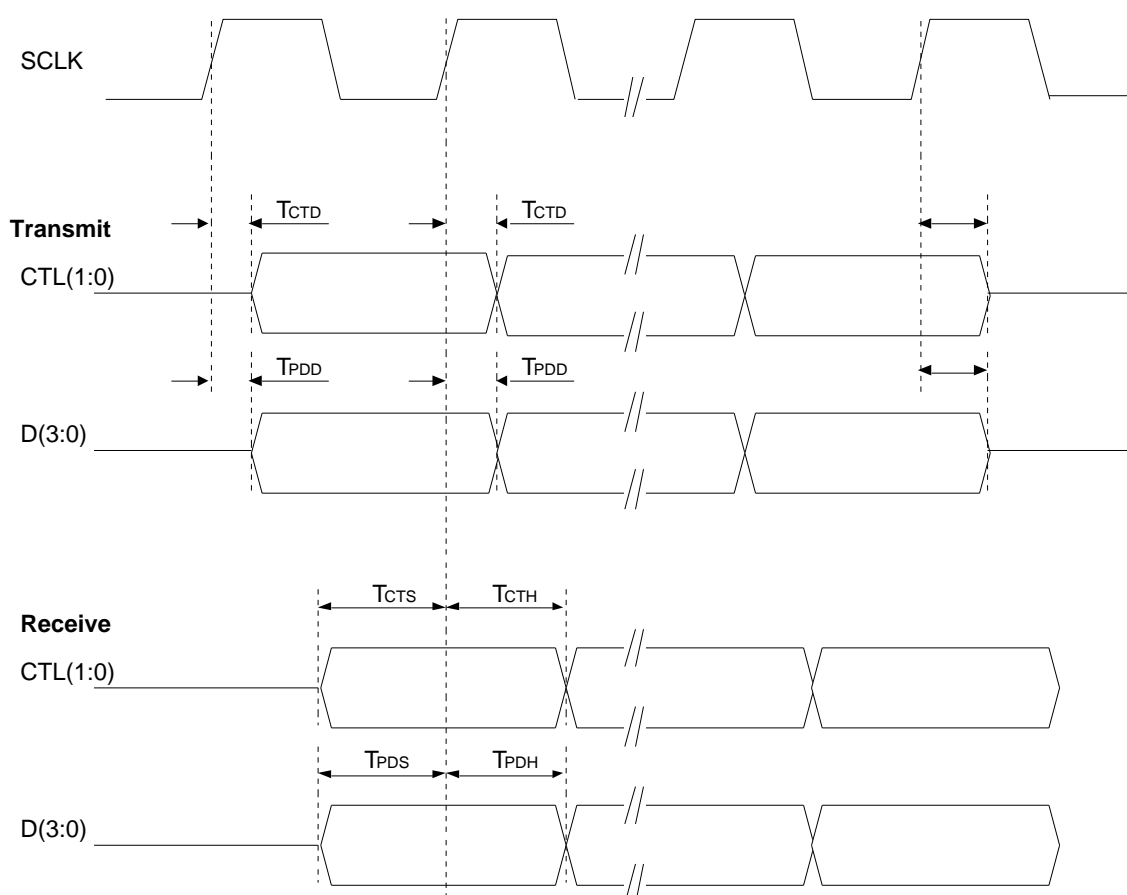


Figure 9-4-6 PHY Interface AC Characteristics (CTL, D)

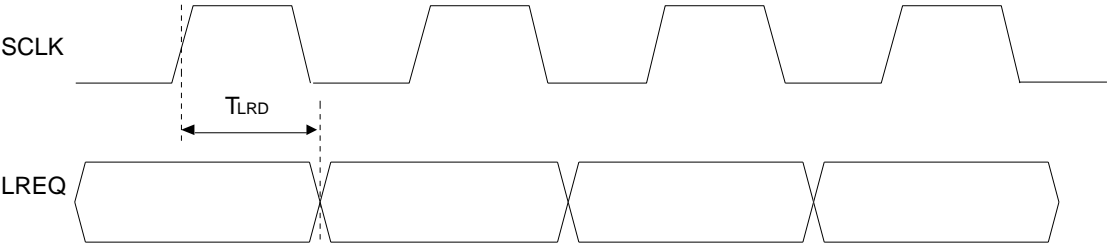


Figure 9-4-7 PHYInterface AC Characteristics (LREQ)

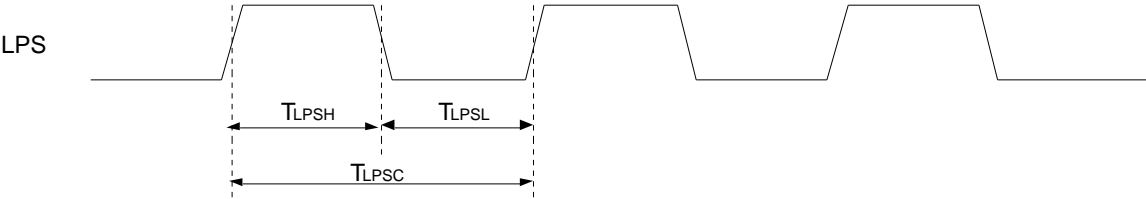


Figure 9-4-8 PHY Interface AC Characteristics (LPS)

Symbol	Item	MIN	TYP	MAX	Unit
T _{ICKD}	ICLK output lagging time	6		16	nS
T _{ICSD}	ICS output lagging time	1		8	nS
T _{ITRS}	ITREQ# setup time	20			nS
T _{ITRH}	ITREQ# holding time	0			nS
T _{ITXD}	ITX# output lagging time	1		8	nS
T _{IEPS}	IEOP# setup time	20			nS
T _{IEPH}	IEOP# holding time	0			nS
T _{IDTS}	IDATA[15:0] write Setup time	12			nS
T _{IDTH}	IDATA[15:0]write holding time	0			nS
T _{IRXD}	IRX# output lagging time	1		8	nS
T _{IRVD}	IRCV# output lagging time	1		8	nS
T _{IDFD}	IDATA[15:0] output lagging time(IRCV#)	18		26	nS
T _{IDTD}	IDATA[15:0] output lagging time(ICLK#)	2		14	nS
T _{IDRD}	IDATA[15:0] output holding time	0		8	nS
T _{BCSD}	BE#,CH,SYNC output lagging time	1		8	nS
T _{IERD}	IRERR# output lagging time	1		8	nS
T _{CTD}	CT output lagging time	1		8	nS
T _{IBRSTD}	BUSRST output lagging time	1		8	nS

(Load capacitance 50pF)

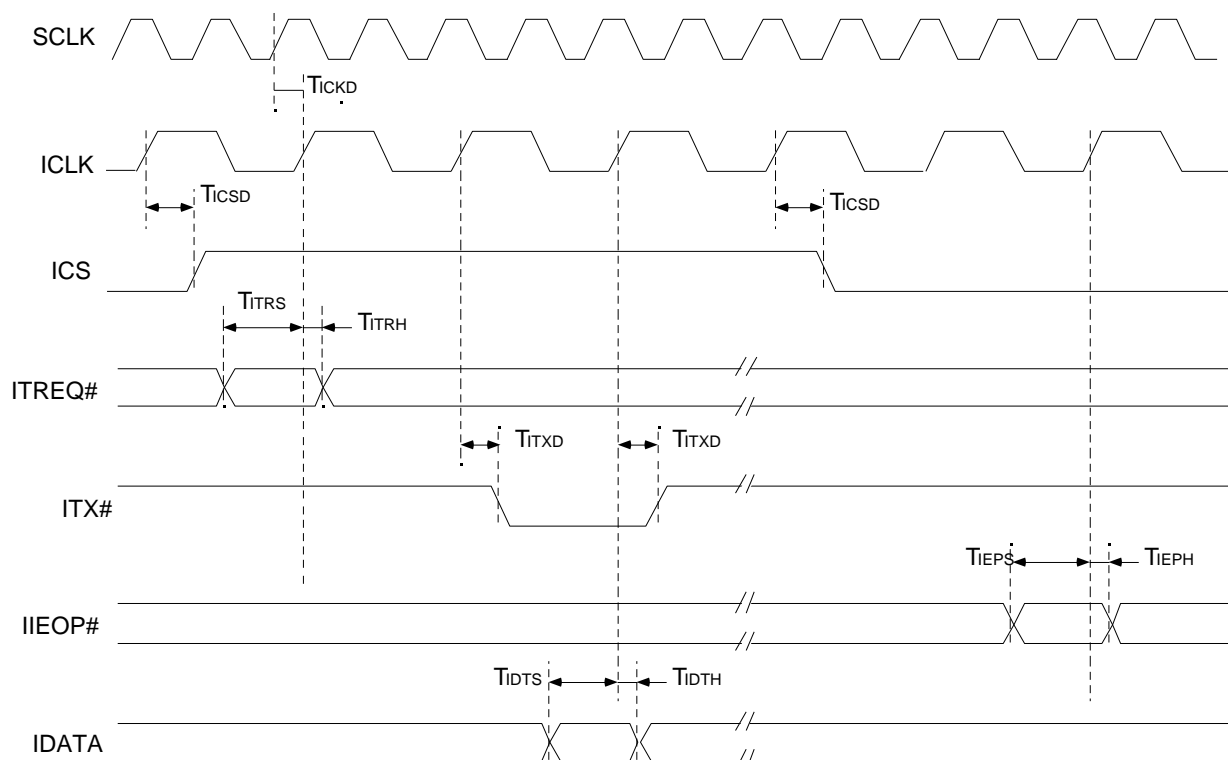


Table 9-4-9 Isochronous Bus AC Characteristics1

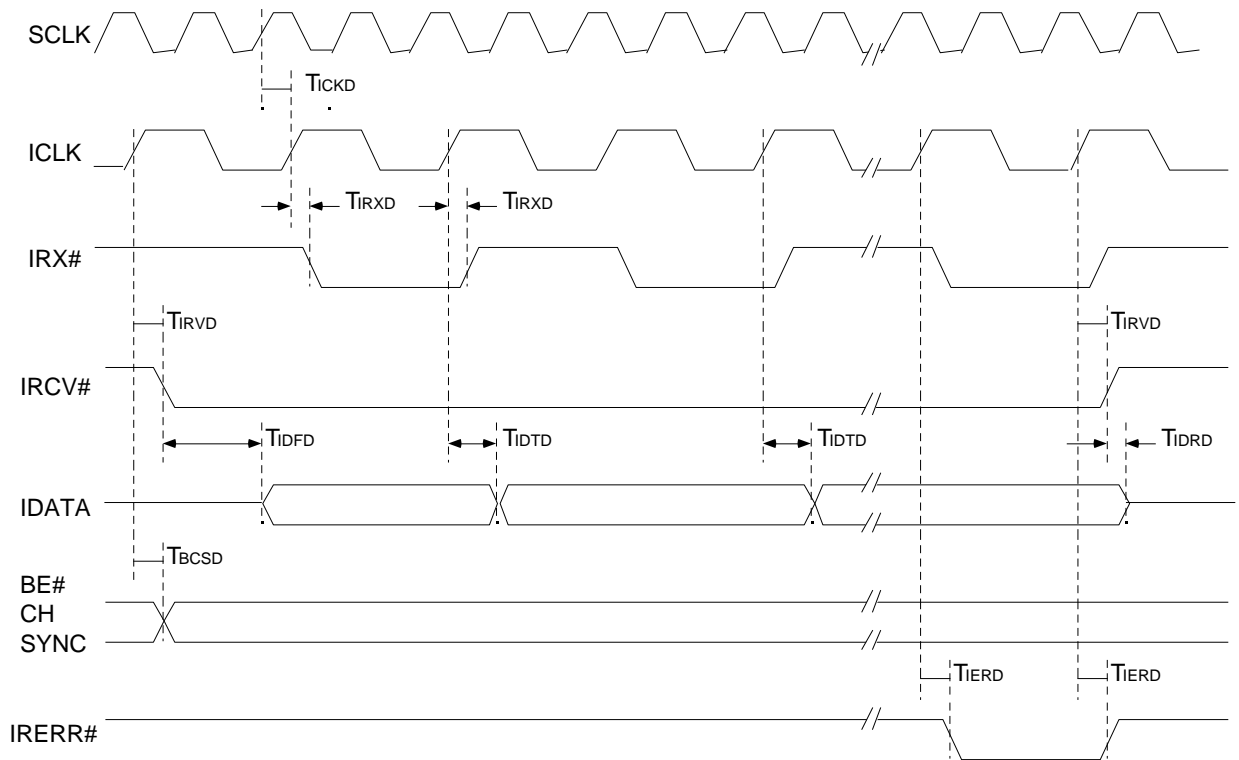


Figure 9-4-10 Isochronous Bus AC Characteristics 2

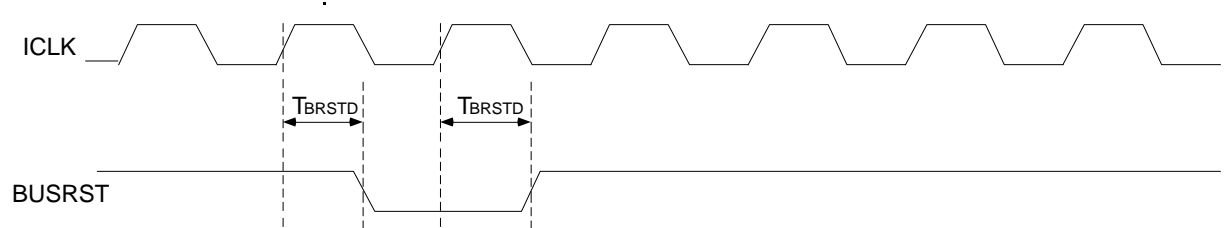
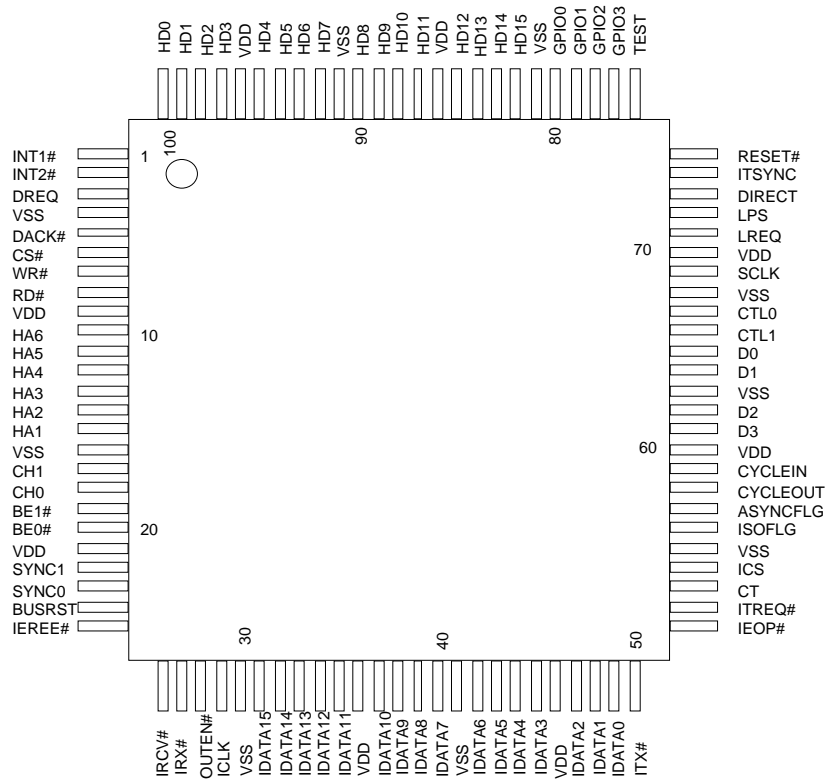


Figure 9-4-11 Isochronous Bus AC Characteristics 3

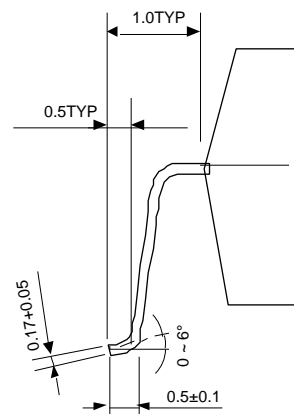
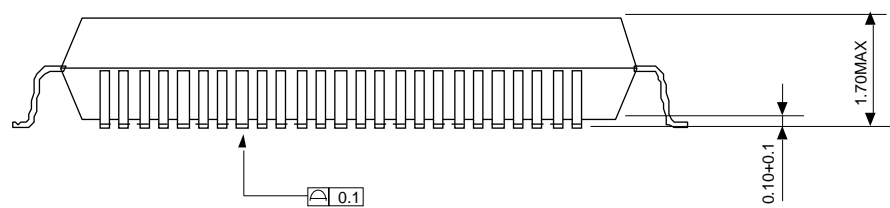
10 Terminal Arrays and Outline Drawings

10-1 Terminal Arrays



Technical drawing of a square plate with dimensions and tolerances. The overall dimensions are 16.0 ± 0.3 mm. The inner square area is 14.0 TYP mm. The thickness of the plate is 1.0 TYP mm. The drawing includes various tolerances and dimensions for the plate's features:

- Overall width: 16.0 ± 0.3
- Overall height: 16.0 ± 0.3
- Inner square width: 14.0 TYP
- Inner square height: 14.0 TYP
- Thickness: 1.0 TYP
- Top edge width: 75
- Top edge height: 51
- Right edge width: 50
- Right edge height: 26
- Bottom edge width: 25
- Bottom edge height: 1
- Left edge width: 76
- Left edge height: 100
- Bottom edge width: 0.18 ± 0.1
- Bottom edge height: 0.10 (M)
- Bottom edge width: 0.5
- Bottom edge height: 0.10 (M)



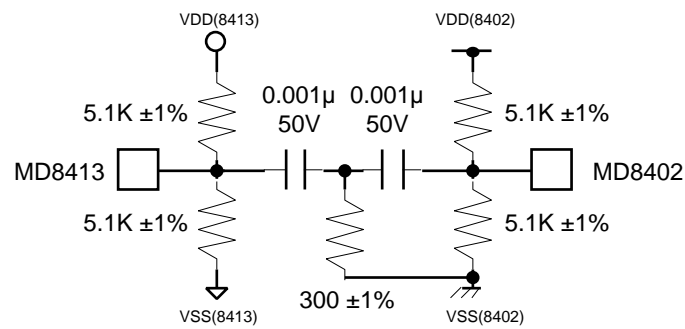
Appendix 1 I/O Status

TBD

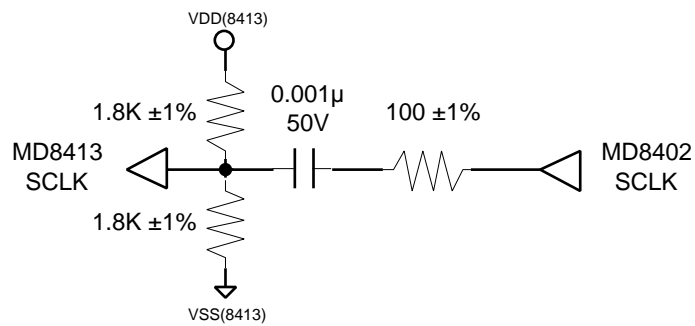
[illegible]

Appendix 2 Example circuit for AC connection

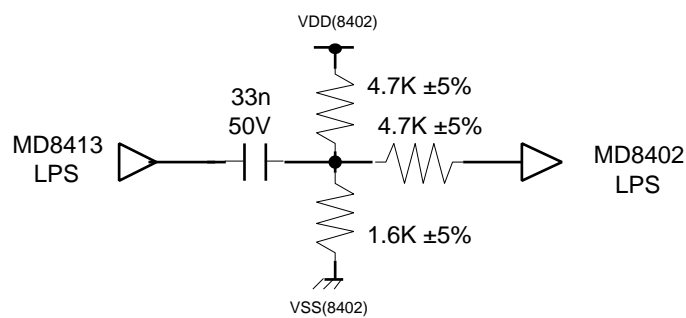
1) LREQ,CTL(1:0),D(3:0)



2) SCLK



3) LPS



Notes

- ☛ Contents of this manual may be modified without notice.
- ☛ Partial or overall reproduction and reprinting of this manual shall be prohibited without permission of the company.
- ☛ Owing this manual shall not fall out permission for the use of industrial and copy rights reserved by the company and Fuji Photo Film Co., Ltd. The company shall not be responsible for industrial and copy rights of the third party.
- ☛ The company shall not be responsible for any damage caused from this manual and from this chip.
- ☛ Prior to use, exchange of invoice specifications is required.
- ☛ Information available from:
 - Head Office
1-6, Matsusakadaira, Taiwa-cho
Kurokawa-gun, MIYAGI, 981-34 JAPAN
TEL: 81-22-347-1128 FAX: 81-22-347-1120
 - Tokyo Office
Fukumasu Bldg. 6F
1-20, Ageba-cho, Shinjuku-ku
Tokyo, 162 JAPAN
TEL: 81-3-3269-2141 FAX: 81-3-5229-7381

Index

A

AACTIVE.....	10
AC connection.....	66
AckErr	40
ackSent.....	52, 54
ackSnP	58
AckStatus.....	20
ARF	73, 74, 76
ARFBusReset	11, 76
ARFEmpty	36
ARFRej.....	38
ARxBufferSize.....	17, 73
ARxEnd	38, 76
asynchronous	75
ATAck.....	20
ATBusy.....	21
ATF	73, 75
ATFEmpty	36
ATFFull	36, 75
ATGo.....	44, 75
ATxBufferSize	73
ATxEnd	38

B

BE#	89
blockData	51, 54
BusNumber	14
BusReset.....	40
BusyCtrl.....	18
BusyState	20
Bus_Info_Block	73

C

CH	89
Channel.....	29, 32
channel.....	55, 56
CmdReset	39
CONTENDER	60
CRC	78, 91
CS#	64
CSEn.....	10
CT	91
CTL(0:1)	66
Cycle Start.....	92
CycleCount.....	26, 27
CycleDone.....	39
CycleLost	39
CycleMaster	4, 9, 86
CycleOffset.....	27
CycleSeconds	26, 39
CycleSource	9
CycleStart.....	39
CycleStart Packet.....	86
CycleTimerEn	9

D

D(0:3),	66
---------------	----

DackEn.....	36
DackHigh.....	11
dataLength	51, 54, 55, 56
DC connection.....	66
destinationID	49, 51, 53
destinationOffset	49, 51, 52, 53
DMA	65, 74
DREQ	3, 65, 74
DreqEn	36, 65
DreqLow	11
E	
EnSnoop	18
extended_tCode	51, 54
G	
GPIO(3:0)	43
GPIOCTL(3:0)	42
H	
HA(6:1)	64
HD(15:0)	64
HdrErr	39, 78
I	
IACTIVE	10
ICLK	91, 92
ICS	86, 92
IDATA(15:0)	86
IDValid.....	13
IEOP#.....	87, 88, 93
INT#	66
IRCV#.....	88, 91
IRERR#.....	91
isochronous.....	88
Isochronous Data	55, 57
isochronous Data	56, 57
IsoMode	9
IsoRxEn.....	33
ITLength.....	30
ITNoTx	38
ITREQ#.....	86, 88, 93
ITX#.....	87
ITZERO	10
L	
link_active	59
LPSON.....	10
LREQ	66, 67
M	
MaxRetryCountLimit	23
MaxRetryCycleLimit	25
MaxRetrySecondLimit	25
N	
NodeNumber.....	14
P	
PhyInt.....	40
PhyRegRcvd	40

physical_ID.....	59
PHY_DELAY	60
PHY_SPEED.....	60
POWER_CLASS.....	60
priority	49, 50, 52, 53

Q

quadletData.....	50, 52
------------------	--------

R

RD#	64
RdReg.....	22
ReceiveEn.....	12
RegAddr	22
RegData	22
RegRcvd	22
ResetARF.....	15, 76
ResetATF	15
ResetDMA	16
ResetLink	15
ResetTx.....	15
RetryCount.....	24
RetryCycleLimit.....	25
RetryLimit	38
RetrySecond/Limit.....	25
RetryStop	24
RetryTimeMax.....	21
Revision	8
root.....	13
rt	49, 50, 52, 53
RxSelfID	18

S

SCLK.....	66, 86
SecondCountHi	28
SecondCountLo	28
SelectDreq	36
SentRej	39
snoopedData.....	57
snpStat	58
sourceID	52, 53
spd	49, 50, 52, 54, 55, 58
Speed	29
StartSync.....	30, 33, 89
STO.....	38
StopSync.....	30, 33, 89
STStart	42
sy.....	55, 56
SYNC	89
Sync	30
SyncEn.....	30, 32

T

Tag.....	29
tag.....	55, 56
tCode.....	49, 50, 52, 53, 56
TCodeErr.....	39
tLabel	49, 50, 51, 53
TransmitEn.....	11
TransmitterEn.....	86

V
version.....8

W
WR# 64, 65
WritePending.....19
WrReg.....22