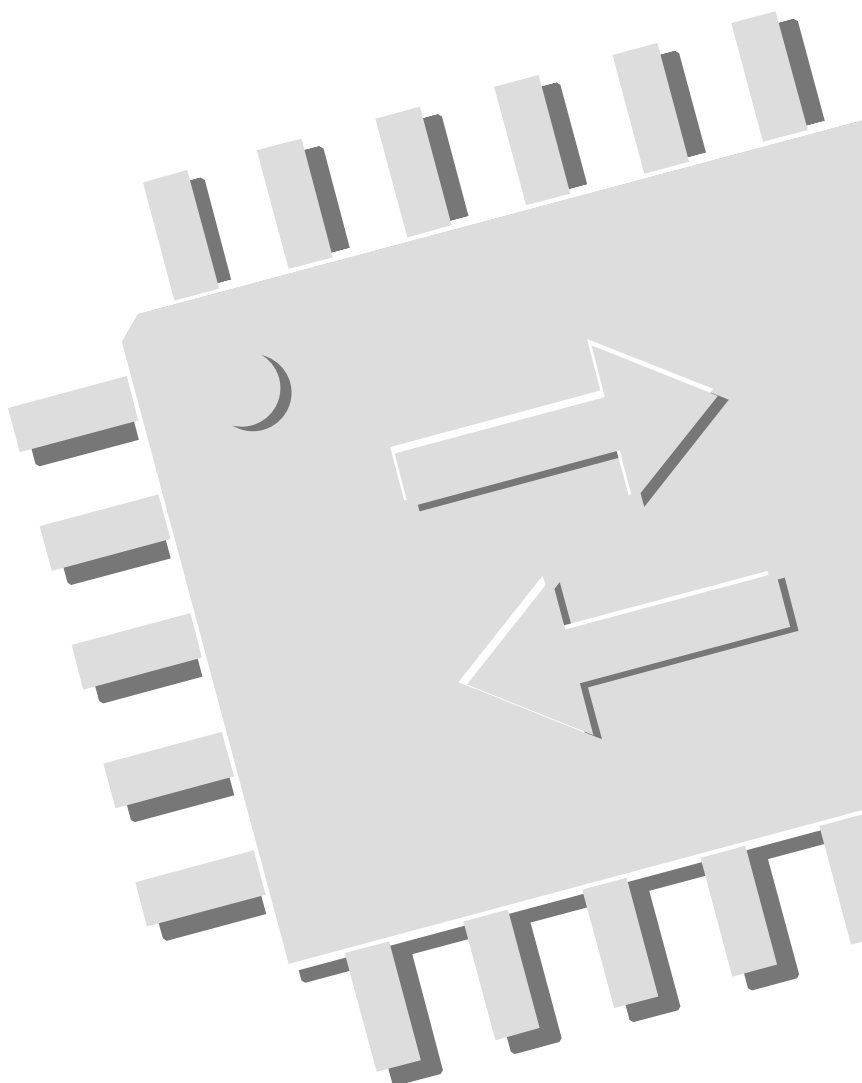


PHY(IEEE 1394)

MD8405E

User's Manual



MEMO

History

Revision	Date	Modified
1.01	07/22/99	An edition complying with MD8405E. MD8405 in the body is considered MD8405E.
1.03	08/25/99	2-2 Functional descriptions for terminals Figure 8-1 Package Dimension
1.10	10/08/99	Figure 5-14 LREQ isolation barrier circuit Figure 5-17 CTL[0:1] isolation barrier circuit Figure 5-18 D[0:7] isolation barrier circuit
1.20	11/30/99	Figure2-1 Terminal Arrays Table2-1 MD8405 Terminals (1)

Keys:

MSB, LSB of data	: MSB on the left and LBS on the right	
Negative logic signal description	: Attached with # at the last end of signal name	
Numeraldescription	: Binary	****b or ****
	Decimal	****
	Hexadecimal	****h or 0x****
Terminology	: Byte	Data in 8-bit width
	Word	Data in 16-bit width
	Quadlet	Data in 32-bit width
	Octlet	Data in 64-bit width

Note: PC[0:2] terminals defined as follows in the specifications to MD8404.

Most significant bit(MSB): PC2

Least significant bit(LSB): PC0

This is modified as follows to after MD8405.

Most significant bit(MSB): PC0

Least significant bit(LSB): PC2

therefore, PC2 is replaced with PC0 by the pinout of MD8405 in comparison with MD8404.

It will be unified in the PHY including MD8405 as follows from now on.

The part (for example, "0") whose data number is small, most significant bit (MSB).

The part (for example, "7") whose data number is big, least significant bit (LSB).

Comparison with MD8405B

A function is added with MD8405E so that it can change BIAS_HANDSHAKE_TIME in the P1394a Draft Ver2.0 standard.

Change point

- An EnDV bit is added to Register71. The initial value of this bit is based on "1". BIAS_HANDSHAKE_TIME value is changed under the condition of this bit.
- The value of Register17 changes it from 62h to 65h.

Comparison with MD8405D

1. Bug Fix

This subject of Md8405D's Errata is modified.

- 1.1 TpBias Down
- 1.2 Suspend Fault (S/R="H" only)
- 1.3 Resume Fault (S/R="H" only)
- 1.4 SelfID Reception
- 1.5 gap_count
- 1.6 EnDV

2. Product ID

The value of product ID changed for "0x303565(05e)".

Associated Material

IEEE Std 1394-1995 Standard for a High Performance Serial Bus
IEEE P1394a Draft 2.0 Standard for a High Performance Serial Bus

License

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1 Introduction

The MD8405 is a physical-layer IC intended to support the transfer speed of 400/200/100Mbit/sec., conforming to IEEE P1394a Draft Ver2.0. It offers three ports for the 1394-based cable interface, an interface for the link-layer IC, and the state machine logic for bus initialization and arbitration.

1-1 Features

- A low-voltage amplitude differential transceiver conforming to IEEE P1394a Draft Ver2.0.
- Used to support the data rates of 393.216 Mbit/sec., 196.608 Mbit/sec., and 98.304 Mbit/sec.
- 393.216 MHz PLL incorporated.
- An auto-shutdown function for the stop port to save power.
- 3-port independent TpBias.
- Sensing the reduction of cable power according to the cable power state.
- State machine logic for bus initialization and arbitration conforming to P1394a Draft Ver2.0.
- A port connection state machine conforming to P1394a Draft Ver2.0.
- PHY/Link interface conforming to P1394a Draft Ver2.0.
- Supports the PHY-Link interface through either AC or DC connections.
- AC timing setting terminal for the PHY-Link interface.
- Supports the disabling of individual ports via terminal pins.
- Supports enabling En_Accel and En_Multi via terminal pins.
- Supports the definition pins for Configuration Manager Capable and Power Class.

1-2 Applications

Digital camera	Digital VCR	Digital audio
Electronic musical instrument	Scanner	Printer
Various storage		

1-3 Internal Block Diagram

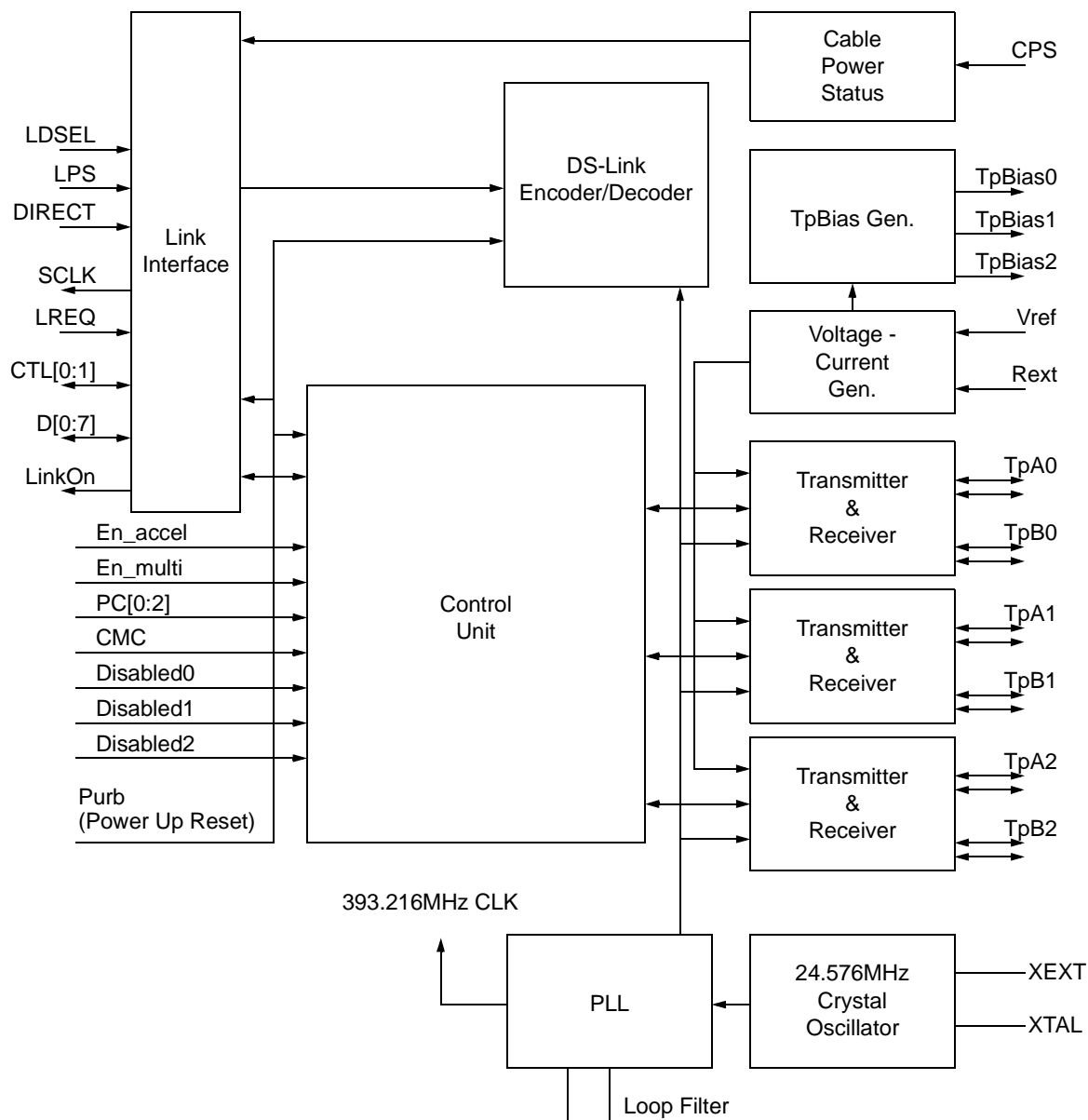


Figure 1-1 MD8405 Block Diagram

2 Terminal Description

2-1 Terminal Arrays

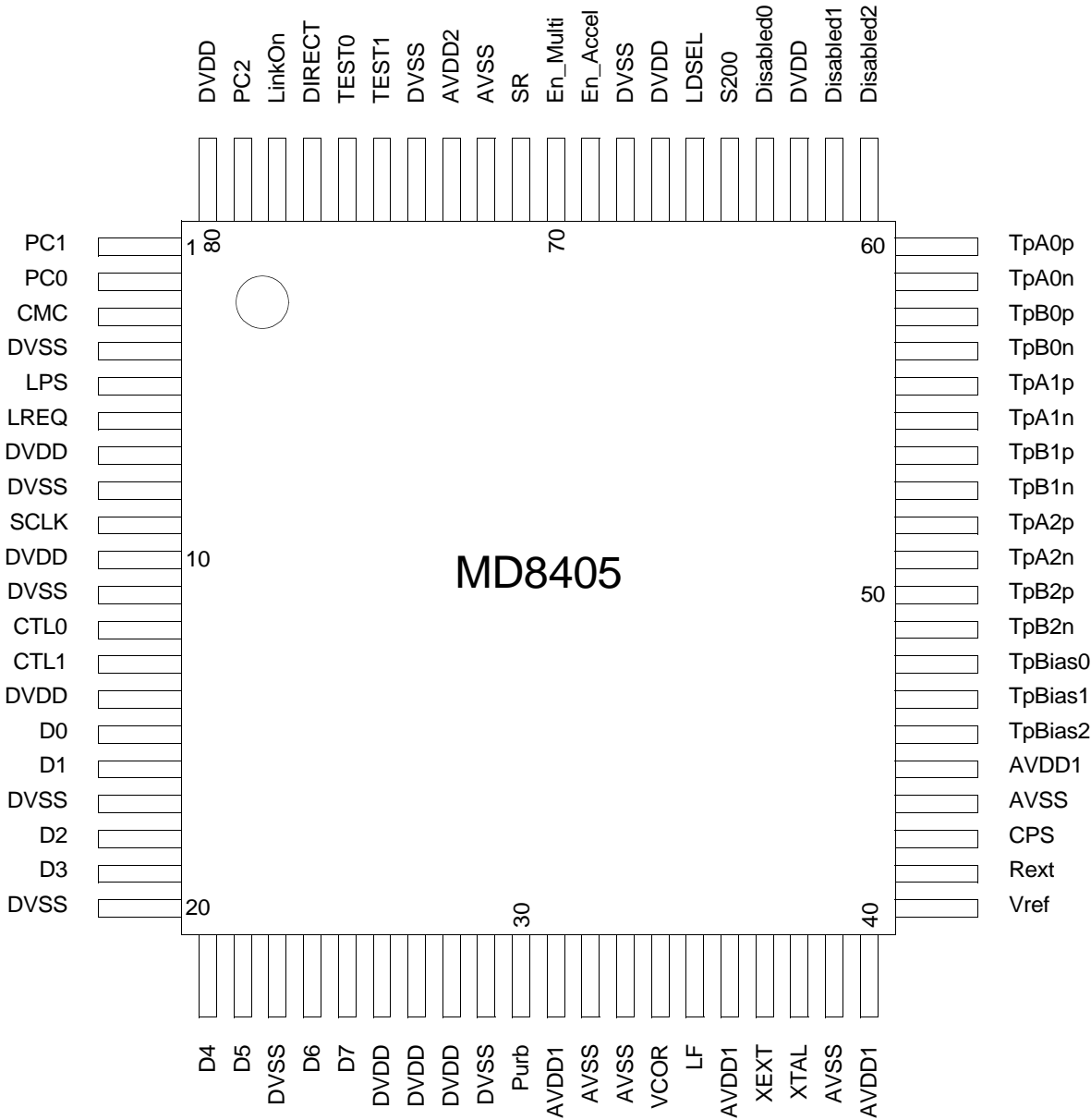


Figure 2-1 Terminal Arrays

2-2 Functional descriptions for terminals

Pin No.	Pin Name	I/O	Function
2,1,79	PC[0:2]	I	Power Class[0:2]. These pins are used to define the initial value of the Pwr_class bits in PHY register 4 after a hardware reset. Also the condition of the terminal of the level is reflected. Connected to DVDD or DVSS according to the setting condition.
3	CMC	I	Configuration management capable setting terminal. This pin defines the initial value of the Contender bit of the PHY register 4 after a hardware reset.
4,8,11,17,20,23, 29,68,74,	DVSS	-	Digital ground.
5	LPS	I	Link power status. [See 5-1-2]
6	LREQ	I	Link request. Link performs read/write of the PHY register and bus request via the LREQ terminal. [See 5-1-4]
7,10,14,26,27,28, 63,67,80	DVDD	-	Digital power supply.
9	SCLK	O	49.152MHz link system clock. The PHY-Link interface and the cable interface are synchronized with SCLK.
12,13	CTL[0:1]	I/O	PHY-Link interface control signals. [See 5-1-4]
15,16,18,19,21,22, 24,25	D[0:7]	I/O	PHY-Link interface data signals. [See 5-1-4]
30	Purb	I	External capacitor connection terminal for power-up reset. Connected to AVSS through 0.1[μF]. The minimum reset period is 15[msec]. During the reset period, the internal state machine is completely initialized. [See 5-5]
65	S200	I	Phy Speed Control signal. "H": Maximum bit rate is S200. "L": Maximum bit rate is S400. This pin is usually is "L".

Table 2-1 MD8405 Terminals (1)

Pin No.	Pin Name	I/O	Function
71	SR	I	Suspend/Resume function control signal "H": P1394a Draft Ver2.0 conformity. "L": P1394a Draft Ver1.3 conformity. A Suspend/Resume function is turned off because of this. Usually, "H".
31,36,40,45	AVDD1	-	Analog power supply 1. Power supplies other than those for the cable interface driver.
32,33,39,44,72	AVSS	-	Analog ground.
34	VCOR	I	A connection terminal for an external loop filter.
35	LF	O	
37,38	XEXT, XTAL	I/O	For crystal connections. Connection terminals for quartz crystal oscillators. 24.576MHz \pm 100ppm is required for the oscillator output frequency. The crystal used is required to have accuracy of 50ppm in the state that the load of 10[pf] is connected. [See 5-3]
41	Vref	I	A connection terminal for an external standard resistor. An external resistor of 18k [ohm] + 510 [ohm] (\pm 1%) with a capacitor of 0.01 μ F in parallel are inserted between this terminal and AVSS.
42	Rext	I	A connection terminal for an external standard resistor. An external resistor of 11k [ohm] + 6200 [ohm] (\pm 1%) is inserted between this terminal and AVSS.
43	CPS	I	A terminal for Cable Power Status detection. Connected to Cable Power (Vp) through 220k(\pm 5%) [ohm]. Connected to AVDD1 while unused. [See 5-2-9]
46,47,48	TpBias[2:0]	O	A cable bias output terminal. Connected to AVSS through a 0.33[μ F] capacitor.
49,53,57	TpB[2:0]n	I/O	An Arbitration/Speed Signal/Data output. An Arbitration/Strobe input. A negative-phase-sequence I/O terminal.
50,54,58	TpB[2:0]p	I/O	An Arbitration/Speed Signal/Data output. An Arbitration/Strobe input. A positive-phase-sequence I/o terminal.
51,55,59	TpA[2:0]n	I/O	An Arbitration/Strobe output. An Arbitration/Speed Signal/Data input. A negative-phase-sequence I/O terminal.
52,56,60	TpA[2:0]p	I/O	An Arbitration/Strobe output. An Arbitration/Speed Signal/Data input. A positive-phase-sequence I/O terminal.

Table 2-2 MD8405 Terminals (2)

Pin No.	Pin Name	I/O	Function
61,62,64	Disabled[2:0]	I	These pin define the initial value of the disable bits in the PHY port status page after a hardware reset, and the condition of the terminal of the level is reflected. [See 3-4-1 Bit 7]
66	LDSEL	I	Timing setting terminal for the PHY-Link interface. [See 5-1-6]
69	En_Accel	I	This bit defines the initial value of the Enab_accel bit after a hardware reset. Enab_accel is found in the PHY register address 5. [See 3-2-6 Bit 6]
70	En_Multi	I	This bit defines the initial value of the Enab_multi bit after hardware reset. Enab_multi is found in the PHY register address 5. It is made hardware resetting Initial value of the Enab_multi bit of the PHY register Address 5, and the condition of the terminal of the lever is reflected.
73	AVDD2	-	Analog power supply 2. Power supplies for the cable interface driver.
75,76	TEST[1:0]	I	Test mode control terminals. Connected to DVDD.
77	DIRECT	I	Defines operation mode setting terminal for the PHY-Link interface. L: AC connection H: DC connection [See 5-1-5]
78	LinkOn	O	Link-On signal output. When active Link-On is an AC signal of 6.144[MHz] and duty 50[%]. [See 5-1-3]

Table 2-3 MD8405 Terminals (3)

3 Control Register

3-1 Register access

Each register of the MD8405 is usually accessed from the link layer IC. Refer to section 5-1-4-1 (LREQ) for more detail.

3-2 Register features

3-2-1 Register 0

Address 00h

0	1	2	3	4	5	6	7
Physical_ID						R	PS

Bit 0~5 Physical ID: Physical Node ID (R - Initial value: 00h)

The ID of this node is held in this field. These bits are initialized upon bus reset and are determined during the Self-ID period for Self-ID packet transmission. After the completion of Self-ID packet transmission, the register address 00h including these bits automatically output to the link interface for status transmission.

Bit 6 R: Root indicator (R - Initial value: 0h)

Value 1 indicates that this node has been set at the root. This bit is initialized upon bus reset and determined during the Tree-ID period.

Bit 7 PS: Cable Power Status (R - Initial value: CPS terminal setting)

The CPS terminal value is reflected and the status of power from the cable is indicated. Value 1 denotes that power is fed from the cable.

3-2-2 Register 1

Address 01h

0	1	2	3	4	5	6	7
RHB	IBR	Gap_count					

Bit 0 RHB: Root Hold Bit (R/W - Initial value: 0h)

When the value is 1, this node calls for the condition that it becomes a root with the next reset. This bit is also automatically set according to the PHY configuration packet send/receive condition.

Bit 1 IBR: Initiate Bus Reset (R/W - Initial value: 0h)

Bus reset is started immediately after the setting of this bit at 1. This bit is initialized by bus reset.

Bit 2~7 Gap_Count: Gap Count (R/W - Initial value: 3Fh)

A Gap Count value. This bit is also automatically set according to the PHY configuration packet send/receive condition. The bit value is held in the case of the first bus reset occurring after the setting of this bit. However, it is initialized upon the next bus reset.

3-2-3 Register 2

Address 02h

0	1	2	3	4	5	6	7
Extended				Total_ports			

Bit 0~2 Extended: (R - Initial value: 111b)
Register Map which MD8405 supports, 111b are read.

Bit 3 Reserved: (R - Initial value: 0h)
Always, 0 (00b) is read out.

Bit 4~7 Total_ports: Total of Port (R - Initial value: 3h)
Used to indicate the number of ports possessed by the MD8405. Value 3 (0011) is always read out.

3-2-4 Register 3

Address 03h

0	1	2	3	4	5	6	7
Max_speed				Delay			

Bit 0~2 Max_Speed: Speed (R - Initial value: S200="L": 2h,S200="H": 1h)
Used to show the maximum transfer speed supported by the MD8405.
02h (010) is read when a S200 terminal is "L". 01h (001) is read when a S200 terminal is "H".
When the value 02h is read the max speed is 400Mbps.
When the value 01h is read the max speed is 200Mbps.

Bit 3 Reserved: (R - Initial value: 0h)
Always, 0 (00b) is read out.

Bit 4~7 Delay: (R - Initial value: 1h)
When MD8405 repeats it, the worst case time of Delay is shown. 01h (0001) is always read, and the maximum repeat delay time of MD8405 is 164ns.

3-2-5 Register 4

Address 04h

0	1	2	3	4	5	6	7
Link_active	Contender	Jitter			Power_class		

Bit 0 Link_active: Link active (R/W - Initial value: 1h)

This bit is used to control the L (link_active) field value of the Self-ID packet.
 The value that the logic product of the Link active signal detected by this bit and LPS was taken in the Self-ID packet L (Link_active) field is reflected.
 This bit is initialized to 1 upon hardware reset.

Bit 1 Contender: CMC (R/W - Initial value: A setup of a CMC terminal)

This bit is reflected on the c (CONTENDER) field of the Self-ID packet.
 This bit is initialized to the value of CMC pin upon hardware reset.

Bit 2~4 Jitter: Jitter (R - Initial value: 1h)

When MD8405 repeats it, the difference in the maximum of Delay and the minimum time is shown. 1 is always read. jitter when MD8405 repeats it is 40ns.

Bit 5~7 Power_class: Power Class (R/W - Initial value: A setup of a PC terminal)

This bit is reflected on the pwr (POWER_CLASS) field of the Self-ID packet.

This bit is initialized to PC[0:2] upon hardware reset.

bit5: PC0(Pin2)

bit6: PC1(Pin1)

bit7: PC2(Pin79)

3-2-6 Register 5

Address 05h

0	1	2	3	4	5	6	7
Resume_int	ISBR	Loop	Pwr_fail	Timeout	port_event	Enab_accel	Enab_multi

Bit 0 Resume_int: Resume interrupt enable (R/W - Initial value:0h)

The Port_event bit is set when Resume on any port happens and this bit is set to 1.

Bit 1 ISBR: Initiate Short (Arbitrated)Bus Reset (R/W - Initial value: 0h)

Arbitration short bus reset is started when this bit is set at 1.

This bit is initialized by bus reset automatically.

Bit 2 Loop: Loop detect (R/W - Initial value: 0h)

Value 1 indicates that the bus has been a loop.

This bit is cleared by writing 1 or upon hardware reset.

Bit 3 Pwr_fail: Cable power failure detect (R/W - Initial value: 0h)

It is shown that a PS bit changed in 0 from 1 in the case of 1.

This bit is cleared by writing 1 or upon hardware reset.

Bit 4 Timeout: Arbitration state machine timeout (R/W - Initial value: 0h)

The case of 1, this node, A0: It is shown that it didn't come beyond the MAX_ARB_STATE_TIME time out of state with Idle, the one except for T0:Tree_IDStart.

This bit is cleared by writing 1 or upon hardware reset.

Bit 5 **Port_event:** Port_event detect (R/W - Initial value: 0h)

MD8405 sets this bit to 1 when Connected, Bias, Disabled, a change in the Fault bit are detected and Int_enable is set to 1. And, 1 is set in this bit when Resume happens when Resume_int is set up in 1.

This bit is cleared by writing 1 or upon hardware reset. Also, this bit is set to 1 when a Resume operating is detected while the Resume_int bit is set 1.

Bit 6 **Enab_accel:** Enable arbitration acceleration

(R/W - Initial value: Determine by the state of the En_Accel pin at hardware reset.)

When this bit is set at 1, the MD8405 performs Ack-acceleration arbitration and Fly-by arbitration.

When this bit is set at 0, the MD8405 does not perform acceleration arbitration.

This bit is initialized by hardware reset.

Bit 7 **Enab_multi:** Enable multi-speed packet concatenation

(R/W - Initial value: A setup of a En_Multi terminal determined by the state of the En_multi pin at hardware reset.)

When this bit is set at 1, the MD8405 is enabled to transfer concatenated packet of different speeds.

When this bit is set at 0 the MD8405 performs concatenated packet transfer at the same speed as that of the initial packet.

This bit is initialized by hardware reset.

3-2-7 Register 6

Address 06h

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved** (R - Initial value: 0h)

Reserved.

3-2-8 Register 7

Address 07h

0	1	2	3	4	5	6	7
Page_select				Port_select			

Bit 0~2 **Page_select** (R/W - Initial value: 0h)

This bit field define what page is to be access when PHY registers 08h through 0Fh are referenced.

Bit 3 **Reserved** (R - Initial value: 0h)

Reserved.

Bit 4~7 **Port_select** (R/W - Initial value: 0h)

This field determine the port whose data is accessible while page 0 (port status) registers are visible to the system's link.

3-3 List of registers

Name	Address	0	1	2	3	4	5	6	7
Register0	0000	Physical_ID						R	PS
Register1	0001	RHB	IBR	Gap_count					
Register2	0010	Extended				Total_ports			
Register3	0011	Max_speed				Delay			
Register4	0100	Link_active	Contender	Jitter			Power_class		
Register5	0101	Resume_int	ISBR	Loop	Pwr_fail	timeout	port_event	Enab_accel	Enab_multi
Register6	0110								
Register7	0111	Page_Select				Port_Select			
-	1000	Register8							
-	1001	Register9							
-	1010	RegisterA							
-	1011	RegisterB							
-	1100	RegisterC							
-	1101	RegisterD							
-	1110	RegisterE							
-	1111	RegisterF							

Table 3-1 List of registers

3-4 Page_select=0 (Port Status page)

This register reflects the condition of each port. A port is chosen by setting the Port_select bits in register 7 to the desired port number.

3-4-1 Register 00

Address 08h

0	1	2	3	4	5	6	7
Astat		Bstat		Child	Connected	Bias	Disabled

Bit 0~1 **Astat**: Status of TPA (R - Initial value: 3h)

The condition of TpA is shown. The meaning of the bits is as follows:

11b: Z

01b: 1

10b: 0

00b: invalid

Bit 2~3 **Bstat**: Status of TPB (R - Initial value: 3h)

The condition of TpB is shown. The meaning of the values is as follows:

11b: Z

01b: 1

10b: 0

00b: invalid

Bit 4 **Child**: Child (R - Initial value: 0h)

This bits reports the child/parent status of the port. The port is Parent when the bit is 0. It is initialized by bus resetting. The bit is decided during the Tree-ID period.

Bit 5 **Connected**: Connected (R - Initial value: 0h)

This bit indicates if the port is connected to a peer PHY device when set to 1.

Bit 6 **Bias**: Cable Bias (R - Initial value: 0h)

Cable Bias detected by the port.

When this bit is 1, TpBias has been detected by the port.

Bit 7 **Disabled**: Port Disabled

(R/W - Initial value: Determine by the state of DISABLED pin at hardware reset)

This port is Disabled when it is set up in 1.

This bit is initialized by hardware resetting.

3-4-2 Register 01

Address 09h

0	1	2	3	4	5	6	7
Negotiated_speed			Int_enable	Fault			

Bit 0~1 **Negotiated_speed:** Negotiate speed (R - Initial value: 0h)

This bit field defines the max speed of the peer port connect to this port. The field is initialized during the Self-ID period following a bus reset. The meaning of the value is as follows:

000b: It is shown that the maximum transfer speed of confrontation node is ps 100MB.

001b: It is shown that the maximum transfer speed of confrontation node is ps 200MB.

010b: It is shown that the maximum transfer speed of confrontation node is ps 400MB.

Bit 2 **Int_enable:** Enable port event interrupt (R/W - Initial value: 0h)

The Port_event bit is set to 1 when the any of the status bits connected, Bias, Disabled, or Fault change state while this bit is set to 1. This bit is initialized by hardware resetting.

When set to 1, this bit enable the setting of the Port_event bit (register 5 bit 5) to 1 due to any change of state of several status bits. These status bits are connected Bias, Disabled, or Fault. This bit is set to 0 upon hardware reset.

Bit 3 **Fault:** (R/W - Initial value: 0h)

It is shown that an error happened in the case of 1 during the Suspend/Resume movement. This bit is cleared by a hardware resetting or writing a one to this bit position.

This bit reports an error when either a resume fault or suspend fault is detected. This bit is set to 1 when an error is detected.

Bit 4~7 **Reserved:** (R - Initial value: 0h)

Reserved.

3-4-3 Register 02

Address 0Ah

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)

Reserved.

3-4-4 Register 03

0	1	2	3	4	5	6	7

Address 0Bh

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-4-5 Register 04

0	1	2	3	4	5	6	7

Address 0Ch

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-4-6 Register 05

Address 0Dh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-4-7 Register 06

Address 0Eh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-4-8 Register 07

Address 0Fh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-5 Page_select=0 List

Name	Address	0	1	2	3	4	5	6	7
Register00	1000	Astat		Bstat		Child	Connected	Bias	Disabled
Register01	1001	Negotiated_speed			Int_enable	Fault			
Register02	1010								
Register03	1011								
Register04	1100								
Register05	1101								
Register06	1110								
Register07	1111								

Table 3-2 page_select=0 List

3-6 Page_select=1 (Vendor Identification page)

3-6-1 Register 10

Address 08h

0	1	2	3	4	5	6	7
Compliance_level							

Bit 0~7 Compliance_level: (R - Initial value: 1h)
Reading always return the value 01h. Writing has no effect.

3-6-2 Register 11

Address 09h

0	1	2	3	4	5	6	7

Bit 0~7 Reserved: (R - Initial value: 0h)
Reserved.

3-6-3 Register 12

Address 0Ah

0	1	2	3	4	5	6	7
Vendor_ID[23:16]							

Bit 0~7 Vendor_ID[23:16]: (R - Initial value: 00h)
Always, 00h is read out.

3-6-4 Register 13

Address 0Bh

0	1	2	3	4	5	6	7
Vender_ID[15:8]							

Bit 0~7 Vender_ID[15:8]: (R - Initial value: C0h)
Always, C0h is read out.

3-6-5 Register 14

Address 0Ch

0	1	2	3	4	5	6	7
Vender_ID[7:0]							

Bit 0~7 Vender_ID[7:0]: (R - Initial value: 2Dh)

Always, 2Dh is read out.

3-6-6 Register 15

Address 0Dh

0	1	2	3	4	5	6	7
Product_ID[23:16]							

Bit 0~7 Product_ID[23:16]: (R - Initial value: 30h)

Always, 30h is read out.

3-6-7 Register 16

Address 0Eh

0	1	2	3	4	5	6	7
Product_ID[15:8]							

Bit 0~7 Product_ID[15:8]: (R - Initial value: 35h)

Always, 35h is read out.

3-6-8 Register 17

Address 0Fh

0	1	2	3	4	5	6	7
Product_ID[7:0]							

Bit 0~7 Product_ID[7:0]: (R - Initial value: 65h)

Always, 65h is read out.

3-7 Page_select=1 List

Name	Address	0	1	2	3	4	5	6	7
Register10	1000	Compliance_level							
Register11	1001								
Register12	1010	Vendor_ID[23:16]							
Register13	1011	Vender_ID[15:8]							
Register14	1100	Vender_ID[7:0]							
Register15	1101	Product_ID[23:16]							
Register16	1110	Product_ID[15:8]							
Register17	1111	Product_ID[7:0]							

Table 3-3 page_select=1 List

3-8 Page_select=7 (Vendor Dependent page)

3-8-1 Register 70

Address 08h

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-2 Register 71

Address 09h

0	1	2	3	4	5	6	7
LPSISBR							EnDV

Bit 0 **LPSISBR:** (R/W - Initial value: 0h)
When this bit is 1 and the PHY/LINK interface becomes to be disabled, MD8405 issues ISBR and initializes Power_class bits and contender bit automatically.

Bit 1~6 **Reserved:** (R - Initial value: 0h)
Reserved.

Bit 7 **EnDV:** (R/W - Initial value: 1h)
BIAS_HANDSHAKE_TIME is changed by setting it on 1.
The case of 0 works with the P1394a Draft Ver2.0 standard.
It is initialized after hardware resetting.
This bit is invalid in the time of the SR terminal = "L".

3-8-3 Register 72

Address 0Ah

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-4 Register 73

Address 0Bh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-5 Register 74

Address 0Ch

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-6 Register 75

Address 0Dh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-7 Register 76

Address 0Eh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-8-8 Register 77

Address 0Fh

0	1	2	3	4	5	6	7

Bit 0~7 **Reserved:** (R - Initial value: 0h)
Reserved.

3-9 Page_select=7 List

Name	Address	0	1	2	3	4	5	6	7
Register70	1000								
Register71	1001	LPSISBR							EnDV
Register72	1010								
Register73	1011								
Register74	1100								
Register75	1101								
Register76	1110								
Register77	1111								

Table 3-4 page_select=7 List

4 Data Format

4-1 Self-ID Packet

The Self-ID is transmitted by the MD8405 as a 2-quadlet packet, the format of packet is shown if Fig. 4-1. During the Self-ID period of bus initialization, the MD8405 transmits the Self-ID packets. Upon reception of the Ping packet, the MD8405 also sends out a Self-ID packet automatically as a response.

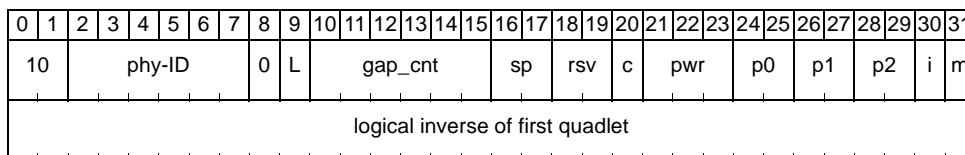


Figure 4-1 Self-ID packet format

phy_ID : Physical_ID field

A physical_ID of the PHY's node.

L : Link_active field

The logical "AND" of the LPS terminal and the Link_active bit of (Reg 4 Bit 0). The definition of bit is:

0: Link off

1: Link on

The logical product of the LPS terminal during Self_ID packet transmission and the Link_active bit of PHY Register4 is reflected.

gap_cnt : Gap_count field

The Gap_Count value of PHY Register1 is returned.

sp : PHY_SPEED field

00 = 98.304Mbps

01 = 98.304 and 196.608Mbps

10 = 98.304 and 196.608 and 393.216Mbps

11 = Reserved

The value returned is base on state of the S200 pin. S200:

L: The return value is 01.

H: The return value is 10.

rsv : 00b fix

C : CONTENDER field

The Contender bit value of PHY Register4 is returned.

pwr : POWER_CLASS field

bit21 = PC0(Pin2)

bit22 = PC1(Pin1)

bit23 = PC2(Pin79)

The pwr bit of PHY Register4 is reflected. The following is defined by IEEE P1394a Draft Ver2.0:

000 = This node does not require any power. Node doesn't repeat a power supply.

- 001 = This node has its own power supply, capable of supplying a minimum of 15W.
- 010 = This node has its own power supply, capable of supplying a minimum of 30W.
- 011 = This node has its own power supply, capable of supplying a minimum of 45W.
- 100 = This node consumes a maximum of 3W from the cable. No additional power is needed to enable the link.
- 101 = Reserved
- 110 = This node consumes a maximum of 3W from the cable. In addition, it consumes up to 3W to enable the link or its higher layers.
- 111 = This node consumes a maximum of 3W from the cable. In addition, it consumes up to 7W to enable the link or its higher layers.

p0 ... p2 : Port status field

- 11 = Active and connected to a child node.
- 10 = Active and connected to a parent node
- 01 = Not active (disabled, disconnected, suspended)
- 00 = Not present on this PHY

Used to indicate the port status.

i : Initiated_reset field

This bit is used to indicate if this node issued a BusReset. The definition of the bit is:

- 1: Node issued BusReset.
- 0: Node did not issue BusReset.

Indicates that this node has issued BusReset.

m : more_packets field

Used to transmit multiple Self-ID packets. This field is set at 1, but it is fixed at 0 for the MD8405.

4-2 Link-on Packet

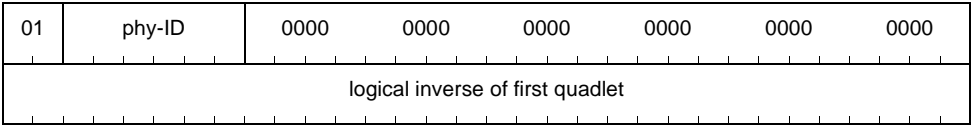


Figure 4-2 Link-on packet format

Refer to the section in the 1394 spec.

4-3 PHY Configuration Packet

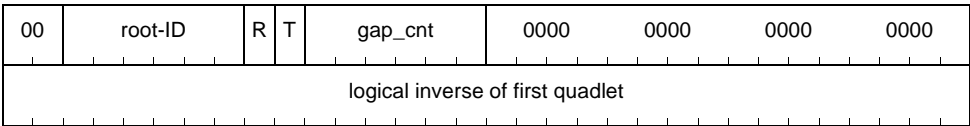


Figure 4-3 PHY Configuration packet format

Refer to the section in the 1394 spec.

4-4 Extended PHY Packet

4-4-1 Ping Packet

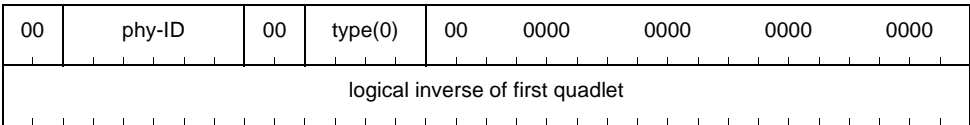


Figure 4-4 Ping packet format

Refer to the section in the 1394 spec.

4-4-2 Remote Access Packet

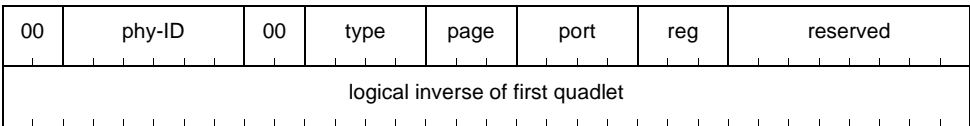


Figure 4-5 Remote Access packet format

Refer to the section in the 1394 spec.

4-4-3 Remote Reply Packet

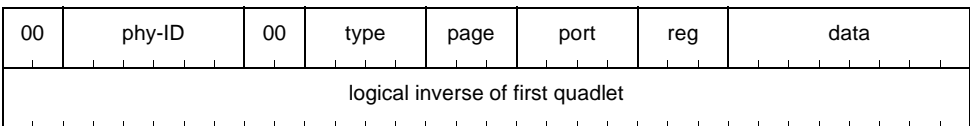


Figure 4-6 Remote Reply packet format

Refer to the section in the 1394 spec.

4-4-4 Remote Command Packet

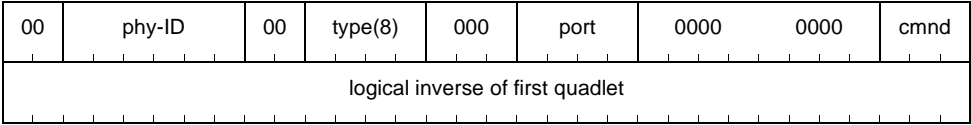


Figure 4-7 Remote Command packet format

Refer to the section in the 1394 spec.

4-4-5 Remote Confirmation Packet

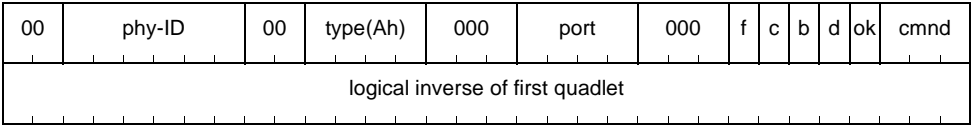


Figure 4-8 Remote Confirmation packet format

Refer to the section in the 1394 spec.

4-4-6 Resume Packet

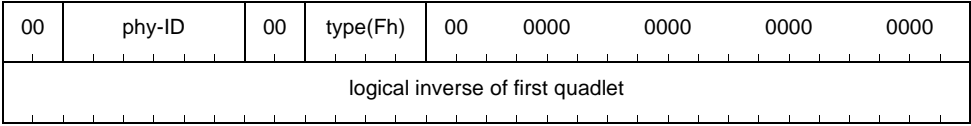


Figure 4-9 Resume packet format

Refer to the section in the 1394 spec.

5 Functional Descriptions

5-1 Link Chip Interface

5-1-1 Connections

5-1-1-1 DC connection

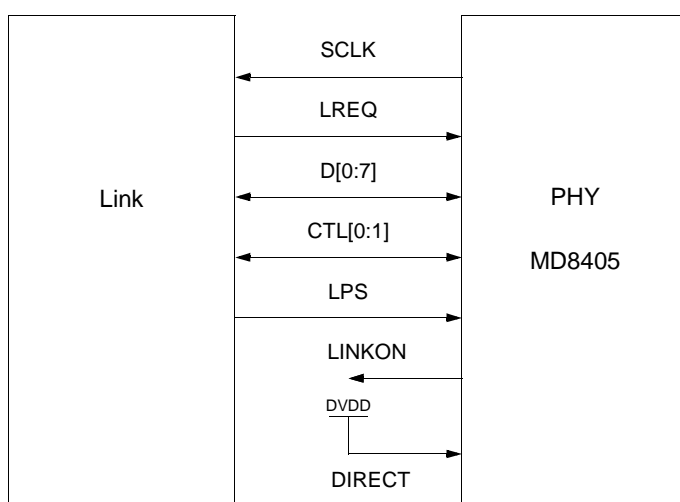


Figure 5-1 Connections between MD8405 and Link Chip (DC connection)

5-1-1-2 AC connection

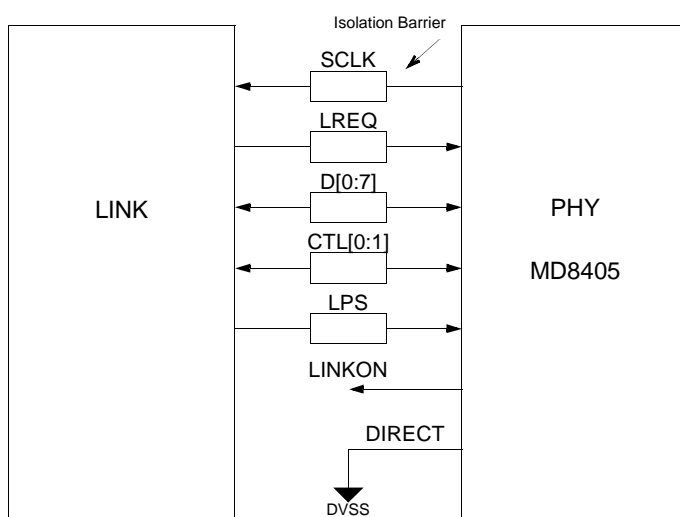


Figure 5-2 Connections between MD8405 and Link Chip (AC connection)

5-1-2 LPS (Link Power State)

According to the input in the LPS terminal, the MD8405 either enable or disable the PHY/Link interface, when the MD8405 identifies the LPS terminal is logically deassert for a period of TLPS_RESET, it resets the PHY/Link interface. When the PHY/Link interface is in a DC connection, the MD8405 provides an output of 0 to Ctl[0:1] and D[0:7]. If the PHY/Link interface is in an AC connection, the Hi-Z state is assumed.

In addition, when the MD8405 identifies the LPS terminal is logically deassert for a period of TLPS_DISABLE, it disables the PHY/Link interface. When the PHY/Link interface is in a DC connection, the MD8405 provides an output of 0 to SCLK, Ctl[0:1], and D[0:7]. If the PHY/Link interface is in an AC connection, the Hi-Z state is assumed.

If the PHY/Link interface is reset, all bus requests and register read requests are canceled.

If the PHY/Link interface is reset during packet transfer through the link, the MD8405 identifies that packet transfer has been finished and it performs the related operation.

There is no generation of state output while the PHY/Link interface is disabled. In addition, this information is not output even after the PHY/Link interface has been enabled.

Once the reset/disabled MD8405 detects the assertion of the LPS, MD8405 begins to generate an output of SCLK. If the PHY/Link interface is the DC connection mode, the MD8405 provides an output of 0 to Ctl and D lines for 7 SCLK cycles after the detection of LPS. At the eighth SCLK, a Receive (Ctl[0:1]=10b, D[0:7]=ffh) output of Data_Prefix is given to the PHY/Link interface and regular operation then begins. If the PHY/Link interface is in an AC connection, the MD8405 provides an output of 0 to Ctl and D for one SCLK cycle during one to six SCLK cycles after the detection of LPS. At the eighth SCLK, a Receive (Ctl[0:1]=10b, D[0:7]=ffh) output of Data_Prefix is given to the PHY/Link interface and regular operation then begins. In other periods, the Hi-Z condition is assumed.

If this node is in the middle of packet reception at that time, a Receive output of Data_Prefix is presented to the PHY/Link interface until the completion of packet reception.

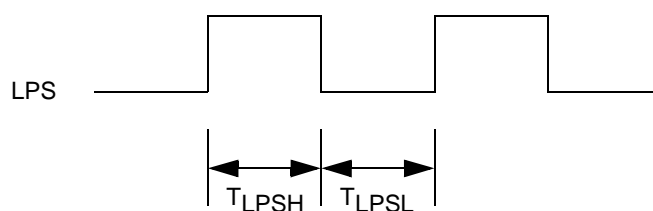


Figure 5-3 LPS waveform at AC connection

Symbol	Item	Unit	MIN	MAX
TLPSL	LPS low time (with pulses)	μs	0.09	1.00
TLPSH	LPS high time (with pulses)	μs	0.09	1.00
TLPS_RESET	The time period required to reset the PHY/Link interface when the MD8405 identifies that the LPS is logically in deassertion.	μs	1.2	2.7
TLPS_DISABLE	The time period required to disable the PHY/Link interface when the MD8405 identifies that the LPS is logically in deassertion.	μs	25	30

Table 5-1 LPS Timing

5-1-3 LinkOn

The MD8405 identifies that the LPS is logically in deassertion or that the link is non-active while the Link_active bit of the PHY register is 0.

Generally, LinkOn maintains the output at the "L" level, but it begins to generate an output of LinkOn signal when a LinkOn packet to this node is received while the MD8405 is identifying that the link is non-active.

In this phase also, a LinkOn signal output is generated as an Interrupt output when the Loop bit, the Pwr_fail bit, the Timeout bit, and the Port_event bit are turned to 1. The LinkOn signal output is kept generated while the link remains to be non-active. Since then, when the link is turned to be active, LinkOn begins to generate an "L" output.

The Link-On signal is an AC signal with a duty factor of 50% to be output at a frequency of 6.144MHz.

5-1-4 Link Interface (LREQ,CTL[0:1],D[0:7])

The PHY-Link interface of the MD8405 conforms to IEEE P1394a Draft Ver2.0.

The PHY-Link interface is capable of 4 types of operation; request by LREQ, status transmission by CTL, packet transfer, and packet reception. Any operation other than request, which employs CTL, is controlled by PHY. Upon reception of a packet, the MD8405 starts operation of packet reception in the first preference.

Tables 5-2 and 5-3 show the CTL status and meanings.

CTL[0:1]	Operation	Description
00b	Idle	Idle condition when nothing is performed. (default mode)
01b	Status	Status information is transferred.
10b	Receive	Contents of the received packet are transferred.
11b	Grant	PHY-Link interface is given to the link for packet transfer.

Table 5-2 Operation for CTL Control by PHY

The operation mode as shown in Table 5-3 is assumed after the above-mentioned Grant is finished and the link begins to control the PHY-Link bus.

CTL[0:1]	Operation	Description
00b	Idle	Completion of packet transfer. PHY-Link interface is released.
01b	Hold	PHY-Link interface is held until transfer packet data are defined. Concatenated packet transfer is requested.
10b	Transmit	Transfer packet data are input in the PHY.
11b	Reserved	Reserved

Table 5-3 Operation for CTL Control by Link

5-1-4-1 LREQ

A Link chip inputs serial signal which synchronized in the LREQ terminal in SCLK to require Packet transmission, the access of the PHY register or Acceleration Control. This serial signal includes the various information about request type, transferring packet rate, and read/write command.

The length of the LREQ serial signal varies in the type of the requirement, and it is six bits with Acceleration Control Request. And, it is 7 bits in the bus request. It is 9 bits in the register read request. It is 17 bits in the register write request.

This serial signal calls for the transmission of 0 as a stop bit, to be attached to the end of the signal.

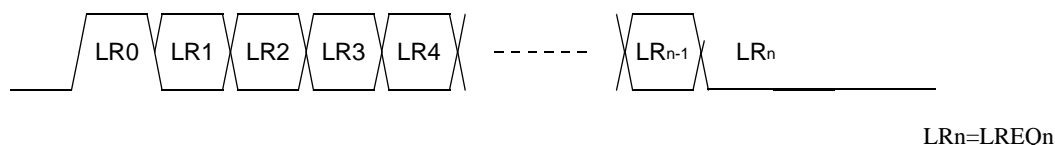


Figure 5-4 LREQ stream

The request for packet transfer is performed according to the format with the 7-bit length as shown in Table 5-4.

Bit(s)	Type	Description
0	Start Bit	Indicates start of requests. Always 1.
1~3	Request Type	Indicates type of bus request - immediate, isochronous, priority or fair. See Table 5-9 for the encoding of this field.
4~5	Request Speed	The speed at which the PHY will transmit the packet on Serial Bus. This field has the same encoding as the speed code from the first symbol of the receive packet. See Table 5-9 for the encoding of this field.
6	Stop Bit	Indicates end of transfer. Always 0. If bit 6 is zero, this bit may be omitted.

Table 5-4 Request Format

LREQ[4:5]	Data Rate
00	100Mbps
01	200Mbps
10	400Mbps
11	Reserved

Table 5-5 Speed format

The request for register read by the PHY chip is performed using the 9-bit message format shown in Table 5-6. In addition, the request for register write is performed using the 17-bit message format shown in Table 5-7.

Bit(s)	Type	Description
0	Start Bit	Indicates start of request. Always 1.
1~3	Request Type	Indicates that this is a register read. See Table 5-9 for the encoding of this field.
4~7	Address	The internal PHY address to be read.
8	Stop Bit	Indicates end of transfer. Always 0.

Table 5-6 Read Register Format

Bit(s)	Type	Description
0	Start Bit	Indicates start of request. Always 1.
1~3	Request Type	Indicates that this is a register write. See Table 5-9 for the encoding of this field.
4~7	Address	The internal PHY address to be written.
8~15	Data	For a write transfer, the data to be written to the specified address.
16	Stop Bit	Indicates end of transfer. Always 0.

Table 5-7 Write Register Format

An Acceleration Control requirement is done by the format of the head who shows it 6 bits in the Table 5-8.

Bit(s)	Type	Description
0	Start Bit	Indicates start of request. Always 1.
1~3	Request Type	Indicates that this is an acceleration control request. See Table 5-9 for the encoding of this field.
4	Accelerate	When zero, instructs the PHY to disable arbitration accelerations. A value of one requests the PHY to enable arbitration accelerations.
5	Stop Bit	Indicates end of transfer. Always 0.

Table 5-8 Acceleration Control Request Format

LREQ[1:3]	Type	Description
000	ImmReq	Immediate request
001	IsoReq	Isochronous request
010	PriReq	Priority request
011	FairReq	Fair request
100	RdReg	Set register read-out
101	WrReg	Write in the set register
110	AccCtrl	Disable or enable PHY arbitration accelerations.
111	Reserved	Reserved

Table 5-9 Request Type

For the fair request and the priority request, LREQ issuing must be started 1SCLK after the CTL has been idle. If the CTL indicator the PHY is in the Receive mode while the link is issuing these requests or after the link has issued them, the MD8405 cancels these requests. Thus if the request was canceled, the link is required to issue these requests again when the CTL becomes idle.

The request is NOT canceled by 'Receive' if the Enab_accel bit of PHY Register5 is set at 1 and acceleration arbitration (Ack-Acceleration arbitration, Fly-By arbitration) is enabled and when the received packet is found to be the Ack packet (a packet in 8-bit length).

To transfer a cycle start packet, PriReq is issued by the cycle master link.

To transmit an isochronous packet, the link issues a IsoReq during either the cycle start packet or a isochronous packet reception or within 4 SCLK cycle after the packet reception, or during the packet transmission or within 8 SCLK cycle after the packet transmission.

The MD8405 clears IsoReq only if it overcomes the arbitration and transmits Grant to the link, or when a sub-action gap is detected, or when bus reset occurs.

To transmit an Ack packet, the link issues ImmReq during packet reception or within 4 SCLK cycles after packet reception. To satisfy the condition of ACK_RESPONSE_TIME, the link examines the destination_ID of the received packet. After confirming that the received packet is addressed to this node, ImmReq must be issued promptly. The MD8405 acquires the bus immediately after the completion of packet reception and Grant is returned to the link. If the link discovers a CRC error, the link must cancel that request without returning data to that Grant. (See 5-1-4-3 Transmit.)

Shortly after the reception of register write request reception, the MD8405 updates the addressed register with the new data.

Upon reception of the register read request, the MD8405 sends out the output to the link as the state transmission for the addressed data. If this output is interrupted by packet reception/transmission, the MD8405 repeats transmission of the state output, starting with the first bit again, until this state output is finished completely.

When one bus request (FairReq, PriReq, IsoReq, ImmReq) is received, the MD8405 keeps disregarding the next bus request until this request is canceled as a result of packet reception, packet transmission, sub-action gap (for IsoReq or ImmReq only), etc.

If the next register read request is received before the previous register read request is completed, the MD8405 operation becomes unstable.

All bus requests are cleared upon the occurrence of bus reset.

Even when the Enab_accel bit of PHY Register5 is set at 1 and the acceleration arbitration (Ack-Acceleration arbitration, Fly-By arbitration) is enabled, the MD8405 disables the acceleration arbitration of the asynchronous packet while the accelerating bit is 0 according to the acceleration control request.

The MD8405 can enable acceleration arbitration even with IsoReq, by automatically setting up the accelerating bit.

5-1-4-2 Status output

The MD8405 generates an output to the link interface as a status output for the information specified in Table 5-10. The MD8405 asserts 01b at the CTL terminal and transfers the data to the D [0:1] terminal. During the period when the status data is being sent, an output of 01b is generated from the CTL terminal.

For the status output, the MD8405 generates an output with the first 4 bits needed for the link state machine. (Arbitration Reset Gap, Sub-action Gap, Bus Reset, PHY interrupt)

When a register read request is received from the link, however, all status information is output as a return value. During the Self-ID period, the MD8405 automatically generates a status output of address 00h PHY register information, including its own physical_ID, to the link at the point in time when its own Self-ID packet has been transmitted (the point in time when its own physical_ID has been defined).

Status output may be stopped by the reception/transmission of packet and so on. When status output is stopped, the status information is repeated in accordance with the next rule and outputted. The status information is repeatedly output according to the following rules:

- The bits which have been successfully transferred to the link are zeroed.
- Status transfers are commence with S[0:1] in all cases.

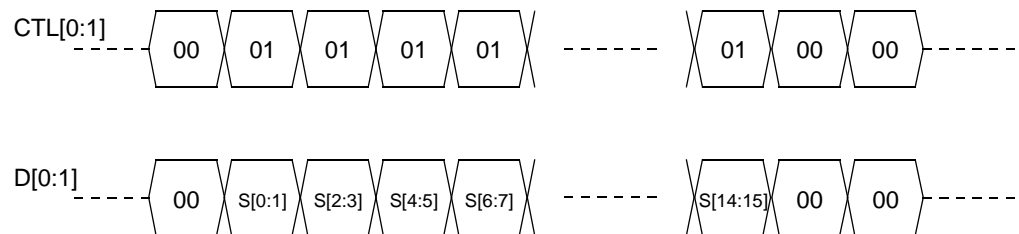


Figure 5-5 Status

Bit(s)	Type	Description
0	Arbitration Reset Gap	The PHY has detected that Serial Bus has been idle for an arbitration reset gap time.
1	Subaction Gap	The PHY has detected that Serial Bus has been idle for a subaction gap time.
2	Bus Reset	The PHY has entered bus reset state.
3	PHY Interrupt	This indicates one or more of the following interrupt conditions: - Loop detect interrupt - Cable power fail interrupt - Arbitration state machine time-out - Port_event interrupt
4~7	Address	Register number
8~15	Data	Register contents

Table 5-10 Status Format

The MD8405 generates a status output as PHY interrupt in the following cases:

- When a condition is detected that the bus configuration is arranged as a loop.
- When reduction of cable voltage is detected.
- When State Machine of MD8405 had time out.
- When a Port_event bit changed in 1.

5-1-4-3 Transmit

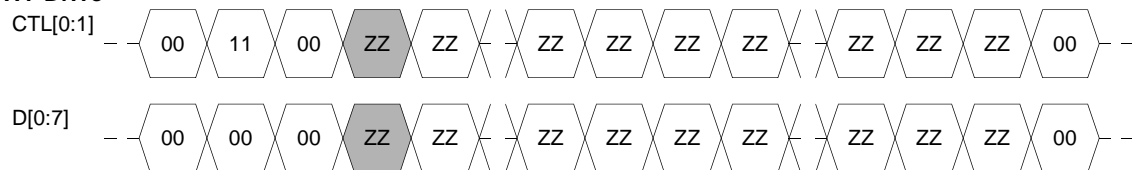
The MD8405 performs arbitration upon reception of a bus request from the link. When MD8405 wins this arbitration, the MD8405 returns 1SCLK cycle Grant 11b and 1SCLK cycle Idle to the CTL terminal as Grant to the link, and gives CTL and D control to the link.

The link the signals either a Transmit (10b) or a Hold (01b) on the CTL terminal for the control of PHY-Link interface. To avoid the collision of data on the CTL bus, however, the MD8405 permits the link to place an input of idle (00b) for 1SCLK only beforehand. (Refer to Fig. 5-6.)

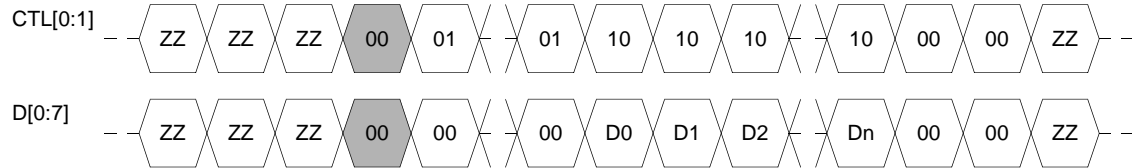
The link can keep using the bus by sending a Hold (01b) to the PHY via the CTL signals until transfer data become ready. In this case, however, the MAX_HOLD time cannot be exceeded. Then the Transmit (10b) code is sent to the PHY to show the data is valid for transfer.

Single Packet

PHY Drive

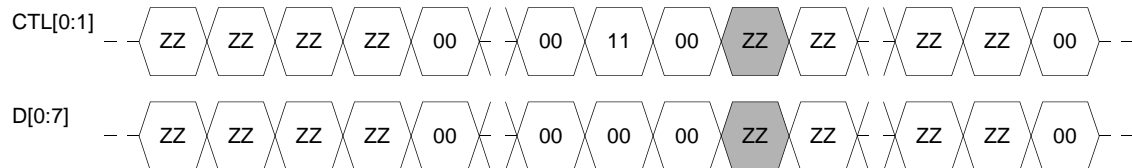


Link Drive



Concatenated Packet

PHY Drive



Link Drive

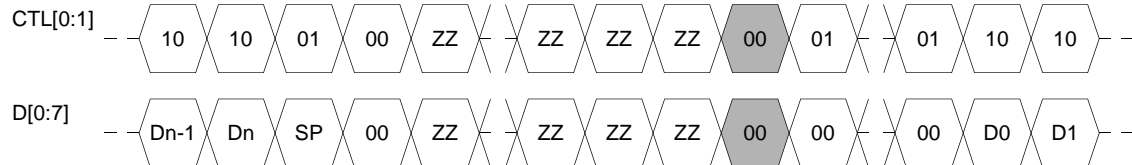


Figure 5-6 Transmit

When the last bit of the packet data has been input, the link sends either 1SCLK Cycle Idle (00b) or Hold (01b) to the PHY. Then Cycle Idle for 1SCLK is sent to the PHY. After that, the MD8405 takes the control of PHY-Link interface. The Hold (01b) command is used to transfer another packet without releasing the serial bus after the link has completed packet transfer (Concatenated Packet). Upon detection of this hold bit, the MD8405 generates an output of Grant to the CTL terminal for the link again, after the lapse of time for MIN_PACKET_SEPARATION. Then, the link performs similar operation for packet transfer.

This holding operation is used when a response packet is transferred after the transmission of an Ack packet or when multiple isochronous packets are transferred in the period of the same isochronous cycle (Sub-action Concatenation).

In the case of concatenated packet transfer, the MD8405 determines the concatenated packet transfer speed according to the setting for the Enab_multi bit of PHY Register5.

If the Enab_multi bit is set at 0, the MD8405 assumes that the packet speed of the second or thereafter packets is identical with the speed of the initial packet.

If the Enab_multi bit is set at 1, the MD8405 identifies the transfer speed of the concatenated packet according to the SP value entered in D while Hold (01b) is input in the CTL. The meaning of this SP value is specified in Table 5-11.

There is, however, a limitation in regard to the transfer speed according to IEEE1394 in the case of concatenated packet transfer. In other words, a packet for S100 transfer cannot be transmitted as a concatenated packet, when preceded by a packet transferred at S200 or above. To observe this speed limitation, the MD8405 will release the IEEE1394 bus and perform an arbitration again in order to send the 100Mbps packet as a single packet if a request of 100Mbps concatenated packet transfer is received after the acceptance of a packet transfer request at 200Mbps or higher. For this reason, a request of 100Mbps concatenated packet transfer attempted from the link is handled in the same manner as for a bus request input with an ordinary LREQ. In such a case, the CTL other than Grant may be returned (the case when a request is canceled).

After the Link gain control of the PHY/LINK interface, the Link can cancel the transfer of a packet in one of two ways. First, if the Link issues an Idle command (00b) for three consecutive SCLKs, the transfer is aborted, the control of the interface is transferred from the Link to the PHY. The other way to abort the transfer is for the Link to issue two consecutive Idle followed by a Hold (01b).

5-1-4-4 Receive

When the MD8405 receives a packet, it sends to the link Receive (10b) on the CTL terminal and FFh on the D terminal. Then, the MD8405 sends out an output of speed code (SP) to start packet data output. Until the completion of data reception, the MD8405 keeps asserting the Receive (10b) at the CTL terminal. After that, the MD8405 sends the Idle (00b) command, and shows that the reception of packet was finished.

During the Self-ID period, the MD8405 also transfers its own Self-ID packet to the link interface as a Receive operation.

Also, the MD8405 outputs a Response packet toward Extended PHY packet for this node as a Receive movement in the Link interface.

After the assertion of Receive, the MD8405 may complete its receiving operation without generating any output of packet data.

If the link is arranged to support 100Mbps only, it is necessary to check the speed code (SP) and disregard the reception packet data of 200Mbps and 400Mbps.

If the link is arranged to support 100/200Mbps only, it is necessary to check the speed code (SP) and disregard the reception packet data of 400Mbps.

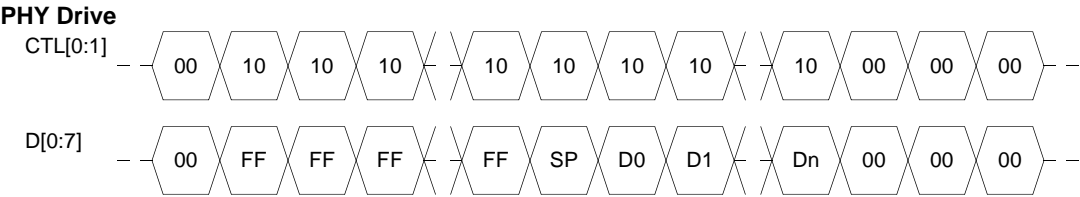


Figure 5-7 Receive

D[0:7]	Data Rate
00XXXXXXb	100Mbps
0100XXXXb	200Mbps
01010000b	400Mbps

Table 5-11 Speed code (SP[0:7])

5-1-4-5 Link interface initialization

The MD8405 performs initialization of the PHY/Link interface as specified by P1394a Draft Ver2.0. Initialization is conducted as specified below, according to the SCLK clock after the assertion of the LPS.

Interface Mode (DIRECT)	
AC connection (DIRECT="L")	DC connection (DIRECT="H")
LPS is asserted and SCLK output is generated thereafter. After the second SCLK, "0" for one clock is driven to CTL[0:1], D[0:7] HiZ is driven for the next 6 clock. At the 8th clock thereafter, "10b" is driven to CTL[0:1] and "FFh" driven to D[0:7].	LPS is asserted and SCLK output is generated thereafter. Up to the 7th clock of that SCLK, "0" is driven to CTL[0:1] and D[0:7]. In addition, CTL[0:1]="10b" and D[0:7]="FFh" are driven at the 8th clock.

Table 5-12 Operation of Link Interface Initialization

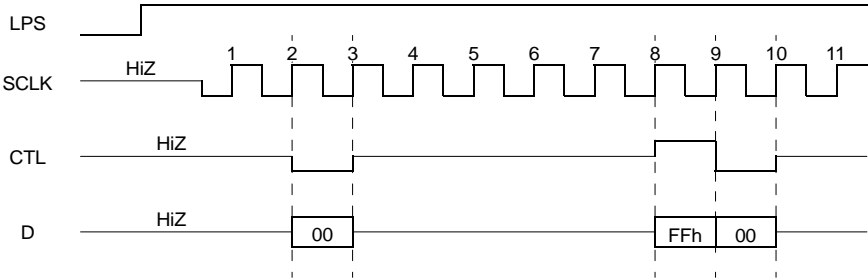


Figure 5-8 PHY/Link Interface Initialization at AC connection

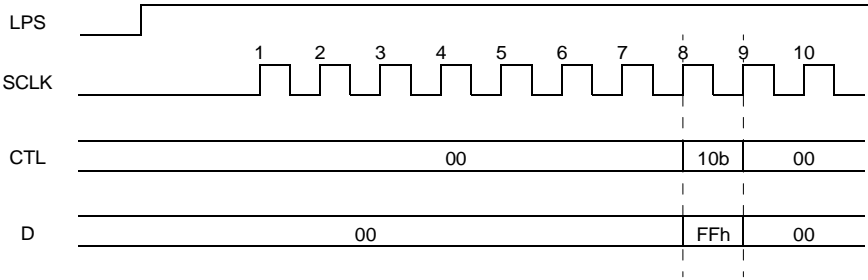


Figure 5-9 PHY/Link Interface Initialization at DC connection

5-1-5 DIRECT

Connection-related definition for the PHY-Link interface is input at this terminal.

When the PHY-Link interface is to operate with a DC connection, this terminal is to be set to High (DVCC).

When the PHY-Link interface is to operate with a AC connection, this terminal is to be set to Low (DGND).

If this terminal is set at L, the MD8405 recognizes that there is an isolation barrier in the PHY-Link interface and an output of logical differential waveform is generated for the CTL and D signals.

(For more details, refer to 5-1-7 Isolation barrier.)

5-1-6 LDSEL

This terminal is used to set up the AC timing for the PHY-Link interface.

As a result of setting at this terminal, it is possible to change the input setup/hold time for the MD8405. This adjustment is for the timing delay caused by the isolation barrier.

Table 6-5 shows the AC timing of the PHY-Link interface arranged for this terminal.

5-1-7 Isolation barrier

For the IEEE1394 bus where the DS (Data-Strobe) encode system is adopted for physical coding, a standard ground potential is directly connected between the opposing nodes to be connected through cables. In other words, the physical layer ID (PHY)-1394 cable-PHY is arranged for DC connections. For this reason, if system equipment units with different standard potentials are connected through the IEEE1394 cables, it is necessary to provide isolation between power supplies of the commercial AC power system and the IEEE1394 physical layer system.

To enable the use of the IEEE1394 bus without depending on the power supply design for system equipment, the PHY-Link interface is designed on the assumption that an isolation circuit is used. An example of isolation barrier circuit is introduced in IEEE P1394a Draft Ver2.0.

The MD8405 supports an isolation circuit defined by the P1394a Draft Ver2.0. It is applicable to no other isolation systems. To use this isolation circuit, the link controller IC side is also required to support the isolation circuit found in the P1394a Draft Ver2.0. There is no limitation as above if a direct connection is made toward the link controller IC without using any isolation circuit.

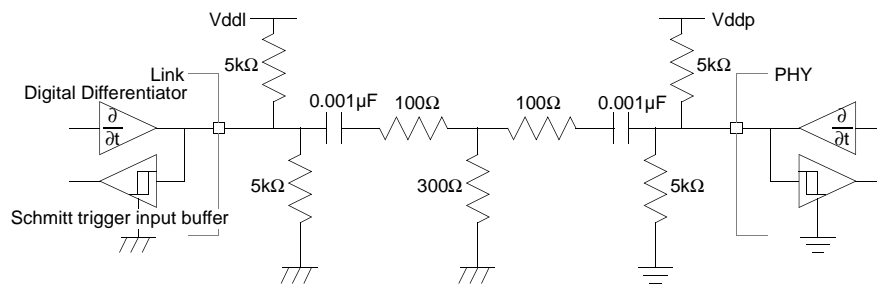


Figure 5-10 IEEE P1394a Draft Ver2.0 Isolation barrier (an example)

Fig. 5-10 shows an example of isolation barrier circuit introduced in IEEE P1394a Draft Ver2.0.

In this section, an operational explanation is presented in regard to the isolation barrier of capacitor type. P1394a Draft Ver2.0 also introduces a transformer type isolation barrier. From a standpoint of withstand voltage for the part to be used, the transformer type generally withstands a greater ground potential difference. From a standpoint of size, however, the capacitor type can be mounted in a smaller board area. The operational principle itself is the same.

At the pre-stage of the output block in the IC, there is a 'digital differential circuit' as shown in Fig. 5-10. The interface is actually 'driven' only for the cycle where the data array of output logic changes from 0 to 1 or from 1 to 0. For the cycle where the data array of output logic makes no change (concatenation of 1 or 0), a state of Z (high impedance) is maintained. Fig. 5-11 shows an example of waveform change before and after the passage through the differential circuit.

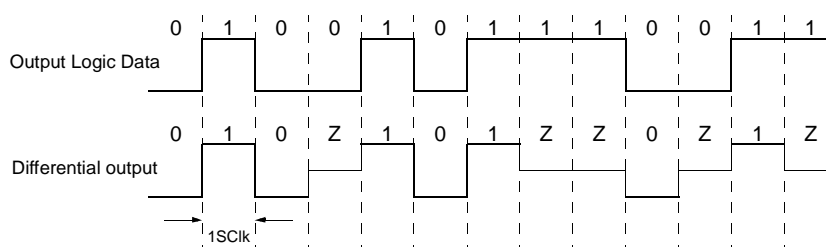


Figure 5-11 Differential Output Waveform in the Driver Circuit

On the other hand, the input block in the IC is composed of a so-called Schmitt trigger buffer having a hysteresis feature in its I/O characteristics. It regenerates the original logical data array after the above-mentioned differential waveform has passed the Schmitt trigger buffer again.

To use an isolation barrier circuit as described above, both the above-mentioned 'digital differential circuit' and the 'Schmitt trigger buffer' are indispensable for the PHY IC and the link controller IC. In the case of direct connection without the use of any isolation circuit, the differential circuit is bypassed and the original output logic data array is directly output to the interface.

Fig. 5-10 shows the 100 ohm series resistors located on both sides of PHY and Link. Usually, however, either side requires such a resistor, functioning as an attenuator that absorbs a source voltage difference between the two ICs. Since the MD8405 is designed for 3.3V driving, a 100 ohm resistor is connected to the Link IC side, only if a link controller for 5V driving is used. With this resistor, the drive waveform in the Link → PHY direction is attenuated. However, the drive waveform in the PHY → Link direction is directly transmitted with a 3.3V amplitude almost unchanged. This series resistor can be a major cause of RC delay together with pin capacitance and such parasitic capacitances. When a link controller for 3.3V driving is used, these series resistors are not required.

Practical circuit operation is explained below, according to Fig. 5-12.

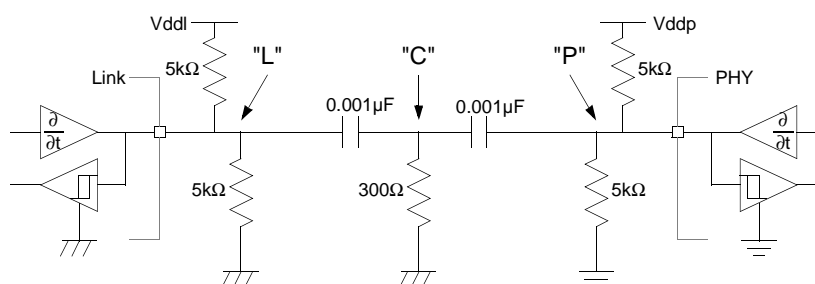


Figure 5-12 Isolation barrier circuit

To make explanations simple, it is assumed that the ground potential difference between PHY and Link is 0V, and both PHY and Link are designed for 3.3V operation. Since the DC potential difference is always stored in the 0.001μF capacitor, AC operation can be studied in the same manner as when the potential difference is 0V.

When both ICs of PHY and Link are in the state of Z (high impedance) output, Vdd/2 is maintained at the I/O pin (Node P hereafter) of the PHY IC and the I/O pin (Node L hereafter) of the Link IC respectively, because of 5k ohm resistance division. (At that time, the logic level before assuming the state of Z is successively 'received' by the function of Schmitt trigger buffer inside.) On the other hand, the remaining center node (Node C hereafter) is maintained at 0V because of 300 ohm.

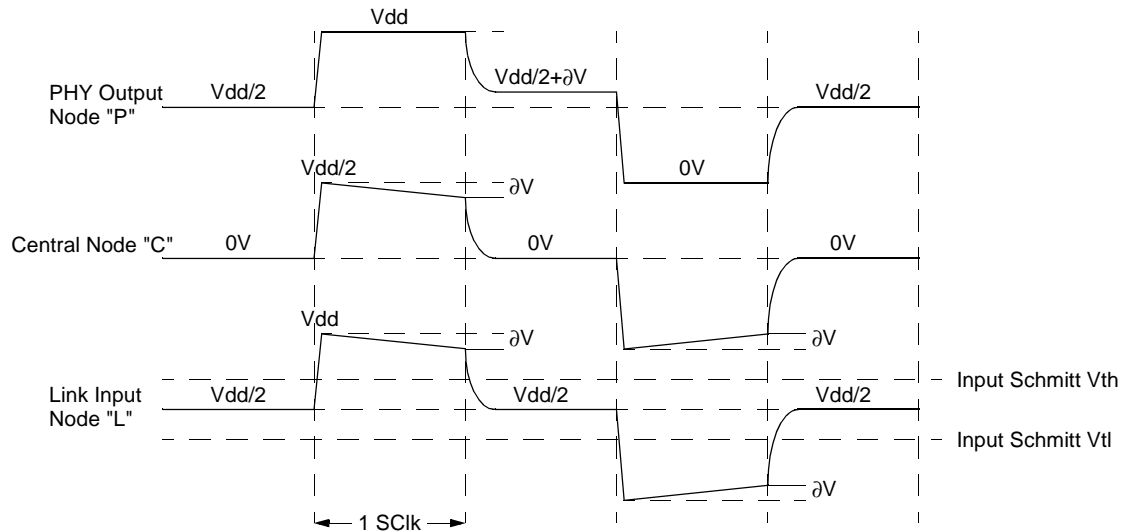


Figure 5-13 Example of waveform at each node

When 1 is driven by the PHY, Vdd is maintained at Node P. This potential change of $V_{dd}/2 \rightarrow V_{dd}$ is transmitted to Node C, and further to Node L. As a result, there is a potential rise of $0 \rightarrow V_{dd}/2$ at Node C, and $V_{dd}/2 \rightarrow V_{dd}$ at Node L. At Node P, Logic 1 or Potential Vdd is maintained for one cycle. At Node C, the potential is discharged through 300 ohm but the time constant at that time is $300[\text{ohm}] \times 0.001[\mu\text{F}] = 0.3\mu\text{sec}$ and this setting is far longer than one cycle ($= 20 \text{ nsec}$). Therefore, potential drop ΔV is feeble during one cycle. (To be explained later) The waveform at Node C is directly transmitted to Node L and after all, the step waveform of $Z \rightarrow 1$ driven by PHY is directly sent to the link almost without change.

If the output logic data to be sent in the next cycle is 0, there is a change of $V_{dd} \rightarrow 0$ at Node P, succeeding the above operational sequence. By similar operation, there is a change of $V_{dd}/2 \rightarrow V_{dd}/2$ at Node C, and a change of $V_{dd} \rightarrow 0$ at Node L.

On the contrary, if the output logic data to be sent in the next cycle is 1 and the same as that of the previous cycle (as shown in Fig. 5-13), the PHY arranges the output buffer for Z with the previously described 'digital differential circuit'. At that time, the remaining low-impedance node is only C and the same potential change takes place at Node P ($V_{dd} \rightarrow V_{dd}/2$) and Node L ($V_{dd} \rightarrow V_{dd}/2$) upon the recovery of the initial value at Node C that is $V_{dd}/2 \rightarrow 0$. At that time, the time constant is set at $2 \times 300[\text{ohm}] \times 10[\text{pF}] = 6 \text{ nsec}$ that is far smaller than one cycle ($= 20 \text{ nsec}$), assuming that the pin capacitance is 10pF, for example. At Node L, the potential returns to $V_{dd}/2$ again but the logic level 1 is successively received at the Schmitt trigger buffer in the input block. Strictly speaking, Node C performs a voltage drop of ΔV due to discharges during the cycle when the PHY is driving 1. For this reason, the amplitude is $V_{dd}/2 - \Delta V$ when Node C recovers the initial value of 0V. At Node P on the driving side, a potential change of $V_{dd} \rightarrow V_{dd}/2 + \Delta V$ appears but the initial value of $V_{dd}/2$ is not recovered. ($V_{dd}/2$ is recovered at Node L on the receiving side.)

This difference ΔV is canceled when the PHY drives 0 in the next phase (Fig. 5-13). As such, this difference cannot be accumulated in the future. (The 'digital differential circuit' always functions to put one 1SClk cycle of 0, after the driving of one 1SClk cycle1 and before the driving of next one.)

Fig. 5-14 to Fig. 5-19 show the isolation barrier circuit concerned with each link interface pin.

LREQ, CTL[0:1], and D[0:7] use isolation barrier circuits of the above-mentioned IEEE1394-1995 Annex J type. LPS and SCLK intended to produce clock waveforms of duty factor 50% use comparatively simplified AC connection circuits.

The LPS input block is a CMOS receiver. When a clock signal from the Link IC stops, the potential lowers below the CMOS input threshold level due to the effect of the external resistance. If this L period continues for $2.56\mu\text{sec}$, the condition of $LPS=L$ is identified. If the H period continues for 80n sec on the contrary, the condition of $LPS=H$ is then identified. In the case of AC connection, the SCLK calls for a Schmitt trigger input buffer on the link side. The CMOS output appears on the MD8405 side.

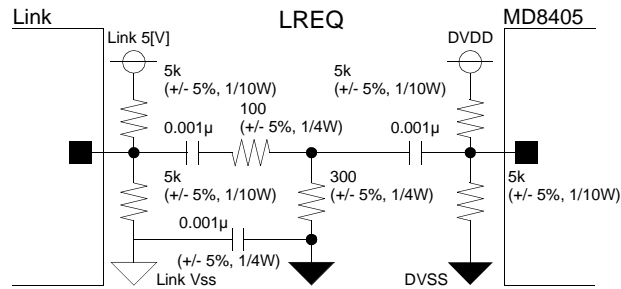


Figure 5-14 LREQ isolation barrier circuit

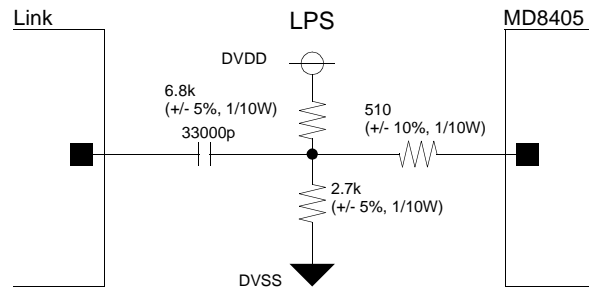


Figure 5-15 LPS isolation barrier circuit

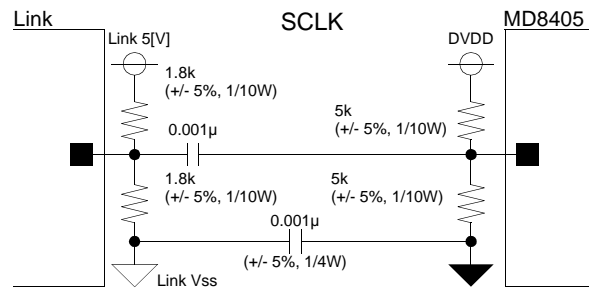


Figure 5-16 SCLK isolation barrier circuit

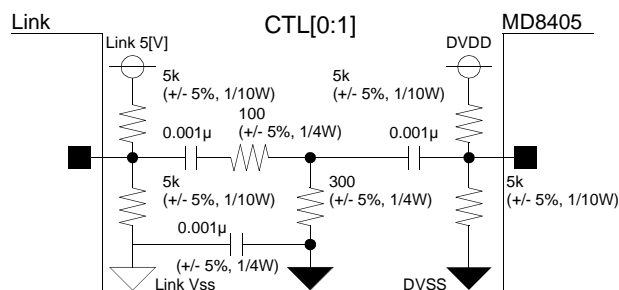


Figure 5-17 CTL[0:1] isolation barrier circuit

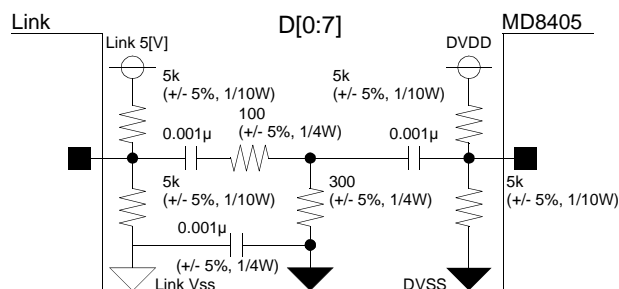


Figure 5-18 D[0:7] isolation barrier circuit

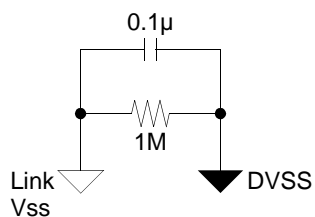


Figure 5-19 VSS connections

In Fig. 5-14 (LREQ), Fig. 5-17 (CTL[0:1]), and Fig. 5-18 (D[0:7]), the 100 ohm resistors inserted in series with the link side are required only if the link chip I/O section source voltage of 5V. They are not required if the link chip works at a source voltage of 3.3V.

5-2 Cable interface

5-2-1 Cable interface circuit

Fig. 5-20 shows a connection circuit for the cable interface.

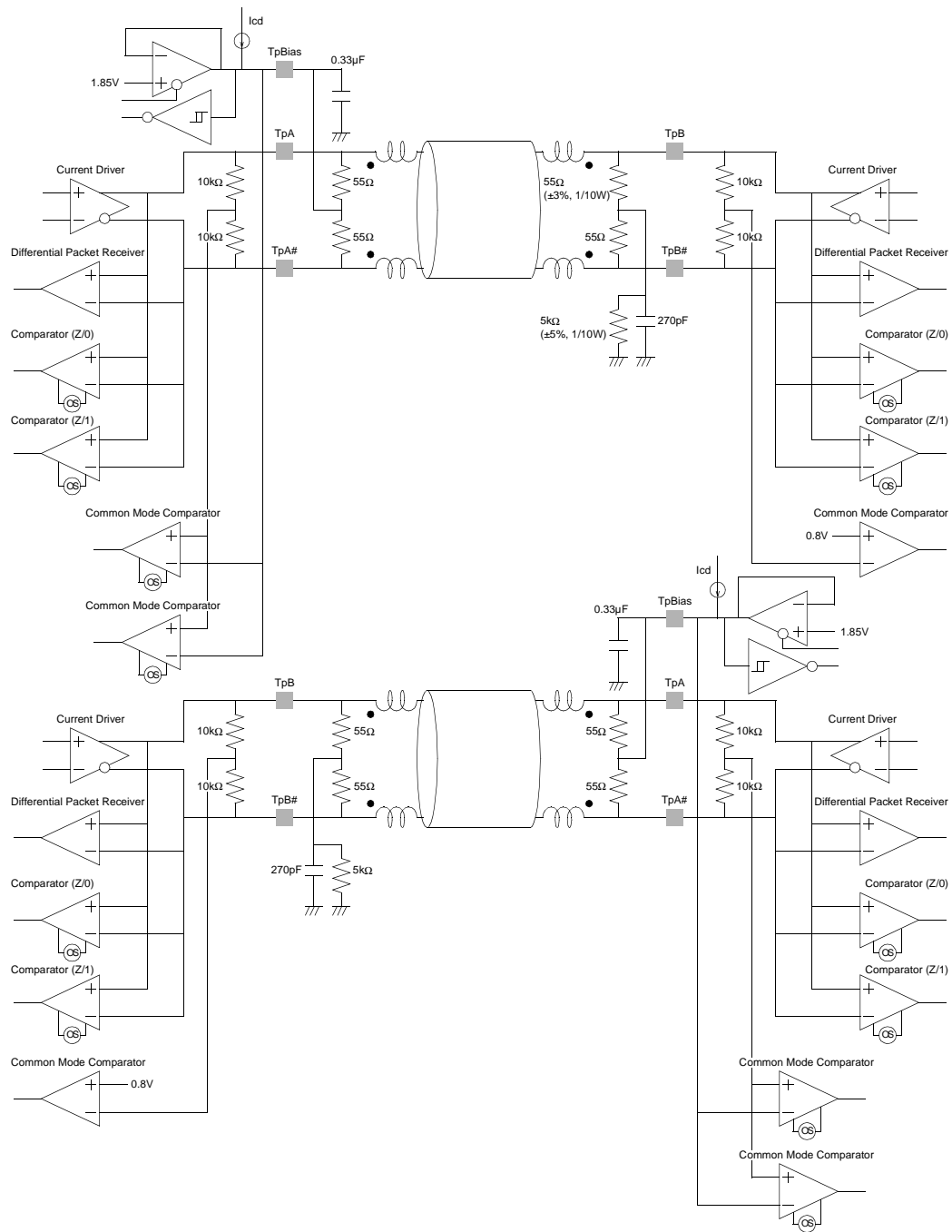


Figure 5-20 Cable interface

Exclusively designed IEEE1394 cables are used as cable media. For data exchange, two sets of shield-twisted pairs are used. As shown in Fig. 5-20, each twisted pair cable is connected so that the TpA pair of its own node is connected to the TpB pair of the distant node.

Both TpA and TpB sides call for a termination resistance of $55\ \text{ohm} (\pm 3\ \text{ohm}, 1/10\text{W}) \times 2$, according to the cable impedance. The cabling distance from this termination resistance to the IC pin should be arranged as short as possible.

To set up a cable's common-mode DC potential on the TpA side, a TpBias (standard 1.85V) is connected to the center node of the termination resistance. A capacitor of $0.33\ \mu\text{F}$ for decoupling should be connected to the TpBias. For the speed signal to be described later, the common-mode current is fed from here. This capacitor is also intended for internal OPE AMP phase compensation. Therefore, it is required even though the TpBias is not used practically (unused port, etc.).

On the TpB side, $5\ \text{kohm} (\pm 5\%, 1/10\text{W})//270\text{pF} (10\text{V})$ should be connected for pull-down to the center node of the termination resistance. By this resistance, if the cable is pulled out and the DC bias from the distant node TpA is interrupted, the DC potential on the TpB side drops as low as 0V and this can be sensed at the common-mode comparator. 270pF is used for decoupling.

The balun placed between the termination resistance and the cable, shown in Fig. 5-20, is a common-mode coil ($250\ \text{nH}$, $K > 0.97$) intended for the band limitation of the common-mode signal. When it is used, it should be connected in this position. It offers an effect of reducing the electromagnetic emission (EMI) due to common-mode noise generated at the signal changing point. There is no influence on data exchange, and there is no problem in communications even though it is not used.

5-2-2 Outline description of cable interface operation

The communication phase toward the opposing node is roughly classified into 'arbitration' and 'data packet exchange'. Arbitration exchange is effected in the tristage logic (differential) of 0, 1, and Z, and in full-duplex communication mode. The speed signal (common mode) is superposed on this communication. Packet exchange is effected on the basis of the binary logic (differential) of 0 and 1, and in half-duplex communication mode. In any case, transmission employs a high-impedance current driver and reception is effected by detecting a differential voltage at both ends of termination resistance or a common-mode voltage by the use of a comparator and a packet receiver.

The signals exchanged at TpA and TpB are as specified below.

TpA:	Differential signal	Arbitration exchange, packet transmission (Strobe signal), packet reception (Data signal)
	Common-mode signal	Speed signal reception Cable bias (TpBias)
TpB:	Differential signal	Arbitration exchange, packet transmission (Data signal), packet reception (Strobe signal)
	Common-mode signal	Speed signal transmission Connect status detection

Fig. 5-21 shows an example of current driver status during data transmission of various kinds, currents carried in cables, differential and common-mode voltage waveforms observed at the termination resistance. (Fig. 5-21 explains the status of each signal. It does not show any waveform in a specific bus phase.) (The example shown is for a speed signal of S200.)

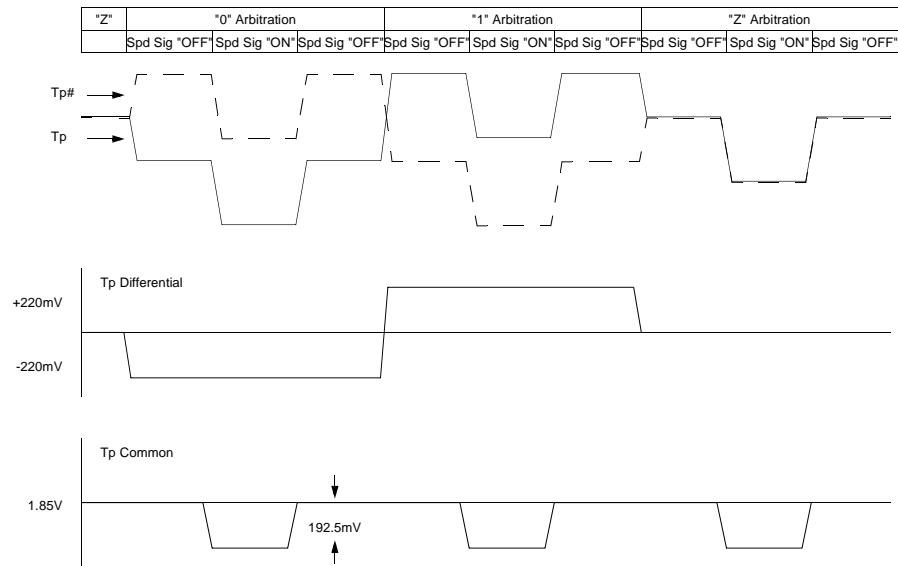
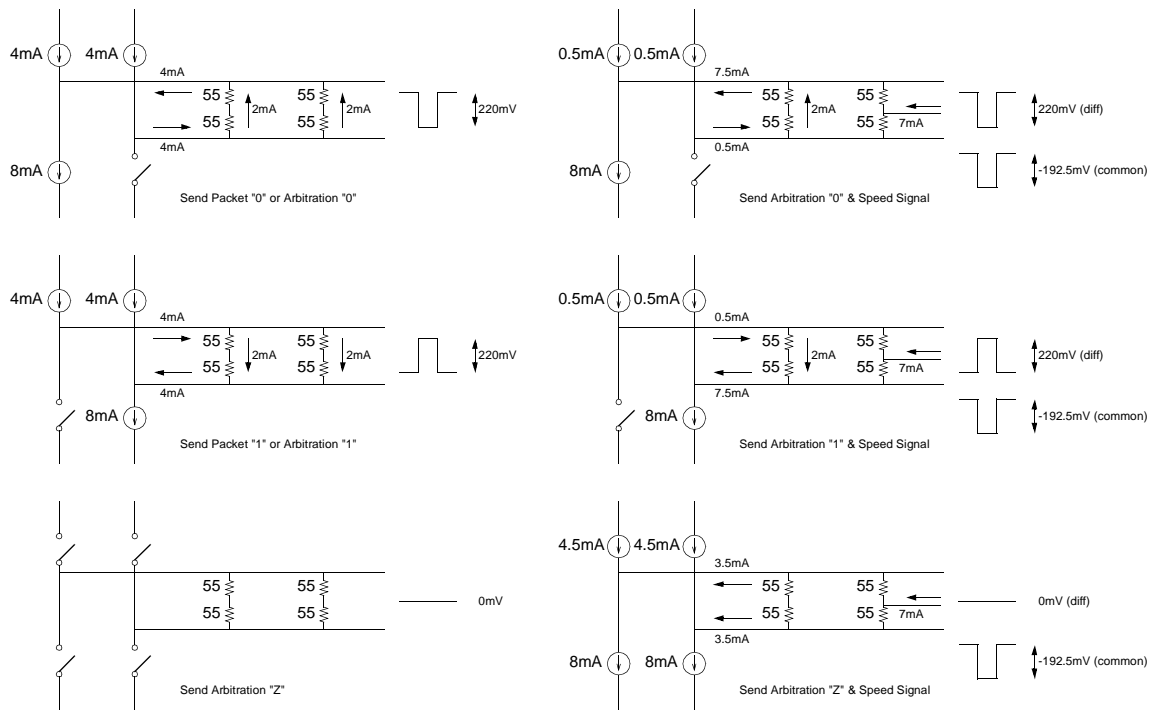


Figure 5-21 Driver currents and Output waveforms (for S200 Speed Signal)

5-2-3 Port State

The MD8405 is designed in accordance with P1394a Draft Ver2.0. In the P1394a Draft Ver2.0, the following four types of state are defined:

- | | |
|--------------|---|
| Disabled | : This port does not generate any signal output to TpBias and TpA/TpB. It does not detect any signal input to Bias and TpA/TpB. The connection detector circuit only operates in this port.
When any change in cable connection state is detected at the connection detector circuit, an interrupt output by State/LinkOn is generated and sent to higher layers, provided that the int_enable bit has been set. |
| Disconnected | : This port has no physical cable connections toward another node PHY. Therefore, there is no signal output toward TpBias and TpA/TpB. It does not detect any signal input to Bias and TpA/TpB. The connection detector circuit only operates in this port. |
| Suspend | : This port has physical cable connections toward another node PHY. However, there is no signal output toward TpBias and TpA/TpB. It does not detect any signal input to TpA/TpB. The bias detector circuit and the connection detector circuit only operate in this port. |
| Active | : This port has physical cable connections toward another node PHY and there are signal outputs toward TpBias and TpA/TpB. In addition, the signal inputs in Bias and TpA/TpB are detected. |

According to the result of comparison with port power consumption in active state, the MD8405 lowers power consumption of ports in the suspended, disabled, or disconnected state.

If all three ports are in the state other than active, the LPS signal is at the Low level, and the Link is non-active, then the MD8405 automatically assumes the low power consumption mode. In the mode of low power consumption, power consumption is extremely reduced compared with regular operation. (See 6-3 DC Characteristics.)

5-2-4 Connection detector circuit

To examine physical cable connections, the MD8405 incorporates a connection detector circuit. This circuit detects the presence of any physical connections toward the port while the port does not generate the TpBias output.

5-2-5 Suspend/Resume

Transition from Active State to Suspended State is performed in one of two ways.

In one case, a Remote Command packet may be received or transmitted, where a suspend bit has been set up for the port that has this node. This Remote Command packet may be transmitted from a local link of this node or from any other node. In any case, the MD8405 sends out the Remote Confirmation packet to all ports after the transmission or reception of the Remote Command packet. Since then, a bus reset signal is output to the ports other than the port (suspend indicator) where the suspend bit has been set up. As a result, this port moves to the suspended state.

In the other case, a TX_SUSPEND signal output may be received from the suspend initiator (RX_SUSPEND). The port (suspend target), which has received the RX_SUSPEND, then moves to the suspended state. This node also sends out an output of TX_SUSPEND to the active ports other than the port where the RX_SUSPEND signal has been received. Thus these ports remain in the state of suspend initiator. The suspend initiator ports also move to the suspended state.

As described above, the suspended state is propagated as far as the leaf node. However, propagation of the suspended state is stopped when encountering a port of IEEE Std1394-1995, a disabled port, or a suspended port is encountered on the way.

If the port has identified a bias in the destination port even in the suspended state, a fault bit is set up to indicate that a normal suspended state is not assumed.

The port in the suspended state begins to perform Resume operation and moves to the active state, in the following cases:

- When a Fault bit is cleared and a Bias is detected.
- When a Resume packet is transmitted or received.
- When a Remote Command packet is transmitted or received, for which the resume bit has been set to this port.

If this is not a Boundary node and a Resume operation is started for any reason other than the transmission or reception of the Resume or Remote Command packet in the port that is in the suspended or disconnected state, any suspended port other than this port also begins to perform Resume operation at the same time.

Resume operation is normally finished and it moves to the active state after the TpBias output is sent out and the Bias signal from the distant node is detected. If no bias is detected from the distant node, a Fault bit is set up and the suspended state is assumed again to indicate that there has been no normal completion of Resume operation.

5-2-6 Suspend/Resume OFF mode (Terminal SR = "L")

In the mode where no Suspend/Resume functions are used, the MD8405 performs the following operation:

- Remote Command packet is disregarded.
- Resume packet is disregarded.
- The Disabled, int_enable, and Resume_int bits of the PHY register are disregarded.
- Connections are detected with a Bias. (According to P1394a Draft Ver1.3)

```
void connection_status() { // Continuously monitor port status in all states
int i;
isolated_node = TRUE; // Assume true until first connected port found
for (i = 0; i < NPORT; i++) {
    isolated_node &= !connected[i];
    if (connection_in_progress[i]) {
        if (!port_status[i])
            connection_in_progress[i] = FALSE; // Lost attempted connection
        else if (connect_timer >= (isolated_node)
            2 * CONNECT_TIMEOUT :
CONNECT_TIMEOUT) {
            connection_in_progress[i] = FALSE;
            connected[i] = TRUE; // Confirmed connection
            if (isolated_node) // Can we arbitrate?
                ibr = TRUE; // No, transition to R0 for reset
            else
                isbr = TRUE; // Yes, arbitrate for short reset
        }
    } else if (!connected[i]) {
        if (port_status[i]) { // Possible new connection?
            connect_timer = 0; // Start connect timer
        }
    }
}
```

```
        connection_in_progress[i] = TRUE;
    }
} else if (!port_status[i]) { // Disconnect?
    connected[i] = FALSE; // Effective immediately!
    if (child[i]) // Parent still connected?
        isbr = TRUE; // Yes, arbitrate for short reset
    else
        ibr = TRUE; // No, transition to R0 for reset
}
}
```

- The port state is only for Disconnected (!Connected) and Active (Connected). (Conforming to P1394a Draft Ver1.3)

In any state, an output of 1.85V is output to TpBias. However, TpBias is pulled down during the hardware reset period.

5-2-7 Low power consumption (Power Down) mode

The conditions for PowerDown are as follows:

- 1) When LPS is L and Link is non-active, and
- 2) When LinkOn output is not generated, and
- 3) All ports are in the state of Disconnected, Suspended, or Disabled.

When all of the above conditions are met, PowerDown can take place after waiting for 680ms.

The conditions for Resetting are as follows:

- 1) When LPS is H, or
- 2) When CPS reduction is detected, or
- 3) When Connect is detected in a Disconnected port, or
- 4) When !Connect is detected in a Suspended port, or
- 5) When Bias is detected in a Suspended port, or
- 6) When Bias is detected in a Suspended and Suspend_fault port, or
- 7) When a change in Connect is detected in a Disabled and Int_enable port.

The present operation is restored to regular operation after the lapse of about 11 to 12ms.

Operation takes place as if no PowerDown were performed. However, when the resetting conditions are as described above, the following operation takes place:

- 1) LCLK output
- 2) LinkOn (Interrupt)
- 3) connection_status(), P0:P1
- 4) connection_status(), P5:P0
- 5) connection_status(), P5:P1
- 6) connection_status(), P5:P5
- 7) LinkOn (Interrupt)

5-2-8 S200 mode (S200 terminal = "H")

In the S200 mode, the MD8405 performs the following operation:

- An output of 01 is given to the sp bit of the Self-ID packet that is transmitted from the MD8405, in order to indicate that the maximum operating frequency of this node is 196.608Mbit/s.
- An output of 001 is given to the Max_speed bit of the PHY register, in order to indicate that the maximum operating frequency of this node is 196.608Mbit/s.
- A speed signal output of S200 is generated during the Self-ID period, in order to indicate that the maximum operating frequency of this node is 196.608Mbit/s.

In this mode, the D[4:7] terminal should be used as the NC.

In this mode, the bus request of 400Mbps should not be input from the LREQ terminal.

5-2-9 CPS (Cable Power State)

The CPS pin should be connected to cable power (V_p) through the external resistor R_{cps} (generally $220\text{k}\Omega$). This connection is intended to detect a condition that cable power has lowered below the threshold level (generally 7.5V). If this arrangement is not required, this connection should be extended to AVDD.

The relationship between the detection threshold value V_t and the external resistor R_{cps} is given by the expression shown below.

$$V_t = 1.85 + R_{cps} \times 25\mu$$

5-2-10 Handling of unused ports

The MD8405 employs three ports. If only one or two ports are used, the following connections should be made for the unused port terminals:

Unused Port Name	Connection
TpAp, TpAn	Not connected
TpBp, TpBn	AVSS
TpBias	To AVSS via $0.33\mu\text{F}$

Table 5-13 Treatment for Unused Port Terminals

For example, the circuit diagram shown below on the assumption that only one port is used.

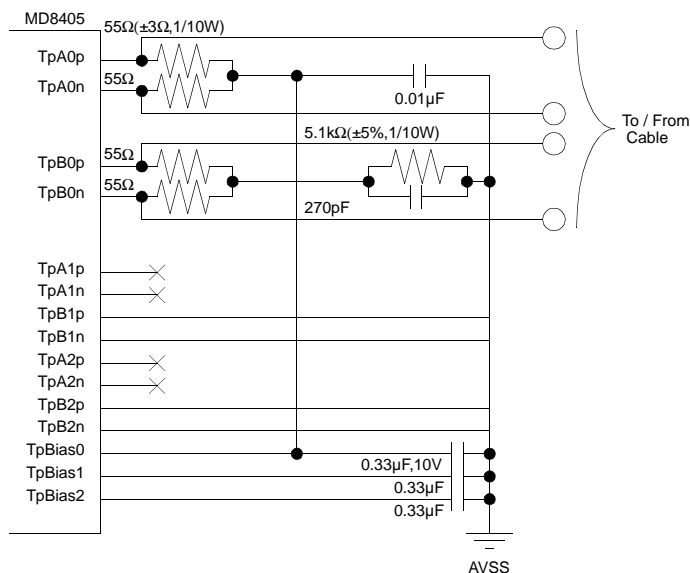


Figure 5-22 Circuit diagram when only one port is used

5-3 Clock Circuit

5-3-1 Crystal oscillator

The output frequency of this oscillator is required to be $24.576\text{MHz} \pm 100\text{ppm}$. The crystal itself requires an accuracy of $\pm 50\text{ppm}$ under the condition that a load capacitance of 10pF is connected.

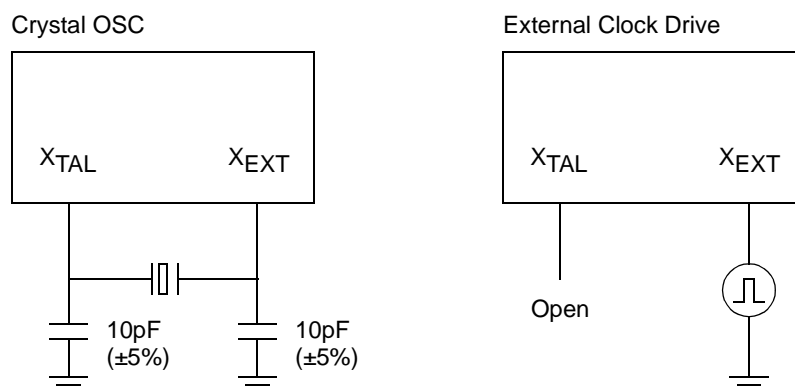


Figure 5-23 Clock Drive Condition

5-3-2 PLL

A PLL is used to produce 393.216MHz . This frequency is 16 times the 24.576MHz produced by the crystal oscillator.

The PLL lock time is $100\mu\text{sec}$ or less.

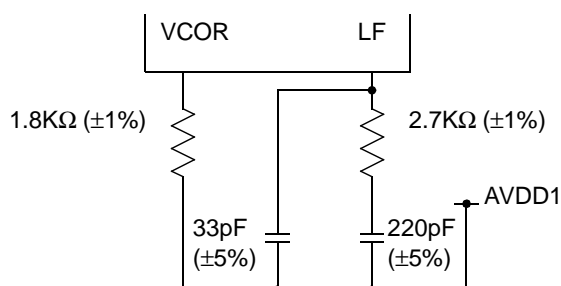


Figure 5-24 PLL External Circuit

5-4 External Circuit

5-4-1 CPS Terminal

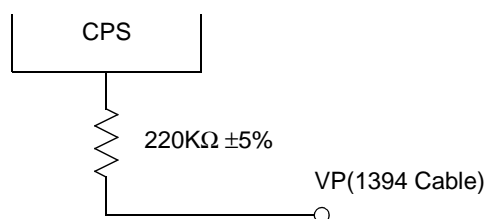


Figure 5-25 CPS External Circuit

5-4-2 Rext Terminal

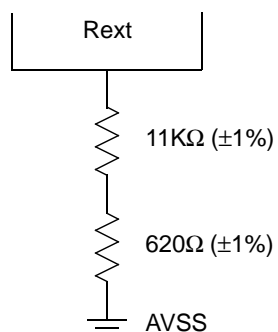


Figure 5-26 Rext External Circuit

5-4-3 Vref Terminal

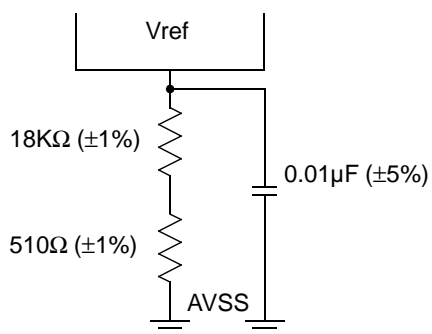


Figure 5-27 Vref External Circuit

5-5 Hardware Reset

A reset width of a minimum of 15msec is produced during power up, by connecting the Purb terminal to ground via an external capacitor of 0.1 μ F. By applying the "L" level externally to this terminal, all state machines are reset.

At that time, operation of the cable interface is as described below.

- 1) The MD8405 maintains TpBias at 0V (Pull Down) while Purb is kept at the "L" level.
- 2) After the completion of reset, physical cable connections are examined in the time period of CONNECT_TIMEOUT. During this time, TpBias is kept in the HiZ state.
 - To state 3) if no connection is confirmed. (P0 for port connection state machine)
 - To state 4) if any connection is confirmed. (P0:P1 for port connection state machine)
- 3) Disconnected. The connection detector circuit only is in operation.
- 4) Resumed. An output of 1.85V is given to TpBias, waiting for a Bias signal from the distant node in the time period of BIAS_HANDSHAKE.
 - To state 5) if a Bias signal is detected from destination in the time period of BIAS_HANDSHAKE. (P1:P2 for port connection state machine)
 - To state 6) if no Bias signal is detected from destination in the time period of BIAS_HANDSHAKE. (P1:P5 for port connection state machine)
- 5) Regular operation will begin (Active) with the next bus reset. The Bias detector circuit is in operation.
- 6) Suspended. TpBias is maintained at 0V (Pull Down). Then the TpBias is turned HiZ to actuate the connection detector circuit. The Bias detector circuit is also in operation.

6 Electric characteristics

6-1 Absolute rating

(VSS=0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	-0.5~5.0	V
VIN	Input voltage	-0.5~VDD+0.5	V
VOUT	Output voltage	-0.5~VDD+0.5	V
TSTG	Strong temp.	-65~150	deg.

Table 6-1 Absolute rating

6-2 Recommended operating condition

Symbol	Item	Rating	Unit
VDD	Supply voltage	3.0~3.6	V
VIN	Input voltage	0~VDD	V
VOUT	Output voltage	0~VDD	V
TA	Ambient temp.	0~70	deg.

Table 6-2 Recommended operating condition

6-3 DC Characteristics

Electrical characteristics under the recommended operating conditions are as specified below. (For no particular exceptions)

(VSS=0V)

Symbol	Item	Terminal	Test Condition	MIN	TYP	MAX	Unit
VT+	Input Schmitt rising threshold value	LREQ, CTL[0:1], D[0:7]		VDD/2+0.3		VDD/2+0.8	V
VT-	Input Schmitt lowering threshold value	LREQ, CTL[0:1], D[0:7]		VDD/2-0.8		VDD/2-0.3	V
VIH	H level input voltage	LPS, LDSEL, DIRECT, PC[0:2], Disabled[0:2], En_Accel, En_Multi, CMC, XEXT		VDD-1.0			V
VIL	L level input voltage	LPS, LDSEL, DIRECT, PC[0:2], Disabled[0:2], En_Accel, En_Multi, CMC, XEXT				1.0	V
IIH	H level input current	LREQ, CTL, D[0:7]	VIH=VDD	-10			
		LPS, LDSEL, DIRECT, PC[0:2], Disabled[0:2], En_Accel, En_Multi, CMC	VIH=VDD	-10			μA
IIL	L level input current	LREQ, CTL, D[0:7]	VIL=VSS			10.0	
		LPS, LDSEL, DIRECT, PC[0:2], Disabled[0:2], En_Accel, En_Multi, CMC	VIL=VSS			10.0	μA
VOH	H level output voltage	SCLK, CTL[0:1] D[0:7]	IOH=-12mA	VDD-0.4			V
		LinkOn	IOH=-6mA	VDD-0.4			
VOL	L level output voltage	SCLK, CTL[0:1] D[0:7]	IOH=+12mA			0.4	V
		LinkOn	IOH=+6mA			0.4	
IDD	Dynamic current consumption		VDD=3.6V 3 port transmission			195	mA
IDDS	Static consumption electric current		VDD=3.6V no transmission, reception.			110	mA
IDDS2	At the PowerDown, consumption electric current		VDD=3.6V no cable connection. LPS=L			19	mA

Table 6-3 DC characteristics (Link interface)

Symbol	Item	Test Condition	MIN	TYP	MAX	Unit
VOD	Differential output amplitude	Load 55 ohm	175		265	mV
VTPBIAS	TpBias output voltage	Source 3[mA], Sink 1.3[mA]	1.72		1.92	V
ICM	Tp Tp common-mode current	Driver disable (Z state)	-25		5	μA
		Driver enable other than speed signal	-0.18		0.18	mA
ISPD2	TpB200Mbit TpB200Mbit speed signal		2.76		4.6	mA
ISPD4	TpB400Mbit TpB400Mbit speed signal		8.4		11.5	mA
ZDIFFZ	Differential input , Impedance	Driver disable (Z state)	21.0		4	pF
ZDIFFEN	Differential input , Impedance	Driver enable	3.4		4	k ohm pF
CCM	Common-mode input capacitance	Tp pin short , Z-state driver			16	pF
VT NOCONN	Non-live threshold voltage	TPB common-mode voltage	0.64		0.96	V
VT CPWD	CPS threshold voltage	Vp pin (R=220k ohm)	6.0		7.6	V

Table 6-4 DC characteristics (Cable interface)

6-4 AC characteristics

Symbol	Item	LDSEL=0			LDSEL=1			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
TSU	D, CTL, LREQ, setup time	6			2			ns
TH	D, CTL, LREQ, holding time	0			5			ns
TD	D, CTL, output timing	2		10	2		10	ns
TCLK	SCLK cycle time	20			20			ns
TCLKH	SCLK H-level time	9		11	9		11	ns
TCLKL	SCLK L- level time	9		11	9		11	ns
TLINKON	Link-On cycle time	160			160			ns

Table 6-5 AC characteristics

Symbol	Item	Test Condition	MIN	MAX	Unit
TTJITTER	TpA, TpB transfer jitter			± 0.15	ns
TTKEW	TpA strobe TpB data transfer skew			± 0.10	ns
TTRF	TpA, TpB transfer Rise and lower	10% to 90% via 55 ohm and 10pF		1.2	ns

Table 6-6 AC characteristics (Twist pair interface)

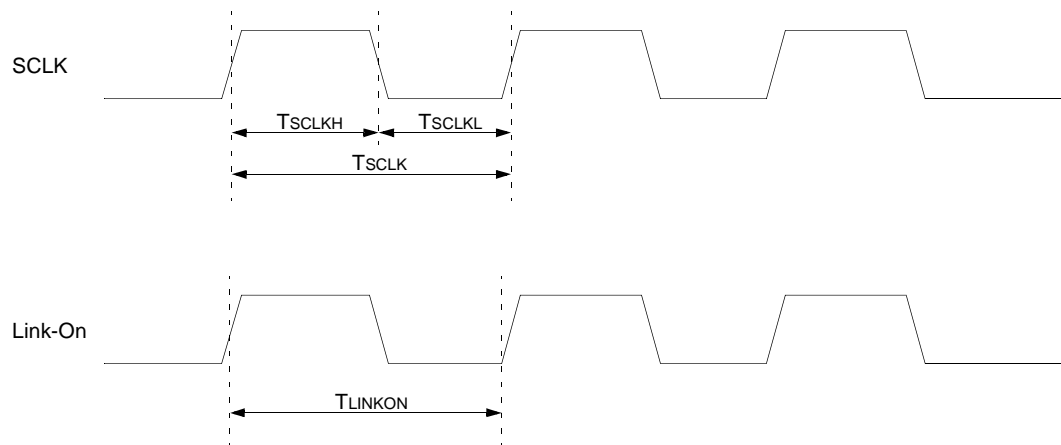


Figure 6-1 Link interface AC characteristics (SCLK, Link-On)

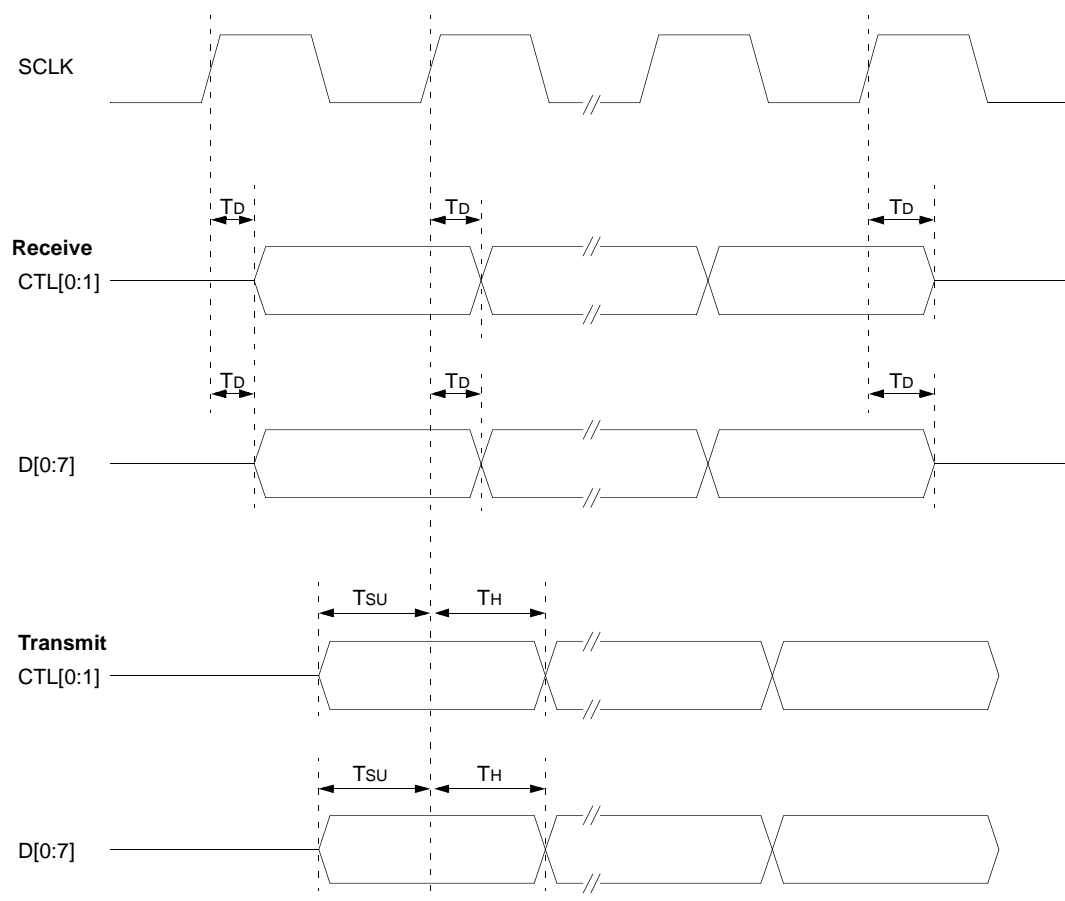


Figure 6-2 Link interface AC characteristics (CTL,D)

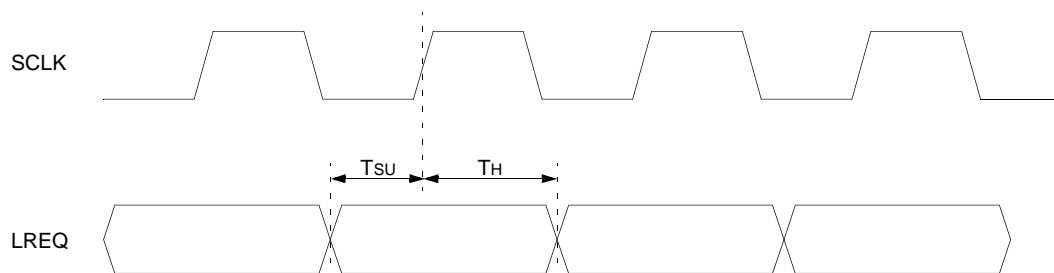


Figure 6-3 Link interface AC characteristics (LREQ)

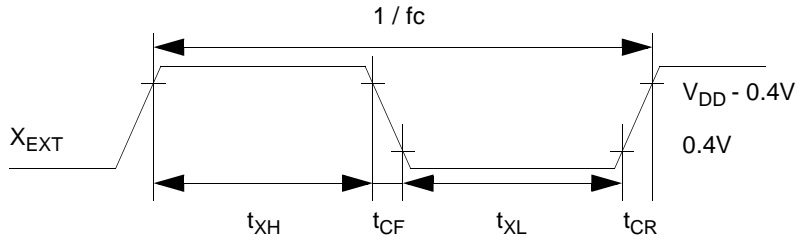


Figure 6-4 Clock Timing

Item	Sign	Terminal	Condition	MIN	TYP	MAX	Unit
Clock Frequency	f_c	X_{TAL} X_{EXT}			24.576 $\pm 100\text{ppm}$		MHz
Input Clock Pulse Width	t_{XL} t_{XH}	X_{EXT}	External Clock Drive	8			nS
Input Clock Rise & Fall	t_{CR} t_{CF}	X_{EXT}	External Clock Drive			10	nS
Input Clock Drive Current	I_{OL} I_{OH}	X_{EXT}	External Clock Drive	10			mA

Table 6-7 Clock Circuit AC characteristics



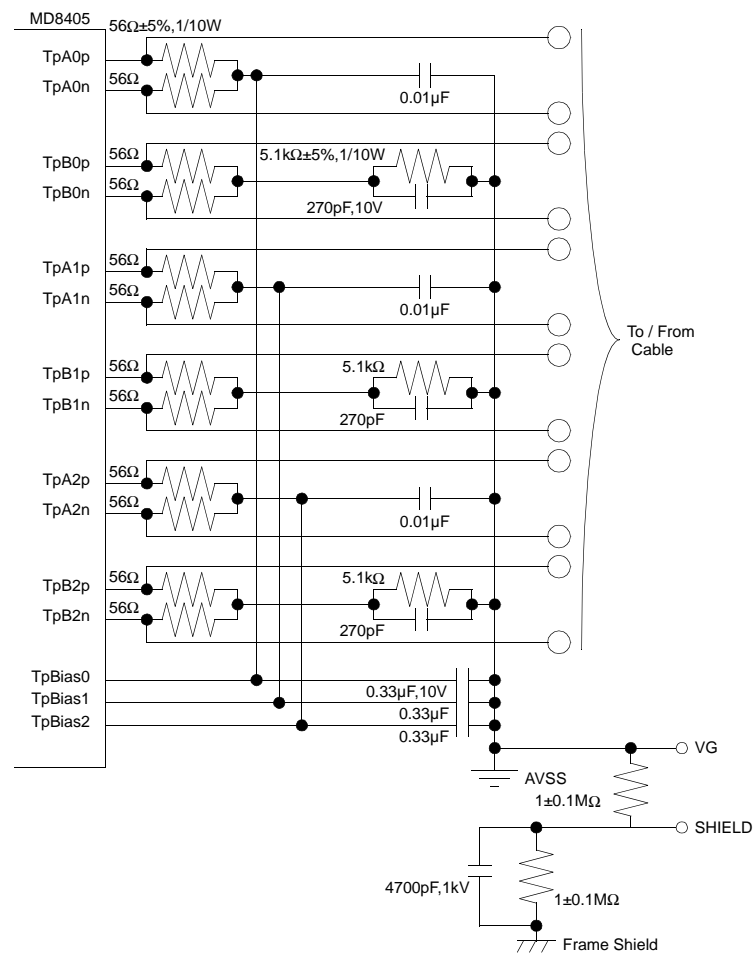


Figure 7-2 Cable Interface Connection Circuit

- Cable Interface (TPA,TPB) needs low inductance.

8 Package External Dimensions

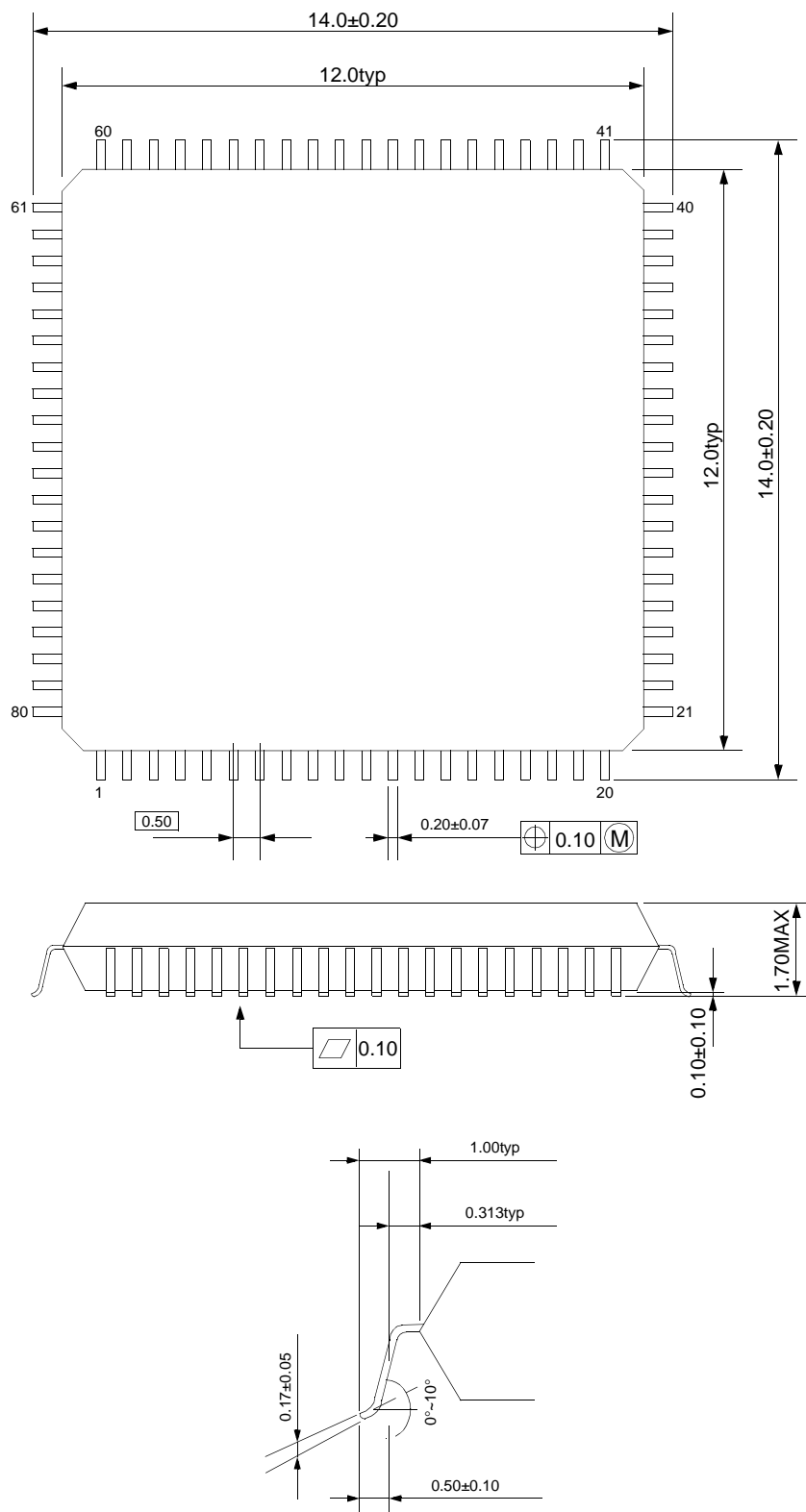


Figure 8-1 Package Dimension

9 Parts Layout

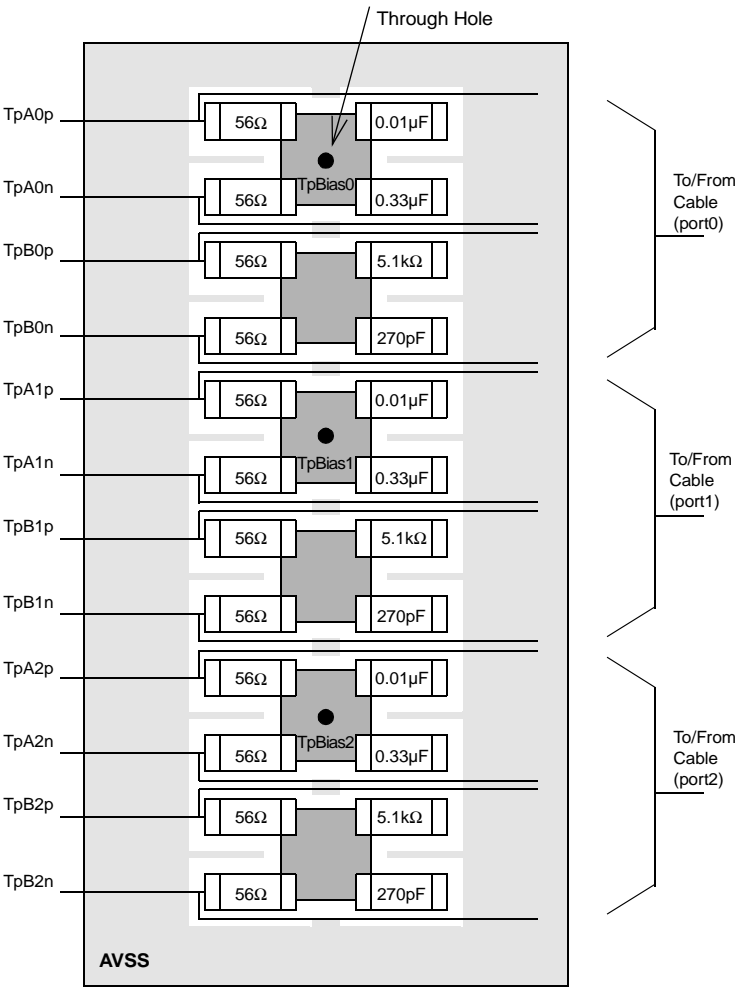


Figure 9-1 Parts Layout

10 Pin interchange

10-1 Pin interchange with MD8404

MD8405E becomes the same pin arrangement about PHY/Link I/F, the cable I/F, Clock circuit part. But, the establishment pin of a part to function newly with MD8405E and which is added is different. MD8405E works on the following condition when MD8405E is mounted by the pin arrangement of MD8404.

Pin No.	MD8404	MD8405E	Operation
61	DVSS	Disable2	It works as Initial value= "0" of the Disable bit of the port 2.
62	DVSS	Disable1	It works as Initial value= "0" of the Disable bit of the port 1.
64	DVSS	Disable0	It works as Initial value= "0" of the Disable bit of the port 0.
65	DVSS	S200	S400 operation
69	DVSS	En_Accel	It works as Initial value= "0" of the Enab_Accel bit.
70	DVSS	En_Multi	It works as Initial value= "0" of the Enab_Multi bit.
71	DVSS	SR	P1394a Draft Ver1.3 conformity. It works in Suspend/Resume function off.
78	CMC/LINKON	LinkOn	Only the output of LinkOn.
3	DVSS	CMC	It works as Initial value= "0" of the Contender bit.

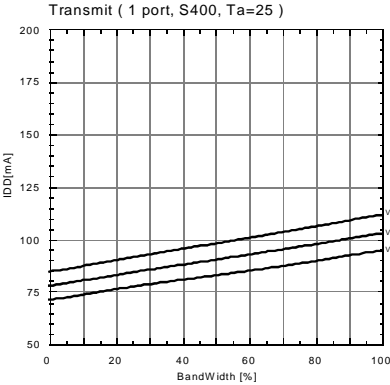
Table 10-1 MD8405E Operation

10-2 Pin interchange with MD8405B/MD8405D

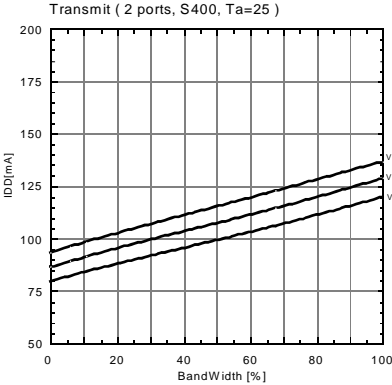
MD8405E becomes the pin arrangement which is the same as MD8405B/MD8405D.

11 Appendix A Consumption current in the transmit / reception conditions (typical)

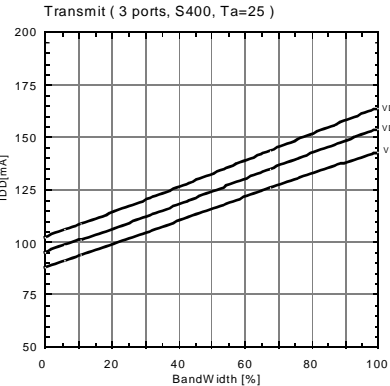
1) Transmit (1 port, S400)



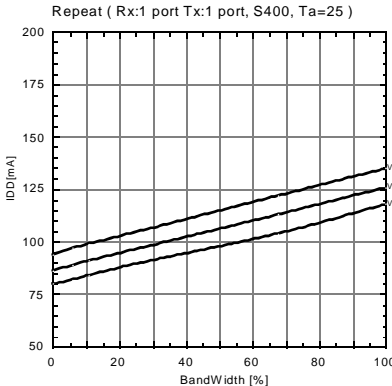
2) Transmit (2 ports, S400)



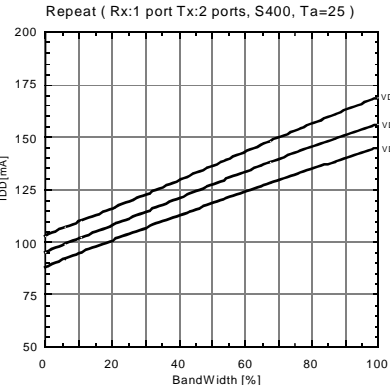
3) Transmit (3 ports, S400)



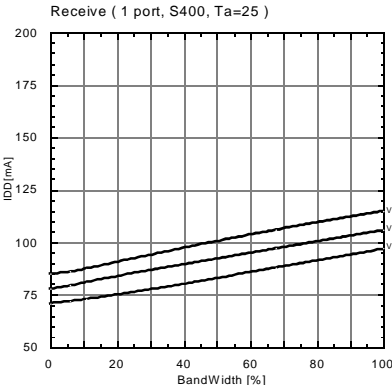
4) Repeat (Rx: 1 port, Tx: 1 port, S400)



5) Repeat (RX: 1 port, Tx: 2 ports S400)



6) Receive (1 port, S400)



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