TRUE TIME AVERAGE OVER VARYING PERIODS

Versatile Time-Independent Averaging Circuit Uses IC DAC

by C. Barker

The circuit described here[1] obtains the true time average of a varying input signal over a wide range of differing periods. It was designed for use in a system for the control of plastic film-thickness, but the technique has many other potential uses. A few that come to mind include: measurements of average pressure- or volume-per-stroke in pumps and bellows, measurements of true-rms over varying periods, measurement of quasi-electrometer currents without high-value resistors, and normalized integration of one-shot phenomena.

The simple, yet effective, circuit shown here uses a standard integrating circuit and an AD7521* monolithic multiplying D/A converter in the feedback path of an operational amplifier to obtain a gain inversely-proportional to time, as determined by the count of a stream of pulses from a clock circuit (Fig. 1).

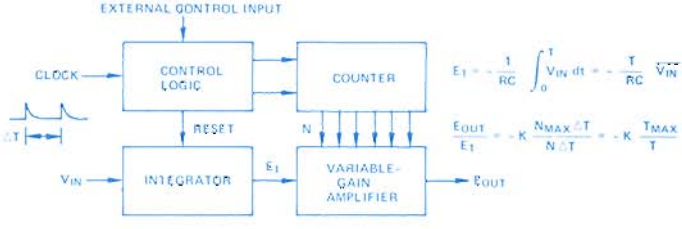

Figure 1. Block diagram of the averager. $T_{max} = N_{max}\Delta T$ is the time required for the counter to reach full-scale.

The integrator output over a time interval, T, is inherently equal to the product of the average value of the input and the ratio of T to the characteristic time, RC. The gain of the variable-gain amplifier is inversely proportional to the number of pulses, and hence to the elapsed time $N\Delta T$ (which is equal to T at each instant the count is updated). The output is

$$E_O = \left[\frac{T}{RC}\,\overline{V_{IN}}\right]\left[\frac{KT_{max}}{T}\right] = \left[K\,\frac{T_{max}}{RC}\right]\overline{V_{IN}} \qquad (1)$$

E_O depends only on $\overline{V_{IN}}$ and is essentially independent of T.

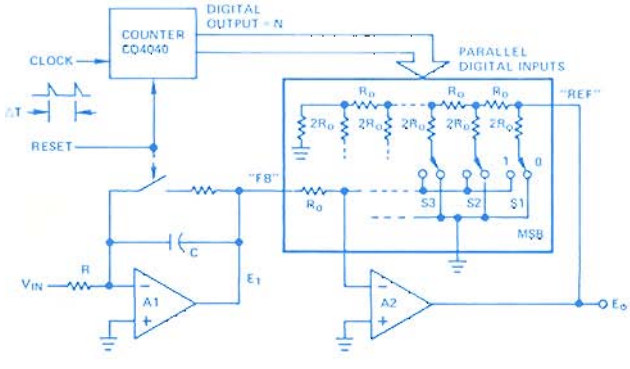

Figure 2. Simplified circuit diagram

The variable-gain amplifier (Figure 2) consists of a D/A converter in the feedback path of an operational amplifier. The converter used here is the 12-bit AD7521, which consists of an R-2R ladder attenuator, a set of switches, and a "feedback" resistor, which tracks the resistances in the ladder network. A set of binary-weighted currents flows through the "2R" resistors, either to ground, or to a summing bus, as determined by the position of the CMOS switches, operated by the logic inputs from the counter. For example, if the input to S1 is "1", and all the other switches are "0", a current equal to $\frac{1}{2}(E_O/R_O)$ flows through the summing node to match the input current $(-E_1/R_O)$, and the output voltage E_O must be $-2E_1$. If S1 & S2 are "1", with everything else "0", the feedback current is $(3/4)(E_O/R_O)$, and the output voltage, E_O, must be $-(4/3)E_1$.

Since the above two examples occur when the count is $N_{max}/2$ and $(3/4)N_{max}$, the times at which they occur are $T_{max}/2$ and $(3/4)T_{max}$. Similarly, for any other values of N, the gain of amplifier circuit A2 is *inversely* proportional to N (and thus to $T = N\Delta T$). Since the output of the integrator is *directly* proportional to T and the average value of V_{IN} for the interval, T, their product, E_O, is proportional to $\overline{V_{IN}}$ only (Eq. 1).

The integrator must not be allowed to saturate for the worst-case time (T_{max}) and input voltage ($\overline{V_{IN}}_{max}$). At T_{max}, the gain of the A2 circuit is $1/(1 - 2^{-n}) \cong 1$; at that time, the integrator output should be less than or equal to an arbitrary limiting value, V_{LIM}, below saturation:

$$|E_1| = \frac{1}{RC}\,\overline{V_{IN}}\,T_{max} \leq V_{LIM} \qquad (2)$$

Therefore,

$$RC \geq T_{max}\left[\frac{\overline{V_{IN}}_{max}}{V_{LIM}}\right] \qquad (3)$$

$\overline{V_{IN}}_{max}$ can actually be greater than V_{LIM}, if RC is scaled properly. Since T_{max} is also equal to $N_{max}\Delta T$, and $N_{max} = 2^n$ (= 4096 for the AD7521), the clock frequency, $1/\Delta T$, is $2^n/T_{max}$.

A moderate filter capacitance between the output and the summing-point of A2 will reduce switching transients as the gain is switched. A sample-hold following A2 will reduce "ripple" due to the continuing integration between counts (this ripple becomes very small as T_{max} is approached); the new sample should be taken immediately after switching-transients die out. Integrator drift due to offset and bias current in A1 will show up as output offset, reducible by amplifier choice and/or offset trimming with grounded input. Scale-factor errors can be trimmed by adjusting R. Overall accuracy, which improves towards the 0.1% level as T approaches T_{max}, can be well within 1% for $T > 0.1T_{max}$.

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[1] The circuit described here was developed by the author at Industrial Nucleonics Corporation, Columbus OH 43202.

*Use the reply card to request technical data on the AD7520 & AD7521.